

5 MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

- Like JFET, it has a source, Drain and Gate.
- It is also called IGFET (Insulated Gate FET) because gate terminal is insulated from channel. Therefore it has extremely high input resistance.

5.1 Types of MOSFET

It has two types

Ø Depletion mode MOSFET

ü N-channel

ü P-channel

Ø Enhancement mode MOSFET

ü N-channel

ü P-channel

The enhancement-type MOSFET is usually referred to as an E-MOSFET, and the depletion type, a D-MOSFET. The drain current in a MOSFET is controlled by the gate-source voltage V_{GS} .

5.2 Depletion mode-MOSFET [D-MOSFET]

In depletion mode of operation the bias voltage on the gate reduces the number of charge carriers in the channel and therefore reduces the drain current I_D . It operates in both depletion mode and enhancement mode.

5.2.1 Symbol

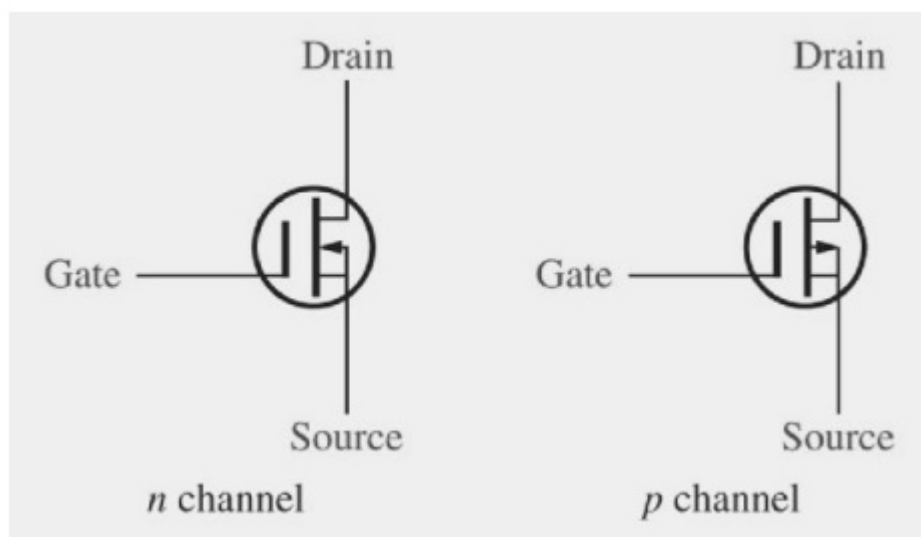


Figure 3.5 D-MOSFET symbol for n-channel and p-channel

5.2.2 Construction

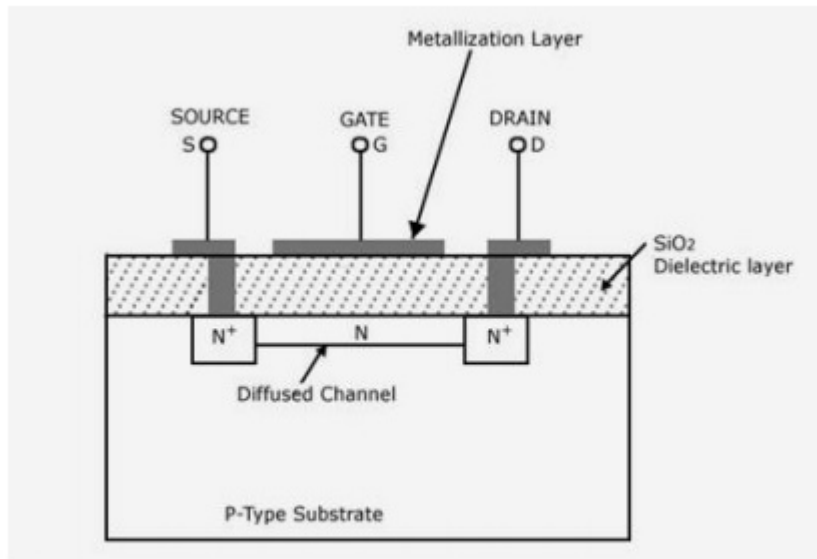


Figure 3.6 structure of n-channel D-MOSFET

Figure 3.6 structure of n-channel D-MOSFET

- It consists of lightly doped p-type substrate in which two highly doped n-regions are diffused.
- The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel. The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide (SiO₂) layer. SiO₂ is a particular type of insulator referred to as a dielectric that sets up opposing (as revealed by the prefix di-) electric fields within the dielectric when exposed to an externally applied field.
- Then the thin layer of metal aluminium is formed over the SiO₂ layer. This metal covers the entire channel region and it forms the gate(G).

5.2.3 Operation of N-channel D-MOSFET

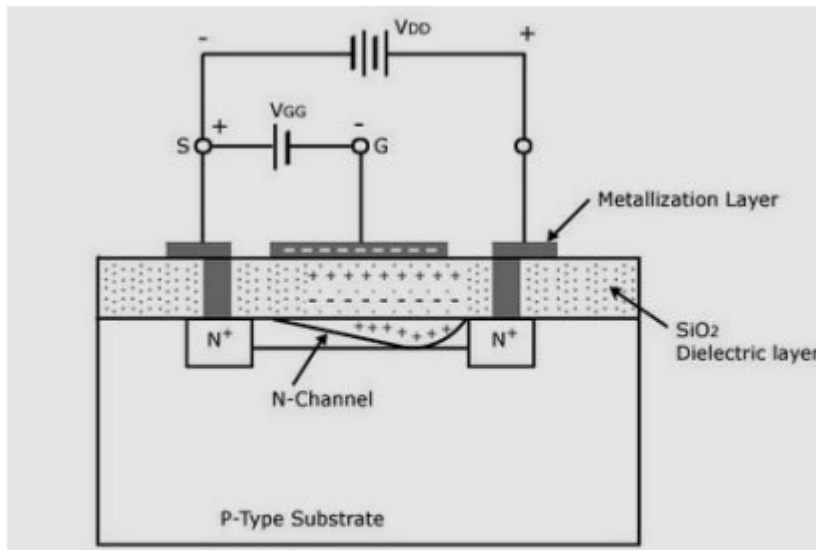


Figure 3.7 n-channel D-MOSFET under applied bias

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Case (i) “when V_{GS} is increased from zero”

- Here N-base (Drain) is connected to positive supply. It act as a reverse bias. Due to this, depletion region gets increases.
- Free electron from n-channel are attracted towards positive potential of drain terminal. This establishes current through channel flows from drain to source and denoted as I_{DSS} .

Pinch off voltage

The pinch off voltage is the voltage at which the junction is depleted of charge carriers.

Case (ii) “when V_{DS} is increased from zero”

- The negative charge on gate repels conduction electrons from the channel and attract holes from the p-type substrate.
- Due to this electron-hole recombination occurs and reduce the number of free electrons in the channel available for conduction, reducing Drain current (I_D).
- When negative voltage of V_{GS} is increased the pinch off voltage decreased. When V_{GS} is further increased the channel is fully depleted and no current flows through it.
- The negative voltage on the gate deplete the channel, the device is referred to as a depletion MOSFET.

Case (iii) “when and is increased from zero”

- Due to positive ,ad ditional electrons are induced in the channel. Hence the conductivity of the channel increase s and current (I_D) increases.
- This mode of operation is called as a enhancement mode and it is also called as dual mode MOSFET or ON-MOS FET.

5.2.4 Characteristics curve

Two types

- Drain characteristics
- Transfer characteristics

D-MOSFET's are biased to operate in two modes :depletion or enhancement mode.

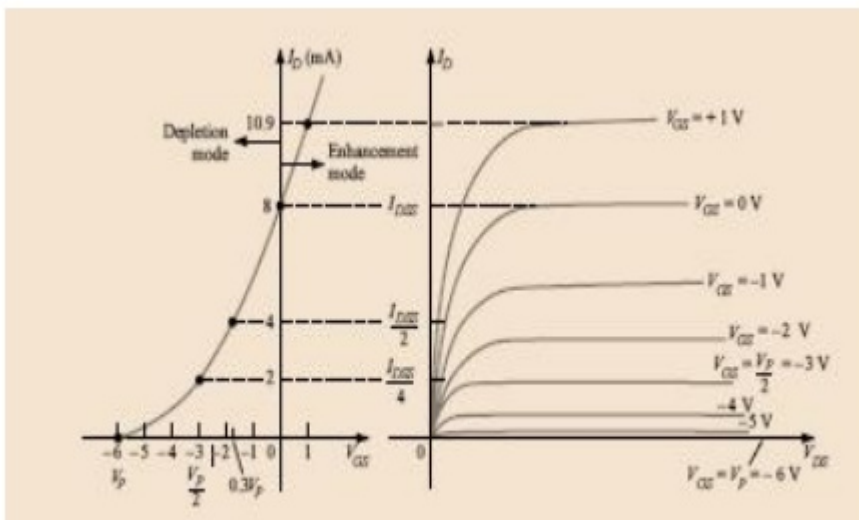


Figure 3.8 Drain and transfer characteristics

Figure 3.8 Drain and transfer characteristics

5.3 ENHANCEMENT- M ODE MOSFET [E-MOSFET]

In this mode bias on th e gate increases the number of charge carriers in the channel and increases the drain current (I_D).

It operates only in the enhancement mode and has no depletion mo de of operation.It has no physical channel.

5.3.1 Symbol of E-MOSFET

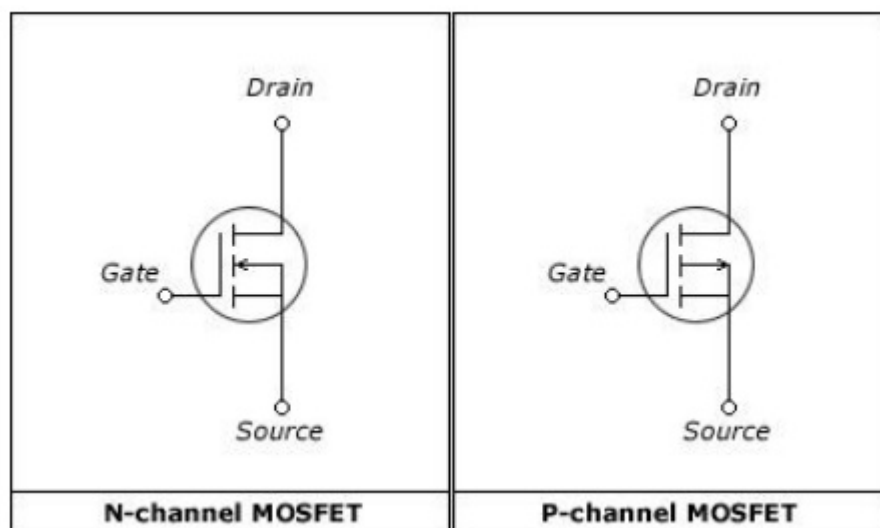


Figure 3.9 symbol of n-channel and p-channel E-MOSFET

5.3.2 Basic Construction

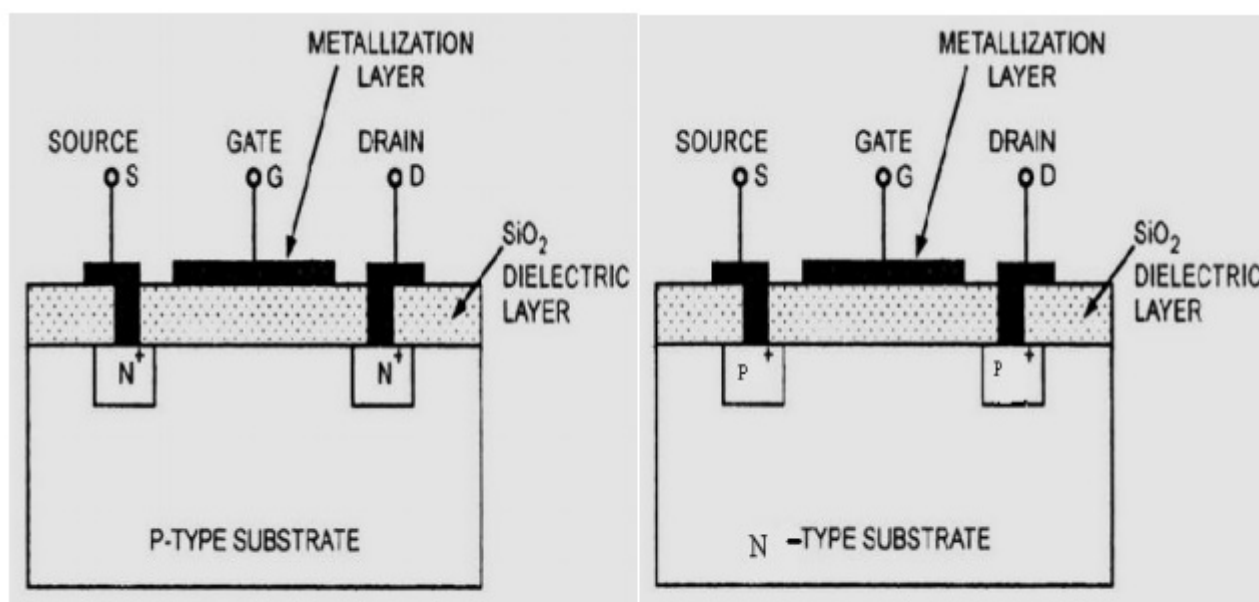


Figure 3.10 Construction of n-channel and p-channel E-MOSFET

Figure 3.10 Construction of n-channel and p-channel E-MOSFET

In the basic construction of the n-channel enhancement-type MOSFET, a slab of p-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, while in other cases a fourth lead is made available for external control of its potential level.

The SiO₂ layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material.

In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

5.3.3 Operation

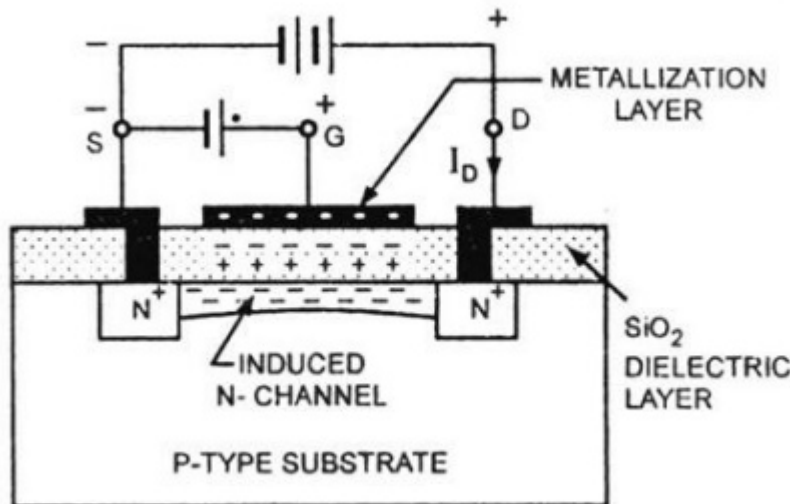


Figure 3. 11 N-channel E-MOSFET under applied bias

- If V_{GS} is set at 0 V and a voltage applied between the drain and source of the device, the absence of an n-channel (with its generous number of free carriers) will result in a current of effectively zero amperes—quite different from the depletion-type MOSFET and JFET where $I_D = I_{DSS}$.
- It is not sufficient to have a large accumulation of carriers (electrons) at the drain and source (due to the n-doped regions) if a path fails to exist between the two. With V_{DS} some positive voltage, V_{GS} at 0 V, and terminal SS directly connected to the source, there are in fact two reverse-biased p-n junctions between the n-doped regions and the p-substrate to oppose any significant flow between drain and source.
- When both V_{DS} and V_{GS} have been set at some positive voltage greater than 0 V, establishing the drain and gate at a positive potential with respect to the source. The positive potential at the gate will pressure the holes (since like charges repel) in the p-substrate along the edge of the SiO_2 layer to leave the area and enter deeper regions of the p-substrate.
- As V_{GS} is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if

we hold V_{GS} constant and increase the level of V_{DS} , the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET.

- The conductivity of the channel is enhanced by the positive bias voltage on the gate, the

device is known as enhancement MOSFET. E-MOSFET's are normally called as "OFF – MOSFET"

5.3.4 Characteristics of E-MOSFET

Drain characteristics curve

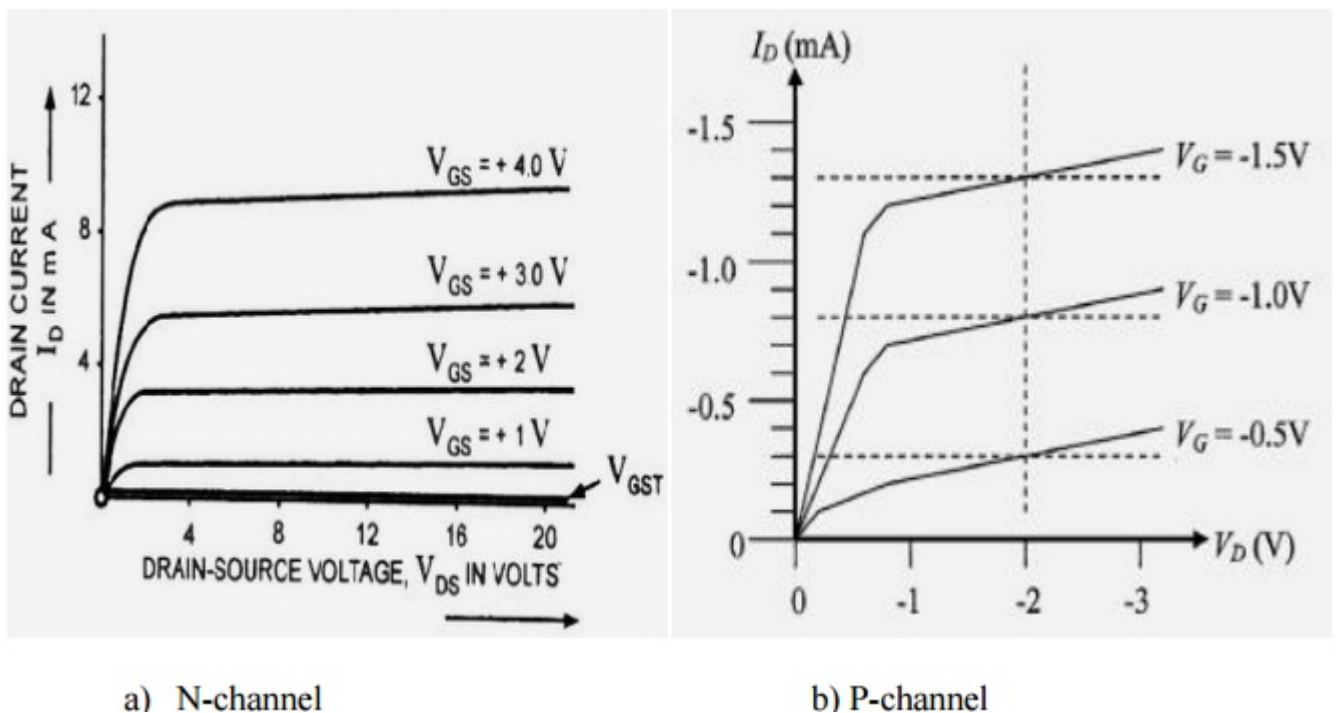


Figure 3.12 Drain characteristics curve a) n-channel b) p-channel

Transfer characteristics curve

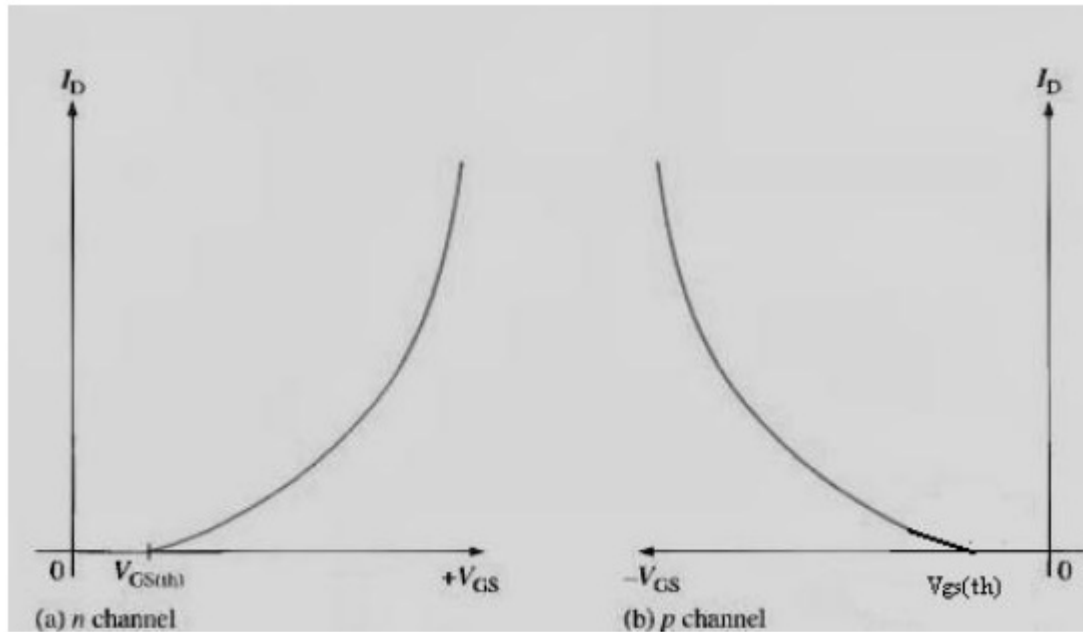


Figure 3.13 T transfer characteristics curve a) n-channel b) p-channel

For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_{GS(th)})^2$$

Where, k-constant depends upon type of MOSFET.

Again, it is the squared term that results in the nonlinear (curved) relationship between I_D and V_{GS} . The k term is a constant that is a function of the construction of the device. The value of k can be determined from the following equation where $I_{D(on)}$ and $V_{GS(on)}$ are the values for each at a particular point on the characteristics of the device.

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(th)})^2}$$

5.4 Applications:

1. Used in digital VLSI circuits
2. Used as amplifiers
3. Used in computer memories

4. Used as oscillator and in communication.

6 CHANNEL LENGTH MODULATION

One of several short-channel effects in MOSFET scaling, channel length modulation (CLM) is a shortening of the length of the inverted channel region with increase in drain bias for large drain biases. The result of CLM is an increase in current with drain bias and a reduction of output resistance. Channel length modulation occurs in all field effect transistors, not just MOSFETs.

To understand the effect, first the notion of pinch-off of the channel is introduced. The channel is formed by attraction of carriers to the gate, and the current drawn through the channel is nearly a constant independent of drain voltage in saturation mode. However, near the drain, the gate and drain jointly determine the electric field pattern. Instead of flowing in a channel, beyond the pinch-off point the carriers flow in a subsurface pattern made possible because the drain and the gate both control the current. In the figure at the right, the channel is indicated by a dashed line and becomes weaker as the drain is approached, leaving a gap of uninverted silicon between the end of the formed inversion layer and the drain (the pinch-off region).

As the drain voltage increases, its control over the current extends further toward the source, so the uninverted region expands toward the source, shortening the length of the channel region, the effect called channel-length modulation. Because resistance is proportional to length, shortening the channel decreases its resistance, causing an increase in current with increase in drain bias for a MOSFET operating in saturation. The effect is more pronounced the shorter the source-to-drain separation, the deeper the drain junction, and the thicker the oxide insulator.

In bipolar devices a similar increase in current is seen with increased collector voltage due to base-narrowing, known as the early effect. The similarity in effect upon the current has led to use of the term "Early effect" for MOSFETs as well, as an alternative name for "channel-length modulation".

Channel length modulation: the channel pinch-off point moves slightly away from drain as V_{DS} increases. The effective channel length L_{eff} reduces with V_{DS} . Electrons travel to pinch-off point will be swept to drain by electric field.

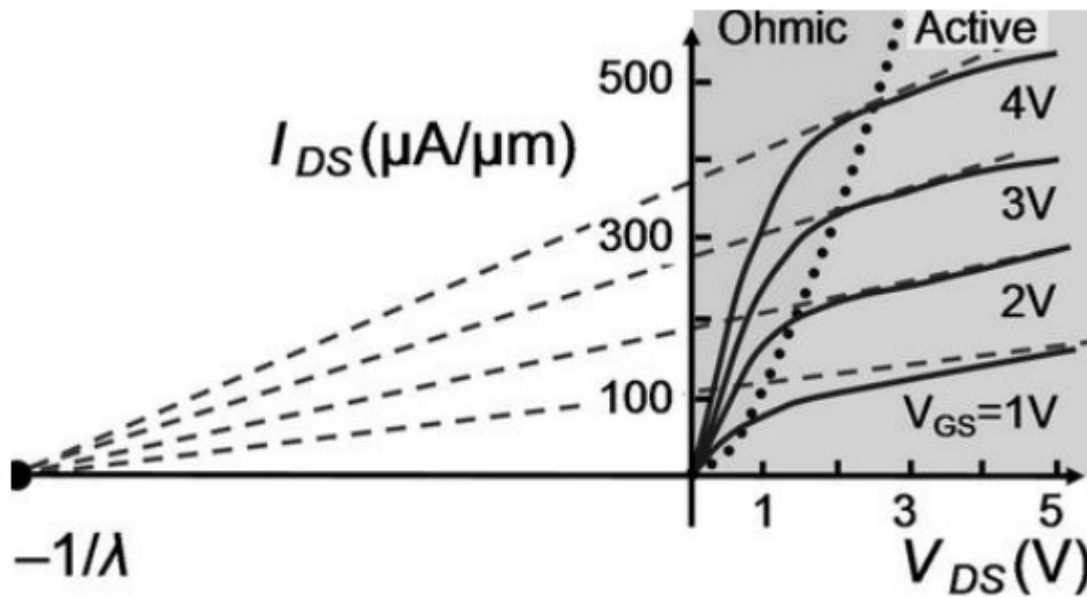


Figure 3.14 Effect of channel length modulation due to the non-zero slope in saturation region, resulting in a finite output resistance

For an N-channel device the slope of the curve in the saturation region can be expressed by using the drain current I_D given by

The output resistance can be determined at the Q-point by

The output resistance is an important factor in the analysis of small signal equivalent circuit of MOSFET.

7 THRESHOLD VOLTAGE

The threshold voltage, commonly abbreviated as V_{th} or $V_{GS(th)}$, of a field-effect transistor (FET) is the minimum gate-to-source voltage differential that is needed to create a conducting path between the source and drain terminals.

At gate-to-source voltages above the threshold voltage ($V_{GS} > V_{th}$) but still below saturation (less than "fully on", $(V_{GS} - V_{th}) > V_{DS}$), the transistor is in its 'linear region', also known as ohmic mode, where it behaves like a voltage-controlled variable resistor.

In n-channel enhancement-mode devices, a conductive channel does not exist naturally within the transistor, and a positive gate-to-source voltage is necessary to create one. The positive voltage

attracts free-floating electrons within the body towards the gate, forming a conductive channel. But first, enough electrons must be attracted near the gate to counter the dopant ions added to the body of the FET; this forms a region with no mobile carriers called a depletion region, and the voltage at which this occurs is the threshold voltage of the FET. Further gate-to-source voltage increase will attract even more electrons towards the gate which are able to create a conductive channel from source to drain; this process is called inversion.

In contrast, n-channel depletion-mode devices have a conductive channel naturally existing within the transistor. Accordingly, the term 'threshold voltage' does not readily apply to turn such devices 'on', but is used instead to denote the voltage level at which the channel is wide enough to allow electrons to flow easily. This ease-of-flow threshold also applies to p-channel depletion-mode devices, in which a positive voltage from gate to body/source creates a depletion layer by forcing the positively charged holes away from the gate-insulator/semiconductor interface, leaving exposed a carrier-free region of immobile, negatively charged acceptor ions.

8 DUAL GATE MOSFETS

MOSFET can be provided with two gates. Both gates can be used independently to control the drain current or the channel resistance. Dual gate MOSFET are normally of the n-channel depletion type. The dual-gate MOSFET has a tetrode configuration, where both gates control the current in the device.

8.1 Symbol and Construction

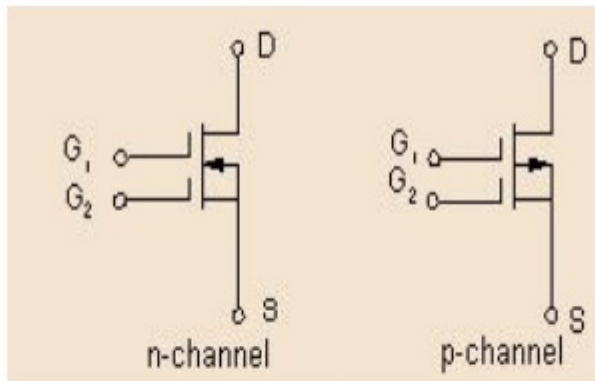


Figure 3.15 Symbol of dual gate MOSFET

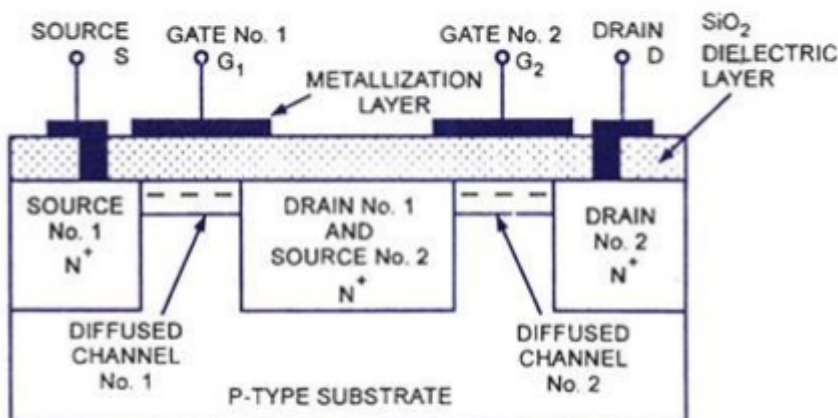


Figure 3.16 N-channel Dual gate MOSFET

The output signal of the dual gate MOSFET is approximately proportional to the PRODUCT of the input voltages:

8.2 Applications :

- This makes this device suitable for applications where the multiplication of signals is required. E.g. modulation, mixing, demodulation, automatic gain control etc.
- It is also used as signal switch
- One gate serves as input for the signal to be amplified or transferred, the other as the control input. The advantage is, that the signal and the control voltage are fully separated.

9 FINFET

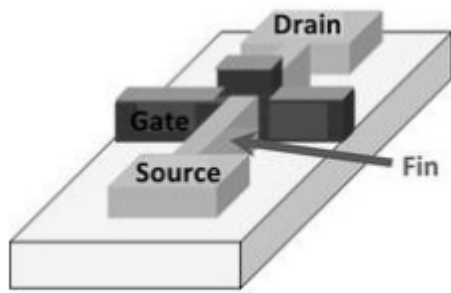


Figure 3.17 FinFET structure

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The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the body of the device. The thickness of the fin (measured in the direction from source to drain) determines the effective channel length of the device.

The "Omega FinFET" design is named after the similarity between the Greek letter omega (Ω) and the shape in which the gate wraps around the source/drain structure. It has a gate delay of just 0.39 picosecond (ps) for the N-type transistor and 0.88 ps for the P-type. Fin FET can also have two electrically independent gates, which gives circuit designers more flexibility to design with efficient, low-power gates.

Applications:

The double gate FinFETs which are driven independently are used to construct low power logic gates, single transistor mixers and SRAMs

FIELD EFFECT TRANSISTORS

1. Define FET?

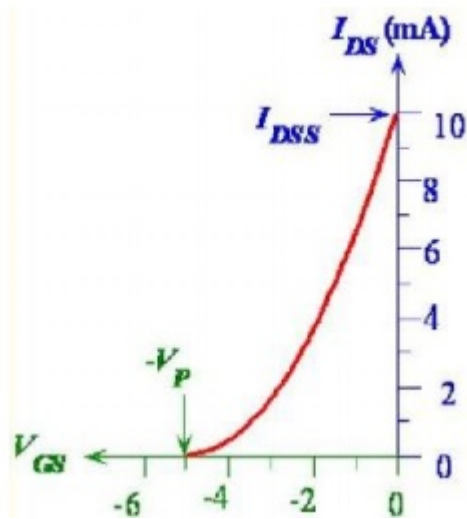
A field effect transistor (FET) is a three terminal semiconductor device which can be used as an amplifier or switch. The three terminals are Drain (D), Source (S), and Gate (G).

2. Define channel?

It is a bar like structure which determines the type of FET. Different types of N channel are FET and P channel FET.

3. Draw the transfer characteristic for n-channel depletion type MOSFET?

Transfer characteristic:



4. What do you understand by pinch off voltage and out of voltage?

As the reverse bias is further increased, the effective width of the channel decreases, the depletion region or the space charge region widens, reaching further into the channel and restricting the passage of electrons from the source to drain. Finally at a certain gate to source voltage $V_{GS} = V_P$.

5. Why FET is called as “voltage operated device”?

In FET the output current, I_D is controlled by the voltage applied between gate and source (V_{GS}). Therefore FET is said to be voltage controlled device.

6. Which MOSFET is called as Normally ON MOSFET and NORMALLY OFF MOSFET? Why?

This is just one type of MOSFET, called 'normally -off' because it is only the application of a positive gate voltage above the critical voltage which allows it to pass current between source and drain. Another type of MOSFET is the 'normally-on', which has a conductive channel of less heavily doped n-type material between the source and drain electrodes.

7. Compare BJT and MOSFET

S.No	BJT	MOSFET
1	CB,CE,CC configurations	CS,CG,CD configurations
2	Less input resistance compared to JFET	Very high input resistance
3	Input output relation is linear	Input output relation is non-linear
4	Gain bandwidth product is high	Gain bandwidth product is low
5	Thermal noise is more	Thermal noise is less
6	Thermal stability is less	Thermal stability is more
7	Bigger size than MOSFET	Smaller size

BJT

- 1 CB,CE,CC configurations
- 2 Less input resistance compared to JFET
- 3 Input output relation is linear
- 4 Gain bandwidth product is high
- 5 Thermal noise is more
- 6 Thermal stability is less
- 7 Bigger size than MOSFET

MOSFET

- 1 CS,CG,CD configurations
- 2 Very high input resistance
- 3 Input output relation is non-linear
- 4 Gain bandwidth product is low
- 5 Thermal noise is less
- 6 Thermal stability is more
- 7 Smaller size