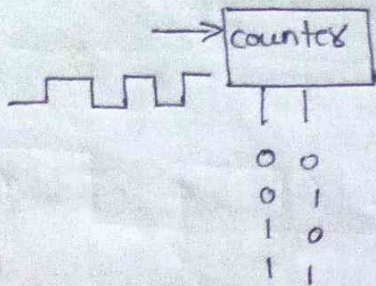


Unit-IV

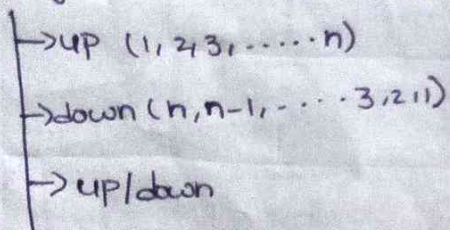
Counter:-

The counter counts the no. of times the specific event has been occurred.

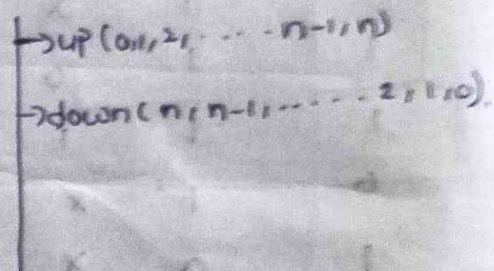


Types of counters

Asynchronous/Ripple counter



Synchronous

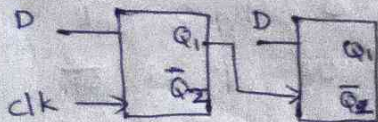


n-bit counter requires n flts.

Difference b/w Asynchronous & Synchronous:-

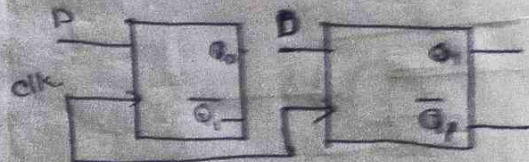
Asynchronous

Flipflops are connected in such a way that the output of the first flipflop drives the clock of the next flipflop.



Synchronous

There is no connection b/w output of first flipflop and clock of next flipflop.



→ Flipflops are not clocked simultaneously. → Flipflops are clocked simultaneously.

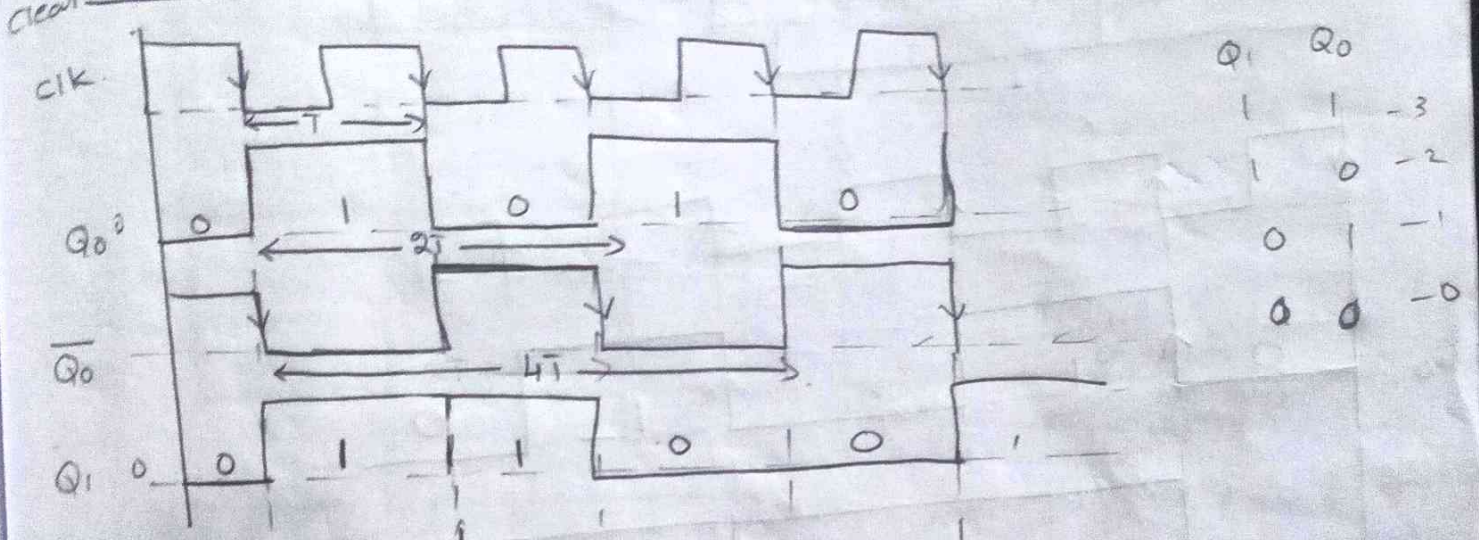
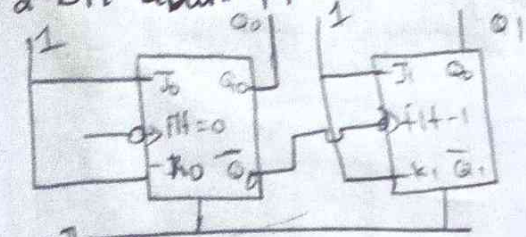
→ Circuit is simple for more no. of states.

→ Circuit becomes complicated as no. of states increases.

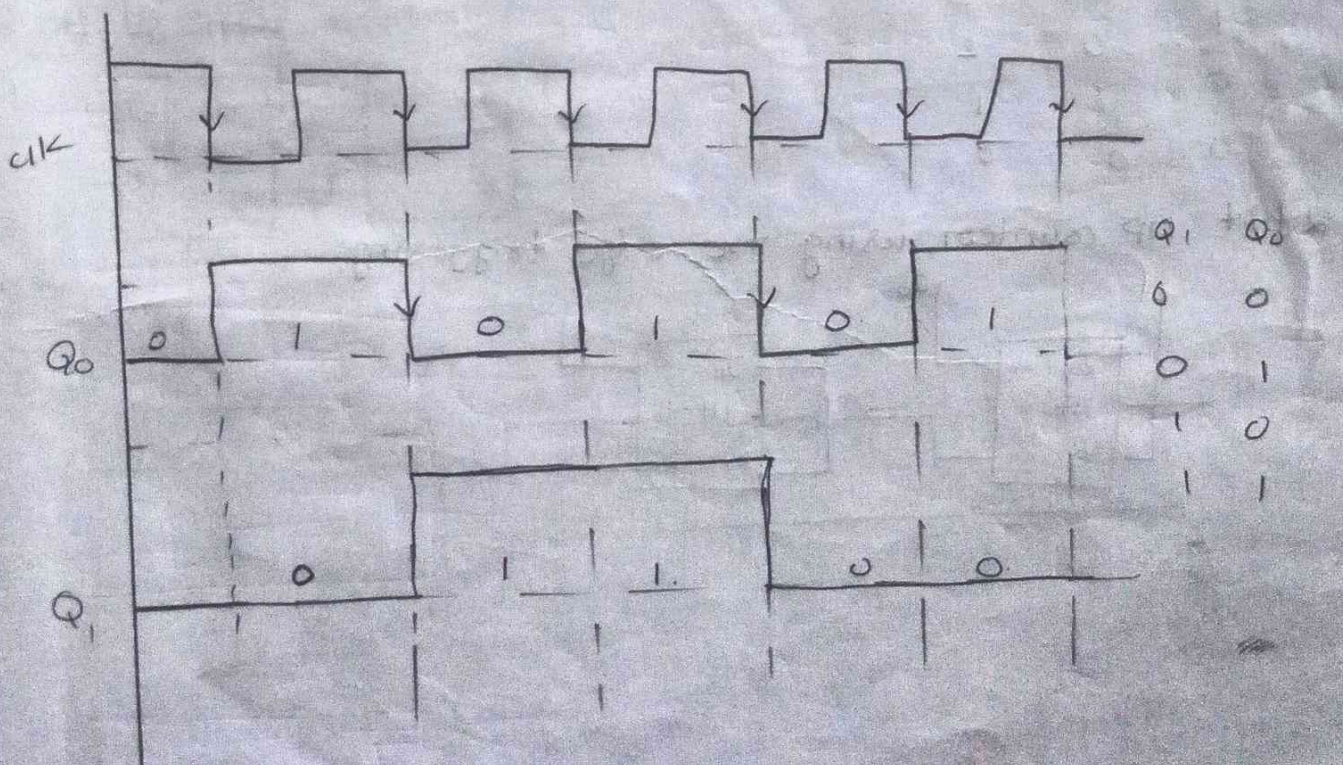
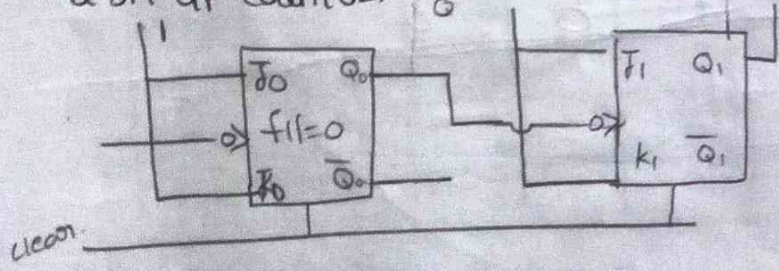
→ Speed is slow as clock is propagated through no. of states.

→ Speed is high as clock is given at the same time.

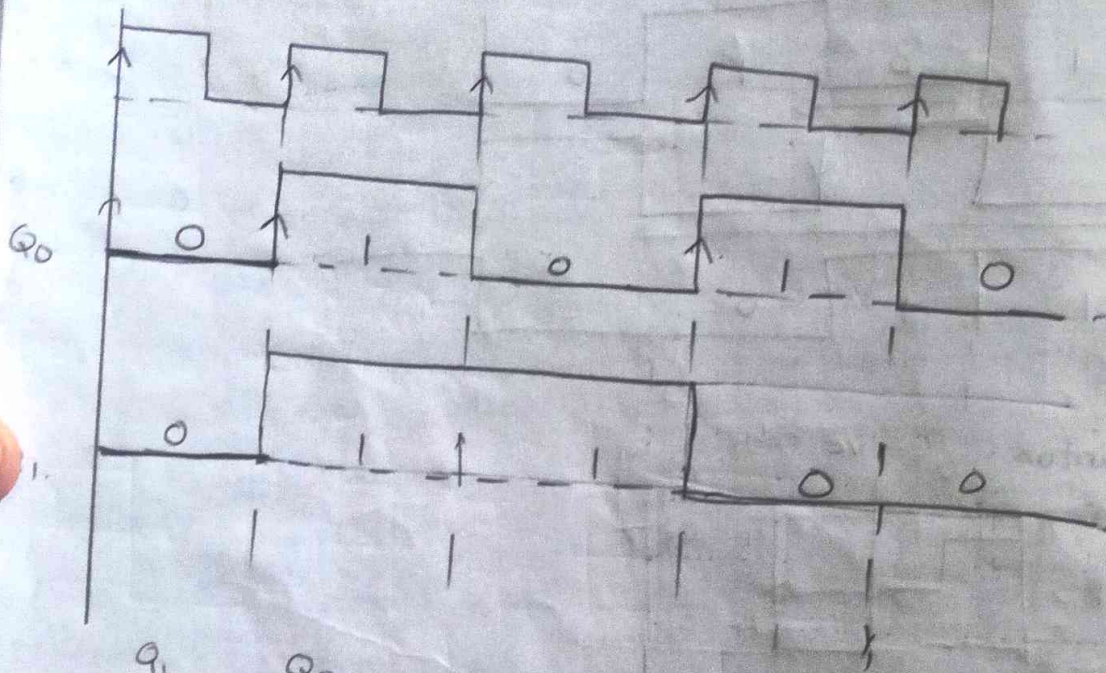
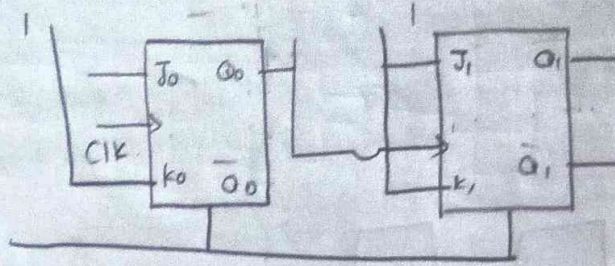
2-bit downRipple counter:- (using -ve edge triggering).



2-bit UP counter:- (-ve edge)

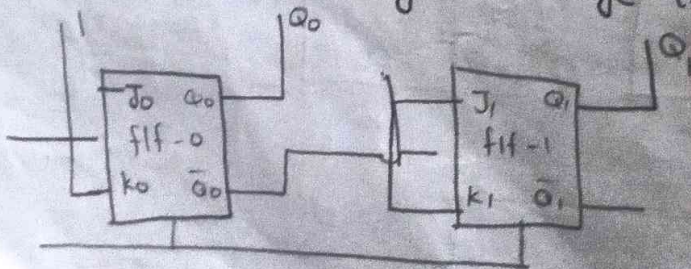


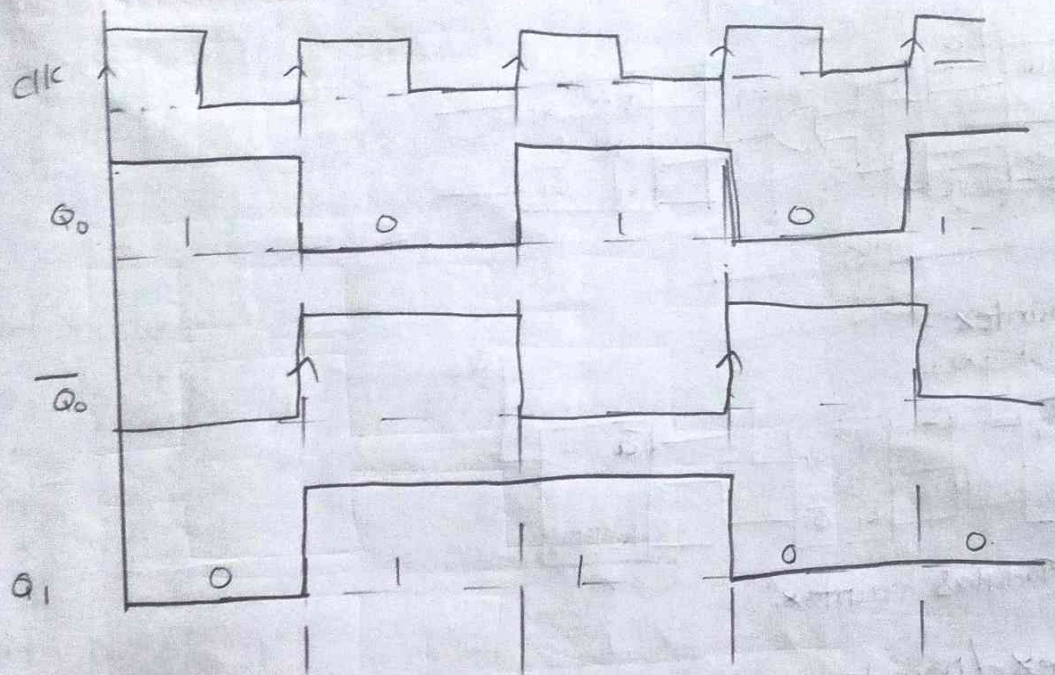
2-bit ^{down} counter using +ve edge triggering.



Q_1	Q_0	
1	1	3
1	0	2
0	1	1
0	0	0

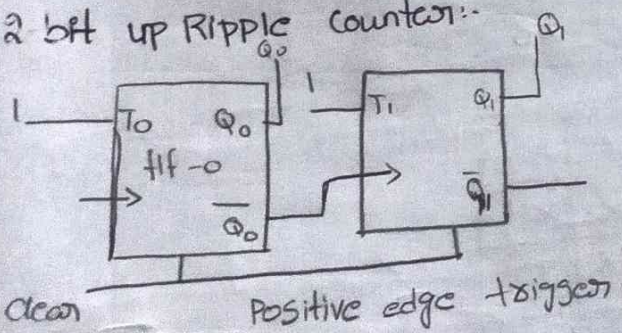
2-bit up counter using +ve edge triggering.



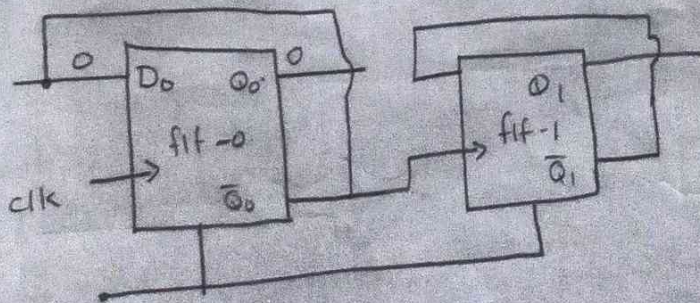


Triggering	Counter	clk.
Negative	UP	Q ₀
Negative	Down.	Q ₀
Positive	UP	Q ₀
Positive	Down	Q ₀

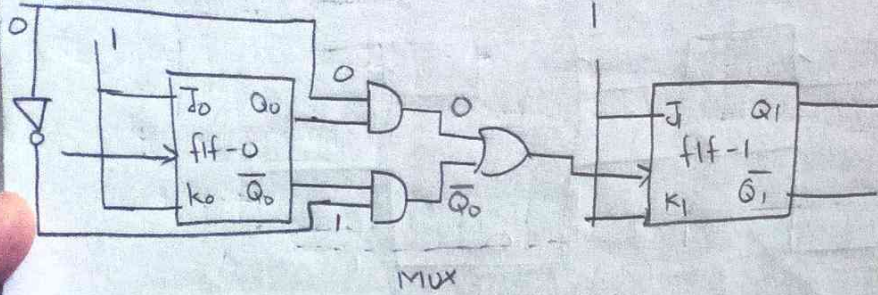
2 bit up Ripple counter:-



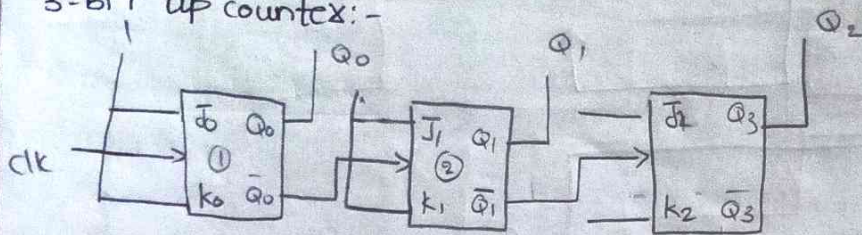
D-flip:-



VLS UP and down Counter:

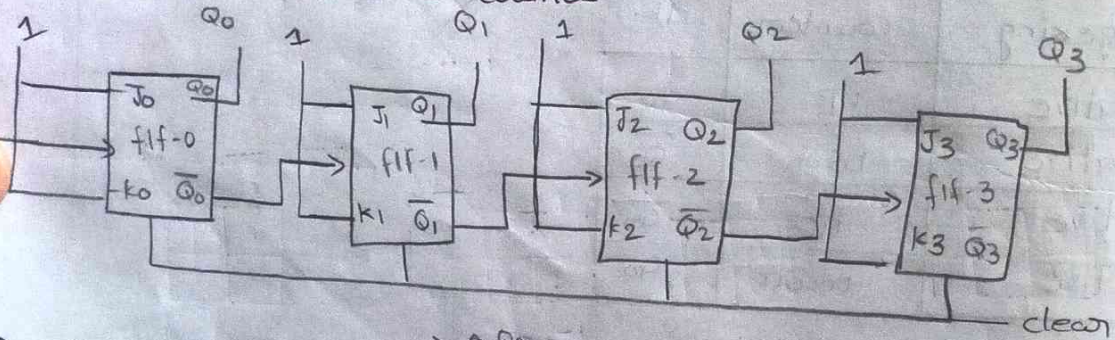


3-bit up counter:-



Full modulus counter.

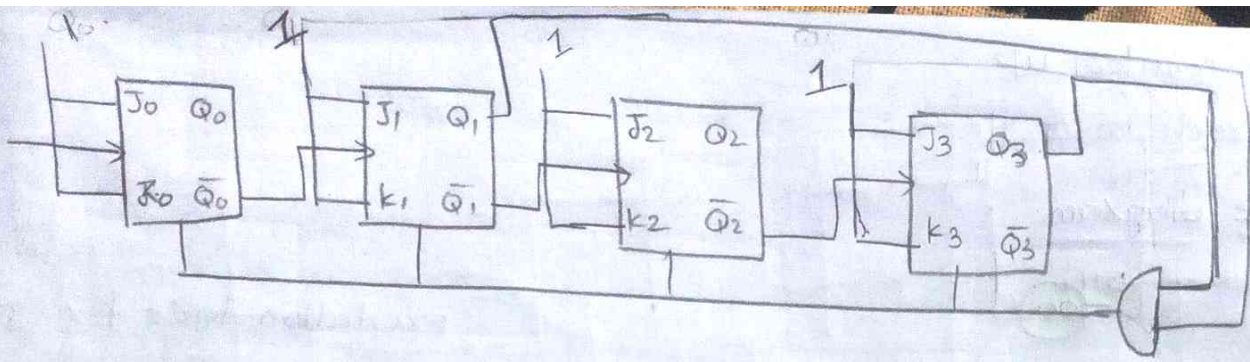
MOD 10 counter / Decade counter.



Q ₃	Q ₂	Q ₁	Q ₀	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	X
1	1	0	0	X
1	1	0	1	X
1	1	1	0	X
1	1	1	1	X

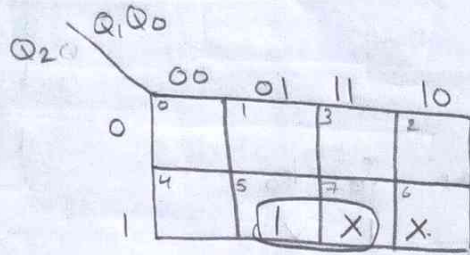
Q ₃ Q ₂	Q ₁ Q ₀	00	01	11	10
00					
01					
11		X	X	X	X
10				X	1

$$F = Q_3 Q_1$$

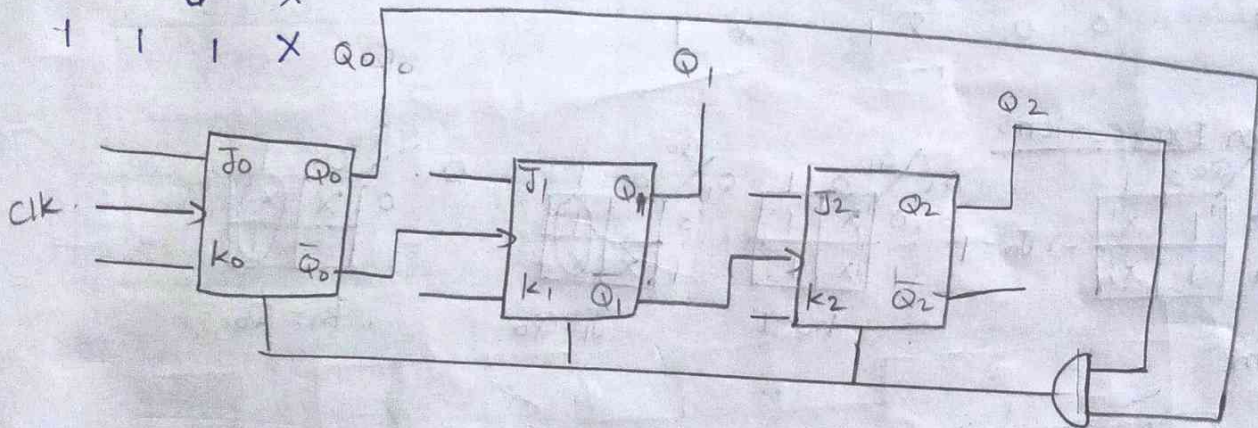


Mod-5 counter:-

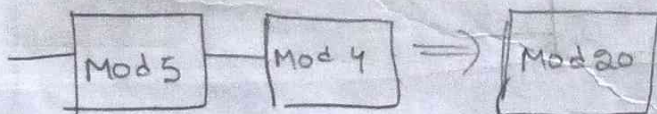
Q_2	Q_1	Q_0	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	X
1	1	1	X



$$F = Q_2 Q_0$$



cascading



Design of Synchronous counters.

1) Find the Required no. of flipflops.

2) Draw the state diagram

3) Select the flipflop and draw excitation table.

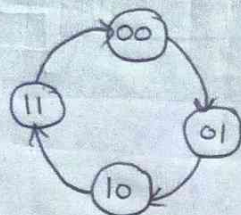
4) Find minimal expression for the excitation each flipflop.

5) Draw the logic diagram.

2 bit counter up.

1) Required no. of flip $\rightarrow 2$

2) State diagram:-



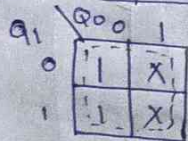
3) Excitation table:

Present state		Next state					
Q_1	Q_0	Q_1^+	Q_0^+	J_1	k_1	J_0	k_0
0	0	0	1	0	x	1	x
0	1	1	0	1	x	x	1
1	0	1	1	x	0	1	x
1	1	0	0	x	1	x	1

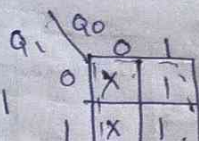
Excitation table for $\bar{Q}$

Q_n	Q_{n+1}	J	k
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

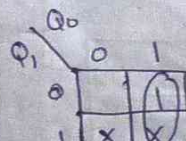
Minimum Expressions



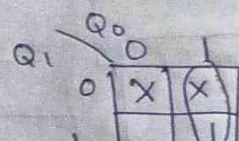
$$\Rightarrow J_0 = 1$$



$$k_0 = 1$$

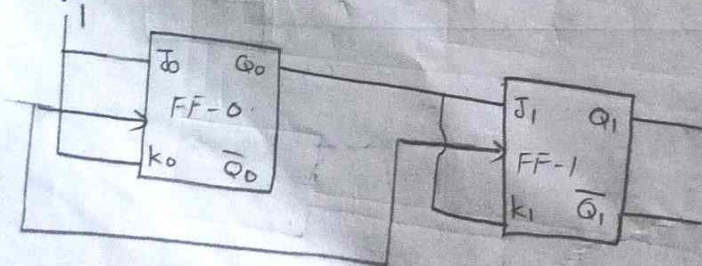


$$J_1 = Q_0$$



$$k_1 = Q_0$$

Diagram:-

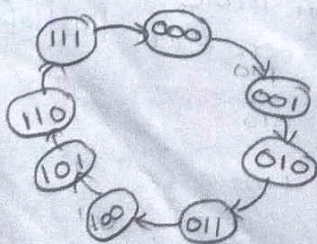


3-bit up counter.

1) Required flipflop $\rightarrow 3$.

$$2^3 \rightarrow 8$$

2) state diagram:-



3) Excitation table:

PS			NS			i/ps.					
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	$\bar{J}_2$	K_2	$\bar{J}_1$	K_1	$\bar{J}_0$	K_0
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	0	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	1	1	0	x	0	1	x	x	1
1	1	0	1	1	1	x	0	x	0	1	x
1	1	1	0	0	0	x	1	x	1	x	1

Minimum Expressions:-

Q_2 $Q_1 Q_0$

0	00	01	10	11
1	x	x	x	x

$$\bar{J}_2 = Q_1 Q_0$$

Q_2 $Q_1 Q_0$

0	x	x	x	x
1				

$$K_2 = Q_1 Q_0$$

Q_2 $Q_1 Q_0$

0				
1	x	x	x	x

$$\bar{J}_1 = Q_0$$

Q_2 $Q_1 Q_0$

0	x	x	1	
1	x	x	1	

$$K_1 = Q_0$$

Q_2 $Q_1 Q_0$

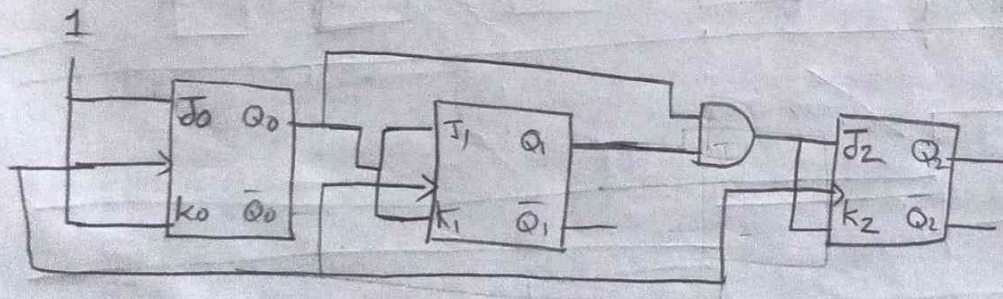
0	1	x	x	1
1	1	x	x	1

$$\bar{J}_0 = 1$$

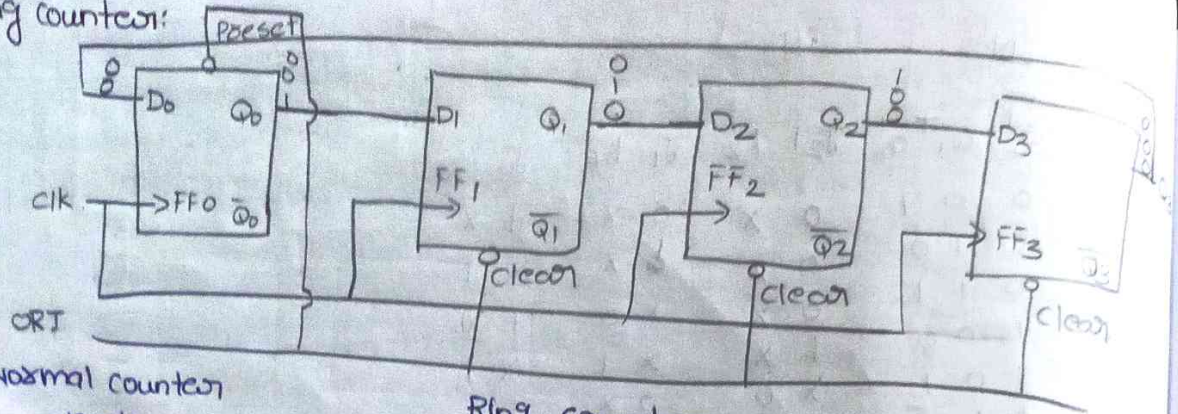
Q_2 $Q_1 Q_0$

0	x	1	1	x
1	x	1	1	x

$$K_0 = 1$$



Ring counter:



Normal counter
 $n=4$

Ring counter
 $n=4$

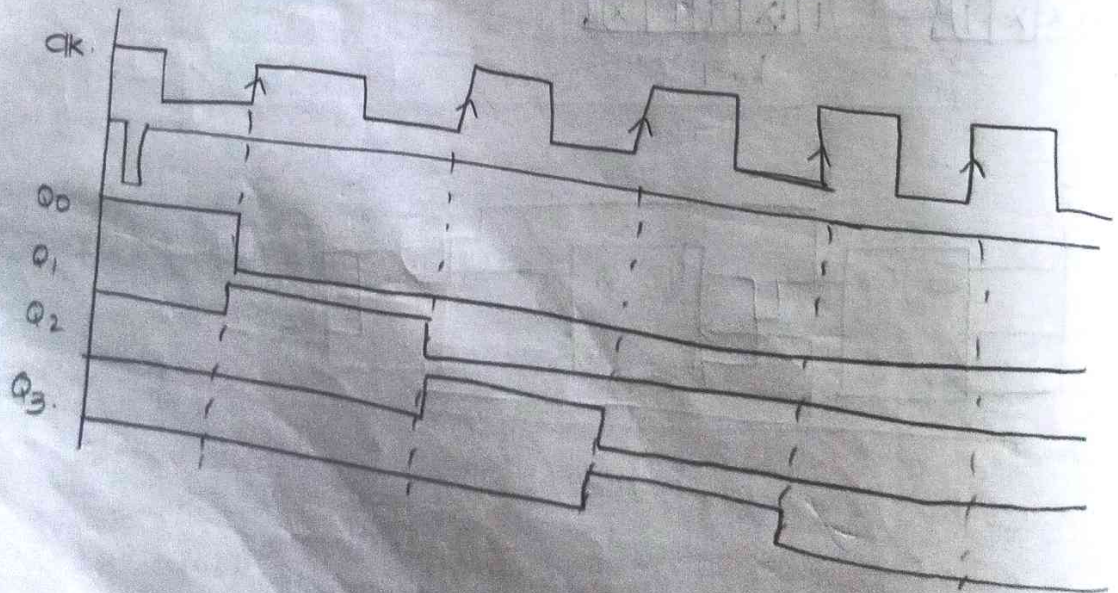
$2^n \Rightarrow 2^4 = 16$ states

$n=4$
 $4 \rightarrow$ states.

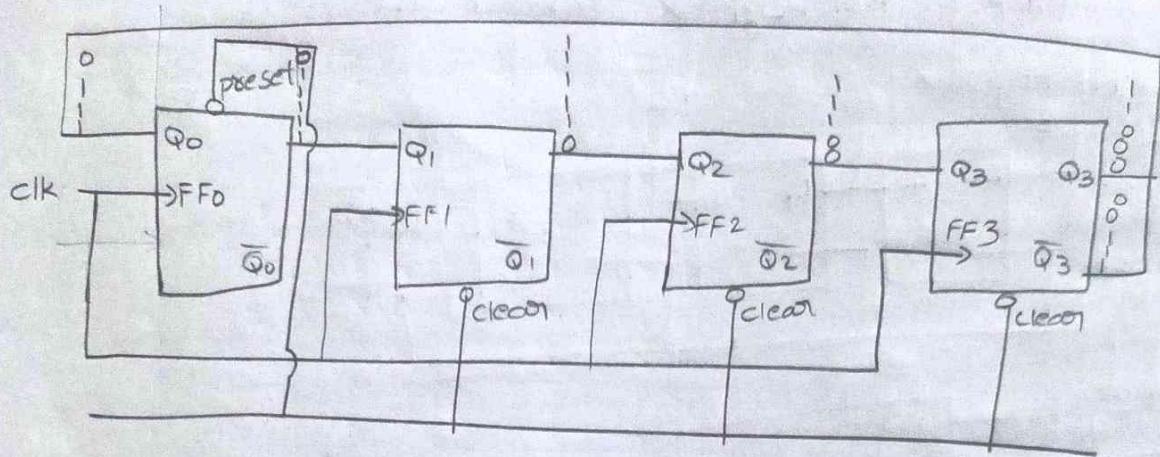
Active low input

ORI (over side)
Input

ORI (over side) Input	clk	Q_0	Q_1	Q_2	Q_3
0	X	1	0	0	0
1		0	1	0	0
1		0	0	1	0
1		0	0	0	1
1		1	0	0	0



Johnson counter.

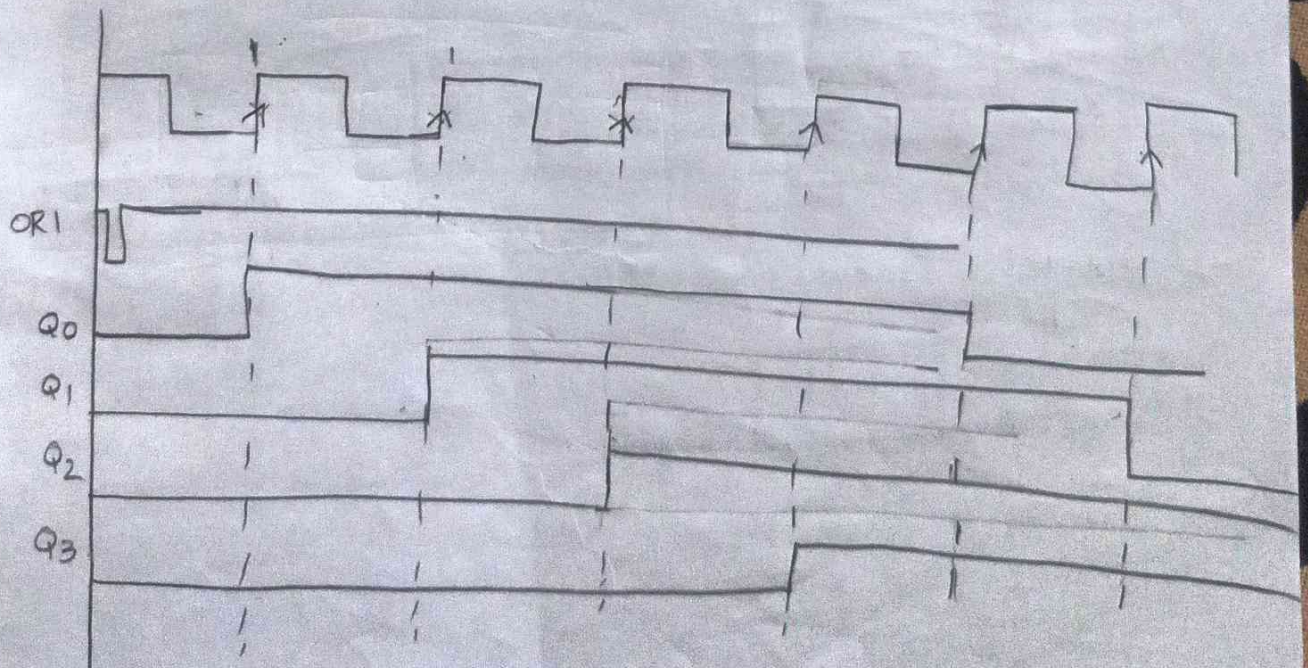


OR ₁	clk	Q ₀	Q ₁	Q ₂	Q ₃
0	x	1	0	0	0
1		1	1	0	0
1		1	1	1	0
1		1	1	1	1
1		0	1	1	1
1		0	0	1	1
1		0	0	0	1
1		0	0	0	0
1		1	0	0	0

$$N=4$$

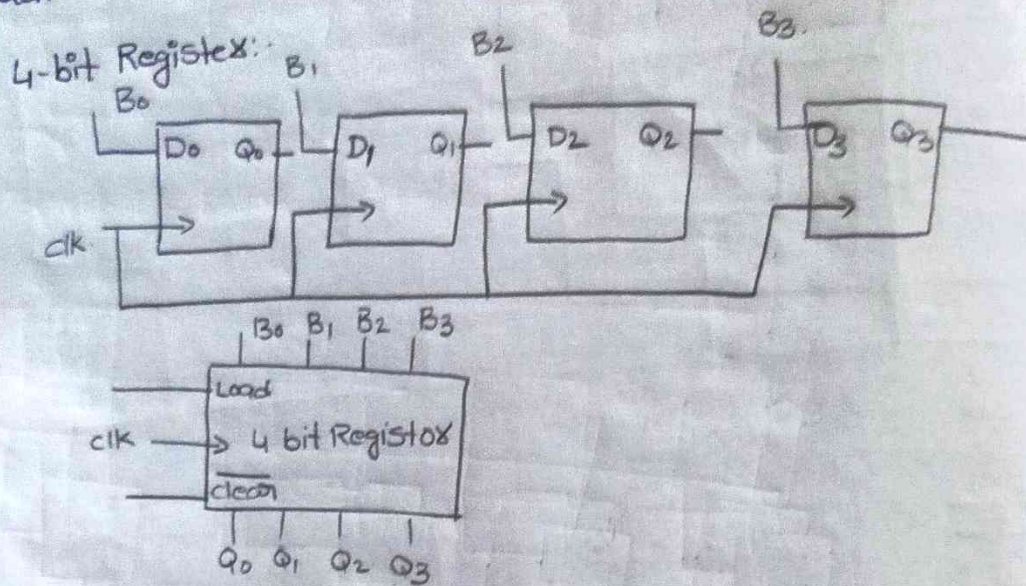
$$\text{No. of states} = 2n$$

$$4 \text{ ff} \Rightarrow 2 \times 4 = 8 \text{ states}$$



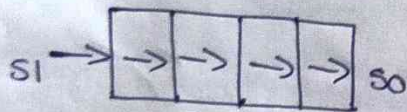
Shift Register:-

- It is the group of flipflops which stores n-bit of data.
- each flipflop in the register shares a common clock.

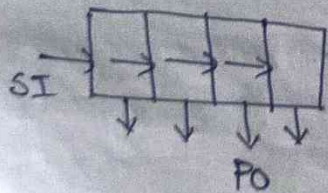


→ A register capable of shifting the data b/w the neighbouring flipflop in a selected direction is called Shift Register.

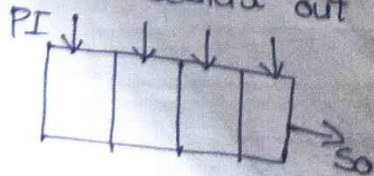
→ Serial in serial out (SISO):-



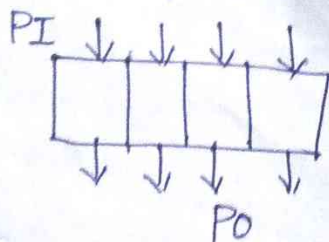
→ Serial in parallel out (SIPO):-



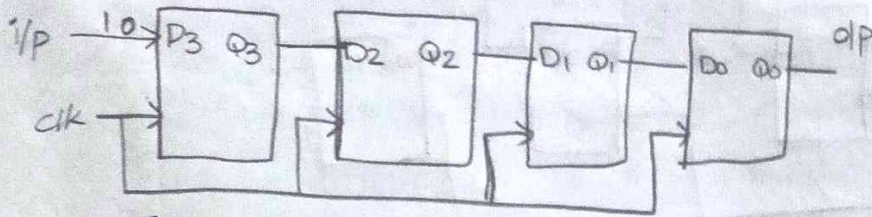
→ Parallel in serial out (PISO):-



→ Parallel in parallel out (PIPO):-



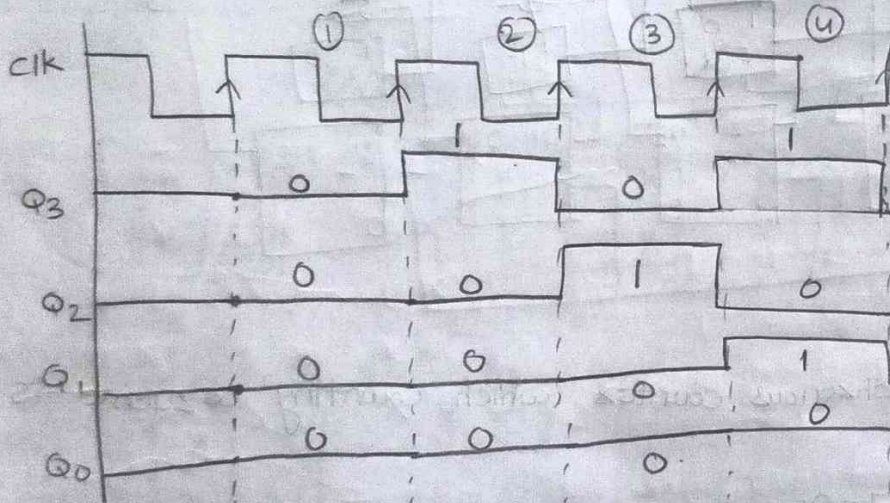
Serial In Serial Out:- (SISO):



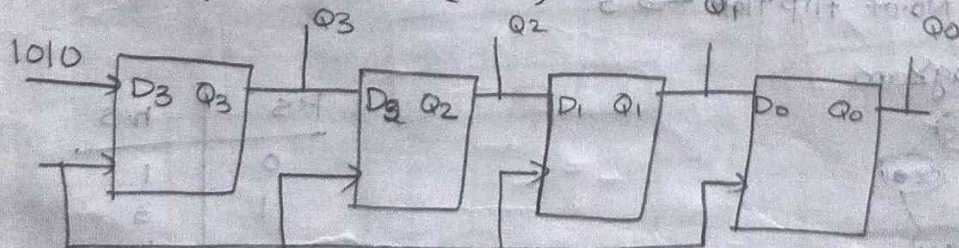
clk	i/p	Q3	Q2	Q1	Q0
0	x	0	0	0	0
↑	0	0	0	0	0
↑	1	1	0	0	0
↑	0	0	1	0	0
↑	1	0	0	1	0

data 1010

To store n bit n- clk signals req.
To retrieve n bit n- clk signals req.

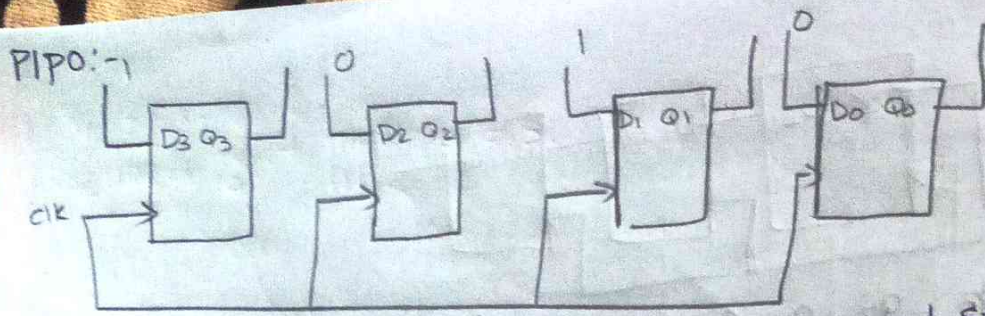


Serial In Parallel Out:- (SIPO)

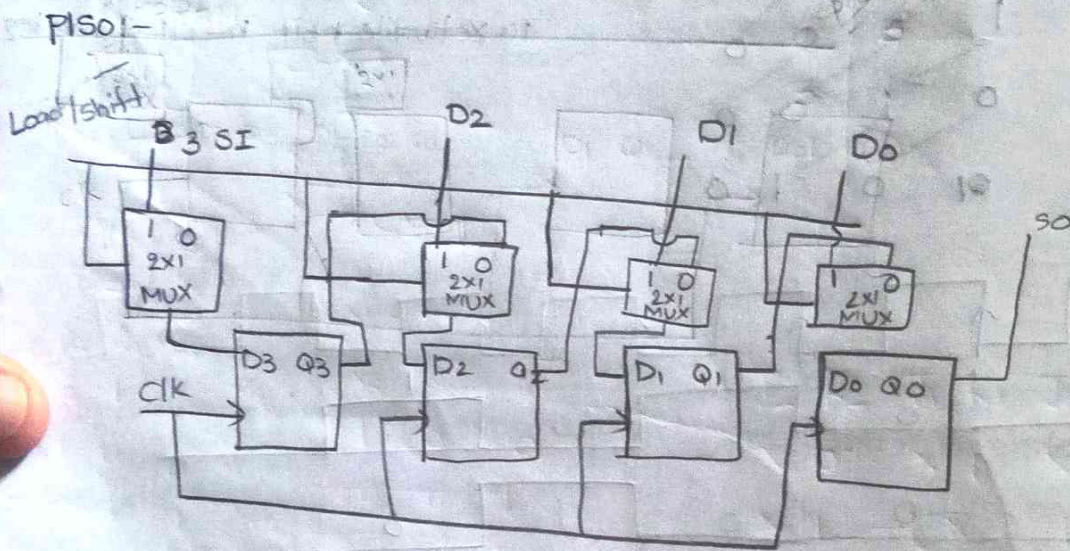


clk	i/p	Q3	Q2	Q1	Q0
0	x	0	0	0	0
↑	0	0	0	0	0
↑	1	1	0	0	0
↑	0	0	1	0	0
↑	1	1	0	1	0

To store n bit n- clk signals.
To retrieve no clk signal
required because o/p is
directly available.



signal clk pulse is required to rewrite and store.

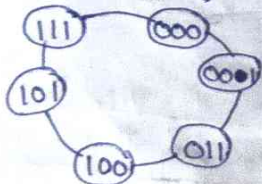


Q:- Design a synchronous counter which counting sequence is as follows

0-1-3-5-7-0

1) Required No. of flip flop $\rightarrow 3$.

2) State diagram



3) JK flip flop excitation table:

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

PS	n.s
0	1
1	3
3	4
5	7
7	0

P.S	N.S	IP
$Q_2 Q_1 Q_0$	$Q_2^+ Q_1^+ Q_0^+$	$J_2 k_2 \quad J_1 k_1 \quad J_0 k_0$
0 0 0	0 0 1	0 x 0 x 1 x
0 0 1	0 1 1	0 x 1 x x 0
0 1 1	1 0 0	1 x x 1 x 1
1 0 0	1 0 1	x 0 0 x 1 x
1 0 1	1 1 1	x 0 1 x x 0
1 1 1	0 0 0	x 1 x 1 x 1

$J_2 = Q_1$

$Q_2 \backslash Q_1 Q_0$	00	01	10	11
0			1	x
1	x	x	x	x

In The Given sequence 2,6 are not given
so take don't care values at 2,6th position.

$K_2 = Q_1$

$Q_2 \backslash Q_1 Q_0$	00	01	10	11
0	x	x	x	x
1			1	x

$J_1 = Q_0$

$Q_2 \backslash Q_1 Q_0$	00	01	10	11
0		1	x	x
1		1	x	x

$K_1 = 1$

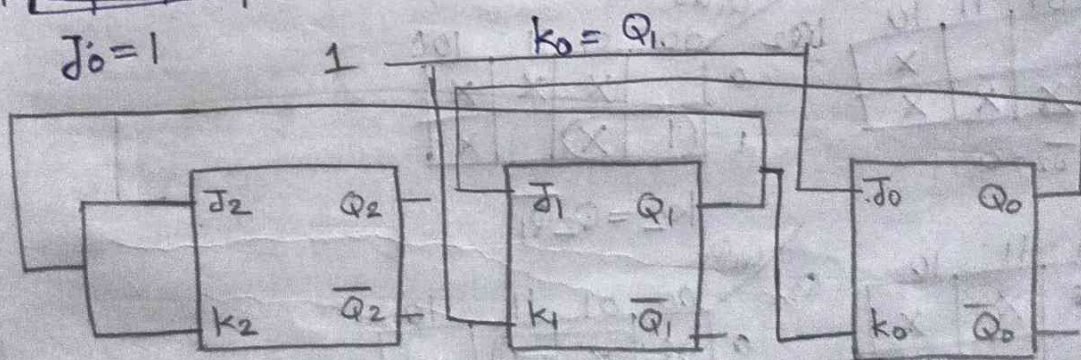
$Q_2 \backslash Q_1 Q_0$	00	01	10	11
0	x	x	1	x
1	x	x	1	x

$J_0 = 1$

$Q_2 \backslash Q_1 Q_0$	00	01	10	11
0	1	x	x	x
1	1	x	x	x

$K_0 = Q_1$

$Q_2 \backslash Q_1 Q_0$	00	01	10	11
0	x		1	x
1	x		1	x



0-1-3-4-

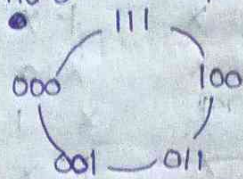
Q) 7-4-3-1-0

HW

7-4-3-1-0

1) Required no. of flipflops = 3.

2)



3) JK flipflop excitation table.

Q	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

P.S	N.S
7	4
4	3
3	1
1	0

P.S

Q_2	Q_1	Q_0
1	1	1
1	0	0
0	1	1
0	0	1

N.S

Q_2^+	Q_1^+	Q_0^+
1	0	0
0	1	1
0	0	1
0	0	0

J_2 k_2

X	0
X	1
0	X
0	X

J_1 k_1

X	1
1	X
X	1
0	X

J_0 k_0

X	1
1	X
X	0
0	X

2, 5, 6 are not given take don't cares at 2, 5, 6.

Q_2	Q_1	Q_0
0	00	01
1	11	10

$J_2 = 0$

Q_2	Q_1	Q_0
0	00	01
1	11	10

$k_2 = Q_2 \bar{Q}_1$

Q_2	Q_1	Q_0
0	00	01
1	11	10

$J_1 = Q_2$

Q_2	Q_1	Q_0
0	00	01
1	11	10

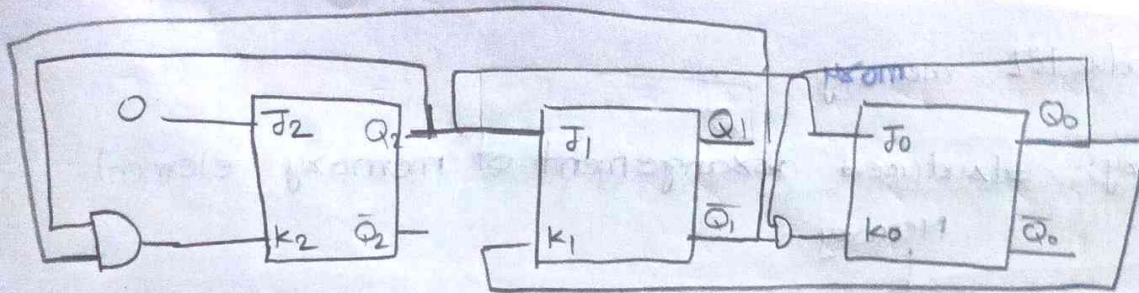
$k_1 = Q_0$

Q_2	Q_1	Q_0
0	00	01
1	11	10

$J_0 = Q_2$

Q_2	Q_1	Q_0
0	00	01
1	11	10

$k_0 = \bar{Q}_1 + Q_2 Q_1$



(clock) input

(clock) input

Shift register will be used when data is to be shifted.

Shift register

Shift register

FROM

TO

Shift register

Shift register

Shift register

Shift register

Shift register

Shift register

Shift register

Shift register



Data input

Data output

Shift register

Shift register

Shift register

Shift register

Shift register

Shift register

Shift register

Shift register