

82-08-24

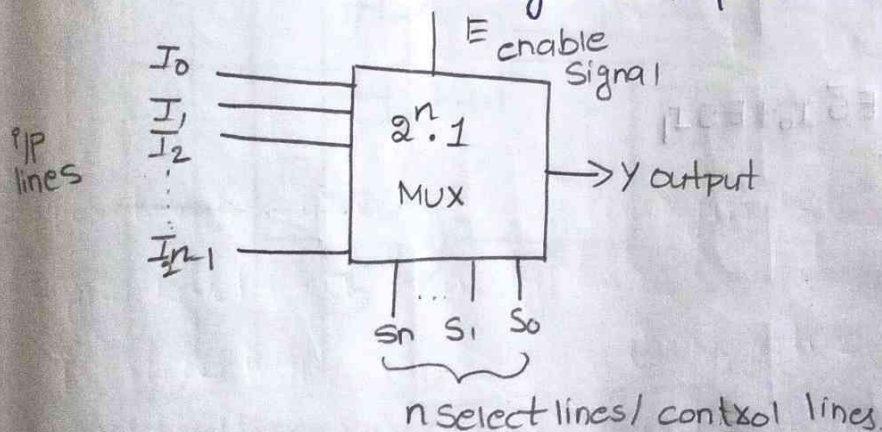
Multiplexer:- (Mux):

It is a digital combinational circuit that selects binary information from one of many i/p line and directs to a single o/p line.

→ The selection of particular i/p line is controlled by a set of selection lines.

→ There are 2^n i/p lines where n is the select lines ^{whose} bit combination determine which i/p is selected.

→ Multiplexer can also be named as data selector, many to one ckt, universal logic ckt, parallel to serial converter.



Types

- i) 2:1 Mux (1 select line) or 2x1
- ii) 4:1 Mux (2 select line)
- iii) 8:1 Mux (3 select lines)
- iv) 16:1 Mux (4 select lines)

$$\begin{matrix} 2^1 \\ 2^2 \\ 2^3 \\ 2^4 \end{matrix}$$

2:1 Mux (IC 74157)

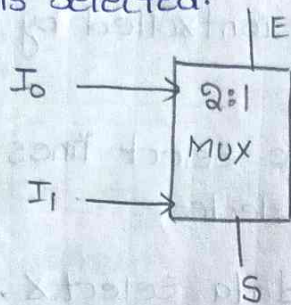
→ The 2:1 Multiplexer has 2 data or i/p lines (I_0, I_1), 1 select line (S), 1 output (Y).

operation:-

→ When Enable i/p is ~~said~~ set to zero the multiplexer will not work

→ When Enable i/p is set to one we get the output from Multiplexer.

→ When $S=0$, The data i/p I_0 is selected, when $S=1$, The data i/p I_1 is selected.



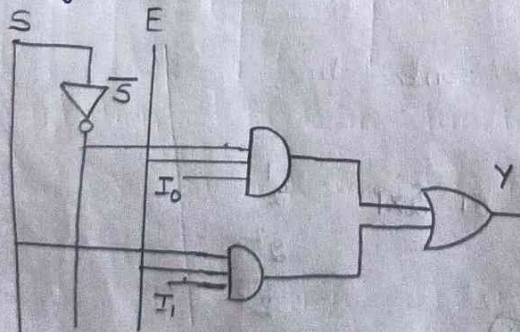
Active high
to Activate this
apply 1

Active low
to Activate this
apply 0

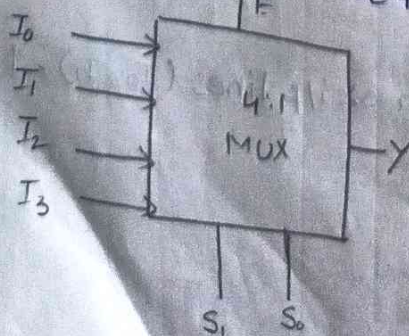
E	S	Y
0	X	X
1	0	I_0
1	1	I_1

$$Y = E\bar{S}I_0 + ES I_1$$

Logic diagram.



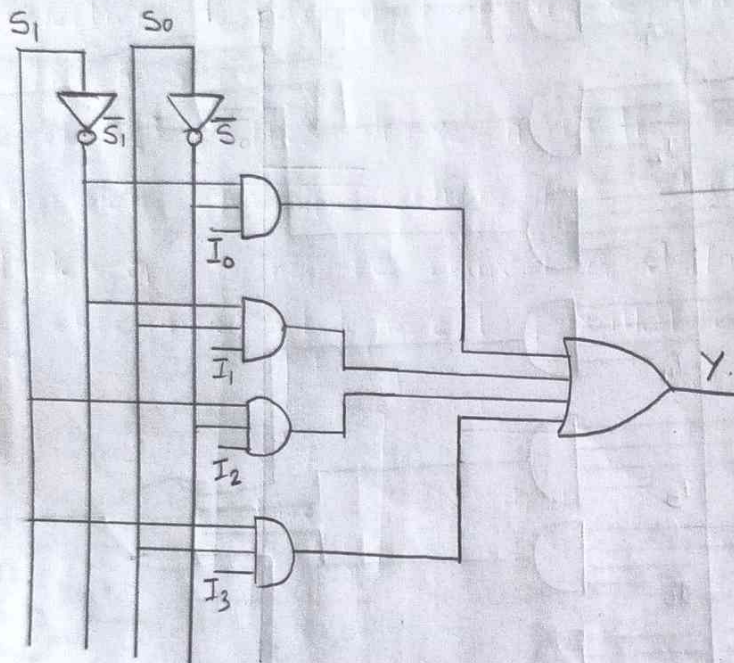
a) 4:1 Multiplexer (MUX) (IC 74153)



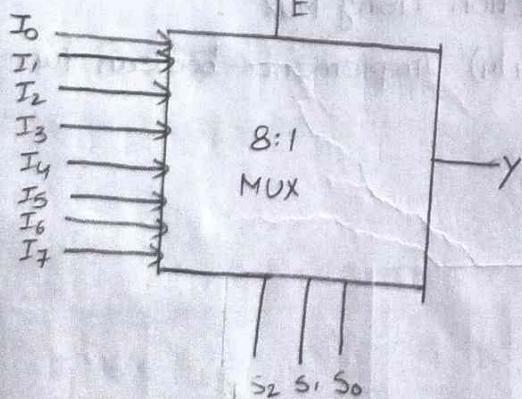
E	S ₁	S ₀	Y
0	X	X	X
1	0	0	I ₀
1	0	1	I ₁
1	1	0	I ₂
1	1	1	I ₃

$$Y = E\bar{S}_1\bar{S}_0I_0 + E\bar{S}_1S_0I_1 + ES_1\bar{S}_0I_2 + ES_1S_0I_3$$

$$Y = \bar{S}_1\bar{S}_0I_0 + \bar{S}_1S_0I_1 + S_1\bar{S}_0I_2 + S_1S_0I_3$$

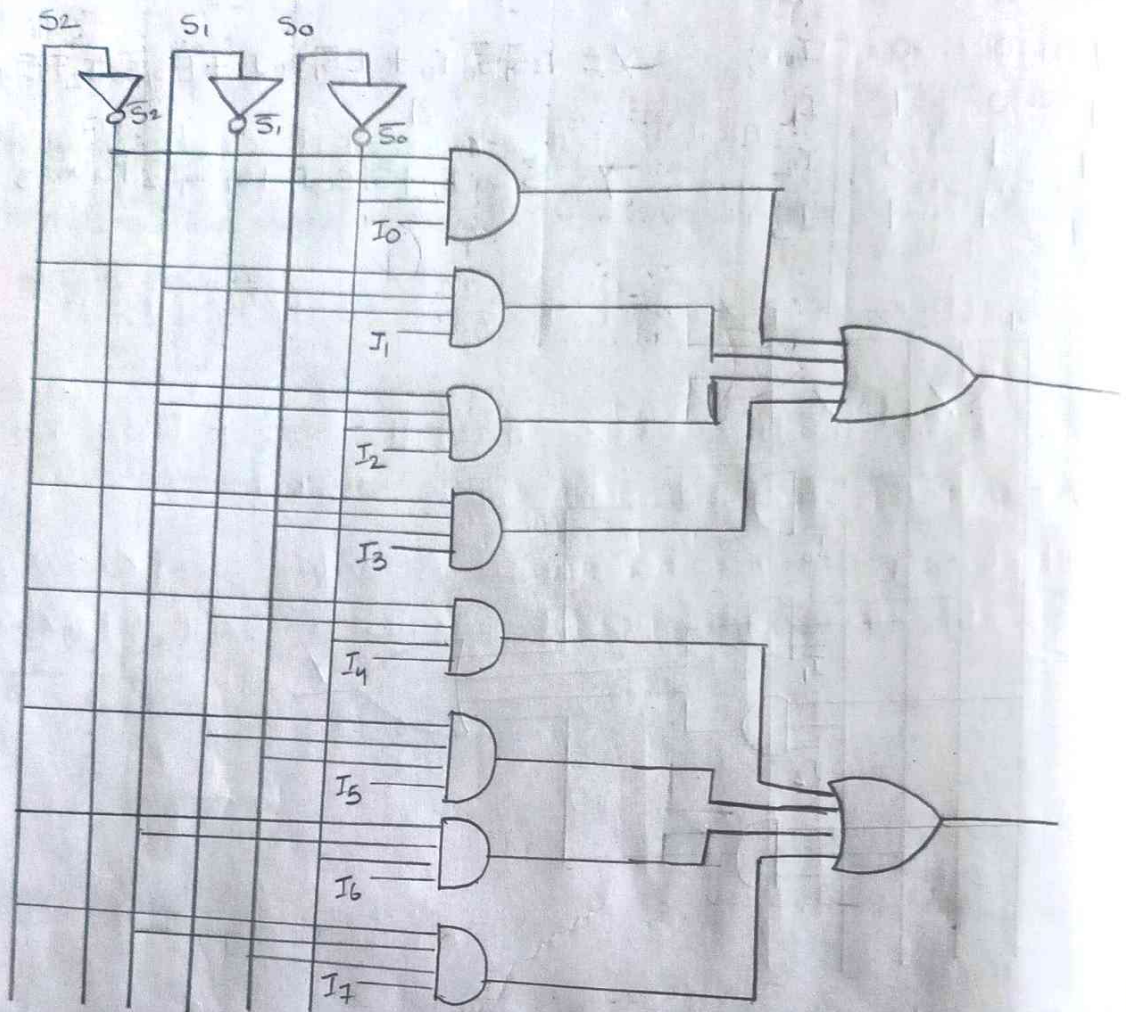


3) 8:1 Multiplexer (Mux) (IC 74151)



E	S ₂	S ₁	S ₀	Y
0	X	X	X	X
1	0	0	0	I ₀
1	0	0	1	I ₁
1	0	1	0	I ₂
1	0	1	1	I ₃
1	1	0	0	I ₄
1	1	0	1	I ₅
1	1	1	0	I ₆

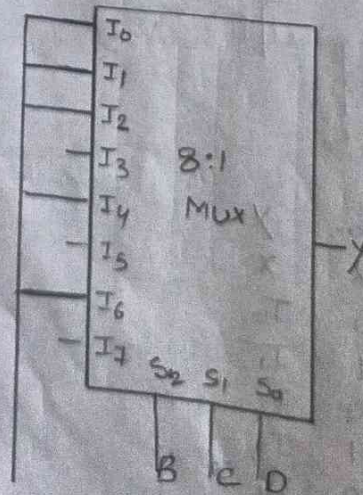
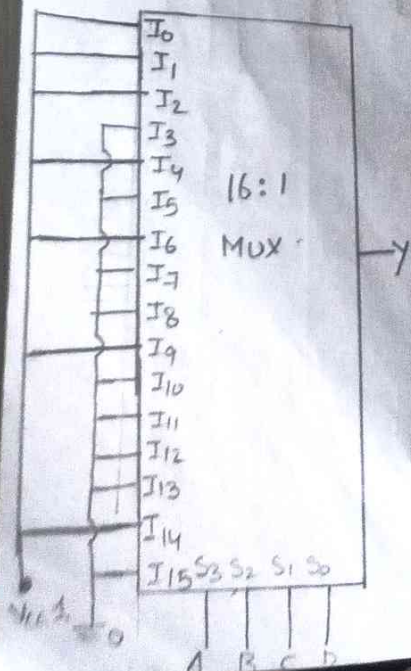
$$Y = \bar{S}_2 \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_2 \bar{S}_1 S_0 I_1 + \bar{S}_2 S_1 \bar{S}_0 I_2 + \bar{S}_2 S_1 S_0 I_3 + S_2 \bar{S}_1 \bar{S}_0 I_4 + S_2 \bar{S}_1 S_0 I_5 + S_2 S_1 \bar{S}_0 I_6 + S_2 S_1 S_0 I_7$$



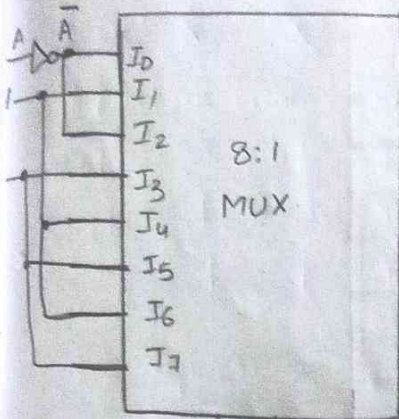
Implementation of Boolean function using Mux

① $F(A, B, C, D) = \Sigma(0, 1, 2, 4, 6, 9, 12, 14)$ Implement boolean function using

- i) 16×1 ii) 8×1 iii) 4×1 iv) 2×1



ii) 8x1



B	C	D
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

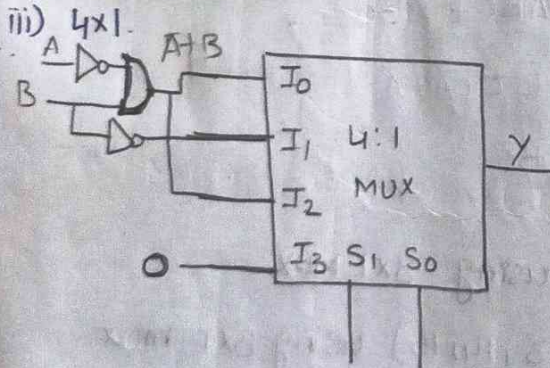
Implementation.

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
	$\bar{B}\bar{C}\bar{D}$	$\bar{B}\bar{C}D$	$\bar{B}C\bar{D}$	$\bar{B}CD$	$B\bar{C}\bar{D}$	$B\bar{C}D$	$BC\bar{D}$	BCD
$\bar{A}$	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
F	$\bar{A}$	1	$\bar{A}$	0	1	0	1	0

No grouping = 0

All are grouped = 1

iii) 4x1



$$I_1 = \bar{A}\bar{B} + A\bar{B}$$

$$= \bar{B}(\bar{A} + A)$$

$$I_1 = \bar{B}$$

$$I_2 = \bar{A}\bar{B} + \bar{A}B + AB$$

$$= \bar{A} + B$$

	I_0	I_1	I_2	I_3
	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
$\bar{A}\bar{B}$	0	1	2	3
$\bar{A}B$	4	5	6	7
$A\bar{B}$	8	9	10	11
AB	12	13	14	15
F				0

$$I_0 = \bar{A}\bar{B} + \bar{A}B + AB$$

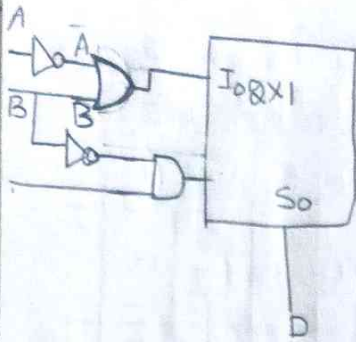
$$I_0 = \bar{A}(\bar{B} + B) + AB$$

$$I_0 = \bar{A} + AB$$

$$I_0 = \bar{A} + B$$

$$I_3 = 0$$

IV) 2:1 MUX



	I_0	I_1
$\bar{A}\bar{B}\bar{C}$	0	1
$\bar{A}\bar{B}C$	2	3
$\bar{A}B\bar{C}$	4	5
$\bar{A}BC$	6	7
$A\bar{B}\bar{C}$	8	9
$A\bar{B}C$	10	11
$AB\bar{C}$	12	13
ABC	14	15

$$I_0 = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + A\bar{B}C$$

$$= \bar{A}\bar{B}(C + \bar{C}) + \bar{A}B(C + \bar{C}) + A\bar{B}(C + \bar{C})$$

$$I_1 = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C$$

$$= \bar{A}\bar{B} + \bar{A}B + A\bar{B} + AB$$

$$= \bar{A}(B + \bar{B}) + AB$$

$$= \bar{A} + AB$$

$$= \bar{A} + B$$

$$I_1 = \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$$

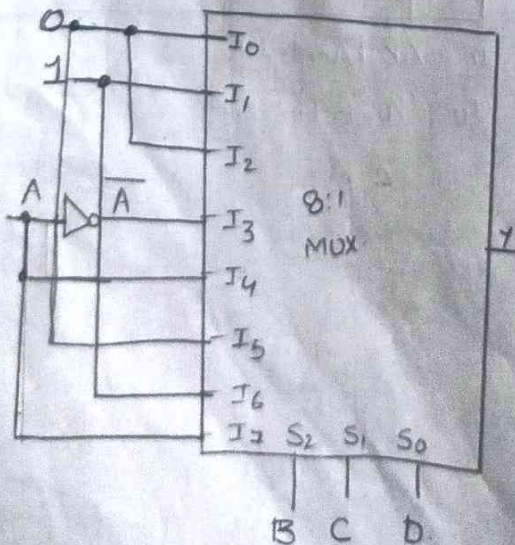
$$= \bar{B}\bar{C}(\bar{A} + A)$$

$$= \bar{B}\bar{C}$$

H.W.:-

① $F(A, B, C, D) = \sum m(1, 3, 6, 9, 12, 14, 15)$ using 8:1 MUX.

② $F(A, B, C, D) = \sum m(1, 3, 14, 11, 12, 13, 14, 15)$ using 8:1 MUX.



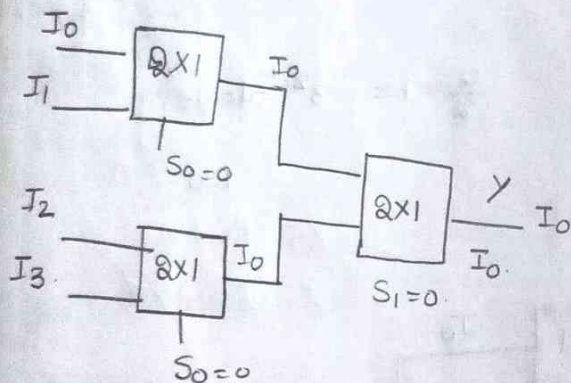
	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
	$\bar{B}\bar{C}\bar{D}$	$\bar{B}\bar{C}D$	$\bar{B}C\bar{D}$	$\bar{B}CD$	$B\bar{C}\bar{D}$	$B\bar{C}D$	$BC\bar{D}$	BCD
$\bar{A}$	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
F	0	1	0	$\bar{A}$	A	0	1	A

Implementation of Higher order Multiplexer using lower order multiplexer.

① Implement 4:1 MUX using 2:1 MUX

$$\frac{\text{Required MUX}}{\text{Available MUX}} = \frac{4}{2} = 2 \quad (2 - 2:1 \text{ MUX}) \text{ first stage}$$

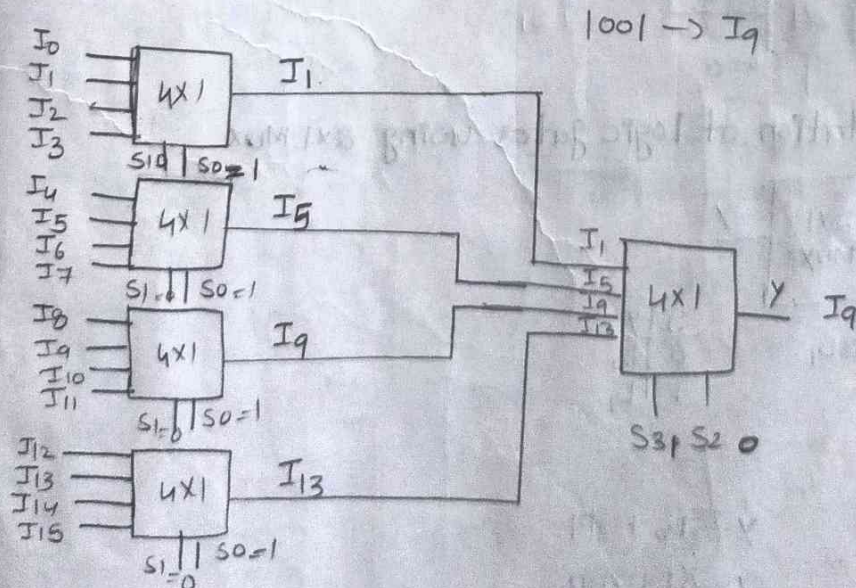
$$\frac{2}{2} = 1 \quad (1 - 2:1 \text{ MUX}) \text{ Second Stage.}$$



② 16:1 MUX using 4:1 MUX

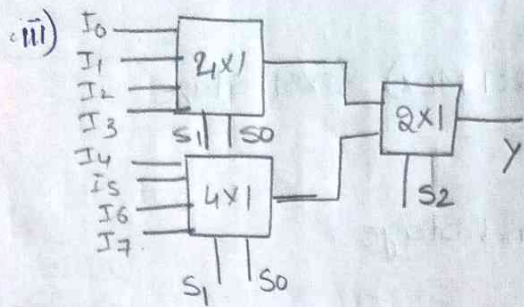
$$\frac{16}{4} = 4 \quad \text{first stage}$$

$$\frac{4}{4} = 1 \quad \text{second stage.}$$



iii) 8x1 MUX using 4x1 MUX

iv) 8x1 MUX using 2x1 MUX

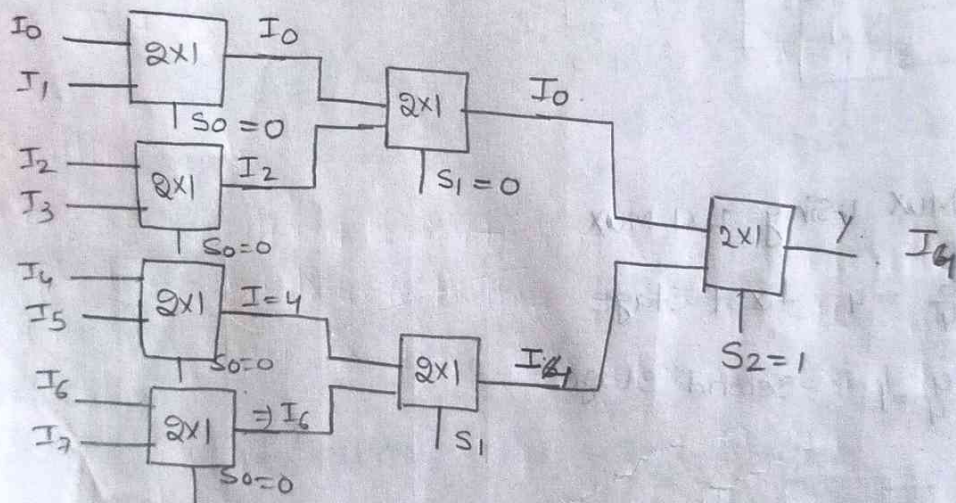


iv) $\frac{8}{2} = 4$ 1st stage

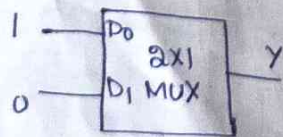
$\frac{2}{2} = 1 = 3^{rd}$ stage.

$\frac{4}{2} = 2$ 2nd stage.

100



Implementation of Logic gates using 2x1 MUX



$$Y = \bar{S}D_0 + SD_1$$

S	Y
0	D ₀
1	D ₁

NOT



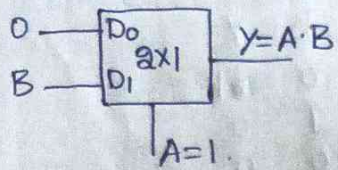
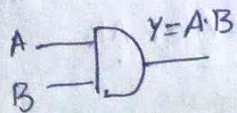
A	$\bar{A}$
0	1
1	0

$$Y = \bar{S}D_0 + SD_1$$

$$Y = \bar{A} \cdot 1 + A \cdot 0$$

$$Y = \bar{A}$$

AND:-



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

$$Y = \bar{S}D_0 + SD_1$$

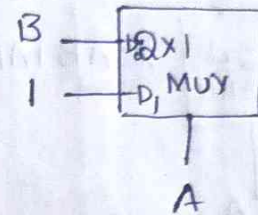
$$= \bar{A} \cdot 0 + A \cdot B$$

$$= AB$$

OR:-



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



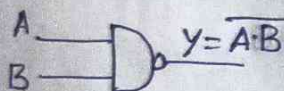
$$Y = \bar{S}D_0 + SD_1$$

$$= \bar{A}B + A \cdot 1$$

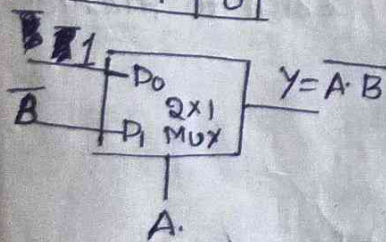
$$= \bar{A}B + A$$

$$= A + B$$

NAND



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



XOR

$$Y = \bar{S}D_0 + SD_1$$

$$= \bar{A} \cdot 1 + A \bar{B}$$

$$= \bar{A} + A \bar{B}$$

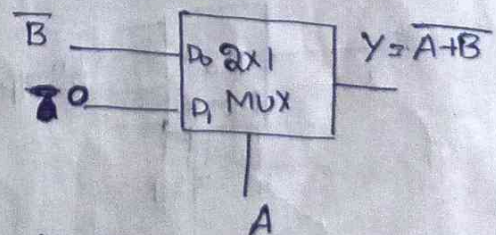
$$= \bar{A} + \bar{B}$$

$$= \overline{A \cdot B}$$

NOR:-



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



$$Y = \bar{S}D_0 + SD_1$$

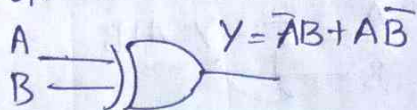
$$= \bar{A} \bar{B} + A \cdot 0$$

$$= \bar{A} \bar{B} + A$$

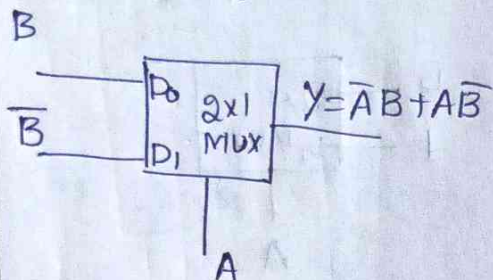
$$= \overline{A \cdot B}$$

$$= \overline{A + B}$$

X-OR



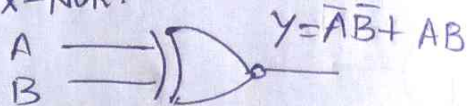
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



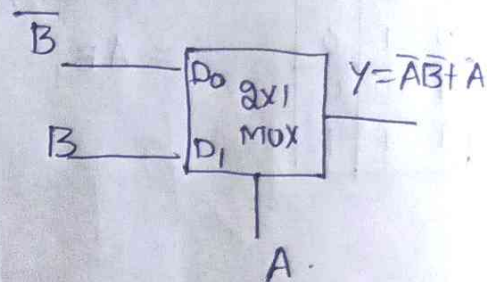
$$Y = \bar{B}D_0 + BD_1$$

$$Y = \bar{A}B + A\bar{B}$$

X-NOR:-



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

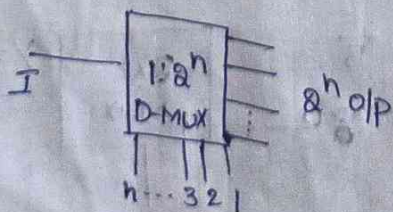


$$Y = \bar{B}D_0 + BD_1$$

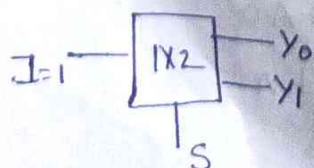
$$Y = \bar{A}B + A\bar{B}$$

Demultiplexer:-

It is a combinational circuit that receives information on a single line and transmits this of 2^n possible output lines.
 → It is also known as data distributor or serial to parallel converter.



1x2 MUX

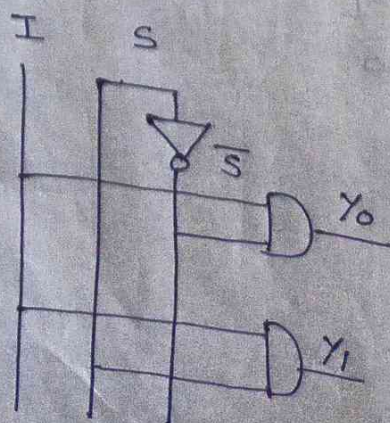


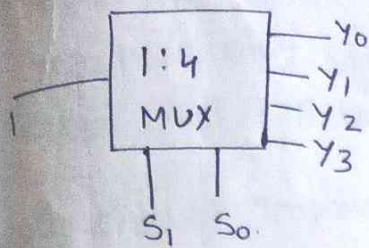
I	S	Y0	Y1
1	0	1	0
1	1	0	1

$$Y_0 = I\bar{S} + I_S$$

$$Y_0 = I\bar{S}$$

$$Y_1 = I_S$$





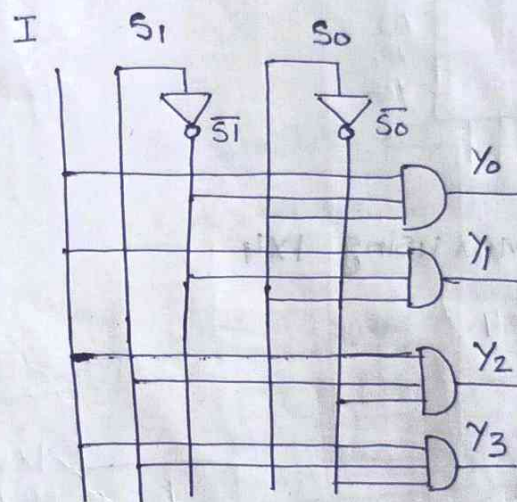
I	S ₁	S ₀	Y ₀	Y ₁	Y ₂	Y ₃
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

$$Y_0 = I \bar{S}_1 \bar{S}_0$$

$$Y_1 = I \bar{S}_1 S_0$$

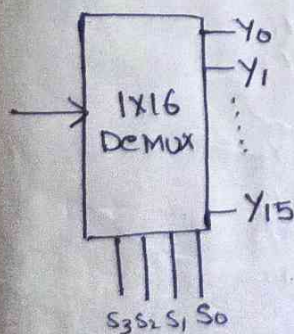
$$Y_2 = I S_1 \bar{S}_0$$

$$Y_3 = I S_1 S_0$$



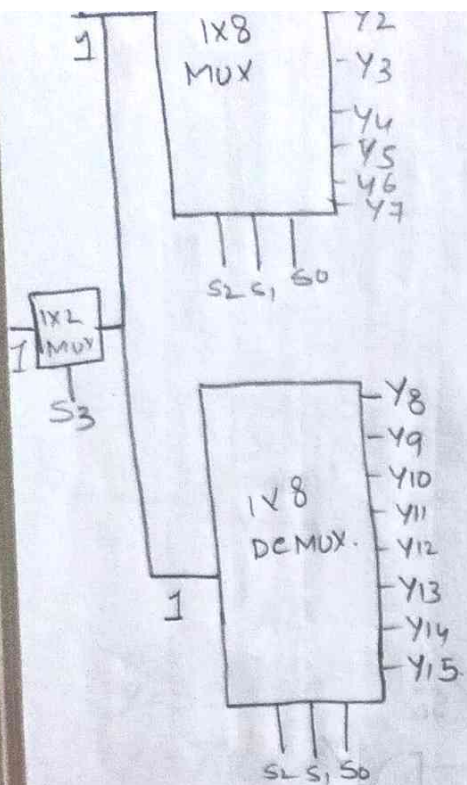
Higher order De-Mux using Lower order De-Mux

① 1x16 De-Mux using 1x8 De-Mux



2^n o/p.

$$\frac{16}{8} = 2$$

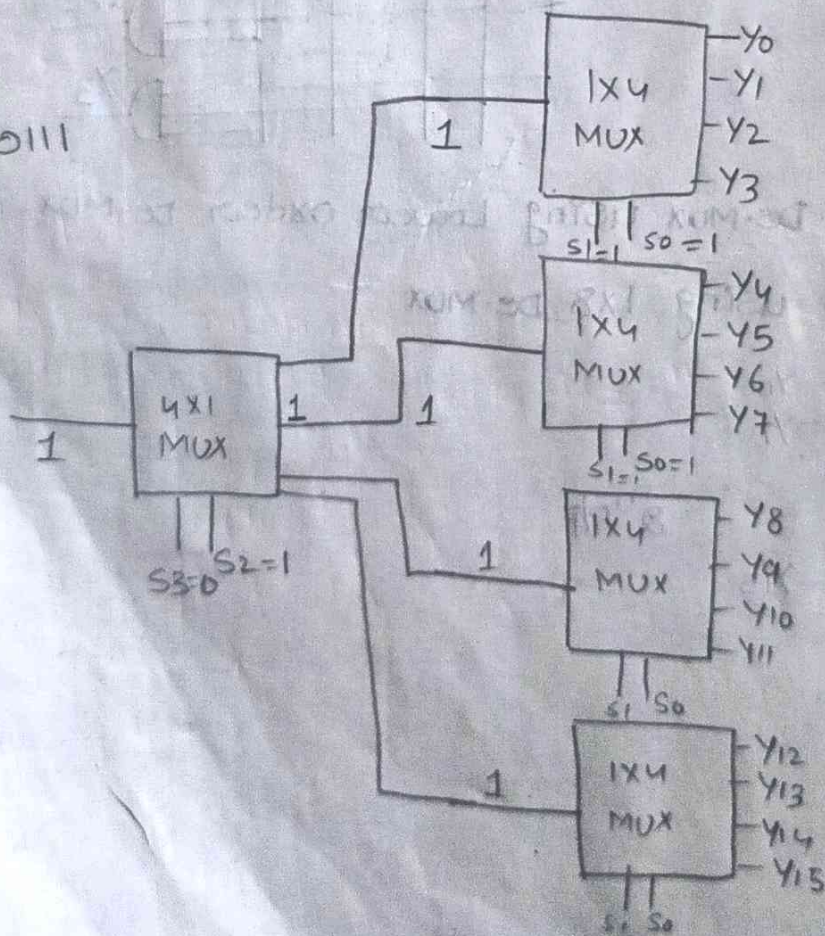


1x16 DeMUX using 1x4

$$\frac{16}{4} = 4 \text{ st stage}$$

$$\frac{4}{4} = 1 \rightarrow 2^{\text{nd}}$$

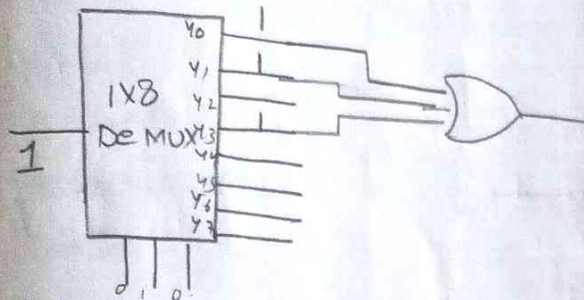
0111



- ③ Implement 1×16 De-Mux using 1×2 MUX
 1×32 MUX using 1×16 De-Mux
 1×32 using 1×8 De-Mux.

Logic circuit implementation using De-Mux:

$$F(A, B, C) = \sum m(0, 1, 14)$$

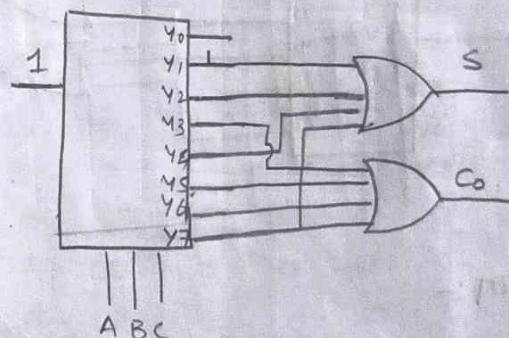


Full Adder:-

A	B	C _{in}	S	C _o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$S = \sum m(1, 2, 4, 7)$$

$$C_o = \sum m(3, 5, 6, 7)$$

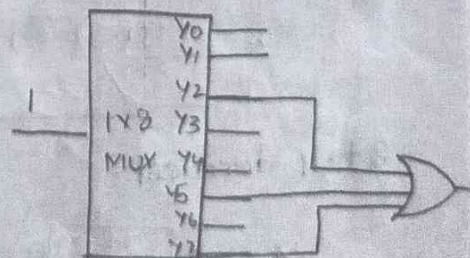


③ Implement

$$F_1(x, y, z) = \overline{x}y\overline{z} + xz$$

$$F_2(x, y, z) = x\overline{y}\overline{z} + \overline{x}y$$

$$\begin{aligned} F_1(x, y, z) &= \overline{x}y\overline{z} + xz \\ &= \overline{x}y\overline{z} + xz \cdot 1 \\ &= \overline{x}y\overline{z} + xz(y + \overline{y}) \\ &= \overline{x}y\overline{z} + xzy + x\overline{y}z \\ &= 010 + 111 + 101 \\ &= (2, 5, 7) \end{aligned}$$



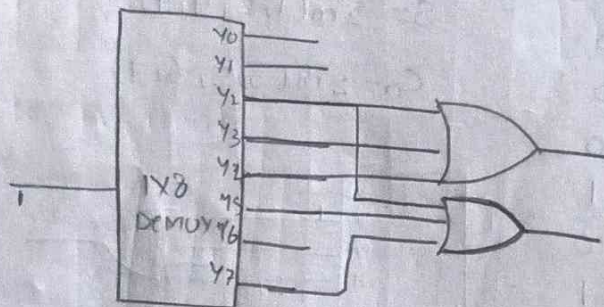
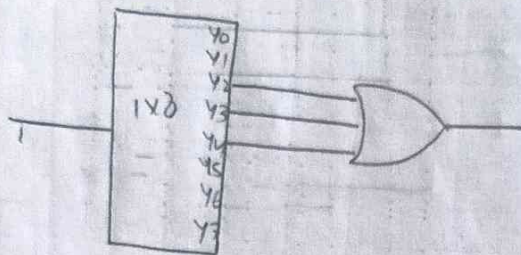
$$F_2(x, y, z) = x\bar{y}\bar{z} + \bar{x}y \cdot 1$$

$$= x\bar{y}\bar{z} + \bar{x}y(z + \bar{z})$$

$$= x\bar{y}\bar{z} + \bar{x}yz + \bar{x}y\bar{z}$$

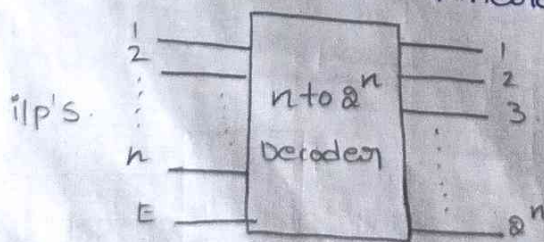
$$= 100 + 011 + 010$$

$$F_2(x, y, z) = \Sigma(2, 3, 4)$$

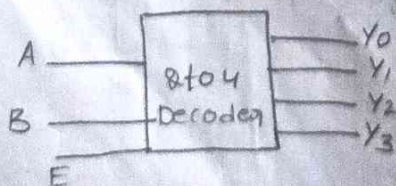


Decoder:-

Decoder is a combinational ckt which ~~accepts~~ accepts n i/p's & produce M outputs where $M \leq 2^n$.



2 to 4 decoder:-



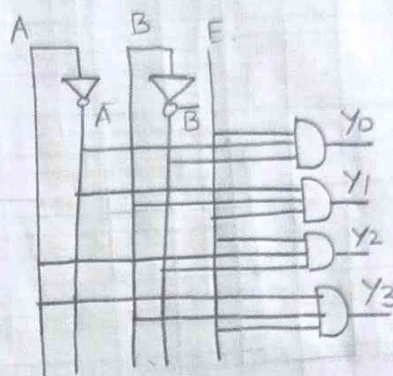
E	A	B	Y_0	Y_1	Y_2	Y_3
0	x	x	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

$$Y_0 = \bar{E} \bar{A} \bar{B}$$

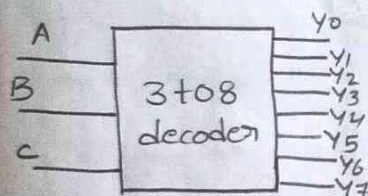
$$Y_1 = \bar{E} \bar{A} B$$

$$Y_2 = \bar{E} A \bar{B}$$

$$Y_3 = \bar{E} A B$$



3-to-8 decoder:-



E	A	B	C	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

$$Y_0 = \bar{E} \bar{A} \bar{B} \bar{C}$$

$$Y_1 = \bar{E} \bar{A} \bar{B} C$$

$$Y_2 = \bar{E} \bar{A} B \bar{C}$$

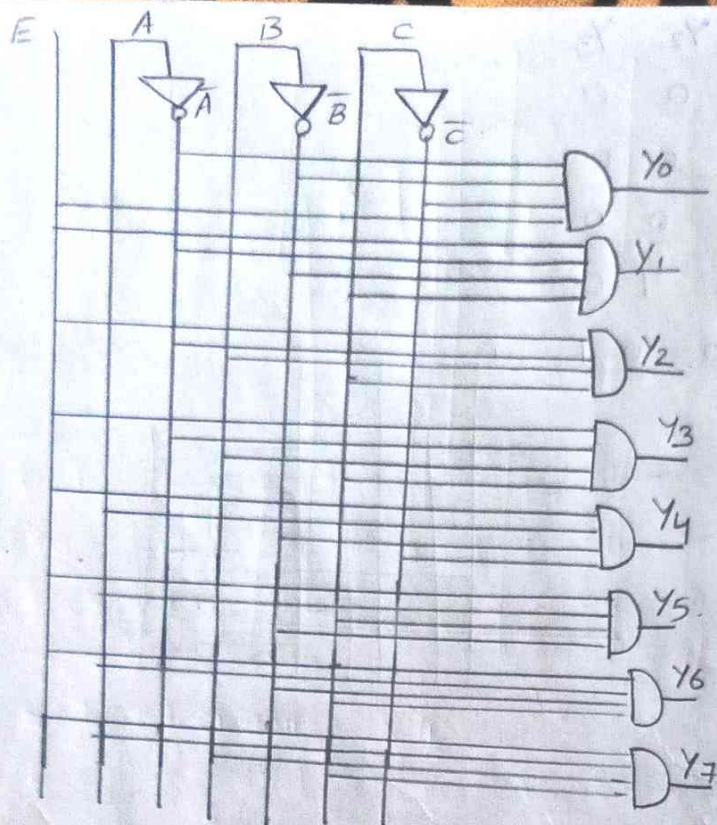
$$Y_3 = \bar{E} \bar{A} B C$$

$$Y_4 = \bar{E} A \bar{B} \bar{C}$$

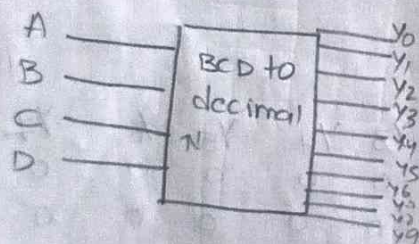
$$Y_5 = \bar{E} A \bar{B} C$$

$$Y_6 = \bar{E} A B \bar{C}$$

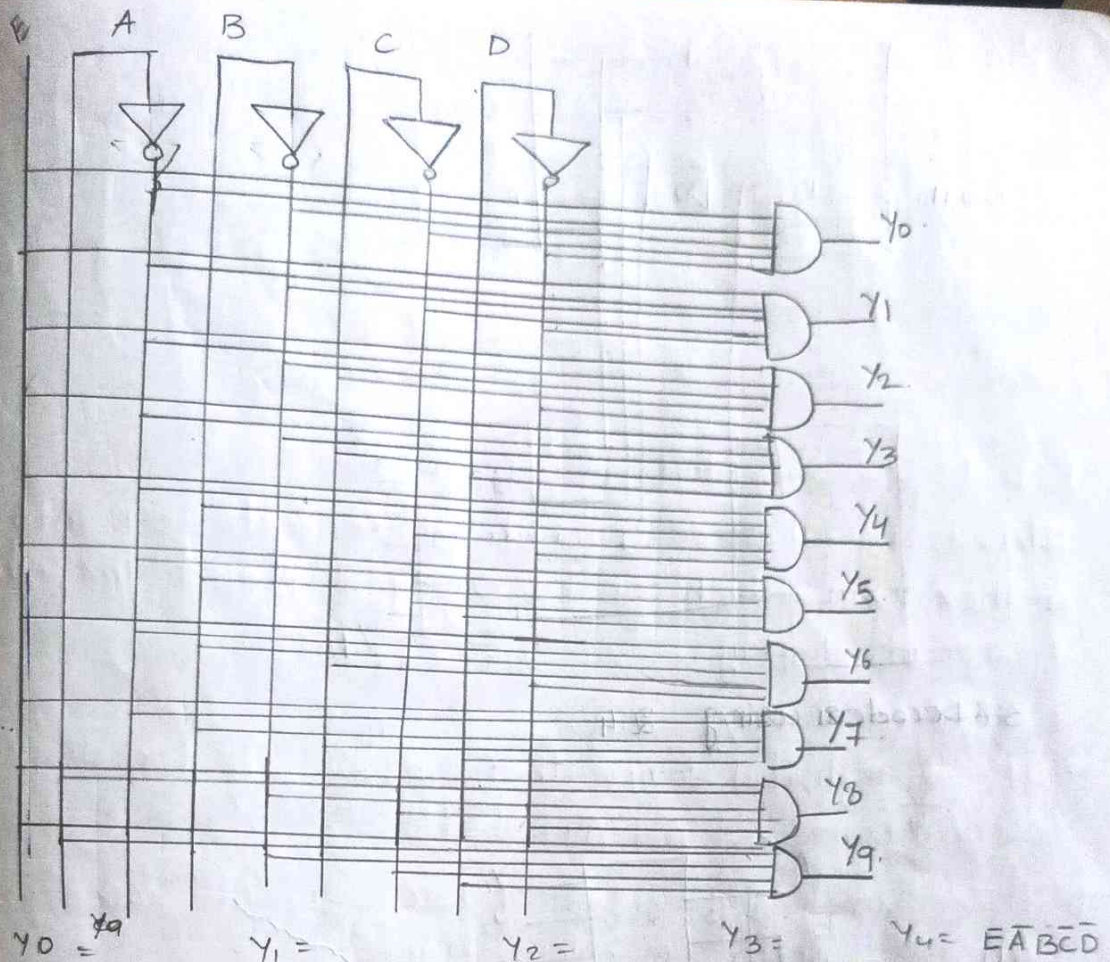
$$Y_7 = \bar{E} A B C$$



BCD to Decimal:-

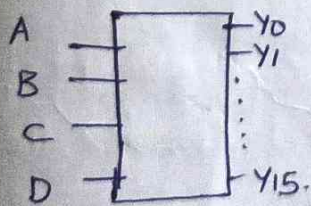


E	A	B	C	D	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇	Y ₈	Y ₉
0														
1	0	0	0	0	1	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	1	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	1	0	0	0	0	0	0
1	0	1	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	1	0	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	1	0	0	0	0
1	0	1	1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	0	0	1	0	0	0	0	0	0	0	0	1	0
1														



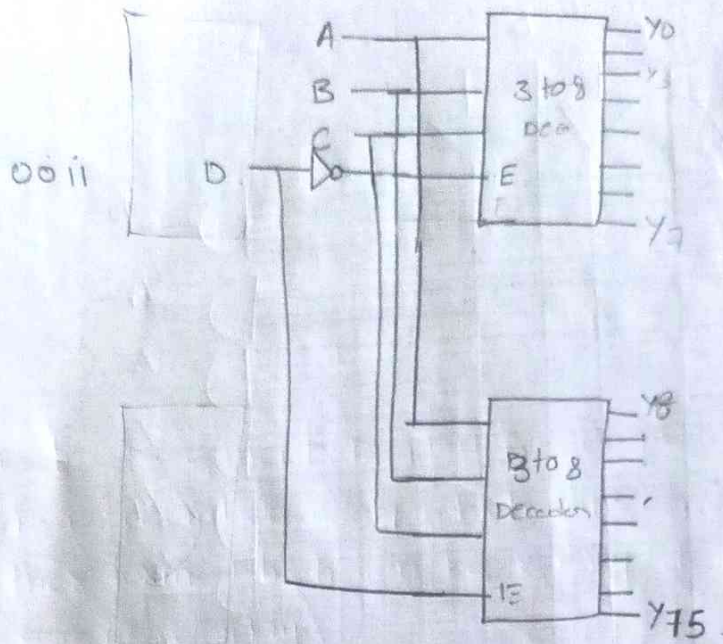
Implementation of Higher order decoder using lower order decoder:

4:16 Decoder using 3:8 decoder



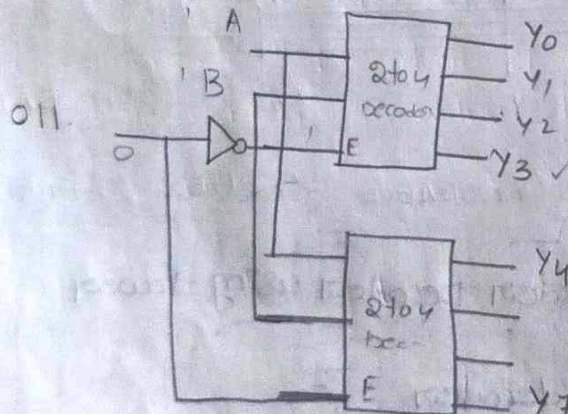
$$\frac{16}{8} = 2 - 3:8 \text{ decoders}$$

$A+B+C$
 $A+B \cdot C$
 $A \cdot B \cdot C$

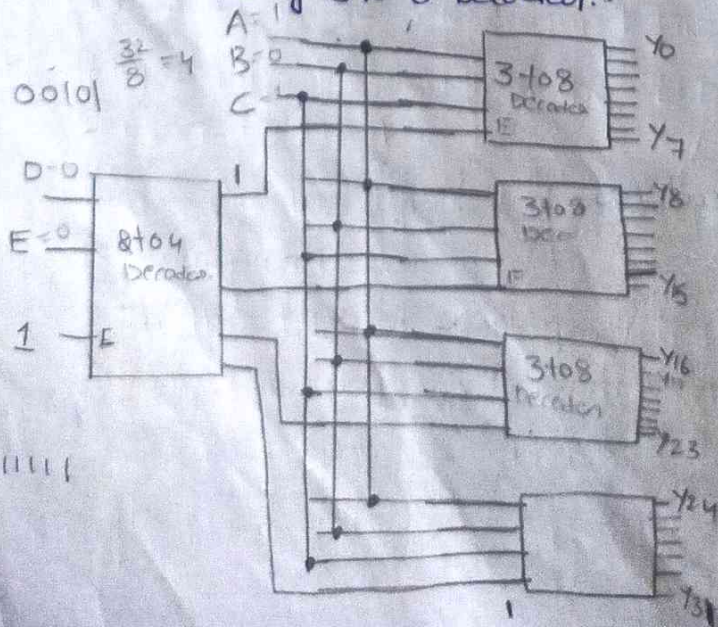


3:8 decoder using 2:4.

$$\frac{8}{4} = 2$$



5 to 32 using 3 to 8 Decoder:-



$$\frac{32}{8} = 4$$

$$2 \times \frac{4}{2} = 4$$

Implementation of logic function using decoder:-

① Full adder using decoder:

A B C_{in} S C_o

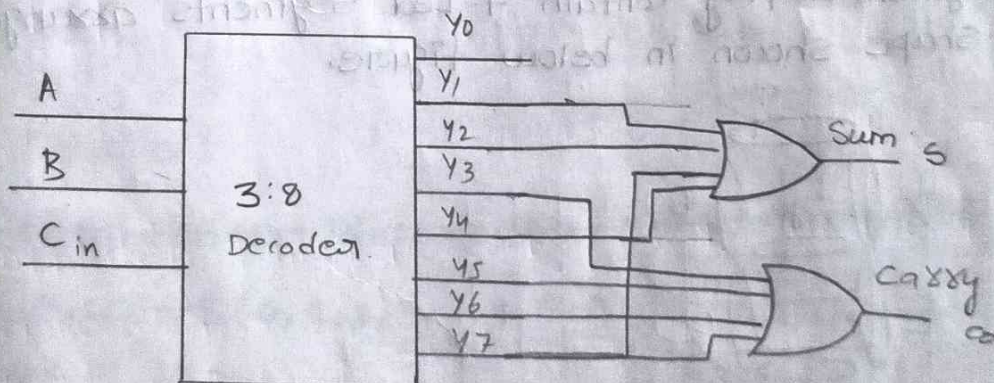
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0	0

Sum:-

$$S(A, B, C_{in}) = \sum (1, 2, 4, 7)$$

Carry

$$C(A, B, C_{in}) = \sum (3, 5, 6, 7)$$

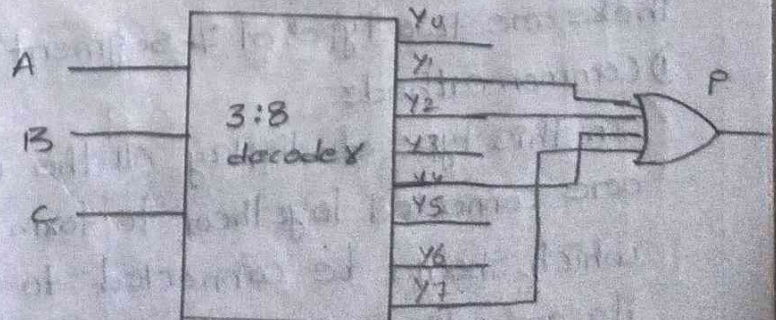


② Even parity decoder using

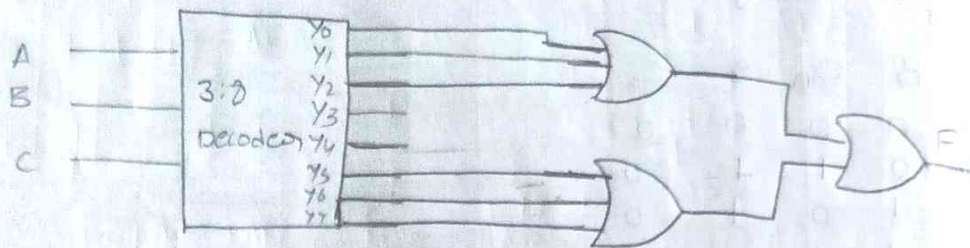
A B C P

0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$$P(A, B, C) = \sum (1, 2, 4, 7)$$



3) $F(A, B, C) = \sum(0, 4, 5, 6, 7)$

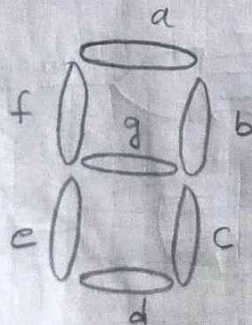


BCD to 7-Segment Display Decoder:-

It is a special decoder which can convert BCD into another form, which can be easily displayed through a 7-segment display.

7-Segment display:

- It is a digital device that can be used for displaying decimal numbers and Alphabets.
- 7-segment display contains 7 LED segments arranged in a shape shown in the below figure.

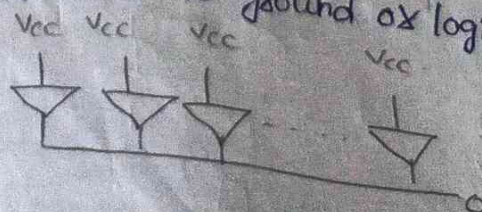


Generally, there are 8 input pins in a 7-segment display. 7 input pins for each of the LEDs and 1 pin for the common terminal.

There are two types of 7-segment displays

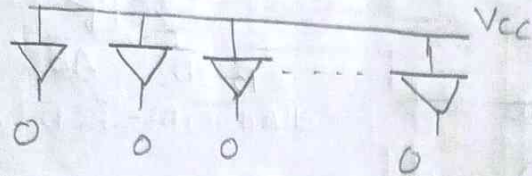
1) Common cathode

In this type of display, all the cathodes of 7 LEDs are connected together to form a common terminal, which should be connected to ground or logic 0 during its operation.



Common Anode:-

In this type of display All the Anode terminals of 7-LEDS are connected together to form a common Anode terminal. This terminal should be connected with logic 1 or V_{cc} .

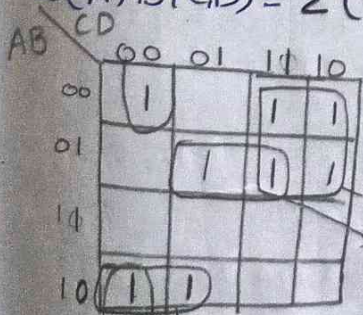


Common Cathode:-

D	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

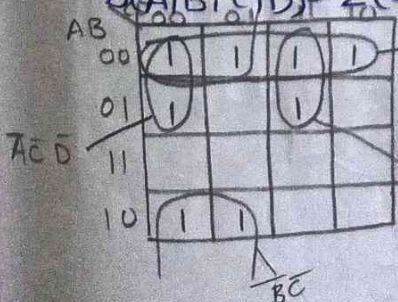
$$\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}BC\bar{D} + \bar{A}BCD$$

$$a(A, B, C, D) = \sum(0, 2, 3, 5, 6, 7, 8, 9)$$



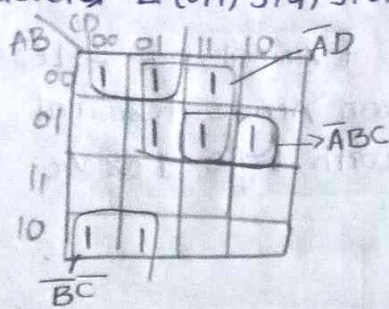
$$a = \bar{A}C + \bar{A}BD + \bar{A}\bar{B}\bar{C} + \bar{B}\bar{C}\bar{D}$$

$$b(A, B, C, D) = \sum(0, 1, 2, 3, 4, 7, 8, 9)$$

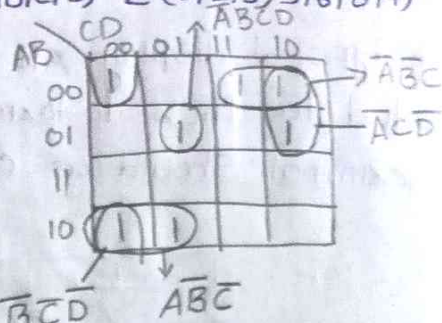


$$b = \bar{B}\bar{C} + \bar{A}CD + \bar{A}\bar{B} + \bar{A}C\bar{D}$$

$$c(A,B,C,D) = \sum (0,1,3,4,5,6,7,8,9) \quad d(A,B,C,D) = \sum (0,2,3,5,6,8,9)$$

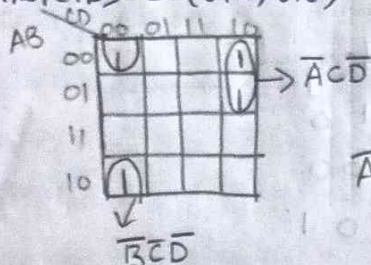


$$c(A,B,C,D) = \overline{B}\overline{C} + \overline{A}BC + \overline{A}D$$



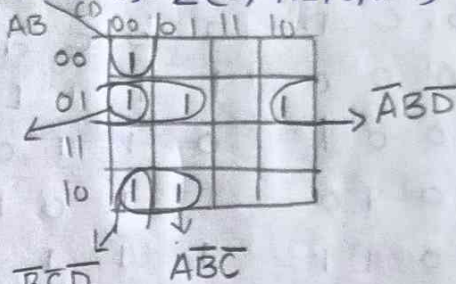
$$d(A,B,C,D) = \overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C} + \overline{A}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{D}$$

$$e(A,B,C,D) = \sum (0,2,6,8)$$



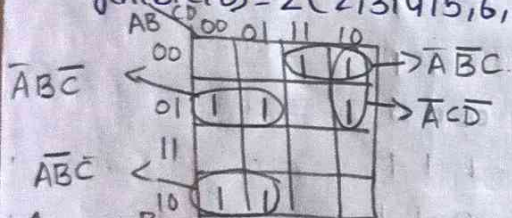
$$e = \overline{A}\overline{C}\overline{D} + \overline{B}\overline{C}\overline{D}$$

$$f(A,B,C,D) = \sum (0,4,5,6,8,9)$$

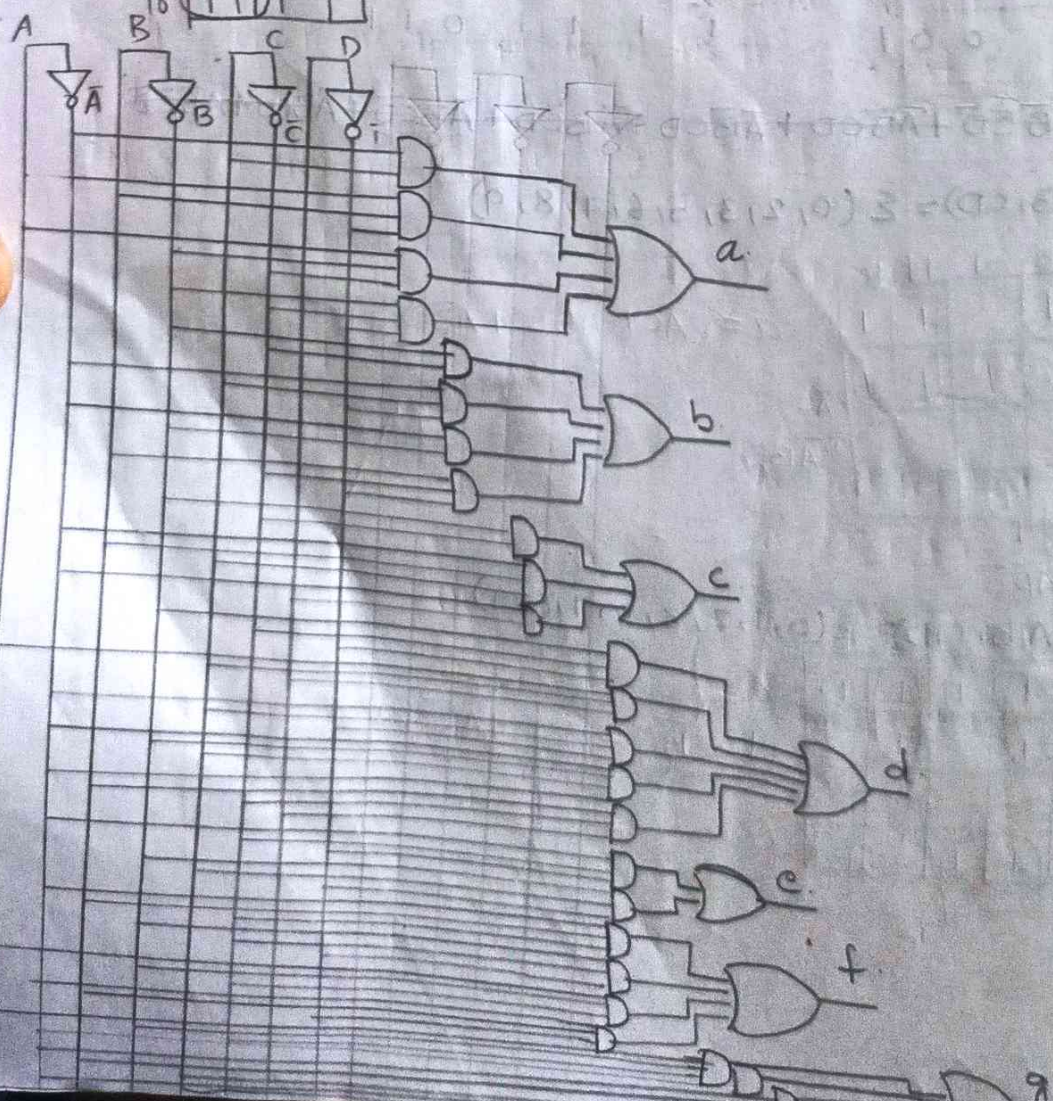


$$f = \overline{A}\overline{B}\overline{C} + \overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{D} + \overline{A}\overline{B}\overline{C}\overline{D}$$

$$g(A,B,C,D) = \sum (2,3,4,5,6,8,9)$$



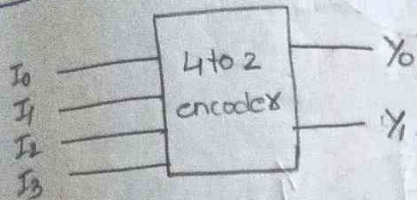
$$g = \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}\overline{D} + \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}D$$



Encoder:-

Encoder is a combinational ckt having m inputs and n outputs
Where $M \leq 2^n$

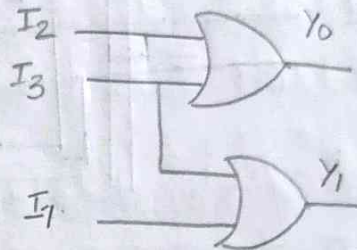
4 to 2 Line Encoder



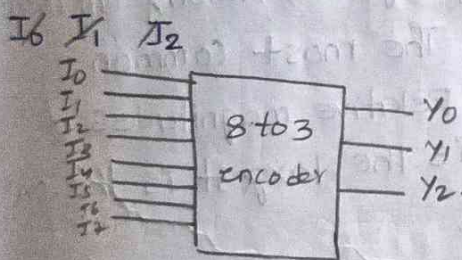
$$Y_0 = I_2 + I_3$$

$$Y_1 = I_1 + I_3$$

I_0	I_1	I_2	I_3	Y_0	Y_1
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1



8 to 3 encoder

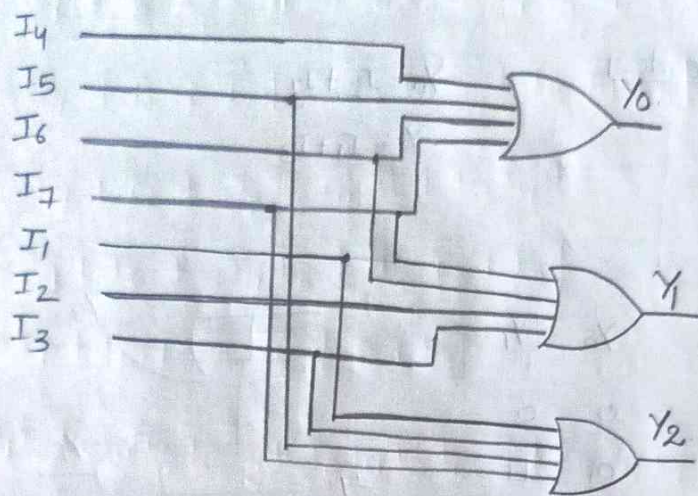


I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Y_0	Y_1	Y_2
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0	1	0
0	0	0	0	1	0	0	0	1	0	1
0	0	0	0	0	1	0	0	1	1	0
0	0	0	0	0	0	1	0	1	1	1
0	0	0	0	0	0	0	1	1	1	1

$$Y_0 = I_4 + I_5 + I_6 + I_7$$

$$Y_1 = I_2 + I_3 + I_6 + I_7$$

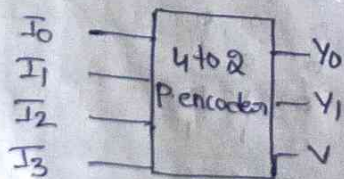
$$Y_2 = I_1 + I_3 + I_5 + I_7$$



Priority encoder:

A priority encoder is a logic ckt that responds to just 1 i/p in accordance with sum priority system. Among all these that may be simultaneously high. The most common priority system is based on the relative magnitudes of the i/p's, which ever decimal i/p is the largest is the one that is encoded.

4-to-2 priority encoder:



$$I_3 > I_2 > I_1 > I_0$$

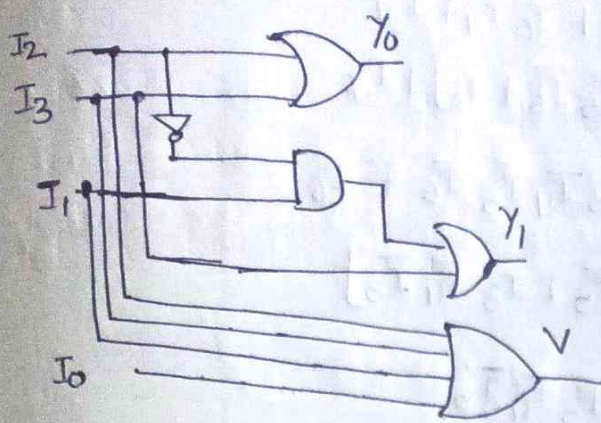
I_0	I_1	I_2	I_3	Y_0	Y_1	V
0	0	0	0	x	x	0
1	0	0	0	0	0	1
x	1	0	0	0	1	1
x	x	1	0	1	0	1
x	x	x	1	1	1	1

$$V_0 = I_0 + I_1 + I_2 + I_3$$

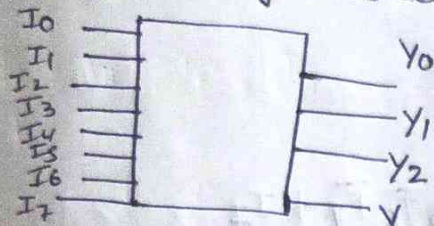
$$Y_0 = I_2 \bar{I}_3 + I_3 = I_2 + I_3$$

$$Y_1 = I_1 \bar{I}_2 \bar{I}_3 + I_3$$

$$Y_1 = I_1 \bar{I}_2 + I_3$$



to 3 priority encoder



$$V = I_0 + I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7$$

I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Y_0	Y_1	Y_2	V
0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	x	x	x	0
x	1	0	0	0	0	0	0	0	0	0	1
x	x	1	0	0	0	0	0	0	1	0	1
x	x	x	1	0	0	0	0	0	1	1	1
x	x	x	x	1	0	0	0	1	0	0	1
x	x	x	x	x	1	0	0	1	0	1	1
x	x	x	x	x	x	1	0	1	1	0	1
x	x	x	x	x	x	x	1	1	1	1	1

$$V = I_0 + I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7$$

$$Y_0 = I_4 \bar{I}_5 \bar{I}_6 \bar{I}_7 + I_5 \bar{I}_6 \bar{I}_7 + I_6 \bar{I}_7 + I_7$$

$$Y_1 = \bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 \bar{I}_7$$

$$Y_0 = \bar{I}_7 (I_4 \bar{I}_5 \bar{I}_6 + I_5 \bar{I}_6 + I_6) + I_7$$

$$Y_0 = I_7 + I_4 \bar{I}_5 \bar{I}_6 + I_5 \bar{I}_6 + I_6$$

$$Y_0 = \bar{I}_6 (I_4 \bar{I}_5 + I_5) + I_6 + I_7$$

$$Y_0 = I_6 + I_4 \bar{I}_5 + I_5 + I_7$$

$$Y_0 = I_6 + I_5 + I_4 + I_7$$

$$Y_0 = I_4 + I_5 + I_6 + I_7$$

$$I_7 + \bar{I}_7 \cdot Y = I_7 + Y$$

$$x + \bar{x}y = x + y$$

$$Y_1 = I_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 \bar{I}_7 + I_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 \bar{I}_7 + I_6 \bar{I}_7 + I_7$$

$$Y_1 = \bar{I}_7 [I_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 + I_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 + I_6] + I_7$$

$$Y_1 = I_7 + I_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 + I_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 + I_6$$

$$Y_1 = I_7 + I_6 + \bar{I}_6 [I_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 + I_3 \bar{I}_4 \bar{I}_5]$$

$$= I_7 + I_6 + I_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 + I_3 \bar{I}_4 \bar{I}_5$$

$$= I_7 + I_6 + \bar{I}_4 \bar{I}_5 [I_2 \bar{I}_3 + I_3]$$

$$= I_7 + I_6 + \bar{I}_4 \bar{I}_5 [I_2 + I_3]$$

$$Y_2 = I_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 \bar{I}_7 + I_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 \bar{I}_7 + I_5 \bar{I}_6 \bar{I}_7 + I_7$$

$$= \bar{I}_7 [I_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 + I_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 + I_5 \bar{I}_6] + I_7$$

$$= I_7 + I_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 + I_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 + I_5 \bar{I}_6$$

$$= I_7 + \bar{I}_6 [I_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 + I_3 \bar{I}_4 \bar{I}_5 + I_5]$$

$$= I_7 + \bar{I}_6 [I_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 + I_3 \bar{I}_4 \bar{I}_5 + I_5]$$

$$= I_7 + \bar{I}_6 [I_5 + \bar{I}_4 \{I_1 \bar{I}_2 \bar{I}_3\}]$$

$$= I_7 + \bar{I}_6 [I_5 + I_3 \bar{I}_4 \bar{I}_5 + I_5]$$

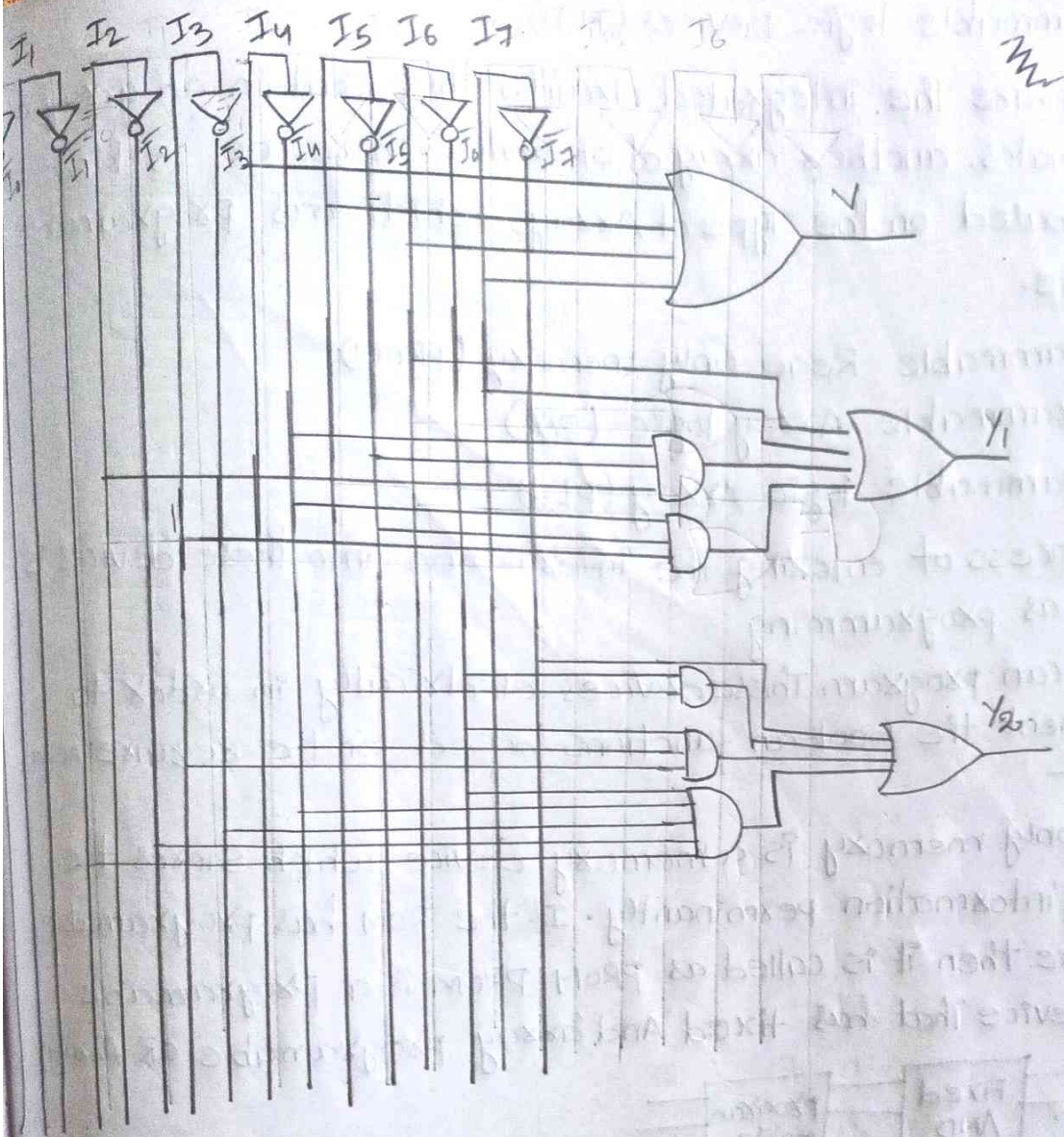
$$= I_7 + \bar{I}_6 [I_5 + I_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 + I_3 \bar{I}_4]$$

$$Y_2 = I_7 + \bar{I}_6 (I_5 + \bar{I}_4 I_3 + \bar{I}_4 \bar{I}_3 \bar{I}_2 \bar{I}_1)$$

$$Y_2 = I_7 + \bar{I}_6 (I_5 + \bar{I}_4 I_3 + \bar{I}_4 \bar{I}_3 \bar{I}_2 \bar{I}_1)$$

Decimal to BCD encoder priority

10 inputs 4 outputs



Implement the following boolean function using 7410 (NAND) and 7411 (OR) chips.

Programmable logic Devices (PLD)

PLDs are the integrated circuits they contain an array of AND Gates, another array of OR Gates. There are 3 kinds of PLDs based on the type of arrays which has programmable feature.

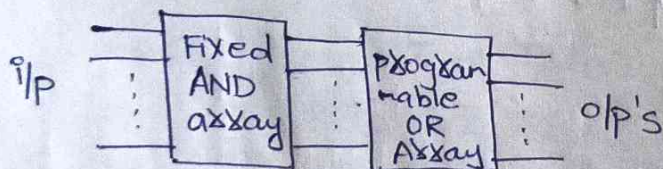
- ① Programmable Read only memory (PROM)
- ② Programmable Array logic (PAL)
- ③ Programmable logic Array (PLA)

The process of entering the information into these devices is known as programming.

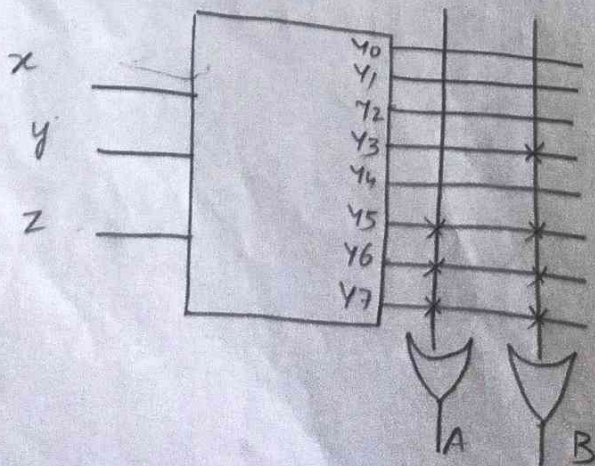
Users can program these devices electrically in order to implement the boolean functions based on the requirement.

PROM:-

Read only memory is a memory device which stores the binary information permanently. If the ROM has programmable feature then it is called as PROM. PROM is a programmable logic device that has fixed 'AND array' 'programmable OR array'.



Implement the following boolean function using PROM.
 $A(x, y, z) = \sum m(1, 5, 6, 7)$ $B(x, y, z) = \sum m(3, 5, 6, 7)$



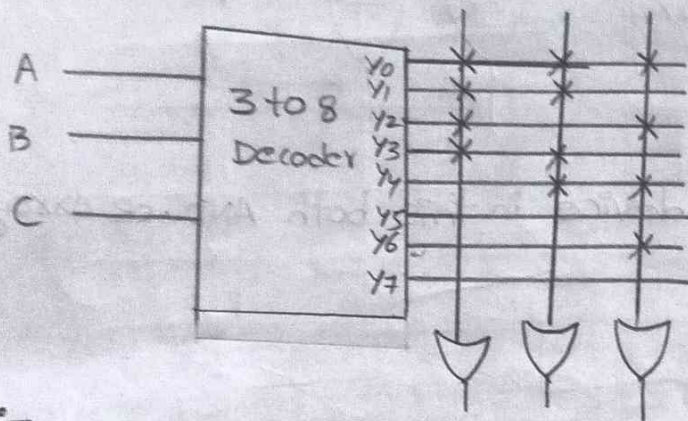
2) Design a PLD using PROM which accepts 3' i/p binary data & produce o/p as is complement of i/p

A	B	C	x	y	z
0	0	0	1	1	1
0	0	1	1	1	0
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	0	1	0
1	1	0	0	0	1
1	1	1	0	0	0

$$x(A,B,C) = \sum m(0,1,2,3)$$

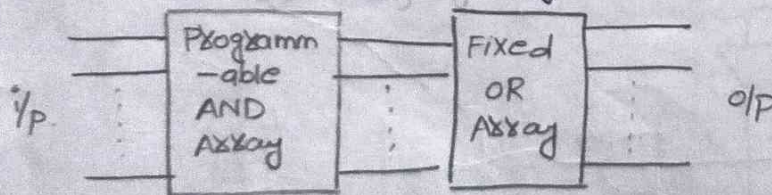
$$y(A,B,C) = \sum m(0,1,4,5)$$

$$z(A,B,C) = \sum m(0,2,4,6)$$



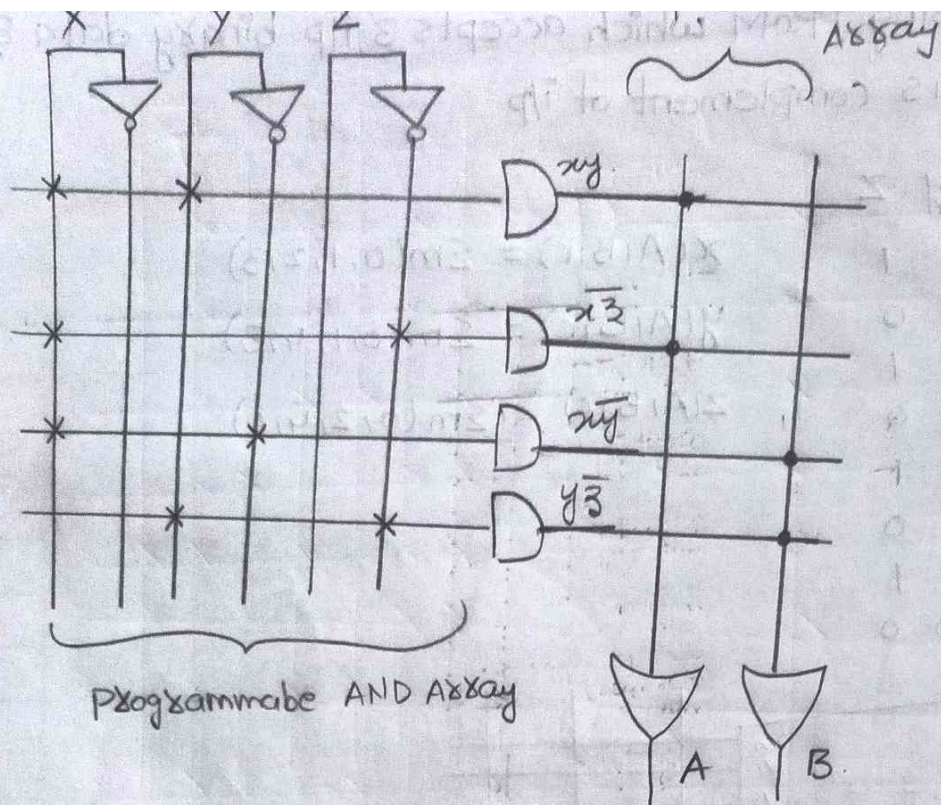
PAL:-

PAL is a programmable logic device that has programmable AND array, Fixed OR array. The Advantage of PAL is that we can generate only the required product terms of the boolean function instead of generating all the min terms.



Implement the following function using PAL.

$$A(x,y,z) = xy + x\bar{z} \quad B(x,y,z) = \bar{x}y + y\bar{z}$$



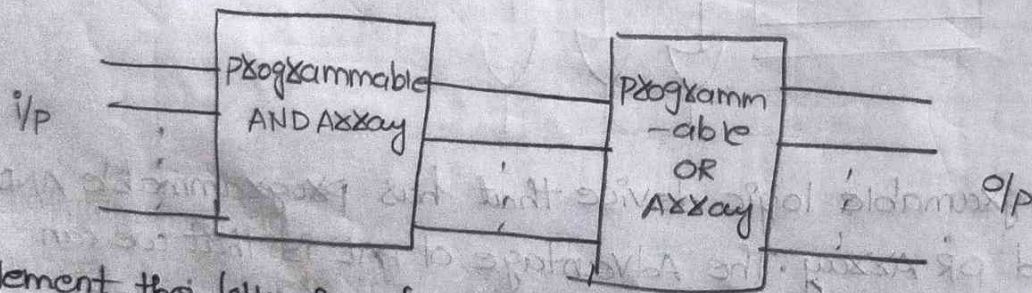
Another

$$A = \sum m(3, 5, 7)$$

011	101	111
$\bar{x}y\bar{z}$	$x\bar{y}z$	xyz

PLA:-

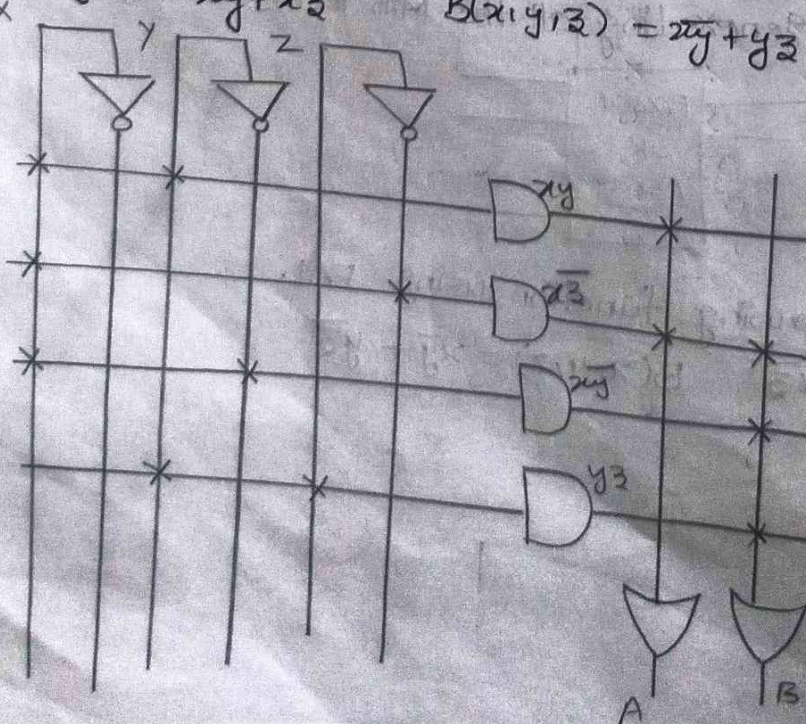
PLA is a programmable logic device in this both AND, OR array are programmable.



Implement the following function using PLA

$$A(x, y, z) = xy + \bar{x}z$$

$$B(x, y, z) = \bar{x}y + yz + \bar{x}\bar{z}$$



$$F_1(W, X, Y, Z) = m(0, 1, 3, 5, 9, 13)$$

$$F_2(W, X, Y, Z) = m(0, 2, 4, 5, 7, 9, 11, 15)$$

Implement following boolean function using PROM, PAL/PLA

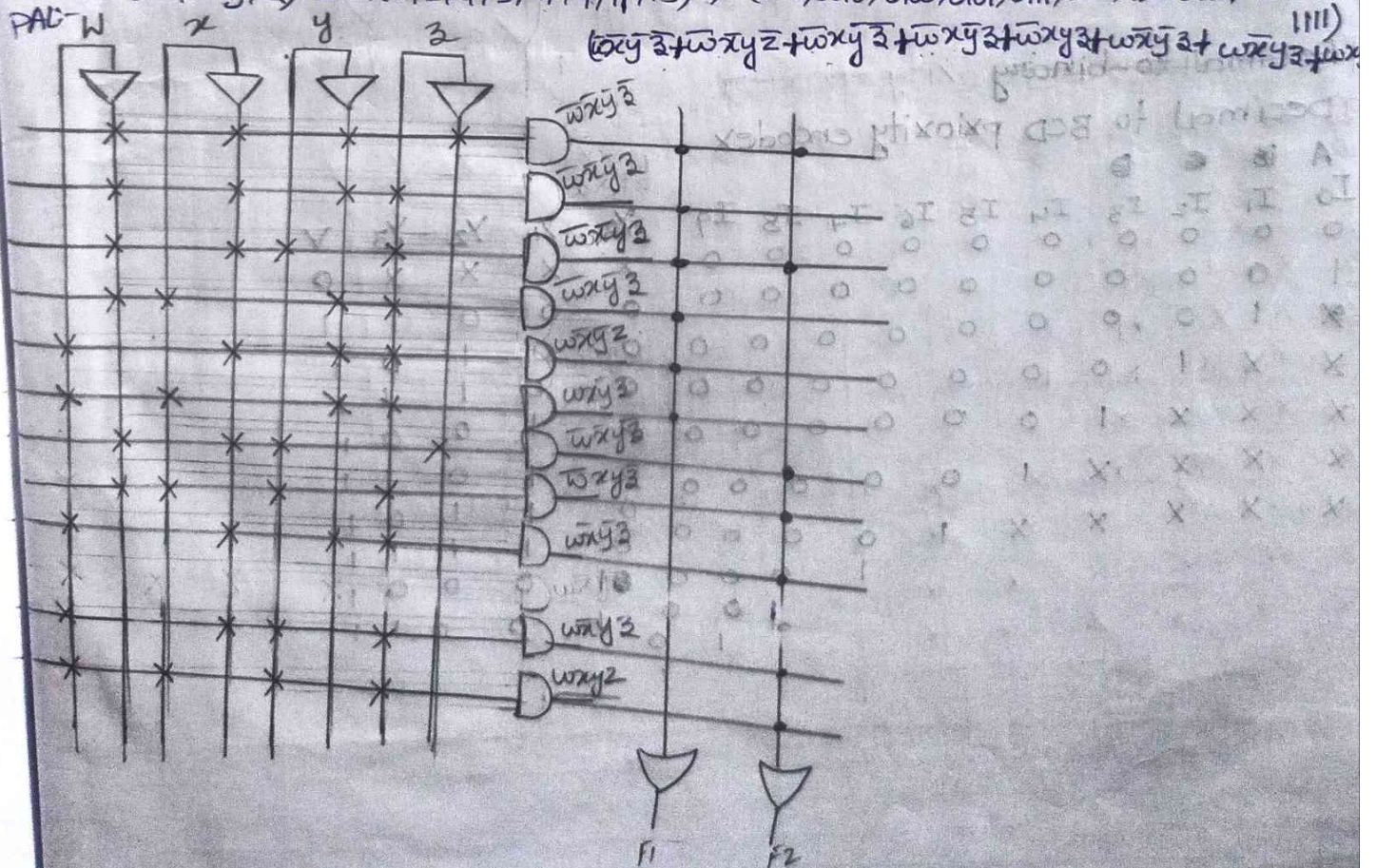


Given

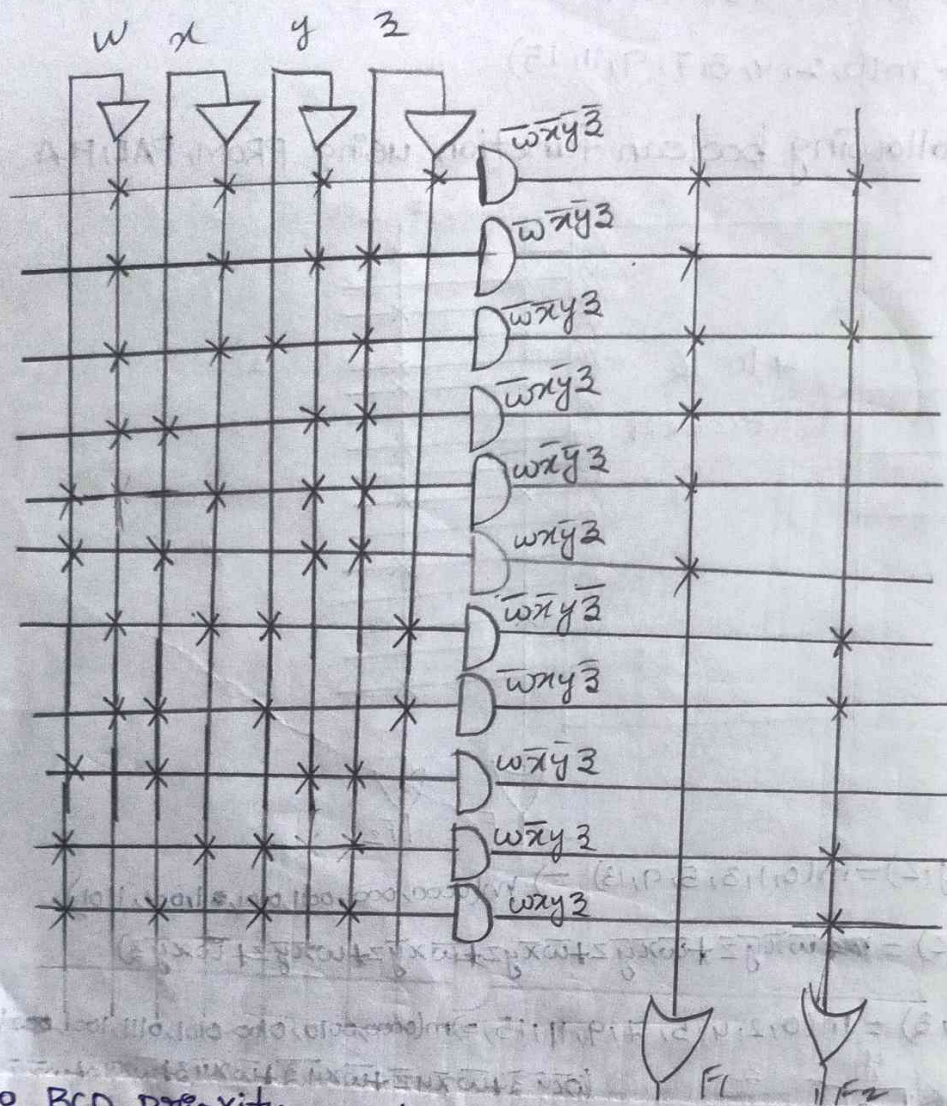
$$F_1(W, X, Y, Z) = m(0, 1, 3, 5, 9, 13) \Rightarrow m(0000, 0001, 0011, 0101, 1001, 1101)$$

$$F_1(W, X, Y, Z) = \bar{w}\bar{x}\bar{y}\bar{z} + \bar{w}\bar{x}y\bar{z} + \bar{w}x\bar{y}\bar{z} + \bar{w}xy\bar{z} + w\bar{x}\bar{y}\bar{z} + wxy\bar{z}$$

$$F_2(W, X, Y, Z) = m(0, 2, 4, 5, 7, 9, 11, 15) \Rightarrow m(0000, 0010, 0100, 0101, 0111, 1001, 1011, 1111)$$



PLA:-



Decimal to BCD parity encoder

I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	Y_0	Y_1	Y_2	Y_3	V
0	0	0	0	0	0	0	0	0	0	x	x	x	x	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
x	1	0	0	0	0	0	0	0	0	0	0	0	1	1
x	x	1	0	0	0	0	0	0	0	0	0	1	0	1
x	x	x	0	1	0	0	0	0	0	0	0	1	1	1
x	x	x	x	1	0	0	0	0	0	0	1	0	0	1
x	x	x	x	x	1	0	0	0	0	0	1	0	1	1
x	x	x	x	x	x	1	0	0	0	0	1	1	0	1
x	x	x	x	x	x	x	1	0	0	0	1	1	1	1
x	x	x	x	x	x	x	x	1	0	1	0	0	0	1
x	x	x	x	x	x	x	x	x	1	1	0	0	1	1

$$V = I_0 + I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7 + I_8 + I_9$$

$$Y_0 = I_6 \bar{I}_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5$$

$$Y_0 = I_8 \bar{I}_9 + I_9$$

$$Y_0 = I_8 + I_9$$

$$Y_1 = \bar{I}_4 \bar{I}_5 \bar{I}_6 \bar{I}_7 \bar{I}_8 \bar{I}_9 + I_5 \bar{I}_6 \bar{I}_7 \bar{I}_8 \bar{I}_9 + I_6 \bar{I}_7 \bar{I}_8 \bar{I}_9 + I_7 \bar{I}_8 \bar{I}_9$$

$$Y_1 = (I_4 \bar{I}_5 + I_5) \bar{I}_6 \bar{I}_7 \bar{I}_8 \bar{I}_9 + (I_6 \bar{I}_7 + I_7) \bar{I}_8 \bar{I}_9$$

$$Y_1 = (I_4 + I_5) \bar{I}_6 \bar{I}_7 \bar{I}_8 \bar{I}_9 + (I_6 + I_7) \bar{I}_8 \bar{I}_9$$

$$Y_1 = I_4 \bar{I}_6 \bar{I}_7 \bar{I}_8 \bar{I}_9 + I_5 \bar{I}_6 \bar{I}_7 \bar{I}_8 \bar{I}_9 + I_6 \bar{I}_8 \bar{I}_9 + I_7 \bar{I}_8 \bar{I}_9$$

$$Y_2 = I_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 \bar{I}_7 \bar{I}_8 \bar{I}_9 + I_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 \bar{I}_7 \bar{I}_8 \bar{I}_9 + I_6 \bar{I}_7 \bar{I}_8 \bar{I}_9 + I_7 \bar{I}_8 \bar{I}_9$$

$$Y_2 = (I_2 \bar{I}_3 + I_3) \bar{I}_4 \bar{I}_5 \bar{I}_6 \bar{I}_7 \bar{I}_8 \bar{I}_9 + (I_6 \bar{I}_7 + I_7) \bar{I}_8 \bar{I}_9$$

$$Y_2 = (I_2 + I_3) \bar{I}_4 \bar{I}_5 \bar{I}_6 \bar{I}_7 \bar{I}_8 \bar{I}_9 + (I_6 + I_7) \bar{I}_8 \bar{I}_9$$

$$Y_2 = I_2 \bar{I}_4 \bar{I}_5 \bar{I}_6 \bar{I}_7 \bar{I}_8 \bar{I}_9 + I_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 \bar{I}_7 \bar{I}_8 \bar{I}_9 + I_6 \bar{I}_8 \bar{I}_9 + I_7 \bar{I}_8 \bar{I}_9$$

$$Y_3 = I_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 \bar{I}_7 \bar{I}_8 \bar{I}_9 + I_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 \bar{I}_7 \bar{I}_8 \bar{I}_9 + I_5 \bar{I}_6 \bar{I}_7 \bar{I}_8 \bar{I}_9 + I_7 \bar{I}_8 \bar{I}_9 + I_9$$

$$Y_3 = I_1 \bar{I}_2 \bar{I}_3 \bar{I}_9 + I_7 \bar{I}_8 + I_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5$$

