

CHAPTER

7

SEQUENTIAL CIRCUITS-II

7.1 FINITE STATE MACHINE

The most general model of a sequential circuit has inputs, outputs and internal states. A sequential circuit is referred to as a finite state machine (FSM). A finite state machine is an abstract model that describes the synchronous sequential machine. Since in a sequential circuit the output depends on the present input as well as on the past inputs, i.e. on the past histories and since a machine might have an infinite varieties of possible histories, it would need an infinite capacity for storing them. Since it is impossible to implement machines which have infinite storage capabilities, we consider only finite state machines. Finite state machines are sequential circuits whose past histories can affect their future behaviour in only a finite number of ways, i.e. they are machines with a fixed number of states. These machines can distinguish among a finite number of classes of input histories. These classes of input histories are referred to as the internal states of the machine. Every finite state machine therefore contains a finite number of memory devices.

Figure 7.1 shows the block diagram of a finite state model. $x_1, x_2, \dots, x_l$ are inputs. $z_1, z_2, \dots, z_m$ are outputs. $y_1, y_2, \dots, y_k$ are state variables, and $Y_1, Y_2, \dots, Y_k$ represent the next state.

7.1.1 Capabilities and Limitations of Finite State Machines

1. Periodic sequence of finite states: With n -state machine, we can generate a periodic sequence of n states or smaller than n states. For example, in a 6-state machine, we can have a maximum

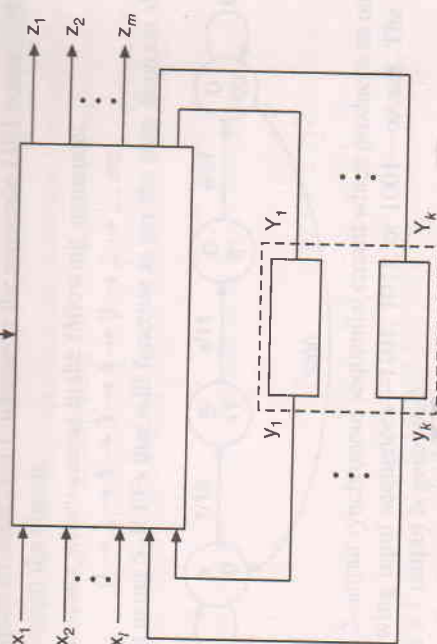


Figure 7.1 Block diagram of a finite state model.

2. No infinite sequence: Consider an infinite sequence such that the output is 1 when and only, when the number of inputs received so far is equal to $P(P+1)/2$ for $P = 1, 2, 3, \dots$, i.e. the desired input-output sequence has the following form:

Input:	x	x	x	x	x	x	x	x	x	x
Output:	1	0	1	0	0	1	0	0	1	0

Such an infinite sequence cannot be produced by a finite state machine.

3. Limited memory: The finite state machine has a limited memory and due to limited memory it cannot produce certain outputs. Consider a binary multiplier circuit for multiplying two arbitrarily large binary numbers. If we implement this with a finite state machine capable of performing serial multiplication, we can find that it is not possible to multiply certain numbers. Such a limitation does occur due to the limited memory available to the machine. This memory is not sufficient to store arbitrarily large partial products resulted during multiplication.

Finite state machines are of two types. They differ in the way the output is generated. They are:

1. Mealy type model: In this model, the output is a function of the present state and the present input.

2. Moore type model: In this model, the output is a function of the present state only.

7.2 MATHEMATICAL REPRESENTATION OF SYNCHRONOUS SEQUENTIAL MACHINE

We know that the next state of a sequential machine depends upon the present state and the present input. The relation between the present state $S(t)$, present input $x(t)$, and next state $S(t + 1)$ can be given as

$$S(t+1) = f\{S(t), x(t)\}$$

input x , and an output z . Since the D input of a flip-flop determines the value of the next state, the state equations for the model can be written as

$$y_1(t+1) = y_1(t)x(t) + y_2(t)x(t)$$

$$y_2(t+1) = \bar{y}_1(t)x(t)$$

and the output equation is

$$z(t) = \{y_1(t) + y_2(t)\} \bar{x}(t)$$

where $y(t+1)$ is the next state of the flip-flop one clock edge later, $x(t)$ is the present input, and $z(t)$ is the present output. If $y_1(t+1)$ and $y_2(t+1)$ are represented by $Y_1(t)$ and $Y_2(t)$, in more compact form, the equations are

$$Y_1(t+1) = Y_1 = Y_1x + Y_2x$$

$$Y_2(t+1) = Y_2 = \bar{Y}_1x$$

$$z = (Y_1 + Y_2)\bar{x}$$

The state table of the Mealy model based on the above state equations and output equation is shown in Figure 7.3a. The state diagram based on the state table is shown in Figure 7.3b.

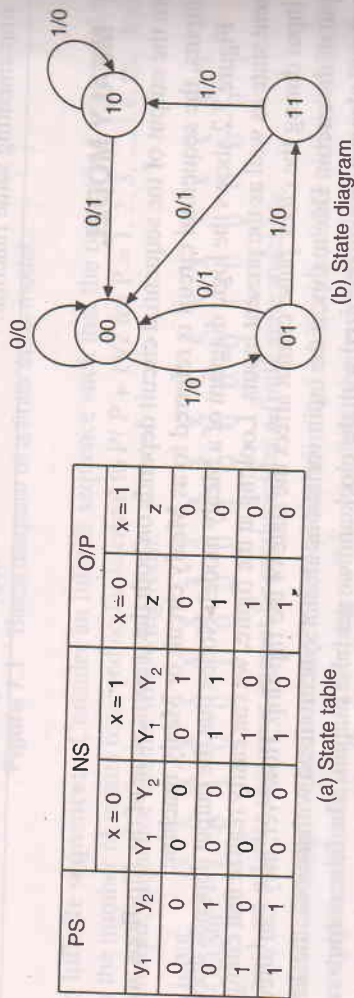


Figure 7.3 Mealy model.

In general form, the Mealy circuit can be represented with its block schematic as shown in Figure 7.4.

7.4 MOORE MODEL

As mentioned earlier, when the output of the sequential circuit depends only on the present state of the flip-flop, the sequential circuit is referred to as the Moore circuit or the Moore machine. Figure 7.5 shows the logic diagram of a Moore circuit.

Notice that the output depends only on the present state. It does not depend upon the input at all. The input is used only to determine the inputs of flip-flops. It is not used to determine the output. The circuit shown has two T flip-flops, one input x , and one output z . It can be described algebraically by two input equations and an output equation.

$$T_1 = y_2x$$

$$T_2 = x$$

$$z = y_1y_2$$