

⇒ Sequential Ckts :-

1) Flip Flops

2) Registers

3) Counters.

0	1	2	3
1	1	1	1

⇒ Flip Flops :-

✓ Basics

✓ SR Latch $\begin{cases} \text{Nand} \\ \text{Nor} \end{cases}$

✓ SR FF

✓ JK FF

✓ D FF

✓ T FF

Truth Table

characteristic Table → characteristic Equation

Excitation Table.

	1	
1	1	1
1	1	1
1	1	1

M-S FF.

conversion from one FF to other.

→ Flip Flop is a basic memory element

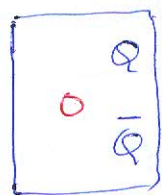
→ a Flip Flop can store one bit.

→ Flip Flop have two o/p's which are complementary to each other.

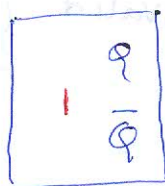
$$Y^0 (P\bar{X} + \bar{P}X) + (P+X) (PX + \bar{P}\bar{X}) =$$

$$= \bar{P}\bar{X} + P\bar{X} + P\bar{X} + \bar{P}\bar{X} =$$

→ Flip Flops have two stable states hence it is known as Bistable multivibrator.

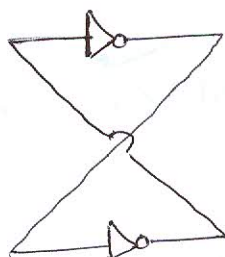
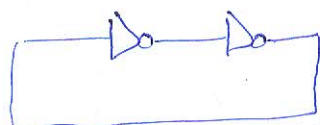


↓
one stable



↓
2nd stable

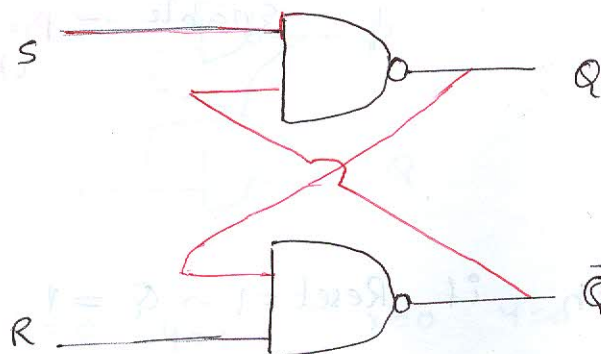
→



Latch

⇒ SR Latch using Nand :-

→

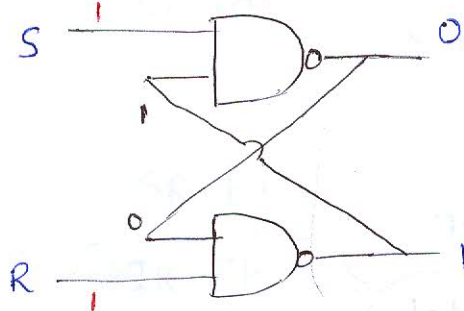


⇒ Truth Table :-

<u>S</u>	<u>R</u>	<u>Q</u>
0	0	Invalid ($Q = \bar{Q} = 1$)
0	1	1
1	0	0
1	1	Previous state

$\left(\begin{array}{l} Q=0, \bar{Q}=1 \\ \text{(or)} \\ Q=1, \bar{Q}=0 \end{array} \right)$

→



⇒ Nand Latch :-

<u>S</u>	<u>R</u>	<u>Q</u>
0	0	Invalid
0	1	→ 1
1	0	→ 0
1	1	Previous state

For Nand

0 - disable - invalid

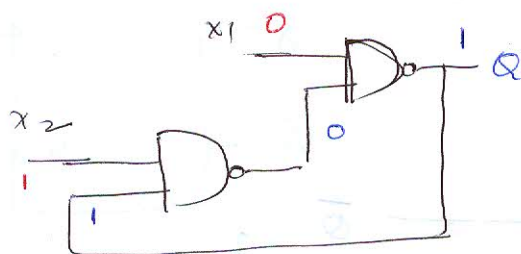
1 - enable - previous state.

→

in SR Nand Latch. if Reset = 1 → $Q = 1$

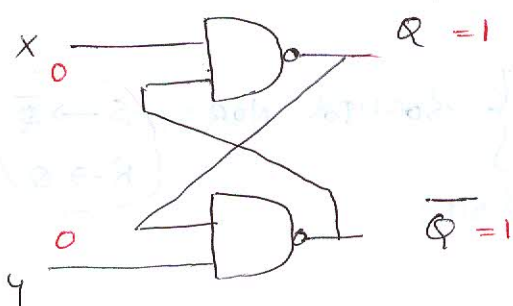
set = 1 → $Q = 0$

Q) → in the ckt shown in fig $x_1=0, x_2=1$ then O/P Q



✓ b) logic 1 a) logic 0

Q2



if $x=0, y=0$ then O/P

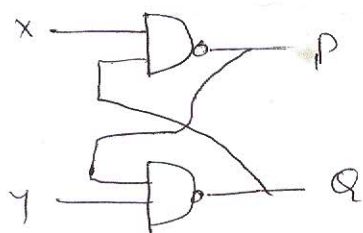
Q will be

✓ a) logic 0 b) logic 1 c) Previous state d) Indetermin.

→ Indeterminate - you can not find out.

✓ invalid - O/P is not valid.

Q3



$x=0, y=1$

$P=1, Q=0$

$x=0, y=0$

$P=1, Q=1$

$x=1, y=1$

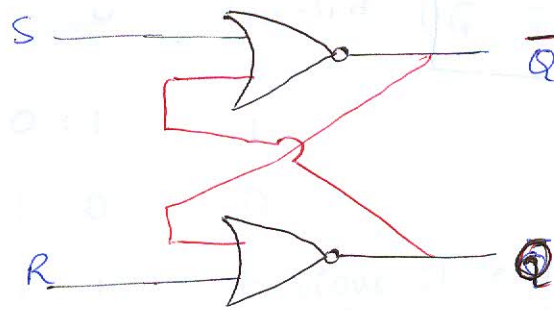
$P=0, Q=1$ ✓

(or)

$P=1, Q=0$ ✓

(indeterminate)

⇒ SR Latch using NOR gates :-



Enable & disable are different for NOR and Nand

→ Enable - NOR 0 Nand 1 } So For NOR. $S \rightarrow \bar{Q}$
 $R \rightarrow Q$
Disable - 1 0

→

<u>S</u>	<u>R</u>	<u>Q</u>
0	0	previous state
0	1	0
1	0	1
1	1	Invalid

 [$Q=0, \bar{Q}=1$ (or) $Q=1, \bar{Q}=0$]
[$Q=\bar{Q}=0$]

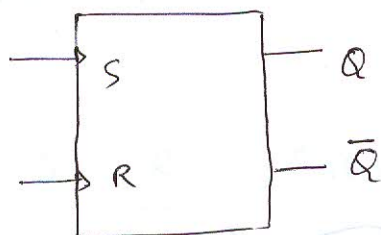
*** ⇒ NOR Latch :-

<u>S</u>	<u>R</u>	<u>Q</u>
0	0	Previous state
0	1	0
1	0	1
1	1	Invalid

Reset

1 → 0 ✓
0 → 1 ✓

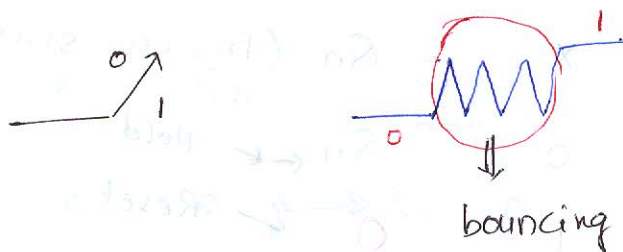
⇒ SR Latch:-



⇒ SR Latch - is used in memory storage as a memory element.

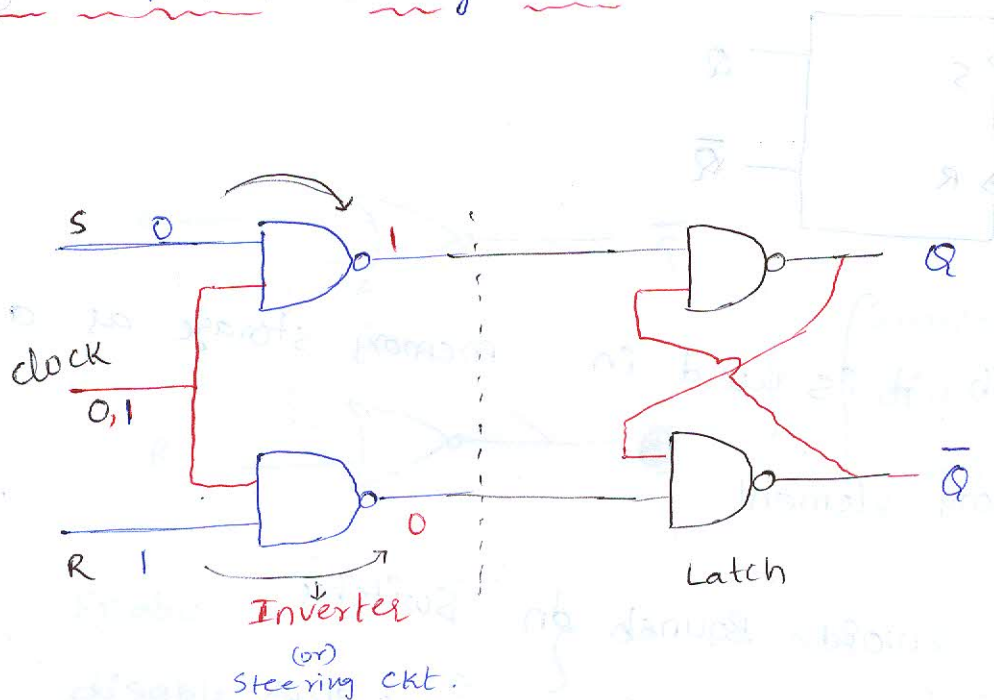
→ To avoid Bounce on Switches

(Debounce Switch)



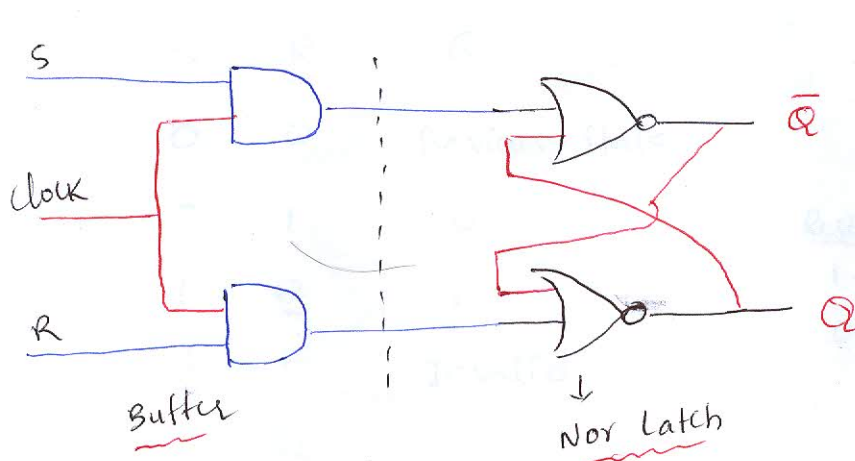
→ SR Latch internal ckt consists of Nand and NOR So two truth Tables will have for SR Latch.

⇒ SR Flip flop using Nand :-



<u>clock</u>	<u>S</u>	<u>R</u>	<u>Q_{n+1}</u>
0	X	X	Q_n (Previous state)
1	0	0	Q_n ← Hold
1	0	1	0 ← Reset
1	1	0	1 ← Set
1	1	1	Invalid (or) unused

⇒ SR Flip flop using NOR :-



⇒ SR Flip Flop :-

<u>S</u>	<u>R</u>	<u>Q_{n+1}</u>
0	0	Q _n ← Hold
0	1	0 ← Reset
1	0	1 ← Set
1	1	unused

⇒ characteristic Truth Table of SR Flip Flop :-

<u>S</u>	<u>R</u>	<u>Q_n</u>	<u>Q_{n+1}</u>
0	0	0	Q _n = 0
0	0	1	Q _n = 1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

⇒ Characteristic Equation :-

$$\rightarrow Q_{n+1} = \sum m(1, 4, 5) + \sum d(6, 7)$$

$$\rightarrow Q_{n+1}(S, R, Q_n) = \sum m(1, 4, 5) + \sum d(6, 7)$$



$S \backslash RQ_n$	$\bar{R}\bar{Q}_n$	$\bar{R}Q_n$	RQ_n	$R\bar{Q}_n$
$\bar{S}$		1		
S	1	1	X	X

$$\boxed{Q_{n+1} = S + \bar{R}Q_n} \quad \text{and} \quad \underline{S = R \neq 1}$$

⇒ Excitation Table :-

<u>Q_n</u>	<u>Q_{n+1}</u>	<u>S</u>	<u>R</u>
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

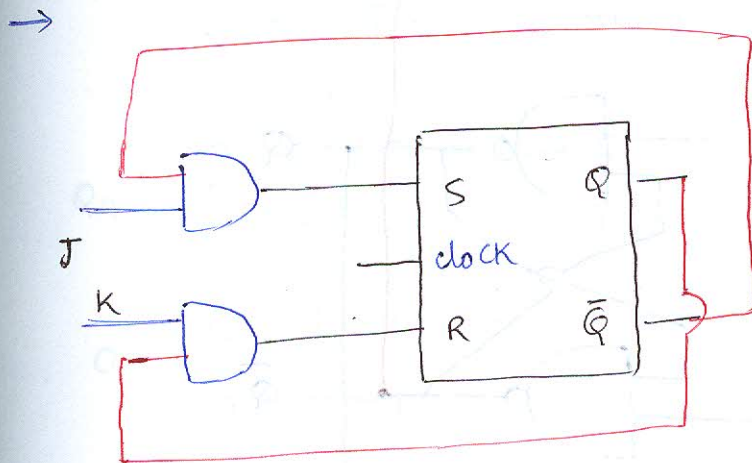
→ disadvantage of SR flip flop is when both

S and R i/p's are 1 then o/p is invalid

hence $S=1$ and $R=1$ is an unused state

To avoid this JK flip flop is used.

⇒ JK Flip Flop :-



$$S = J\bar{Q}$$

$$R = KQ$$

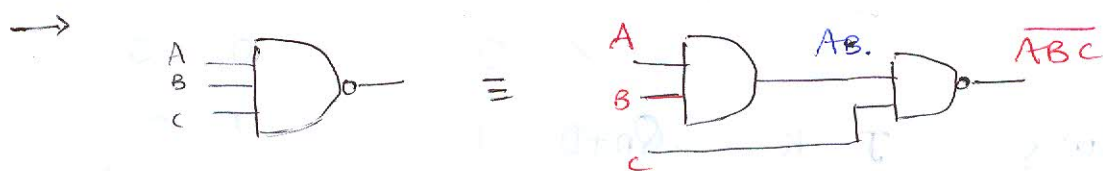
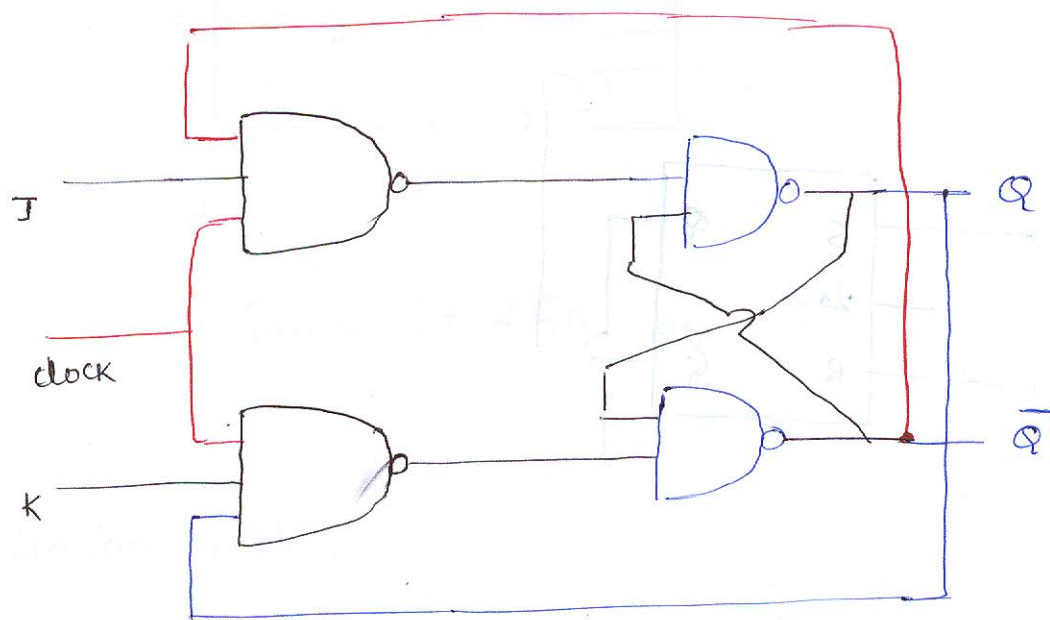
→

<u>clock</u>	<u>J</u>	<u>K</u>	<u>Q_{n+1}</u>	
0	x	x	Q _n	
1	0	0	Q _n	← Hold
1	0	1	0	← Reset
1	1	0	1	← set
1	1	1	$\bar{Q}_n$	← Toggle state

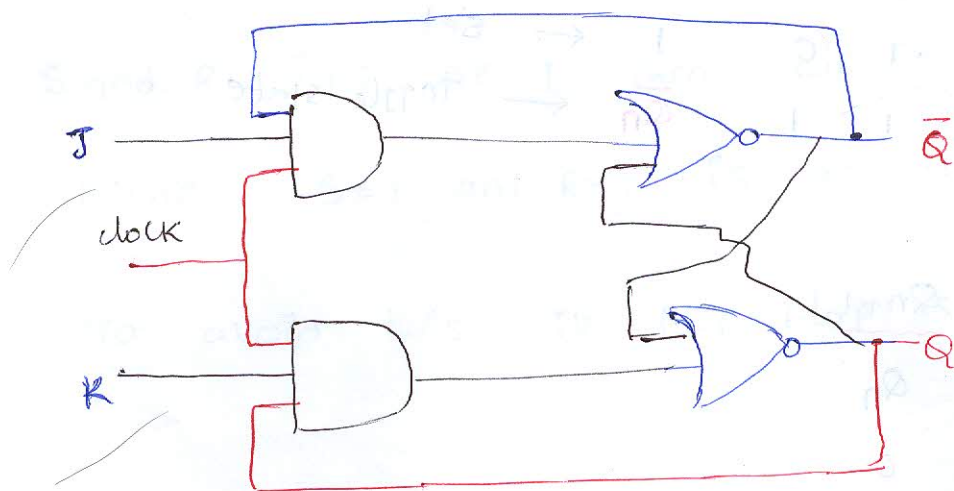
→

<u>J</u>	<u>K</u>	<u>Q_{n+1}</u>
0	0	Q _n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

⇒ JK Flip Flop using Nand gates :-



⇒ JK Flip Flop using Nor gates :-



⇒ Characteristic Table:-

	<u>J</u>	<u>K</u>	<u>Q_n</u>	<u>Q_{n+1}</u>
Q _n	0	0	0	0
	0	0	1	1
0	0	1	0	0
	0	1	1	0
1	1	0	0	1
	1	0	1	1
$\bar{Q}_n$	1	1	0	1
	1	1	1	0

→ $Q_{n+1}(J, K, Q_n) = \Sigma(1, 4, 5, 6)$

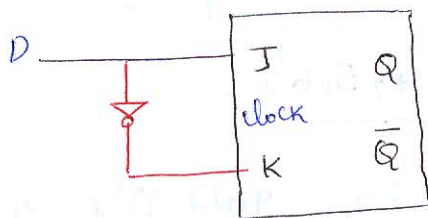
J	KQ _n			
	$\bar{K}\bar{Q}_n$	$\bar{K}Q_n$	KQ_n	$K\bar{Q}_n$
$\bar{J}$		1		
J	1	1		$\bar{1}$

$Q_{n+1} = \bar{K}Q_n + J\bar{Q}_n$

⇒ Excitation Table :-

<u>Q_n</u>	<u>Q_{n+1}</u>	<u>J</u>	<u>K</u>
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

⇒ D Flip Flop :-



$J = D$ $K = \bar{D}$

→

<u>clock</u>	<u>D</u>	<u>Q_{n+1}</u>
0	X	Q_n
1	0	0
1	1	1

⇒ Characteristic Table :-

→ <u>D</u>	<u>Q_n</u>	<u>Q_{n+1}</u>
0	0	0
0	1	0
1	0	1
1	1	1



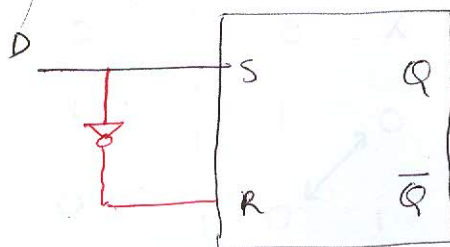
$$\boxed{Q_{n+1} = D}$$

→ D Flip Flop is known as Transparent Latch.

⇒ Excitation Table :-

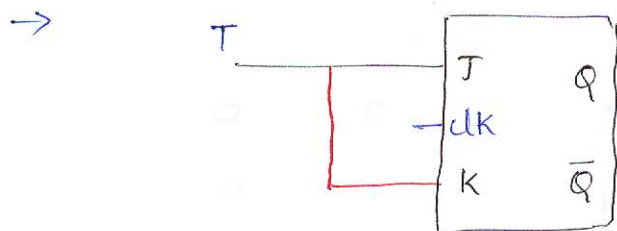
→ <u>Q_n</u>	<u>Q_{n+1}</u>	<u>D</u>
0	0	0
0	1	1
1	0	0
1	1	1

⇒



$$\underline{S = D} \quad \underline{R = \bar{D}}$$

⇒ T Flip Flop :-



$$\boxed{J = K = T}$$

→

<u>clock</u>	<u>T</u>	<u>Q_{n+1}</u>
0	<u>X</u>	Q _n
1	0	Q _n
1	1	$\bar{Q}_n$

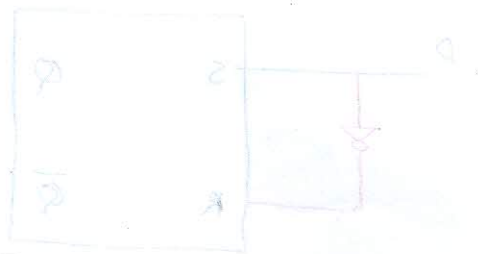
⇒

<u>T</u>	<u>Q_{n+1}</u>
0	Q _n
1	$\bar{Q}_n$

⇒ characteristic Table :-

→

<u>T</u>	<u>Q_n</u>	<u>Q_{n+1}</u>
0	0	0
0	1	1
1	0	1
1	1	0



$$\begin{aligned} Q_{n+1} &= \bar{T}Q_n + T\bar{Q}_n \\ &= T \oplus Q_n \end{aligned}$$

⇒ Excitation Table :-

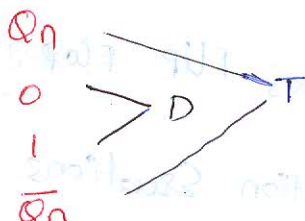
→ <u>Q_n</u>	<u>Q_{n+1}</u>	<u>T</u>
0	0	0
0	1	1
1	0	1
1	1	0

**

$$\boxed{T = Q_{n+1} \oplus Q_n}$$

→

	<u>J</u>	<u>K</u>	<u>Q_{n+1}</u>
SR	0	0	Q_n
	0	1	0
	1	0	1
	1	1	$\bar{Q}_n$



→

<u>Q_n</u>	<u>Q_{n+1}</u>	<u>S</u>	<u>R</u>	<u>J</u>	<u>K</u>	<u>D</u>	<u>T</u>
0	0	0	x	0	x	0	0
0	1	1	0	1	x	1	1
1	0	0	1	x	1	0	1
1	1	x	0	x	0	1	0

⇒ characteristic equation :-

$$\rightarrow Q_{n+1} = S + \bar{R} Q_n$$

$$\rightarrow Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

$$\rightarrow Q_{n+1} = D$$

$$\rightarrow Q_{n+1} = T \oplus Q_n$$

27/6/11.

⇒ conversion from one FF to other :-

→ ① Fill required flip flop characteristic Table

→ ② Fill available Flip flop excitation table

→ ③ write excitation Equations.

⇒ ④ minimize

⇒ ⑤ implement.

⇒ J-K Flip Flop to D-Flip Flop :-

↓
(available)

↓
(required)

Excitation Table (J-K)

Step 1 :-

(Characteristic Table - D)

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

J	K
0	X
X	1
1	X
X	0

→ $J = \underline{D}$

	Q_n	$\bar{Q}_n$
D	0	1
$\bar{D}$	1	0

→

	Q_n	$\bar{Q}_n$
D	1	0
$\bar{D}$	0	1

$K = \bar{D}$

⇒ JK to SR Flip Flop:-

⇒ characteristic Table S-R:-

<u>S</u>	<u>R</u>	<u>Q_n</u>	<u>Q_{n+1}</u>
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

Excitation Table J-K

<u>J</u>	<u>K</u>
0	X
X	0
0	X
X	1
1	X
X	0
X	X
X	X

step 3:-

⇒ J Equation :-

S	R	Q	Q̄
0	1	1	0
1	1	1	1

$$\underline{J = S}$$

⇒ K Equation :-

S	R	Q	Q̄
1	0	1	1
1	0	1	1

$$\underline{K = R}$$

⇒ S-R to JK FF :-

$$S = J\bar{Q}$$

$$R = KQ$$

⇒ SR to D FF :-

$$S = D$$

$$R = \bar{D}$$

⇒ SR to T FF :-

$$S = T\bar{Q}$$

$$R = TQ$$

in JK to T

$$J = T \Rightarrow S = T\bar{Q}$$

$$K = T \Rightarrow R = TQ$$

⇒ D to S.R Flip Flop :-

$$Q_{n+1} = D$$

$$Q_{n+1} = S + \bar{R}Q_n$$

$$\boxed{D = S + \bar{R}Q_n}$$

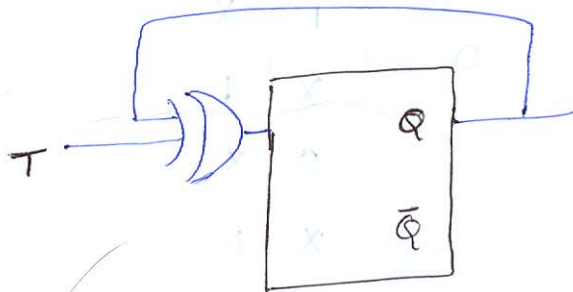
⇒ D to JK F.F :-

$$D = J\bar{Q} + \bar{K}Q$$

$$\left\{ \begin{array}{l} Q_{n+1} = D \\ Q_{n+1} = J\bar{Q} + \bar{K}Q \end{array} \right\} \begin{array}{l} \rightarrow \text{for D} \\ \rightarrow \text{for J.K} \end{array}$$

⇒ D to T :-

$$D = T \oplus Q_n$$



$$\left\{ \begin{array}{l} Q_{n+1} = D \\ Q_{n+1} = T\bar{Q} + Q\bar{T} \end{array} \right\}$$

⇒ T to JK FF :-

$$\underline{T = J\bar{Q} + KQ}$$

⇒ TO to SR FF:-

$$T = S\bar{Q} + RQ$$

⇒ T to D FF:-

$$T = D \oplus Q$$

$$\left\{ \begin{array}{l} D = T \oplus Q \\ T = D \oplus Q \end{array} \right.$$

Q) TO design XY Flip Flop using JK Flip Flop where

XY Flip Flop truth table is given below.

X	Y	Q_{n+1}
0	0	$\bar{Q}_n$
0	1	0
1	0	1
1	1	Q_n

what is J and K.

Sol:-

Characteristic SE XY

X	Y	Q_n	Q_{n+1}
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Excitation Table:-

J	K
1	X
X	1
0	X
X	1
1	X
X	0
0	X
X	0

J

Q_n

n

1	x	x	
1	x	x	

$$J = \bar{y}$$

K

Q_n

n

x	1	1	x
x			x

$$K = \bar{x}$$

Q)

Design AB FF using JK FF.

<u>A</u>	<u>B</u>	<u>Q_{nt+1}</u>
0	0	1
0	1	Q_n
1	0	$\bar{Q}_n$
1	1	0

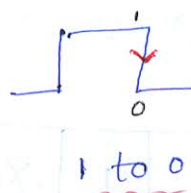
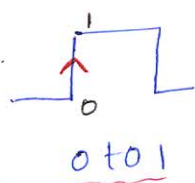
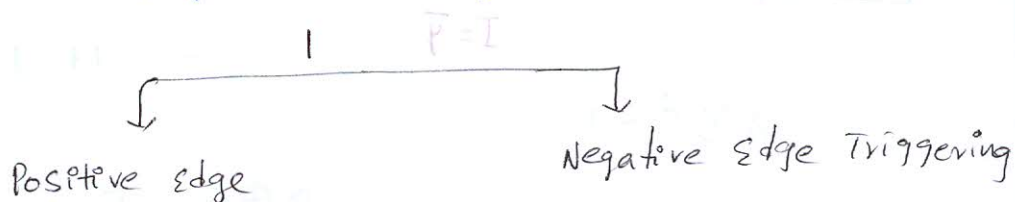
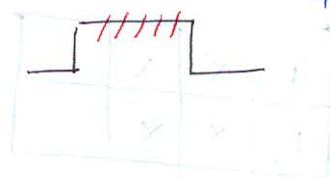


$$t_{setup} < t_{hold} < T_{clk}$$

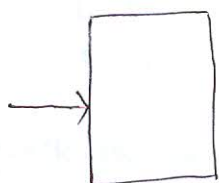
⇒ Triggering :-

- 1) Level Triggering
- 2) Edge Triggering

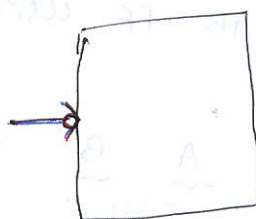
(o/p gets change in this position)



→ Level Triggering may be asynchronous o/p can not be exactly determined.

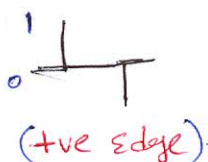
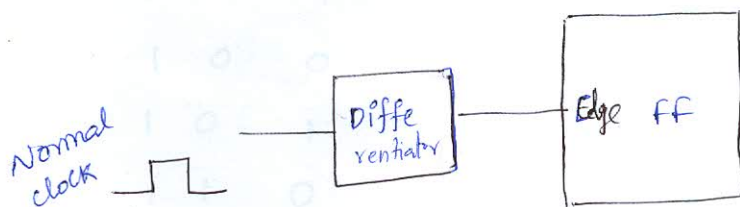


+ve edge

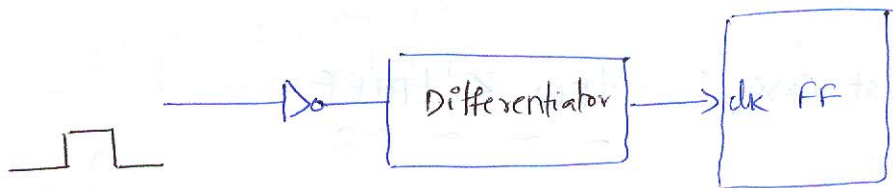


-ve Edge

→ Conversion of clock to edge triggered :-

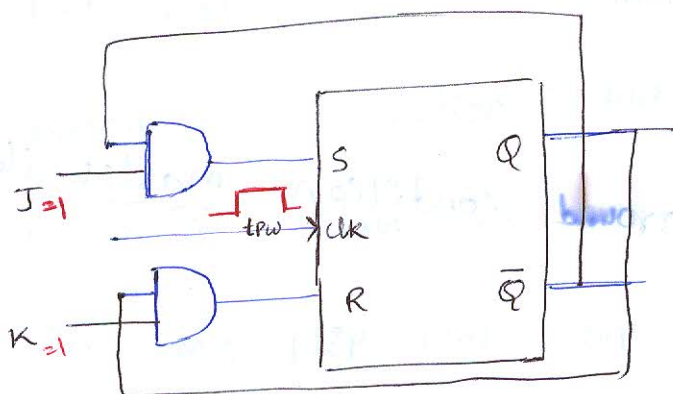


→



⇒

Race-around condition :-



→ where $t_{pd\ FF}$ = Propagation delay of FF

t_{pw} = Pulse width of clock

→ In JK Flip Flop race around condition occurs when J and K inputs are 1. and $t_{pd\ FF} < t_{pw}$

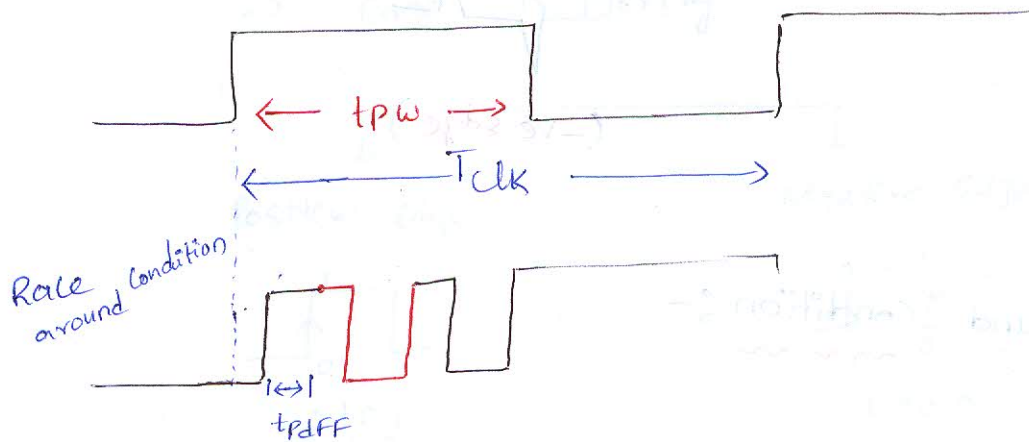
→ During race around o/p will change many times in single clock pulse

→ To avoid Race condition is

$$\underline{t_{pw} < t_{pd\ FF} < T_{clk}}$$

→ worst case

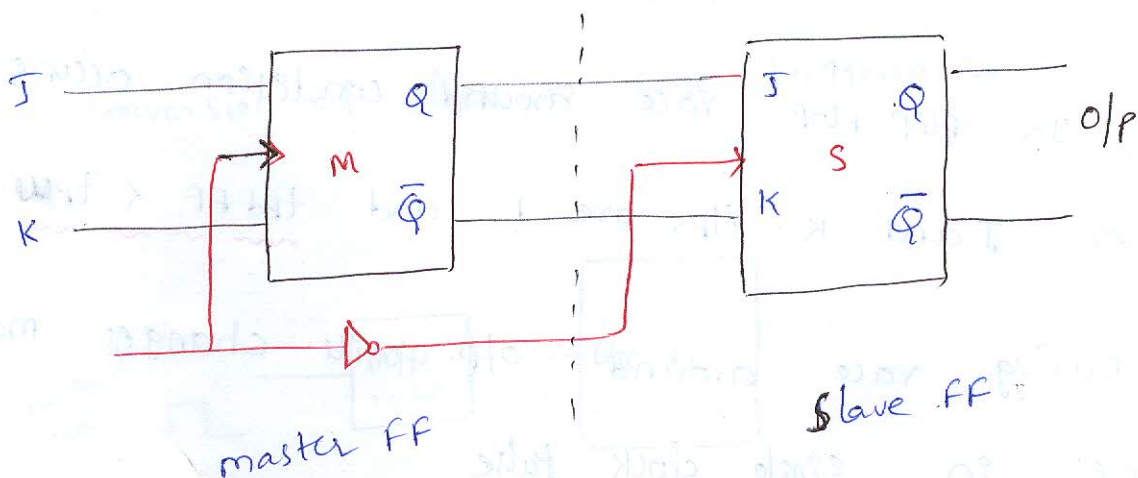
$$\underline{tpw \leq t_{pdFF}}$$



when $J=1$
 $K=1$ } Kept constant.

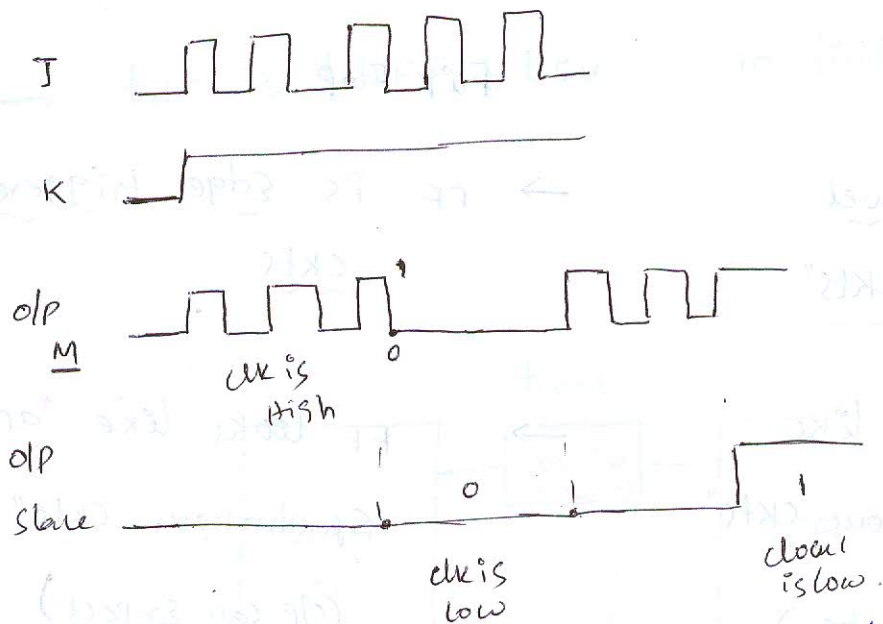
→ To avoid Race around condition master-slave
Flip flop is used.

⇒ Master-slave Flip Flop using JK Flip Flop :-



→





→ Master Slave Configuration is of Pulse triggered

Flip Flops

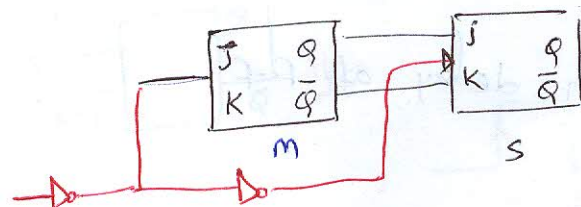
→ Based on operation Master is Level triggered where as Slave is Edge triggered.

→ In MS Flip Flop olp will change when Slave olp is changing.

→ In this No race around at the olp of Slave

→ Master - Level Triggered

Slave - -ve Edge Triggered



M - Level Triggered

S - +ve Edge Triggered.

Latch

Flip Flop

→ Latch is "Level
triggered CKts"

→ FF is Edge triggered
CKts

→ Latch looks like
an "asynchronous CKts"

→ FF looks like "an
Synchronous CKts"

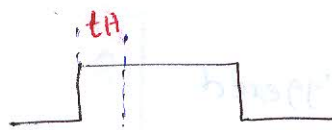
(O/p can not be
Predicted)

(O/p can expect)

⇒ Set up time :- It is the minimum time required to
keep i/p at proper level before applying clock.



⇒ Hold Time :- It is the minimum time required to
keep same data after applying clock to provide
proper O/p.



t_{su} - Set up time

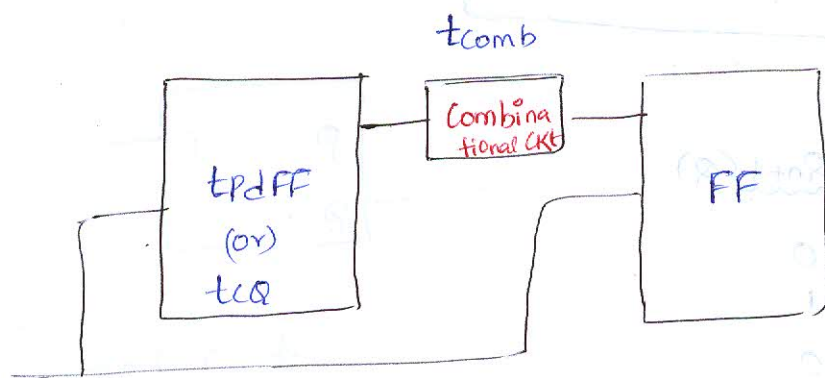
t_H - Hold Time

T_{pdFF} - Propagation delay of F.F.

$$t_H \leq t_{pdFF}$$

→ $t_{ak} \geq t_{pdFF} + t_{su}$ to find clock pulse of signal

→



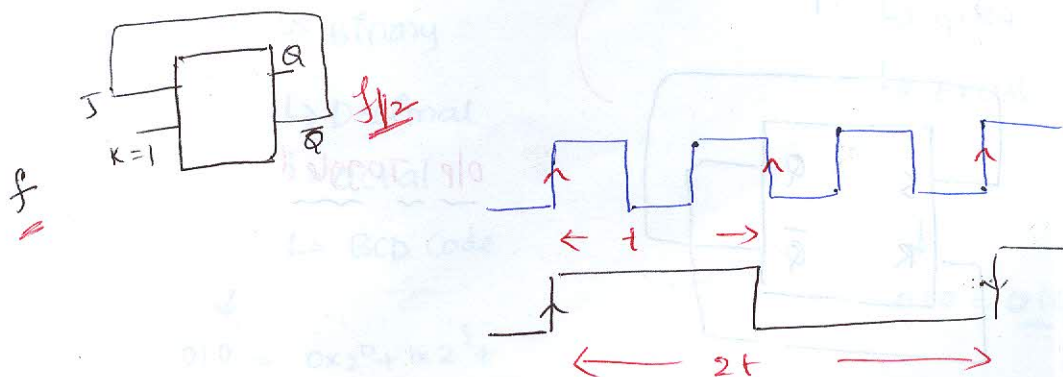
→ $t_{pdFF} = t_{cq} \Rightarrow$ clock to o/p delay.

$$\left\{ \begin{array}{l} T_{clk} \geq t_{pdFF} + t_{comb} + t_{su} \\ \text{(or)} \\ t_{cq} \end{array} \right\}$$

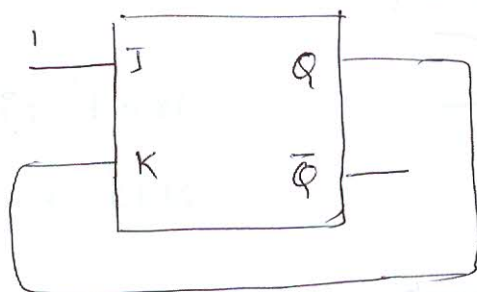
→ DFF - Data Flip Flop

→ J-K - first integrated IC (Name of scientist)

→

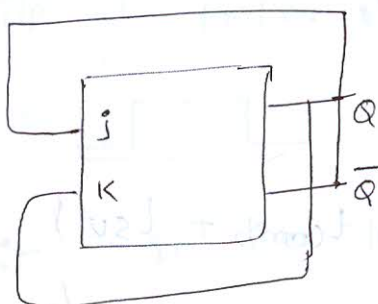


Q>



<u>clk</u>	<u>Q_{n+1}(Q)</u>
0	0
1	1
2	0
3	1
4	0
5	1

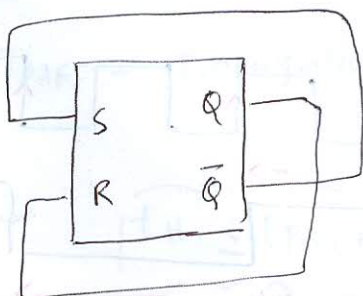
Q>



<u>clk</u>	<u>Q_{n+1}</u>
0	0
1	1
2	0
3	1
4	0
5	1

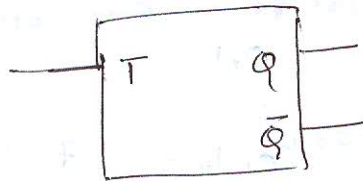
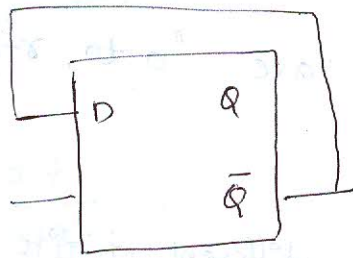
o/p Toggled

Q>



o/p Toggled

→



→

Toggled mode

⇓

above CKTs

Toggle is complement.

⇒ Number systems :-

- 1> Conversions
- 2> Arithmetic operation
- 3> Complements

Number systems & codes

weighed

↳ Binary

↳ Decimal

↳ Octal

↳ BCD code.

↓

$$010 = 0 \times 2^0 + 1 \times 2^1 +$$

↓ weighted position.

unweighted

↳ Gray

↳ Excess-3

↓

$$010 = \underline{010}$$