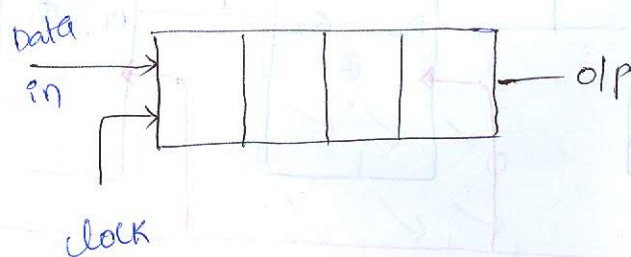
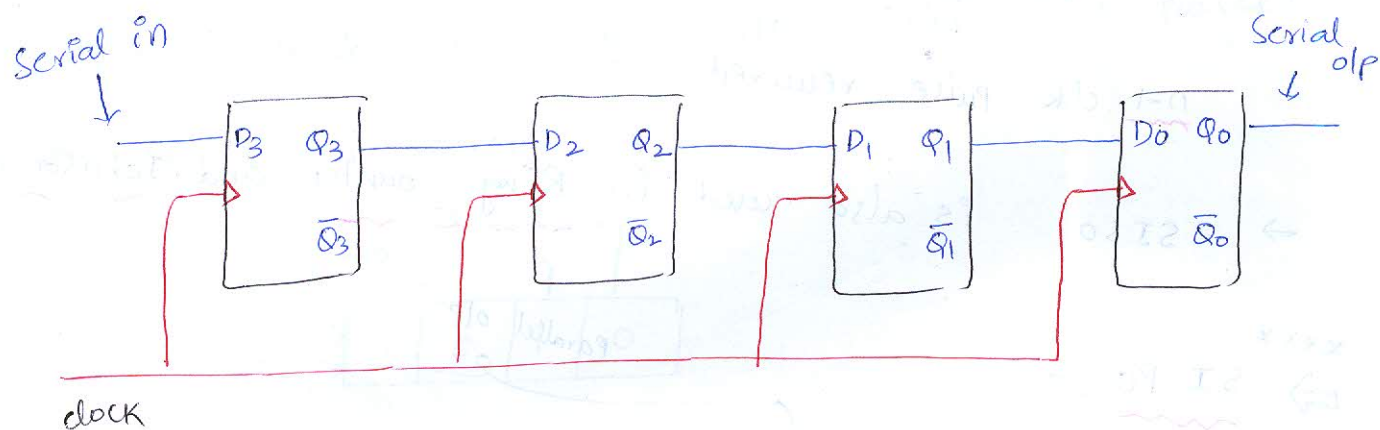


## ⇒ Registers :-

- Registers are used to store group of bits
- To store n bits in register n flip flop's are used.
- Depending on input and output. Registers are four types

- 1) SISO (Serial in serial out)
- 2) SIPO ( " " Parallel out)
- 3) PISO (Parallel in serial out)
- 4) PIPO (Parallel in parallel out)

## ⇒ SISO :-





→ In SISO Register to store  $n$  bit data  
Serially in then  $n$ -clk pulses is required

→ SISO register is used to provide  $n$ -clk pulse  
delay to the i/p data [ $nT_{clk}$ ]

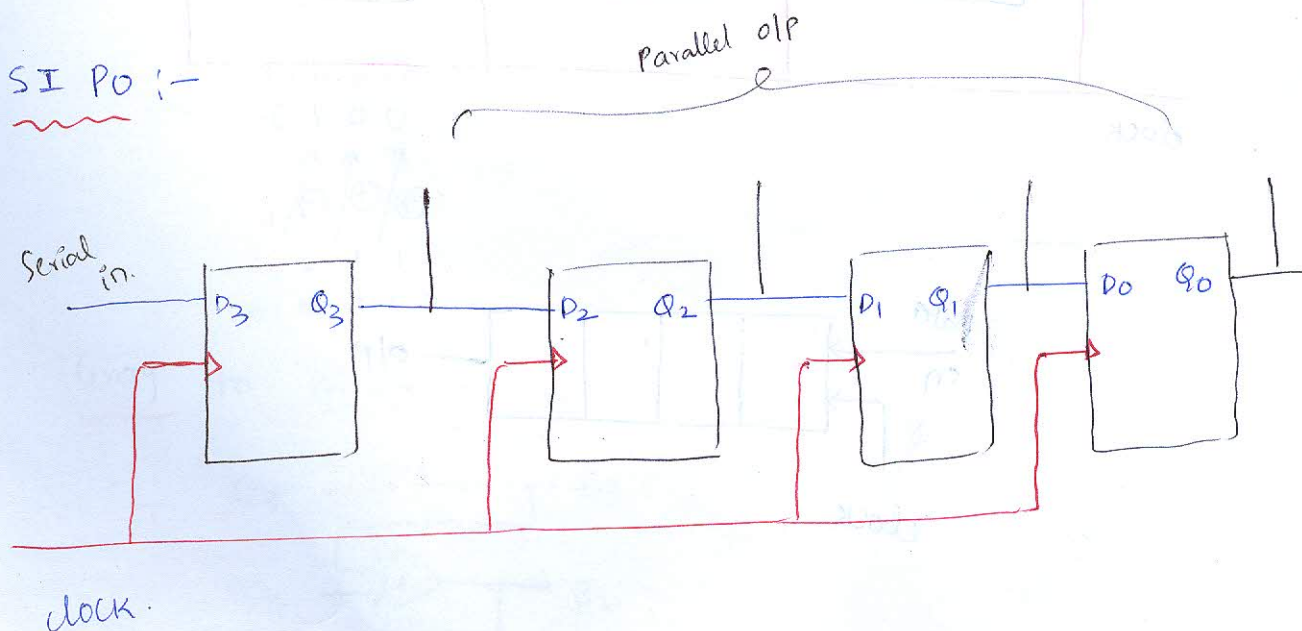
→ To provide  $n$  bit data Serially out then minimum

$n-1$  clk pulse required

→ SISO is also used in Ring counter and Johnson counter

\*\*\*\*

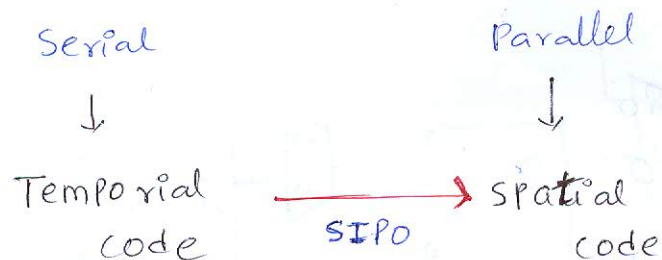
⇒ SI PO :-



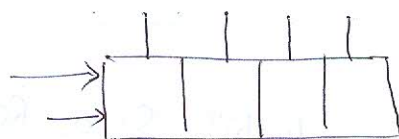
→ To store  $n$  bit -  $n$  clocks

To get Parallel o/p -  $n$  clks

→



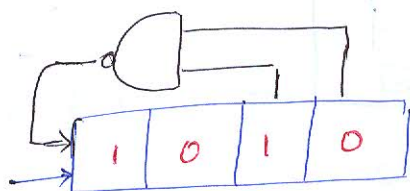
→



SISO

Q1

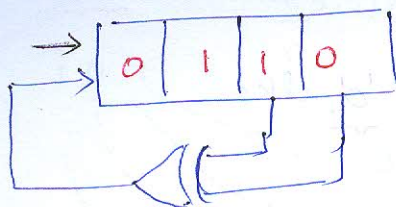
The ckt shown in fig is a 4 bit SISO Register which is loaded with 1010 after applying 3 clk pulses the content of register is



Sol

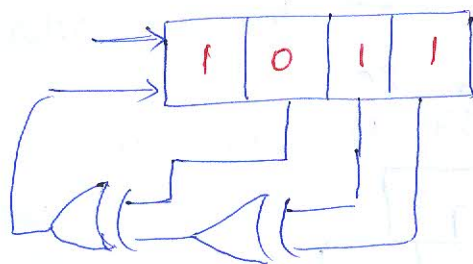
| <u>clk</u> | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
|------------|-------|-------|-------|-------|
| 1          | 1     | 0     | 1     | 0     |
| 2          | 1     | 1     | 1     | 0     |
| 3          | 1     | 1     | 1     | 1     |

Q1



| clk | Q <sub>3</sub> | Q <sub>2</sub> | Q <sub>1</sub> | Q <sub>0</sub> |
|-----|----------------|----------------|----------------|----------------|
| 0   | 0              | 1              | 1              | 0              |
| 1   | 1              | 0              | 1              | 1              |
| 2   | 0              | 1              | 0              | 1              |
| 3   | 1              | 0              | 1              | 0              |

Q2> The ckt shown in fig is 4-bit SISO Register which is loaded with 1011 if clk pulses are applied continuously then after how many clk pulses again data will become.



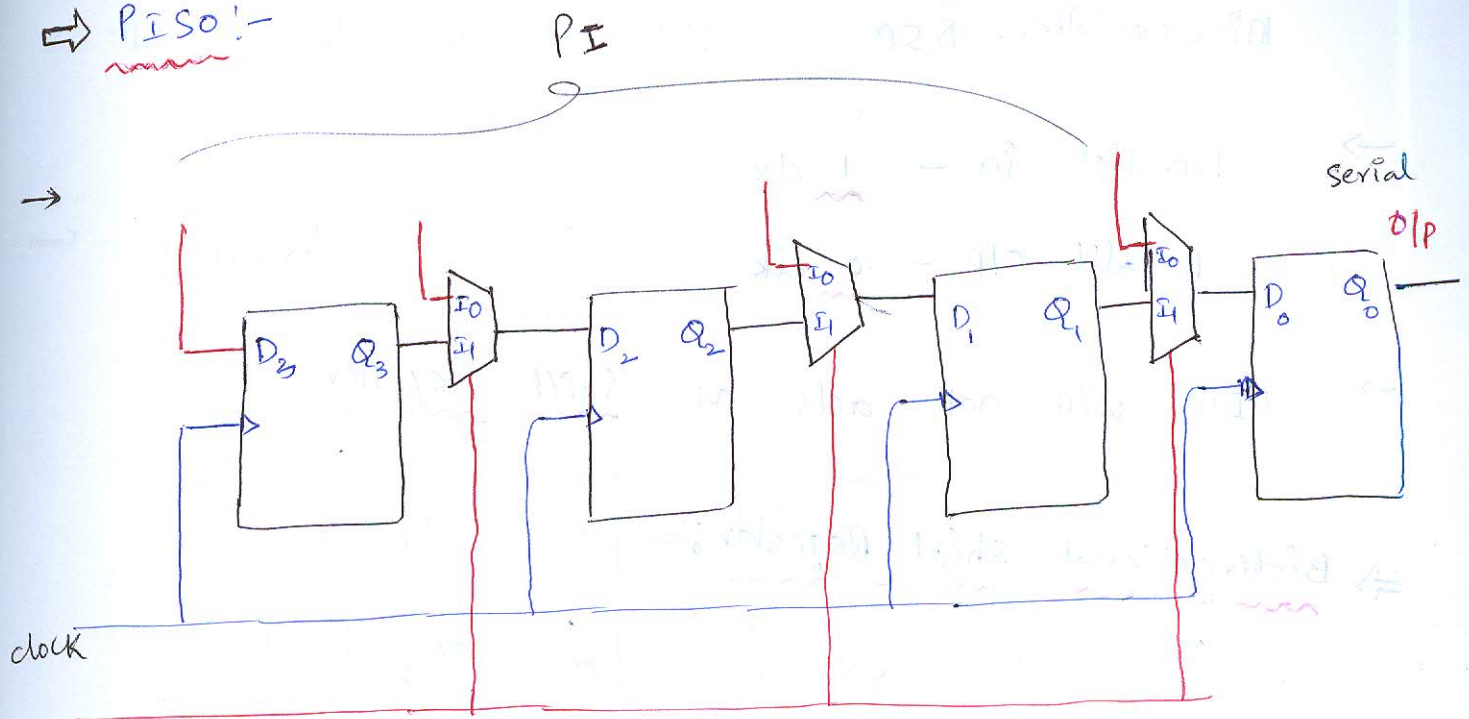
Sol:-

| clk | Q <sub>3</sub> | Q <sub>2</sub> | Q <sub>1</sub> | Q <sub>0</sub> |
|-----|----------------|----------------|----------------|----------------|
| 0   | 1              | 0              | 1              | 1              |
| 1   | 0              | 1              | 0              | 1              |
| 2   | 0              | 0              | 1              | 0              |
| 3   | 1              | 0              | 0              | 1              |
| 4   | 1              | 0              | 0              | 0              |
| 5   | 1              | 1              | 1              | 0              |
| 6   | 0              | 1              | 1              | 1              |
| 7   | 0              | 0              | 1              | 1              |

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⇒ PISO :-



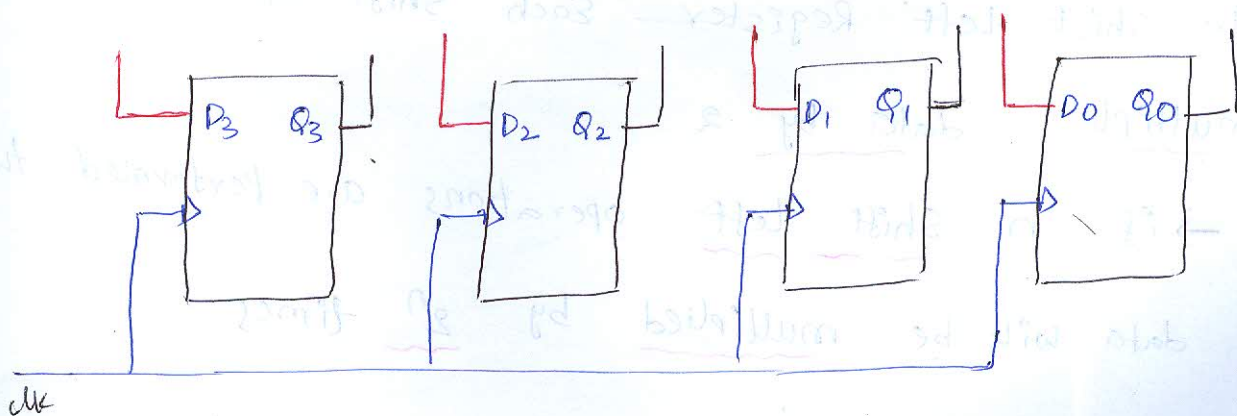
Control = 0 ⇒ PI  
= 1 ⇒ Serial O/P

P - S  
⇓ ⇓

Spatial to Temporal code.

→ No. of clk pulses for Parallel in - 1  
serial out - n-1

⇒ PIPO :-



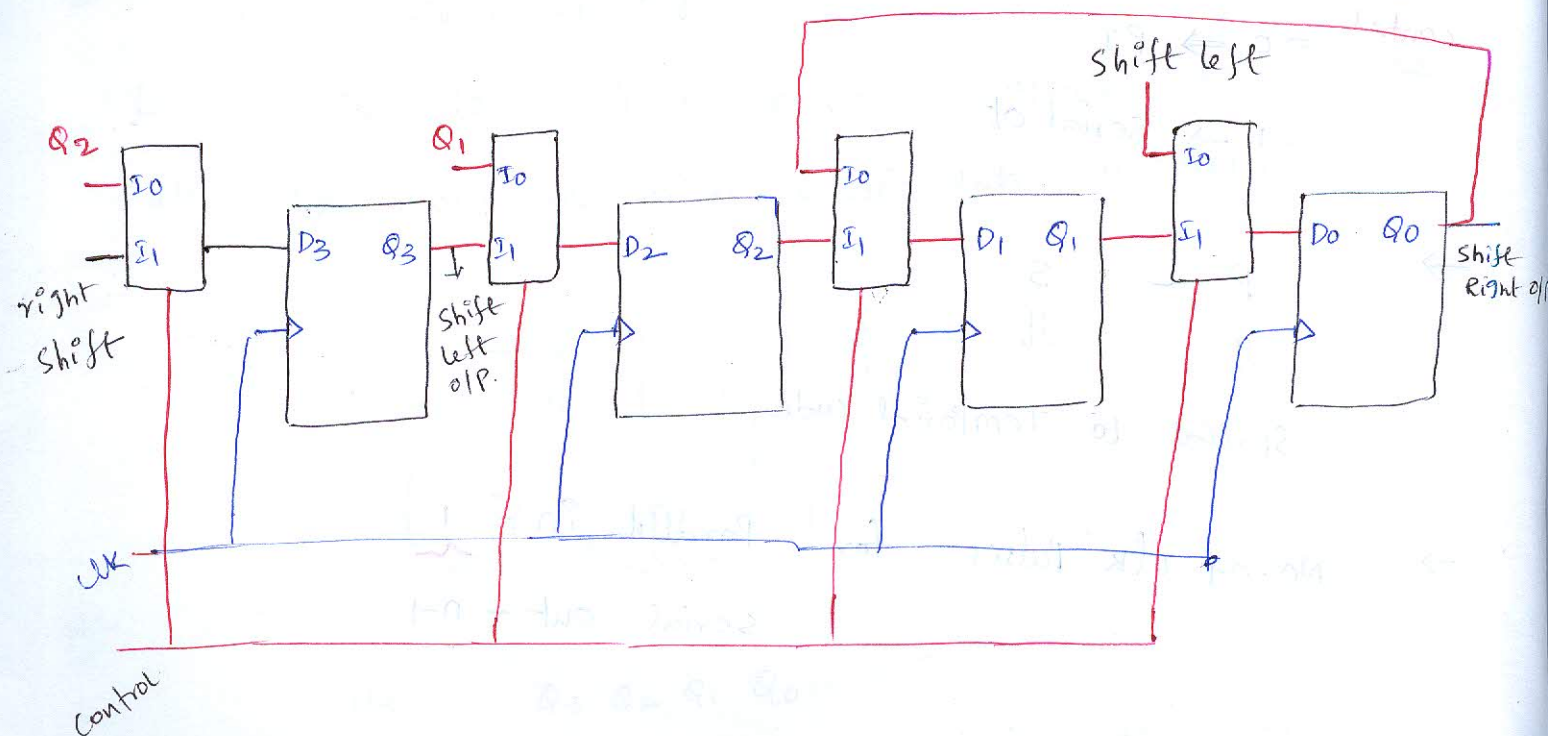
→ PIPo is mostly used as storage register in microprocessor  
Microcontroller, DSP

→ Parallel in - 1 clk

Parallel o/p - 0 clk

→ PIPo will not act as Shift Register

⇒ Bidirectional Shift Register:-

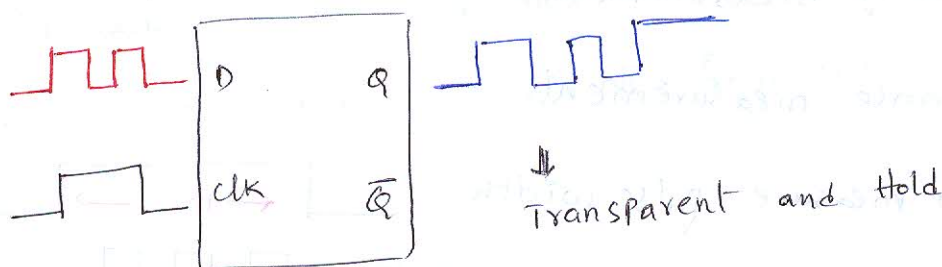


→ In Shift Left Register Each Shift operation will  
multiply data by 2

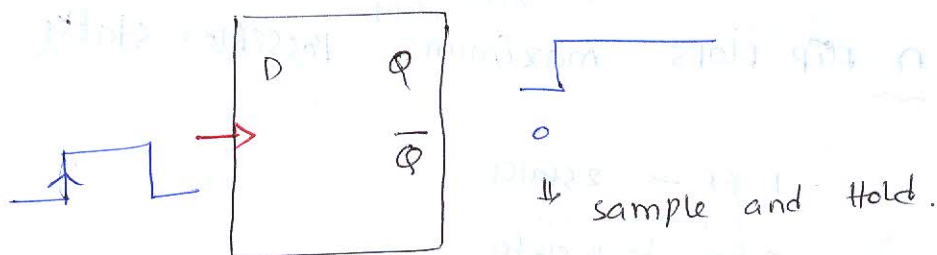
→ if n Shift Left operations are performed then  
data will be multiplied by  $2^n$  times

→ by n shift right operations are performed  
 then data will be divide by  $2^n$

→ D Latch :-



→ D FLIP FLOP



1) Synchronous ( $n \geq 4$ )  
 2) Asynchronous

## Counter

→ counters are basically used to count no. of clk pulses are applied

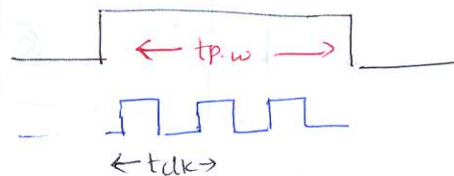
→ frequency dividers

→ Timers

→ frequency measurement

→ Distance measurement

→ To measure pulse width



→ To generate wave forms

$$t_{pw} = n t_{dk}$$

→ with  $n$  flip flops maximum possible states are  $2^n$ .

1 FF - 2 states

2 FF - 4 states

$n$  FF -  $2^n$

→

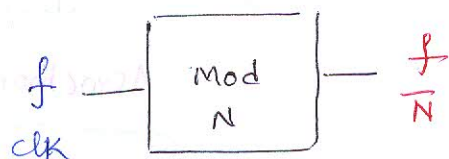
$n$  - no. of FF

$N$  - no. of states

$$\boxed{N \leq 2^n}$$

→ No. of states in a counter is known as Modulus  
Count or Mod Number.

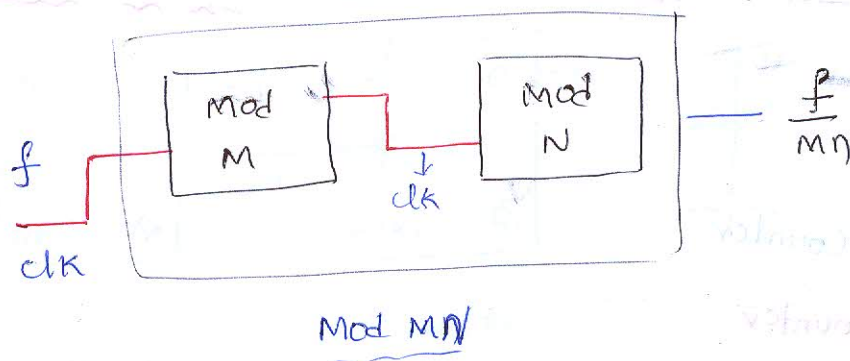
→



Q> A Decade Counter (or) Mod 10 Counter is applied with  
clk frequency of 10MHz then o/p frequency is.

$$\frac{10}{10} = 1\text{MHz}$$

→ If Mod M and Mod N counters are cascaded then  
it will become Mod MN Counter



→ Depending on clk counters are two types

- 1) Synchronous Counter
- 2) Asynchronous Counter

Lab 10

## Counters

| depends on

clock

Synchronous

Asynchronous

→ All FFs are applied with same clock

→ different FF are applied different clock frequency

→ In Synchronous o/p changes at the time so

→ Slower

faster

→ any count sequence

→ fixed count sequence up  
down

→ No decoding errors

→ Decoding errors

Ex:- Ring Counter, Jhonson

Ex:- <sup>\*\*</sup> Ripple Counter

→ Basics

✓ Ripple Counter

✓ Bcd Counter

✓ Ring Counter

✓ Jhonson Counter

✓ Synchronous Series Carry

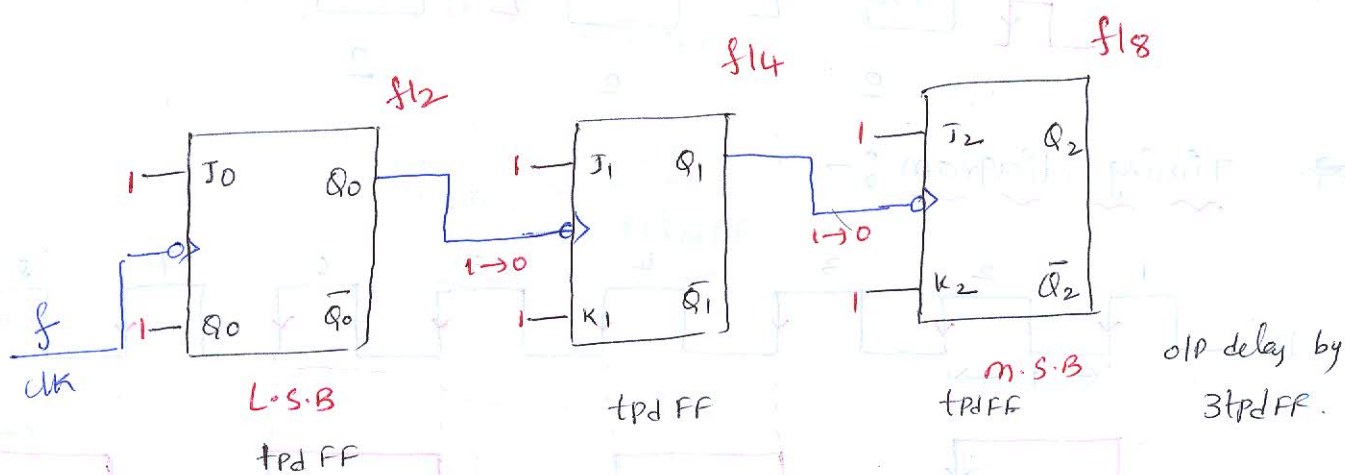
✓ Synchronous parallel Carry Counter

✓ Synchronous counter design for a given sequence

## ⇒ Ripple Counter :-

- Ripple Counter is an asynchronous Counter
- In this Flip Flops are operate in Toggle mode.
- In this External clk [ip clk] is applied to only one Flip Flop and clock to the other stages is derived from olp of previous Flip Flop.
- The Flip Flop applied with External clock will acts as L.S.B

## ⇒ 3 bit Ripple Counter :- (Up Counter)

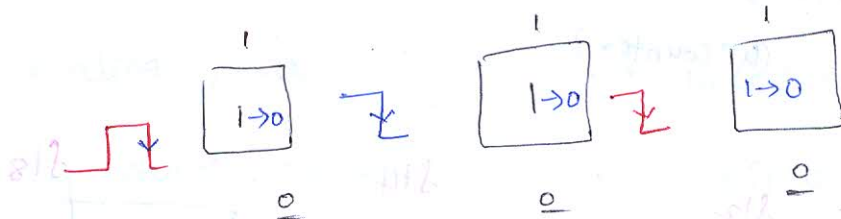


- In the ckt shown in fig Q<sub>0</sub> toggles for every clock
- Q<sub>1</sub> toggles when Q<sub>0</sub> is changes from 1 → 0
- Q<sub>2</sub> " " Q<sub>1</sub> " " 1 → 0

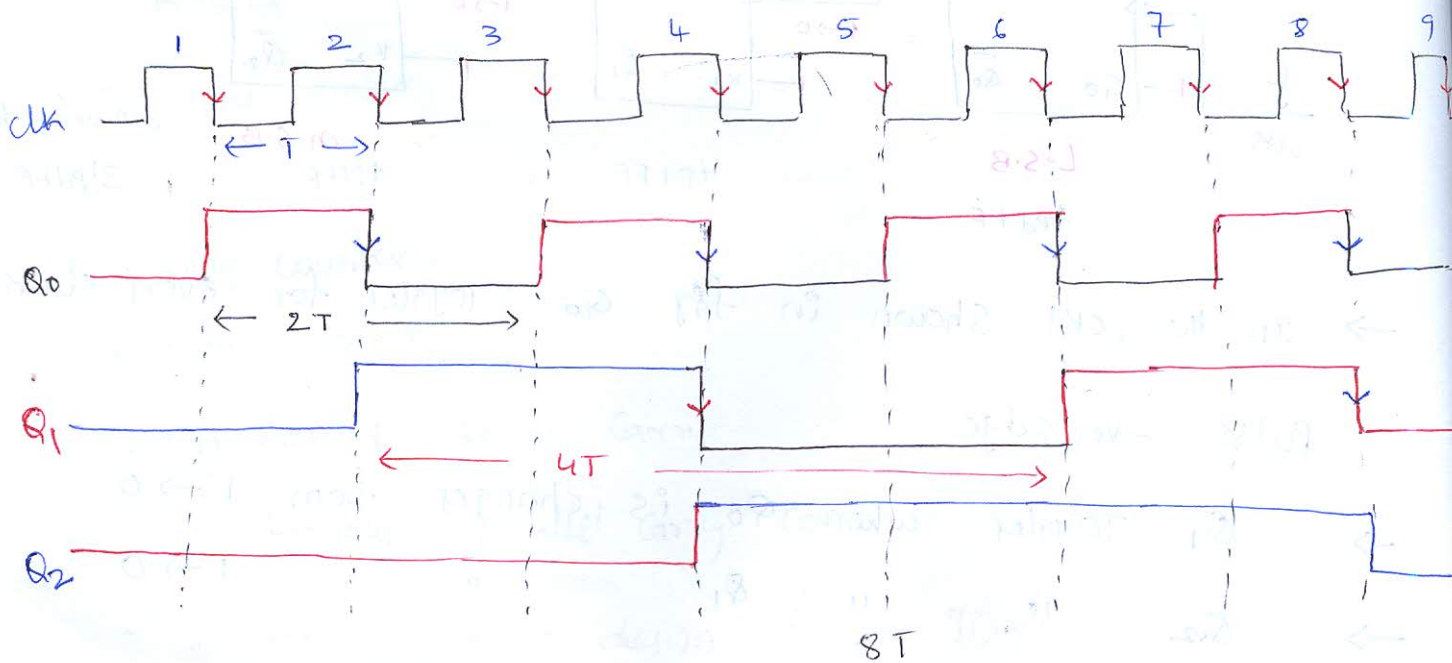
# Truth Table :-

| <u>clock</u> | <u>Q<sub>2</sub></u> | <u>Q<sub>1</sub></u> | <u>Q<sub>0</sub></u> |
|--------------|----------------------|----------------------|----------------------|
| 0            | 0                    | 0                    | 0                    |
| 1            | 0                    | 0                    | 1                    |
| 2            | 0                    | 1                    | 0                    |
| 3            | 0                    | 1                    | 1                    |
| 4            | 1                    | 0                    | 0                    |
| 5            | 1                    | 0                    | 1                    |
| 6            | 1                    | 1                    | 0                    |
| 7            | 1                    | 1                    | 1                    |
| 8            | <u>0</u>             | <u>0</u>             | <u>0</u>             |

→



## → Timing diagram :-



→ with  $n$  FF Maximum states -  $2^n$   
maximum count -  $2^n - 1$

→ another Name - Ripple Counter  $2^n : 1$  scalar  
↓  
divider

$$2^3 \text{ kHz} = 1 \text{ kHz}$$

$$f \rightarrow \frac{f}{2^n}$$

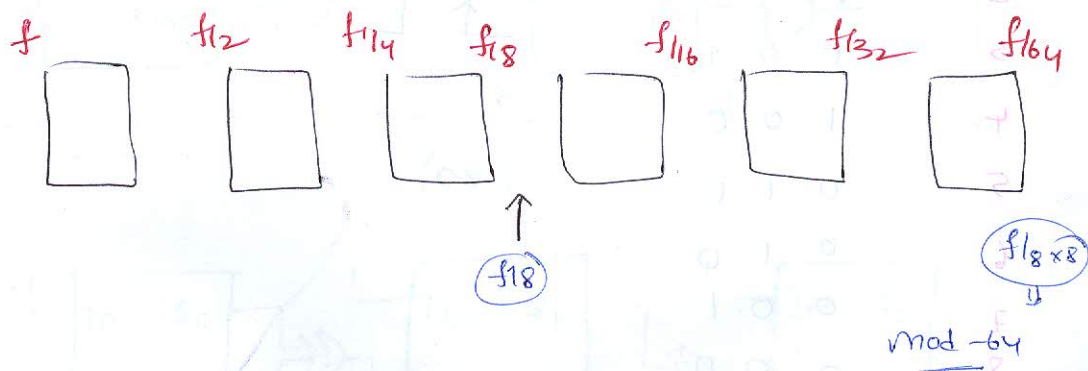
→ In  $n$ -bit Ripple Counter Propagation delay of Each flip flop is  $t_{p\text{FF}}$  then

$$t_{\text{clk}} \geq n t_{p\text{FF}}$$

$$\rightarrow f_{\text{clk}} \leq \frac{1}{n T_{p\text{FF}}}$$

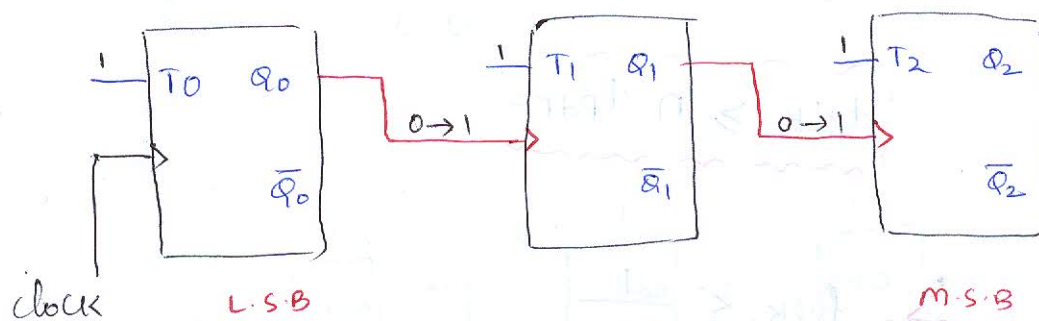
$$f_{\text{max}} = \frac{1}{n t_{p\text{FF}}}$$

→

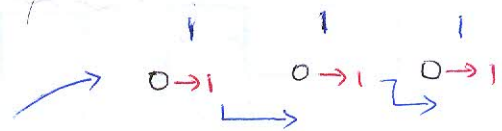


- -ve Edge Trigger  $\bar{Q}$  as clock - UP -  
 → +ve Edge Trigger  $\bar{Q}$  as clock - UP -  
 → -ve Edge Trigger  $\bar{Q}$  as clock - down -  
 → +ve Edge Trigger  $Q$  as clock - down ✓
- valid for only ripple counters

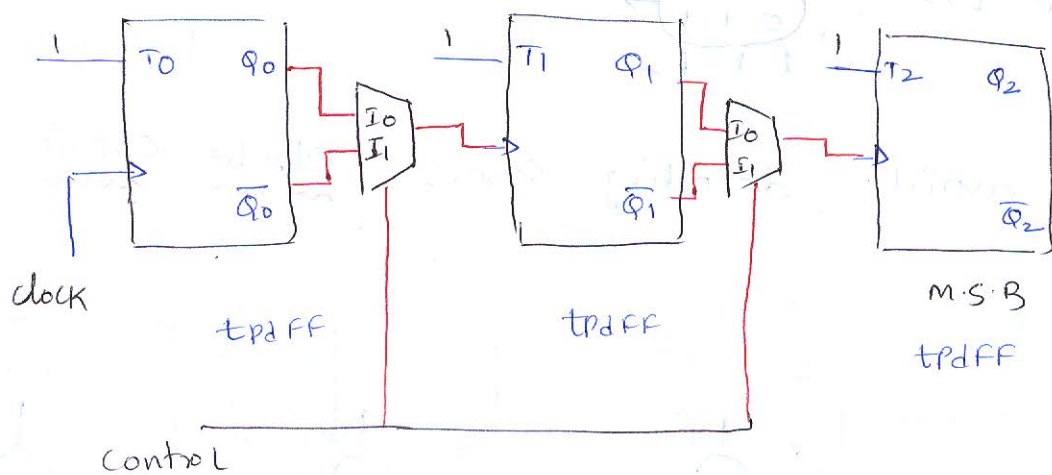
⇒ 3 bit Ripple Counter (down):-



| <u>clk</u> | <u><math>Q_2</math></u> | <u><math>Q_1</math></u> | <u><math>Q_0</math></u> |
|------------|-------------------------|-------------------------|-------------------------|
| 0          | 0                       | 0                       | 0                       |
| 1          | 1                       | 1                       | 1                       |
| 2          | 1                       | 1                       | 0                       |
| 3          | 1                       | 0                       | 1                       |
| 4          | 1                       | 0                       | 0                       |
| 5          | 0                       | 1                       | 1                       |
| 6          | 0                       | 1                       | 0                       |
| 7          | 0                       | 0                       | 1                       |
| 8          | 0                       | 0                       | 0                       |



⇒ Ripple (UP-Down) Counter :-

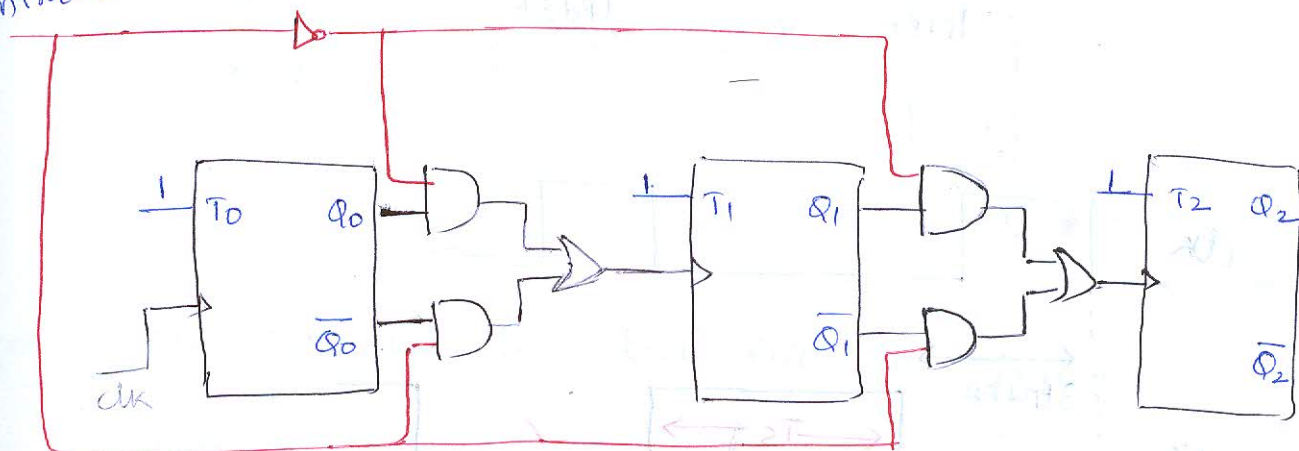


→ Control = 0 down

→ Control = 1 up

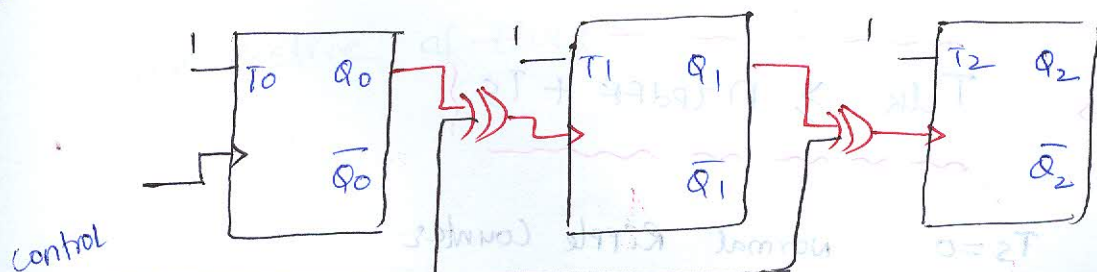
(OR)

→ Control = 0



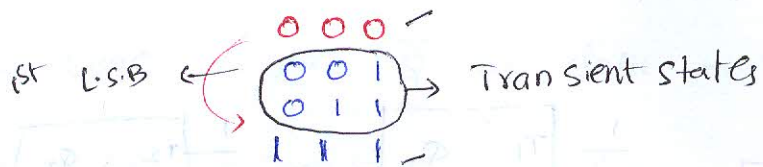
(OR)

→

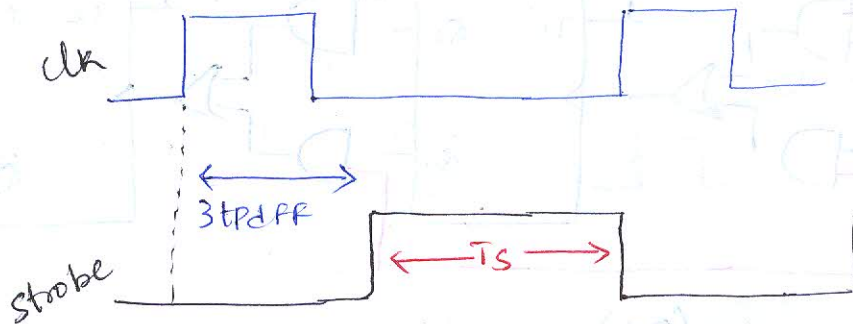
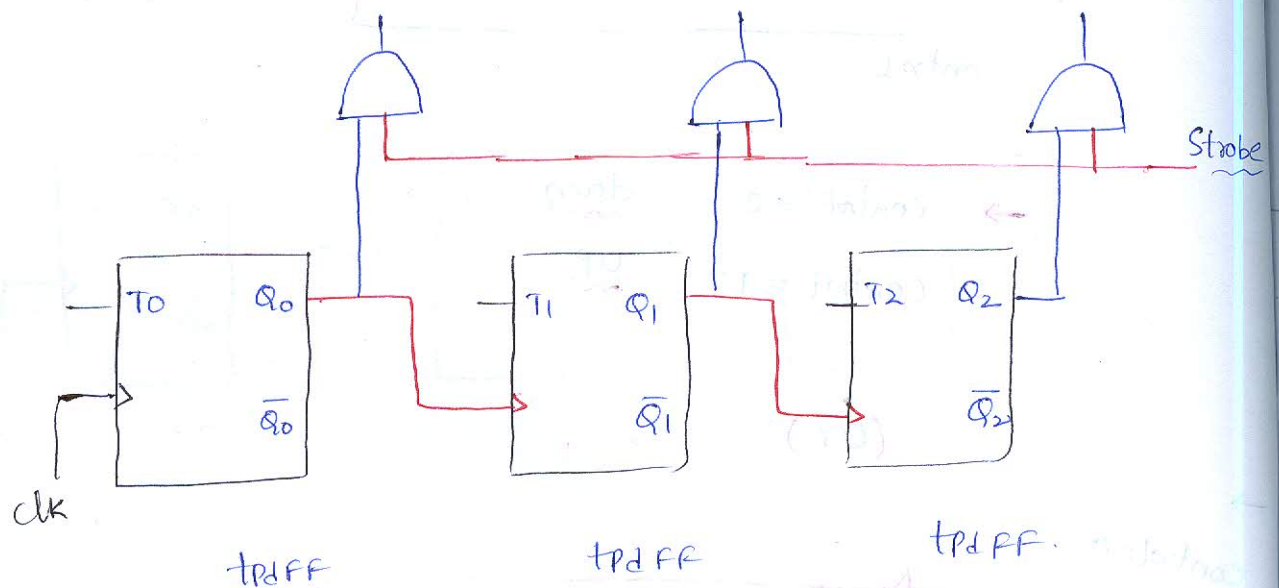


0 - Down (buffer)  
1 - UP (invert)

→ In Ripple Counter Transient States (~~000~~) decoding  
errors will be present due to propagation delay



→ TO avoid decoding errors Strobe Circuit is used



→  $T_{clk} \geq n t_{pdff} + T_s$

Note :-

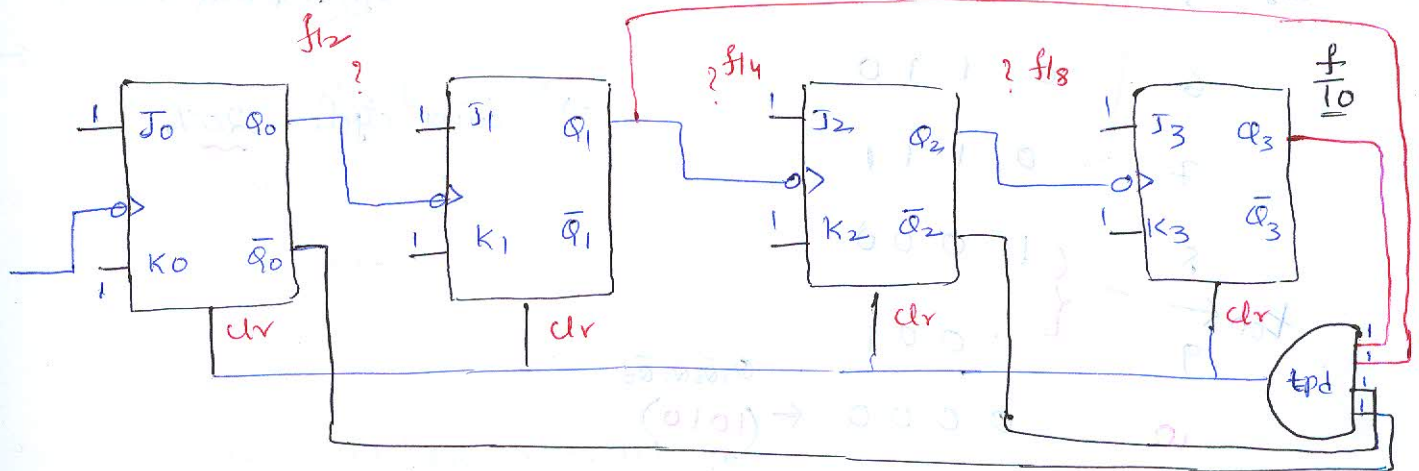
$T_s = 0$

Normal Ripple Counter

## ⇒ Non-Binary Ripple Counter :-

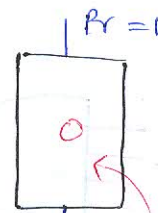
Mod 5  
BCD Counter } all states are not used.

## ⇒ BCD Counter :-



→ J, K, D, T, S, R → Synchronous

→ (0) Clear } Asynchronous  
→ (1) Preset }



clr = 1 - clear

0 → No effect

→ clear is used to clear Flip Flop irrespective of clock.

→ Preset is used to set Flip Flop (or) Counter irrespective of clock.

clk    Q<sub>3</sub> Q<sub>2</sub> Q<sub>1</sub> Q<sub>0</sub>

BCD Counter

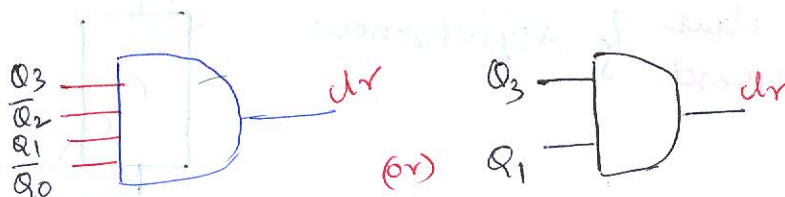
|    |   |   |   |   |
|----|---|---|---|---|
| 0  | 0 | 0 | 0 | 0 |
| 1  | 0 | 0 | 0 | 1 |
| 2  | 0 | 0 | 1 | 0 |
| 3  | 0 | 0 | 1 | 1 |
| 4  | 0 | 1 | 0 | 0 |
| 5  | 0 | 1 | 0 | 1 |
| 6  | 0 | 1 | 1 | 0 |
| 7  | 0 | 1 | 1 | 1 |
| 8  | 1 | 0 | 0 | 0 |
| 9  | 1 | 0 | 0 | 1 |
| 10 | 0 | 0 | 0 | 0 |

toff ← 5  
ton ← 9  
Q<sub>3</sub>Q<sub>2</sub>Q<sub>1</sub>Q<sub>0</sub> ← (1010)  
Clear

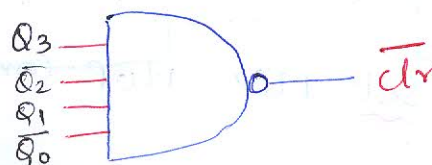
→ BCD counter is not an Symmetrical Counter

→ duty cycle = 20%

⇒ BCD Counter :-



→



→ In BCD Counter the frequency of output is  $\frac{f}{10}$

→ (0 → 9) BCD Counter is a decade Counter

→ but all Decade counters are not BCD counters  
↓  
any 10 states

→ mod-2 ckt → Symmetrical square wave generator:

TO Know which Counter:-

① Ripple Counter

② trigger

③ clock

④ up/down

⑤ clr/preset → 1111  
↓  
0000

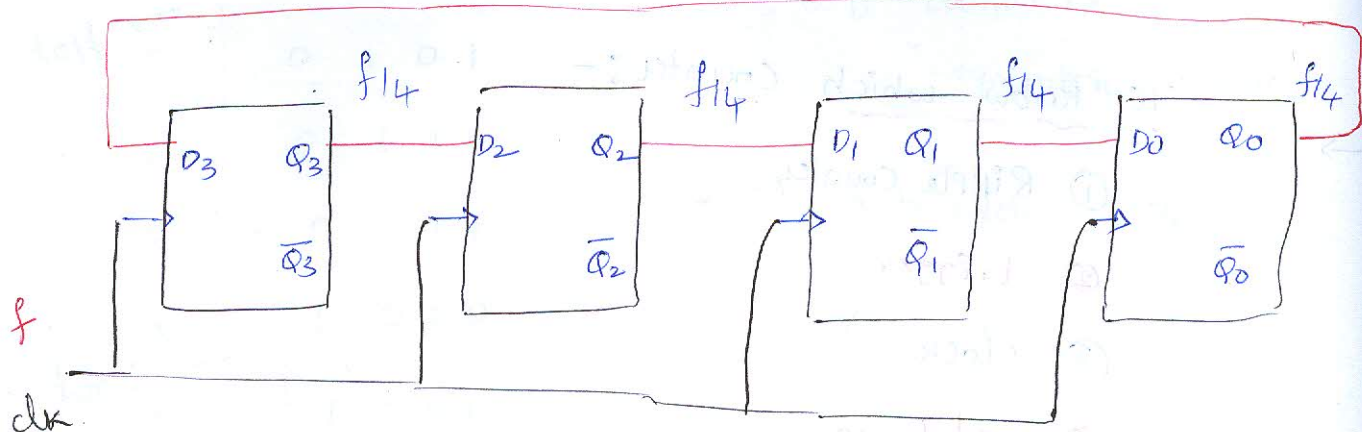
⑥ Terminating count



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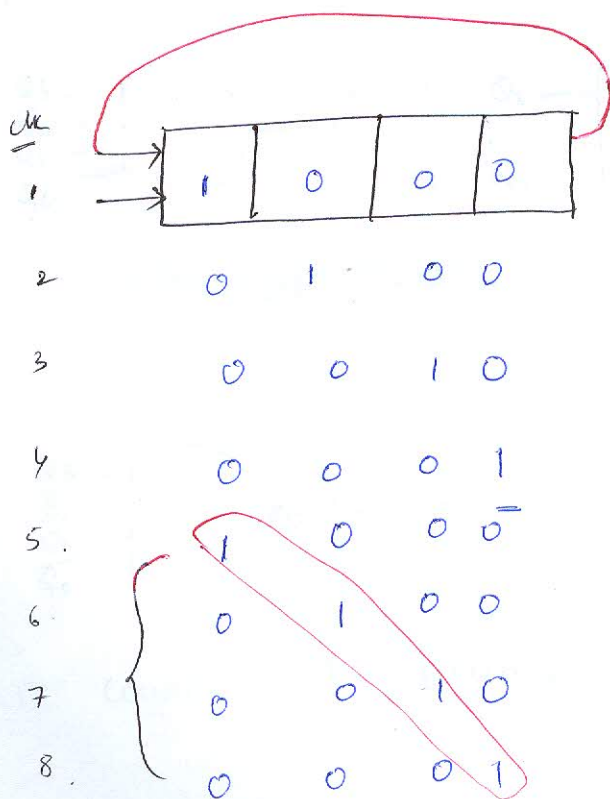
⇒ Synchronous Counter:-

⇒ Ring Counter:-



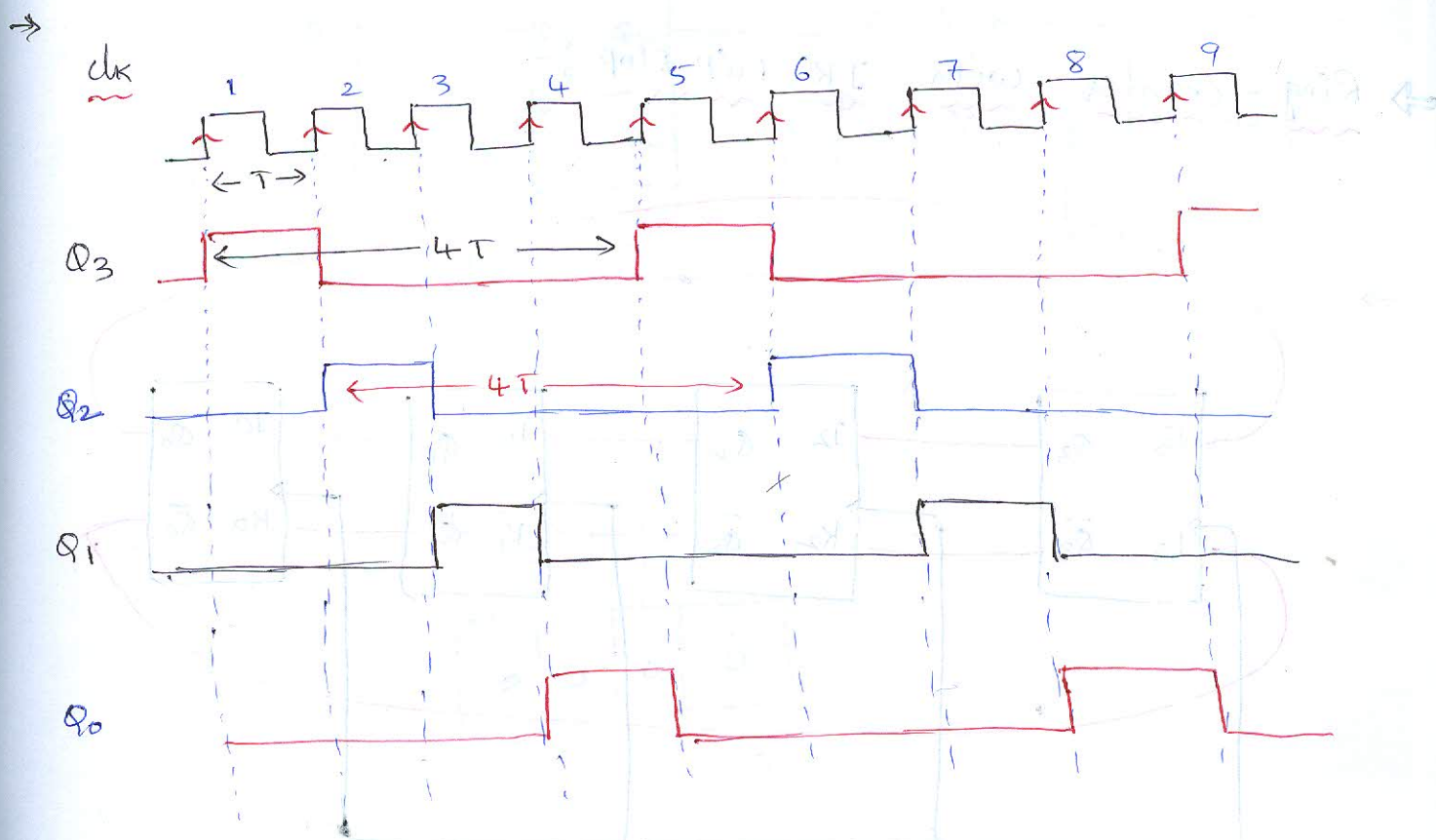
→ In Ring Counter only one Flip Flop is high and it rotates among all Flip Flops

→



→ In Ring Counter with  $n$  Flip Flops maximum possible states are  $n$ .

→ with  $n$  Flip Flops no. of unused states  $2^n - n$



→ In Ring Counter if input frequency is  $f$  then output frequency  $\frac{f}{N}$ .

→ Ring Counter is used in SAR type A/D converters and in stepper motors control, wave form generation

→ Phase shift in Ring Counter  $\frac{360^\circ}{n}$  ✓

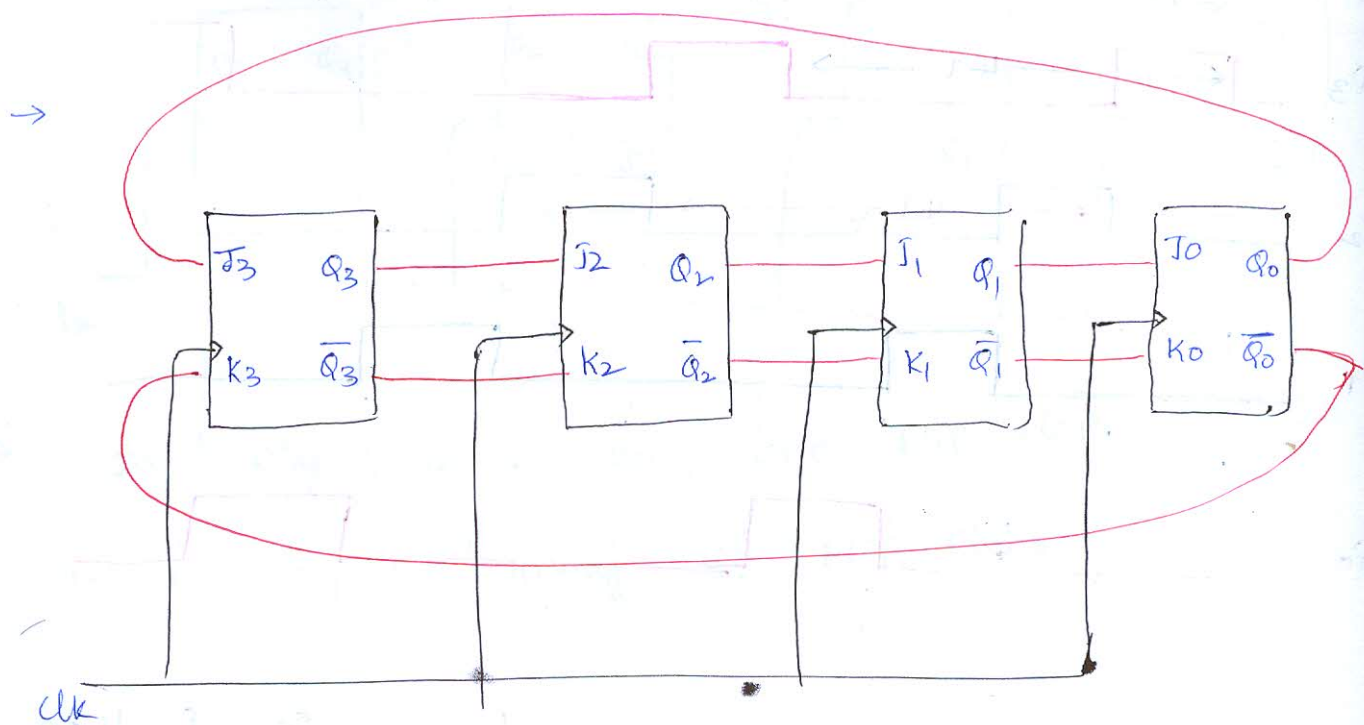
→ In Ring Counter delay for o/p is  $t_{pdFF}$

→

$$T_{clk} > t_{pd FF}$$

$$f_{clk} \leq \frac{1}{t_{pd FF}}$$

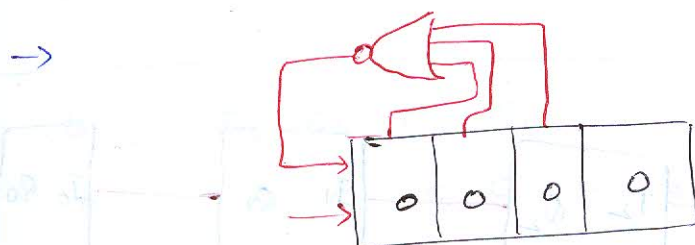
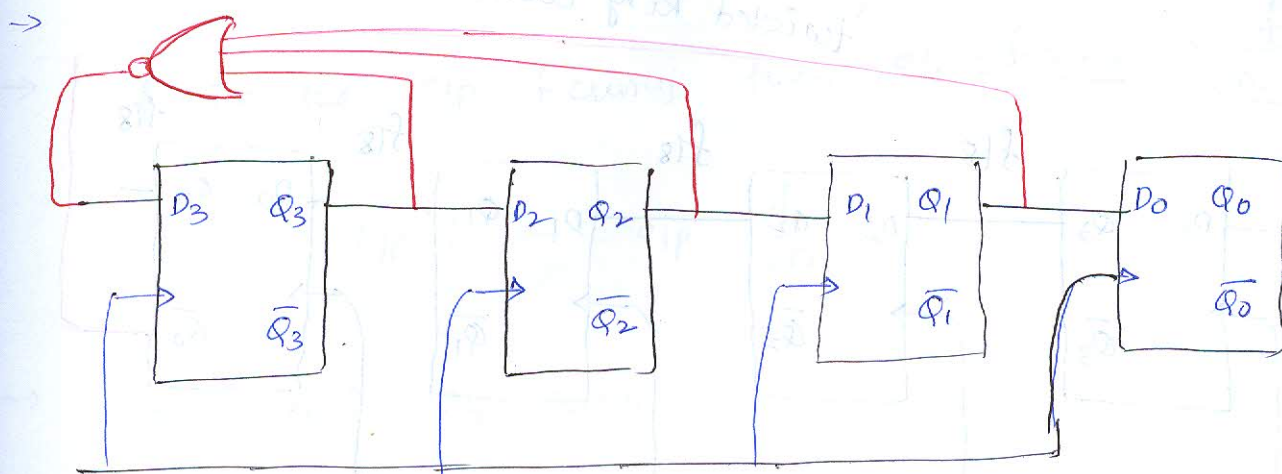
⇒ Ring Counter with JK Flip Flop :-



→ JK FF is mostly used in Shift Registers

→ It will not self start so we are using self starting

⇒ self starting Ring Counter :-



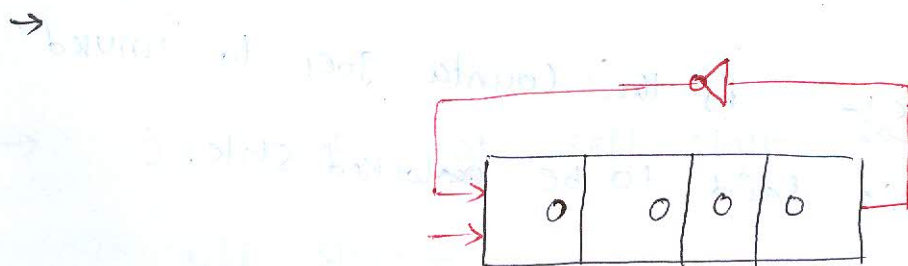
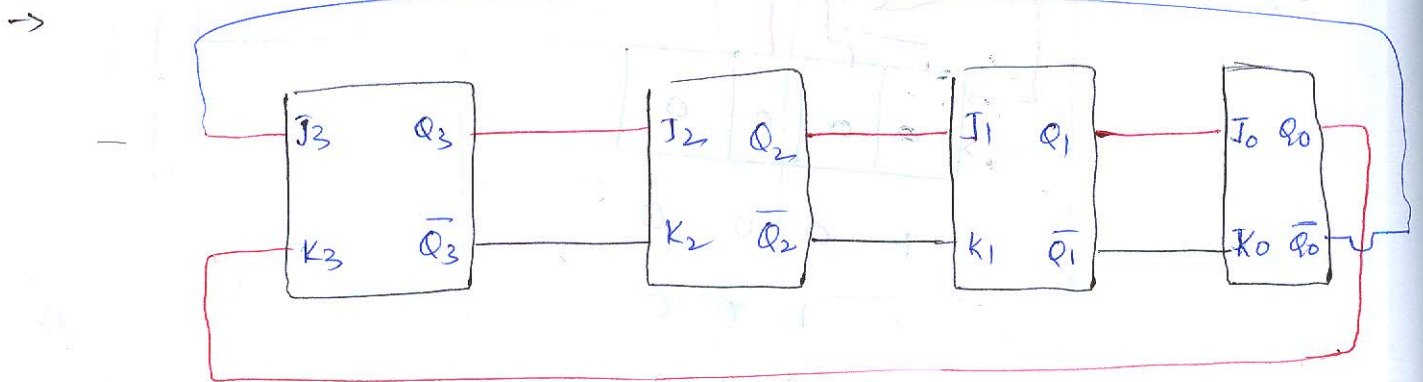
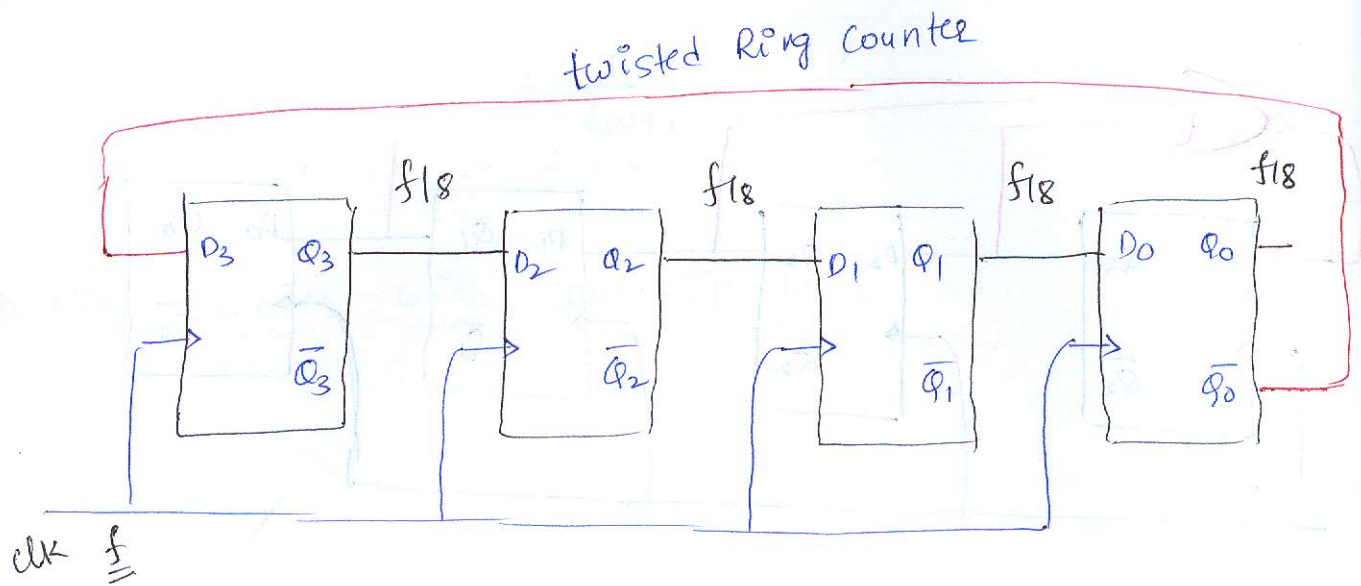
|   |   |   |   |
|---|---|---|---|
| 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 |

→ Lock out state :- if the counter goes to unused state then it is said to be ~~un~~locked state.

→ It will avoid lock out state.

→ Decoding is very simple in Ring counter.

→ Thomson Counter :-



8 states

|   |   |   |   |
|---|---|---|---|
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 |

- with  $n$  FF maximum used states  $2n$ .
- no. of unused states  $2^n - 2n$ .
- $f$  is the i/p frequency then o/p frequency  $\rightarrow \frac{f}{\text{no. of states}}$
- i/p  $f$  — o/p  $\frac{f}{2n}$
- duty cycle is 50%.
- Phase shift Remains Same.
- Decoding :-

| <u>clk</u> | <u><math>Q_3</math></u> | <u><math>Q_2</math></u> | <u><math>Q_1</math></u> | <u><math>Q_0</math></u> |                                   |
|------------|-------------------------|-------------------------|-------------------------|-------------------------|-----------------------------------|
| 0          | <u>0</u>                | 0                       | 0                       | <u>0</u>                | $\rightarrow \bar{Q}_3 \bar{Q}_0$ |
| 1          | <u>1</u>                | 0                       | 0                       | 0                       | $\rightarrow Q_3 \bar{Q}_2$       |
| 2          | 1                       | <u>1</u>                | 0                       | 0                       | $\rightarrow Q_2 \bar{Q}_1$       |
| 3          | 1                       | 1                       | <u>1</u>                | 0                       | $\rightarrow Q_1 \bar{Q}_0$       |
| 4          | <u>1</u>                | 1                       | 1                       | <u>1</u>                | $\rightarrow Q_3 Q_0$             |
| 5          | <u>0</u>                | 1                       | 1                       | 1                       | $\rightarrow \bar{Q}_3 Q_2$       |
| 6          | 0                       | <u>0</u>                | 1                       | 1                       | $\rightarrow \bar{Q}_2 Q_1$       |
| 7          | 0                       | 0                       | <u>0</u>                | 1                       | $\rightarrow \bar{Q}_1 Q_0$       |
| 8          | 0                       | 0                       | 0                       | 0                       |                                   |

- In Johnson Counter to decode Each state one two i/p And gate (or) Nor gate is used.

→ Advantage of Ring Counter is <sup>decoding</sup> Simple.

→ Another names for Johnson Counter

✓ mobile Counter

✓ Switch tail Counter

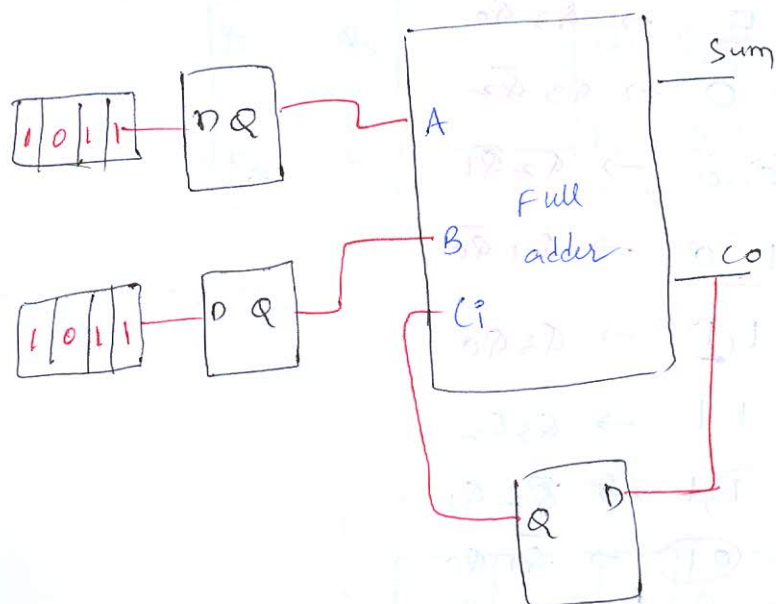
✓ creeping Counter

↓

Successive terms differ by 1 unit.

✓ Walking Counter

Serial Adder:-

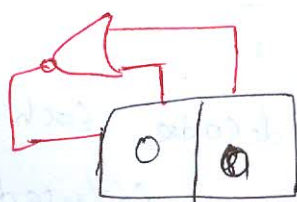


$$\begin{array}{r} 1011 \\ 1011 \\ \hline 010 \\ \textcircled{1}0 \\ \text{second clk.} \end{array}$$

P.No-30

27

Q1

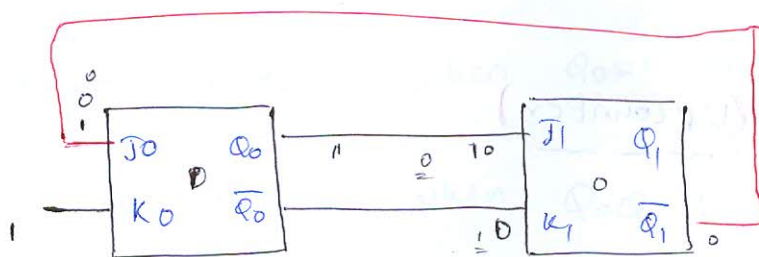


| Q <sub>0</sub> | Q <sub>1</sub> |
|----------------|----------------|
| 0              | 0              |
| 1              | 0              |
| 0              | 1              |
| 0              | 0              |

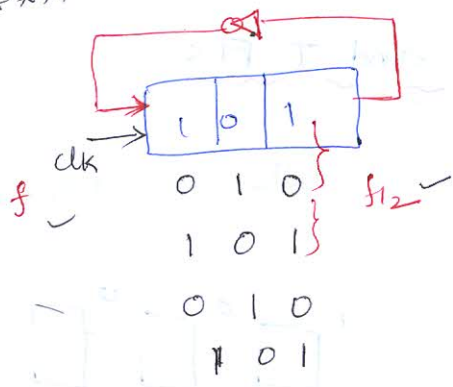
Q<sub>1</sub> Q<sub>0</sub>

|   |   |
|---|---|
| 0 | 0 |
| 0 | 1 |
| 1 | 0 |
| 0 | 0 |

Q3  
→



Q4  
29



unused states

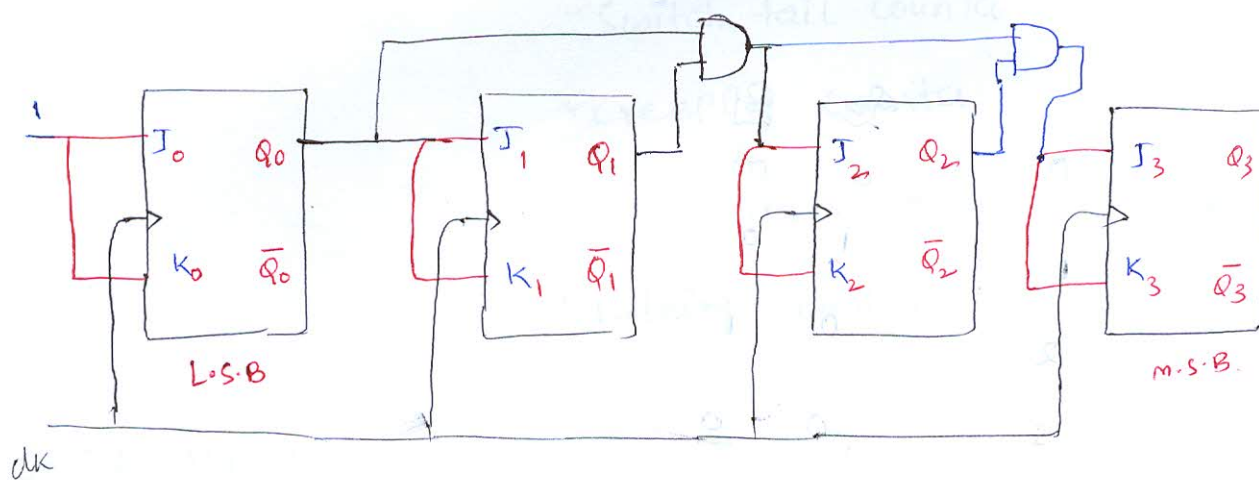
010 ✓  
001 ✓

Counters

Synchronous Counter

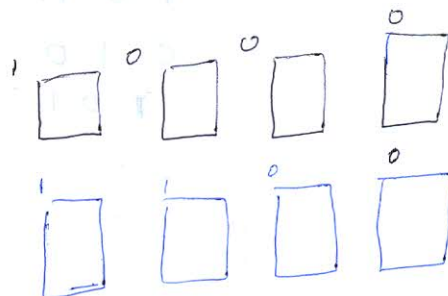
⇒ Synchronous Series Carry Counter :-

(Up Counter)



→ Here we use only JK and T FFs

| <u>clk</u> | <u>Q<sub>3</sub></u> | <u>Q<sub>2</sub></u> | <u>Q<sub>1</sub></u> | <u>Q<sub>0</sub></u> |
|------------|----------------------|----------------------|----------------------|----------------------|
| 0          | 0                    | 0                    | 0                    | 0                    |
| 1          | 0                    | 0                    | 0                    | 1                    |
| 2          | 0                    | 0                    | 1                    | 0                    |
| 3          | 0                    | 0                    | 1                    | 1                    |



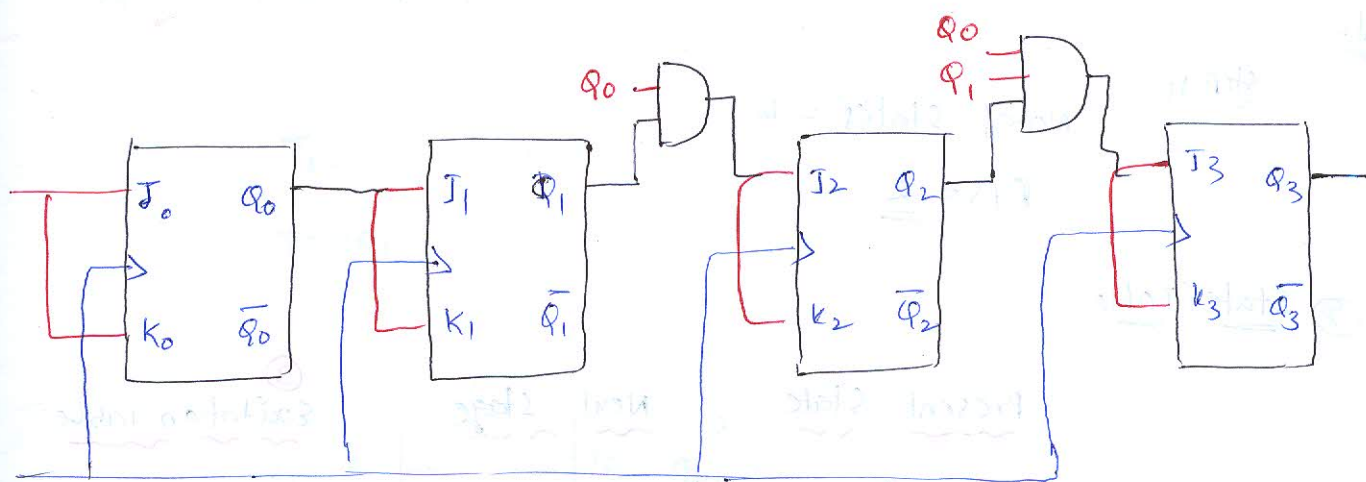
|    |   |   |   |   |
|----|---|---|---|---|
| 15 | 1 | 1 | 1 | 1 |
| 16 | 0 | 0 | 0 | 0 |

- $Q_0 \rightarrow$  Toggles for every clock pulse
- $Q_1 \rightarrow$  Toggles when  $Q_0=1$  and Toggles clk
- $Q_2 \rightarrow$  Toggles when  $Q_0 Q_1=1$  and clock pulse is applied
- $Q_3 \rightarrow$  Toggles when  $Q_0 Q_2 Q_1=1$  and clk pulse is applied

→ To provide down counter connect  $\bar{Q}$  dps to the next stage i/p.s.

→ \*\*\*  
✓  $T_{clk} \geq t_{pd FF} + (n-2)t_{pd And}$

Synchronous Parallel Carry Counter :-



clk

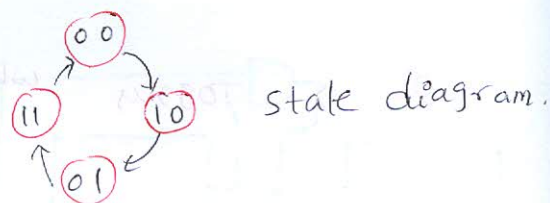
$T_{clk} \geq t_{pd FF} + t_{pd And}$

Fastest Counters :-

Ring > Johnson > synchronous parallel > series > ripple counter

Q) Design a synchronous Counter using +ve edge triggered 'D' Flip Flops to count sequence

$00 \rightarrow 10 \rightarrow 01 \rightarrow 11 \rightarrow 00$



state diagram.

Sol:-

⇒ Design Procedure :-

- ① Identify No. of <sup>states</sup> and <sup>FFs</sup>
- ② Construct State Table
- ③ write Excitation Equation
- ④ minimize
- ⑤ implement.

Sol:-

Step 1;

No. of states = 4

FFs = 2

② State Table

Present State

$Q_1 \quad Q_0$

0 0

1 0

0 1

1 1

Next Stage

$Q_{1+} \quad Q_{0+}$

1 0

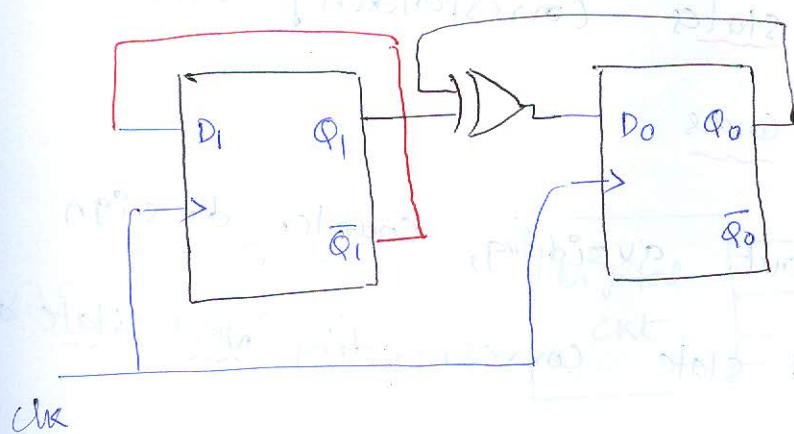
0 1

1 1

0 0

③ Excitation Table

| $D_1$ | $D_0$ | $T_1$ | $T_0$ |
|-------|-------|-------|-------|
| 1     | 0     | 1     | 0     |
| 0     | 1     | 1     | 1     |
| 1     | 1     | 1     | 0     |
| 0     | 0     | 1     | 1     |



→ minimize

$$D_1 = \bar{Q}_1 \bar{Q}_0 + \bar{Q}_1 Q_0$$

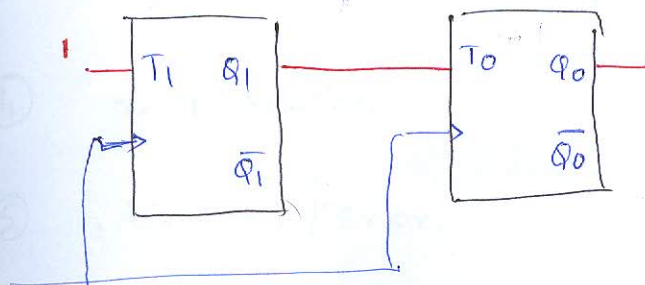
$$\underline{D_1 = \bar{Q}_1}$$

$$\underline{D_0 = Q_1 \oplus Q_0}$$

using T Flip Flops :-

$$T_1 = 1$$

$$T_0 = Q_1$$



note

1> Consider unused states corresponding excitation  
ilps as don't cares

2> During lock out avoiding, counter design  
consider unused state corresponding next state as  
one of used state.

