

ADC/DAC



① Counter type

② SAR TYPE

③ Flash TYPE

④ dual slope integrating TYPE.

MP
MC
DSP

① weighted Resistor

② R-2R Ladder

→ over sampling A-D Converter $\Sigma-\Delta$ ADC

⇒ characteristics of DAC :-

① Resolution (or) Step size

② Analog o/p voltage.

③ maximum voltage V_{FS}

④ % Resolution

⑤ Accuracy / error.

⇒ Resolution :-

Resolution of DAC is change in Analog voltage

Corresponding 1 L.S.B bit increment at the o/p

0000 — 0V
0001 — 1V

$$\rightarrow \text{Resolution of } n \text{ bit DAC} = \frac{V_r}{2^n - 1}$$

n - no. of bits

V_r - Reference voltage.

⇒ Analog o/p voltage :-

It is given by Resolution multiplied with Decimal Equivalent of binary data.

$$V_o = \frac{V_r}{2^n - 1} \times \sum_{i=0}^{n-1} 2^i b_i$$

Q> In a 4-bit D to A Conv $V_R = 5V$ if binary data 1001 is applied then analog o/p voltage is

Sol:-

$$\text{Resolution} = \frac{V_r}{2^n - 1} = \frac{5}{2^4 - 1} = \frac{5}{15} = \frac{1}{3}$$

$$V_o = \frac{V_r}{2^n - 1} \times \sum_{i=0}^{n-1} 2^i b_i$$

$$\underline{V_o} = \frac{1}{3} \times 9 = \underline{3V}$$

⇒ VFS :-

maximum analog o/p voltage is known as

VFS

$$\rightarrow V_{FS} = \frac{V_r}{2^n - 1} \times 2^n - 1 \quad \rightarrow \text{all bits are 1111 then i get maximum o/p.}$$

$$\boxed{V_{FS} = V_r}$$

⇒ % Resolution :-

$$\% \text{ Resolution} = \frac{\text{Resolution}}{V_{FS}} \times 100$$

$$\frac{\frac{V_r}{2^n - 1}}{V_r} \times 100$$

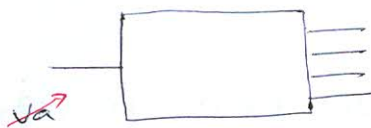
$$\% \text{ Resolution} = \frac{1}{2^n - 1} \times 100$$

→ maximum error acceptable in ADCs (or) DAcs is Equivalent to one bit [1 L.S.B] = resolution.

① weighted Resistor $\rightarrow \frac{V_r}{2^n - 1}$

② $\checkmark$ R-2R ladder $\rightarrow \frac{V_r}{2^n}$

$\Rightarrow$ Characteristics of ADC:-



$\rightarrow \checkmark$ Resolution = $\frac{V_{\text{range}}}{2^n - 1}$

$$V_{\text{range}} = \text{Max} - \text{min}$$

$$\pm 5V$$

$$V_{\text{range}} = \underline{10V}$$

$\rightarrow$ % Resolution = $\frac{1}{2^n - 1} \times 100$

$\rightarrow$ error / accuracy = Resolution

$\rightarrow$ Dynamic Range ADC = $(6n + 1.7) \text{ dB}$
= $\underline{6n \text{ dB}}$

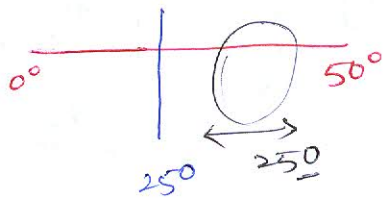
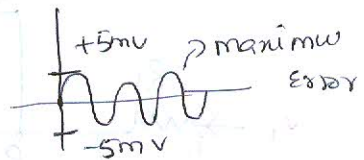
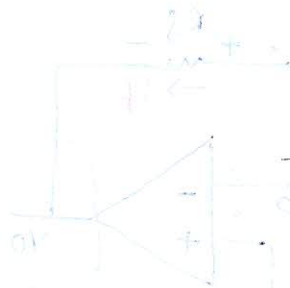
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$$n=10$$

$$VFS = 10.24 = V_r$$

$$Res = \frac{10.24}{2^{10-1}} = 10mV$$

$$\pm \frac{LSB}{2} = \pm 5mV$$



calibrated i.e. Error is zero

$$25^\circ \rightarrow 5mV$$

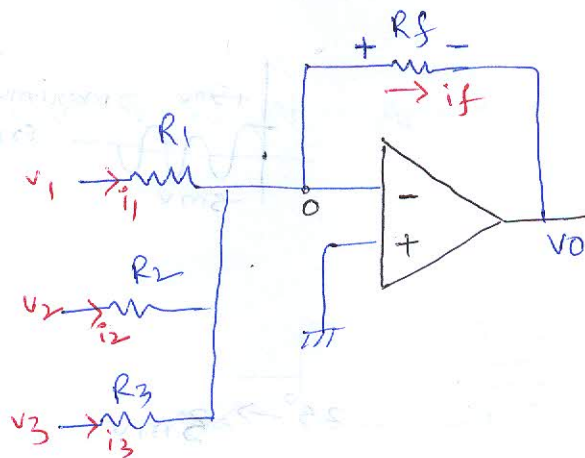
$$1^\circ \rightarrow \frac{5}{25} mV$$

$$\downarrow$$

$$200\mu V/c$$

⇒ DAC CKTS:-

⇒ Summing amplifier:-



$$i_1 = \frac{V_1}{R_1}$$

$$i_2 = \frac{V_2}{R_2}$$

$$i_3 = \frac{V_3}{R_3}$$

$$i_f = i_1 + i_2 + i_3$$

$$V_0 = -i_f R_f = -R_f (i_1 + i_2 + i_3)$$

$$\rightarrow V_0 = -R_f \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \dots \right]$$

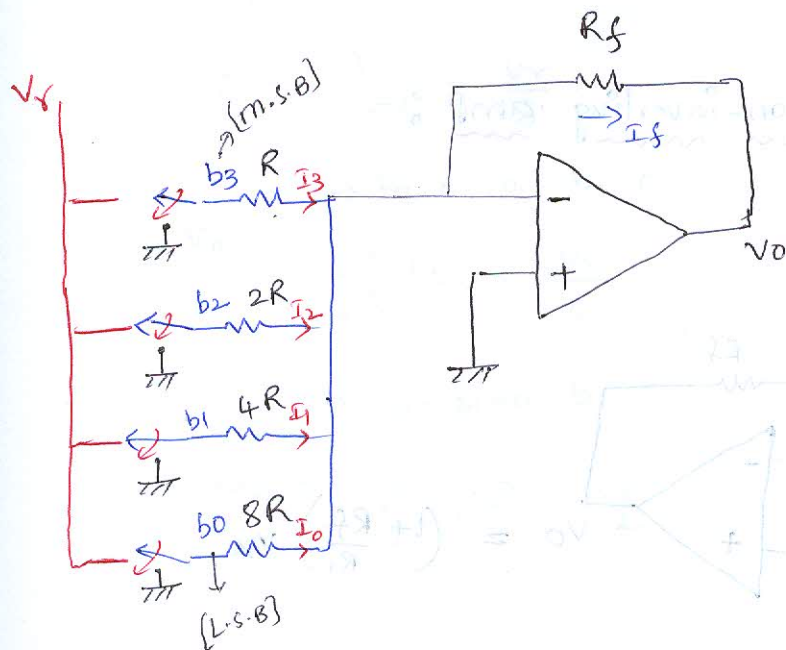
→ DAC — weighted Resistor

R-2R ladder Resistor

$$\rightarrow V_0 = \text{Resolution} \times \text{Decimal} \times \text{gain of amplifier}$$

DAC

⇒ Weighted Resistor DAC :-



→

$$I_3 = \frac{V_R}{R} b_3 -$$

$$I_2 = \frac{V_R}{2R} b_2 -$$

$$I_1 = \frac{V_R}{4R} b_1 -$$

$$I_0 = \frac{V_R}{8R} b_0 -$$

$$\rightarrow I_f = I_0 + I_1 + I_2 + I_3 + \dots$$

→

$$V_o = -I_f R_f$$

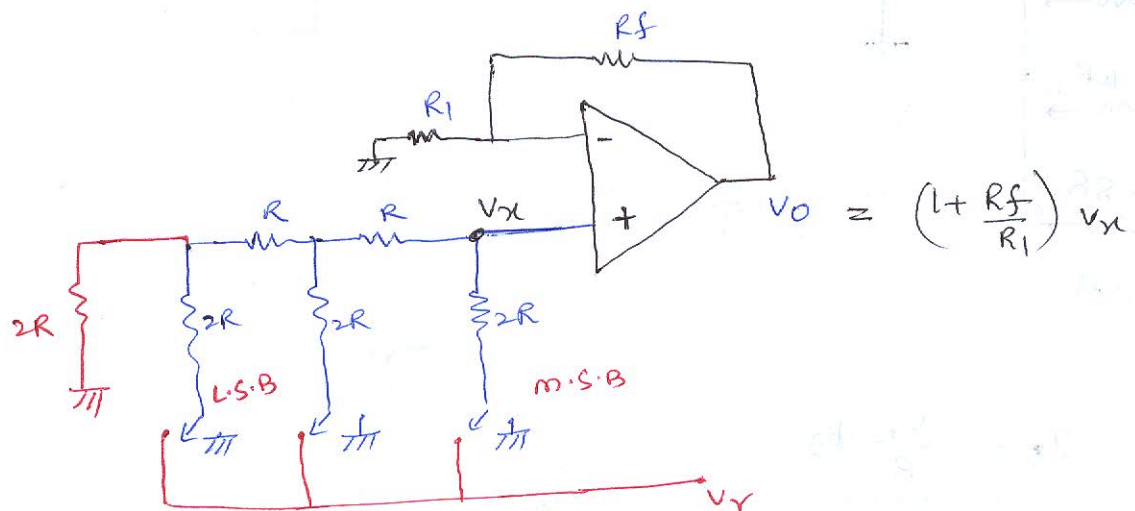
→ disadvantage of weighted Resistor DAC is

Accuracy is less to overcome this R-2R ladder
N/w is used.

⇒ R-2R Ladder Nlw :-

- 1) Normal Ladder { Non-inverting amp
 2) Inverted Ladder { Inverting amp.

⇒ R-2R Ladder using Non-inverting amp :-



→ adjacent of Last $\left(\begin{matrix} 2R \\ \parallel \\ \text{Ground} \end{matrix} \right)$ resistor is an L.S.B which is connected to Ground

→ $V_o = \left(1 + \frac{R_f}{R_1}\right) V_x$

→ $V_x = \text{Resolution} \times \text{Decimal value}$

$$V_o = \underbrace{\frac{V_r}{2^n}}_{\text{Resolution}} \times \underbrace{\sum_{i=0}^{n-1} 2^i b_i}_{\text{Decimal}} \underbrace{\left(1 + \frac{R_f}{R_1}\right)}_{\text{gain}}$$

$$\rightarrow V_n = \frac{V_r}{2^n} \sum_{i=0}^{n-1} 2^i b_i$$

$$\rightarrow b_0=1 \quad b_2=0=b_1=0$$

$$\rightarrow V_{n0} = \frac{V_r}{2^3} = \frac{V_r}{8}$$

$$\rightarrow b_0=b_2=0 \quad b_1=0$$

$$\rightarrow V_{n1} = \frac{V_r}{2^3} [2] = \frac{V_r}{4}$$

$$\rightarrow b_0=b_1=0 \quad b_2=1$$

$$\rightarrow V_{n2} = \frac{V_r}{2^3} [4] = \frac{V_r}{2}$$

$$\rightarrow V_n = V_{n0} + V_{n1} + V_{n2}$$

$$= \frac{V_r}{2} b_2 + \frac{V_r}{4} b_1 + \frac{V_r}{8} b_0$$

$$\left\{ V_n = \frac{V_r}{8} [4b_2 + 2b_1 + b_0] \right\}$$

$$V_n = \frac{V_r}{2^n} \sum_{i=0}^{n-1} 2^i b_i$$

$$\rightarrow V_o = \frac{V_r}{2^n} \sum_{i=0}^{n-1} 2^i b_i \left(1 + \frac{R_f}{R_i} \right)$$

Res. decimal gain.

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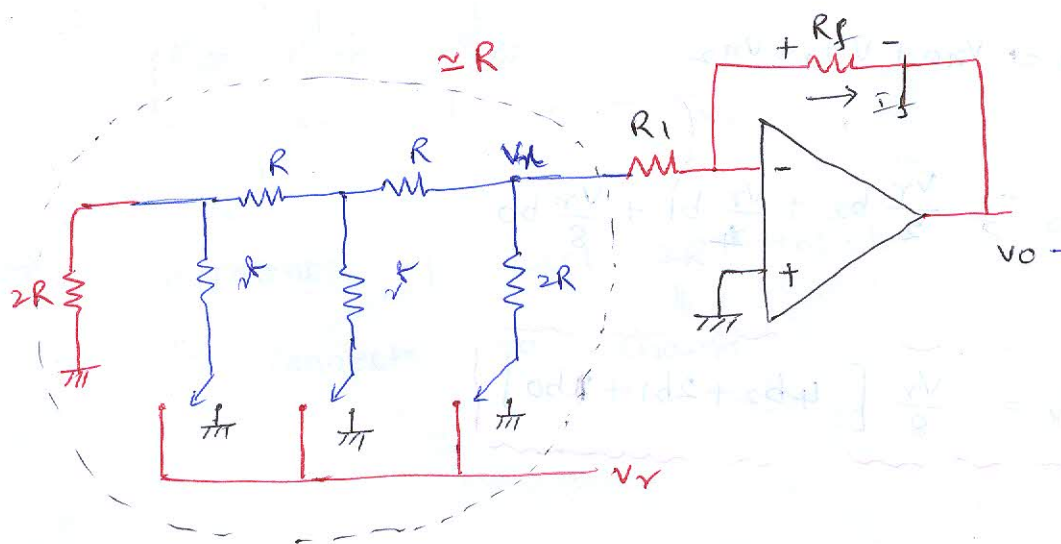
$$V_o = \frac{V_r}{2^n} \times \text{Decimal} \times \text{gain}$$

$$1010 \rightarrow \underline{10}$$

$$= \frac{V_r}{2^4} \times 10 \times (1+7)$$

$$= \frac{1}{16} \times 10 \times 8 = \underline{5}$$

⇒ R-2R Ladder using inverting amp :-



$$\rightarrow V_o = \frac{V_r}{2^n} \times \sum_{i=0}^{n-1} 2^i b_i \times \left(\frac{-R_f}{R_1 + R} \right)$$

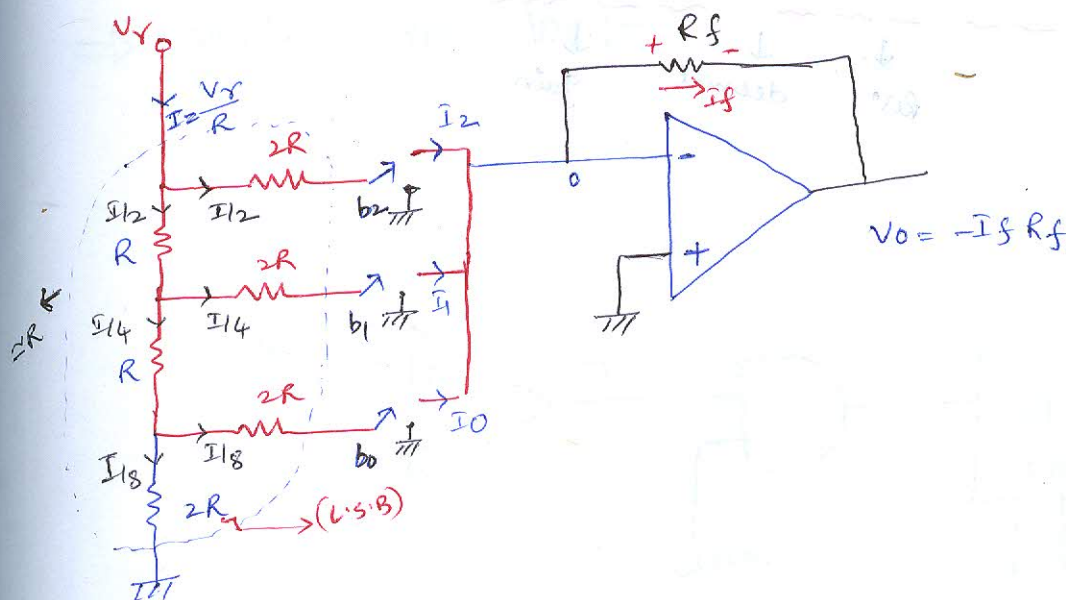
↓
gain

$$\rightarrow V_o = -I_f R_f$$

$$\rightarrow I_f = \frac{V_r}{2^n} \times \sum_{i=0}^{n-1} 2^i b_i \left(\frac{1}{R_1 + R} \right)$$

→ In normal ladder ckt when logic 1 and 0 signals are applied then transients will present at the o/p due to charging and discharging action of switch (mosFET). To overcome this inverted Ladder ckt is used.

⇒ Inverted R-2R Ladder DAC :-



$$\rightarrow I_2 = \frac{I}{2} \times b_2 \quad I_1 = \frac{I}{4} \times b_1 \quad I_0 = \frac{I}{8} \times b_0$$

$$\left\{ I_f = \frac{I}{2} b_2 + \frac{I}{4} b_1 + \frac{I}{8} b_0 \right\}$$

$$I_f = \frac{I}{8} (4b_2 + 2b_1 + b_0)$$

$$I_f = \frac{I}{8} \{4b_2 + 2b_1 + b_0\}$$

$$\rightarrow I_f = \frac{I}{2^n} \sum_{i=0}^{n-1} 2^i b_i$$

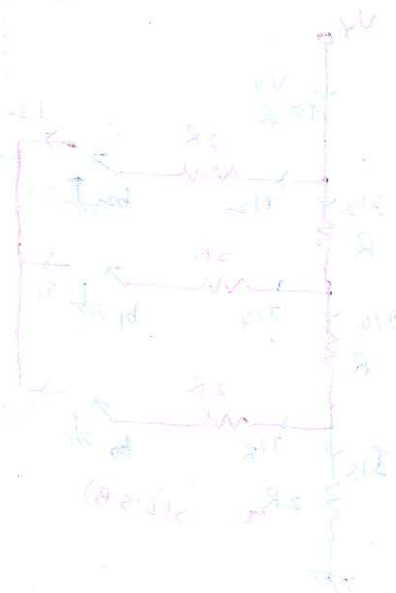
$$I = \frac{V_r}{R}$$

$$I_f = \frac{V_r}{2^n} \times \left(\sum_{i=0}^{n-1} 2^i b_i \right) \frac{1}{R}$$

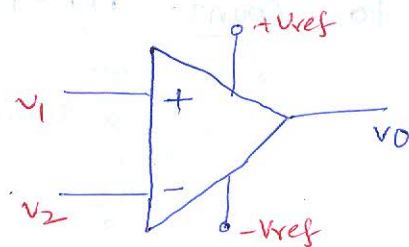
$$V_o = -I_f R_f$$

$$\rightarrow V_o = \frac{V_r}{2^n} \times \sum_{i=0}^{n-1} 2^i b_i \times \left(-\frac{R_f}{R} \right)$$

↓
Res.
↓
decimal
↓
gain.



ADC



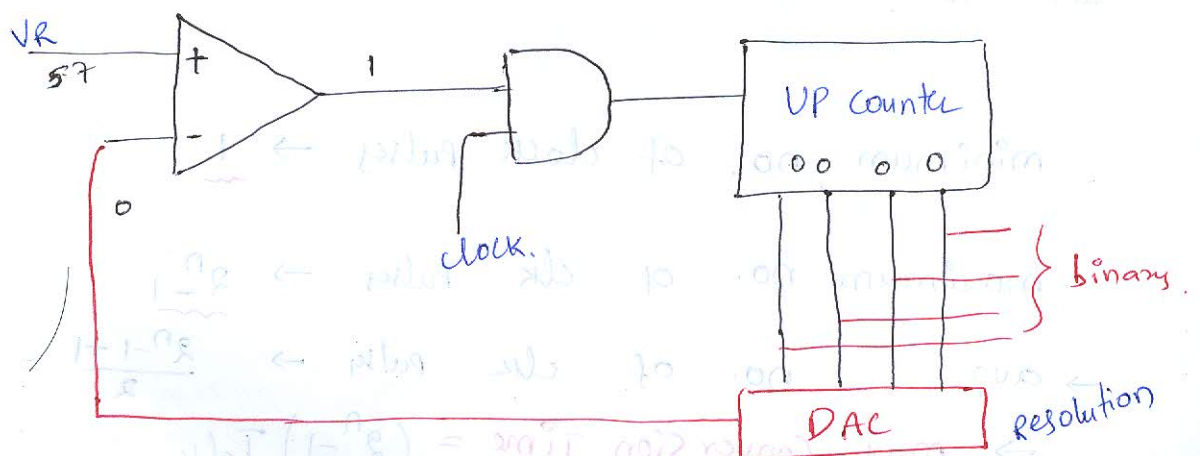
$$(V_1 = V_2 = ?)$$

$$\rightarrow V_1 > V_2 \Rightarrow V_0 = +V_{ref} = \text{logic } 1 \checkmark$$

$$\rightarrow V_1 < V_2 \Rightarrow V_0 = -V_{ref} = \text{logic } 0 \checkmark$$

→ Comparator is an 1-bit Quantizer:-

⇒ Counter Type ADC:-



$$\rightarrow \text{max Error} = \text{Resolution of DAC}$$

→ In Counter Type ADC a Comparator is used at i/p to compare i/p Analog voltage with feed back voltage provided by DAC in feedback.

→ a up counter is used to count no. of clock pulses

⇒ operation :-

→ when Analog voltage is greater than feedback voltage then olp of comparator will become logic 1 and counter will increments continuously

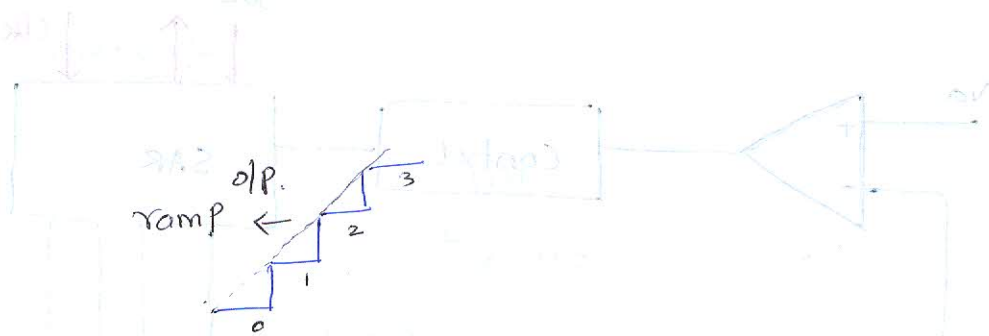
→ when Analog voltage is less than feedback voltage then olp of comparator is logic 0 and counter will stop at this time olp of counter will provide binary equivalent of Analog voltage.

→ / minimum no. of clock pulses → 1
maximum no. of clk pulses → $2^n - 1$
→ avg. no. of clk pulses → $\frac{2^n - 1 + 1}{2} = \underline{2^{n-1}}$
→ max Conversion Time = $(2^n - 1) T_{clk}$

→ Avg Conversion Time = $(2^{n-1}) T_{clk}$

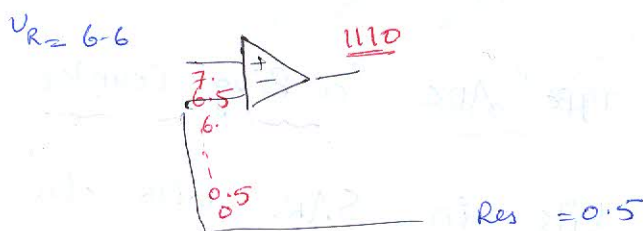
→ Conversion Time depend on i/p Analog voltage.

→ Counter Type ADC is also known as Ramp Type ADC

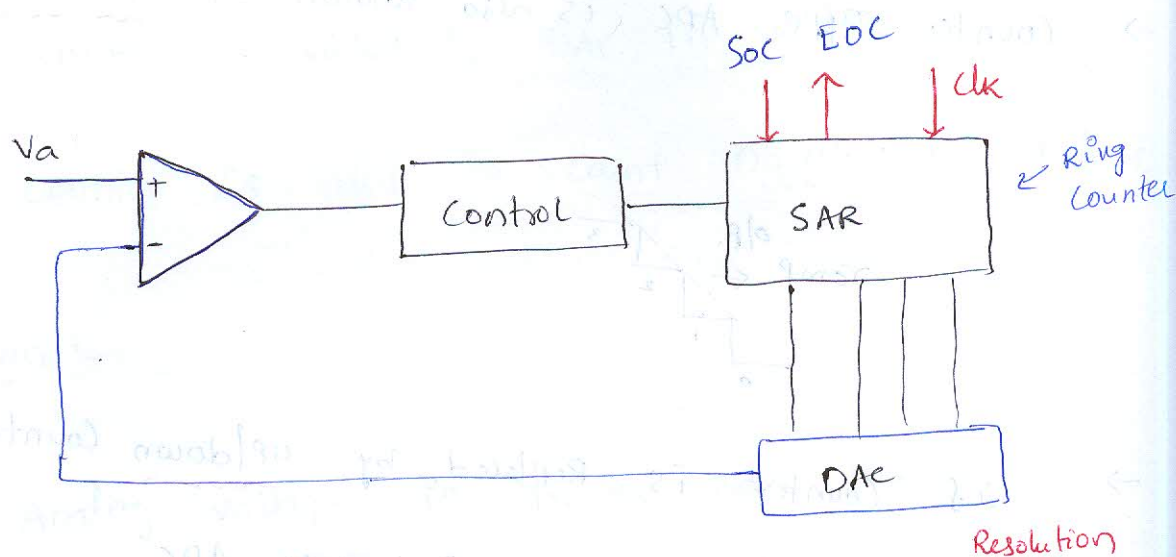


→ If Counter is Replaced by up/down Counter then it is known as Tracking Type ADC.

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→ Successive Approximation Register ADC :-



→ Soc - Start of Conversion

→ EOC - End of Conversion [Interrupt]

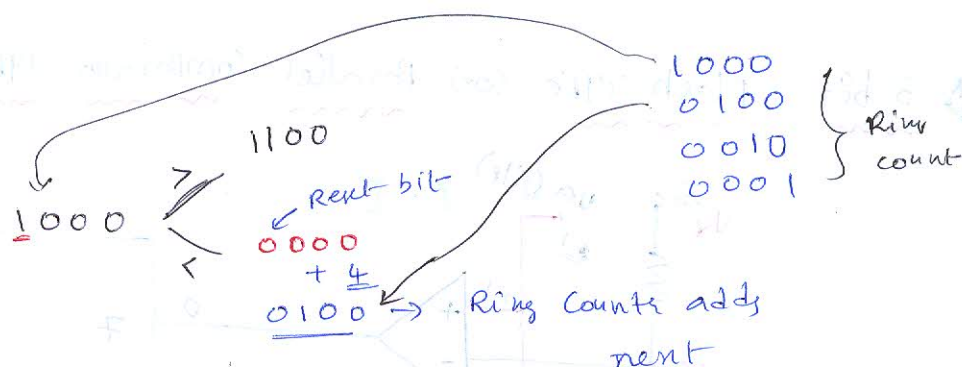
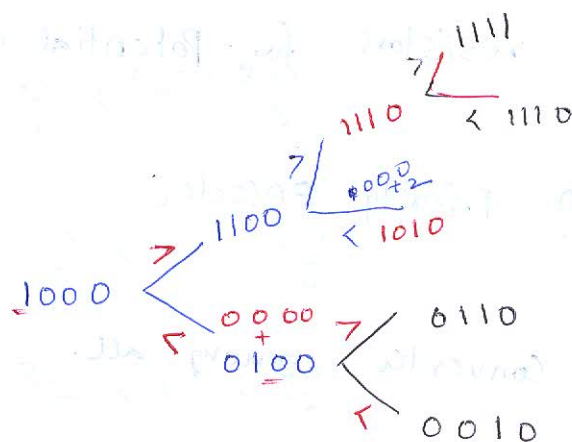
→ In a SAR type ADC a Ring Counter is used successively to set bits in SAR. with clk

→ control ckt is used to reset current set bit by ring counter when Analog voltage is less than feedback voltage

→ m.s.B will be set

1 0 0 0 -
 0 1 0 0 - } Ring Counter
 0 0 1 0 -
 0 0 0 1 -

→ operation :-



→ In SAR TYPE ADC maximum no. of clk pulses required
for n-bit conversion only n

⇒ Conversion Time = $n T_{clk}$

→ Conversion Time is independent of i/p Analog voltage.

→ It have uniform conversion time of $\frac{1}{f_{clk}}$ per μs for any analog vol

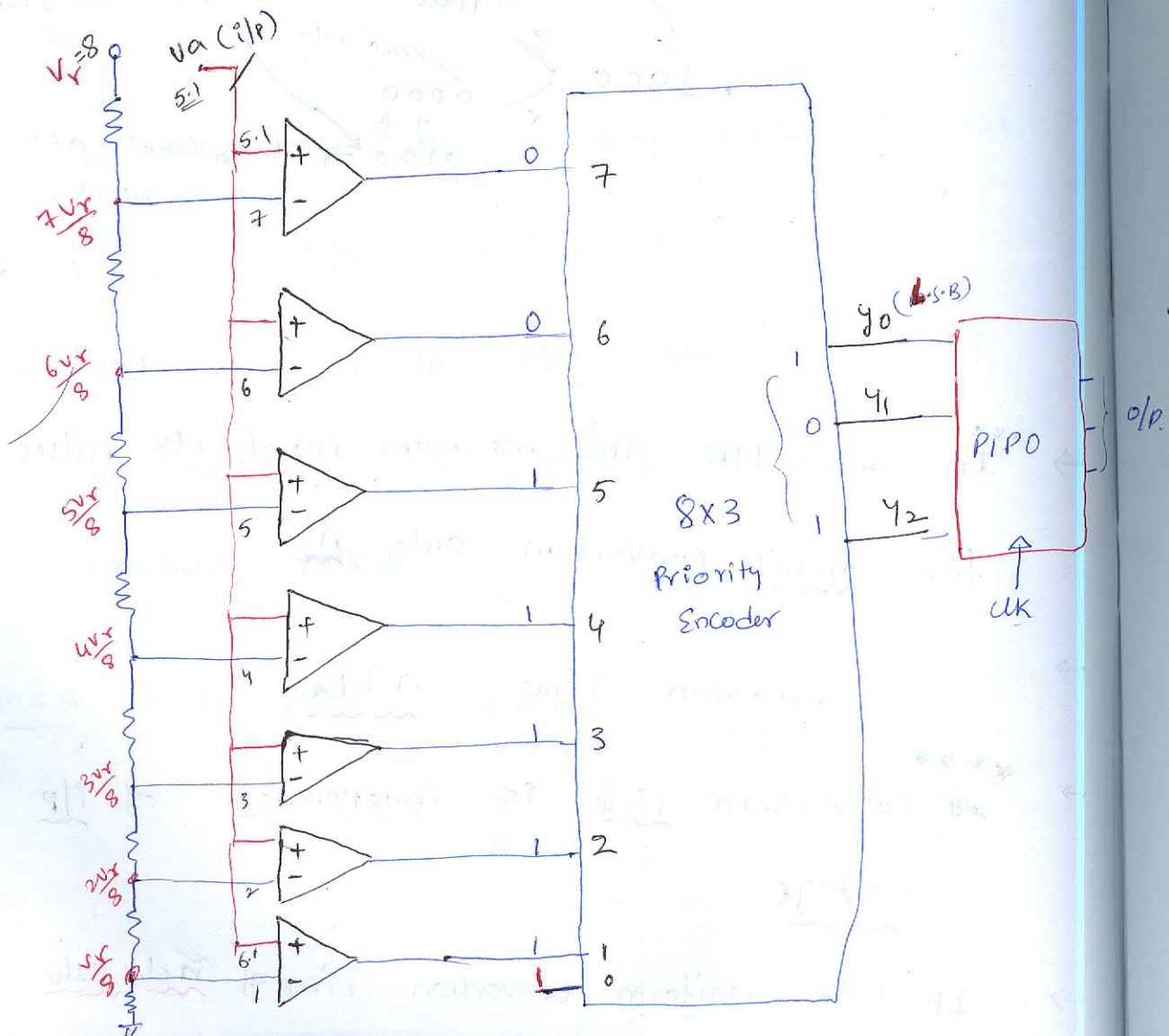
Comparator

⇒ Flash Type (or) Parallel Type (or) Simultaneous Converter Type :-

- * n-bit → $2^n - 1$ Comparators required
- 2^n resistors for Potential divider
- $2^n \times n$ Priority Encoder

→ *** fastest ADC Converter among all.

⇒ 3 bit Flash Type (or) Parallel Comparator Type :-



→

analog voltage

Range

$$V_a < \frac{V_r}{8}$$

$$\frac{V_r}{8} < V_a < \frac{2V_r}{8}$$

$$\frac{2V_r}{8} < V_a < \frac{3V_r}{8}$$

$$\frac{3V_r}{8} < V_a < \frac{4V_r}{8}$$

o/p
y₂ y₁ y₀

0 0 0

0 0 1

0 1 0

0 1 1

$$V_a > \frac{7V_r}{8}$$

1 1 1

Q

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$$V_o = -I_f \times R_f$$

$$= -I_f \times \frac{V}{R} \left[\frac{K}{1} \right]$$

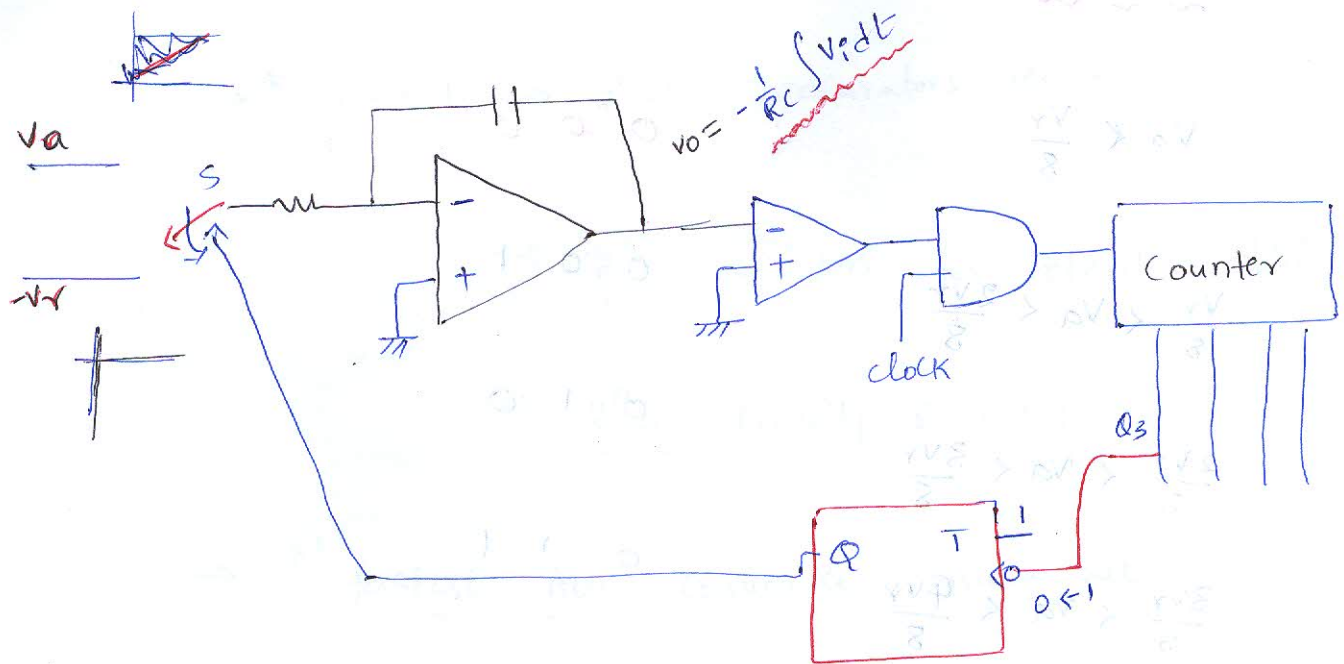
Tolerance $R = \pm 10\%$, $V = \pm 10\%$

$$V_o \text{ with TOL} = \frac{-(1+0.1)I_f (1+0.1)V}{(1-0.1)R} = \frac{-(1.1)I_f \times (1.1)V}{0.9R}$$

$$\frac{V_o \text{ TOL}}{V_o} = 0.345 \%$$

or take sub as TOL

⇒ Dual slope Integrating Type :-



→ most accurate ADC

→ mostly used in Digital voltmeter

→ max no. of clock pulses - 2^{n+1}

→ Slower ADC

→ Analog voltage is integrated for 2^n clock pulses

Q.14

→ The ckt shown in fig is dual slope ADC ckt

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D₃ D₂ D₁ D₀
 ↓ ↓ ↓ ↓
 Q₂ Q₁ Q₀

0 0 0 0

0 0 0 1

0 0 1 0

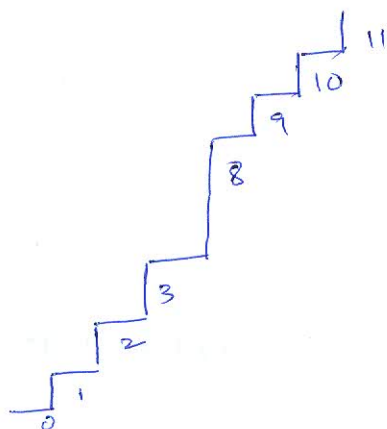
0 0 1 1

1 0 0 0

1 0 0 1

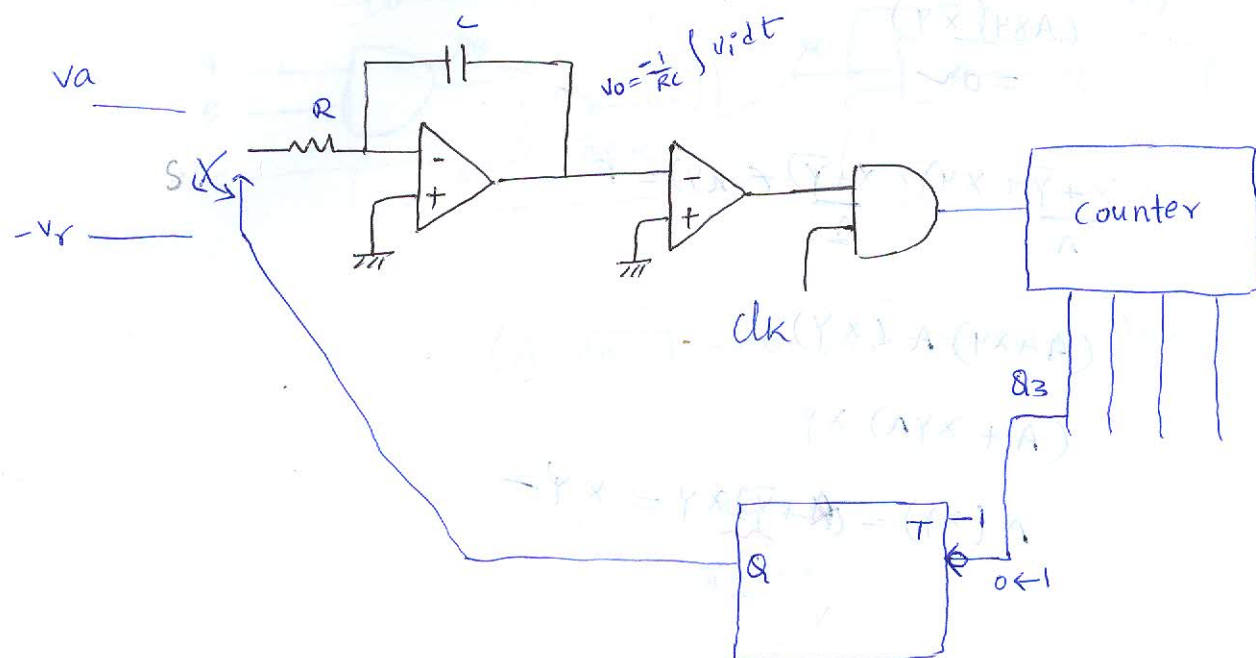
1 0 1 0

1 0 1 1



05/08/11

dual slope integrator ckt:-



→ A integrator ckt is used at input to integrate analog voltage V_a and reference voltage $-V_r$ ($|V_r| > |V_a|$)

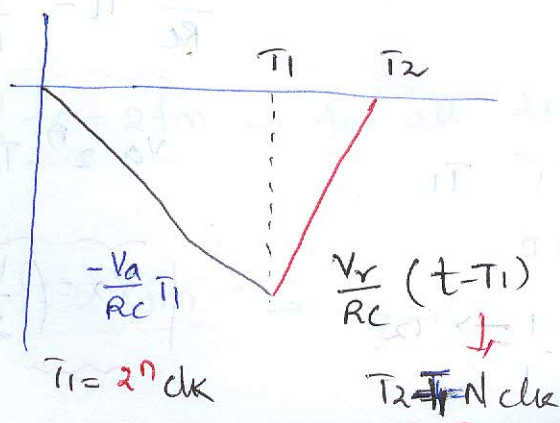
→ When conversion is started counter and T Flip Flop is reset into 0 and switch 'S' is connected to analog voltage V_a .

→ When analog voltage is integrating output of integrator is -ve and comparator output is

Logic 1

due to this clock pulses are continuously applied to counter and count will increment at time T_1 counter will reach again count to 0 at this time. Toggle Flip Flop toggles to logic 1 and switch S is connected to $-V_r$

→ during reference voltage integration slope will become positive but o/p of integrator is still negative voltage due to this o/p of comparator will become logic 1. the counter again starts counting clock pulses. at time T_2 o/p of integrator will become positive and comparator o/p will become logic 0 and counter will stop. let N is the count when counter is stopped at time T_2



→ The o/p integrator is given by

$$V_o = -\frac{V_a}{R_c} T_1 + \frac{V_r}{R_c} (t - T_1)$$

$$t = T_2 ; V_o = 0$$

$$0 = -\frac{V_a}{R_c} T_1 + \frac{V_r}{R_c} (t - T_1)$$

$$\frac{V_a}{R_c} T_1 = \frac{V_r}{R_c} (t - T_1)$$

$$(V_a + V_r) T_1 = V_r t$$

$$\frac{T_1}{t} = \frac{V_r}{V_a + V_r}$$

$$t = T_2$$

$$\frac{T_1}{T_2} = \frac{V_r}{V_a + V_r}$$

$$\rightarrow T_1 = 2^n T_{clk}$$

$$\rightarrow T_2 - T_1 = N T_{clk}$$

Q₃ Q₂ Q₁ Q₀
0 0 0 0

$$\frac{V_a}{R_c} T_1 = \frac{V_r}{R_c} (T_2 - T_1)$$

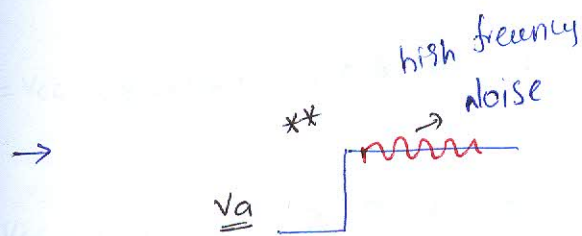
$$V_a 2^n T_{clk} = V_r N T_{clk}$$

T₁ flip change

1 1 1 1 T₁
↓
0 0 0 0
1 0 1 → T₂
1 1 1 1

$$V_a = \left(\frac{V_r}{2^n} \right) N$$

→ $V_a \propto N$



→ High frequency ripple is removed from analog voltage by low pass integrator so it is more accuracy

→ Total no. of clk pulses required is n bits

$clk = 2^n + N$

→ max no. of clk pulses = $2^n + (2^n - 1)$
 $\approx 2^{n+1}$

→

Sample | Hold circuit → before all ADCs

Normal ADC Converters use Normal sampling rate

$f_s = 2f_m$ → for all ADCs

→ $f_s > 2f_m$ → $\leq -\Delta$