

Logic families

→ fundamentals

characteristics

RTL

DCTL

I^2L

DTL

HTL

TTL

ECL ✓

NMOS ✓

(CMOS) ✓

→

I_{EB}

I_{CB}

RB

RB

→ cutoff → off switch

FB

FB

→ Sat → on

FB

RB

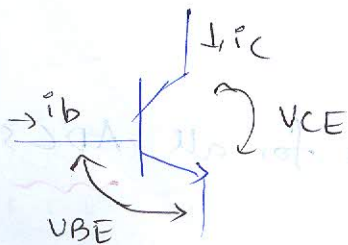
→ Active

RB

FB

→ Reverse active

⇒



$V_{BE} < 0.6V$

$V_{BE} 0.6 \text{ to } 0.7$

→ $V_{CE} = V_{CC} \rightarrow V_{BE} < 0.6V \rightarrow$ Cut-off → $I_C \approx 0$

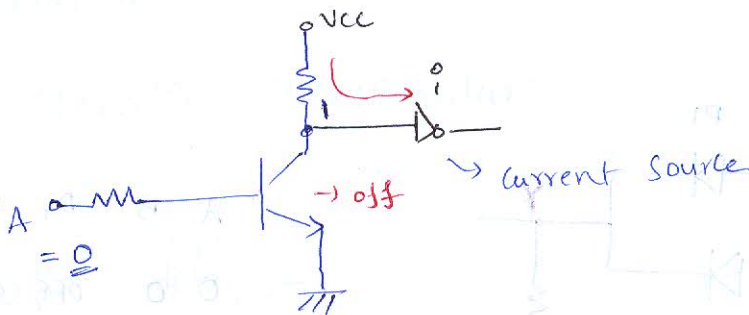
→ $V_{CE} = V_{CC} - I_C R_C \rightarrow V_{BE} \rightarrow 0.6$ to $0.7V \rightarrow$ Active → $I_C = \beta I_B$

→ $V_{CE} \approx 0.2V \rightarrow V_{BE} \gg 0.7V \rightarrow$ Sat → $I_C = \frac{V_{CC}}{R_C}$

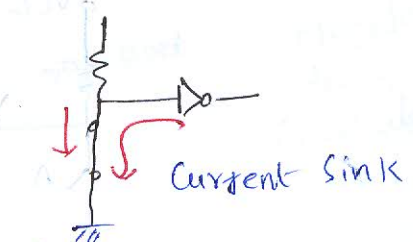
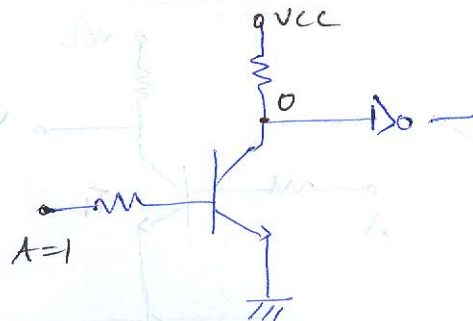
$V_{CE\text{ sat}} = 0.2V$ ✓

$V_{BE\text{ sat}} = 0.7V$ ✓

⇒ Not gate :-

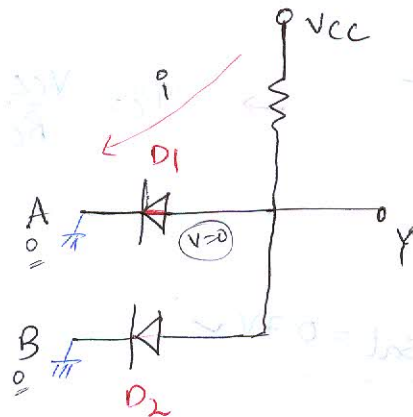


→ when logic gate o/p is in logic 1 level [Trans off]
then it will acts as Current Source



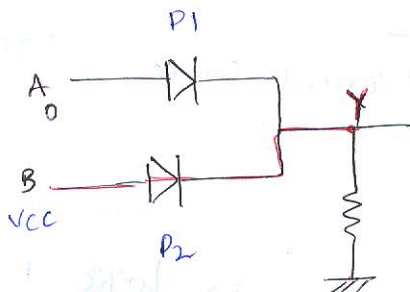
→ when logic gate o/p is 0 [Trans in on state]
then it will acts as Current Sink

⇒ AND gate using diode :-



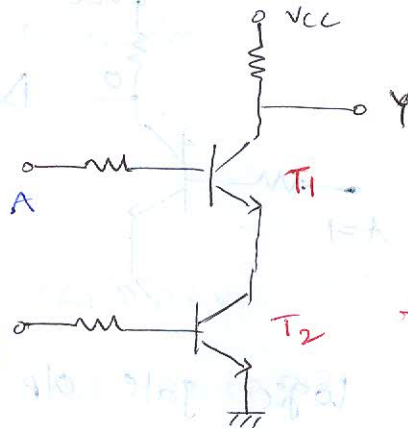
<u>A</u>	<u>B</u>	<u>D₁</u>	<u>D₂</u>	<u>Y</u>
0	0	on	on	0
0	1	on	off	0
1	0	off	on	0
1	1	off	off	1 ✓

⇒ OR gate :-



<u>A</u>	<u>B</u>	<u>D₁</u>	<u>D₂</u>	<u>Y</u>
0	0	off	off	0
0	1	off	on	1
1	0	on	off	1
1	1	on	on	1

⇒ NAND



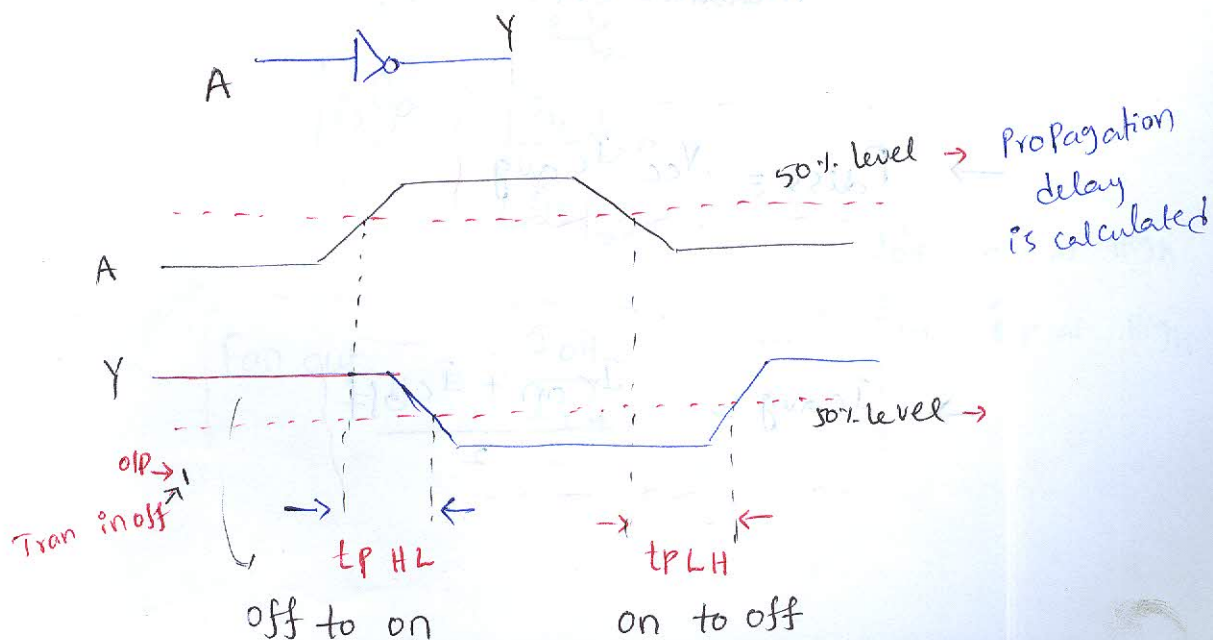
<u>A</u>	<u>B</u>	<u>Y</u>
0	0	V _{CC} = 1
0	1	1
1	0	1
1	1	0 ✓

⇒ characteristics of Logic families :-

- 1) t_{pd} ✓
- 2) Power dissipation ✓
- 3) Figure of merit ✓
- 4) Fan out ✓
- 5) Noise margin ✓
- 6) Wired logic ✓
- 7) Fan in
- 8) operating Temperature.

⇒ Propagation delay :-

→ Propagation delay is measured in Nano Seconds



→ In Transistor $t_{p\text{ LH}} > t_{p\text{ HL}}$ due to
on to off off to on

Saturation delay (or) storage time

→

$$\rightarrow t_{pd} = \frac{t_{p\text{ HL}} + t_{p\text{ LH}}}{2}$$

→ Propagation delay is calculated at 50% level
of voltage.

⇒ Power dissipation :-

it represents power dissipated for logic
gate.

→ mw

↓

measured in mw

$$\rightarrow P_{diss} = V_{cc} I_{c\text{ avg}}$$

$$\rightarrow I_{c\text{ avg}} = \frac{I_{c\text{ on}} + I_{c\text{ off}}}{2}$$

⇒ Figure of merit :-

Product of propagation delay and power dissipation

$$\Rightarrow \text{Figure of Merit} = \uparrow t_{pd} \times P_{diss} \downarrow$$

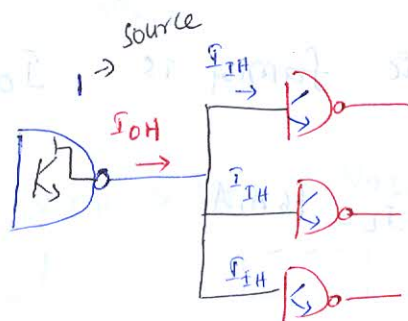
$$\downarrow \text{constant} \quad \downarrow \text{mw} \quad \downarrow \text{ns}$$

$$= \underline{PJ}$$

→ *** I_L^2 → less figure merit 0.1 PJ - 0.7 PJ

⇒ Fanout :-

Fan out is the maximum no. of logic gates
that can be driven by a logic gate output



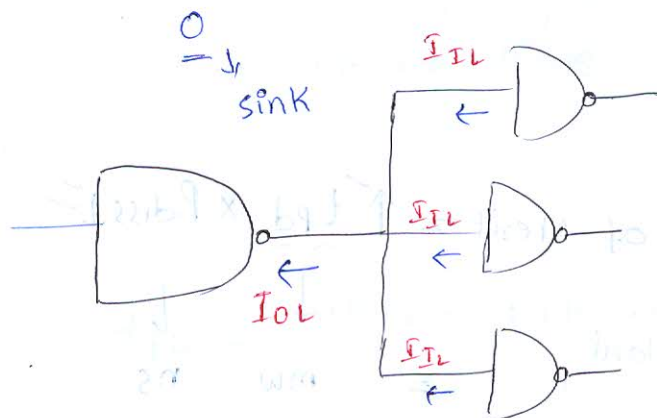
I_{OH} = o/p at High

I_{IH} = i/p at High

$$\boxed{\text{Fan out}_H = \frac{I_{OH}}{I_{IH}}}$$

$\downarrow$
i/p

⇒ fanout in low level:-



$$\text{fan out}_L = \frac{I_{OL}}{I_{IL}} \quad **$$

**

$$\text{over all fan out} = (\text{fan out}_H, \text{fan out}_L)_{\min}$$

$$f_H \rightarrow 10 \quad f_L \rightarrow 4$$

$$(f \rightarrow 4)$$

Q) In TTL logic family is $I_{OH} = 40 \mu A$ $I_{IH} = 4 \mu A$

$$I_{OL} = 16 \text{ mA} \quad I_{IL} = 1.6 \text{ mA}$$

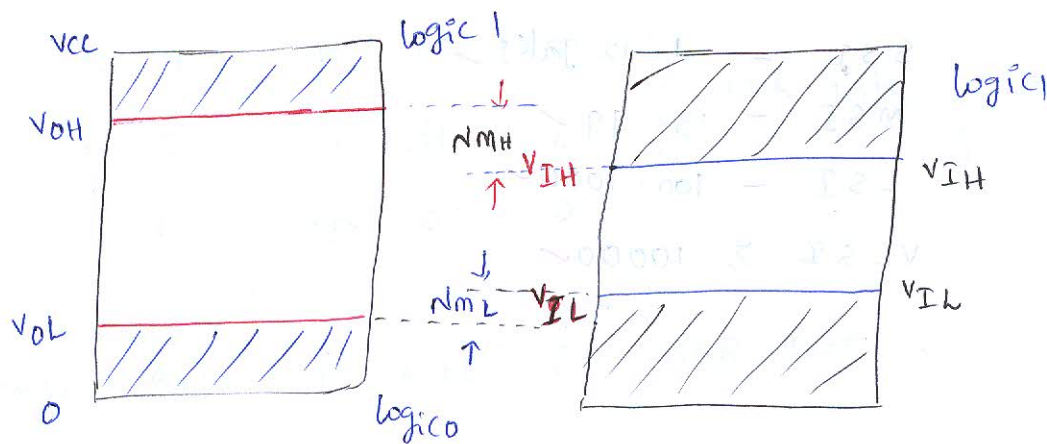
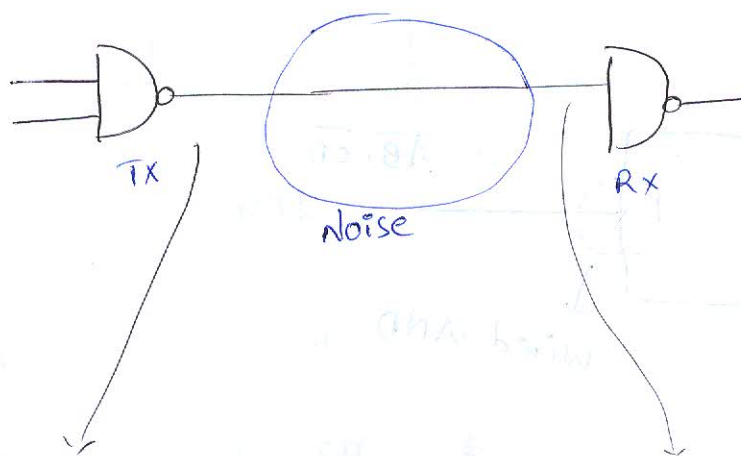
$$\text{Fanout} = (\text{Fanout}_H, \text{Fanout}_L)_{\min}$$

$$\text{fan out}_H = \frac{I_{OH}}{I_{IH}} = \frac{40}{4} = 10 \checkmark$$

$$\text{fan out}_L = \frac{I_{OL}}{I_{IL}} = \frac{16}{1.6} = 10 \checkmark$$

⇒ Noise Margin :-

Noise margin is the Maximum Noise Voltage that can be added to a logic gate input which will not effect the output



$$V_{OH} > V_{IH} > V_{IL} > V_{OL}$$



$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = 0.4$$

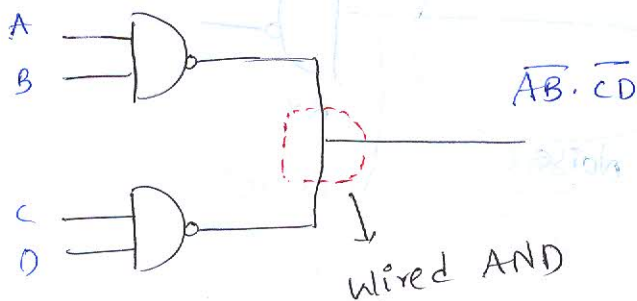
$$NM_L = 0.7$$

$$NM = 0.4$$

xx

$$\rightarrow \left(NM = (NM_H, NM_L)_{\min} \right)$$

Wired Logic :-



→

SSI - 1-12 gates

MSI - 13-99 ✓

LSI - 100-1000 ✓

VLSI ≥ 10000 ✓

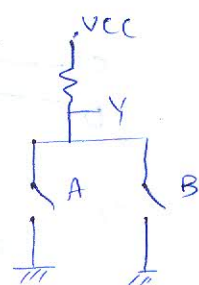
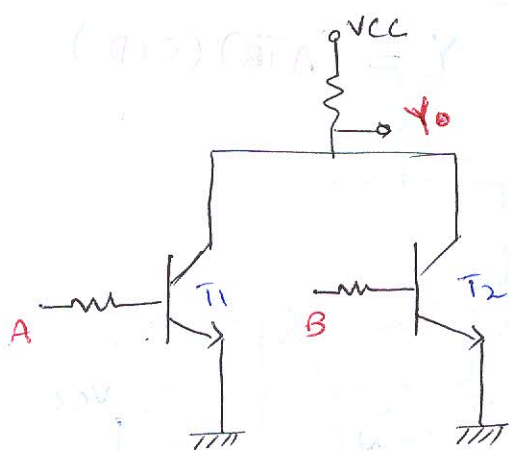
$f_{0.0} = 1 \text{ ns}$ $f_{0.0} = 1 \text{ ns}$

$\mu_{0.0} = \text{ms}$

$V_{OH} - V_{IH} = 1 \text{ ns}$

$V_{OL} - V_{IL} = 1 \text{ ns}$

Resistor Transistor Logic family (RTL) :-



NOR gate

RTL

<u>A</u>	<u>B</u>	<u>T₁</u>	<u>T₂</u>	<u>Y</u>
0	0	off	off	1
0	1	off	on	0
1	0	on	off	0
1	1	on	on	0

NOR gate

basic gate of RTL is NOR gate

Propagation delay = 50ns

Noise margin = 0.2V

P_{diss} = 10mW

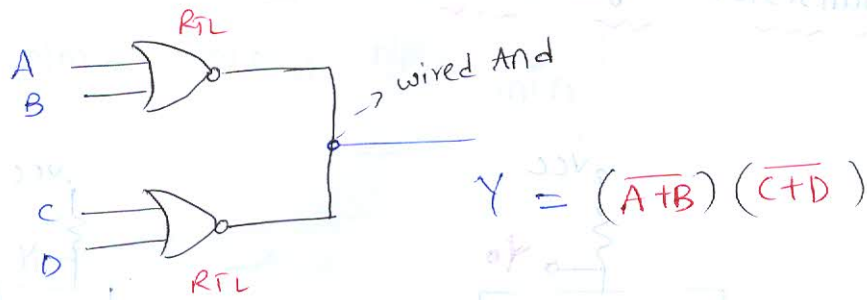
Figure of merit = 10 x 50 = 500 PT

Fan out = 3

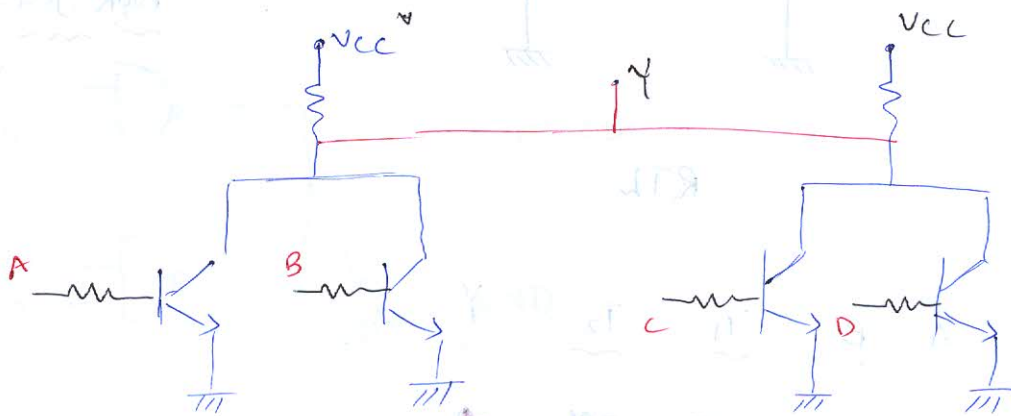
Wired AND logic

Two RTL gates are connected as shown in fig

→



⇒



A	B	C	D	Y
0	0	0	0	1 ✓
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0 ✓

$$\overline{A} \overline{B} \overline{C} \overline{D}$$

↓

$$= (\overline{A+B})(\overline{C+D})$$

$$= Y$$

↓

xx

→ So wire is acting as

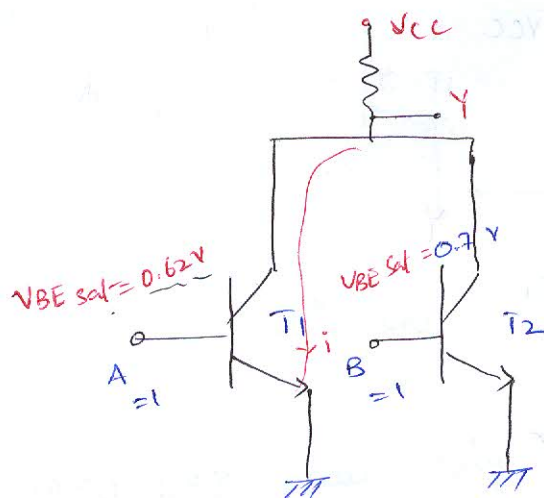
And gate

disadvantages

- 1) Speed of operation is less
- 2) lower fan out
- 3) Lower noise margin

OC/OS/11

⇒ Direct Coupled Transistor Logic :-



R_C - is low

→ $t_{pd} = 40\text{ns}$

→ NOR gate

A	B	T ₁	T ₂	Y
0	0	off	off	1
0	1	off	on	0
1	0	on	off	0
1	1	on	off	0

→ disadvantage of DCTL logic family is current hogging

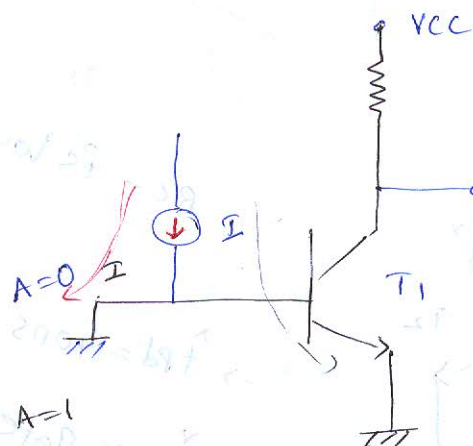
→ In DCTL logic family if transistors having

different $V_{BE\text{ sat}}$ voltage is used then transistor

having lower $V_{BE\text{ sat}}$ will be come on and it will not allow to other transistor to on.

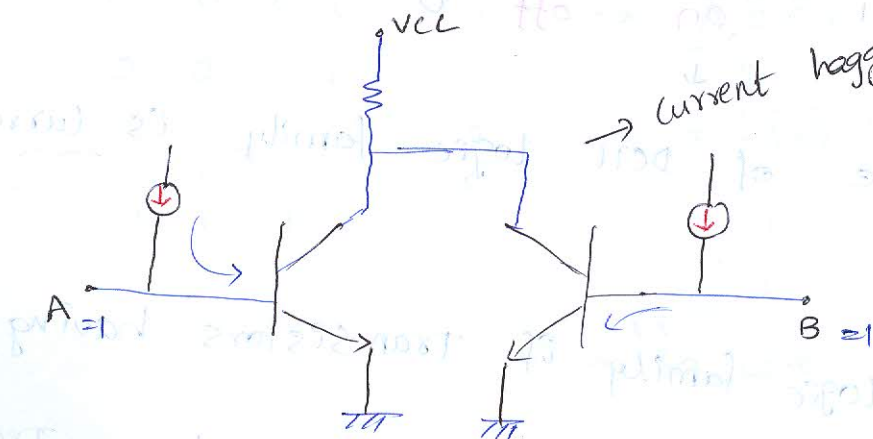
(IL)

⇒ Integrated Injection Logic :-



A	T ₁	Y
0	off	1
1	on	0

→

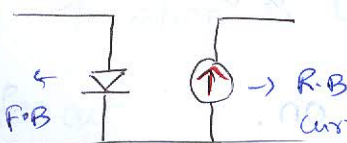


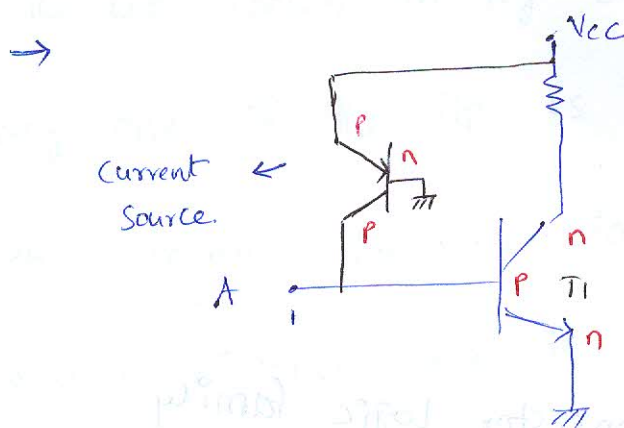
→ current lagging is Not Present in this ckt

→

BJT
EB → FB
CB → RB

PNP





I^2L ckt

→ MSI, LSI uses only - I^2L ckt

↓
Bipolar logic family used in LSI, MSI is I^2L

→ In I^2L logic family due to use of Current Source
no current hogging problem.

→ In this PNP and NPN transistors are integrated
together due to this transistors will occupies
less area hence density is more

→ It is mostly used in MSI and LSI logic family

→ It have best figure of merit among all logic
families

0.1 PS → 0.7 PS

→ $t_{pd} = 40\text{ns}$

fanout = 8

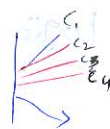
NM = 0.35V

MTL → Merged Transistor logic family

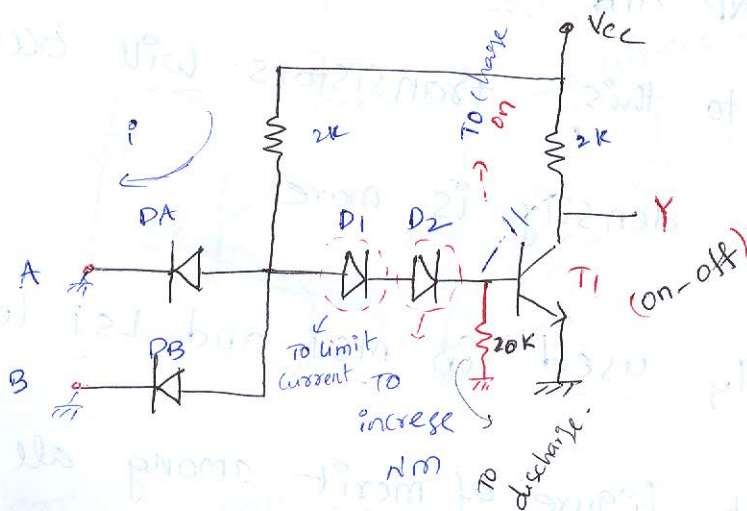
↓

I^2L (another name)

→ multi collector o/ps will present in I^2L family



⇒ DTL → Diode Transistor logic family:-



<u>A</u>	<u>B</u>	<u>T₁</u>	<u>Y</u>
0	0	OFF	1
0	1	OFF	1
1	0	OFF	1
1	1	ON	0

NAND gate.

→ The ckt shown in fig Basic DTL gate. In this any one of the i/p is low then i/p diodes DA (or) DB become forward biased where as D_1 and D_2 are reverse biased. due to this Transistor T_1 is off o/p is logic 1.

→ when all the i/p's are high i/p diodes are reverse biased where as D_1 and D_2 are forward diode biased where as Transistor on o/p is Logic 0.

→ Basic gate - NAND

→ $t_{pd} = 30 \text{ ns}$ ✓

→ $P_{diss} = 8 \text{ mW}$ ✓

→ figure of merit = 240 PJ

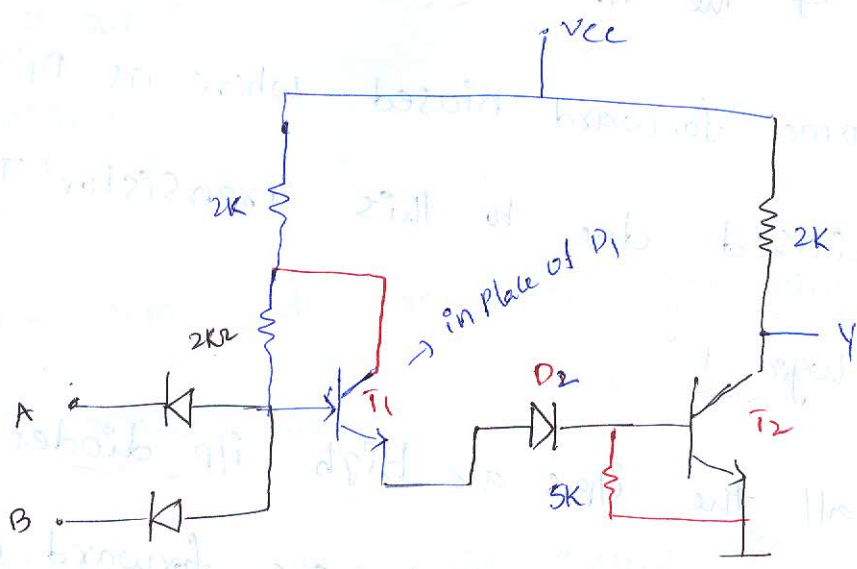
→ $N_m = 0.75 \text{ V}$ ✓

→ $\text{fan out} = 3$

*
→ Wired AND logic

→ If one more diode is placed in Series with D_1, D_2 then N_m may increase but fan out will decrease [$I_B \downarrow, I_C \downarrow \rightarrow \text{so fan out} \downarrow$]

⇒ To improve fanout :-



ICDTL
Integrated DTL

Now

→ Fanout = 8

$I_E = (\beta + 1) I_B$

→ To improve fanout diode D1 is replaced by Transistor T2 and resultant logic family is known as ICDTL

→ Diode Temperature co-efficient

↓

$\frac{dv}{dT} = -2.3 \text{ mV}/^\circ\text{C}$

Transistor



Zener diode

Zener break

→ Heavily doped

Electric field

rupture of covalent bonds

$< 6V$

-ve Temp/°C

Avalanche Breakdown

lightly doped

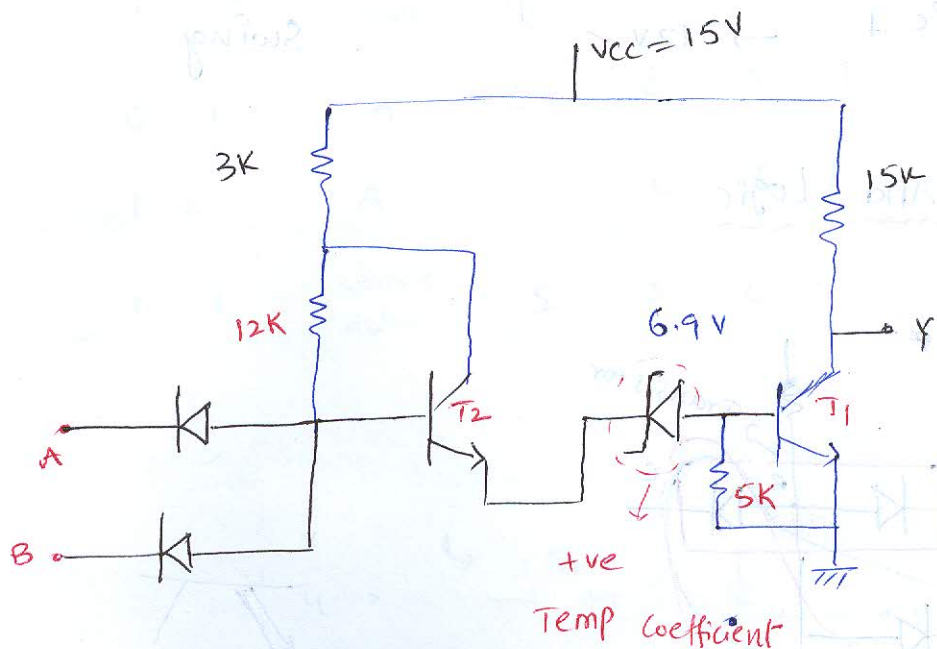
Temp

collisions

$> 6V$

+ve Temp/°C

⇒ High Threshold logic family (HTL) :-



→ Basic gate - Nand

**

→ NM → 4V - 5V ✓

↓
(Industrial)

→ more Noise immunity

↓
with standing

→ *

$t_{pd} = 90 \text{ ns}$ →

$R_C \approx R_{\uparrow C}$ So

→ *

$P_{diss} = 55 \text{ mW}$

→ *

figure of merit = 5000 PJ

→

Fan out = 10 → ($V \uparrow$ $I_C \uparrow$ so Fanout $\uparrow$)

→

**

logic = 0 →

2V ✓

**

logic 1 →

12V ✓

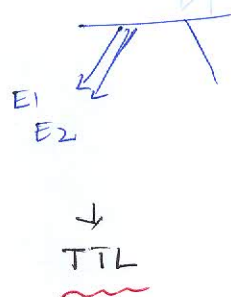
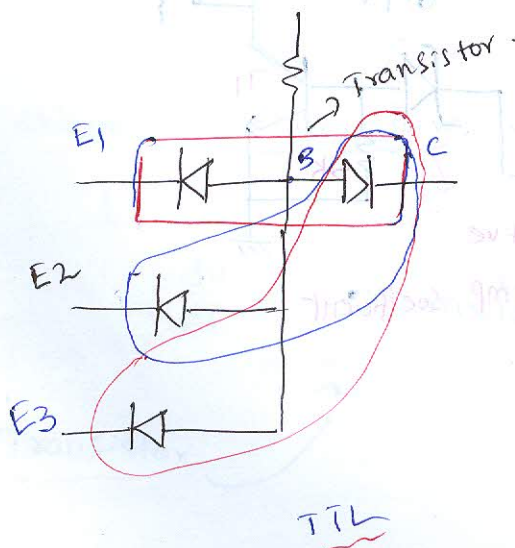
10V

Higher voltage
Swing

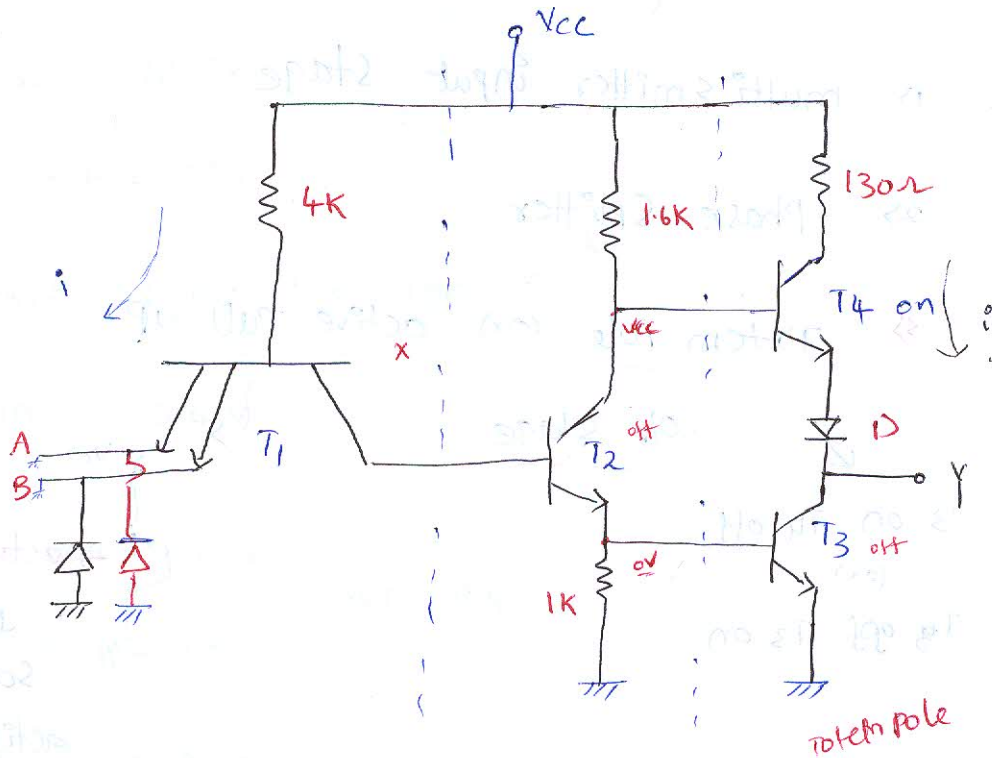
→

Wired And Logic

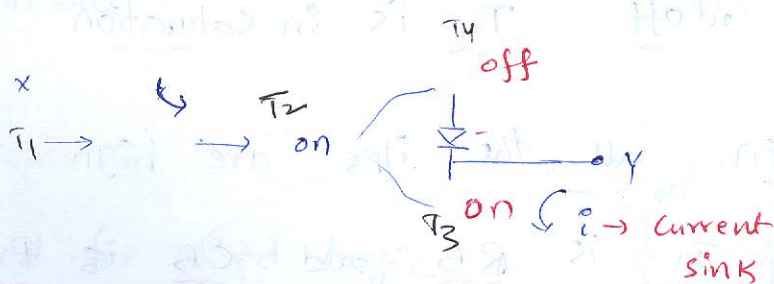
→



⇒ TTh → Transistor Transistor Logic family! -



	A	B	T ₁	T ₂	T ₃	T ₄	Y
→	0	0	Active mode	Cut off	Cut off	Sat	1
	0	1	A	C	C	S	1
	1	0	A	C	C	S	1
	1	1	Reverse active	S	S	C	0



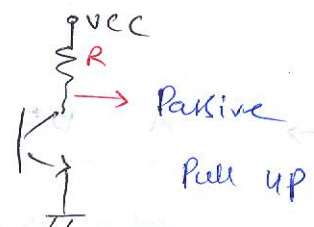
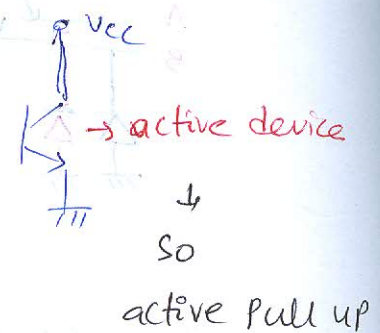
→ The ckt shown in fig is standard TTL
it basically contains Three stages

1) multi emitter input stage

2) Phase Splitter

3) Totem Pole (or) active pull up

o/p stage
 T_3 on T_4 off
 (or)
 T_3 off T_4 on



→ In TTL logic family if any one of the i/p is low E.B of T_1 is F.B and C.B R.B
 [T_1 is in active mode] due to this T_2 & T_3
 are Cutoff T_4 is in saturation and o/p is 1

→ When all the i/p's are high then emitter
Base T_1 is R.B and C.B is F.B [T_1 is in inverse
active mode] due to this T_2 & T_3 are in ON state
 T_4 is cutoff o/p is logic 0

① Basic gate — Nand

② ^{**} $t_{pd} = \underline{10ns}$

③ $P_{diss} = \underline{10mw}$

④ ^{**} Fan out = 10 ✓

⑤ ^{**} Figure of merit = 100 PJ ✓ ^{**}

⑥ ^{**} $N.M = \underline{0.4V}$ ✓

Logic 1 { $V_{OH} = 2.4V$
 $V_{IH} = 2V$ } $N.M = 0.4V$

Logic 0 { $V_{IL} = 0.8V$
 $V_{OL} = 0.4V$ } $N.M = 0.4V$

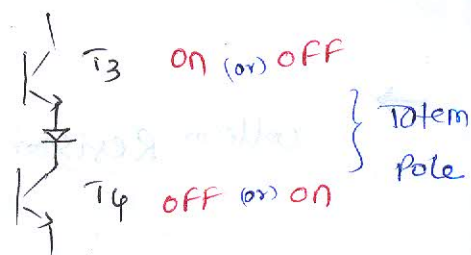
⇒ advantage of Totem Pole :-

1) Propagation delay is less

2) higher speed of operation

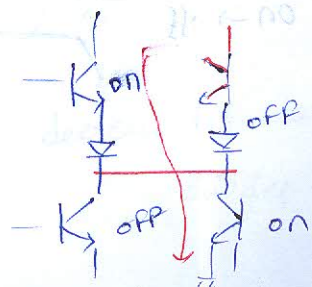
3) Low power dissipation

^{*} 4) Higher Fan out



⇒ disadvantage :-

→ It is not used for wired logic



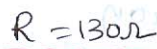
used.



Cut off Transistor T_4 when T_3 is on



Collector Resistor



So at one time
both will melt then
Tr will damage

✖✖

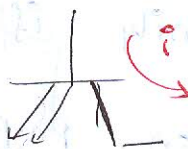
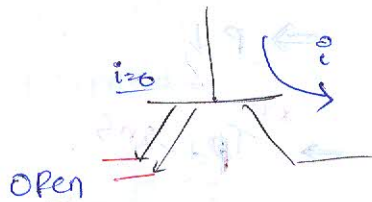
→ DTL

HTL

TTL

→ if any i/p is opened

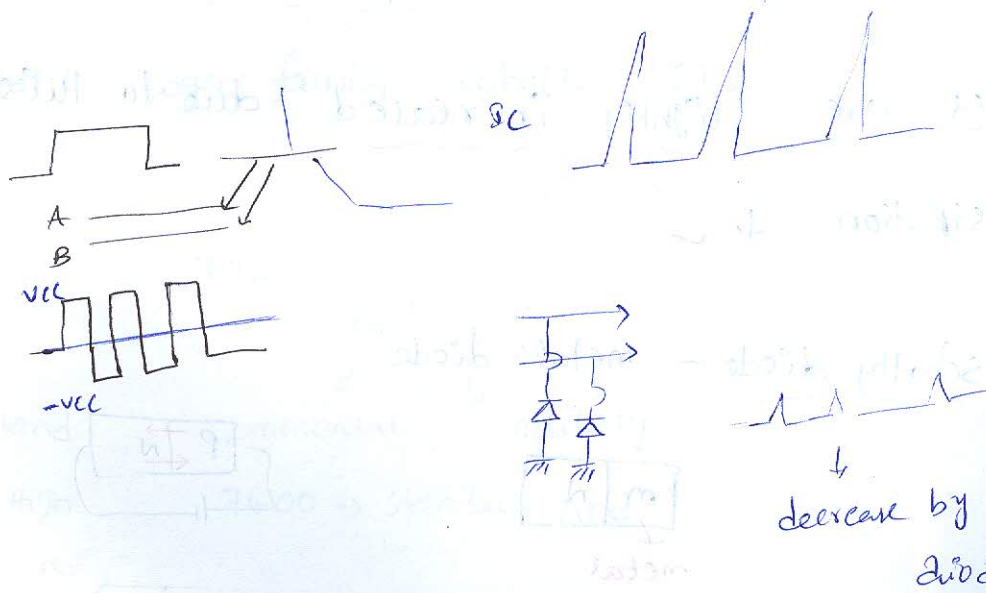
then it is logic 1



So operation
is same

→ clamping diodes are used at i/p stage in order to
protect Transistor T1 during high frequency Transitions

(or) ringing



TTL

- 1) standard TTL — $t_{pd} = 10\text{ns}$
- 2) High Speed TTL — 6ns
- 3) Low Power TTL $\Rightarrow P \downarrow$
- 4) Schottky TTL $\Rightarrow$ ^{**} $t_{pd} = 2\text{ns}$

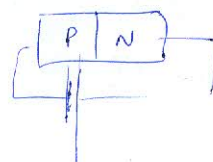
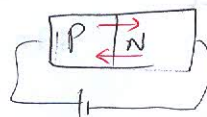
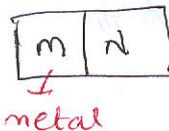
→ In TTL logic family if resistor values are slightly reduced then propagation delay will reduce and RC Time constant decreases and Speed of operation increases resultant logic family is known as high speed TTL

↓

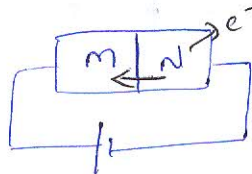
$P_{diss} \uparrow$

→ In low power TTL logic family resistor values are slightly increased due to this power dissipation ↓ ✓

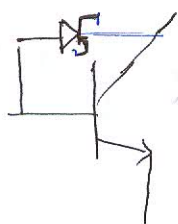
→ ^{**} Schottky diode — metal diode



→



→ metal-semiconductor diode
 → majority
 → ↑ Speed ✓



**

$$t_{pd} = 2ns$$

→ In TTL logic family when Schottky diode is placed b/w Base and collector region then it will remove storage time (or) saturation delay due to this Speed of operation will increase and resultant logic family Schottky TTL

TTL

74 | 54

↓

↓

commercial

military

74 → stand

74 H → High

74 L → low

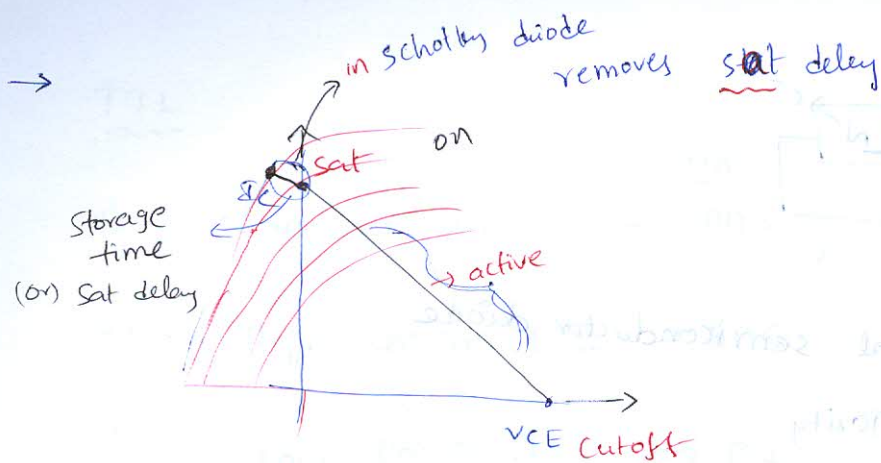
74 S → Schottky

7400 → standard And

74 LS → Low Power Schottky

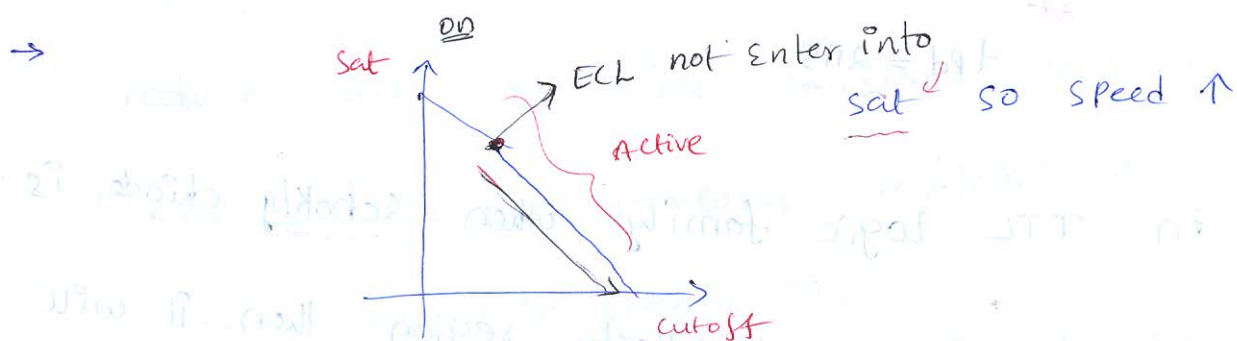
74ALS → Advanced Low Power Sch

**



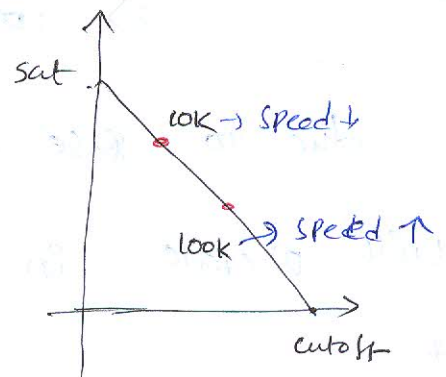
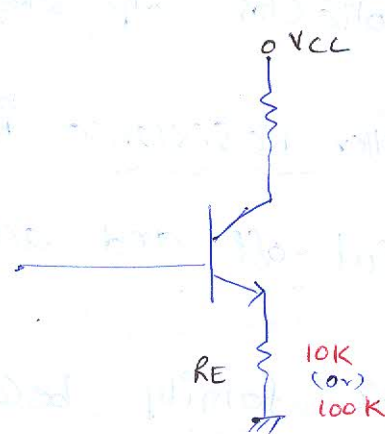
off ← on

on ← off ↑

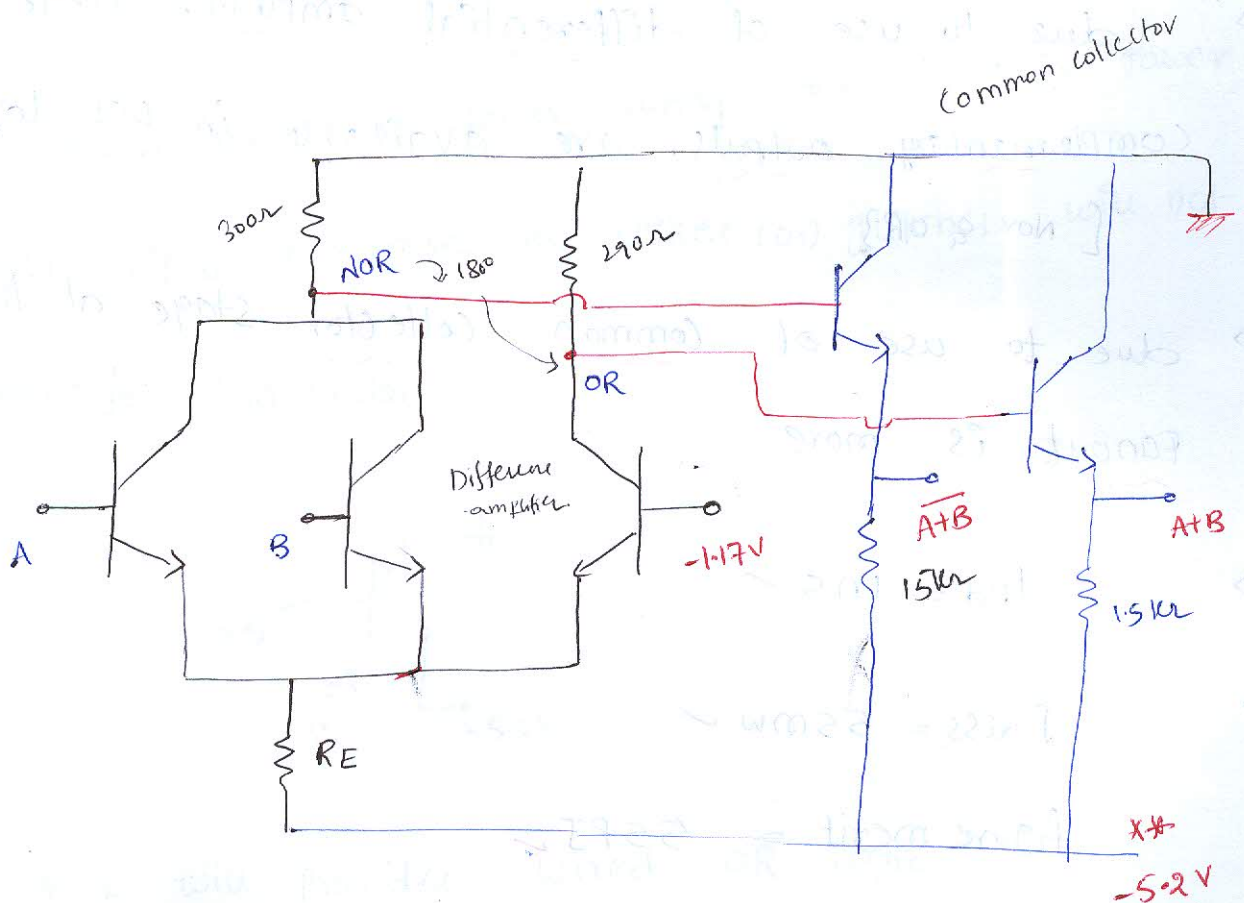


→ ~~***~~ ECL will not go to Saturation and it will go to only active region.

⇒ ECL logic family :-



→ due to ~~RE~~ RE transistor will not goto sat



ECL family cat

→ ECL Basically Contains two stages

1) differential amplifier ip stage

2) common collector op stage

→ due to use of Emitter Resistance R_E transistors will operate in only cut-off and active mode

→ ECL is the fastest logic family because it operates in non-saturated region.

→ due to use of differential amplifier stage

complementary outputs are available in ECL logic family
[NOR & OR]

→ due to use of common collector stage at the op
Fanout is more

→ $t_{pd} = 1 \text{ ns}$ ✓

→ $P_{diss} = 55 \text{ mW}$ ✓

→ figure merit = 55 PJ ✓

→ noise margin = 0.3 V ✓

→ fan out = 25 ✓

✖✖

logic 0 → -1.7V

logic 1 → -0.85V

✖✖✖

$$V_{OL} = -1.7V$$

$$V_{IL} = -1.4V$$

0.3V

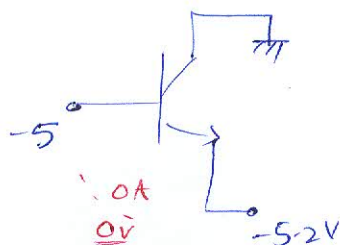
$$V_{IH} = -1.1V$$

$$V_{OH} = -0.8V$$

0.3V

→ ECL uses -ve Power Supply due to this Power Supply ripple (or) Noise (or) spikes (or) glitches will not damage Transistor

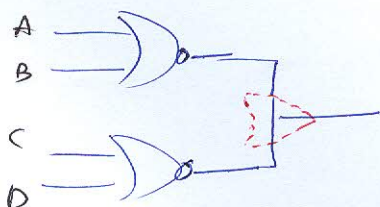
→



✖✖

→ ECL will provide wired OR logic

→



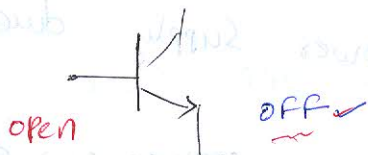
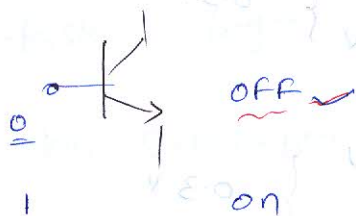
$$\overline{A+B} + \overline{C+D}$$

→ * Current mode logic family [ECL]

→

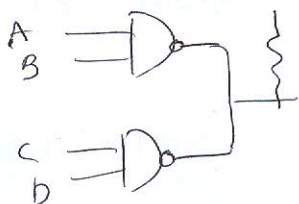
RTL
DCTL
 I^2L
ECL

if any ilp is opened it
acts as logic 0



→

3)



$$\overline{AB} \cdot \overline{CD}$$

→

S_2 S_1 S_0

	S_2	S_1	S_0	
1		B	A	
1	0	0	0	$\xrightarrow{x4} 0$
1	0	0	1	$\xrightarrow{x5} 1$
1	1	0	0	$\xrightarrow{x6} 1$
1	1	1	1	$\xrightarrow{x2} 0$