MOSFET

MOSFET :-

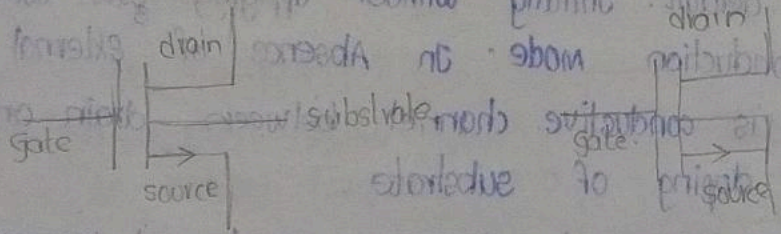
⇒ MOSFET is "metallic oxide semiconducter Field effect transistor" in whic metallic oxide semiconducter is its structure and field effect transistor describes its function.

⇒ MOSFET is a Four terminal device. they are

1. Drain
2. Source
3. Gate
4. Substrate

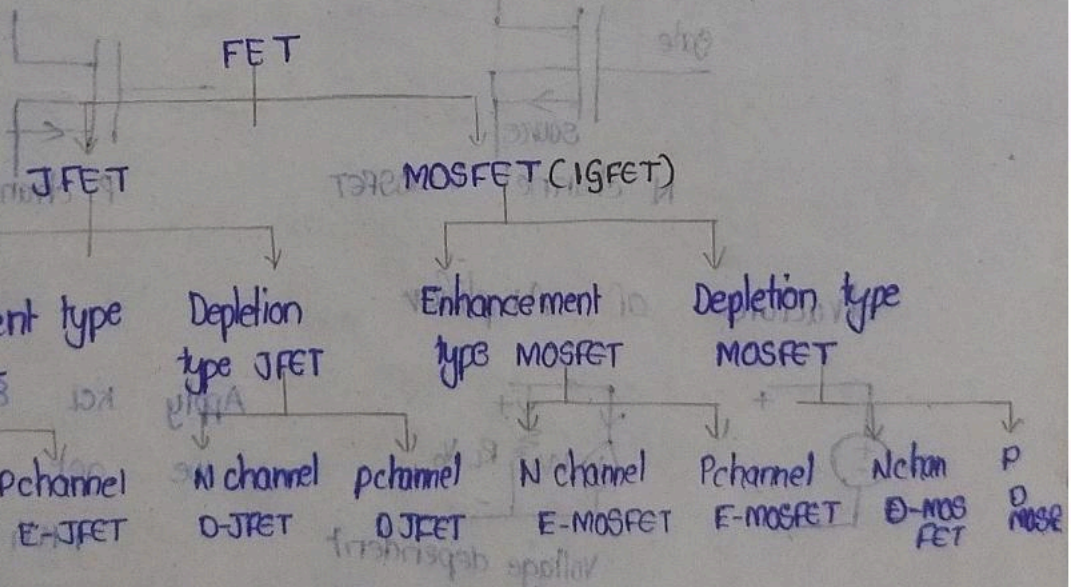
⇒ MOSFET is a symmetrical device [i.e drain & source can be changed]

⇒ The source and substrate are internally connected. Thus MOSFET is a three terminal device.



CLASIFICATION

FET :



⇒ MOSFET is of two types. they are

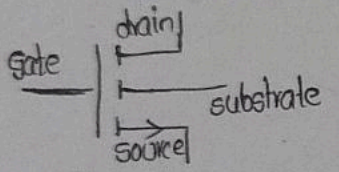
1. Enchancement type MOSFET
2. Depletion type MOSFET

Enchancement type MOSFET :

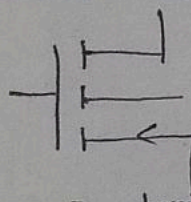
* E MOSFET is a MOSFET in which there is no channel between drain and source initially. As we increase gate terminal voltage, the current will from drain to source, thus creating a channel between drain and source.

* E-MOSFET are of two types:

1. N channel EMOSFET
2. P channel EMOSFET



N channel EMOSFET

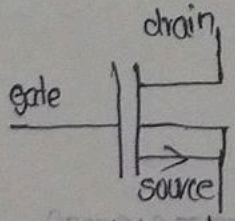


P channel EMOSFET

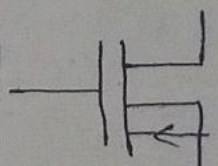
Depletion type MOSFET :

* D MOSFET is a MOSFET which operates with conductive channel by default. Intially without applying gate voltage, DMOSFET is under conduction mode. In Absence of external voltage, intially there is conductive channel between drain and source due to inherent doping of substrate.

* D MOSFET is of two types : 1) N channel D MOSFET
2) P channel D MOSFET

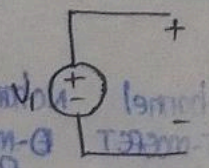


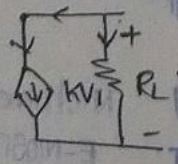
N channel D MOSFET



P channel D MOSFET

Structure of Amplifier





Voltage dependent current source

Apply KCL Equation :-

we get

$$+KV_i + \frac{V_o}{R_L} = 0$$

$$\frac{V_o}{R_L} = -KV_i$$

$$V_o = -KV_i R_L$$

$$V_o = -KR_L V_i$$

$$V_o \propto V_i$$

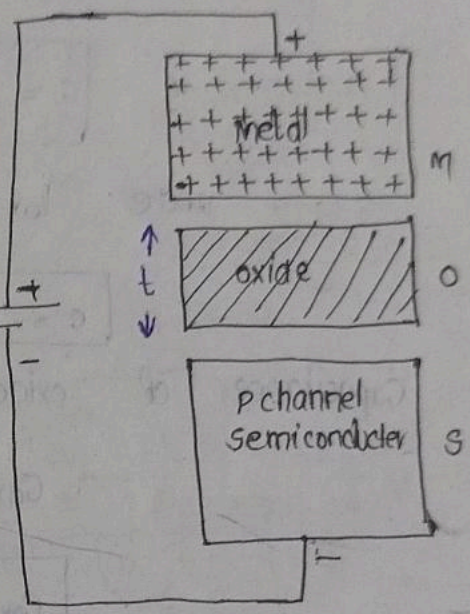
∴ output voltage depends on input voltage.

* MOSFET is a voltage controlled device.

MOSFET capacitor:-

case(i): what happens if V_i increases

As we increase V_i, the metal layer will become more positive thus increases charge density, As a result electrons density increase Thus there will be flow of current



$V_i \uparrow$ $Q \uparrow$ $\bar{e}$ density $\uparrow$ $I \uparrow$

* flow of electrons - channel.

case(ii): If t decreases

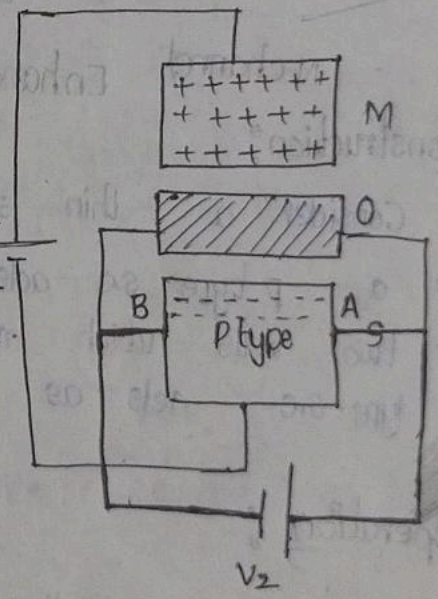
As $t \downarrow$ $Q \uparrow$ $\bar{e}$ density $\uparrow$ $I \uparrow$

case(iii): when External voltage is applied

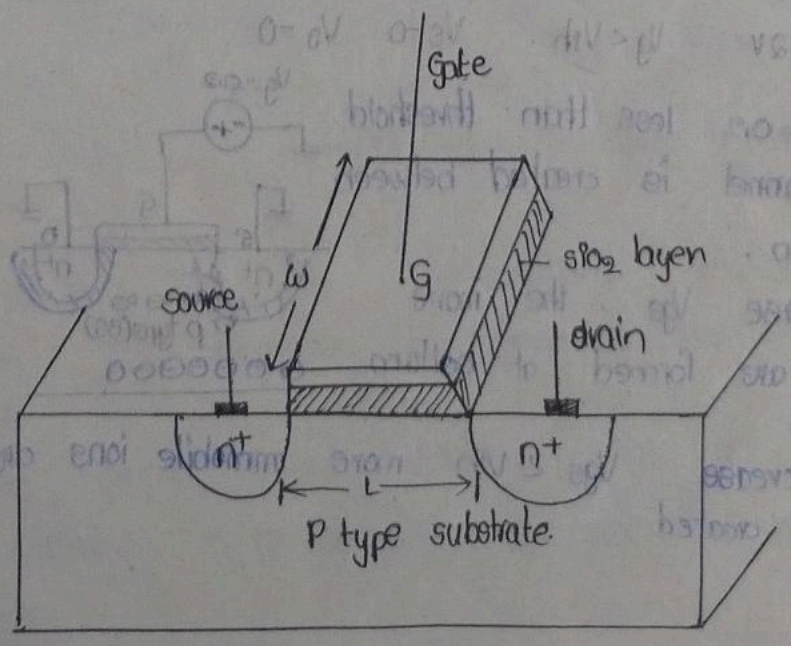
As $V_i \uparrow$ $Q \uparrow$ $\bar{e}$ density $\uparrow$

* electrons will from B to A Thus there will be current flow from A to B.

*As whe increase voltage, the current flow from A to B thus resistance between A and B decreases



Development of MOS structure:



Gate area = L x W = LW

* electrons will from source to drain. Thus current flows from drain to source

* Capacitance of MOSFET ($\dot{C}$) = $\frac{A\varepsilon_0}{t_{ox}}$

$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} A$$

where t_{ox} = thickness of oxide layer

$$C = C_{ox} A \Rightarrow C_{ox} = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}}$$

* Capacitance of oxide layer is given by

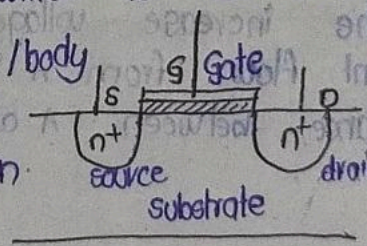
$$C_{ox} = \frac{C}{A} = \frac{\text{Capacitance of device}}{\text{gate area}}$$

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} = \frac{C}{A}$$

N channel Enhance type MOSFET OPERATION

Construction:

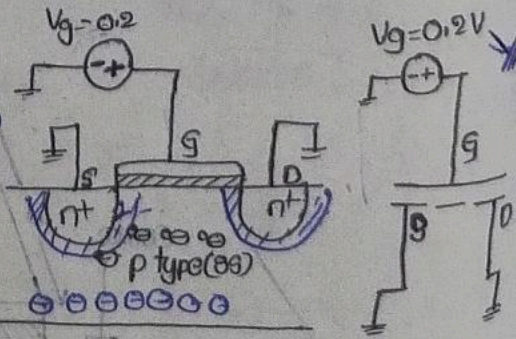
* Consider a thin silicon layer which is act as gate terminal
* a p type s.c acts as substrate / body
* two wells which are highly doped n type s.c. acts as source and drain



Operation:

case (i): $V_g = 0.2V$ $V_g < V_{th}$ $V_S = 0$ $V_D = 0$

* when $V_{gs} = 0.2$ less than threshold voltage no channel is created between source and drain.
* As we increase V_{gs}, the more immobile ions are formed at bottom of substrate
* As we increase $V_{gs} < V_{th}$ more immobile ions are formed no channel is created

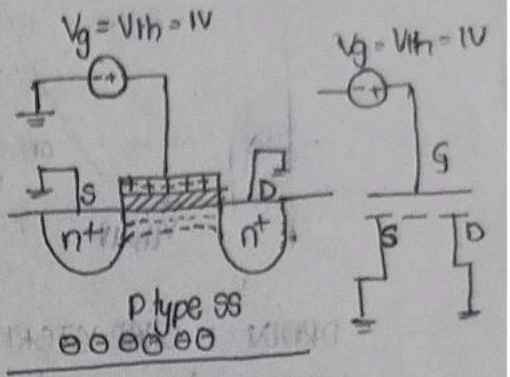


case 2: $V_{gs} = V_{th} = 1V$ $V_D = 0$ $V_S = 0$

* the voltage required for MOSFET to come under conduction mode is called "threshold voltage".

* when $V_{gs} = V_{th}$, a channel is developed between drain and source, but there is no current flow since $V_D = 0$.

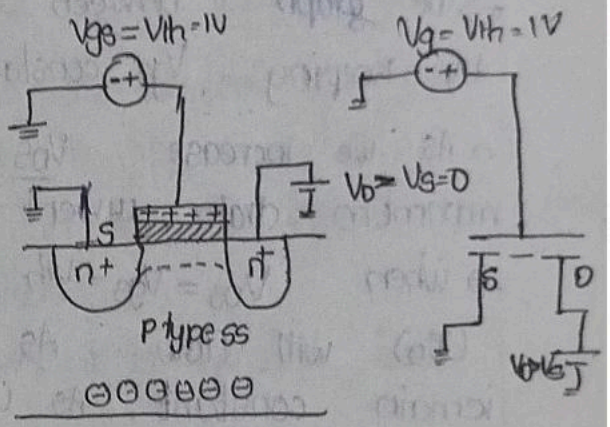
$I_D = 0$.



case 3:- $V_{gs} \geq V_{th}$ $V_D > V_S = 0$ $V_S = 0$

* As we applied drain voltage, there will be current flow across channel.

* Thus I_D (drain current) flows from drain to source when V_D is applied

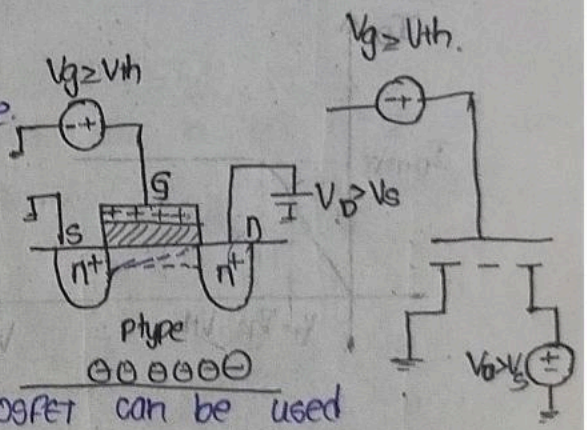


case 4: $V_{gs} \geq V_{th}$ $V_D > V_S$ $V_S = 0$

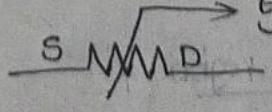
* when we increase drain voltage more current will from drain to source.

* $V_g > V_{th}$, Q ↑ e^- density ↑ I_D ↑

* Thus I_D increases, the resistance between drain and source decreases



* when V_D is increased, the MOSFET can be used as voltage controlled resistor.



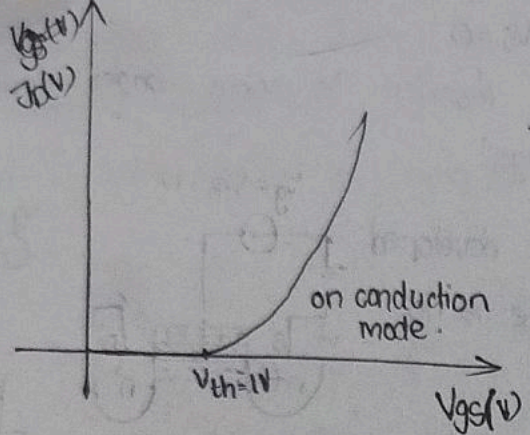
voltage variable resistor.

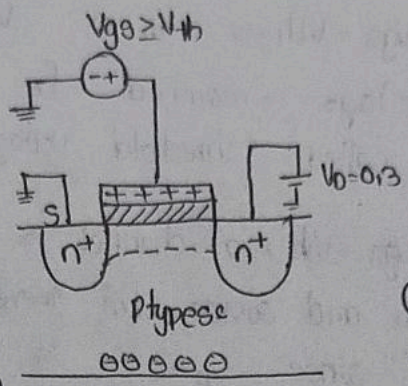
case (5) :-

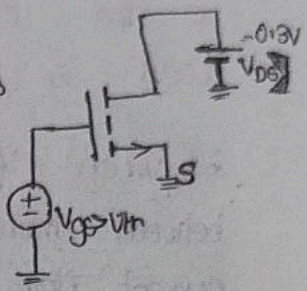
case (a) : $V_{gs} \geq V_{th}$ V_{DS} constant $V_S = 0$

when V_{gs} increases by keeping V_{DS} constant, the I_D current varies

* The graph drawn between V_{gs} and I_D with V_{DS} constant is called "TRANSFER CHARACTERISTICS OF MOSFET".





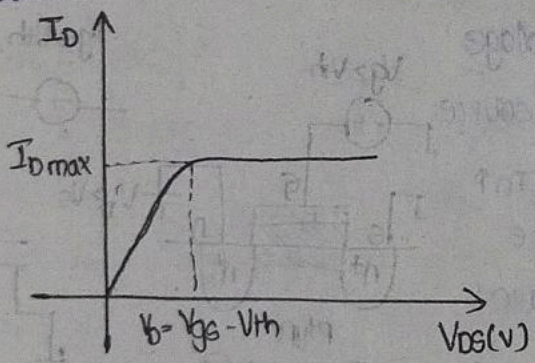


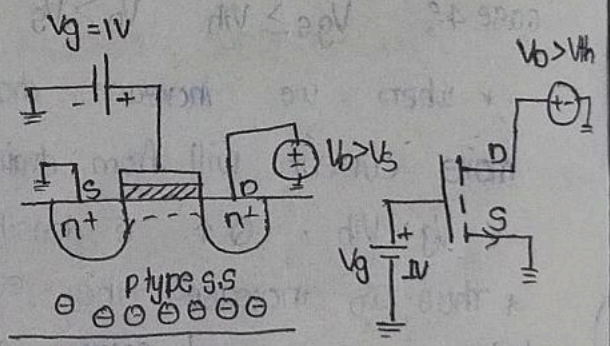
DRAIN CHARACTERISTICS:-

⇒ the graph between drain to source voltage (V_{DS}) & I_D by keeping V_{GS} constant is called drain characteristics.

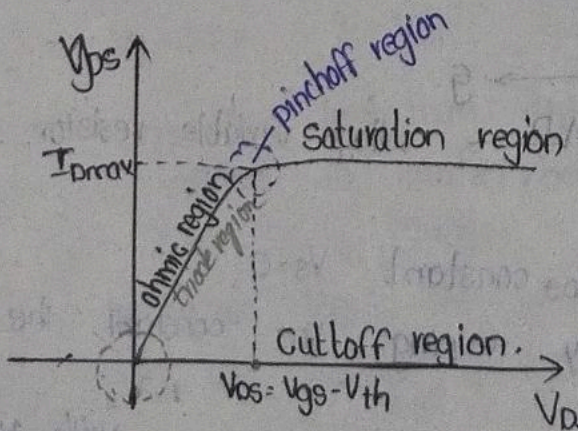
⇒ As we increase V_{DS}, I_D increases exponentially upto it reaches maximum drain current.

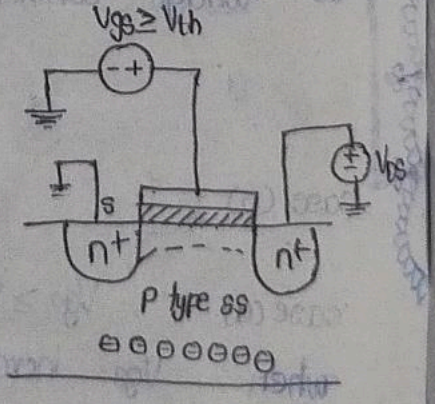
⇒ when $V_{DS} = V_{GS} - V_{th}$ (overdrive voltage) maximum drain current (I_D) will flow. As we $V_{DS} \geq V_{GS} - V_{th}$ the drain current remain constant. As under this region device can be used as current controlled device.





Regions of Operations of MOSFET





* when V_{DS} is less than overdrive voltage the mos. is operated under ohmic region in which I_D (drain current) increases when V_{DS} increase. Under this region, MOSFET is used as voltage controlled or variable resistor.

* when $V_{DS} = V_{GS} - V_{th}$, is maximum drain current (I_{Dmax}) will flow through device - This condition is called as "Pinchoff condition"

* when $V_{DS} \geq V_{GS} - V_{th}$ the MOSFET is operated under saturation region in which I_D remains constant since we increase V_{GS}. Under this region MOSFET is used as constant current source and ON switch.

* when $V_{GS} < V_{th}$ the MOSFET is in cutoff region. Under this condition it is used as OFF switch.

* MOSFET is used as switch when it is operated under saturation and cutoff region.

N channel Depletion type MOSFET

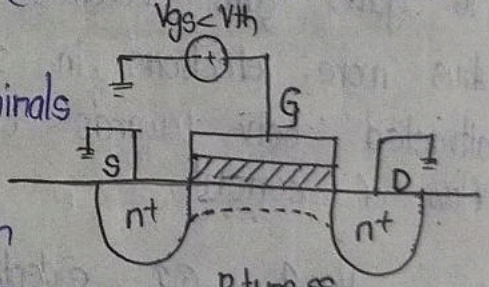
$V_{GS} = 0$

* D-MOSFET is a MOSFET which operates also in off condition due to inherent doping of p type substrate (a conductive channel formed).

* Construction

* N channel D-MOSFET has three terminals source, drain, substrate, gate.

* there is a conductive channel between soure and drain due to inherent doping of p type substrate.



* this substrate is made up of p type S.S.

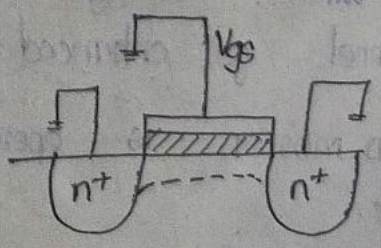
* the channel is made of n type semiconducter.

* this channel is sandwiched between gate oxide and gate electrode

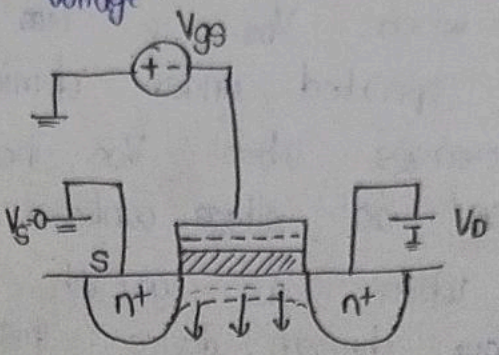
working

case (i) : $V_{GS} < V_{th}$ $V_{GS} = 0V$

when no voltage is applied to gate terminal, there will be a conductive channel between source and drain due to inherent doping of p type ss. due to which there will be current flow from d to s due to conductive channel. thus D MOSFET is usually in

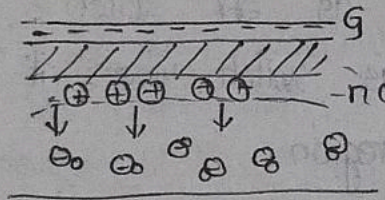


ON condition without any external voltage.



case(ii) : $V_{gs} < 0V$

when negative voltage is applied to gate terminal, gate becomes more negative. thus the ēs in channel gets repelled due to -ve gate voltage, moving away from channel. thus the channel gets depleted. the moved ēs got recombined with holes in p type ss thus flow of current in channel gets depleted. thus the conductivity gets depleted when -Ve gate aplied

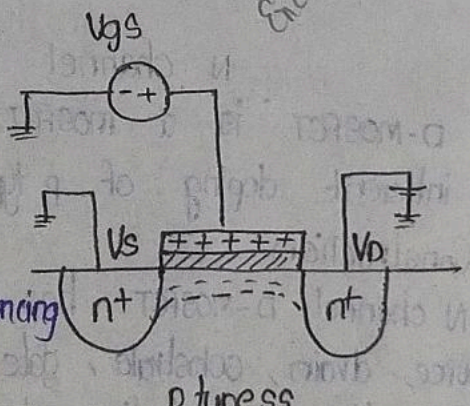


$V_g > V_{th}$ +Ve

Enhancement

case (iii) : $V_{gs} > 0V$

When positive voltage is applied to gate, gate becomes more +Ve thus more electrons in substrate attracted ~~belv~~ towards channel, enhancing flow of current

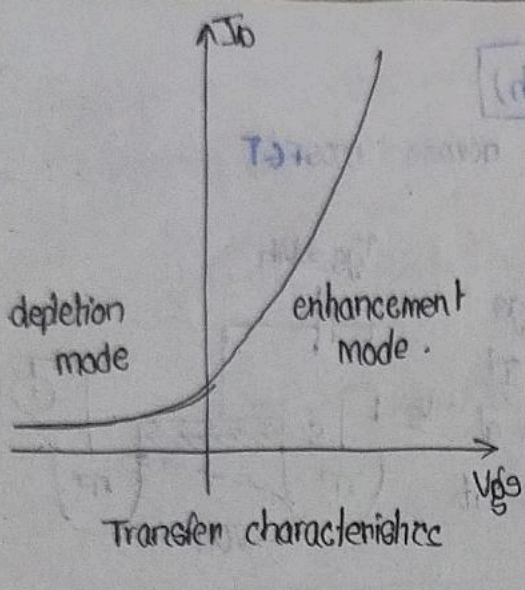


$V_{gs}\uparrow$ @↑ ē density↑ $I_D\uparrow$

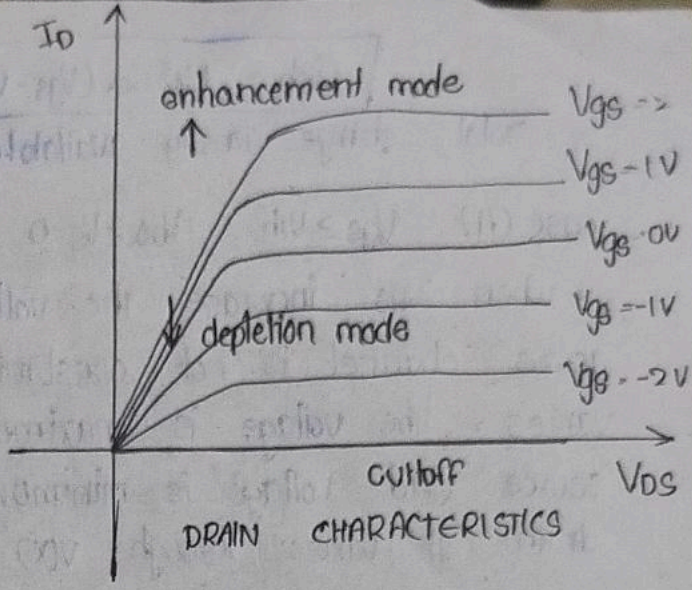
* thus more electrons will flow across channel thus increasing flow of electrons current through channel
* when +Ve gate voltage applied, the conductivity of the channel get enhanced.

⇒ D MOSFET is operated in both enhancement and depletion mode.

⇒ D MOSFET is used as off swith in depletion mode while ON switch in enhancement mode.



Transfer characteristics



DRAIN CHARACTERISTICS

Behaviour of THE CHANNEL :-

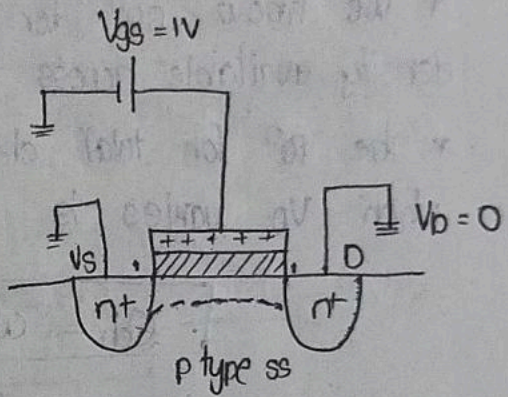
1) case(1): $V_{GS} = V_{th}$ $V_D = 0$ $V_S = 0$

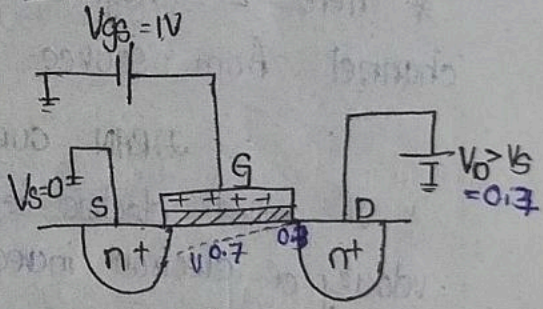
when $V_{GS} = V_{th}$, $V_{DS} = 0$, there will be uniform voltage across the channel thus there will be uniform current flow MOSFET is under conduction mode.

Case (ii): $V_{GS} \geq V_{th}$, $V_D > V_S = 0$ $V_S = 0$

As we increase V_{DS}, the channel voltage is not same. Voltage gets decreased.

1 - 0	1 - 0.3	1 - 0.6
1	0.7	0.4

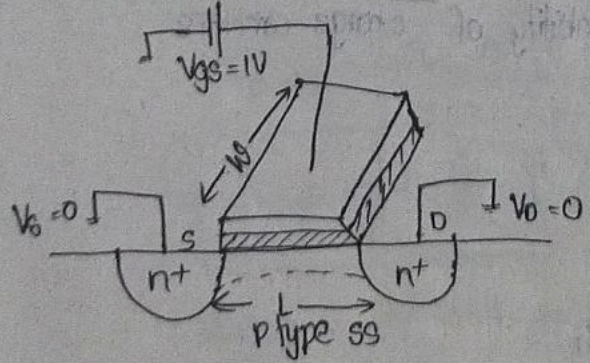


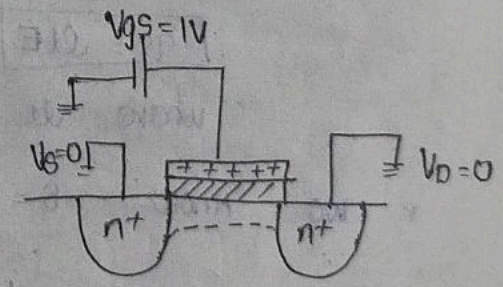


* here Q (charge density) is maximum at source and minimum at drain.

DERIVATION OF DRAIN CURRENT EQUATION

Case (i) : $V_{GS} \geq V_{th}$ $V_D = 0$





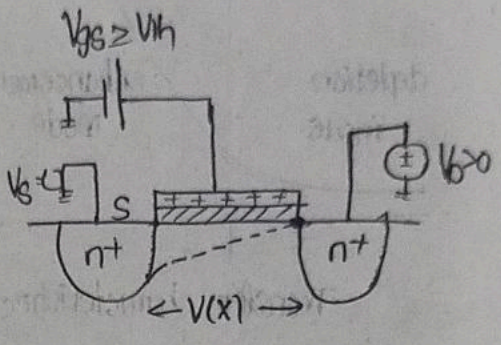
* The total charge density available across channel is given by

$$Q_{ch} = \text{Gate area} \times C_{ox} \times V_{GS} - V_{th}$$

$$Q_{ch} = LW C_{ox} (V_{gs} - V_{th})$$

* Total charge density available across MOSFET

case (ii) $V_{gs} \geq V_{th}$ $V_{DS} \geq V_{GS} = 0$

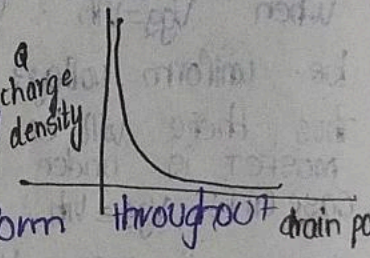


* when V_{DS} increase the voltage across channel is not constant. It varies. The voltage is maximum at source and voltage is minimum at drain. It varies through V(x)

* we know eqn for total charge density available across channel when $V_{gs} = 1V$ & $V_b = 0$

* the eqn for total charge density available across channel when V_D varies is

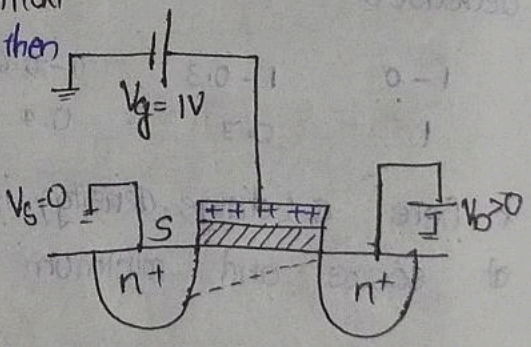
$$Q_{ch} = W C_{ox} [V_{gs} - V_{th} - V(x)]$$



* Here L neglected since it is uniform channel from source to drain.

DRAIN CURRENT DERIVATION

* If applied electric field increases then velocity of electron increases.



$E \propto v$

$E = \mu$

$v \propto E$

$$v = \mu E$$

where μ is mobility of charge carriers.

* we know $E = -\frac{dv}{dx}$

$$v = -\mu \frac{dv}{dx}$$

* $I_D = -v \times Q_{ch}$

$$I_D = \mu \frac{dv}{dx} W C_{ox} [V_{gs} - V_{th} - V(x)]$$

$I_D\,dx = \mu n\, W\, C_{ox}\,[V_{gs} - V_{th} - V(x)]\,dv$

* Integrating on both sides,

$$\int_0^L I_D\,dx = \int_0^{V_{DS}} \mu n\, W\, C_{ox}\,[V_{gs} - V_{th} - V(x)]\,dv$$

$$I_D x\Big]_0^L = \mu n\, W\, C_{ox}\left[(V_{gs} - V_{th})V - \frac{V^2}{2}\right]_0^{V_{DS}}$$

$$I_D L = \mu n\, W\, C_{ox}\left[(V_{gs} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$\boxed{I_D = \mu n C_{ox} \frac{W}{L}\left[(V_{gs} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]}$$

* this is equation for drain current of MOSFET
* For N channel E-MOSFET,

$$\boxed{I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{gs} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]} \quad \text{——— (1)}$$

Maximum drain current derivation

$$\Rightarrow \frac{\partial I_D}{\partial V_{DS}} = 0$$

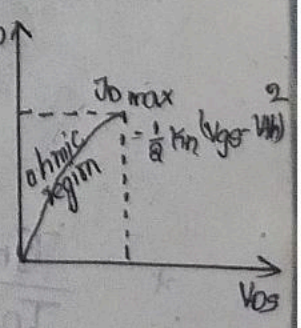
$$0 = I_{Dmax} = \mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{th}) - V_{DS}$$

$$\boxed{V_{DS} = V_{gs} - V_{th}}$$

* when $V_{DS} = V_{gs} - V_{th}$, then maximum current will from drain to source.
* Substituting V_{DS} in Eqn (1)

$$I_{Dmax} = \mu_n C_{ox} \frac{W}{L}\left[(V_{gs} - V_{th})(V_{gs} - V_{th}) - \frac{(V_{gs} - V_{th})^2}{2}\right]$$

$$\boxed{I_{Dmax} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{th})^2}$$



where $\frac{W}{L}$ is called Ascept Ration

here $K_n = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}$

where C_{ox} capatiance oxide

$$\boxed{I_{D\,max} = \frac{1}{2} K_n (V_{gs} - V_{th})^2}$$

DRAIN Resistance :

$$R_D = \frac{V_{DS}}{I_{DS}}$$

$$R_D = \frac{V_{DS}}{\mu_n C_{ox} \frac{W}{L} (V_{gs}-V_{th}) V_{DS}} \quad \left[\text{since } (V_{gs}-V_{th}) V_{ds} \gg \frac{V_{DS}^2}{2}\right]$$

$$\boxed{R_D = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{gs}-V_{th})}}$$

* when $V_{gs} = V_{th}$, $R_D = \frac{1}{0} = \infty \rightarrow I_D = 0$.

Trans Conductance :

* the reciprocal of resistance is called Trans Conductance.

$$G_m = \frac{\partial I_{Dmax}}{\partial V_{gs}}$$

$$G_m = \frac{\partial}{\partial V_{gs}} \left[\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs}-V_{th})^2 \right]$$

$$G_m = \frac{1}{2} \times 2 \times \mu_n C_{ox} \frac{W}{L} (V_{gs}-V_{th})$$

$$\boxed{G_m = \mu_n C_{ox} \frac{W}{L} (V_{gs}-V_{th})} \quad \text{---} (1)$$

* we know $I_{Dmax} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs}-V_{th})^2$

$$V_{gs}-V_{th} = \sqrt{\frac{2 I_{Dmax}}{\mu_n C_{ox} W/L}} \quad \text{---} (2)$$

* Substitute Eq 2 in Eq 1

$$G_m = \mu_n C_{ox} \frac{W}{L} \sqrt{\frac{2 I_{Dmax}}{\mu_n C_{ox} W/L}}$$

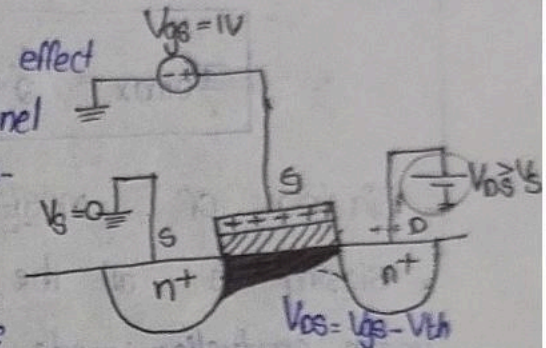
$$\boxed{G_m = \sqrt{2 I_{Dmax} \mu_n C_{ox} \frac{W}{L}}} \quad \text{---} (3)$$

* $\frac{I_m}{I_{Dmax}} = \frac{\mu_n C_{ox} \frac{W}{L} (V_{gs}-V_{th})}{\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs}-V_{th})^2}$

$$G_m = \frac{2 I_{Dmax}}{V_{gs} - V_{th}}$$

CHANNEL LENGTH MODULATION

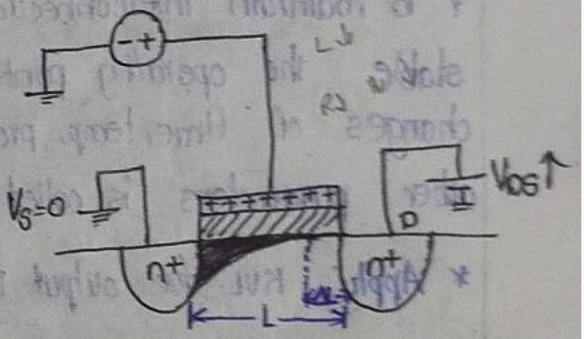
* The channel length modulation is an effect in FETS, the length of inversion channel gets decreased as we increase drain-to-source voltage (V_{DS}).



* As we increase V_{DS}, the pinch off point will move towards source.

* As we increase V_{DS}, the output drain resistance decreases

$$R_D \propto \frac{1}{W/L}$$



* As we decrease length of channel the drain resistance also decreases, thus more drain current will flow

* The channel length modulation decreases drain resistance and saturation region drain current increases since we increasing V_{DS}.

* we know equation for I_{Dmax}

$$I_{Dmax} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2$$

channel

$$I_{Dmax} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L - \Delta L} (V_{gs} - V_{th})^2$$

$$= \frac{1}{2} \mu_n C_{ox} \frac{W}{L\left(1 - \frac{\Delta L}{L}\right)} (V_{gs} - V_{th})^2$$

$$= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 \left(1 - \frac{\Delta L}{L}\right)^{-1}$$

$$\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 \left(1 + \frac{\Delta L}{L}\right)$$

we know $\Delta L \propto V_{DS}$

$$\Delta L = \lambda' V_{DS}$$

$$\frac{\Delta L}{L} = \frac{\lambda'}{L} V_{DS}$$

$\frac{\Delta L}{L} = \lambda V_{DS}$

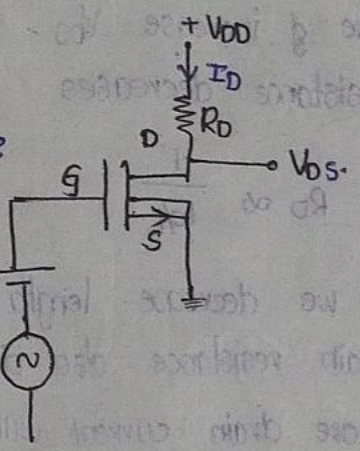
where λ is channel length modulation coefficient.

$\lambda = \text{volt}^{-1}$

$$\therefore \boxed{I_{Dmax} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 (1 + \lambda V_{DS})}$$

Biasing of MOSFET :-

* Biasing is all the arrangements needs for MOSFET to come under conduction mode.
* Basing is needing to operate stable the operating point, irrespective of changes in any parameters
* To maintain interconnection and to stable the operating point irrespective changes of time, temp, press or any other parameters is called Biasing

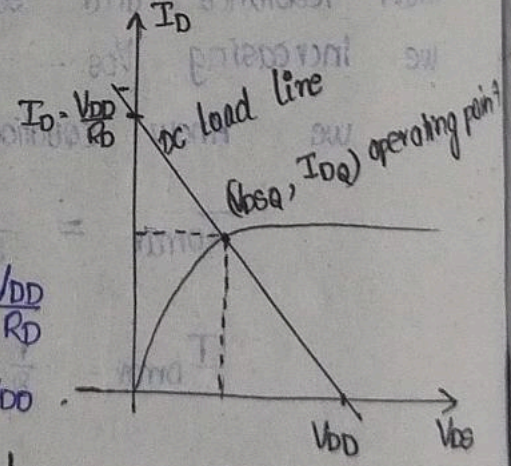


* Apply KVL for output loop

$$-V_{DD} + R_D I_D + V_{DS} = 0$$

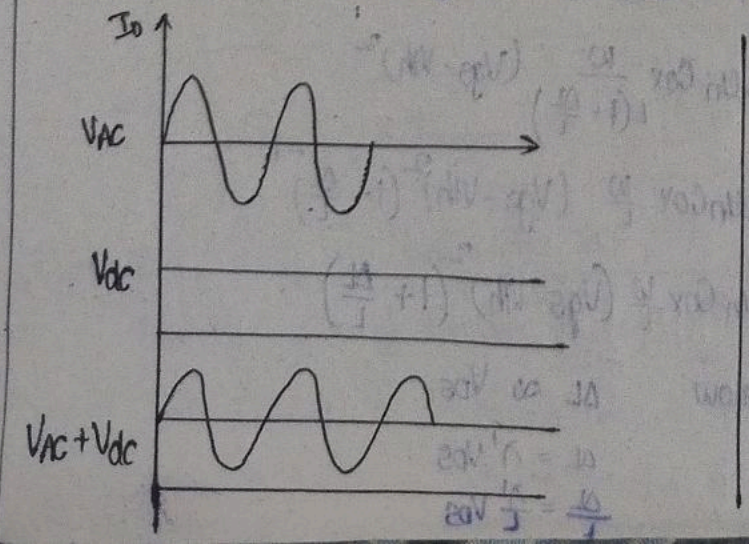
$$V_{DS} = V_{DD} - I_D R_D$$

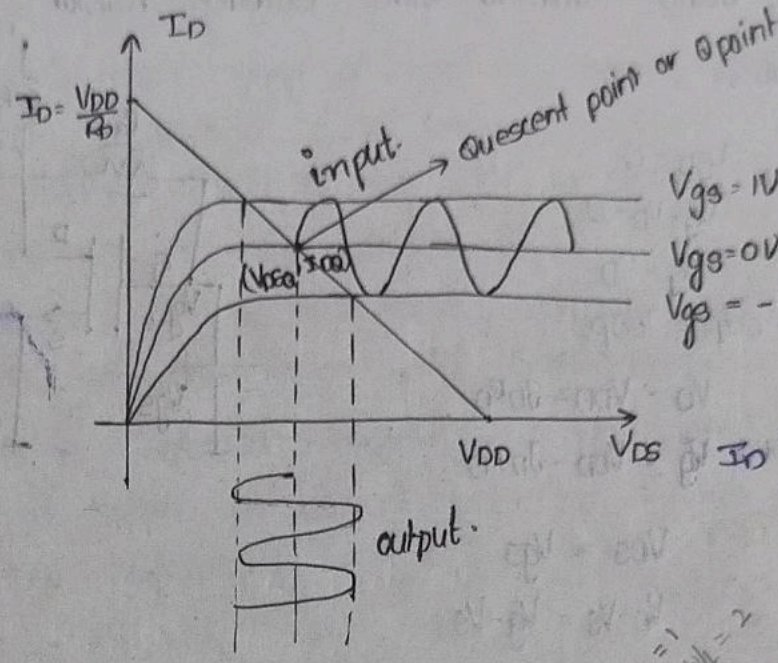
$$\boxed{I_D = \frac{V_{DD} - V_{DS}}{R_D}}$$



case (i): when $V_{DS} = 0$ $I_D = \frac{V_{DD}}{R_D}$

case (ii): when $I_D = 0$ $V_{DS} = V_{DD}$.





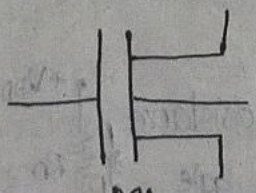
I_D V_{DS} Saturation mode.

Biasing Techniques :-

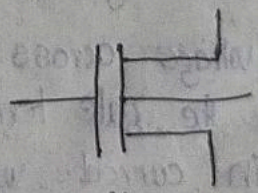
(1) Biasing using V_{gs} constant.
(2) Biasing using drain to source feedback resistor
(3) Biasing using constant current source.

(1) Biasing using V_{gs} constant

* Let us consider two identical mosfet namely M1 and M2,
* From same manufacturer, they have different threshold voltages so mismatching takes place even though they are identical
* If such mosfets are used for finding Q.P



$\mu_n C_{ox} = 1 mA/V^2$
$W/L = 2$
$V_{gs} = 2V$
$V_{th} = 1V$



$\mu_n C_{ox} = 1 mA/V^2$
$W/L = 2$
$V_{gs} = 2V$
$V_{th} = 0.775$

$I_{Dmax} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2$

$I_{Dmax_1} = \frac{1}{2} \times 1 \times 2 \times (1)^2$

$= 1 mA$

$V_{DS} = 1V$

$I_{Dmax} = \frac{1}{2} \times (1) \times 2 \times (2 - 0.775)^2$

$= (2 - 0.775)^2$

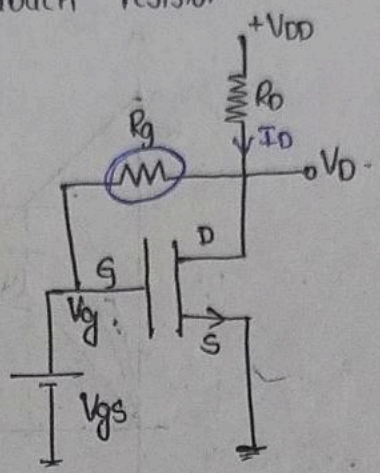
$= 1.5 mA$

$2.000 - 0.775 = 1.225$

$V_{DS} = 1.995$

* From above, even though two mosfets having same V_{gs}, due to change in V_{th}, the I_{Dmax} is different for two mosfets
* Thus the operating point is not stable even though V_{gs} constant
* This is not a best biasing technique.

Biasing using drain-to-source feedback resistor



from above,

$V_{GD} = 0$

$V_G - V_D = 0$

$V_G = V_D$

⇒ from output loop

$V_D = V_{DD} - I_D R_D$

thus $V_G = V_{DD} - I_D R_D$

$V_{DS} = V_{GS}$

$V_D - V_S = V_G - V_S$

$V_D = V_G = V_{DD} - I_D R_D$

$V_D = V_{DD} - I_D R_D$

$V_G = V_D = V_{DD} - I_D R_D$

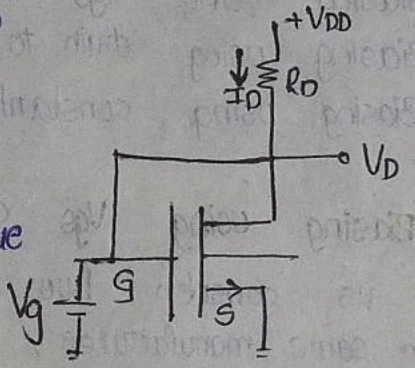
$V_{GS} = V_{DS}$

$V_G = V_D$

* It is -ve feedback between input and output

case(ii) : short circuiting the resistor

$V_G = V_D = V_{DD} - I_D R_D$.

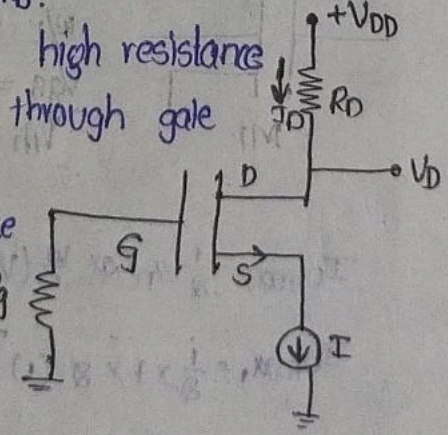


* It provides Negative feedback due to short circuit between gate & drain. It is a best technique to maintain O.P to be stable.

Biasing using constant Current Source

* the voltage across R_D is $I_D R_D$.
* Since the gate terminal offers high resistance the drain current will not flow through gate terminal.
* I_D current flows through source terminal.
* Drain current is in series with current source

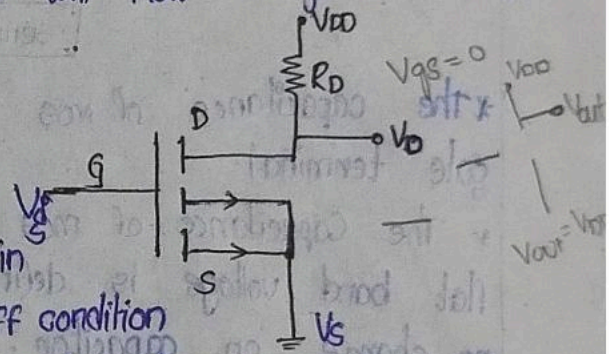
thus $I = I_D$.



* This is a best biasing technique.

MOSFET AS A SWITCH:

* MOSFET exhibit three regions of operations namely triode (or) ohmic region, saturation region and cutoff region.
* MOSFETS is used as Amplifiers when it is operated under triode region in which I_D increases as we increase V_{DS}.
* MOSFETS can be used as electronic switches when they are operated between saturation region and cutoff region.
* when MOSFET is in saturation region, constant current will flow through channel while in cutoff no current will flow through channel just as OFF AND ON switches.



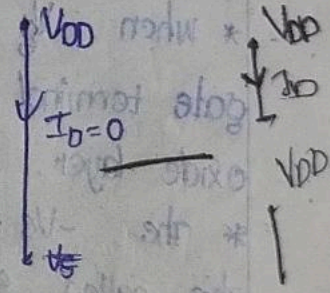
case(i): $V_g < V_T$ $V_g = 0$

when V_g is less than

when $V_g = 0$, the MOSFET is in cutoff region i.e MOSFET is under off condition thus it offers high impedence path thus the drain current flow is equivalent to zero.

the voltage drop across drain to source will be same

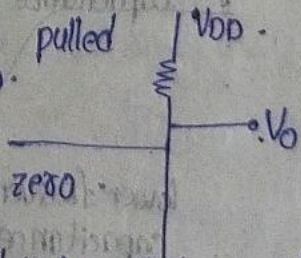
$$\therefore V_o = V_{DD} = V_S$$



case(ii): $V_g > V_T$

when $V_g > V_T$ MOSFET comes under conduction mode. when applied voltage V_{DD} is greather than overdrive voltage (or) pinchoff voltage (V_p) the MOSFET is under saturation condition.

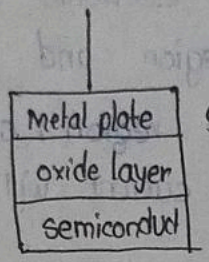
* Since it is in saturation condition, constant drain current will flow
* thus it offer low resistance path for flow of drain current
* As a result output voltage will be pulled towards low voltage which will be ideally zero.



* thus the voltage alters btw V_{DD} & zero.
* so MOSFET can be used as electrical switches when it is operated btw saturation & cutoff region.

MOSFET AS A CAPACITOR:

* MOS capacitor is made up of metal plate, oxide layer and semiconductor.
* Metal plate is gate acts as one of paralle plate and semiconducter will act as another plate



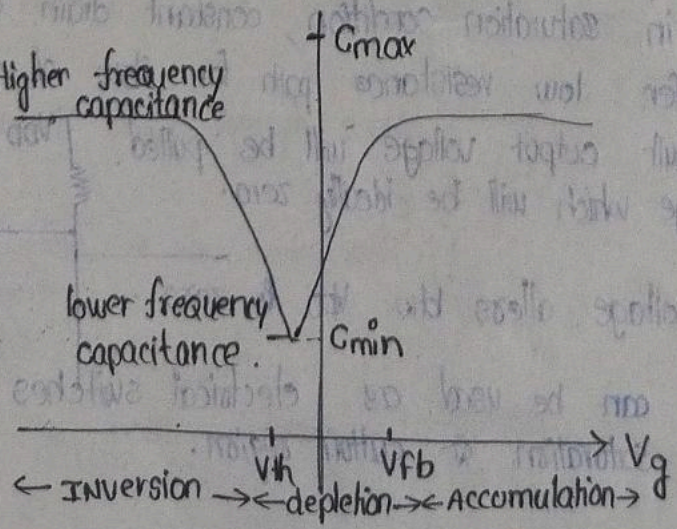
$$C = \frac{A\varepsilon}{tox}$$

$$C = \frac{\varepsilon_0 \varepsilon_r A}{tox}$$

$$C = C_{ox} A$$

$$C_{ox} = \frac{C}{LW} = \frac{\varepsilon_0 \varepsilon_r}{tox}$$

* The capacitance of MOS depends on the voltage applied at gate terminal
* The capacitance of mos capacitor depends on flat band Voltage. flat band voltage is defined as the voltage at which there is no charge on capacitor. Thus there will be no electric field.
* when $V_g > V_{fb}$ (flat band voltage) +Ve charge will accumulate on gate terminal. As result -Ve charge will accumulate below the oxide layer.
* the -Ve charged electrons only accumulate as -Ve charges this called surface Accumulation.
* when $V_g < V_{fb}$, -Ve charge will be on metal gate. so +ve charges will be in semiconducter.
* this is possible by pulling -Ve charges away from layer
* this is called surface depletion.



PROBLEMS

1) In N-E MOSFET is biased in saturation region it measures $I_D = 2mA$ when $V_{DS} = 4V$ while keeping V_{gs} constant & I_D increase to 2.05mA then $V_{DS} = 5V$ find channel length modulation coefficient.

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{gs}-V_{th})^2(1+\lambda V_{DS})$$

$$2 = \frac{1}{2}\mu_n C_{ox} W/L\,(V_{gs}-V_{th})^2(1+4\lambda) \quad -①$$

$$2.05 = \frac{1}{2}\mu_n C_{ox} W/L\,(V_{gs}-V_{th})^2(1+5\lambda) \quad -②$$

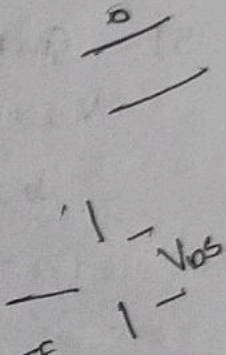
$$\frac{2}{2.05} = \frac{1+4\lambda}{1+5\lambda}$$

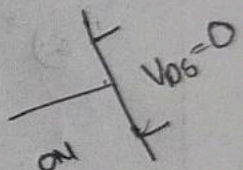
$$2+10\lambda = 2.05+8.2\lambda$$

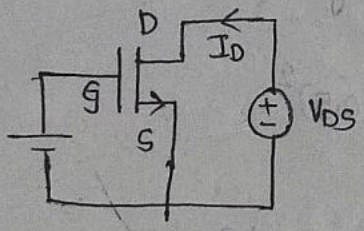
$$1.8\lambda = 0.05$$

$$\lambda = \frac{1.05}{1.8}$$

$$\boxed{\lambda = 0.0833\ V^{-1}}$$





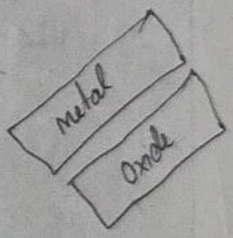
2) 

design 1mA Current Source

$\mu_n C_{ox} = 100\mu A/V^2$

$V_{th} = 0.5V$

$W/L = \frac{5\ um}{0.5\ um}$



$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{gs}-V_{th})^2$$

$$1mA = \frac{1}{2}\times 100\times 10^{-6}\times 10\,(V_{gs}-0.5)^2$$

$$10^{-3} = \frac{1}{2}\times 10^{-3}(V_{gs}-V_{th})^2$$

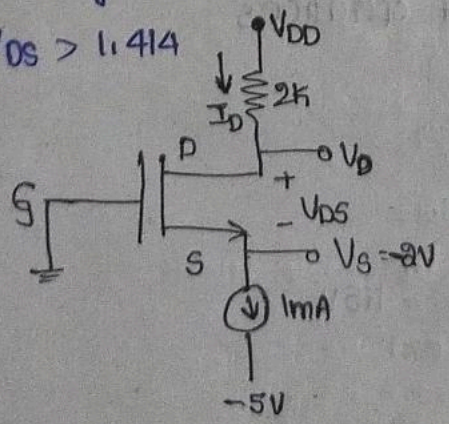
$$2 = (V_{gs}-0.5)^2$$

$$V_{gs} = \sqrt{2}+0.5$$

$$V_{gs} = 1.9V$$

$V_{DS} > V_{gs}-V_{th}$

$V_{DS} > 1.414$

3) 

given $V_{th} = 1V$ $V_{DD} = 5V$

$R_D = 2k$ find

V_{DS}

g_m

overdrive voltage.

$V_{gs} = V_G - V_S = 2$

$V_D = V_{DD} - R_D I_D$

$= 5 - 2k(1mA) = 3V$

$V_{DS} = V_D - V_S = 3+2 = 5V$

$V_{gs}-V_{th} = 2-1 = 1$

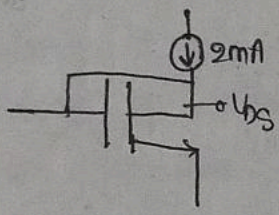
$$g_m = \frac{2I_{Dmax}}{V_{gs}-V_{th}} = \frac{2(1mA)}{1V} = 2 \text{ milli siemens}$$

4) $\mu_n C_{ox} = 1mA/V^2$ $V_{gs} = 2V$ $V_{th} = 1V$ $W/L = 10$ G_m

$$G_m = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})$$
$$= 10^{-3} \times 10 \, (2-1)$$
$$= 10^{-3} \times 10$$
$$= 10^{-2}$$

5) Given NMOS $\mu_n C_{ox} = 2mA/V^2$ $V_{gs} = 2$ $V_{th} = 1V$
$V_{DS} = 1V$ find I_D $W/L = 2$

$$I_D = \frac{1}{2} \mu_n C_{ox} W/L \, (V_{gs} - V_{th})^2$$
$$= \frac{1}{2} \times 2 \times 2 \, (2-1)^2$$
$$= 2mA$$

6) 

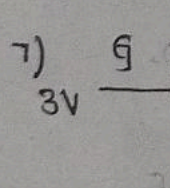
$\mu_n C_{ox} = 1mA/V^2$
$V_{th} = 0.5V$ $W/L = 2$
find V_{DS} & V_{gs}.

$I_D = 2mA$

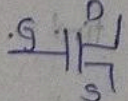
$$2 \times 10^{-3} = \frac{1}{2} \times 1 \times 10^{-3} \times 2 \times (V_{gs} - 0.5)^2$$

$$\sqrt{2} + 0.5 = V_{gs}$$

$V_{gs} = 1.9$ $V_{gs} = V_{DS} = 1.9V$

7) 

$V_{th} = 1V$ $\mu_n C_{ox} = 1mA/V^2$
$W/L = 2$
find which mosfet above ckt
1) mark channels
2) Region of operations

1) NMOS
2) 

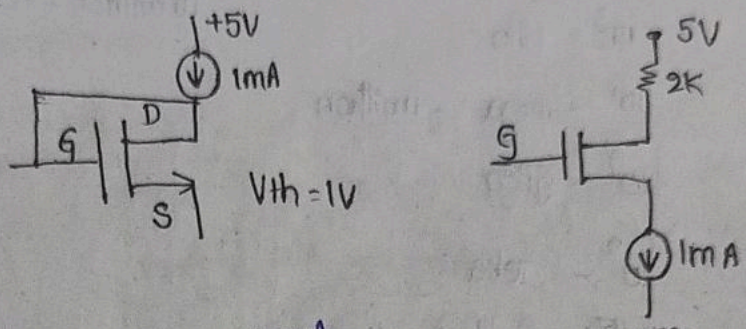
3) $V_{DS} = 2.5 - 1V = 1.5V$

$V_{gs} = 2V$

$V_{gs} - V_{th} = 2 - 1 = 1V$

$V_{DS} > V_{gs} - V_{th}$ saturation region.

find G_m for given MOSFET $\mu_n C_{ox} = 1mA/V^2$ $W/L = 8$



A) $I_{Dmax} = 1mA$

$$g_m = \sqrt{2 I_{Dmax} \mu_n C_{ox} W/L}$$

$$= \sqrt{2 \times 1mA/V^2 \times 1mA \times 8}$$

$$= \sqrt{16 \times 10^{-6}}$$

$= 4$ milli siemens

10^{-3} - milli

10^{-6} - micro

10^{-9} - nano

10^{-12} - pico

10^{-15} - femto

10^{3} - kilo

10^{6} - mega - 1 million

10^{9} - giga

10^{12} - Tera

10^{15} - ~~femto~~ peta

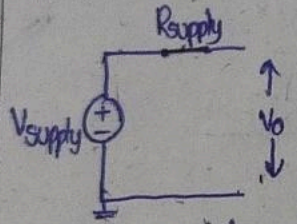
10^{18} - exa

10^{21} - zitla

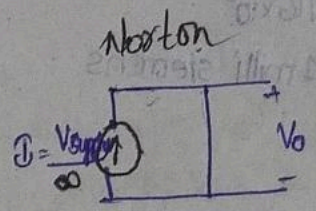
10 million - 1 crore

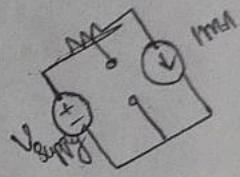
Combinations of voltage sources

Ideal case:



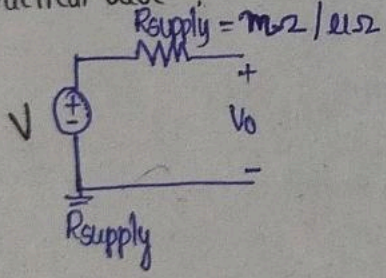
Norton

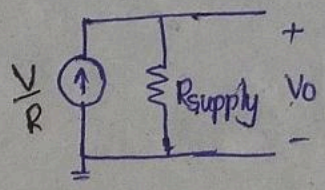




Rsupply - internal resistance of voltage source = 0

practical case:



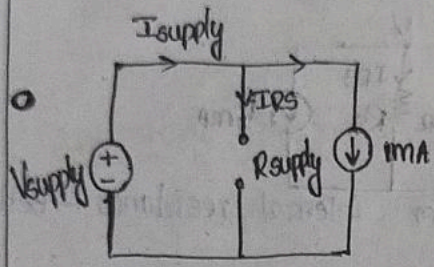


* Vtg source in series with resistant - Thevinin equivalent circuit
* Current source in parallel with resistor - Norton equivalent circuit.
* Internal Resistance of current source = ∞
  Internal resistance of voltage source = 0

10^{-24}	yocto	10^{24}	yotta
10^{-21}	zepto	10^{21}	zetta
10^{-18}	atto	10^{18}	exa
10^{-15}	femto	10^{15}	peta
10^{-12}	pico	10^{12}	tera
10^{-9}	nano	10^{9}	giga
10^{-6}	micro	10^{6}	mega
10^{-3}	milli	10^{3}	kilo
10^{-2}	centi		

DRAWing of I-V characteristics of voltage and current sources

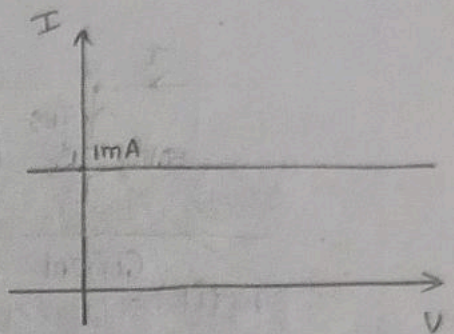
Ideal combination :-



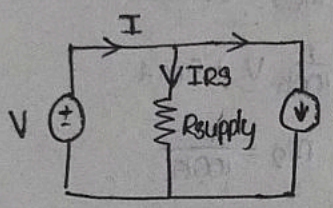
$I = I_{RS} + 1mA$

$I = 1mA \quad (\because I_{RS} = 0)$

$I = 1mA$.



practical:-



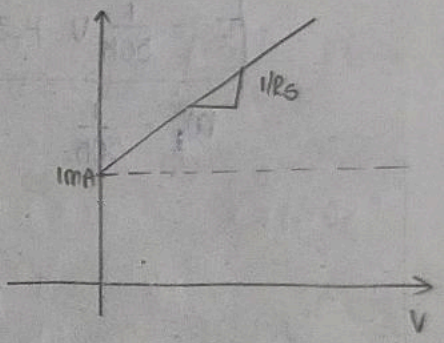
$I = I_{RS} + 1mA$

$I = \frac{V_{supply}}{R_{supply}} + 1mA$.

$I = \frac{1}{R_S} V + 1mA$.

It is of form $y = mx + c$

where $1/R_S$ is slope

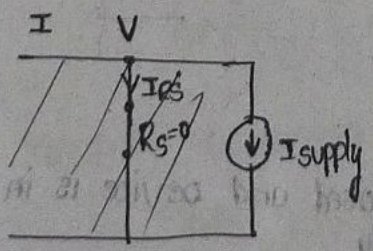


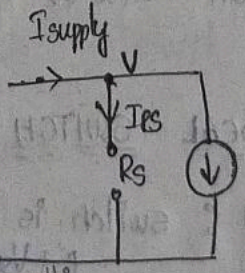
* Practical can be converted to ideal when Vsupply = 0

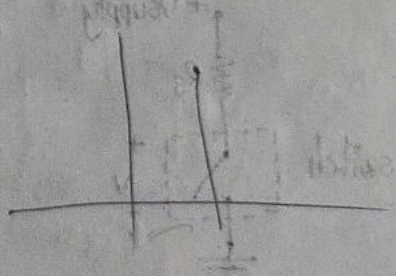
$I = \frac{1}{R_S}(0) + 1mA$

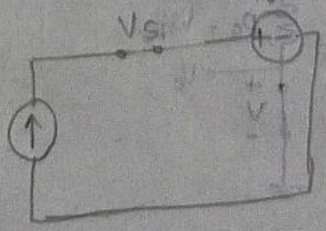
$I = 1mA$ (Ideal)

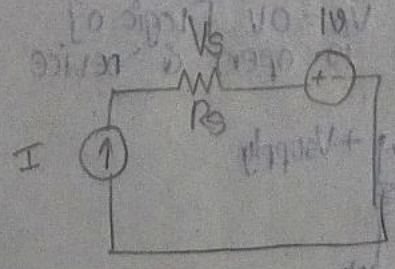
Drawing of I-V characteristics of current.

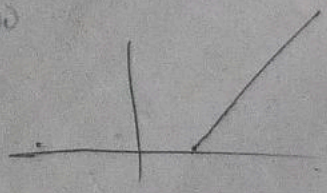




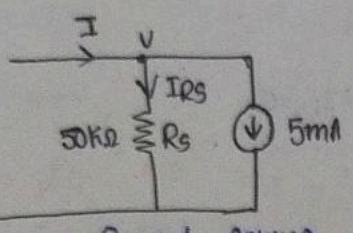


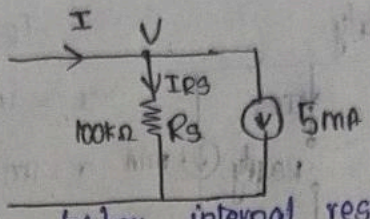






Among the following current sources as shown in below figure which is better current source





Current source having higher internal resistance — Better sou

case(i) :-

$I = I_{RS} + 5mA$

$\boxed{I = \frac{1}{50K} V + 5mA}$

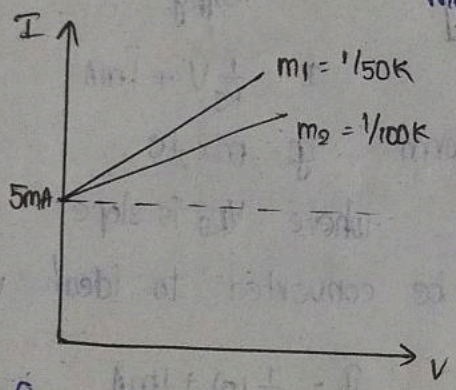
$m_1 = \frac{1}{50K}$

case (ii)

$I = I_{RS} + 5mA$

$I = \frac{1}{100K} V + 5mA$

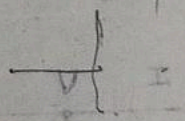
$m_2 = \frac{1}{100K}$



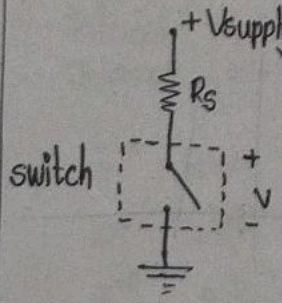
here $m_1 > m_2$

*whenever current source having higher Internal Resistance will be considered as a Better current source.

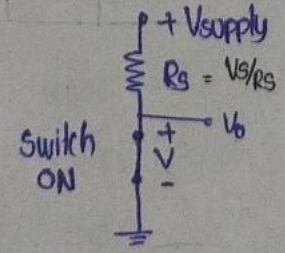
∴ Case (ii) is Better than case (i)



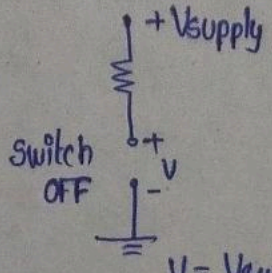
IDEAL SWITCH



case (i) : switch is closed and device is in ON



case (ii) : switch is open & device is in off. $V_o = 0V$ [Logic 0]



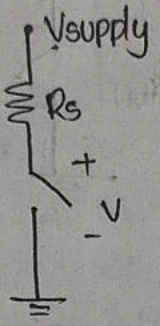
V = Vsupply [Logic 1]

Ideal switch

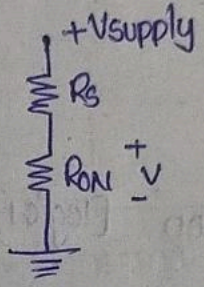
ON → short ckt → V = 0V (logic 0) LOW

OFF → open ckt → V = Vsupply (logic 1) HIGH

PRACTICAL SWITCH :-



case (i) : switch closed, device is in ON

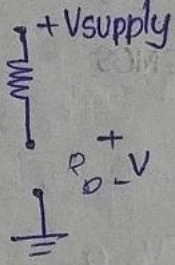


using voltage divider rule,

$$V = V_{supply} \cdot \frac{R_{ON}}{R_{ON} + R_S}$$

$$V = V_{DD} \frac{R_{DON}}{R_{DON} + R_S}$$ [Logic 0]

case (ii) : switch open device OFF



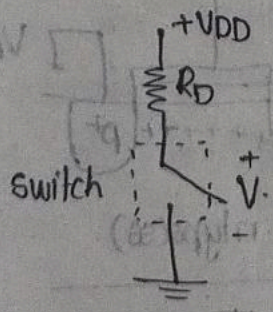
V = Vsupply . [Logic 1]

Practical switch

ON → $V_o = V_{supply} \frac{R_{ON}}{R_{ON} + R_S}$ → [LOGIC 0]

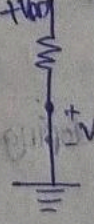
OFF → $V_o = V_{supply}$ → [LOGIC 1]

MOSFET CONSIDERATIONS :-

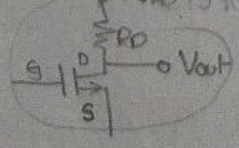


Ideal case:

case(i): switch closed device ON.

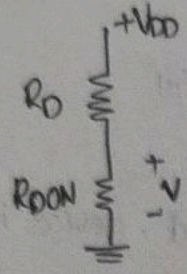


V = 0V

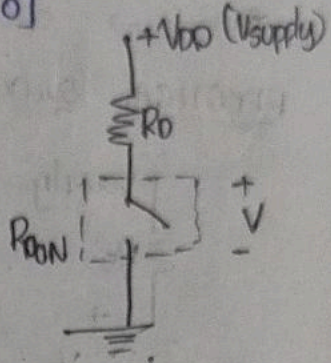


$V_{out} = V_{DD} \frac{R_{DON}}{R_S + R_{DON}}$

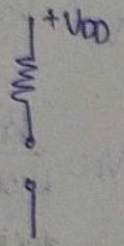
case(i) switch ON



$V = V_{DD} \frac{R_{DON}}{R_{DON} + R_D}$ [logic 0]



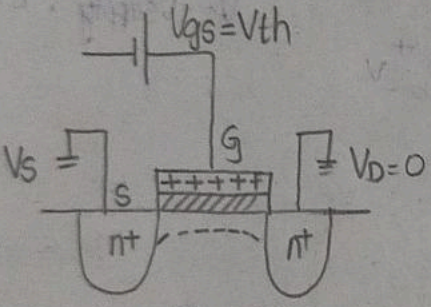
case(ii) switch OFF



V = VDD [logic 1]

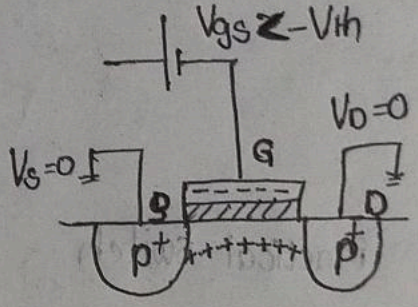
MOSFET STRUCTURES :

Nchannel EMOS



P type (ss)

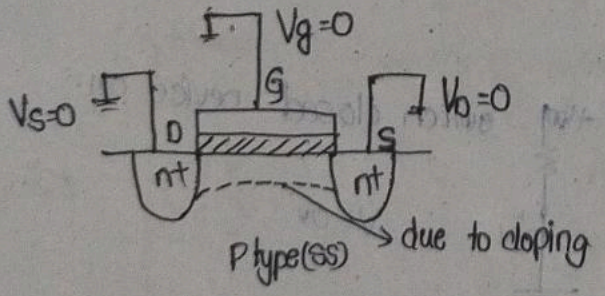
P CHANNEL E-MOS

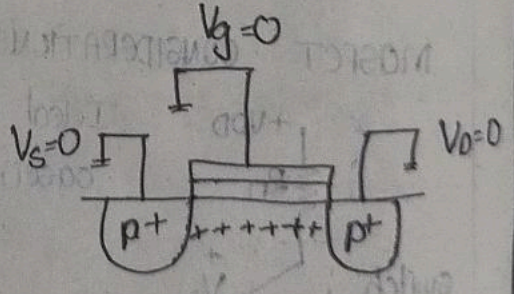


N type (ss)

ENHANCEMENT TYPE MOSFETS

N CHANNEL D-MOS



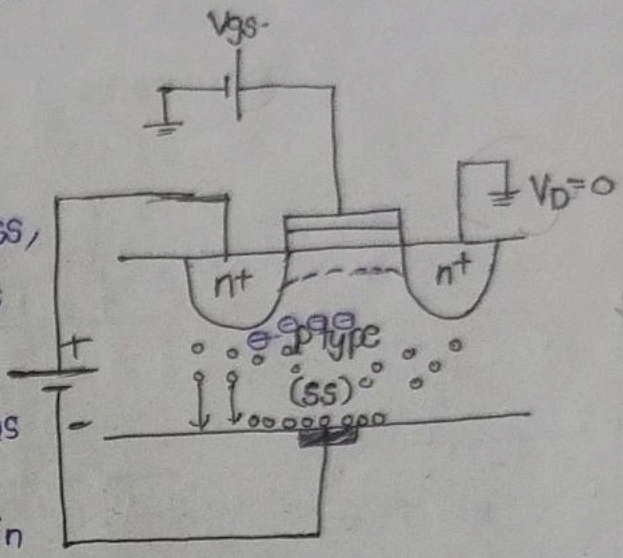


n type (ss)

DEPLETION TYPE MOSFETS

case(i) : when Source and Substrate are biased while grounding drain terminal

case(i) : when -Ve vlg applied to substrate



when -Ve vlg is applied to ss, it attracts more holes towards -Ve terminal of (ss). thus there will be more electrons available in ss. thus there it enhances carrier concentration in the channel. reducing threshold voltage.

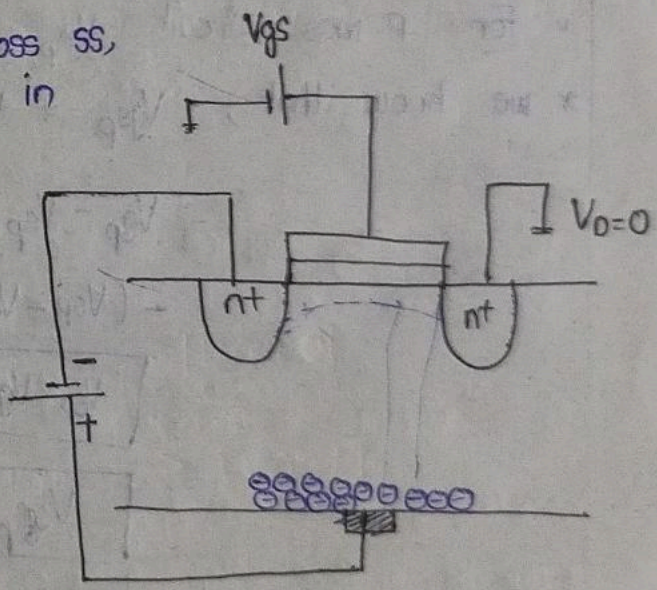
* so that less minimum gate voltage is required to turn ON MOSFET as threshold voltage is decreased.

case(ii) when +Ve vlg applied to ss

when +Ve voltage applied across ss, it depletes carrier concentration in channel region.

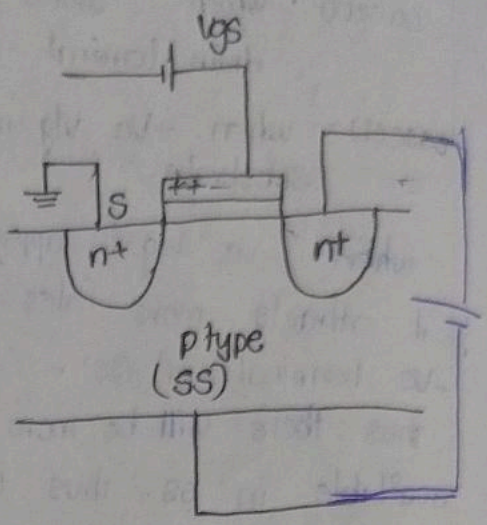
So it MOSFET's threshold voltage increases.

Its needs higher gate to source voltage to turn ON MOSFET.



* when applying voltage btw Source and Substrate by grounding drain terminal, influences threshold voltage of MOSFET. It is as called as "Body effect (or) Back gate terminal effect". Here ss acts as back gate terminal.

When source grounded, drain & subracte are biased



* Condition for Saturation region of N MOS is $V_{DS} \geq V_{gs} - V_{th}$
* For NP-MOS circuit, $V_{gs_n} \geq V_{th_n}$
* For P-MOS circuit $V_{gs_p} \leq V_{th_p}$
* we know that, $V_{gs_p} = V_{g_p} - V_{sp}$

$$V_{g_p} - V_{sp} \leq -V_{th_p}$$

$$-(V_{sp} - V_{g_p}) \leq V_{th}$$

$$\boxed{V_{sp} - V_{g_p} \geq +V_{th}}$$

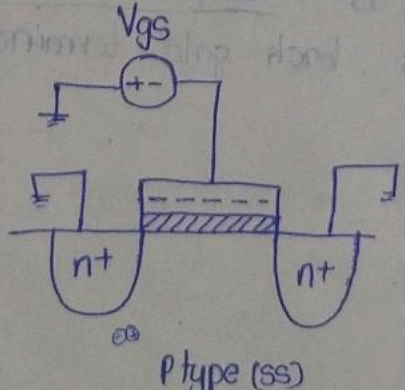
$$\boxed{V_{sg_p} \geq |V_{thp}|}$$

$V_{sg} \geq V_{th}$

$V_{gs} \leq V_{th}$

If we apply V_{gs} is equal to -Ve voltage in NMOS, is there any channel creating or not?

No channel is created

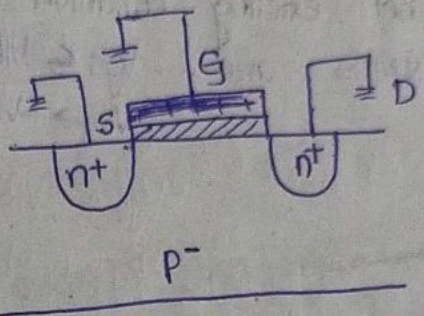


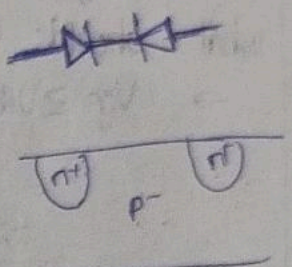
here no channel is created due to -Ve voltage applied at gate. [ē -Ve charge on gate repelled -Ve ēs in ss thus

no channel will be former

* For PMOS, due to -Ve voltage at gate, a channel is created ↓ +Ve conductive channel

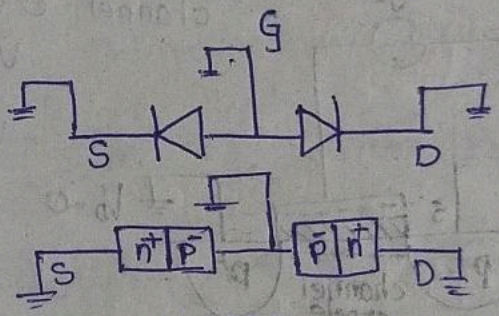
Q) What happens when no gate voltage Applied

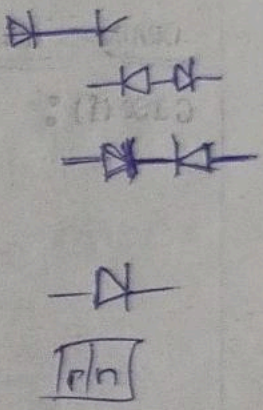




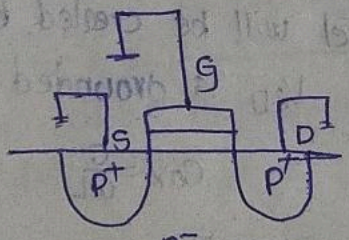
No channel created.

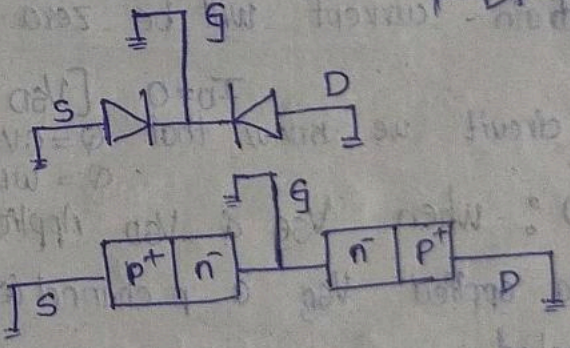
$V_{GS} = 0$





$V_0 = V_t \ln\left(\frac{NAND}{n_i^2}\right)$





If $V_{GS} = 0$ $V_{DS} = 1V$ then what is I_D (EMOS)

$I_D = 0$ since no channel is created due no voltage appled at gate terminal

* For DMOS current will be flowing
* ~~For PMOS current will be flowing~~ in Enhancement MOS

Polarity of V_{TH} in NMOS & PMOS;

ANS: In NMOS $V_{TH} > 0$

In PMOS $V_{TH} < 0$.

In order to create a channel in NMOS, what should be polarity of V_{gs}.

$V_{gs} > 0$ For NMOS

$V_{gs} < 0$ For PMOS

what should be channel existing condition for NMOS & PMOS

→ $V_{gs} \geq V_{th}$ for NMOS and $V_{gs} \leq -V_{th}$ for PMOS

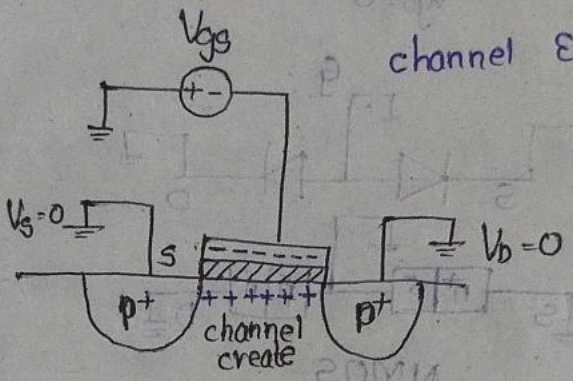
$V_{sg} \geq -V_{th}$. $V_{sg} \geq +V_{th}$

$V_{gs} \leq -V_{th}$

$V_{sg} \geq |V_{th}|$

DRAIN CURRENT DERIVATION FOR P-CHANNEL ENHANCEMENT TYPE

Case (i):



channel Existing condition

$V_{sg} \geq |V_{thp}|$

$V_{sg} \geq -|V_{th}|$

when V_{sg} applied ($V_{sg} > V_{th}$) channel will be created but the drain current will be zero since V_{SD} is grounded

$I_D = 0$ $[V_{SD} = 0]$ $C_{ox} = \frac{C}{WL}$

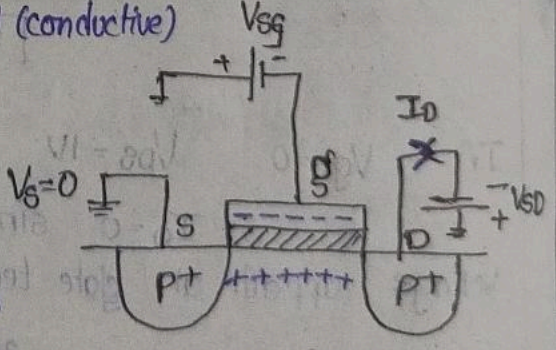
From circuit we know that $Q = CV$

$Q = WL C_{ox} [V_{sg} - |V_{th}|]$

case (ii): when V_{sg} & V_{SD} Applied

* Due to applied V_{sg} a p channel (conductive) is created.

* Due to Applied V_{SD} voltage, the holes in p channel will move from source to drain. Thus there will be flow of drain current from source to drain



* Drain Current will be given by

$$I_D = Q_d \times v$$

$v = \mu_p E$ $\quad cm^2/V\text{-}S$ ~~volt/cm~~

$v = +\mu_p \frac{dv(x)}{dx}$

+ve since holes, current in same direction.

$$Q_d = W C_{ox} [V_{sg} - |V_{tp}| - V(x)]$$

$$\therefore \quad I_D = Q_d v$$

$$I_D = \mu_p W C_{ox} [V_{sg} - |V_{tp}| - V(x)] \frac{dv(x)}{dx}$$

$$I_D dx = \mu_p W C_{ox} [V_{sg} - |V_{tp}| - V(x)] dv(x)$$

Integrating on both sides

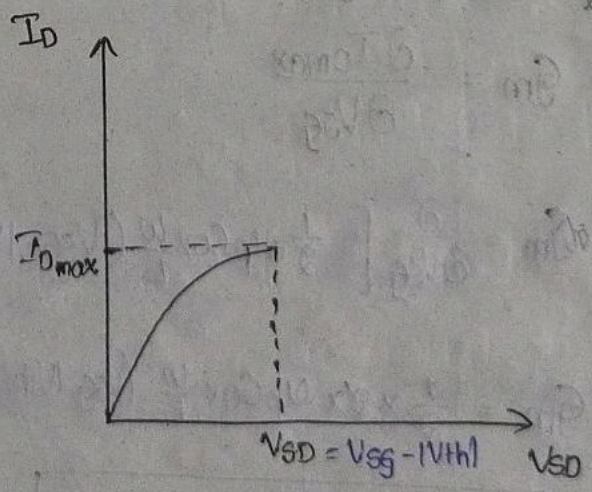
$$\int_0^L I_D dx = \int_0^{V_{SD}} \mu_p W C_{ox} [V_{sg} - |V_{th}| - V(x)] dv(x)$$

$$I_D L = \mu_p W C_{ox} (V_{sg} - |V_{th}|) V_{SD} - \frac{V_{SD}^2}{2}$$

$$I_D = \mu_p \frac{W}{L} C_{ox} \left[(V_{sg} - |V_{tp}|) V_{SD} - \frac{V_{SD}^2}{2} \right]$$

* Above is Drain current equation for p-channel Enhancement type MOSFET.

*



MAXIMUM DRAIN CURRENT EQUATION.

$$\frac{\partial I_D}{\partial V_{SD}} = 0$$

$$\frac{\partial}{\partial V_{SD}} \left[\mu_p \frac{W}{L} C_{ox} \left[(V_{sg} - |V_{th}|) V_{SD} - \frac{V_{SD}^2}{2} \right] \right] = 0$$

$$\mu_p \frac{W}{L} C_{ox} [V_{sg} - |V_{th}| - V_{SD}] = 0$$

$$V_{SG} - |V_{thl}| - V_{SD} = 0$$

$$\boxed{V_{SD} = V_{SG} - |V_{thl}|}$$

* $$I_{Dmax} = \mu_p \frac{W}{L} C_{ox} \left[(V_{SG} - |V_{thl}|)(V_{SG} - |V_{thl}|) - \frac{(V_{SG} - |V_{tpl}|)^2}{2} \right]$$

$$I_{Dmax} = \frac{1}{2} \mu_p \frac{W}{L} C_{ox} (V_{SG} - |V_{thl}|)^2$$

$$\boxed{I_{Dmax} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{thl}|)^2}$$

DRAIN RESISTANCE

$$R_D = \frac{V_{SD}}{I_D}$$

$$R_D = \frac{V_{SD}}{\mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{tpl}|) V_{SD}} \quad [\because \text{Neglecting } \frac{V_{SD}^2}{2}]$$

$$\boxed{R_D = \frac{1}{\mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{tpl}|)}}$$

TRANS CONDUCTANCE (G_m) :-

$$G_m = \frac{\partial I_{Dmax}}{\partial V_{SG}}$$

$$G_m = \frac{\partial}{\partial V_{SG}} \left[\frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{tpl}|)^2 \right]$$

$$G_m = \frac{1}{2} \times 2 \times \mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{tpl}|)$$

$$\boxed{G_m = \mu_p C_{ox} \frac{W}{L} [V_{SG} - |V_{tpl}|]} \quad \text{---- (1)}$$

* we know $I_{Dmax} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{sg}-|V_{thp}|)^2$

$$[V_{sg}-|V_{tp}|]^2 = \frac{2I_{Dmax}L}{\mu_p C_{ox} W}$$

$$V_{sg}-|V_{th}| = \sqrt{\frac{2I_{Dmax}L}{\mu_p C_{ox} W}}$$

$$G_m = \mu_p \frac{W}{L} C_{ox}(V_{sg}-|V_{th}|) \quad \rightarrow V_{sg} \geq |V_{th}| \quad V_{SD} \geq V_{sg}-|V_{thp}|$$

$$G_m = \mu_p \frac{W}{L} C_{ox}\sqrt{\frac{2I_{Dmax}L}{\mu_p C_{ox} W}}$$

$$\boxed{G_m = 2I_{Dmax}\frac{W}{L}\mu_p C_{ox}} \quad -(2)$$

* $$\frac{G_m}{I_{Dmax}} = \frac{\mu_p C_{ox}\frac{W}{L}[V_{sg}-|V_{tp}|]}{\frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{sg}-|V_{tp}|)^2}$$

$$\boxed{G_m = \frac{2I_{Dmax}}{V_{sg}-|V_{th}|}} \quad -(3)$$

* For a given NMOS, $\mu_n C_{ox} = 2mA/V^2$ $(\frac{W}{L})n = 2$ $V_{gsn} = 2$ volt
$V_{thn} = 1$ volt $V_{DS} = 1V$ find I_D. find R_D. G_m

$$I_{Dmax} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[V_{gsn}-V_{thn}]^2 \quad V$$

$$= \frac{1}{2} 2 \times 2 (2-1)^2 = 2mA$$

$$I_{DS} = \mu_n C_{ox}\frac{W}{L}\left[(V_{gsn}-V_{thn})^2 V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$= 2 \times 2 \left[1-\frac{1}{2}\right] = 2 \times 2 \times \frac{1}{2} = 2mA$$

$$R_D = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{sgn}-V_{thn})} = \frac{1}{2\times 10^{-3} \times 2(2-1)} = \frac{1}{4} \times 10^3$$

$$\boxed{R_D = 0.25\,K\Omega} = 250\Omega.$$

$$G_m = \mu_n C_{ox}\frac{W}{L}(V_{sgn}-V_{thn}) = 2\times 10^{-3} \times 2(2-1) = 4 \text{ milli siemes}.$$

$$G_m = \frac{2I_{Dmax}}{V_{eg}-V_{th}} = \frac{2(2mA)}{1V} = 4\,mA/V = 4 \text{ milli siemens}$$

$$G_m = \sqrt{2 \times I_{Dmax}\mu_n C_{ox}\frac{W}{L}} = \sqrt{2\times 2\times 2\times 2\times 10^{-6}} = 4 \text{ milli siemes}$$

Why source and drain in MOSFET are not interchangable.

* Though MOSFET is a symmetrical device, the source and drain of mosfet cannot be interchanged due to

1) manufacturing process: By default manufacturer defines the properties of MOSFET during the time of manufacturing. source & drain are intentionally designed to have slightly different characteristics to optimise device these are non-interchangable.

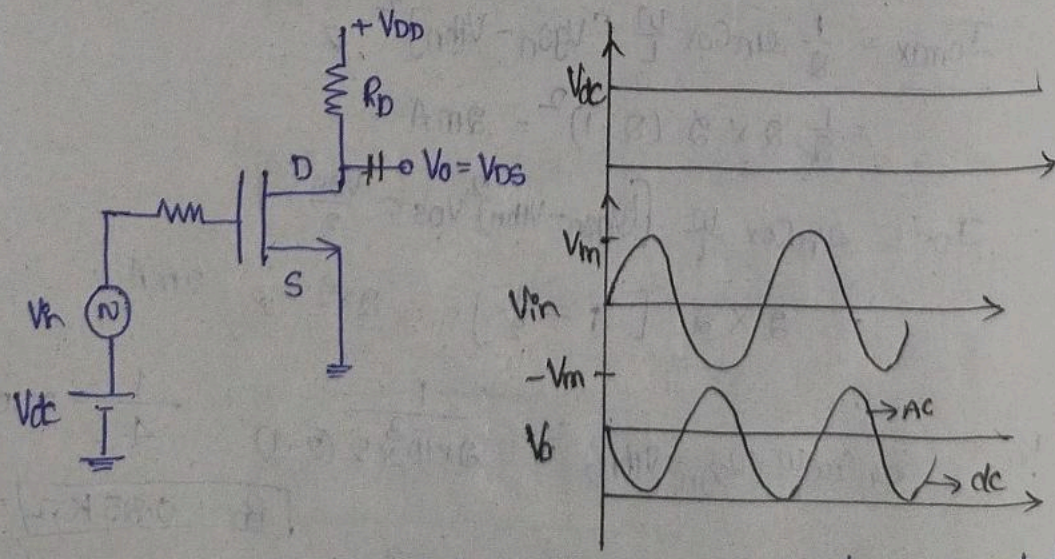
* Also the source and substrate are internally connected but drain not connected. this will lead to slight assymbrical doping so that they can't be interchanged.

* Source provides carriers to flow & drain collects that carriers. these two have different functionalities. maybedue to this they can't be interchangable.

* ~~Oncle~~ silicon Once made of silicon, they are slightly different because of angular doping (not 90°) with respect to silicon substrate. But they cannot be interchangable.

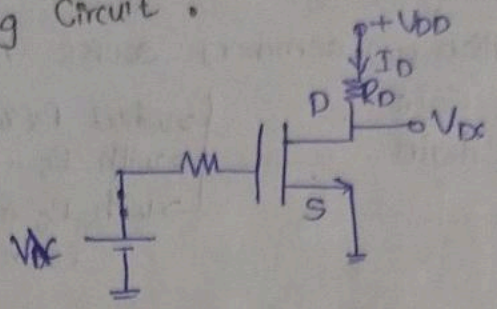
* Body biasing is also one of reason to not interchange drain & source

Biasing of MOSFET



To get pure ac as output we can use capacitor at output.

DC Biasing Circuit :



drain

[less threshold

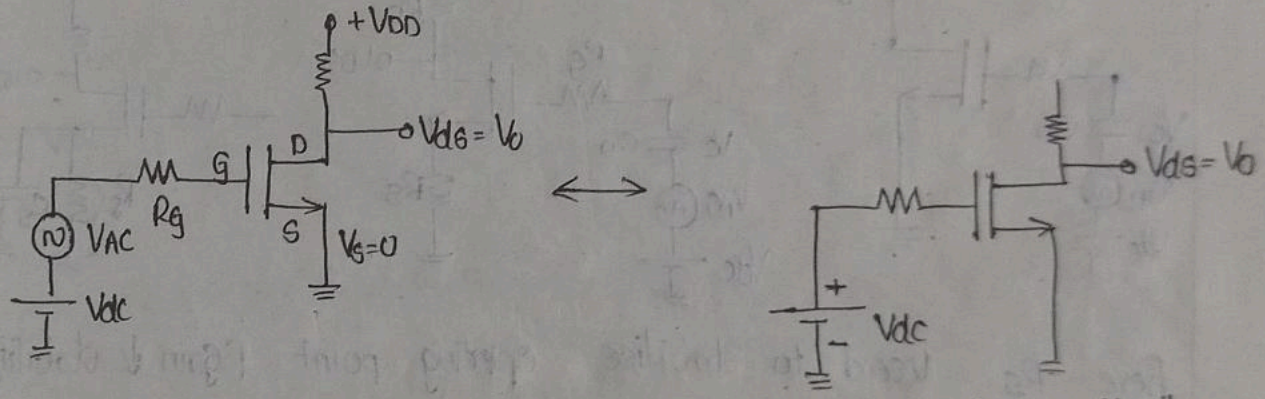
whenever mosfet is used as Amplifier, it must be biased.

* Amplifier strengthens the input weak signal.

SMALL SIGNAL Analysis

* when doing DC analysis, Vtg source - short ckt
  AC current source - open circuit
  capacitor - open circuit
  Inducter - short circuit

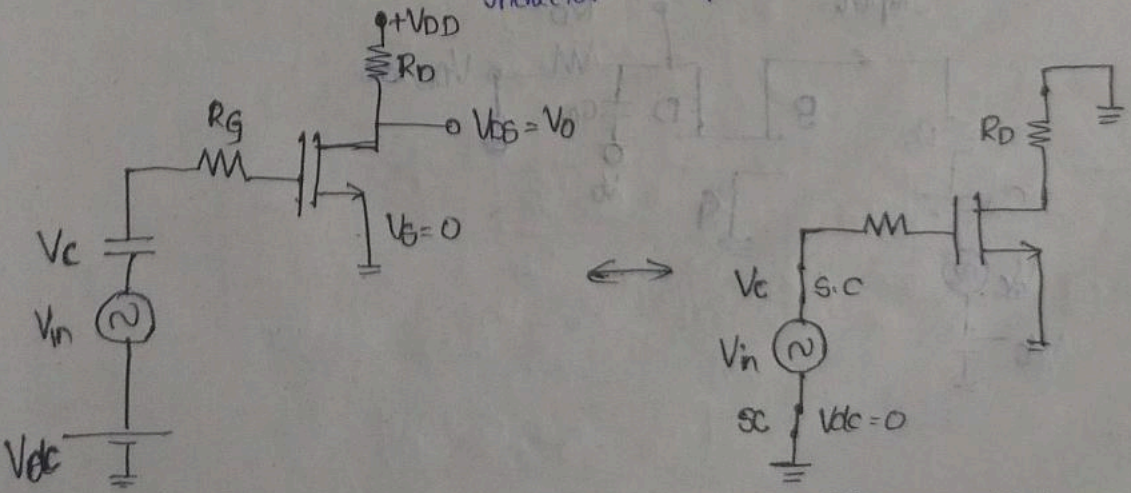
* while doing DC analysis all the AC components must be removed
  i.e AC vlg source - short ckt etc



DC equivalent Circuit

MOSFET

* while doing AC analysis, DC components must be removed
  i.e DC vlg source - short ckt
  DC current source - open ckt
  Capacitor - short circuit
  Inductor - open circuit



AC EQUIVACENT CIRCUIT

common configurations

(1) common source configuration (or) common source Amplifier
- Input terminal = Gate
- output terminal = drain
  - without R_S (source resistance)
  - with R_S
  - with R_S and C_S [source capacitance]

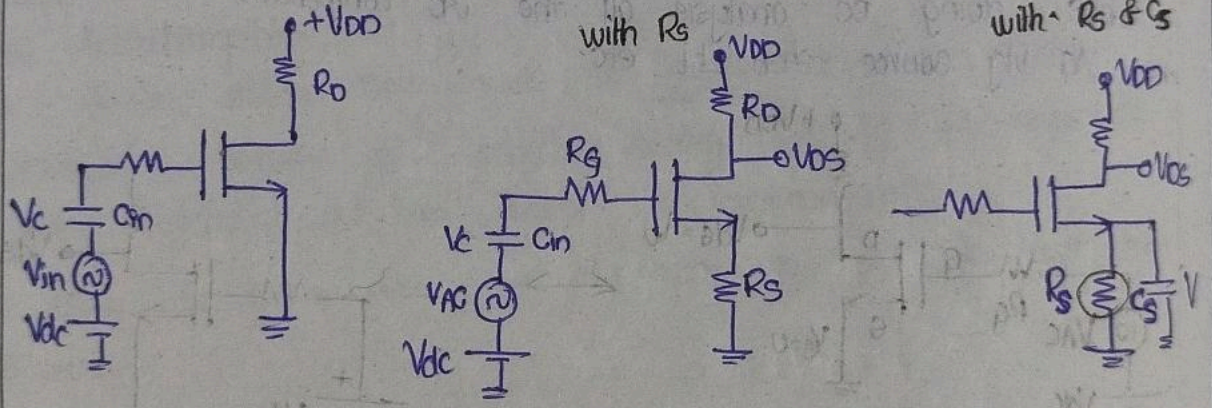
(2) common gate Amplifier
- i/p = source
- o/p = drain

(3) common drain Amplifier
- i/p - gate
- o/p - source

gain ↓ stability ↑

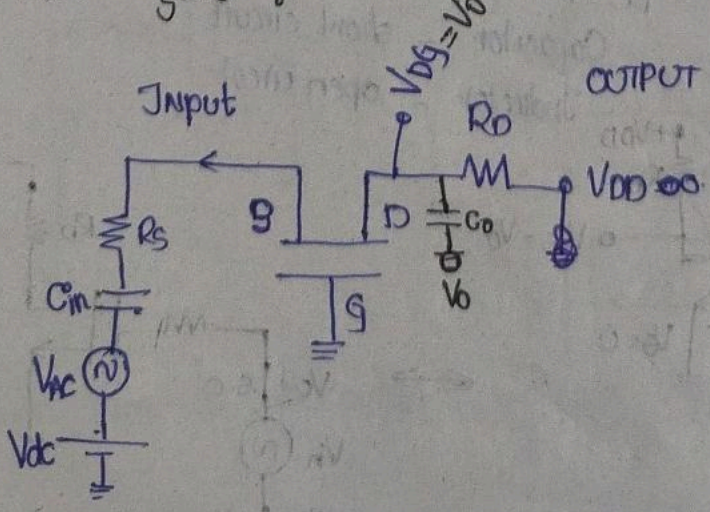
* Capacitor at source → gain increases, stability Increases

common source Amplifiers:-

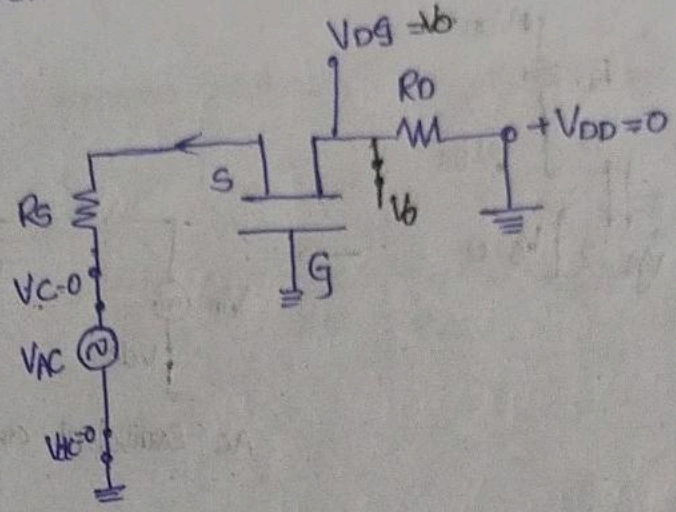


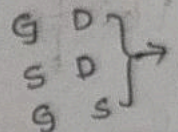
Here R_S used to stabilise operating point [Gain ↓ stability ↑]
when C_S is placed [gain ↑ stability ↑]

common gate :

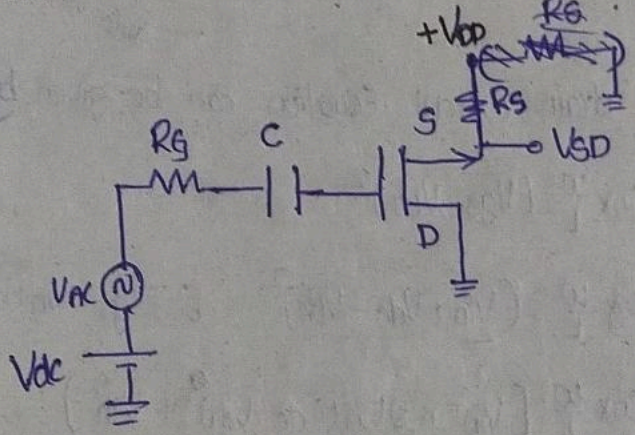


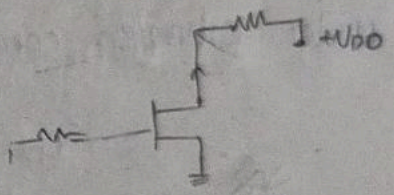
AC EQUAIVALENT CIRCUIT :



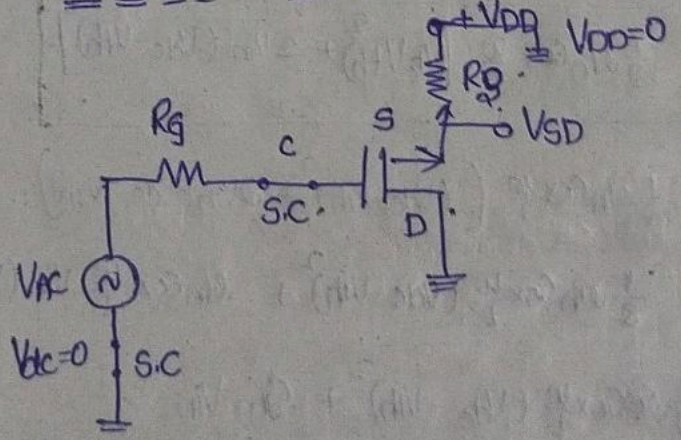


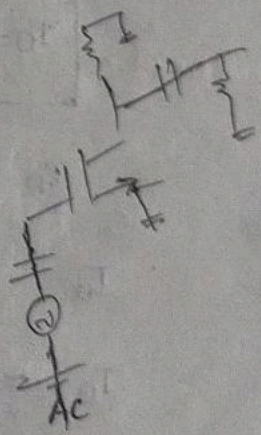
Common DRAIN AMPLIFIER :

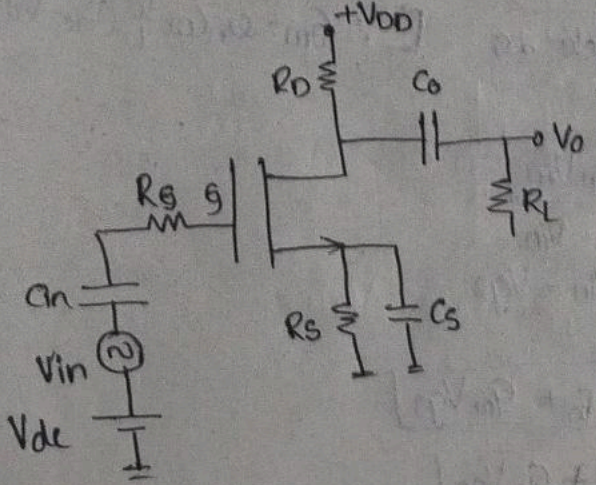


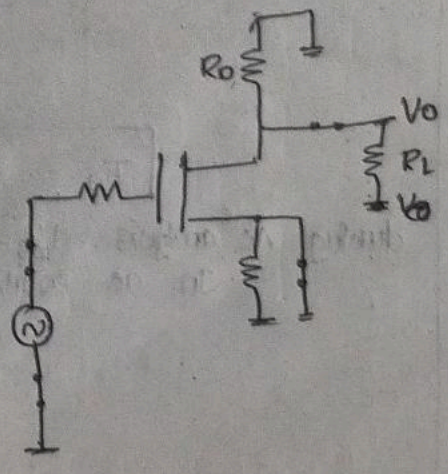


AC EQUIVALENT CIRCUIT :

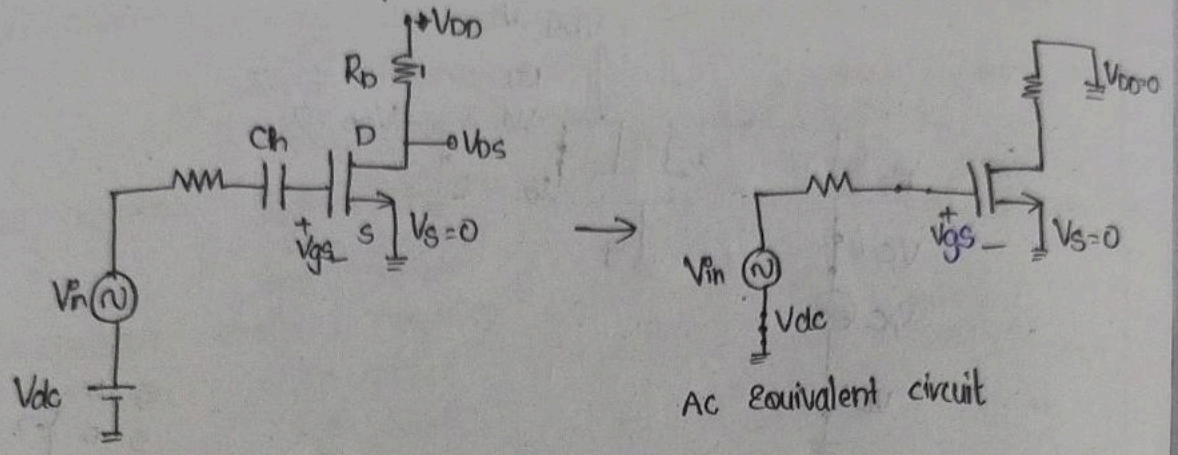








COMMON GATE Amplifier:-



Ac Equivalent circuit

from above circuit,

$$\boxed{V_{gs} = V_{in} + V_{dc}}$$

$V_{in} + V_{dc}$ ... $(V_{dc} - V_{th})^2$ +

under saturation condition, drain current Equation can be given by

$g_D = g_o + g_m V_{gs}$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[V_{in} + V_{dc} - V_{th}]^2 \quad [\because V_{gs} = V_{in} + V_{dc}]$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[V_{in}^2 + 2V_{in}(V_{dc} - V_{th}) + V_{th}^2)$$

here $V_{in}^2 <<< V_{th}(V_{dc} - V_{th})^2$

$$\boxed{I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[(V_{dc} - V_{th})^2 + 2V_{in}(V_{dc} - V_{th})]}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left((V_{dc} - V_{th})^2 + 2V_{in}(V_{dc} - V_{th})\right)$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{dc} - V_{th})^2 + \mu_n C_{ox}\frac{W}{L}V_{in}(V_{dc} - V_{th})$$

$$I_D = \underbrace{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{dc} - V_{th})^2}_{\text{complete dc}} + G_m V_{in} \quad [\because G_m = \mu_n C_{ox}\frac{W}{L}(V_{dc} - V_{th})]$$

$$\boxed{I_D = I_{DO} + G_m V_{in}}$$

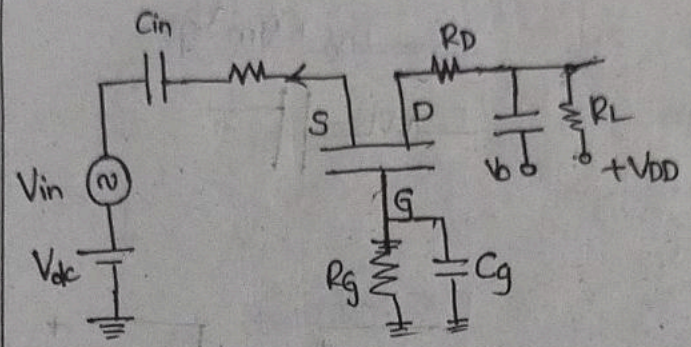
during AC analysis $V_{gs} = V_{dc} + V_{in} = V_{in}$.

In ac equivalent $V_{in} = V_{gs}$

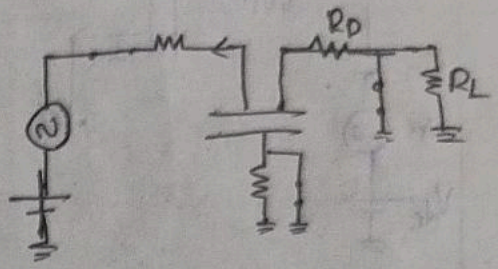
$$\boxed{I_D = I_{DO} + G_m V_{gs}}$$

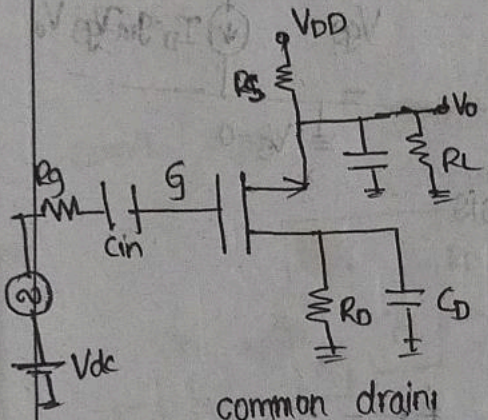
$$\boxed{I_D = I_D + G_m V_{gs}}$$

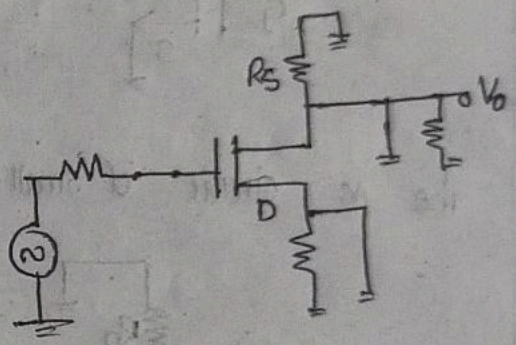
common gate



AC Equivalent

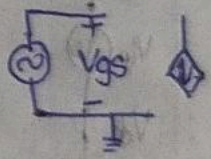


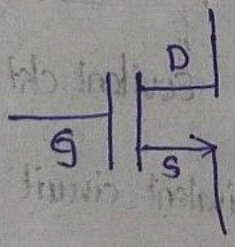


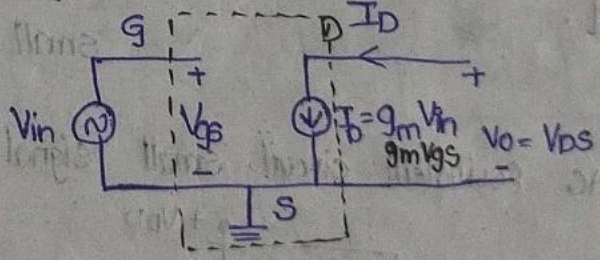


common drain

* In ac analysis, draw AC equivalent circuit from Eq? $I_D = I_{DQ} + g_m V_{gs}$







AC EQUIVALENT CIRUIT

(1) Identify ac components in circuit

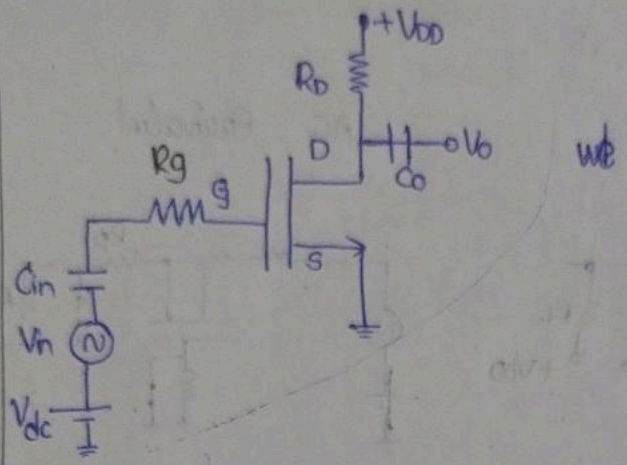
(2) S.C voltage } either independent (or) dependent sources
(3) O.P current

S.C capacitor [all capacitors must be shorted]

O.P Inductor

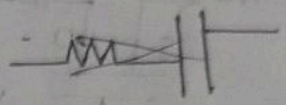
(4) draw AC Equivalent Ckt without ac components.

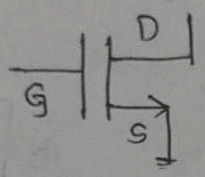
* 0

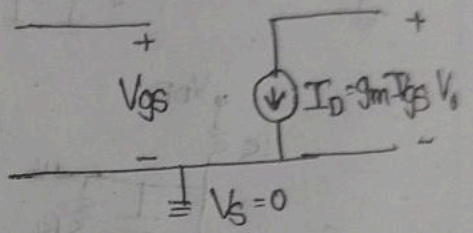


we

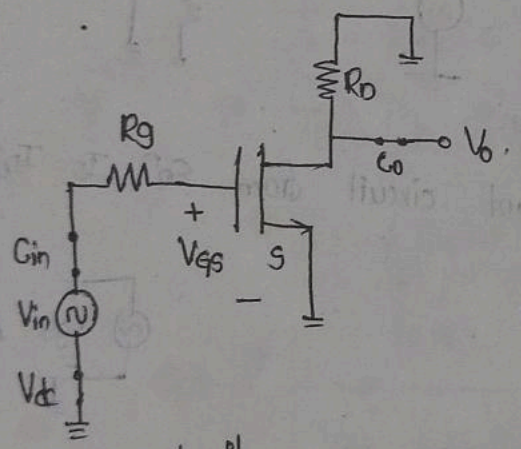
$I_D = I_{DO} + g_m V_{gs}$.



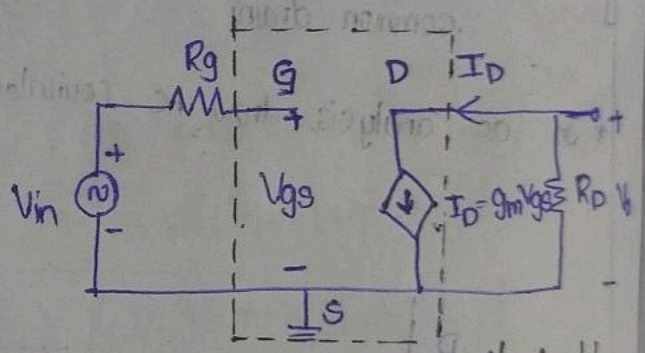




the AC circuit of small signal Analysis

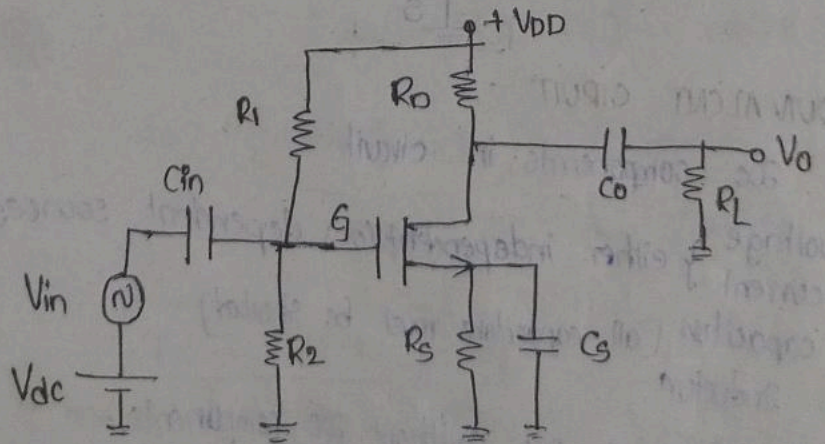


AC circuit.



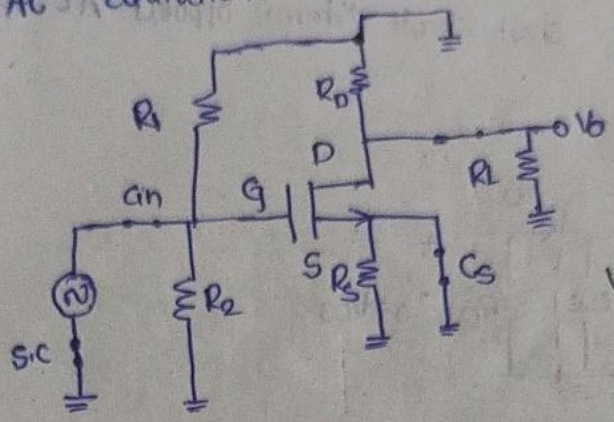
small signal Equilent ckt

Q) draw AC Equivalent circuit, small signal equivalent circuit

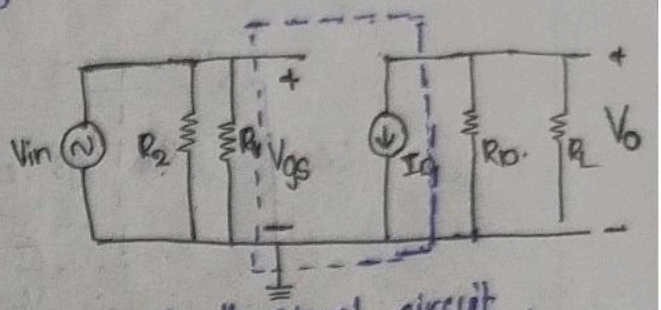


single stage Amplier

AC Equivalent circuit:

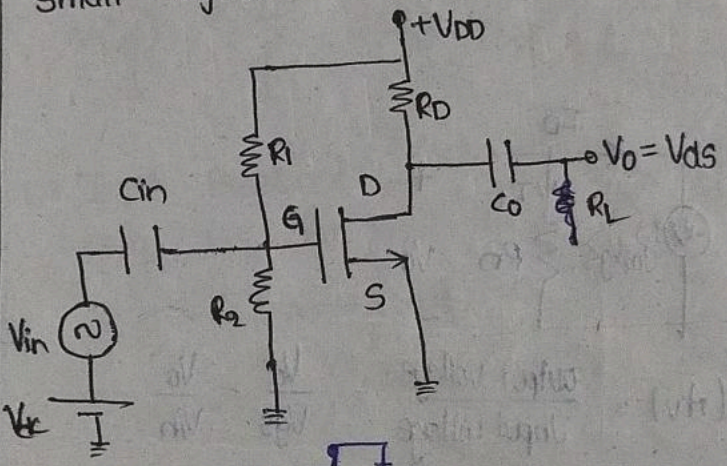


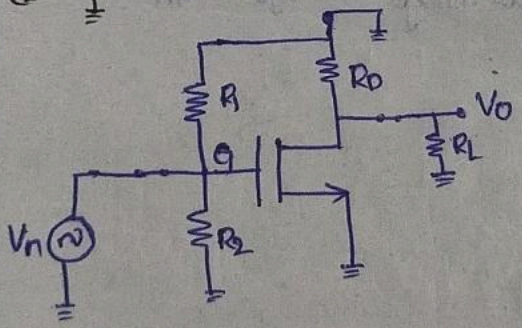
AC Equivalent circuit.

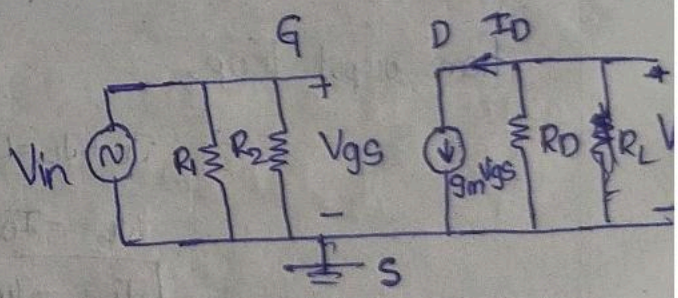


Small signal circuit.

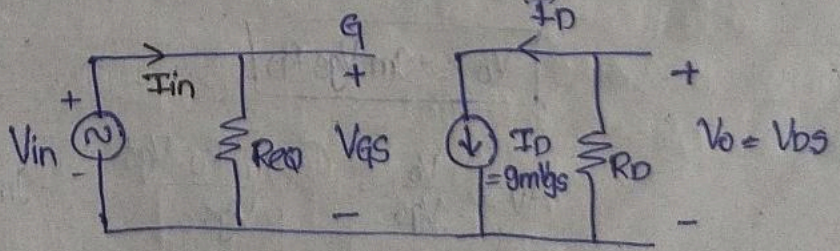
Small signal Analysis of common source Amplifier







here $R_{eq} = \frac{R_1 R_2}{R_1 + R_2}$



1) Input Resistance ($R_{in} = Z_{in}$) :-

Apply KVL for input loop

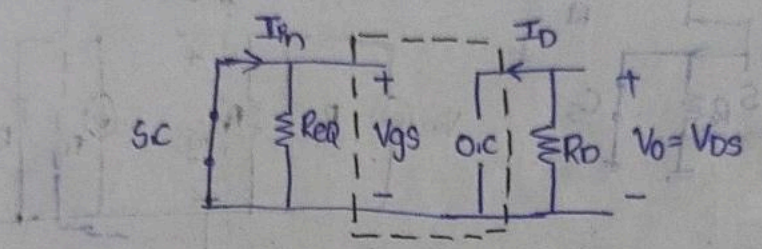
$$-V_{in} + I_{in} R_{eq} = 0$$

$$R_{eq} = \frac{V_{in}}{I_{in}}$$

$$R_{in} = \frac{V_{in}}{I_{in}} = R_{eq} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

2) Output Resistance ($R_{out} = Z_{out}$)

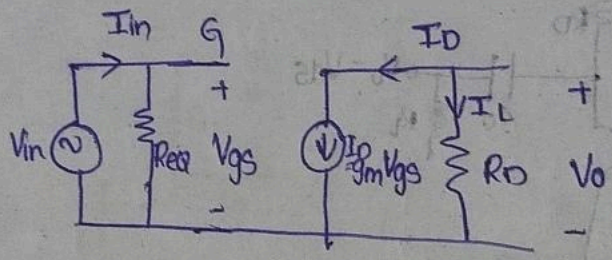
x to obtain output resistance, short circuit external applied AC source, open circuit current source



$$R_o = \frac{V_o}{I_D} = R_D \quad [\lambda = 0]$$

when $(\lambda \neq 0)$ $R_o = r_d // R_D$

3) Voltage Gain :-



$$\text{Voltage Gain } (A_V) = \frac{\text{output voltage}}{\text{Input voltage}} = \frac{V_o}{V_{gs}} = \frac{V_o}{V_{in}}$$

from output loop,

$$I_D + I_L = 0$$

$$I_L = -I_D$$

$$\boxed{I_L = -g_m V_{gs}}$$

$$V_o = I_L R_D$$

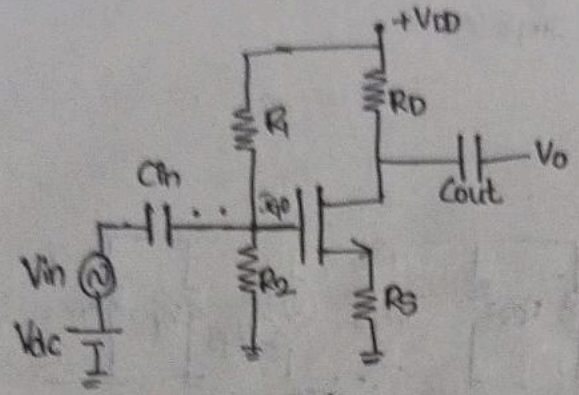
$$\boxed{V_o = -g_m V_{gs} R_D}$$

$$A_V = \frac{V_o}{V_{gs}} = \frac{-g_m R_D V_{gs}}{V_{gs}} = -g_m R_D$$

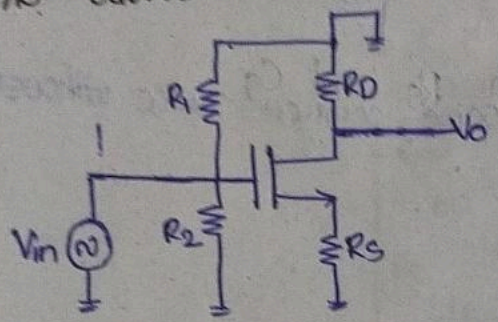
$$\boxed{A_V = -g_m R_D}$$

-Ve indicates output resistance.

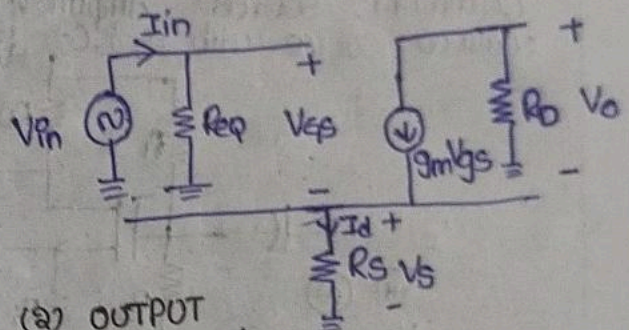
Common Source Amplifier with Source Resistance :-



AC equivalent circuit



small signal Analysis



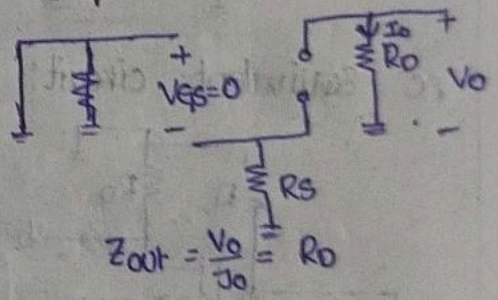
(1) Input Resistance :-

Apply KVL for input

$$-V_{in} + I_{in}(R_{eq}) = 0$$

$$Z_{in} = \frac{V_{in}}{I_{in}} = R_{eq} = R_1 \| R_2$$

(2) OUTPUT Impedence :-



$$Z_{out} = \frac{V_o}{I_o} = R_D$$

(3) Voltage Gain :-

$$A_V = \frac{V_o}{V_{in}}.$$

$$I_o + I_L = 0$$

$$I_o = -I_D = -g_m V_{gs}.$$

$$V_o = I_o R_D = -g_m V_{gs} R_D.$$

apply KVL for input loop,

$$-V_{in} + V_{GS} + V_S = 0$$

$$V_{in} = V_{GS} + V_S.$$

$$V_{in} = V_{GS} + I_D R_S = V_{GS} + g_m V_{GS} R_S$$

$$= V_{GS}[1 + g_m R_S]$$

$$A_V = \frac{V_o}{V_i} = \frac{-g_m V_{GS} R_D}{V_{GS}(1 + g_m R_S)} = \frac{-g_m R_D}{1 + g_m R_S}.$$

$$\boxed{A_V = \frac{-g_m R_D}{1 + g_m R_S}}$$

when $\lambda = 0$

$Z_{out} = R_D$ High → low impedence

$Z_{in} = R_1 \| R_2$

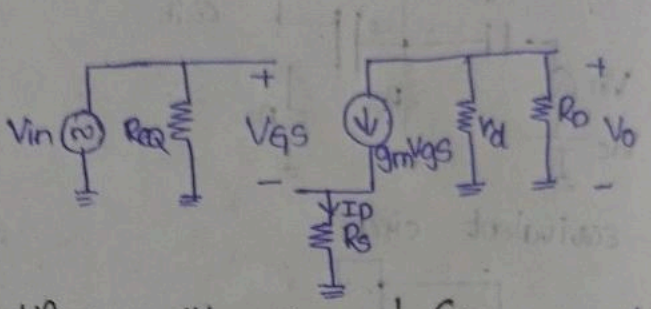
$A_V = \frac{-g_m R_D}{1 + g_m R_S}$

when $\lambda \neq 0$

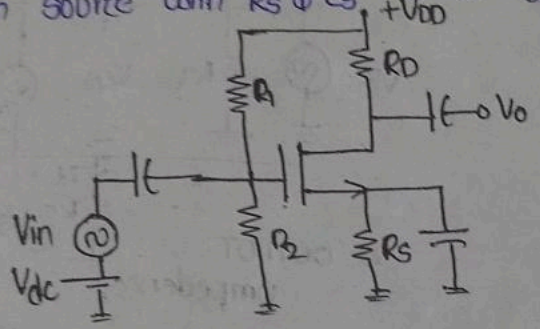
$Z_{in} = R_{eq}$

$Z_{out} = R_D \| r_d$

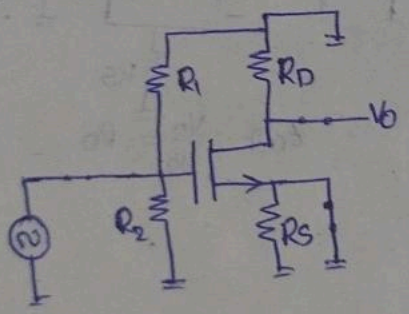
$A_V = \frac{-g_m (R_D \| r_d)}{1 + g_m R_S}$



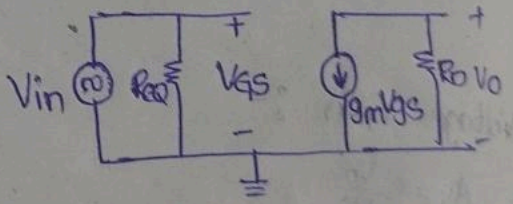
common source Amplifier with R_S and C_S is same as common source without common source with R_S & C_S



AC equivalent circuit:



small signal circuit:-



case(i) : $\lambda = 0$

$Z_{out} = R_D$

$Z_{in} = R_1 R_2 / R_1 + R_2$

$A_V = \frac{V_o}{V_{in}} = \frac{-g_m R_D}{1 + g_m R_S}$

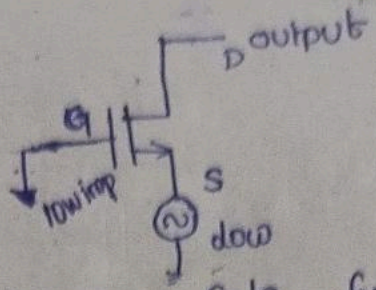
case ii) $\lambda \neq 0$

$Z_{out} = R_D \| r_d$

$Z_{in} = R_{eq}$

$A_V = \frac{-g_m (R_D \| r_d)}{1 + g_m R_S}$

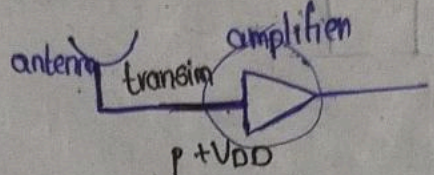
Common Gate Amplifier :-

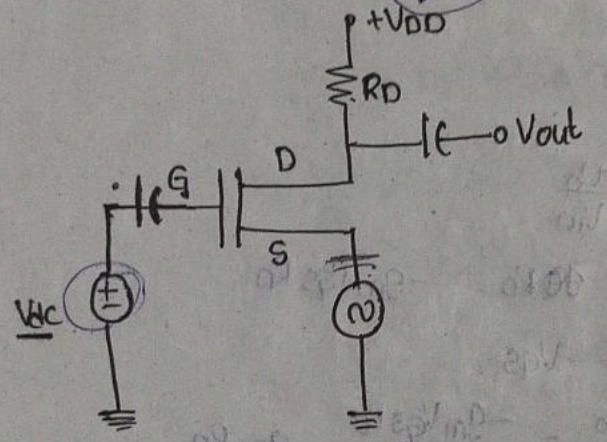


Unlike other, in common Gate, here low input Impendence is provided.

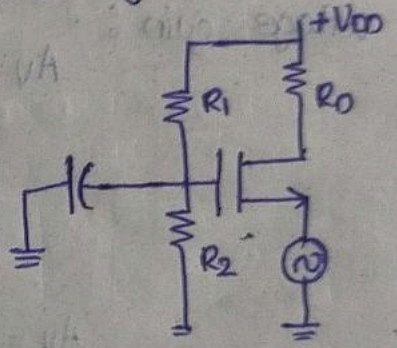
* used in high frequency applications.

cloud



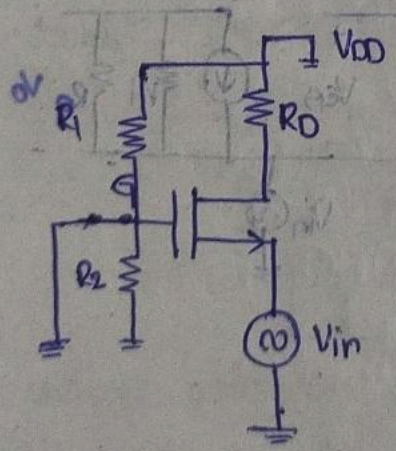


Here Biasing also provided by self biasing circuit

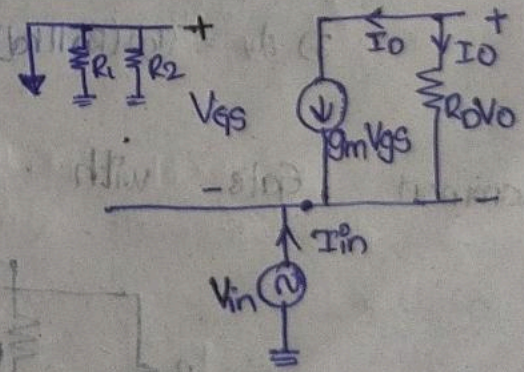


Consider a circuit :

AC equivalent circuit



small signal model



1) Input impedence : $Z_{in} = \frac{V_{in}}{I_{in}}$

apply KCL, $-I_{in} - I_D = 0$

$I_{in} = -I_D$

$I_D = -I_{in}$

$I_D = +g_m V_{gs}$

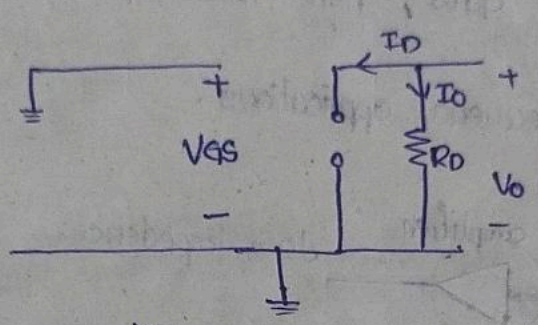
$I_{in} = -g_m V_{GS}$ $\quad V_{in} = -V_{gs}$

$I_{in} = -g_m(-V_{in})$

$I_{in} = g_m V_{in}$

$\frac{V_{in}}{I_{in}} = 1/g_m$

2) output Impedence:-



$Z_{out} = \frac{V_o}{I_D} = R_D$

3) voltage gain :

$A_V = \frac{-V_o}{V_{in}}$

$V_o = -I_D R_D = -g_m V_{GS} R_D$

$V_{in} = -V_{GS}$

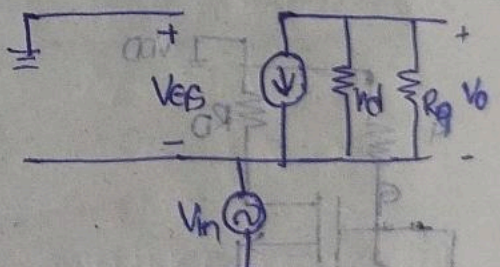
$A_V = \frac{V_o}{V_{in}} = \frac{-g_m V_{GS} R_D}{-V_{GS}} = g_m R_D$

$\boxed{A_V = g_m R_D}$

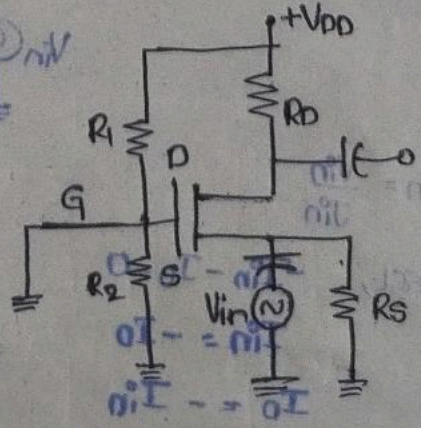
if $\partial \neq 0$:- 1) $Z_{in} = \frac{V}{g_m}$

2) $Z_{out} = R_D \| r_d$

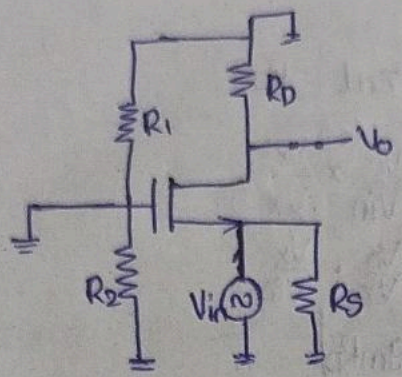
3) $A_V = -g_m(R_D \| r_d)$



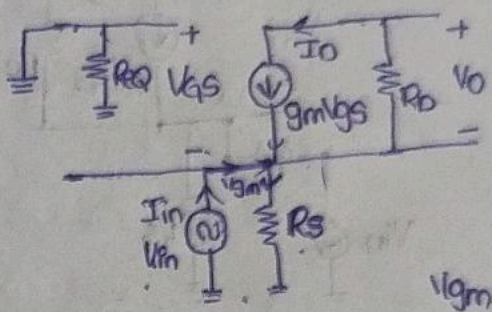
common Gate with Rs



ac Equivalent circuit



small signal model



1/gm ∥ RS

Input impedence:-

applying KCL

1) $-I_{in} + I_D + \frac{V_{in}}{R_S} = 0$

$\frac{V_{in}}{R_S} = I_{in} + I_D$

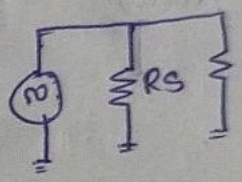
$\frac{V_{in}}{R_S} = I_{in} + g_m V_{GS}$

$\frac{V_{in}}{R_S} = I_{in} - g_m V_{in}$

$I_{in} = V_{in}\left[\frac{1}{R_S} + g_m\right]$

$\frac{V_{in}}{I_{in}} = \frac{1}{\frac{1}{R_S} + g_m}$

$\frac{V_{in}}{I_{in}} = \frac{R_S}{1+g_m R_S} = \frac{1}{g_m} \parallel R_S$

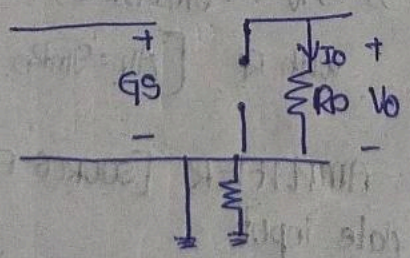


$\frac{I_{in}}{V_{in}} = \frac{1}{R_S} + \frac{1}{1/g_m}$

$\frac{V_{in}}{I_{in}} = \frac{1}{R_S} \parallel g_m$

$\frac{R_S}{1+g_m R_S}$

2) output impedence :



$Z_o = \frac{V_o}{I_o} = R_D$

3) voltage gain :

$A_V = \frac{V_o}{V_{in}} =$

$A_V = \frac{V_o}{V_{in}} = \frac{-g_m V_{GS} R_D}{-V_{GS}}$

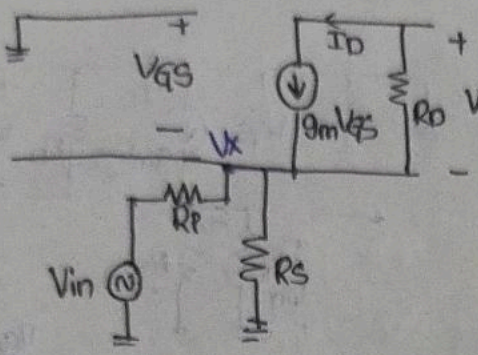
~~$V_o = -g_m V_{GS} R_D$~~

$\boxed{A_V = g_m R_D}$

~~$V_{in} = -V_{GS}$~~

~~$A_V = -g_m V_{GS} R_D$~~

if there is internal resistance b/w voltage & source

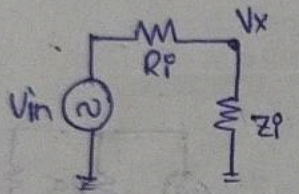


$Z_{out} = R_D$

$A_V = \frac{V_o}{V_{in}} \times \frac{V_x}{V_x}$

$= \frac{V_o}{V_x} \cdot \frac{V_x}{V_{in}}$

$\boxed{\frac{V_o}{V_x} = g_m R_D}$



$V_x = \frac{Z_{in}}{Z_{in} + R_f} V_{in}$

$\boxed{\frac{V_x}{V_{in}} = \frac{Z_{in}}{Z_{in} + R_f}}$

$A_V = g_m R_D \frac{Z_{in}}{Z_{in} + R_i}$ $\left[\because Z_{in} = \frac{1}{g_m} \| R_g\right]$

when $R_i = 0 \Rightarrow A_V = g_m R_D$.

$\boxed{A_V = g_m R_D \frac{\frac{1}{g_m} \| R_g}{\frac{1}{g_m} \| R_g + R_{in}}}$

case (ii) $\partial \neq 0$

1) $Z_{in} = \frac{1}{g_m} \| R_S$ ✓
2) $Z_{out} = R_D$ ✓
3) $A_V = g_m R_D$. ✓

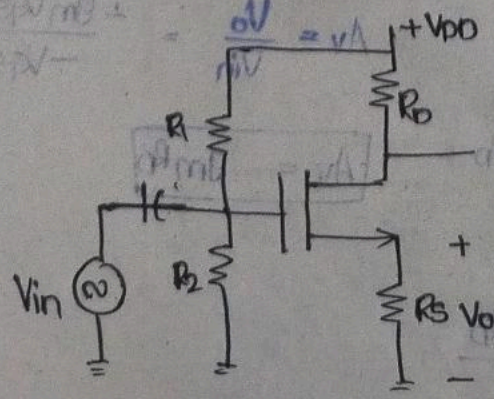
$\partial \neq 0$

1) $Z_{in} = \frac{1}{g_m} \| R_S$ ✓
2) $Z_{out} = R_D \| r_d$ ✓
3) $A_V = g_m (R_D \| r_d)$

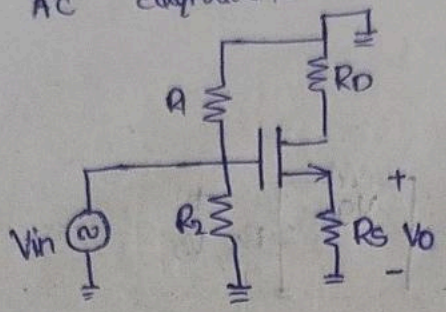
with R_f $\left[A_V = g_m R_D \frac{Z_{in}}{Z_{in} + R_i}\right]$

COMMON DRAIN AMPLIFIER [SOURCE FOLLOWER]

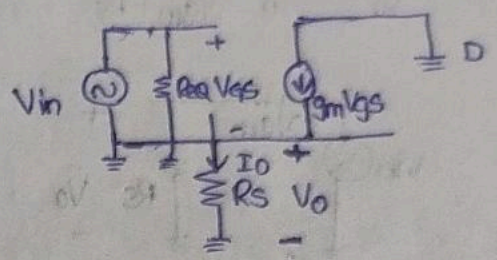
⇒ drain grounded while gate input source output



AC equivalent



Small signal



1) Input Impedence $\left(\frac{Vin}{Iin}\right)$ = ReQ = $R_1 \| R_2$

2) output ~~Ji~~ Voltage Gain (Av) = $\frac{V_o}{V_{in}}$

apply KVL for Input,

$$-V_{in} + V_{gs} + V_o = 0$$

$$V_{gs} = V_{in} - V_o$$

~~$V_{GS} = V_o - V_{in}$~~

apply KCL at RS,

$$V_o = I_D R_S$$

$$\frac{V_o}{R_S} = g_m V_{gs}$$

$$\frac{V_o}{R_S} = g_m (V_{in} - V_o) \Rightarrow \frac{V_o}{R_S} + g_m V_o = g_m V_{in}$$

$$\frac{V_o}{V_{in} g_m R_S} + \frac{V_o}{V_{in}} = 1$$

$$\frac{V_o}{V_{in}} \left[\frac{1}{g_m R_S} + 1\right] = 1$$

$$V_o/V_{in} = \frac{g_m R_S}{1 + g_m R_S}$$

$$A_V = \frac{V_o}{V_{in}} = \frac{g_m R_S}{1 + g_m R_S}$$

$\frac{R_S}{\frac{1}{g_m} + R_S}$

$1 + g_m R_S >> 1 \quad A_V << 1$

if $g_m R_S >>> 1 \quad A_V \approx 1 \quad V_o = V_{in}$

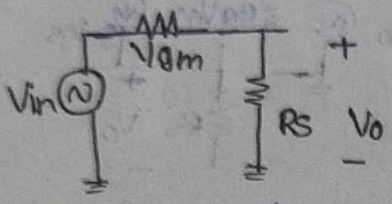
→ unity gain Amplifier

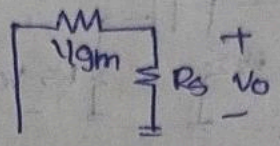
→ Buffer gain Amplifier

→ high to low impedence matching

output Impedence :

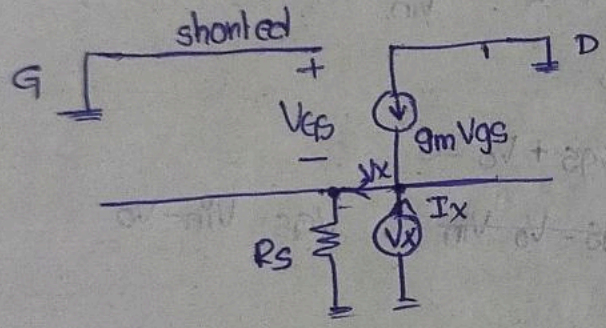
$$V_o = V_{in} \frac{R_S}{1/g_m + R_S}$$





$$Z_{out} = 1/g_m \parallel R_S$$

If test Voltage is given



$$\frac{V_x}{J_x} \qquad V_x = -V_{GS}$$

KCL

$$-I_x - I_D + \frac{V_x}{R_S} = 0$$

$$\frac{V_x}{R_S} = I_x + I_D$$

$$\frac{V_x}{R_S} = I_x + g_m V_{GS}$$

$$\frac{V_x}{R_S} + g_m V_x = I_x$$

$$\frac{I_x}{V_x} = \frac{1}{R_S} + g_m = \frac{1}{Z_{out}}$$

$$\boxed{Z_{out} = \frac{1}{\frac{1}{R_S} + g_m} \parallel R_S}$$

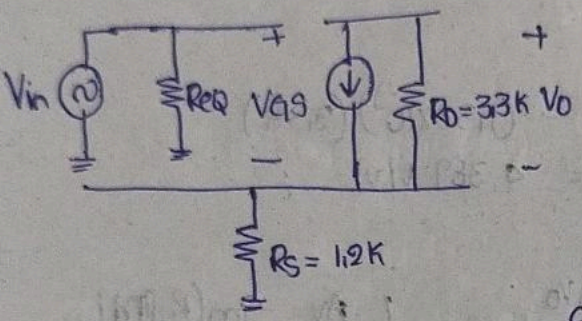
find Voltage Gain Rin Rout for common Amplifier

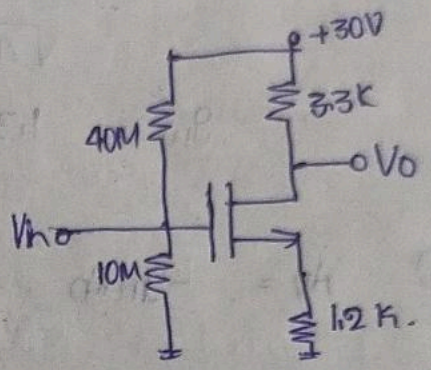
with $R_1 = 40M$ $R_2 = 10M$ $R_D = 3.3K$ $R_S = 1.2K$ $K_1 = 10K$

$V_{DD} = 30V$ $V_{th} = 3V$ $K = 0.4$ milli

① case i $= \lambda = 0$

ii $\Rightarrow \lambda \neq 0$





① $R_{in} = R_1 \| R_2 = \frac{40 \times 10 \times 10^6 \times 10^6}{50 \times 10^6} = \frac{400}{50}\ M\Omega = 8M\Omega$

② $R_{out} = R_D = 3.3K$

③ $A_V = -g_m R_D$

$g_m = \sqrt{2 I_D (2K_n)} = \sqrt{4 I_D K_n}$

$V_g = 30 \frac{10}{50} = 6V$

$V_{gs} = V_g - V_S = 6 - I_D(1.2K)$

$I_D = 0.4 \times 10^{-3} [6 - I_D(1.2K) - 3]^2$ 2x3

$I_D = 0.4 \times 10^{-3} [9 + I_D^2 (1.44 \times 10^6) - 6(1.2K) I_D]$

$I_D = 3.6 \times 10^{-6} + 0.576 \times 10^3 I_D^2 - 2.88 I_D$

0.5 $576 I_D^2 - 3.88 I_D + 3.6 \times 10^{-3} = 0$

$V_g - V_S$

$I_D = 5.62$ mA

$I_D = 1.11$ mA

$I_D = 5.62 \Rightarrow V_{DS} = 6 - (5.62)(1.2) = -0.75 << V_{th}$

$V_{DS} = 6 - (2.1)(1.2) = 4.6 >> V_{th}$

$\boxed{I_D = 1.11\ mA}$

$$g_m = \sqrt{4 \times 1.11 \times 10^{-3} \times 0.4 \times 10^{-3}}$$

$$= \sqrt{2 \times 1.11 \times 10^{-3} \times 2 \times 0.4 \times 10^{-3}}$$

$$= \sqrt{4 \times 1.11 \times 0.4} \text{ milli siemens}$$

$$g_m = 1.33 \text{ milli } \mho$$

① $A_V = -g_m R_D = -(1.33 \times 10^{-3})(3.3\text{K})$

$= 4.389$ V/V

② $R_{in} = 8\text{M}\Omega$

$R_{out} = R_D \| r_o$

$= 3.3\text{K} \| 10\text{K}$

$= \frac{33 \times 10^6}{13.3 \times 10^6}$

$= 24.81\ \text{K}\Omega$

$A_V = -g_m(R_D \| r_d)$

$= -1.33(24.81)$

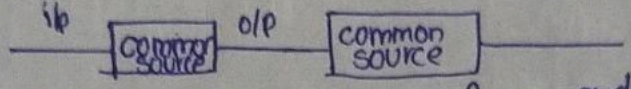
$= 32.99$ V/V

Multistage Amplifiers (or) Cascaded Amplifiers :-

* To increase voltage gain (A_v)
* Cascading - connecting common configuration with same configurations connecting same amplifiers step by step parallelely is cascading.

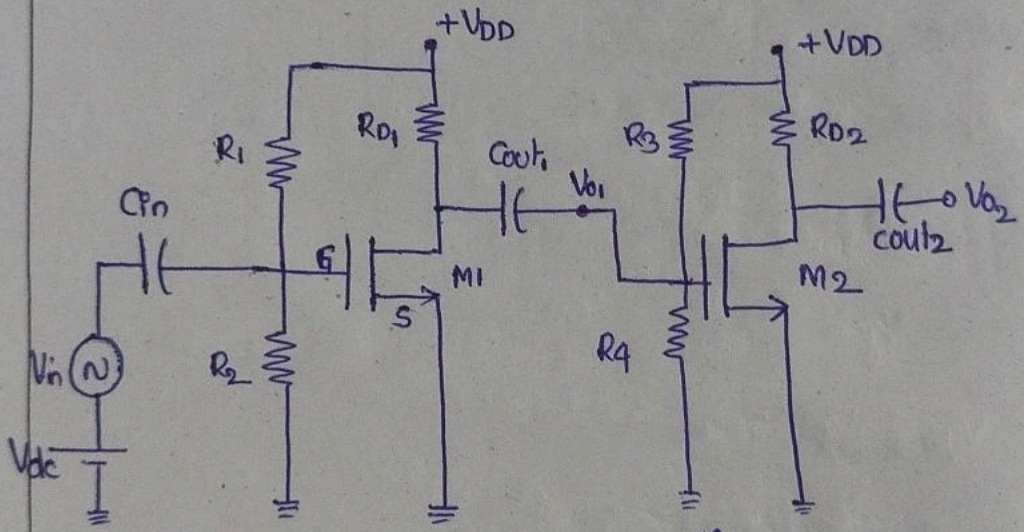
maximum no. of cascading stages = 7

output of common source is input of another Amplifier



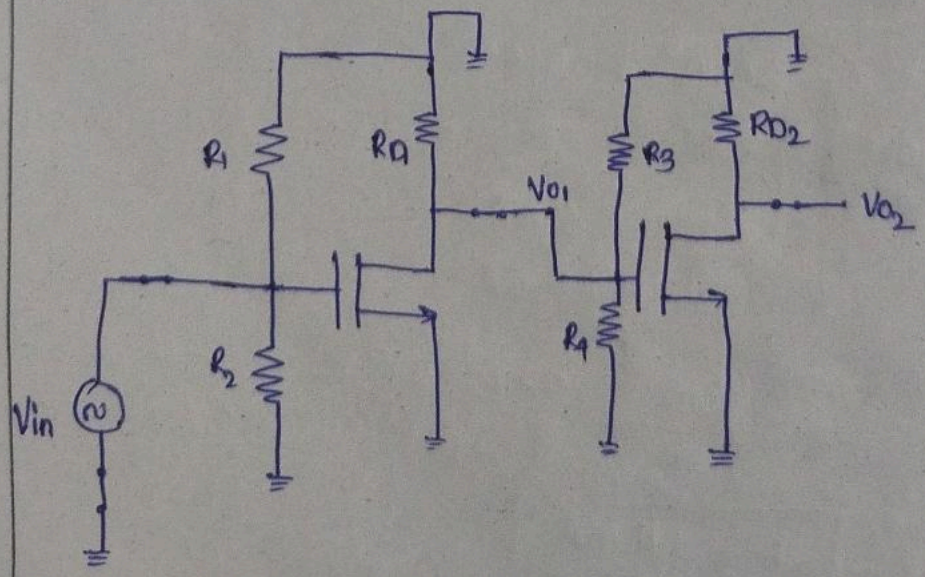
cascoding : connecting different amplifiers end to end

common source — common Gate -

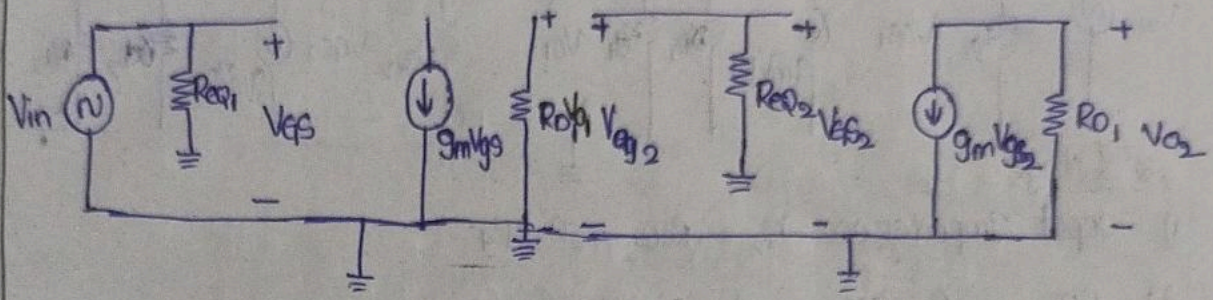


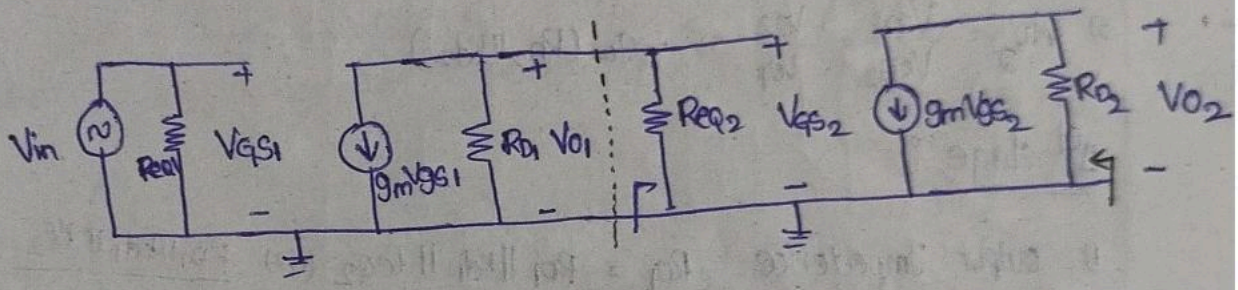
multi stage Amplifier.

AC EQUIVALENT CIRCUIT



Small signal model





2nd stage :-

1) output Impedence = $R_{O_2} = R_{D_2}$

2) $R_{i_2} = R_{EQ_2} = R_3 \| R_4 = \frac{R_3 R_4}{R_3 + R_4}$

3) $A_{V_2} = \frac{V_{o_2}}{V_{o_1}} = -g_m R_{D_2}$ $[\because V_{o_2} = -g_m V_{GS_2} R_{D_2}]$
$= -g_m R_{O_2}$ $[\because R_{O_2} = R_{D_2}]$

1st stage :-

1) $R_{O_1} =$

second stage input impedence can be acting as load for first stage

$\therefore R_{O_1} = R_{D_1} \| R_{i_2}$

2) $R_{i_1} = R_{EQ_1} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$

3) voltage gain (Av) = $\frac{V_{o1}}{V_{in}} = -g_m R_{O_1} = -g_m [R_{O_1} \| R_{i_2}]$

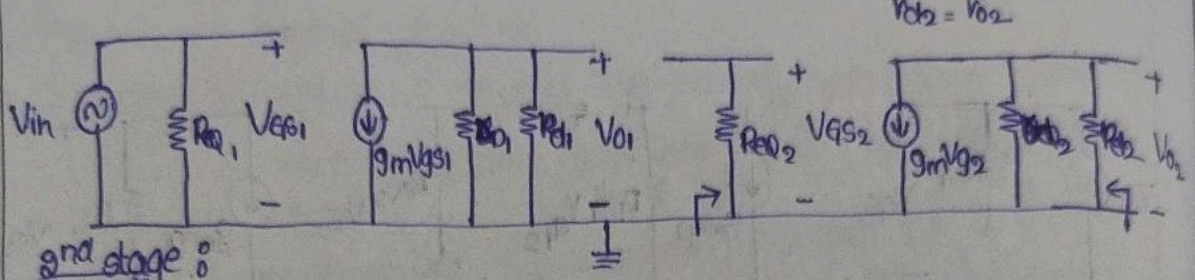
Overall Voltage Gain:

$A_{V_{overall}} = \frac{V_{o_2}}{V_{in}}$

$= \frac{V_{o_2}}{V_{in}} \times \frac{V_{o_1}}{V_{o_1}} = \frac{V_{o_2}}{V_{o_1}} \times \frac{V_{o_1}}{V_{in}} = A_{V_2} \cdot A_{V_1}$

case (??)

case (ii) : $\lambda \neq 0$



2nd stage :

1) Input Impedence = $R_{i_2} = R_{eq_2} = R_3 \| R_4$

2) $R_{O_2} = R_{D_2} \| r_{d_2}$ (or) $R_{D_2} \| r_{o_2}$

3) $A_{V_2} = \frac{V_{o_2}}{V_{GS_2}} = \frac{V_{o_2}}{V_{o_1}} = -g_m (R_{D_2} \| r_{d_2})$

1st stage :

1) output Impedence $R_{O_1} = R_{D_1} \| r_{d_1} \| R_{eq_2}$ (or) $R_{D_1} \| r_{d_1} \| R_{i_2}$

$= \frac{1}{R_{D_1}} + \frac{1}{r_{d_1}} + \frac{1}{R_{eq_2}}$

2) $R_{i_1} = R_{eq_1} = R_1 \| R_2$

3) $A_{V_1} = \frac{V_{o_1}}{V_{in}} = -g_m R_{O_1} = -g_m (R_{D_1} \| r_{d_1} \| R_{eq_2})$

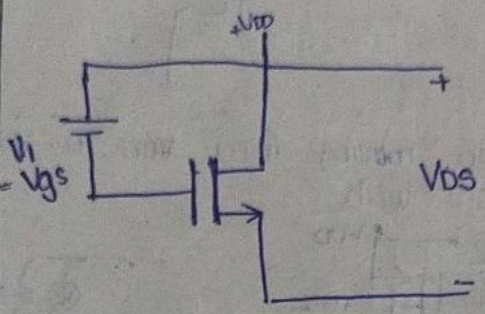
overall voltage Gain ($A_{V\text{overall}}$) $= \frac{V_{o_2}}{V_{in}}$

$= \frac{V_{o_2}}{V_{o_1}} \frac{V_{o_1}}{V_{in}}$

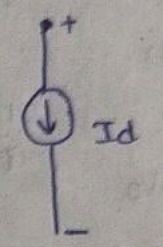
$= A_{V_2} \cdot A_{V_1}$

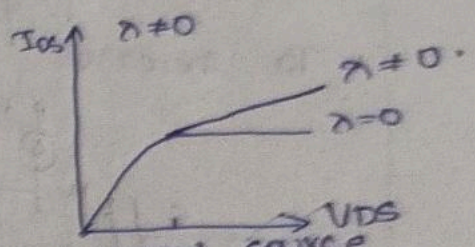
MOS CURRENT SOURCES :-

common source : • high voltage gain
• Negative feedback

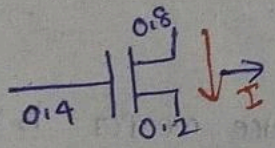


during AC analysis DC S.C

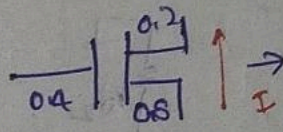




when $V_{DS} > V_{gs} - V_{th}$ MOSFET used as current source

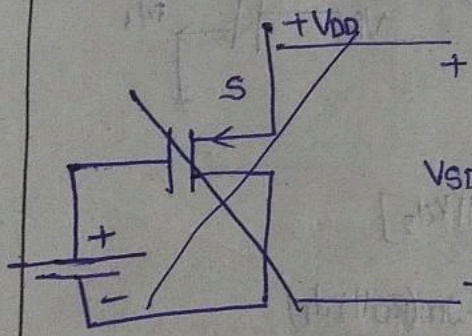


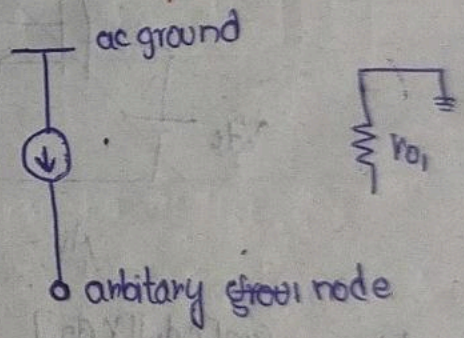
NMOS [∵ $V_D > V_S$]

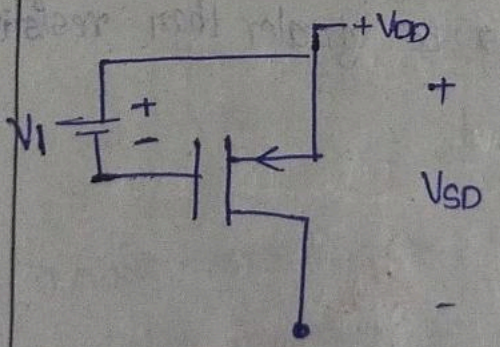


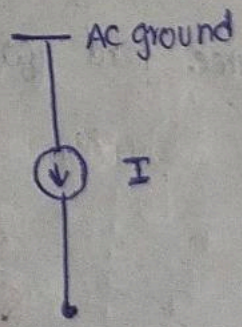
PMOS [$V_S > V_D$]

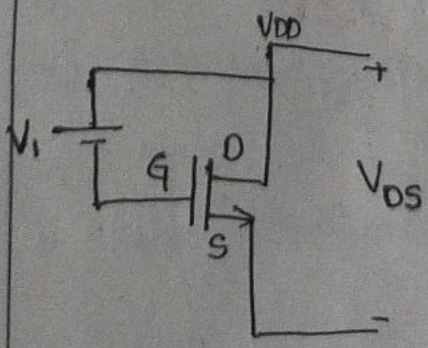
Current NMOS $V_D > V_S$
PMOS $V_S > V_D$



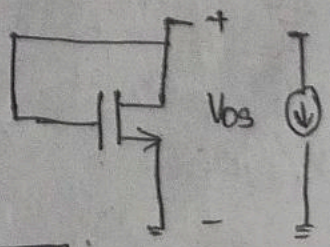




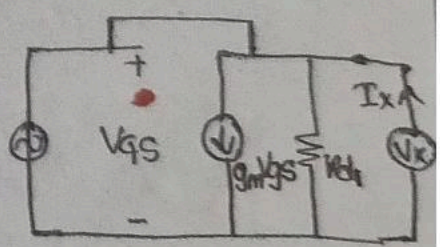


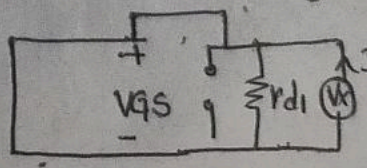


ac Equivalent



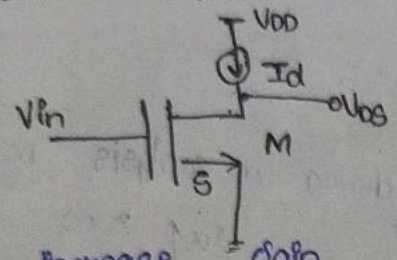
small signal

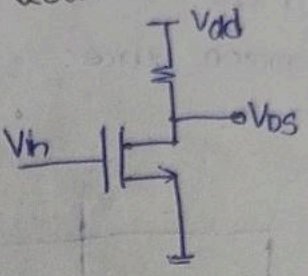




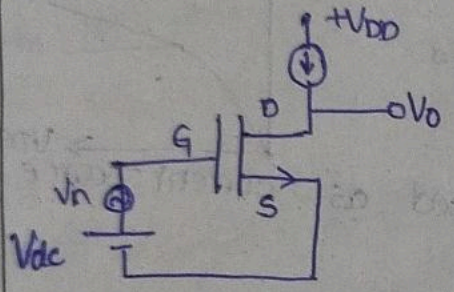
$\frac{V_x}{I_x} = r_{d1}$

Common source with current source load.

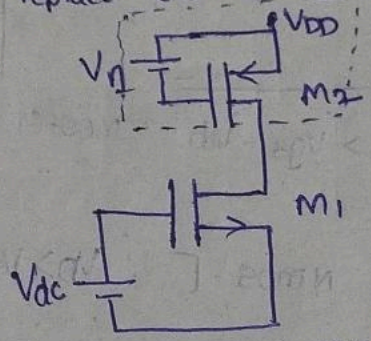


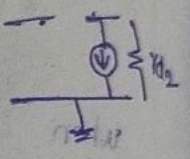


* To increase gain

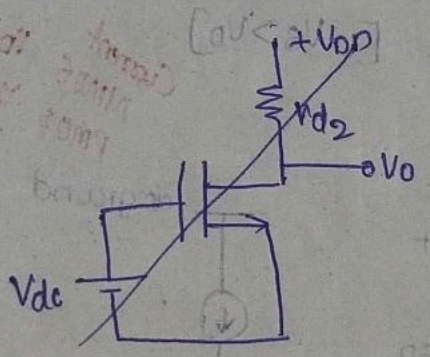


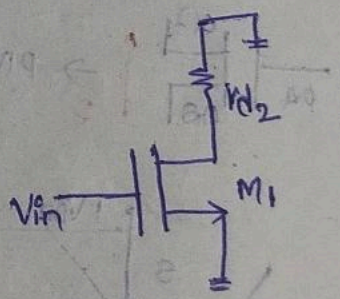
since Io moving from VDD to Node replace c.s with





using small signal analysis, current source mosfet is r_{d_2}

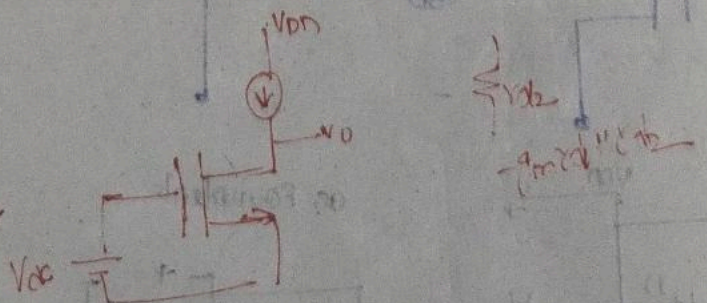




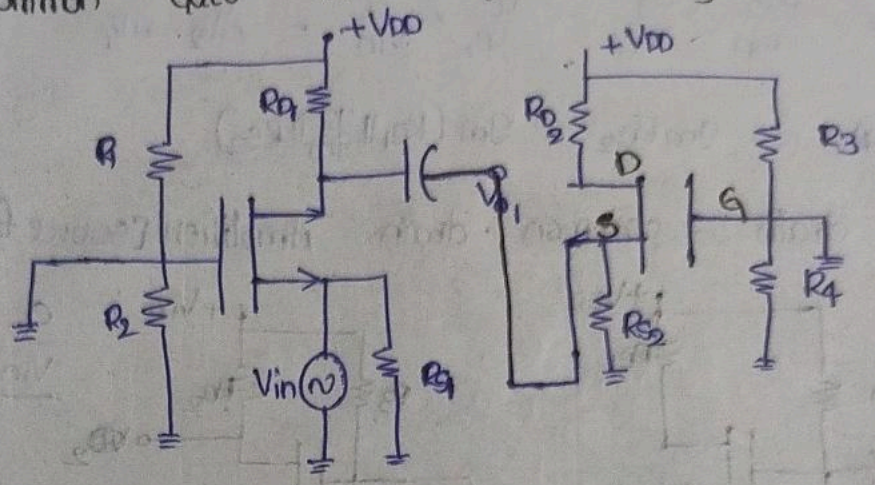
$$A_V = -g_m[r_{d_1} \| r_{d_2}]$$

* $A_V = -g_m[r_{d_1} \| r_{d_2}] > -g_m(R_o \| r_{d_1})$

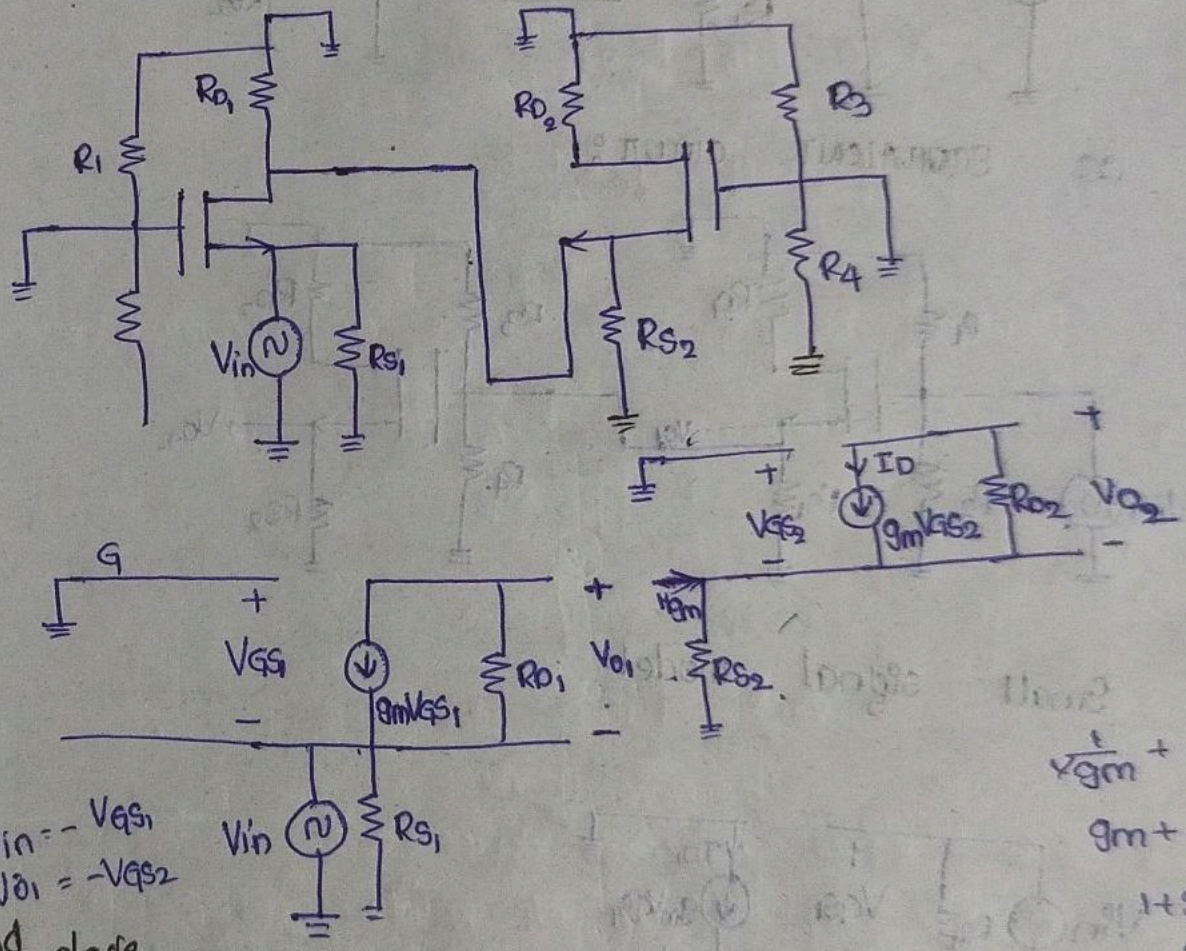
* current source load gain must be greater than resistive load gain.



Common Gate – common Gate Cascading



ac Equivalent circuit



$V_{in} = -V_{GS1}$

$V_{o1} = -V_{GS2}$

$\frac{1}{\frac{1}{g_m} + \frac{1}{R_{S2}}}$

$g_m + \frac{1}{R_{S2}}$

$1 + g_m \frac{R_{S2}}{g_m}$

2nd stage

1) output impedence = $R_{O2} = R_{D2}$

2) Input impedence = $R_{i2} = \frac{1}{g_m} \| R_{S2}$

3) outp voltage gain $(A_v) = \frac{V_{o2}}{V_{o1}} = g_m R_{D2}$ $\left[\frac{+g_m V_{GS2} R_{D2}}{+V_{GS2}}\right.$

1st stage :-

1) output impedence = $R_{o1} = R_{D1} \| R_{i2}$

$= R_{D1} \| \left(\frac{1}{g_m} \| R_{S2}\right)$

2) Input impedent = $R_{i1} = \frac{1}{g_m} \| R_{S1}$

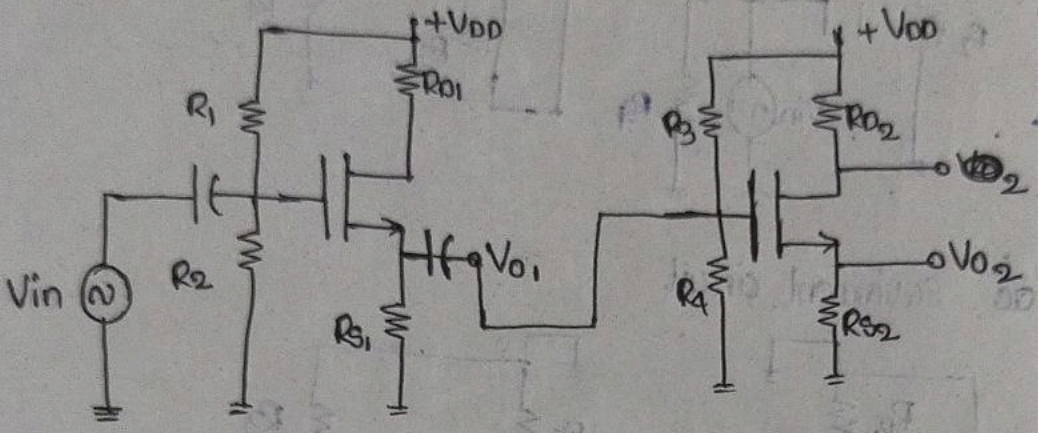
3) Voltage gain = $\frac{V_{o1}}{V_{in}} = g_m R_{o1} = g_m (R_{D1} \| R_{i2})$

$= g_m \left(R_{D1} \| \frac{1}{g_m} \| R_{S2}\right)$

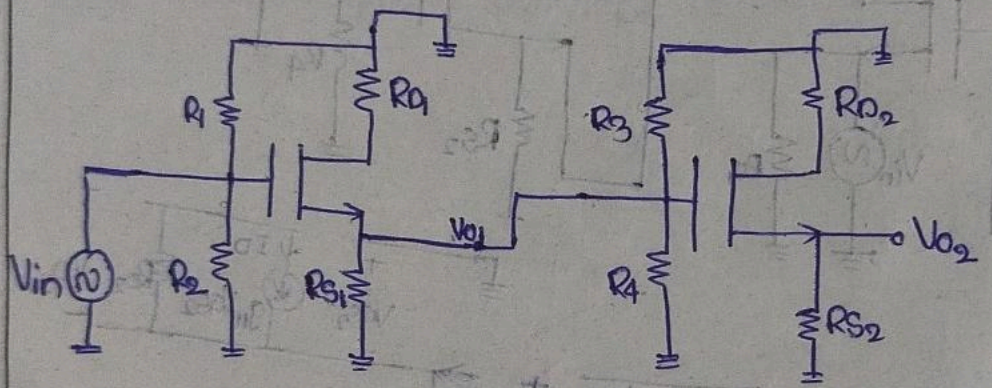
$$A_{V\,overall} = \frac{V_{o2}}{V_{in}} \times \frac{V_{o1}}{V_{o1}} = \frac{V_{o2}}{V_{o1}} \times \frac{V_{o1}}{V_{in}} = A_{V_2} \cdot A_{V_1}$$

$$A_V = g_m R_{D_2} \cdot g_m (R_{D_1} \| \frac{1}{g_m} \| R_{S_2})$$

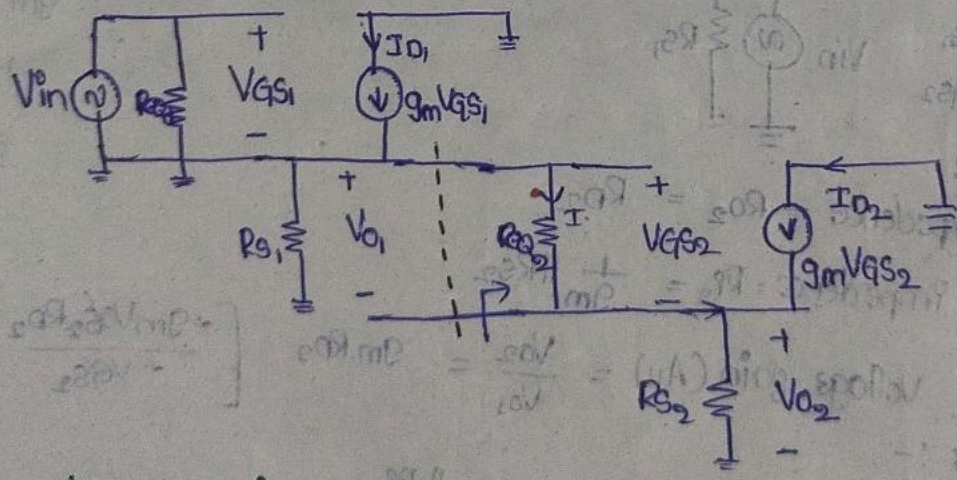
common drain - common drain Amplifier [source follow]



DC EQUIVALENT CIRCUIT:



Small signal model



2nd stage:

$R_{i_2} = R_{eq_2} = R_3 \| R_4$

$R_{o_2} = \frac{1}{g_m} \| R_{S_2}$

$[-V_{o_1} + V_{GS_2} + V_{o_2}$ $\quad \frac{V_{o_2}}{R_{S_2}} = g_m V_{GS_2}$

$V_{GS_2} = V_{o_1} - V_{o_2}$

$A_V = \frac{V_{o_2}}{V_{o_1}} = \frac{g_m R_{S_2}}{1 + g_m R_{S_2}}$

1st stage:

1) output Impedence = $R_{o_1} = \frac{1}{g_m} \| R_{S_1} \| R_{EQ_2}$

2) Input Impedence = $R_{i_1} = R_1 \| R_2$

3) Voltage gain = $A_{V_1} = \frac{V_{o_1}}{V_{in}} = \frac{g_m (R_{S_1} \| R_{EQ})}{1 + g_m (R_{S_1} \| R_{EQ})}$

$$-V_{in} + V_{GS_1} + V_{o_1} = 0$$

$$V_{GS_1} = V_{in} - V_{o_1}$$

$$\frac{V_o}{R_{S_1}} + \frac{V_o}{R_{EQ_2}} = g_m V_{GS_1}$$

$$V_o \left[R_{S_1} \| R_{EQ_2} \right] = g_m (V_{in} - V_{o_1})$$

$$V_o \left[R_{S_1} \| R_{EQ_2} \right] + g_m \right] = g_m V_{in}$$

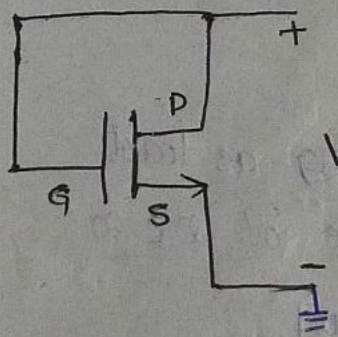
$$\frac{V_{o_1}}{V_{in}} \frac{R_{S_1} \| R_{EQ_2}}{g_m (R_{S_1} \| R_{EQ_2})} + \frac{V_o}{V_{in}} = 1$$

$$\frac{V_{o_1}}{V_{in}} = g_m \frac{1}{\frac{R_{S_1} \| R_{EQ_2}}{g_m} + 1} \left[\frac{1 + g_m (R_{S_1} \| R_{EQ_2})}{g_m (R_{S_1} \| R_{EQ})} \right] = 1$$

$$\frac{V_{o_1}}{V_{in}} = \left[\frac{g_m \, R_{S_1} \| R_{EQ_2}}{1 + g_m \, R_{S_1} \| R_{EQ_2}} \right]$$

$A_{V\,overall} = A_{V_2} \cdot A_{V_1}$

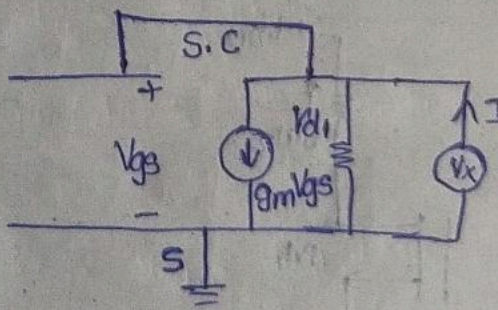
Diode Connected Devices.



⇒ When Gate and Drain are short circuit then it is called as Diode connected device.

⇒ Diode Connected Device can be formed by short circuiting the Gate and Drain terminals so that we observe same voltage at Gate and drain.

Small signal ⇒



since diode connected device $V_D = V_g = V_x$

* from circuit:

$$V_{gs} = V_x$$

* from circuit:

$$I_x = \frac{V_x}{r_d} + g_m V_{gs}$$

$$\frac{I_x}{V_x} = \frac{1}{r_d} + g_m$$

$$\frac{I_x}{V_x} = \frac{1}{R_o} = \frac{1 + g_m r_d}{r_d}$$

$$R_o = \frac{r_d}{1 + g_m r_d}$$

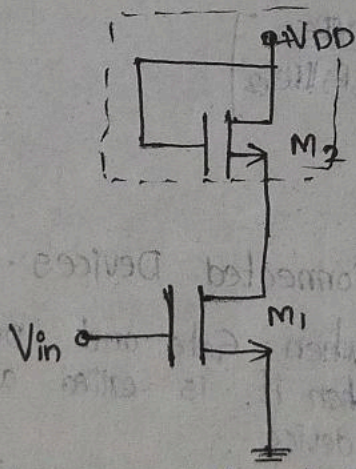
$$R_o = \frac{r_d}{\frac{1}{g_m} + r_d}$$

$$R_o = \frac{1}{1/r_d + g_m} = \frac{1}{\frac{1}{r_d} + \frac{1}{1/g_m}} = 1/g_m \| r_d$$

$\lambda \neq 0$ $\boxed{R_o = \frac{1}{g_m} \| r_d}$

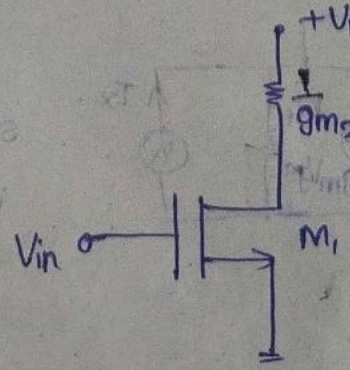
if $\lambda = 0$ $\boxed{R_o = \frac{1}{g_m}}$

Common source with diode connected load [Devices]

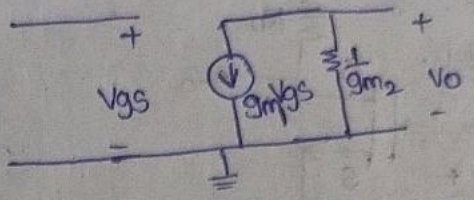


* since diode connected device acting as load it can be replaced by o/p resistance of 2 terminal device.

$\therefore R_o \; 1/g_{m_2}$ [$\lambda \neq 0$]



$A_V = \frac{-g_{m1}}{g_{m2}}$



$A_V = -g_{m_1} R_d$

$A_V = -g_{m_1} \frac{1}{g_{m_2}}$

$A_V = \frac{V_o}{V_{in}}$ $\quad \frac{V_o I_d}{I_d R_d}$

$= \frac{-g_{m_1} V_{gs} \frac{1}{g_{m_2}}}{+V_{gs}}$

$= g_{m_1}/g_{m_2} \quad -g_{m_1}\frac{1}{g_{m_2}}$

Diode $\frac{1}{g_m} \| r_d$.

$$\boxed{A_V = \frac{-g_{m_1}}{g_{m_2}}}$$

for we know that

$g_{m_1} = \sqrt{2 I_{D_1} \mu_n C_{ox} (W/L)_1}$

$g_{m_2} = \sqrt{2 I_{D_2} \mu_n C_{ox} (W/L)_2}$

Here $\boxed{I_{D_1} = I_{D_2}}$

$A_V = -\frac{\sqrt{2 I_D \cdot \mu_n C_{ox} (W/L)_1}}{\sqrt{2 I_D \mu_n C_{ox} (W/L)_2}}$

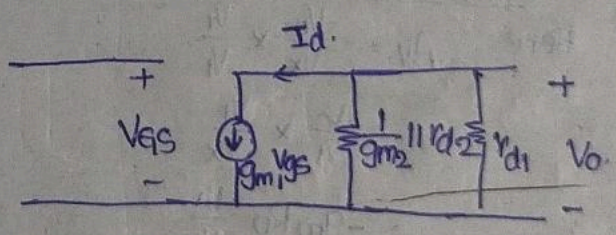
$\sqrt{\frac{(W/L)_1}{(W/L)_2}}$

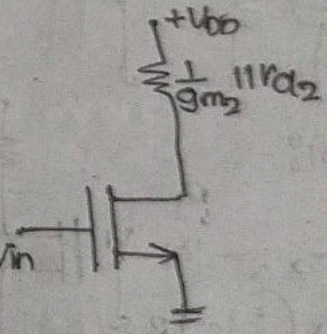
$$\boxed{A_V = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}}$$

* Above equation represents more "stable voltage gain Equation"

case (ii) $\lambda \neq 0$

$R_o = \frac{1}{g_{m_2}} \| r_{d_2}$





$A_V = \frac{V_o}{V_{in}} = \frac{-I_o R_o}{V_{in}} = \frac{-g_{m_1} V_{gs} \frac{1}{g_{m_2}} \| r_{d_2} \| r_{d_1}}{V_{gs}}$

$R_o = \frac{1}{g_{m_2}} \| r_{d_2} \| r_{d_1}$

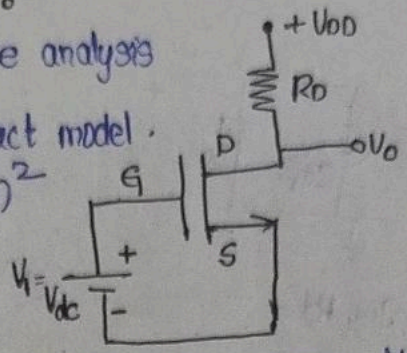
Voltage gain = $\boxed{A_V = -g_{m_1} \left[\frac{1}{g_{m_2}} \| r_{d_2} \| r_{d_1}\right]}$

I/O Impedences :-

ac analysis ⇒ Approximate analysis

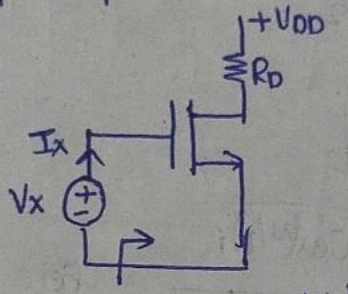
large signal model → Exact model.

$I_D = K(V_{gs} - V_{th})^2$



* To find out input impendence, replace Vdc with test voltage V_x

case(i)



$\frac{V_o}{V_{in}}$

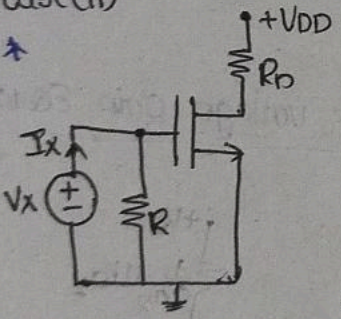
$-g_m R_D$

Here $I_x = 0$ due to high gate "Z" Internally

Ideally $R_{in} = \infty$ $\because I_{gs} = 0$

$$R_{in} = \frac{V_x}{I_x} = \infty$$ at lower frequency

case(ii)

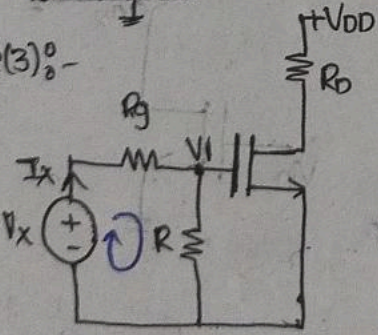


Input Impedence.

$$R_{in} = \frac{V_x}{I_{gs}} = R \| \infty = R$$

$-g_m R_D \frac{R}{R+R_g}$

case(3) :-



$R_{in} = R$

Here $A_V = \frac{V_o}{V_x} \times \frac{V_1}{V_1}$

$= \frac{V_o}{V_1} \times \frac{V_1}{V_x}$

$= -g_m R_D \frac{V_1}{V_x}$

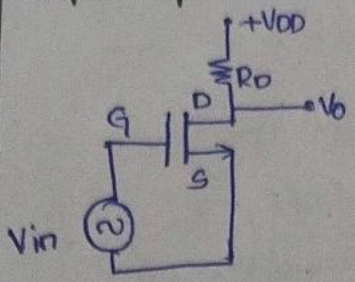
apply KVL voltage divider rule

$$V_1 = \frac{R}{R+R_g} V_{gs}$$

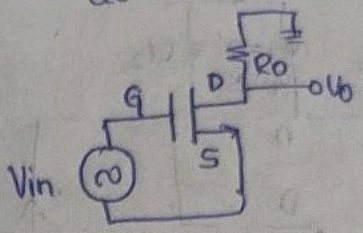
$$\frac{V_1}{V_x} = \frac{R}{R+R_g}$$

$$A_V = -g_m R_D \frac{R}{R+R_g}$$

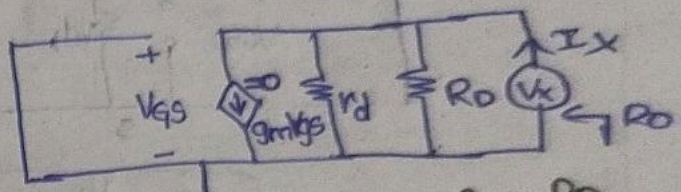
output impedence :



ac Equivalent

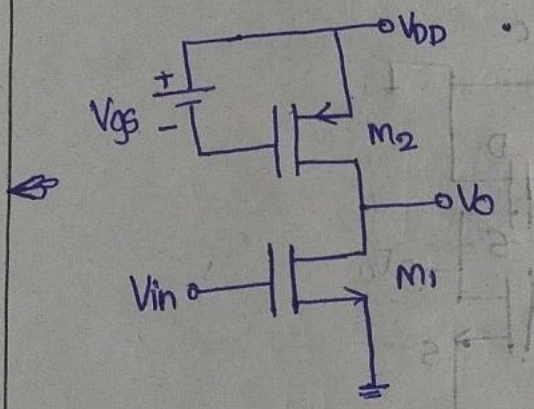


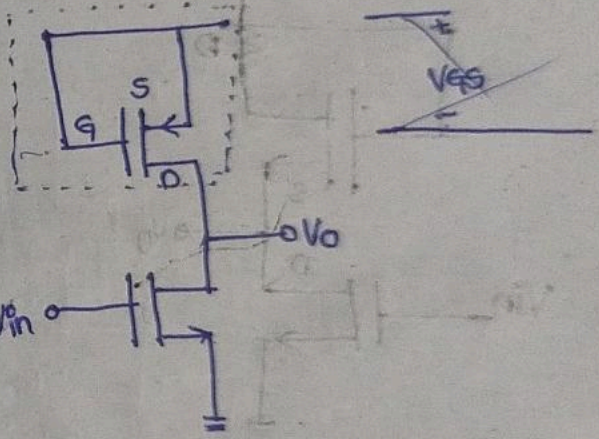
small signal analysis:
of output impendence

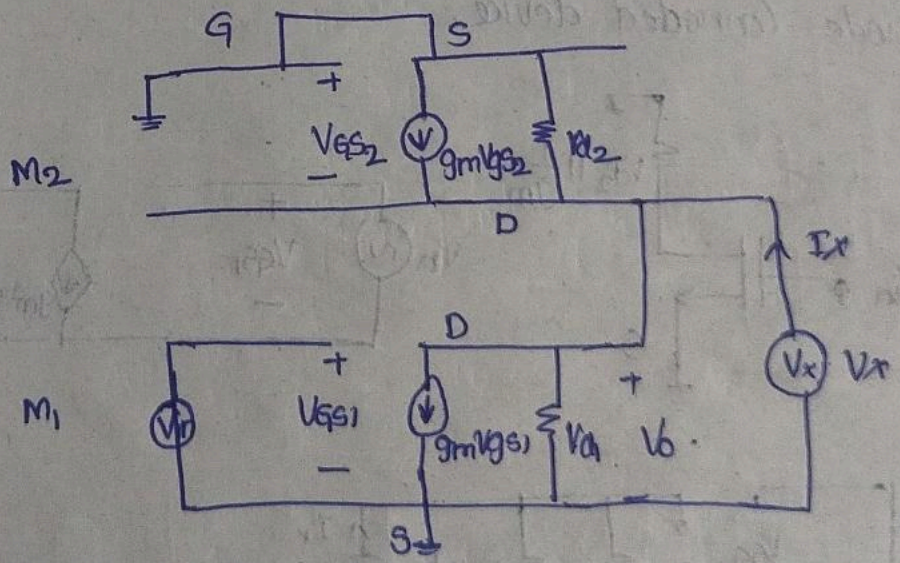


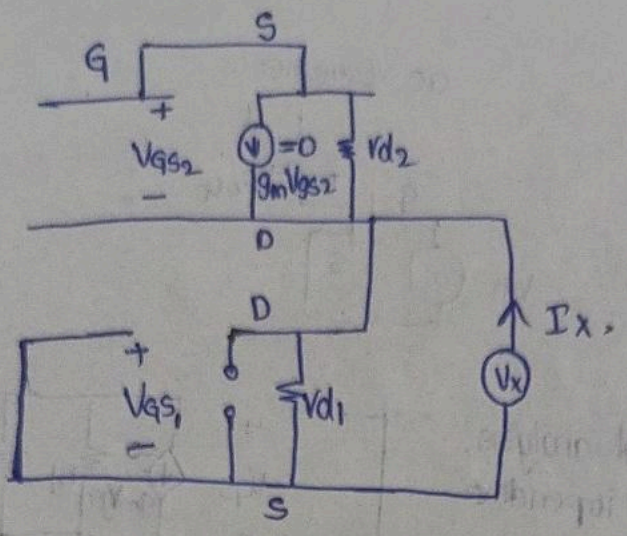
$R_o = R_D \| r_d$ → output impedence. $\lambda = 0$ $R_o = R_D$

OUTPUT Impedence for Current Source As Load.



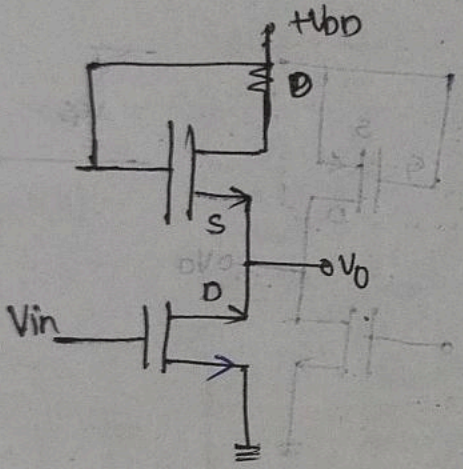


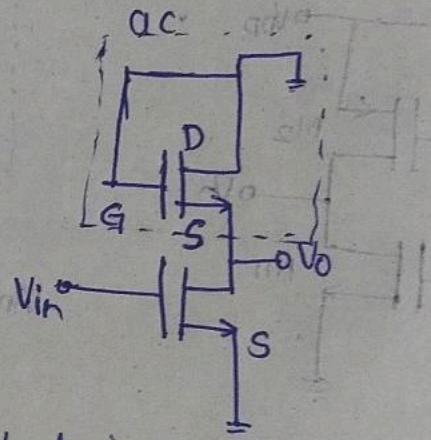




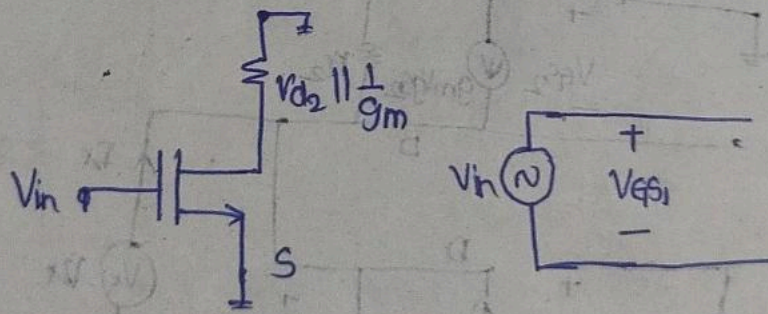
$$R_O = \frac{V_x}{I_x} = r_{d_1} \| r_{d_2}$$

output Impedence of diode Connected device.

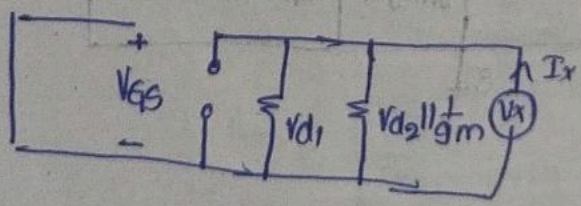




diode Conneded device,



*



$$R_O = \frac{1}{g_m} \| r_{d_1} \| r_{d_2}$$

when $\lambda \neq 0$ $\quad R_O = \frac{1}{g_m}$

→ degradation of gain → degeneration

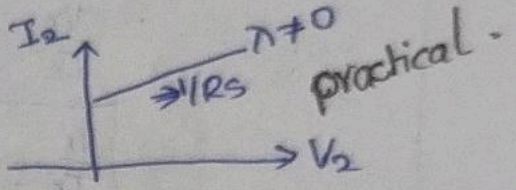
$R_S \uparrow \Rightarrow A_V \downarrow$

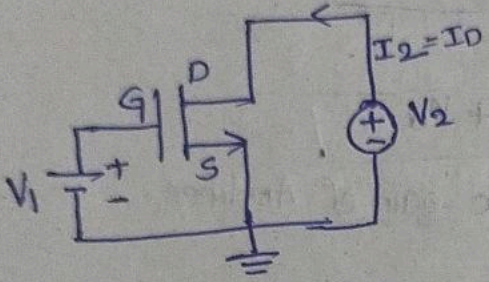
I/O Impedence with Source Resistance (or) Current Source combination

* Impedence of Ideal Voltage & Current Resistance

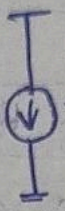
NMOS [Node - gnd]

PMOS [Vdd - Node]



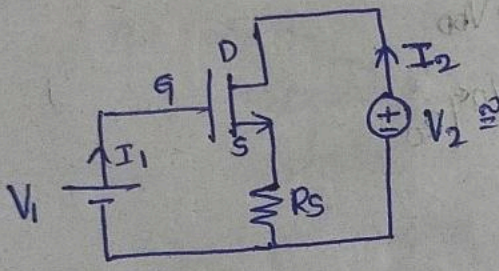


$\cong$

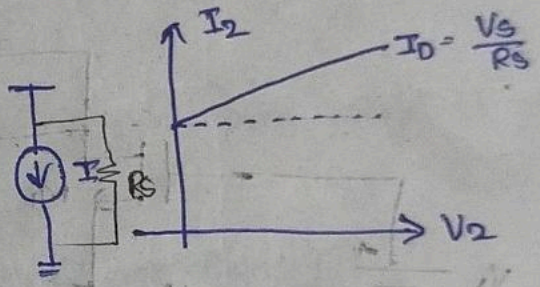


Ideal

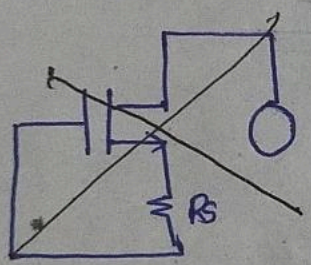
* with Source resistance



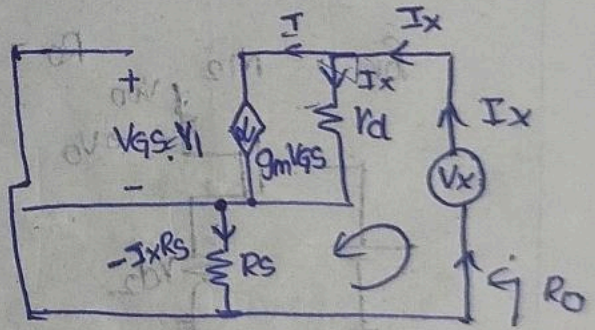
$\cong$



* Small signal Analysis ($\lambda \neq 0$)



$I_x = \frac{V_x}{r_d} + g_m V_{GS}$



$R_O = \frac{V_x}{I_x} =$

$V_{GS} = -I_x R_S$

$- g_m V_{GS} R_S$

$I_x =$

$I_L = g_m (I_x R_S)$ $\quad \therefore I_x + I_L = 0$

$I_O = I_x$

$R_O = I_x + I_x g_m R_S$

$$-V_x + r_d [I_x + I_x g_m R_S] + I_x R_S = 0$$

$$V_x = (r_d + R_S) I_x +$$

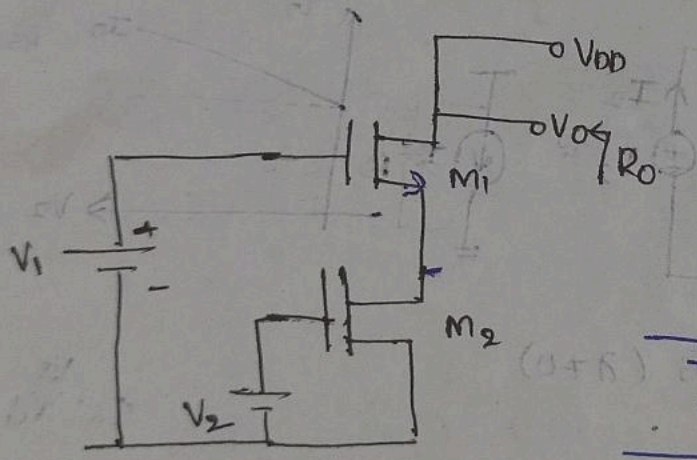
$$V_x = I_x (r_d + R_S + g_m R_S r_d)$$

$$\frac{V_x}{I_x} = R_S + r_d + g_m R_S r_d$$

$$\boxed{\frac{V_x}{I_x} = (1 + g_m r_d) R_S + r_d}$$

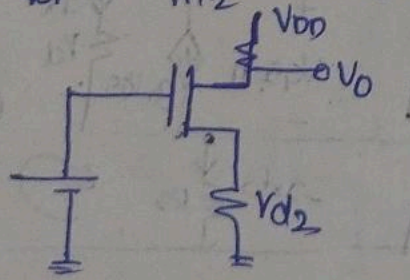
$$\boxed{R_o = R_S (1 + g_m r_d) + r_d}$$

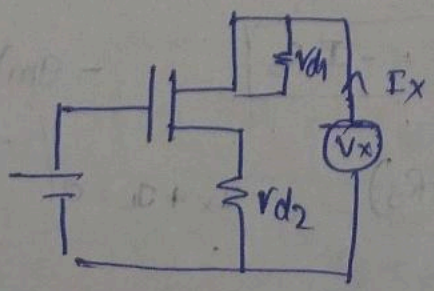
$g_m r_d \rightarrow$ intrinsic gain of Amplifier.

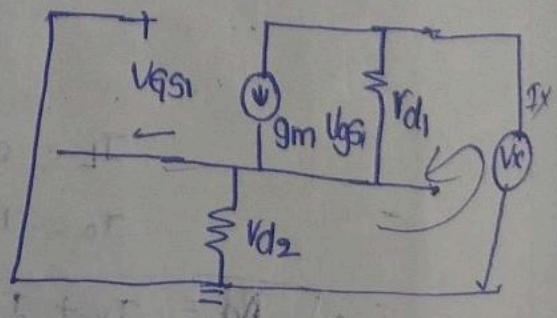


$$+ \frac{1}{V_2}$$

for M_2 $\quad R_o = r_{d_2}$







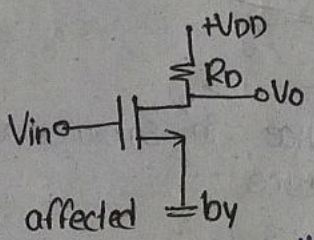
$$-V_x + r_{d1}(I_x + I_x g_m R_S r_{d2}) + I_x r_{d2} - 0$$

$$V_x = I_x (r_{d1} + r_{d2} + g_m r_{d2} r_{d1})$$

$$R_o = \frac{V_x}{I_x} = r_{d2}(1 + g_m r_{d1}) + r_{d1}$$

$$\boxed{R_o = r_{d2}(1 + g_m r_{d1}) + r_{d1}}$$

GAIN VARIATIONS of common source stage.



$$A_V = -g_m R_D$$

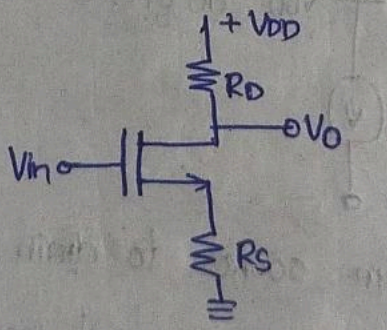
$$G_m = \sqrt{2 I_{Dmax} \mu_n C_{ox} W/L}$$

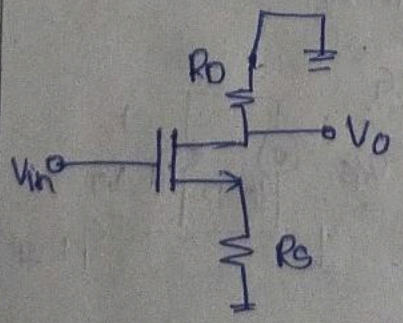
Gain is affected by

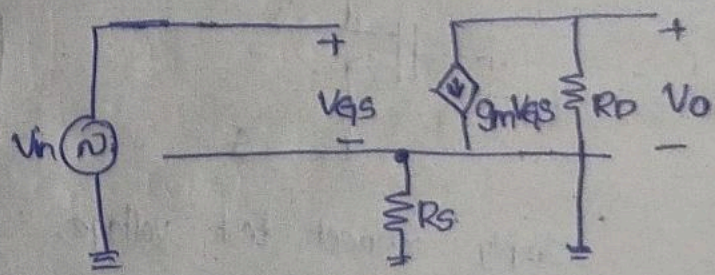
1. supply voltage
2. Process [transferring gain from 1stage to other]
3. Temperature
4. Signal Variation. [Small/large signal]

Gain is affected by R_S, g_m.

*







$$A_V = \frac{V_o}{V_{in}}$$

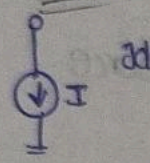
$$A_V = \frac{-g_m R_D}{1 + g_m R_S}$$

$$A_V = \frac{-R_D}{\frac{1}{g_m} + R_S}$$

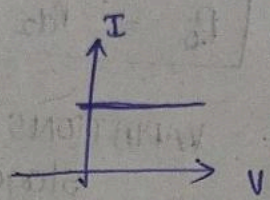
$$\frac{1}{g_m} << R_S$$

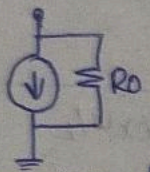
$$\boxed{A_V = \frac{-R_D}{R_S}}$$

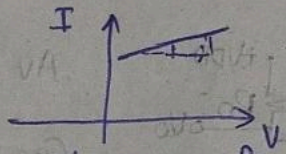
MOS Current Sources:-



Ideal current source



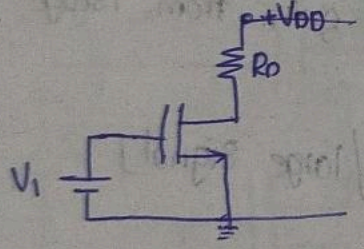


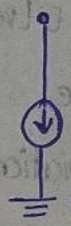


* CMOSFET can be used as current source in saturation region

Let's build an amp MOS current source

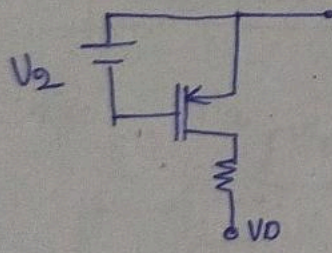
Consider N MOS

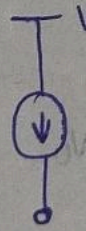




arbitary ground

In Nmos, current travels from Node to ground

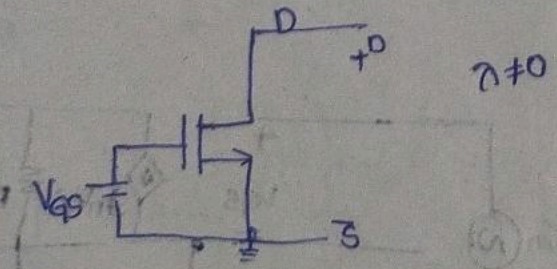




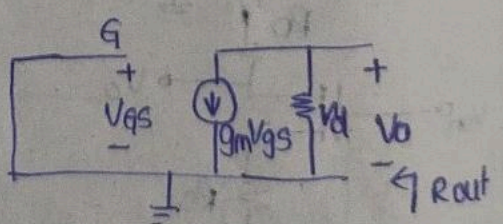
VDD ac ground

In Pmos, current travels from source to drain.

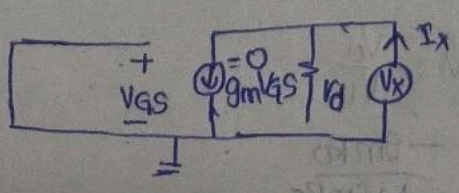
small signal model



$\lambda \neq 0$



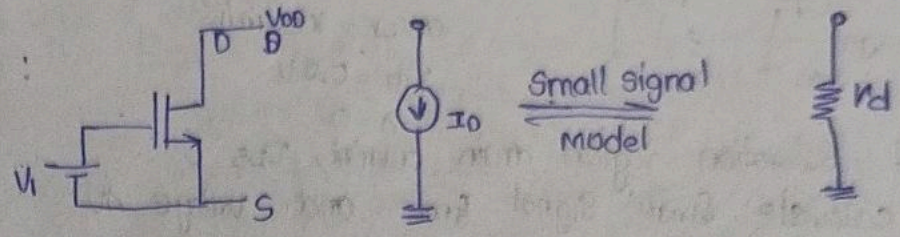
simply connect test voltage,



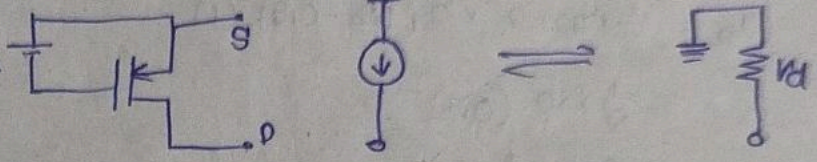
$$\frac{V_x}{I_x} = r_d.$$

when mosfet used as current source as load, simply replace it with small signal model of current source i.e r_d.

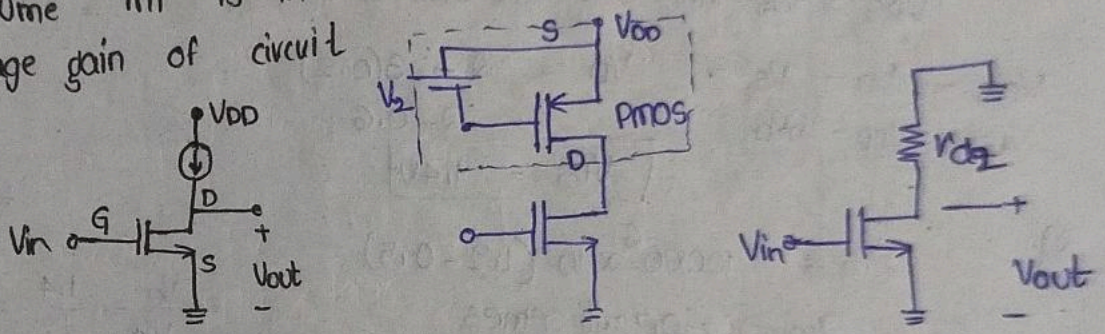
NMOS :



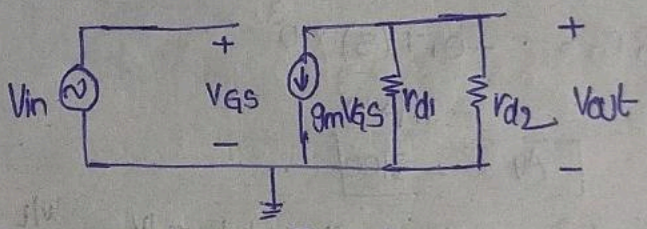
PMOS : V_2



Assume m1 is in biased in saturation, calcubte small signal voltage gain of circuit



$\lambda \neq 0$



$Z_{out} = r_{d_1} \| r_{d_2}$ $[\lambda \neq 0]$

$Z_{out} = r_{d_2}$ $[\lambda = 0]$ impedence of current source.

$$A_V = \frac{V_o}{V_{in}}$$

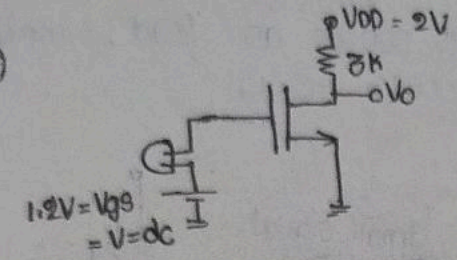
$$V_o = -g_m V_{gs} [r_{d_1} \| r_{d_2}]$$

$$\boxed{A_V = -g_m [r_{d_1} \| r_{d_2}]}$$

When $\lambda = 0$ $A_V = -g_m r_{d_2}$ called Intrinsic gain (maximum Av acheved by mosfet)

Note : If Vin changes, Vout changes to keep I_o constant

(1)



$W/L = 10$

$\mu_n C_{ox} = 100\mu A/V^2$

$V_{th} = 0.5V$

$\lambda = 0$

(1) find Saturation region drain current, V_{DS}

(2) calculate Small Signal g_m and Voltage Av

A) $I_D = \frac{1}{2} \times 100 \times 10^{-3} \times 10 (1.2 - 0.5)^2$ (1)

$= \frac{1}{2} \times 10^{-3} (0.7)^2$

$I_D = 0.245\ mA$

$V_{DS} \geq V_{gs} - V_{th} = 1.2 - 0.5 \geq 0.7V$

$V_{DS} = V_D - V_S = V_D = 2 - 3(0.2)$

$V_{DS} = V_{DD} - I_D R_D = 2 - 0.6.$

$\boxed{V_{DS} = 1.4V}$

2) $g_m = 100 \times 10^{-6} \times 10 (1.2 - 0.5)$

$g_m =$ 0.7 milli siemes

$\frac{V_o}{V_{in}} = \frac{1.4}{1.2} = \frac{14}{12}$ $\frac{7}{6}$

3) $A_V = -g_m R_D = -0.7 (3) \times 10^3$

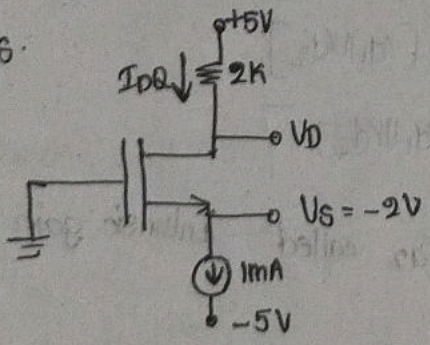
$= -2.1 \times 10^3$

$\boxed{A_V = -2100}$

2) $\mu_n C_{ox} = 1mA/V^2$ $V_{GSQ} = 2V$ $V_{th} = 1V$ $W/L = 10$ $g_m = ?$

A) $g_m = 10^{-3} \times 10 (2 - 1) =$ 10 milli siemes

3) $V_{th} = 1V$ $V_{DD} = 5V$ $R_D = 2K\Omega$ find V_{DS} (or) V_D ii) g_m iii) overdrive voltage and V_{gs}.



$V_{DS} = V_D - V_S$

$= 5 - 2(1mA) + 2$

$V_{DS} = 3 + 2 = 5V$ (1)

$V_D = 3V$

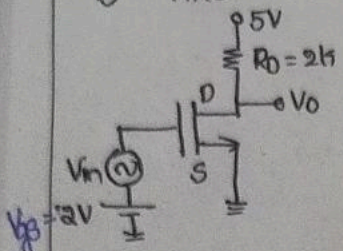
$g_m = \frac{2 I_{Dmax}}{V_{gs} - V_{th}} = \frac{2 \times 10^{-3}}{2 - 1}$

$= 2$ millisiemes

$V_{gs} = 2V$

$V_{DS} = V_{gs} - V_{th} = 2 - 1 =$ (1V)

4) Find Av of amplifier $\mu_n C_{ox} = 1mA/V^2$ $V_{th} = 1V$ $W/L = 2$



since it is common source

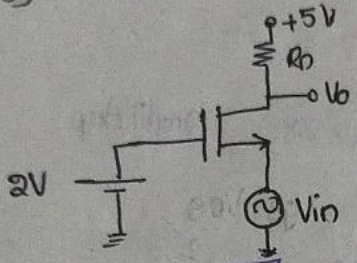
$A_V = -g_m R_D$

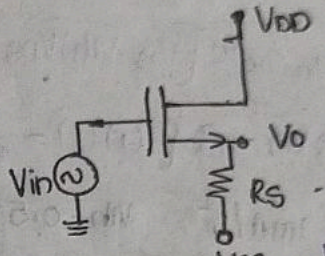
$g_m = 10^{-3} \times 2(2-1) = 2$ millisiemes

$A_V = -2\times10^{-3} \, 2\times10^{3}$

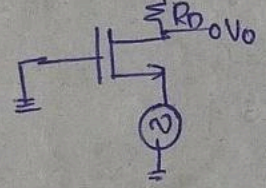
$= -4$ V/V

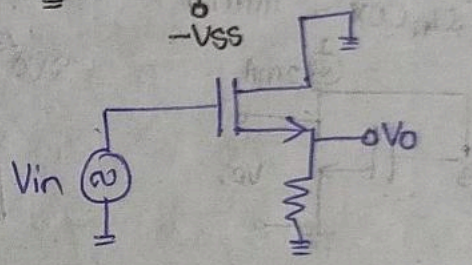
5) Find small signal voltage gain following circuit.

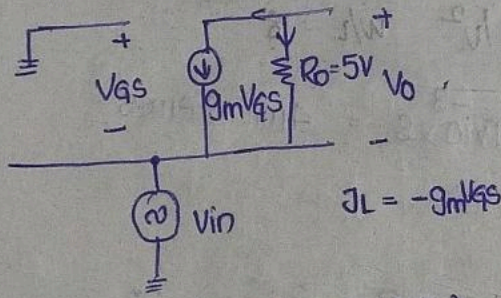




1A)





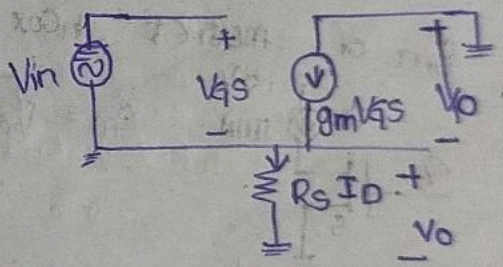


$J_L = -g_m V_{GS}$

$A_V = \frac{V_o}{V_{in}} = \frac{-g_m V_{GS}(R_D)}{-V_{GS}}$

$A_V = g_m R_D$

$\boxed{A_V = g_m R_D}$



$\frac{V_o}{R_S} = g_m V_{GS}$

$-V_{in} + V_{GS} + V_o = 0$

$V_{GS} = V_{in} - V_o$

$\frac{V_o}{R_S} = g_m (V_{in} - V_o)$

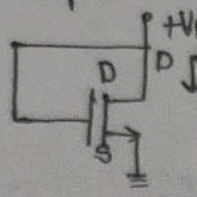
$\frac{V_o}{R_S} + g_m V_o = g_m V_{in}$

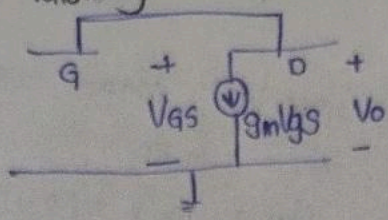
$A_V \left[\frac{1}{g_m R_S} + 1\right] = 0$

$\boxed{A_V = \frac{g_m R_S}{1 + g_m R_S}}$

$A_V = \frac{1}{g_m} \| R_S$

Find input resistance for following



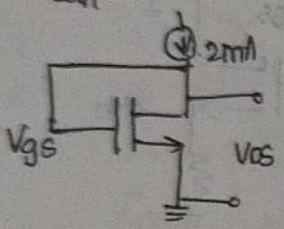


7) Given in NMOS, $\mu_n C_{ox} = 2mA/V^2$ $W/L = 2$ $V_{gs} = 2$ $V_{th} = 1V$ V_{DS} find I_D?

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{gs}-V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$= 2\times10^{-3} \times 2\left[(1)(1) - \frac{1}{2}\right] = 2\times10^{-3}\times 2\times\frac{1}{2} = 2 \text{ milli Amp}$$

8) $\mu_n C_{ox} = 1mA/V^2$ $V_{th} = 0.5$ $W/L = 2$ V_{gs} V_{DS}

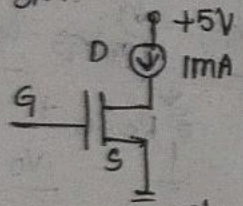


$$2\times10^{-3} = \frac{1}{2}\times10^{-3}\times 2\,(V_{gs}-0.5)^2$$

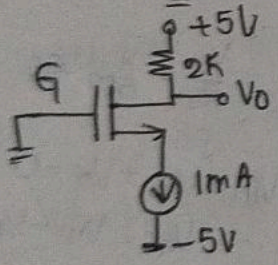
$$\sqrt{2}+0.5 = V_{gs}$$

$$\boxed{V_{gs} = 1.9} = V_{DS}.$$

9) g_m of MOSFET $\mu_n C_{ox} = 1mA/V^2$ $W/L = 8$



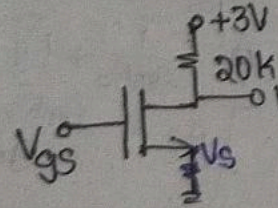
$$g_m = \sqrt{2\times10^{-3}\times 1\times10^{-3}\times 8} = 4 \text{ milli siemes}$$



$V_{th} = 1V$

$$g_m = \sqrt{2\times10^{-3}\times 1\times10^{-3}\times 8} = 4 \text{ milli } \mho$$

10) for given MOSFET $\mu_n C_{ox} = 100\,\mu A/V^2$ $W/L = 10$. MOSFET is at edge of saturation when $V_{gs} = 1V$ find V_{th} of MOSFET



$V_{DS} = V_{gs} - V_{th}$

$V_{th} = V_{gs} - V_{DS}$ $1-3+20K\,I_D$

$V_{DS} = 3 - 20K(I_D)$

$V_{gs} = V_g - V_s$

$V_{gs} = -V_s$

$$I_D = \frac{1}{2}\times10^{-3}(1-V_{th})^2$$

$$-V_{DD} + I_D R_D + V_S = 0$$

$$V_{DS} = V_{DD} - I_D R_D + V_{gs}$$

$$2I_D = 10^{-3}(20K\,I_D - 2)^2$$

$$2I_D = 10^{-3}(400\times10^{6} I_D^2 - 80K\,I_D + 4)$$

$$I_D = K_n(V_{GS} - V_{DD} + I_D R_D - V_{th})$$

$$2I_D = 400\times10^{-3} I_D^2 - 80 I_D + 4\times10^{-3}$$

$2I_D = 0.4 I_D^2 - 80 I_D + 0.04$

$0.4 I_D^2 - 82 I_D + 0.04 = 0$

$I_D = 204.99$

$I_D = 4.8 \times 10^{-4}$

$V_{GS} = \sqrt{\frac{2 I_{Dmax}}{\mu_n C_{ox} W/L}} + V_{th}$

$\frac{2 \times 4.8 \times 10^{-4}}{100 \times 10^{-6} \times 10}$ $2 \times 4.8 \times 10^{1}$

$V_{DS} = 3 - 20 \times 10^{-3}$

$= -6.6$ $V_{th} = \sqrt{\frac{2 I_{Dmax}}{\mu_n C_{ox} W/L}} - V_{GS}$

$0.2 \times 10^{-3} =$

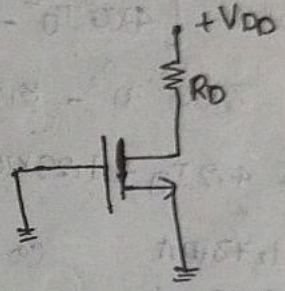
$V_{th} = 0.04$

$V_{th} = 1 + 6.6$

$V_{th} = 7.6V$

7) Design common source Amplifier with following $I_D = 1mA$

$V_{DD} = 5V$ $g_m = 1.8\,\mho$ $A_V = 3.8$ $r_o = 25\Omega$



$A_V = -g_m \frac{R_D r_o}{R_D + r_o}$

$-) \frac{3.8}{1.8} = \frac{25 R_D}{25 + R_D}$

$2.1(25 + R_D) = 25 R_D$

$52.5 + 2.1 R_D = 25 R_D$

$52.5 = 22.9 R_D$

$R_D = 2.29\Omega$

$V_{DS} = V_{GS} - V_{th}$

$0.8 + 0.8 = V_{GS}$

1.6

$0.2 \times 10^{-3} = k_n$ (W/L)

0.25×10^{-3}

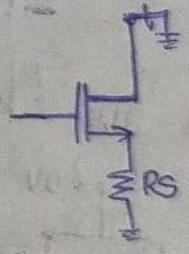
250×10^{-6}

8) Design unity gain Amplifier with $V_{DD} = 8V$ $I_D = 0.5mA$ $g_m = 1.5$ m

$A_V = \frac{g_m R_S}{1 + g_m R_S}$

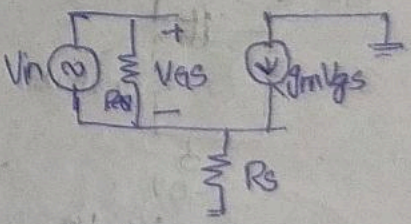
$I_D = g_m V_{GS}$

$V_{GS} = \frac{0.5 \times 10^{-3}}{1.5} = 0.3mV$

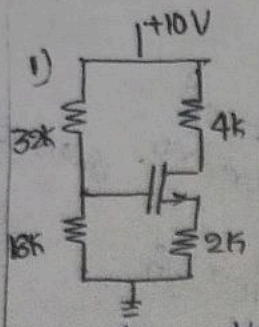


$A = \frac{1.5 R_S}{1 + 1.5 R_S}$

$1 + 1.5 R_S = 1.5 R_S$



1)



$V_{th} = 2V$

$K_n = 0.5 mA/V^2$

V_{GS}, I_D, V_{DS}

$V_{GS} = V_G - V_S$

$V_G = 18 \times \frac{10}{50} = \frac{18}{5} = 3.6$

$V_S = I_D R_S$

$I_D = 0.5 \times 10^{-3} \left[(3.6 - I_D 2K) - 2 \right]^2$

$I_D = 0.5 \times 10^{-3} \left[(1.6 - 2K I_D)^2 \right]$

$I_D = 0.5 \times 10^{-3} \left[4 \times 10^6 I_D^2 - 6.4K I_D + 2.56 \right]$

$I_D = 2 \times 10^{-3} I_D^2 - 3.2 I_D + 1.28 \times 10^{-3}$

$2 \times 10^{-3} I_D^2 - 4.2 I_D + 1.28 \times 10^{-3} = 0$

$I_D = 1.73 mA$

$I_D = 3.69 mA$

$V_{GS} = 3.6 - (1.73)(2) = 0.14$

$V_{GS} = 3.6 - \cdot = -3.78$

$V_{DS} = V_{DD} - I_D R_D - I_D R_S$

$= 10 - (1.73(6)$

$= -0.38$

$V_G = 3.6$

$V_S = 3.6 - V_{GS}$

$I_D R_S = V_S$

$I_D = \frac{V_S}{R_S} = \frac{3.6 - V_{GS}}{2K}$

$I_D = 0.5 (V_{GS} - 2)^2$

$3.6 - V_{GS} = 0.5 (V_{GS} - 2)^2$

$V_{GS}^2 - 4V_{GS} + 4 + V_{GS} - 3.6 = 0$

$V_{GS}^2 - 3V_{GS} + 1.6 = 0$

$V_{GS} = 2.30$

$V_{GS} = 0.69$

$\boxed{V_{GS} = 2.30}$

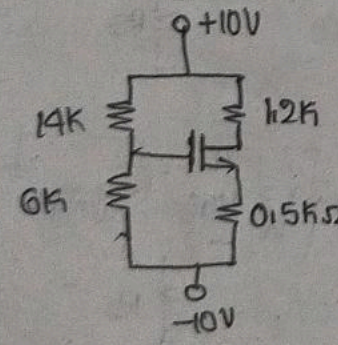
$I_D = 0.5 (0.3)^2 = 0.045 mA$

$V_{DS} = V_{DD} - I_D (R_D + R_S)$

$= 10 - (0.045)(6)$

$= 0.973$

2) $V_{th} = 2V$ $K_n' = 60 \mu A/V^2$ $W/L = 60$



$V_{GS} = ?$

$I_D = ?$

$V_{DS} = ?$

$V_{GS} = V_G - V_S$

$V_G = 10 \frac{6K}{20K} = 3V$

$V_{GS} = 3 - I_D 0.5K\Omega$

$V_{GS} = 0.03 ; -0.69$

$V_{DS} =$

$I_D = \frac{1}{2} \times 60 \times 10^{-6} \times 60 (V_{GS} - V_{th})^2$

$= \frac{1}{2} \times 36 \times 10^{-4} (3 - 0.5K I_D - 2)^2$

$I_D = 1.8 \times 10^{-4} (1 - 0.5K I_D)^2$

$I_D = 1.8 \times 10^{-3} \left[1 + 0.25 \times 10^6 I_D^2 - 1K I_D \right]$

$I_D = 1.8 \times 10^{-3} + 0.45 \times 10^3 I_D^2 - 1.8 I_D$

$450 I_D^2 - 2.8 I_D + 1.8 \times 10^{-3} = 0$

$I_D = 5.94 mA$

$= 7.28 mA$

$V_{GS} = V_{GS} - V_S + 10$

$V_g = 20\left(\frac{6}{20}\right) - 10$

$V_g = -4V$

$I_D = \frac{V_S - 10}{0.5K}$

$I_D = \frac{1}{2} \times 60 \times 10^{-6} \times 60 (V_{GS} - 2)^2$

$\frac{1}{2} \times \frac{1800 - 6}{3600} \times 10$

1.8×10^{-3}

$V_S - 10 = \frac{1}{2} \times \frac{30}{60} \times 0.5 \times 10^{-3} \times 60 (V_{GS} - 2)^2$

$\frac{15}{6}$

$\frac{60}{30}$

~~$V_S - V_{GS} = 15 \times 60 (V_{GS} - 2)^2$~~

~~$-4V - V_{GS} = 900 (V_{GS}^2 - 4V_{GS} + 4)$~~

~~$10 - 4 - V_{GS} = 900 V_{GS}^2 - 3600 V_{GS} + 3600$~~

~~$900 V_{GS}^2 - 3599 V_{GS} + 3594 = 0$~~

$\frac{V_S + 10}{0.5K} = 1.8 \times 10^{-3} (V_{GS} - 2)^2$

$V_S + 10 = 9 (V_{GS} - 2)^2$

$V_G - V_{GS} + 10 = 9 (V_{GS} - 2)^2$

$6 - V_{GS} = 9 (V_{GS}^2 - 4V_{GS} + 4)$

$6 - V_{GS} = 9V_{GS}^2 - 36V_{GS} + 36$

$9V_{GS}^2 - 35V_{GS} + 30 = 0$

$V_{GS} = 2.613$

$V_{GS} = 1.27$

$I_D = \frac{V_S + 10}{0.5K} = \frac{V_G - V_{GS} + 10}{0.5K}$

$= \frac{6 - 2.613}{0.5}$ mA

$I_D = 6.774$ mA

9.46 mA

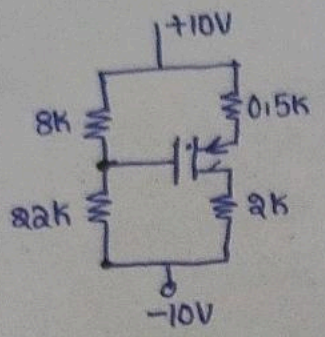
$V_{DS} = 20 - 6.774 (1.2 + 0.5)$

$= 8.48V$

$V_{DS} = 8.613 - 2 = 0.613$

$8.48 > 0.613$

7-9



$V_g = 20\left(\frac{22}{30}\right) - 10$

$= 20\,\frac{44}{3} - 10$

$= \frac{14}{3}$

$V_g = 4.67$

$V_{SG} = V_S - V_G$

$V_S = V_{SG} + V_G$

$I_D R_S = -V_S + 10$

$I_D = \frac{10 - V_S}{2K}$

$= \frac{10 - (V_{SG} - 4.67)}{2}$

$I_D = \frac{5.33 - V_{SG}}{2K}$

$I_D = K_p (V_{SG} - |V_{th}|)^2$

$I_D = 1mA\,(V_{SG} - 2)^2$

$5.33 - V_{SG} = 2(V_{SG}^2 - 4V_{SG} + 4)$

$2V_{SG}^2 - 8V_{SG} + 8 + V_{SG} - 5.33 = 0$

$2V_{SG}^2 - 7V_{SG} + 3.33 = 0$

$V_{SG} = 2.93$

$V_{SG} = 0.56$.

$V_{SG} \geq |V_{th}|$

$\boxed{V_{SG} = 2.93}$

$I_D = \frac{5.33 - 2.93}{2}\,mA$

$I_D = 1.2mA$

$V_{SD} = V_S - V_D$

$V_D = 10 - 0.5(7.2)$

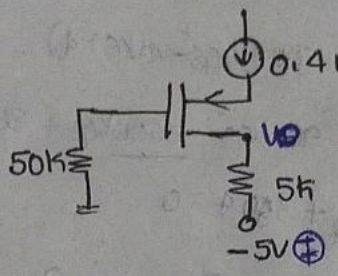
$= 10 - 0.6$

$V_D = 0.4$

$V_{SD} = 7.6 - 0.4$

$\boxed{V_{SD} = 7.2}$

10)
11)



$V_{TP} = -0.8$

$K_p = 200\,\mu A/V^2$

$V_g = 0$

$V_S + 5 = 0.4(5K)$

$V_S = 2$

$V_D = -3$

$V_{gs} = V_g - V_S = +V_S$

$0.4 = 200\times10^{-6}(V_S - 0.8)^2$

$0.4 = 2\times10^{-4}(V_S^2 - 1.6V_S + 6.4)$

$0.4 = 2\times10^{-4}V_S^2 - 3.2\times10^{-4}V_S + 1.28\times10^{-3}$

$2\times10^{-4}V_S^2 - 0.4V_S + 1.28\times10^{-3} = 0$

$0.4 = 0.2(V_S - 0.8)^2$

$2 = (V_S - 0.8)^2$

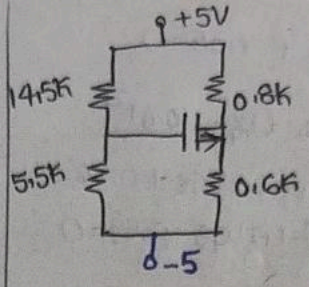
$V_S = 1.414 + 0.8$

$\boxed{V_S = 2.21V}$

$V_{SD} = V_S - V_D$

$= 2.21 + 3$

$= 5.21V$



$V_{th} = -1V$

$K_n = 0.5 mA/V^2$

find V_{GS}, I_D, V_{DS}

$V_G = \frac{10}{5}\left(\frac{5.5}{20}\right) - 5 = \frac{10}{24}$

$\boxed{V_G = -2.25}$

$V_{GS} = V_G - V_S$.

$V_{GS} = -2.25 - V_S$

$V_S = 0.6$

$V_S + 5 = 0.6 I_D$.

$I_D = \frac{V_S + 5}{0.6K}$

$\frac{V_S+5}{0.6K} = 0.5\times10^{-3}(-2.25 - V_S + 1)^2$

$= 0.5\times10^{-3}(-1.25 - V_S)^2$

$V_S + 5 = 0.3(V_S + 1.25)^2$

$V_S + 5 = 0.3[V_S^2 + 2.5V_S + 1.5625]$

$0.3V_S^2 + 0.75V_S - V_S - 3.4375 = 0$

-0.25

$1 - 0.75$

0.25

0

$\boxed{V_S = 3.82}$ $\boxed{V_S = -2.99}$

$V_{GS} = -2.25 + 2.99$

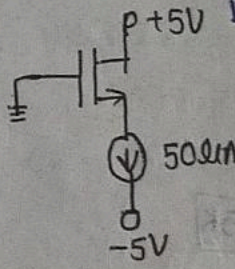
$\boxed{V_{GS} = 0.74}$

$V_{GS} > V_{th}$

$I_D = 0.5\times10^{-3}(0.74+1)^2 = 1.51 mA$

$V_{DS} = V_D - V_S = 5 - 1.51(1.4) = 2.886$.

15) $V_{th} = 1.2$ $K_n = 0.5 mA/V^2$ $\lambda = 0$ The $V_{DS} = ?$



it is saturation region

$50\times10^{-6} = 0.5\times10^{-3}(V_{GS} - 1.2)^2$

$100\times10^{-3} = (V_{GS} - 1.2)^2$

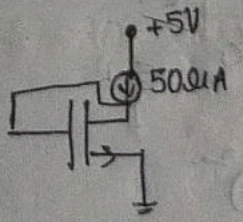
$\sqrt{0.1} + 1.2 = V_{GS}$

$V_{GS} = 1.516$ $V_S = -1.516$

$V_{DS} = V_{GS} - V_{th} = 1.516 - 1.2 = 0.316$

$V_D - V_S = 5 + 1.516 = 6.516V$.

16) $V_{th} = 1.2V$ $K_n = 0.5 mA/V^2$ $\lambda = 0$ $V_{DS} = ?$



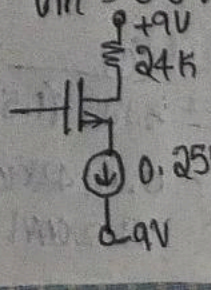
$V_{GS} = V_{DS}$

$50\times10^{-6} = 0.5\times10^{-3}(V_{GS} - 1.2)^2$

$\sqrt{0.1} + 1.2 = V_{GS}$

$\boxed{V_{GS} = V_{DS} = 1.52V}$

17) $V_{th} = 0.6V$ $K_n = 0.2 mA/V^2$ $V_S = ?$



$V_{GS} = -V_S$.

$V_{DS} = 9 - 0.25(24)$

$V_{DS} = 3$

$V_D - V_S = 3$

$V_S = 9 - 3 = 6V$.

$0.25\times10^{-3} = 0.2\times10^{-3}(-V_S - 0.6)^2$

$1.85 = (V_S + 0.6)^2$

$\sqrt{1.85} - 0.6 = V_S$

$V_S = 0.51$

$V_S^2 + 1.2V_S + 2.35 = 0$

$0.25 = 0.2\,(V_{GS} - 0.6)^2$

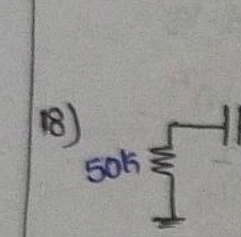
$1.25 = V_{GS}^2 - 1.2V_{GS} + 0.36$

$V_{GS}^2 - 1.2V_{GS} - 0.89 = 0$

$V_{GS} = 1.71$

$V_S = -1.71$

18)



$V_{th} = 1.7V$

$K_n = 0.4 mA/V^2$

$I_D = 0.8mA$ $V_D = 1V$ value of R_S & R_D.

$V_{GS} = 0$

$V_g = 0$

$V_{GS} = -V_S$

$V_S + 5 = 0.8 \times 10^{-3} R_S$

$0.8 \times 10^{-3} = 0.4 \times 10^{-3} (V_{GS} - 1.7)^2$

$2 = (V_{GS} - 1.7)^2$

$V_{GS}^2 - 3.4V_{GS} + 2.89 - 2 = 0$

$V_{GS}^2 - 3.4V_{GS} + 0.89 = 0$

$V_{GS} = 3.11$ $V_{GS} = 0.28$

$V_S = -3.11$

$V_{DS} = V_D - V_S = 5 + 3.11 = 8.11\ V$

$-3.11 + 5$

$\frac{2.11}{0.8} K = R_S$

$R_S = 2.638k$

$8.11 = 5 - 0.8m(R_D + 2.63k)$

$8.11 = 5 - 0.8m R_D - 2.104$

$2.1 + 3.11 = -0.8m R_D$

$\frac{5.21}{0.8} K = R_D$

$R_D = 6.51k$ $R_D = 5k$

$1 = V_{DD} - I_D R_D$

$1 = 5 - 0.8mA(R_D)$

$0.8mA(R_D) = 4$

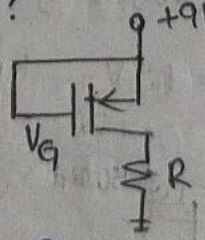
$R_D = \frac{4}{0.8} k\Omega$

$R_D = 5k\Omega$

19) $V_{thp} = -1.5V$ $k_p' = 85 \mu A/V^2$ $L = 4\mu m$ $\lambda = 0$ $I_D = 0.1m$

$V_{SD} = 2.5V$ then value of $W = ?$

$V_g = V_S$ $V_{SG} = 0$



$V_{SD} \geq |V_{SG} - |V_{th}|$

$V_{SD} = 1.5V$

$I_D = \frac{1}{2} \times 25 \times 10^{-6} \times \frac{W}{4 \times 10^{-6}} (V_{SG} - 1.5)^2$

$0.1 \times 10^{-3} = \frac{25}{8} W_D (V_{SG} - 1.5)^2$

$\frac{0.1}{3.125} \times 10^{-3} = W (1.5)^2$

$W = \frac{0.1}{3.125 \times (1.5)^2} \times 10^{-3}$

$= 0.0142 \times 10^{-3}$

$= 14.2 \mu m$

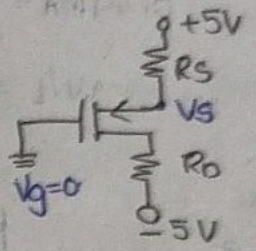
$V_{SD} = V_{SG} = 2.5 - 0$ 2.5

$\frac{0.1}{3.125} \times 10^{-3} = W$ 2.5 − 1.5

$W = 32\mu m$

20) $V_{th_p} = -1.2V$ $W/L = 20$, $K_p' = 30\mu A/V^2$ $I_D = 0.5mA$ $V_D = -3V$

$R_S = ?$ $R_D = ?$



$I_D = \frac{1}{2} \times 30 \times 10^{-6} \times 20 (V_{SG} - 1.2)^2$

$0.5 \times 10^{-3} = 15 \times 20 \times 10^{-6} [V_{SG} - 1.2]^2$

$1.6 = V_{SG}^2 - 2.4 V_{SG} + 1.44$

$V_{SG}^2 - 2.4 V_{SG} - 0.16 = 0$

$V_{SG} = 2.46$

$V_S = 2.46$.

$V_D = -3V$

$V_S + 5 = 0.5 \times 10^{-3} R_S$

$\frac{7.46}{0.5} K = R_S$

$R_S = 14.92K$

$-3 + 5 = 2.46 (R_D)$ / 0.5×10^{-3}

$4K = R_D$

$R_D = 4K\Omega$

$V_{SD} = 2.46 + 3 = 5.46V$

$5.46 = 5 - 0.5 \times 10^{-3} (R_D + R_S)$

$\frac{0.46}{0.5} K = 4K + R_S$

$\frac{5 - V_S}{0.5} K = R_S$

$R_D = 5.08 \cdot K$

21) $V_{th} = 2V$ $K_n = 0.2mA/V^2$

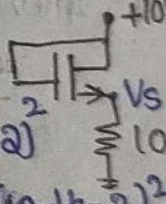
$V_{SD} = V_{SG}$

$V_D = V_G = 10$

$V_D - V_S =$

$V_{DS} = V_{GS}$

$V_D - V_S = 10 - V_S$



$\frac{V_S}{10K} = I_D$

$I_D = 0.2 \times 10^{-3} (V_{GS} - 2)^2$

$\frac{V_S}{} = 0.2 \times 10K \times 10^{-3} (10 - V_S - 2)^2$

$V_S = 2 (8 - V_S)^2$

$2 V_S^2$

$0.5 V_S = V_S^2 - 16 V_S + 64$

64 / 4 / 0.5 / 3.5

$V_S^2 - 16 V_S + 63.5 = 0$

$V_S = 8.70$ $V_S = 7.29$

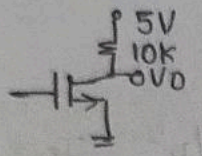
$V_S = 7.29$

$V_{DS} = 10 - 7.29 = 2.71$

$I_D = \frac{7.29}{10} mA = 0.729mA$

$P = V_{DS} I_D = 2.71 \times 0.729 = 1.97mW$

Q8) $V_{th} = 0.8V$ $k_n' = 30\times10^{-6}$ $V_o = 0.1V$ $V_i = 4.2V$ $W/L = ?$



$0.1 = 5 - I_D(10k)$

$I_D(10k) = 4.9$

$I_D = 0.49mA$

$0.49mA = \frac{1}{2}\times30\times10^{-6}(4.2-0.8)^2\, W/L$

$W/L = \frac{8\times0.49\times10^{3}}{30\,(4.2-0.8)^2}$

$\frac{0.98}{}$

$W/L = 2.82$

12
4.2
0.8
3.4

$0.1 < 4.2 - 0.8$

$I_D = \frac{1}{2}k_n\, W/L\,[2(V_{gs}-V_{th})V_{DS} - \frac{V_{DS}^2}{2}]$

In linear region

$I_D = \frac{1}{2}k_n\, W/L\,[2(V_{gs}-V_{th})V_{DS} - \frac{V_{DS}^2}{2}]$

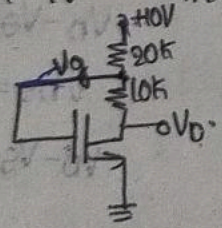
$0.49\times10^{-3} = \frac{1}{2}30\times10^{-6}\, W/L\,[2(3.4)(0.1) - 5\times10^{-3}]$

$0.49\times2 = 30\times10^{-6}\frac{W}{L}[0.68]$

$W/L = \frac{0.49\times2}{30\times0.68}\times10^{3}$

$= 48.03$

$V_{th} = 1V$ $k_n = 12.5\,\mu A/V^2$ (I_D, V_{DS})



$\frac{10-V_g}{I_D} = 20k$

$I_D = \frac{10-V_g}{I_D}$

$\frac{10-V_g}{20k} = \frac{1}{2}\times12.5\times10^{-6}(V_g-1)^2$

$10-V_g = 12.5\times2\times10^{-2}(V_g-1)^2$

$\frac{V_g-V_D}{10k} = 0.246mA$

$10-V_g = 0.25V_g^2 - 0.5V_g + 0.25$

$V_g - V_D = 2.46$

$0.25V_g^2 + 0.5V_g - 9.75 = 0$

$V_D = 5.08 - 2.46$

$V_g = 5.92$

$V_{DS} = 2.62$

$I_D = \frac{10-5.92}{20}\,mA$

$I_D = 4.92$ 246 mA

$= 0.246mA$

$I_D = 0.234mA$

$\frac{V_g - V_D}{10K} = 0.234mA$

$5.32 - V_D = 2.34$

$5.32 - 2.34 = V_D$

$\boxed{V_D = 2.98}$ 3.1V

1) A mos capacitor has $t_{ox} = 50nm$ the capacitance is for si $\varepsilon_r = 3.9$

$C_{ox} = \frac{\varepsilon_o \varepsilon_r}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-12}}{50 \times 10^{-9}}$ $\varepsilon_o = 8.85 \times 10^{-12}$ F/m

$= 0.6903 \times 10^{-3}$

$= 0.69 \times 10^{-3}$

$= 69 \times 10^{-5} \times 10^{-4}$ $\frac{69 \times 10^{-9}}{10^{-4}}$ 69×10^{-5} 0.69×10^{-3}

$\frac{}{10^{-4}} = 69nF/cm^2$

2) Ideal n channel MOSFET has $\mu_n = 525\ cm^2/V\text{-}S$ $V_{th} = 0.75$ $t_{ox} = 400A^{\circ}$ when MOSFET is biased in saturation region at $V_{GS} = 5V$ required $I_D = 6mA$ the required W/L ratio is

$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2$

$C_{ox} = \frac{\varepsilon_o \varepsilon_r}{t_{ox}}$

$6mA = \frac{1}{2} \times 525 \times 10^{-4} \times 0.86 \times 10^{-3} (5 - 0.75)$

$= \frac{3.9 \times 8.85 \times 10^{-12}}{400 \times 10^{-10}}$

$2 \times 6 = 525 \times 10^{-4} \times 0.86\ W/L\ (4.25)^2$

$= \frac{34.515}{8.6 \times 10^{-4}}$

$\frac{W}{L} = \frac{2 \times 6}{525 \times 0.86 \times 18.06 \times \times 10^{-4}}$ $= 0.86 \times 10^{-3}$

$\boxed{W/L = 14.71}$

3) An ideal pmos has $\mu_p = 300\ cm^2/V\text{-}S$ $V_{tp} = -0.75$ $t_{ox} = 400A^{\circ}$ when MOSFET is biased in saturation region $10^{-10}m$ $V_{sg} = 5V$ required W/L is when $I_D = 6mA$ 10^{-12} F/m

$I_D = \frac{1}{2} 300 cm^2/V\text{-}S$

$I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} [V_{sg} - |V_{thp}|]^2$ $C_{ox} = \frac{\varepsilon_o \varepsilon_r}{t_{ox}}$ 10^{-14} F/cm

$6 \times 10^{-3} = \frac{1}{2} \times 300 \frac{cm^2}{V\text{-}S} \times 0.086 \times 10^{-6} \frac{F}{cm^2} \frac{W}{L} [5 - 0.75]^2$ $= \frac{8.85 \times 10^{-14} F/cm \times 3.9}{400 \times 10^{-8} cm}$

$6 = \frac{1}{2} \times 300 \times 0.086 \times 10^{-3}\ W/L\ (4.25)^2$ $= \frac{34.515}{400} \times 10$ F/cm^2

$W/L = \frac{2 \times 6}{300 \times 0.086 (4.25)^2} \times 10^3$ $= 0.086 \times 10^{-6}$

$= 0.0257 \times 10^3$

$= 25.7 V/V$

An NMOS $W = 30\mu m$ $\mu_n = 450\ cm^2/V\text{-}S$ $L = 2\mu m$ $t_{ox} = 350A^0$
$V_{th} = 0.8V$ $V_{GS} = 4V$ value of g_m

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th}) \qquad C_{ox} = \frac{3.9 \times 8.85 \times 10^{-14}}{350 \times 10^{-8}}\ F/cm^2$$

$$= 450 \frac{cm^2}{V\text{-}S} \cdot 0.0986 \times 15 \times 3.2 \times 10^{-6} \qquad = 0.0986 \times 10^{-6}$$

$$= 2.188 \text{ milli siemes}$$

Q) a) N CHANNEL MOSFET $V_{th} = 1.5V$ $K_n = 0.25\ mA/V^2$ $V_{GS} = 5V$ $V_{DS} = 6V$

$I_D = ?$

$V_{DS} = 6$ $V_{GS} - V_{th} = 5 - 1.5 = 3.5$ $[6 > 3.5]$

* Saturation Region

$$I_D = 0.25 \times 10^{-3}[5 - 1.5]^2 = 0.25 \times 3.5^2$$
$$= 0.25 \times 12.25\ mA$$
$$= 3.06\ mA$$

b) $V_{GS} = 5V$ $V_{DS} = 2.5\ V$ then I_D is.

$V_{DS} = 2.5 < V_{GS} - V_{th}$

$$I_D = \mu_n C_{ox} W/L \left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$= 0.5\left[(3.5)(2.5) - \frac{6.25}{2}\right]$$

$$= 0.5\,[8.75 - 3.125]$$

$$= 0.5\,[5.625]$$

$$2.812\ mA$$

* N channel MOSFET $V_{th} = 0.8$ $K_n' = 80\mu A/V^2$ $\frac{W}{L} = 5$

$I_D = 0.5\ mA$ then V_{GS} is

$$0.5 \times 10^{-3} = \frac{1}{2} \times 80 \times 10^{-6} \times 5\,(V_{GS} - 0.8)^2$$

$$\frac{1 \times 10^{-3}}{80 \times 5} = (V_{GS} - 0.8)^2$$

$$2.5 = V_{GS}^2 - 1.6V_{GS} + 0.64$$

$$V_{GS}^2 - 1.6V_{GS} + 3.9 = 0$$

$$V_{GS} =$$

$$V_{GS} = \sqrt{2.5} + 0.8$$

$$\boxed{V_{GS} = 2.38}$$

* $V_{th} = -2.5V$ $K_n = 1.1\,mA/V^2$ $V_{GS} = 0V$ $V_{DS} = 0.5$ $I_D = ?$

$0.5 > 0$ $I_D = 1.1 \times 10^{-3}(-2.5)^2$

$= 6.8\,mA$

* $V_{GS} = 8V$ $V_{DS} = 2.5V$ then current I_D is $K_n = 1.1\,mA/V^2$ $V_{th} = -2.5$

~~$2 < 2.5$~~ Cutoff. $I_D = 1.1 \times 10^{-3}(2+2.5)^2$ $V_{GS} = 2V$

$= 20.25 \times 1.1\,mA$ $V_{DS} = 2.5$

$22.275\,mA$ [SAT Region] $V_{DS} < 4.5$

in triode region

$I_D = 2 \times 1.1 \times 10^{-3}\left[(4.5)(2) - \frac{2^2}{2}\right]$ $V_{DS} = 2.5V$

$I_D = 2.2 \times 10^{-3}[6.5]$ $[10.625 - 3.125]$

$= 14.3\,mA$

$I_D = 2.2 \times 17.5\,mA$

* N channel D MOSFET $V_{TN} = -2V$ $K_n' = 80\,\mu A/V^2$ $I_D = 1.5mA$

at $V_{GS} = 0$ and $V_{DS} = 3$ ration of W/L

$V_{DS} = 3$ $V_{GS} - V_{th} = 2$

$3 > 2$ $1.5 \times 10^{-3} = \frac{1}{2} \times 80 \times 10^{-6} \times \frac{W}{L}(2)^2$

$\frac{2 \times 1.5}{80 \times 4} \times 10^3 = W/L$ $\frac{3}{320} \times 10^3$

$\boxed{W/L = 9.375}$

* N channel E MOSFET $\mu_n = 650\,cm^2/V\text{-}S$ $V_{TN} = 0.8V$ $\frac{W}{L} = 16$.

$t_{ox} = 450A^0$ $K_n = ?$

$C_{ox} = \frac{3.9 \times 8.85 \times 10^{-14}}{450 \times 10^{-8}} = 0.076 \times 10^{-6}$

$K_n = \frac{1}{2}\mu_n C_{ox} W/L = 650 \times 0.076 \times 16 \times 10^{-6}$ $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

$= \frac{1}{2} 797.68\,\mu A/V^2$

$= 398.84\,\mu A/V^2$

$= 0.398\,mA/V^2$

* $V_{GS} = V_{DS} = 3V$ $I_D = ?$

$3 > 2.2$ $I_D = 0.398 \times 10^{-3}(2.2)^2$

$= 1.93\,mA$

* for NMOS $V_{th} = 1V$ $L = 2.4\,\mu m$ $\mu_n = 600 cm^2/V\text{-}S$

$t_{ox} = 400A^0$ $V_{GS} = 5V$ $I_D = 1.2\,mA$ $W = ?$

$1.2 \times 10^{-3} = \frac{1}{2} \times 600 \times 0.086 \times 10^{-6} \times \frac{W}{2.4 \times 10^{-6}}(4)$ $\frac{2 \times 3.9 \times 8.85}{400} \times 10^{-6}$

$W = \frac{2 \times 1.2 \times 2.4}{600 \times 0.086 \times 4 \times 4} = 6.97 \times 10^{-3} \times 10^{-3}$

$= 6.97\,\mu m$.

P MOSFET $k_p = 40\mu A/V^2$

$I_D = 0.225\,mA$ at $V_{SG} = V_{SD} = 3V$

$I_D = 1.4\,mA$ at $V_{SG} = V_{SD} = 4V$ find V_{TH}

$0.225\times10^{-3} = \frac{1}{2}\times40\times10^{-6}\times\alpha\,(3-V_{th})^2$

$1.4\times10^{-3} = \frac{1}{2}\times40\times10^{-6}\times\alpha\,(4-V_{th})^2$

$\frac{0.225}{1.4} = \left(\frac{3-V_{th}}{4-V_{th}}\right)^2$ $\therefore \frac{3-V_{th}}{4-V_{th}} =$

$0.4(4-V_{th}) = 3-V_{th}$

$1.6-0.4V_{th} = 3-V_{th}$

$0.6V_{th} = 1.4$

$V_{th} = 2.33$

$V_{thp} = -2.33$ ∵ PMOS.

ratio of w/L is

$0.225\times10^{-3} = 20\times10^{-6}\times\alpha(3-2.33)^2$

$\alpha = \frac{0.225}{20\times0.67}\times10^3$ $\frac{2\times0.225}{40\,(3-2.33)^2}$

$\alpha = \frac{0.45}{40(0.67)^2} = 16.71$

$= 25.06\ V/V$

→ pchannel EMOS $k_p = 2mA/V^2$ $V_{tp} = -0.5V$

$V_G = 0$ $V_S = 5V$

* If $V_D = 0$ then $I_D = ?$

$V_G - V_S = V_S - V_G = 5 \geq |V_{th}|$

$V_{SD} = V_{SG} - |V_{th}| = 5 - 0.5 = 4.5$

$V_{SD} = V_S - V_D = 5$

$V_{SD} > V_{SG} - |V_{th}|$

$I_D = \frac{k_p}{2}\,2mA\,(5-0.5)^2$

$2\times20.25\ mA$

$= 40.5\ mA$

$V_D = 2V$ then $I_D = ?$

$V_{SG} = 5V$ $V_{SD} = V_S - V_D = 5-2 = 3$

$V_{SG} - V_{th} = 4.5$

$I_D = 2\times2mA/V^2\,(4.5)^2$

$= 2\times2\times20.25\ mA$

$=$

$I_D = 2 \times 2 \left[(V_{sg} - V_{th}) V_{SD} - \frac{V_{SD}^2}{2} \right]$

$= 4 \times 10^{-3} \left[(4.5)(3) - \frac{9}{2} \right]$ (3-1)

$4 \times 10^{-3}\ 4.5 \times 2$

$= 36mA$.

$V_D = 5V$ then I_D

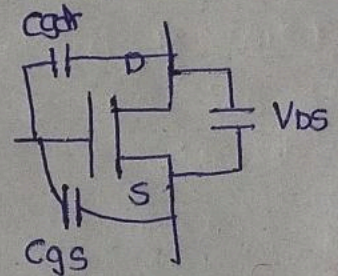
$V_{SD} = V_S - V_D = 0V$

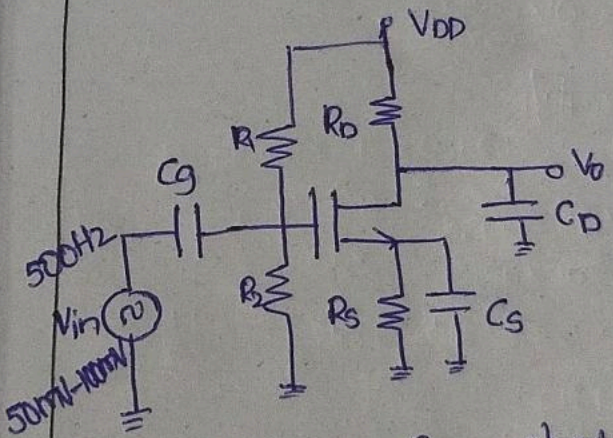
$V_{sg} - V_{th} = 5 - 0.5 = 4.5$.

$0 < 4.5$.

triode region $I_D = 2 \times 2 \times 10^{-3} [4.5(0) - 0] = 0mA$.

Capacitance effect was observed at higher frequencies





$V_{DD} = 12V$

$I_D = 1mA$

when consider C_G, short circuit C_D, C_S. place test voltage in place of C_G.

$f_L = \frac{1}{2\pi R_{across} C_{G1} C_G}$

$f_L = \frac{1}{2\pi (R_1 \| R_2) C_G}$ [nF]

$f_H = \frac{1}{2\pi R_{across} C_D C_D}$

$\boxed{f_H = \frac{1}{2\pi R_D C_D}}$

$f_L = 500Hz$.

$A_V = 5V/V$

$f_H > 50kHz$

$C_G \cong 10C_S$

C_G - nF

C_S - nF

C_D - pF.

$f_L = \frac{1}{2\pi R_{across} C_S \cdot C_S}$

$f_L = \frac{1}{2\pi (\frac{1}{g_m} \| R_S) C_S}$

$f_L = 500kHz$

COLLEGE DOSTH

19) $V_{th} = 1V$ $\frac{1}{2}\mu_n C_{ox} = 1.8\,mA$ $\lambda = 0.015V^{-1}$ $I_{DQ} = 2\,mA$ $g_m = 3.4\,mA/V$

the w/L ratio is

$$g_m = \frac{2I_{Dmax}}{V_{GS} - V_{th}} \qquad 3.4\times10^{-3} = \frac{8\times10^{-3}\times2}{V_{GS}-1}$$

$$V_{GS} - 1 = \frac{4}{3.4}$$

$$V_{GS} = \frac{4}{3.4} + 1$$

$$V_{GS} = 2.176$$

$$V_{DS} = 2 - 1.176$$

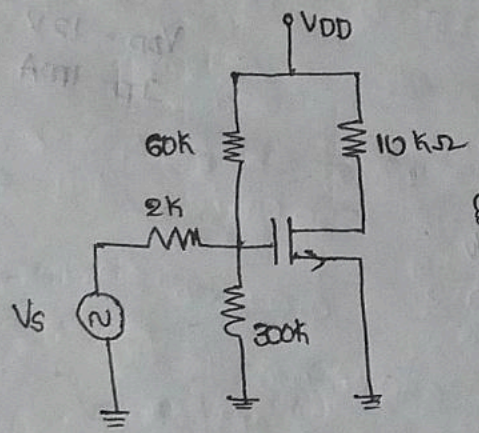
$$g_m = \sqrt{8 I_{Dsat} \mu_n C_{ox} \, W/L}$$

$$3.4\,mA = \sqrt{8\times2\times10^{-3} \times 2\times18\times10^{-3} \times W/L}$$

$$(3.4\times10^{-3})^2 = 8\times2\times2\times18\times10^{-6}\, W/L$$

$$W/L = \frac{11.56}{2\times2\times2\times18} = 0.0802$$

$g_m = 1\,mA/V$ $\quad r_o = 50k\Omega$ $\quad$ gain $= \frac{V_o}{V_s}$ is



common source

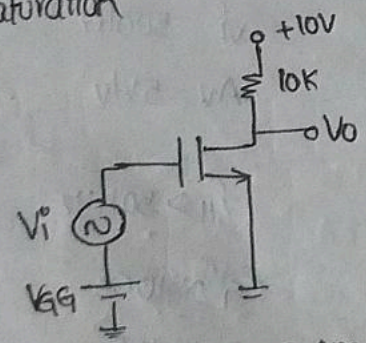
$$\text{gain} = -g_m R_D \| r_o$$

$$= -1\times10^{-3}\left(\frac{10\times50}{60}\right)\times10^{3}$$

$$= -\left[\frac{50}{6}\right]$$

$$= -8.33\ V/V$$

For ckt $V_{th} = 2V$ $\quad k_n = 0.5\,mA/V^2$ $\quad \lambda = 0$ transistor in saturation



if I_{DQ} is 0.4mA value of V_{GS} is

$$0.4mA = 0.5\,mA/V^2\,(V_{GS}-2)^2$$

$$\sqrt{0.8} + 2 = V_{GS}$$

$$V_{GS} = 2.89V$$

g_m & r_o are.

$\lambda = 0 \quad r_o = \infty$

$$g_m = \sqrt{2 I_{Dmax} 2K}$$

$$g_m = \sqrt{2 \times 0.4 \times 10^{-3} \times 2 \times 0.5 \times 10^{-3}}$$

$g_m = 0.89$ milli siemes

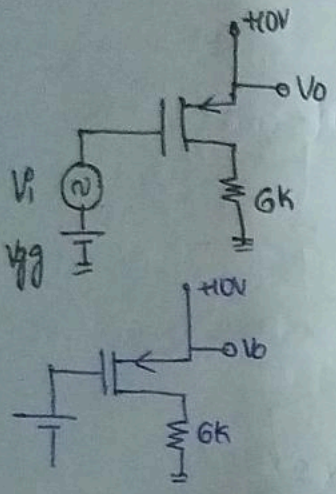
$r_o = \infty$

Small signal voltage gain $(A_v) = -g_m R_D$

$= -0.89 \times 10$

$= -8.9$

* for circuit shown, $V_{tp} = -1V$ $K_p = 2mA/V^2$ $\lambda = 0$ transistor is in saturation.



$V_{SD} = 7V$ then value of V_{SG} is.

$V_{SD} = V_{sg} - |V_{th}|$

$V_{SD} = V_{sg} - 1$

$V_{sg} = 7 + 1 = 8V$

$V_S - V_D = 7$

$10 - I_D 6K = 7$

$10 - 7 = I_D 6$

$I_D = \frac{3}{6}$ mA

$\boxed{I_D = 0.5mA}$

$0.5mA = 2mA (V_{sg} - 1)^2$

$\sqrt{\frac{0.5}{2}} + 1 = V_{SG}$

$V_{SG} = 1.5V$

$\frac{5}{20} \quad \frac{1}{4}$

$$g_m = \frac{2 \times 0.5}{1.5 - 1} = \frac{2 \times 0.5}{0.5} = 2 \text{ millisiemes.}$$

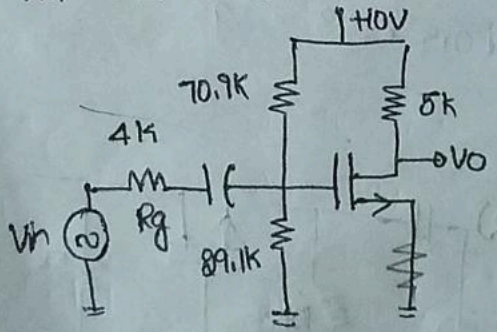
$$A_v = -g_m R_D = -2 \times 6K \times 10^{-3} = -12$$

Common Source Amplifier $V_{th} = 1.5V$ $K_n = 0.5mA/V^2$ $\lambda = 0.01V^{-1}$

$R_S = 4K\Omega$

* Small signal Vig gain A_v is

$$A_v = \frac{-g_m R_D}{1 + g_m R_S} = ?$$

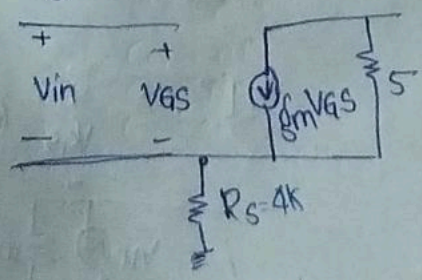


$V_D = V_{DD} - I_D R_D$

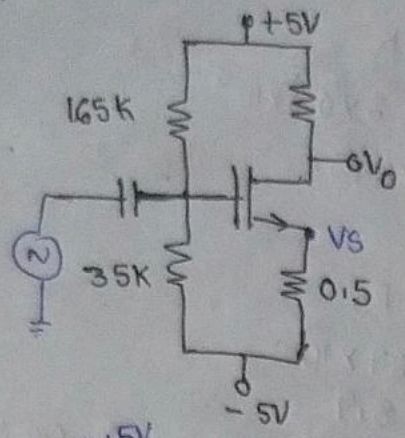
$R_D = 5K\Omega$

$R_i = \frac{70.9 \times 29.1}{70.9 + 29.1} = 20.6K\Omega$

$g_m =$



$V_{th} = 0.8V$ $k_n = 1mA/V^2$ $\lambda = 0$ Small signal voltage gain is



$g_m = ?$

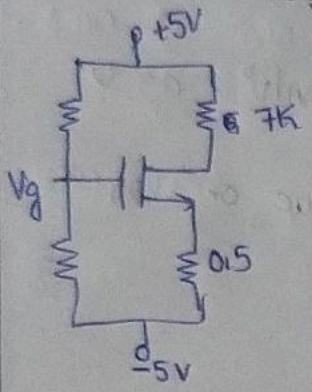
$V_g = \frac{5 \times 35}{200} - 0.875V$

$V_s = I_D R_s$

$V_g - 10\left[\frac{35}{200}\right] - 5$

$V_g = \frac{35}{20} - 5 = 1.75 - 5$

$\boxed{V_g = -3.25}$



$V_g + 5 = 5\frac{35}{165+35} = 0.875$

$V_{gs} = V_g - V_s$

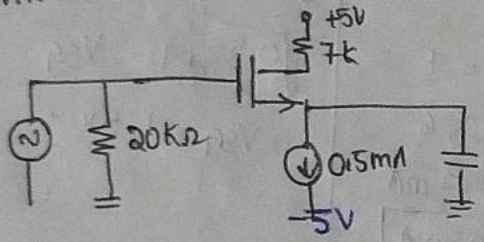
V_g

$\frac{V_s + 5}{0.5} = 1mA(-3.25 - V_s - 0.8)^2$

$V_{gs} = 1.5$ $g_m = 2 \times 10^{-3}(1.5 - 0.8)$

$g_m = 1.4mS$

$V_{th} = 0.8V$ $k_n = 1mA/V^2$ $\lambda = 0$ voltage gain



$-g_m R_D A_V = \frac{1.4 \times 0.5}{1 + 1.4 \times 0.5} = 0.4V/V$

$g_m = ?\sqrt{2 \times 0.5 \times 2 \times 1mA}$

$= \sqrt{4 \times 0.5}\ mA$

$= \sqrt{2}\ mA$

$= 1.414$ milli $\mho$

$V_D = 5 - 0.5 \times 7$

$V_D = 1.5V$

$0.5mA = 1mA(V_{gs} - 0.8)^2$

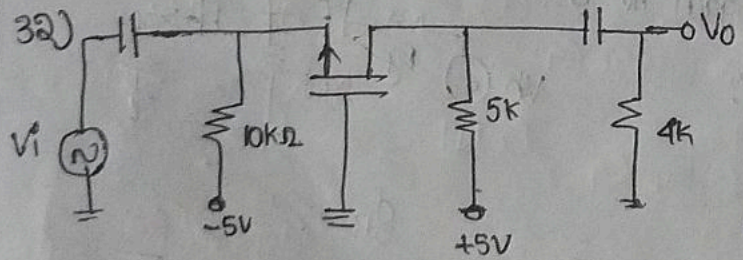
$\sqrt{0.5} + 0.8 = V_{gs}$

$A_V = -1.414(7)$

$= -9.898$

$= -9.9$

32)



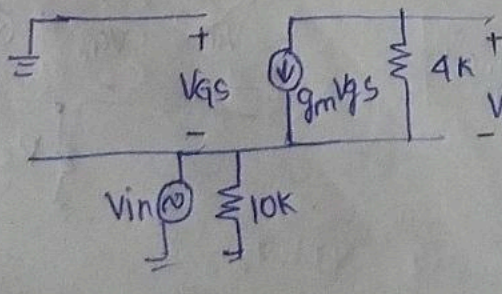
$g_m = 2mS$ $r_o = \infty$

Voltage gain $A_V = ?$

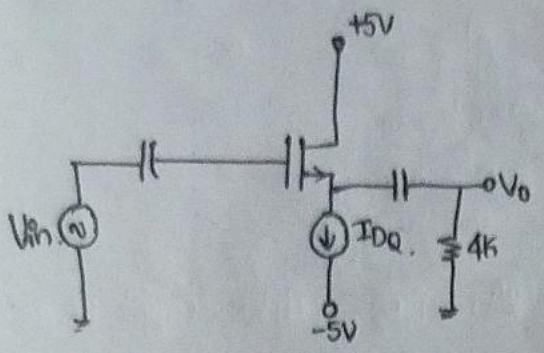
$A_V = g_m R_D$

$= 2 \times 4$

$= 8$



* Source follower circuit $g_m = 2mS$ $r_o = 100K\Omega$



$A_V = ?$

$A_V = \frac{g_m R_S}{1+g_m R_S}$

$= \frac{8 \times 4}{1+8 \times 4} = \frac{8}{9} = 0.89$

$R_S \| r_o$

$R_o = \frac{1}{g_m} \| r_o$

$\frac{1}{R_o} = g_m + \frac{1}{r_o}$

$\frac{1}{R_o} = 2mS + 0.01mA$

$R_o = \frac{1}{2.01} K$

$R_o = 0.49K.$ $\lambda = 0$

output Resistance:

$R_o = \frac{1}{g_m} \| R_S \| r_o$ 2.01

$\frac{1}{R_o} = g_m + \frac{1}{R_S} + \frac{1}{r_o}$

$\frac{1}{R_o} = 2mS + 0.25mA + 0.01mA$

$R_o = \frac{1}{2.26} K = 0.44K$

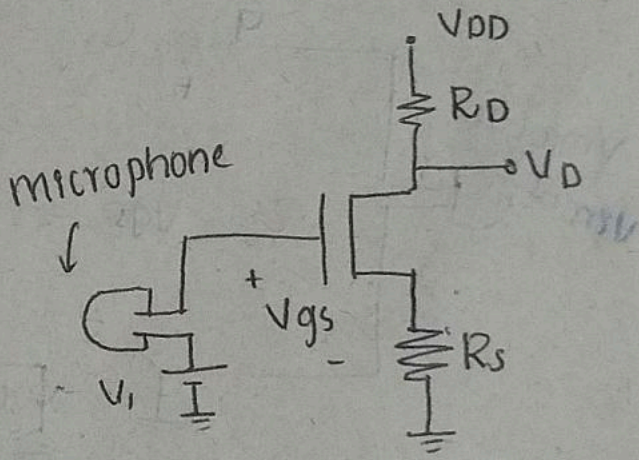
270

Degeneration of source common source stage:

→ Degeneration of gain

→ Gain variations are overcome by this stage (with R_S)

∴ Let the MOS is in SAT region.



→ voice signal to Electrical signal.

Biasing condition (DC):

(A=0)

Step1: Apply KVL for input loop

$$-V_i + V_{gs} + I_D R_S = 0$$

$$V_i = V_{gs} + I_D R_S$$

→ Assume Device is in SAT region.

$$\therefore I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2$$

Step2:

Voltage across drain terminal is given by

$$V_D = V_{DD} - I_D R_D$$

for saturation

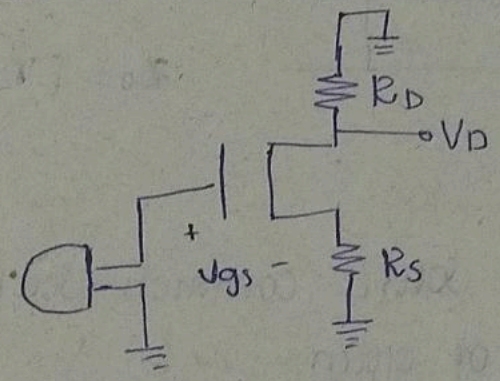
$$V_{DS} \geq V_{GS} - V_{th}$$

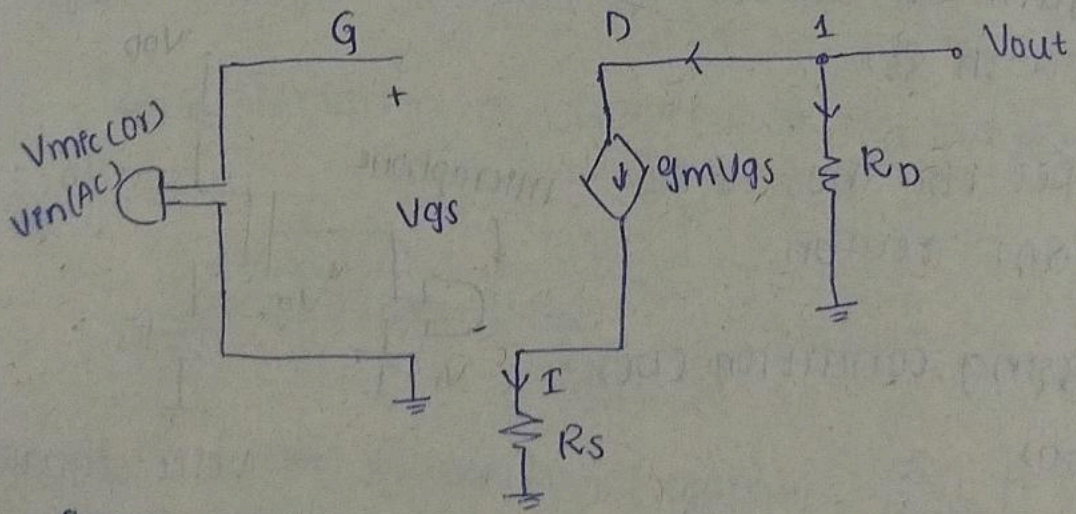
$$V_D \geq V_G - V_{th}$$

$$V_{DD} - I_D R_D \geq V_G - V_{th}$$

Step3: Small signal Analysis

Ac equivalent model:





from ckt

At node 1

current in $R_D = \frac{V_{out}}{R_D}$

and $g_m V_{gs} = -\frac{V_{out}}{R_D}$

$-V_{in} + V_{gs} + IR_S = 0$

$-V_{in} + V_{gs} + g_m V_{gs} R_S = 0$

$$\boxed{V_{in} = V_{gs}(1 + g_m R_S)}$$

$$\frac{V_{out}}{V_{gs}} = -g_m R_D$$

$$\frac{V_{out}}{\left(\frac{V_{in}}{(1+g_m R_s)}\right)} = -g_m R_D$$

$$\boxed{\frac{V_{out}}{V_{in}} = \frac{-g_m R_D}{1+g_m R_s}} = \frac{-R_D}{1/g_m + R_D}$$

$$\therefore I = g_m V_{gs} = \frac{-V_{out}}{R_D}$$

Note:

* If the source Resistance R_s increases then the value of gain decreases.
* If the value of $\frac{1}{g_m} << R_s$, then

$$\boxed{A_V = \frac{V_{out}}{V_{in}} = \frac{-R_D}{R_s}}$$

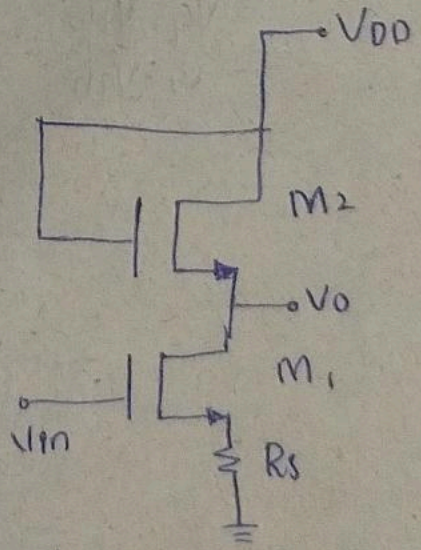
* Voltage gain can be defined as ratio of resistance tied between drain and AC ground (V_{DD}) to $\frac{1}{g_m}$ + Resistance tied to between source & AC ground

$$\boxed{A_V = \frac{-R_D}{\frac{1}{g_m} + R_s}}$$

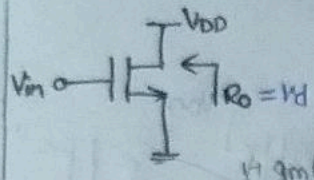
* $\lambda = 0$

$\therefore$ For M_2 diode connected device; Impedance = $1/g_{m2}$

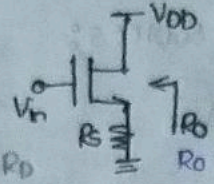
$$\boxed{A_V = \frac{-(1/g_{m2})}{1/g_{m1} + R_s}}$$



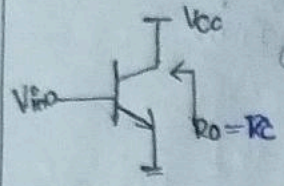
Cascode Current Soures with BJT :-



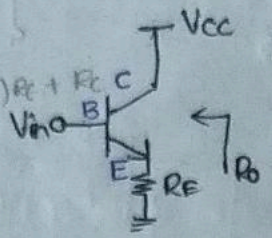
(1+gmRs) Rs + Rs



$R_o = (1+g_m R_s) R_s + r_d$

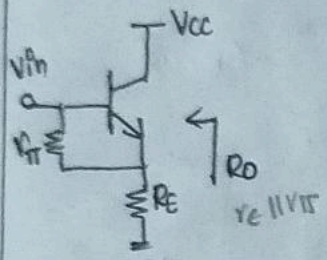


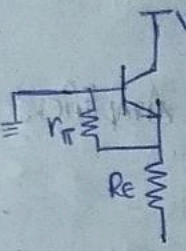
(1+gm RC) RE + RC



$R_o = (1+g_m r_c) R_E + r_c$

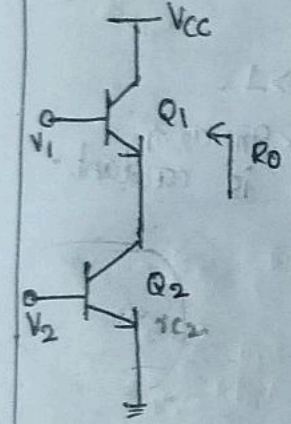
case (i) :

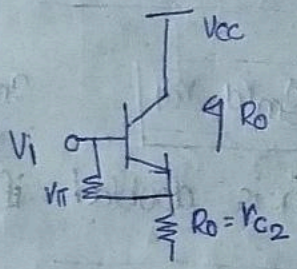




$R_o = (1+g_m r_c) R_E \| r_\pi + r_c$

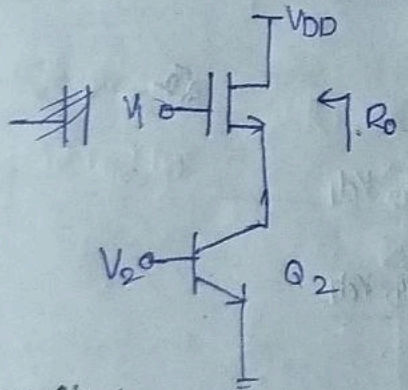
case (ii) :





$R_o = (1+g_m r_{c1})(r_{c2} \| r_\pi) + r_{c1}$

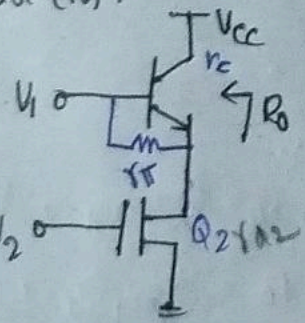
case (iii)



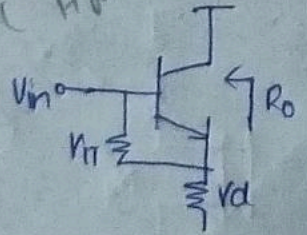
$R_E = r_{c2}$

$R_o = (1+g_m r_d) r_{c2} + r_d$

case (iv) :



(1+gm rc) Rπ ||rd2

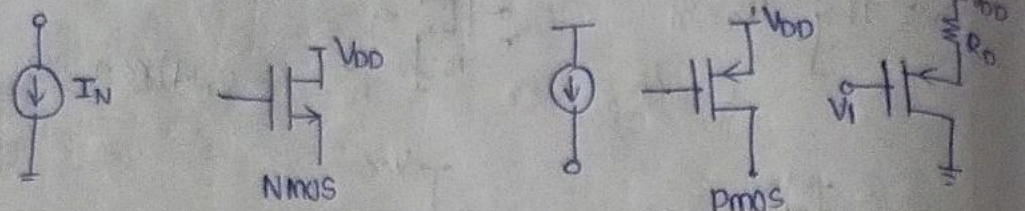


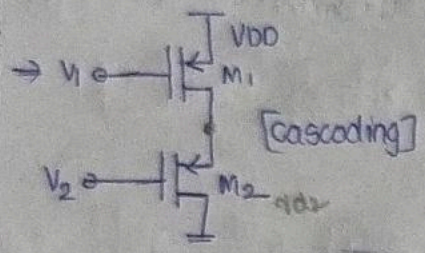
$R_o = (1+g_m r_c)(r_\pi \| r_{d_2}) + r_c$

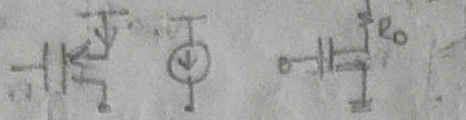
Need for current sources:-

* P-type Cascode Current Sources:

⇒

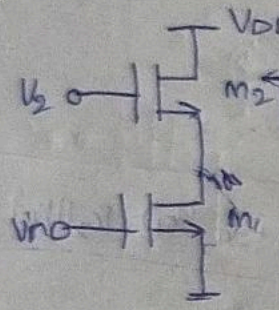






$(1+g_m r_{d1})\, r_{d2} + r_{d1}$

~~Introduction to Cascode Amplifiers~~



$$R_o = (1+g_m r_{d2})\, r_{d1} + r_{d2}$$

$g_m r_{d1} r_{d2}$

$g_m r_{d1} r_{d2}$

$$R_o = g_m r_{d2} r_{d1}$$

$g_m r_{d2} \gg 1$

$r_{d2} \ll g_m r_{d2} r_{d1}$

what happens to R_o if width is doubled if I_D is constant.

$$g_m = \sqrt{2 I_{D\max} \mu_n C_{ox} \frac{W}{L}}$$

if width doubled: $g_m' = \sqrt{2 I_{D\max} \mu_n C_{ox} \frac{2W}{L}}$

$$g_m' = \sqrt{2} \sqrt{2 I_{D\max} \mu_n C_{ox} W/L}$$

$$g_m' = \sqrt{2}\, g_m$$

$\sqrt{2}$

we have $R_o = g_m r_{d2} r_{d1}$

if width doubled, $R_{out}' = \sqrt{2}\, g_m r_{d2} r_{d1}$

$$R_{out}' = \sqrt{2}\, R_o$$

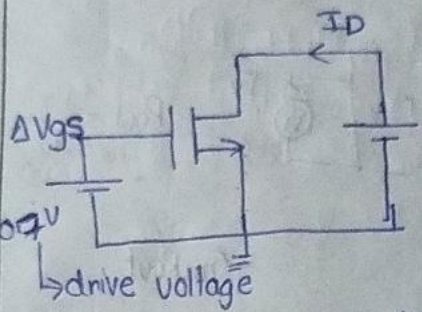
Introduction to Cascode Amplifiers:

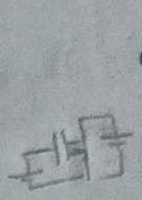
* To reduce complexity, cascode connections are used.

Gm - Alternate gm Analysis method

$$A_V = -G_m R_{out}$$

* To calculate Gm, short circuit the output terminal
* ideally able to damp

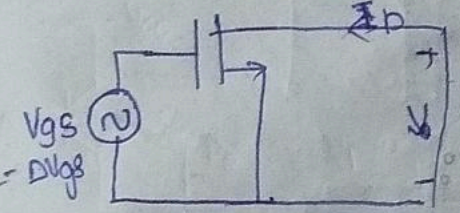


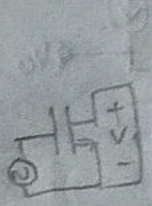


Gm

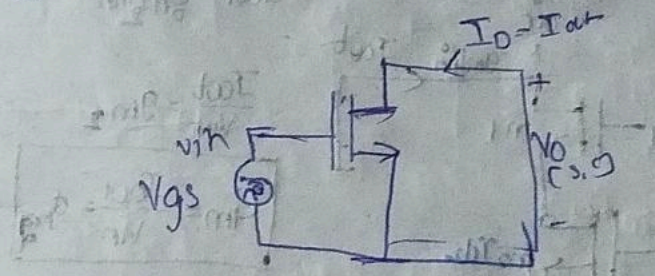
$V_{gs} \cong V_{th}$ → conduction mode, I_D varies $\frac{\partial I_D}{\partial V_{GS}}$

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$





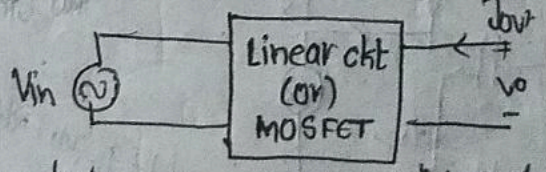
To find Gm, short circuit output terminal

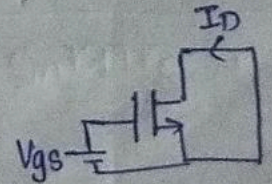


$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_{out}}{V_{in}}$$

$$I_{out} = g_m V_{in}$$

General Linear Circuits:-

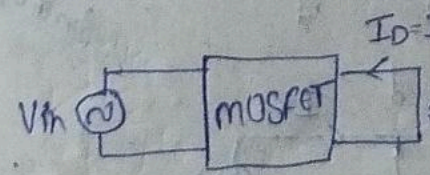




$$G_m \frac{\partial I_D}{\partial V_{GS}} = \frac{I_{out}}{V_{in}}$$

$$I_{out} = G_m V_{in}$$

Step: to find R_o, S.C output terminal.

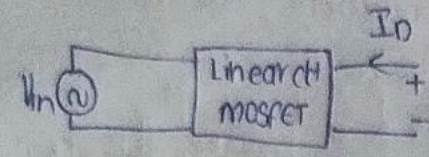


$$G_m = \frac{I_{out}}{V_{in}}$$

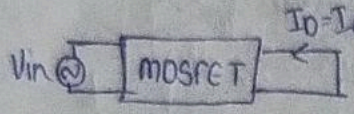
Voltage gain = $A_V = V_o/V_{in} = -g_m r_d$ → small signal gain.

Step

Step1 : Find Gm

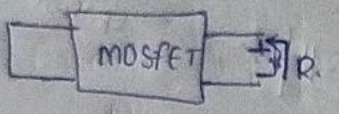


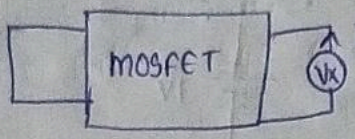
$A_V = \frac{V_o}{V_{in}}$



$= G_m = \frac{I_o}{V_{in}}$ $\quad I_o = G_m V_{in}$

Step2 : find Gm

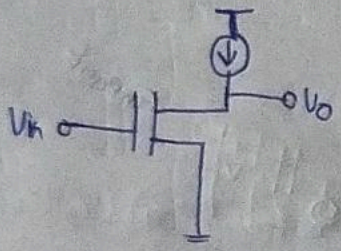


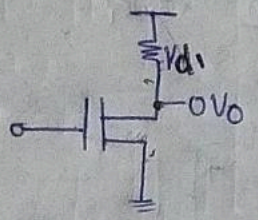


$R_{out} = \frac{V_x}{I_x}$

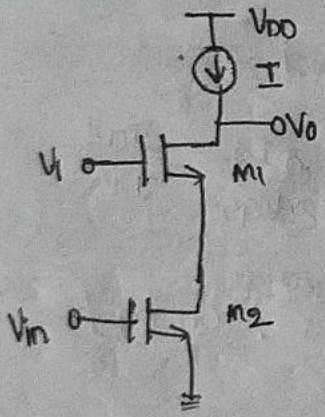
$A_V = -G_m R_{out}$ $\quad -G_m R_{out}$

Cascode Amplifier with Current source

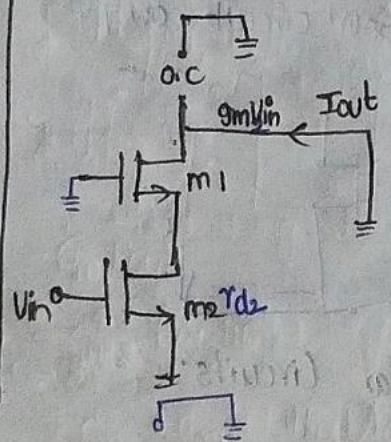




$A_V = -g_m r_d$



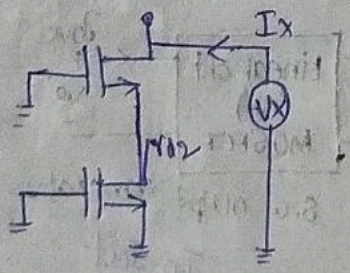
Find Gm :



$I_{out} = g_{m_2} V_{in}$

$\frac{I_{out}}{V_{in}} = g_{m_2}$

$G_m = \frac{I_{out}}{V_{in}} = g_{m_2}$

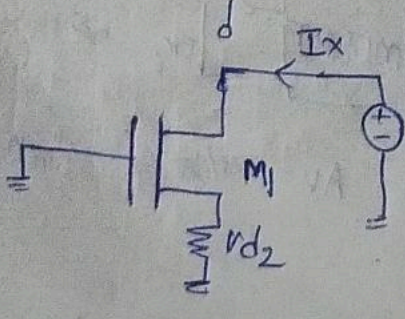


$(1+g_m r_{d_1}) r_{d_2}$

$r_{out} = g_m r_{d_1} r_{d_2}$

$(1+g_m r_{d_1}) r_{d_2} + r_{d_1}$

$g_m r_{d_1} r_{d_2}$



$R_o = (1+g_{m_1} r_{d_1}) r_{d_2} + r_{d_1}$

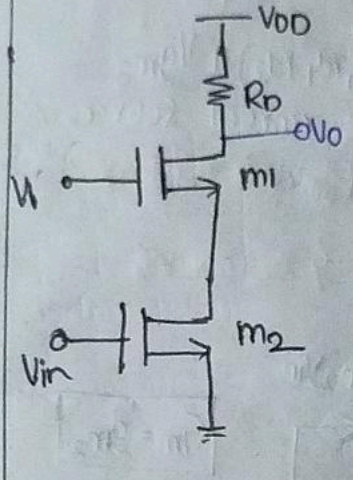
$R_o = g_{m_1} r_{d_1} r_{d_2}$

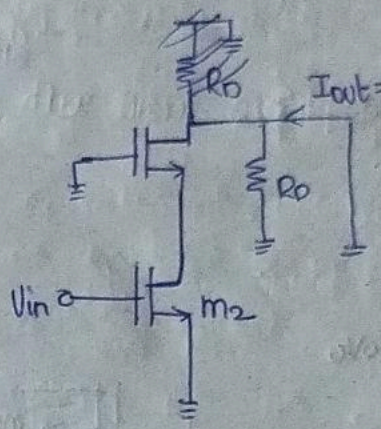
In cascoding

$A_V = -G_m R_{out}$

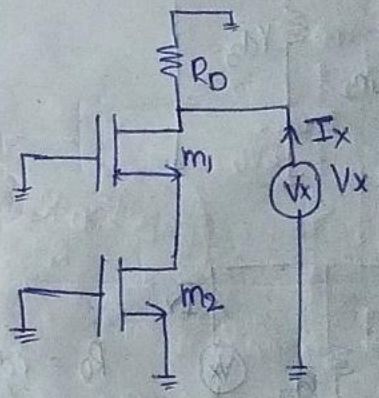
$A_V = -g_{m_2}[(1+g_{m_1}r_{d_1})r_{d_2} + r_{d_1}]$

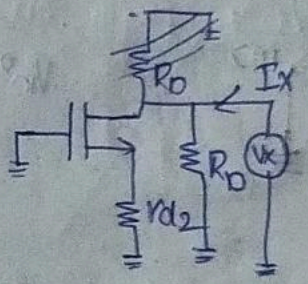
$A_V = -g_{m_2}[\underbrace{g_{m_1} r_{d_1} r_{d_2}}_{\text{Intrinsic gain}}]$





$G_m = \frac{I_{out}}{V_{in}} = g_{m_2}$





$R_O = [1+g_{m_1}(r_{d_1} \| R_D)]r_{d_2} + (r_{d_1} \| R_D)$

$R_O = g_{m_1}(r_{d_1} \| R_D)\, r_{d_2}$

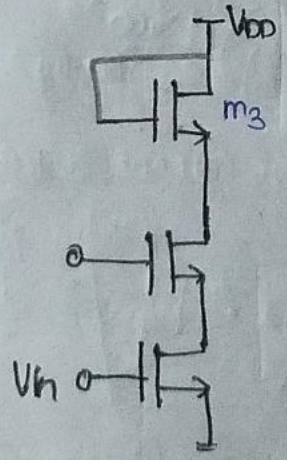
$(g_{m_1} r_{d_1} r_{d_2}) \| R_D$

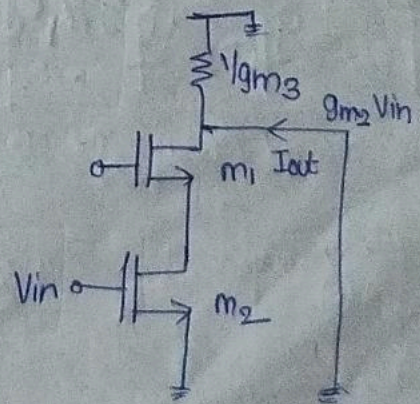
$A_V = -G_m R_{out}$

$A_V = -g_{m_2}[g_{m_1}(r_{d_1} \| R_D) r_{d_2}]$

Cascode Amplifier with diode connected device as load

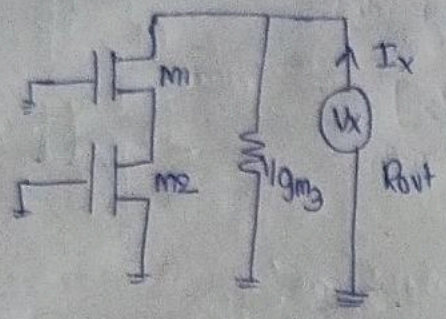
$\gamma = 0$





$G_m = g_{m_2}$

$(g_{m_1} r_{d_1} r_{d_2}) \| \frac{1}{g_{m_3}}$



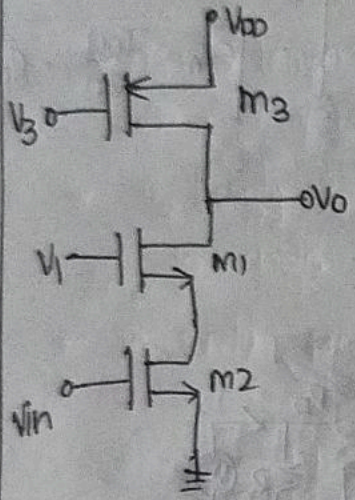
$R_o = 1/g_{m_3} \| R_{out}$

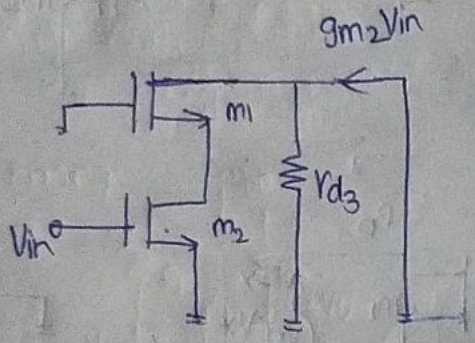
$R_{out} = g_{m_1} r_{d_1} r_{d_2}$

$- g_{m_2} (g_{m_1} r_{d_1} r_{d_2}) \| 1/g_{m_3}$

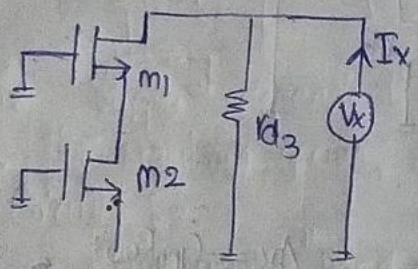
Cascode Amplifers usin with p type current sources As load

$- g_{m_2} (g_{m_1} r_{d_1} r_{d_2}) \| 1/g_{m_3}$





$G_m = g_{m_2}$



$R_o = r_{d_3} \| R_{out}$

$[1 + g_{m_1} (r_{d_3} \| R_{out})] r_{d_2} +$

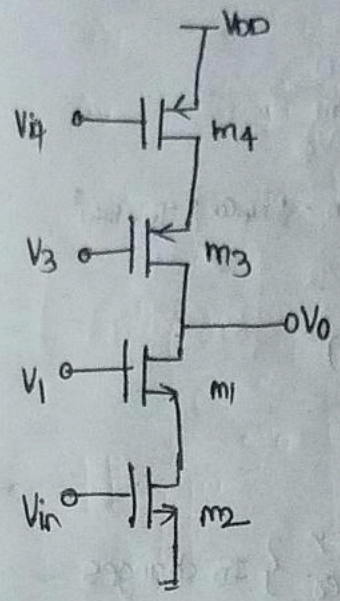
$g_{m_1} [r_{d_3} \| R_{out}] r_{d_2}$

$R_{out} \| r_{d_3}$

$A_v = - G_m R_{out}$

$A_v = - g_{m_2} (r_{d_3} \| R_{out})$

$\cdot - g_{m_2} g_{m_1} (r_{d_3} \| R_{out} \| r_{d_2}$



$G_m = +g_{m_2}$

$R_{out} = R_{out} \| r_{d_3} \| r_{d_4}$

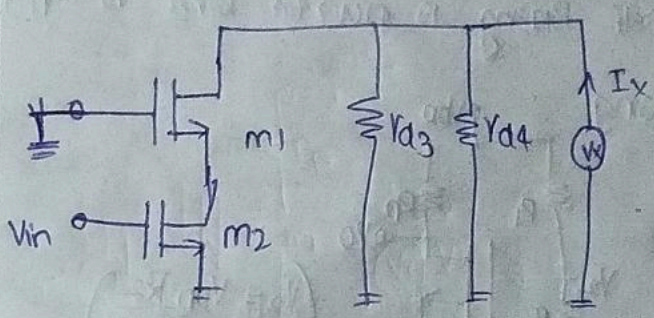
$G_m = -g_{m_2}$

$R_{out} = (g_{m_1} r_{d_1} r_{d_2}) \| r_{d_3} \| r_{d_4}$

$A_V = -G_m R_{out}$

$= -g_{m_2} (g_{m_1} r_{d_1} r_{d_2}) \| r_{d_3} \| r_{d_4}$

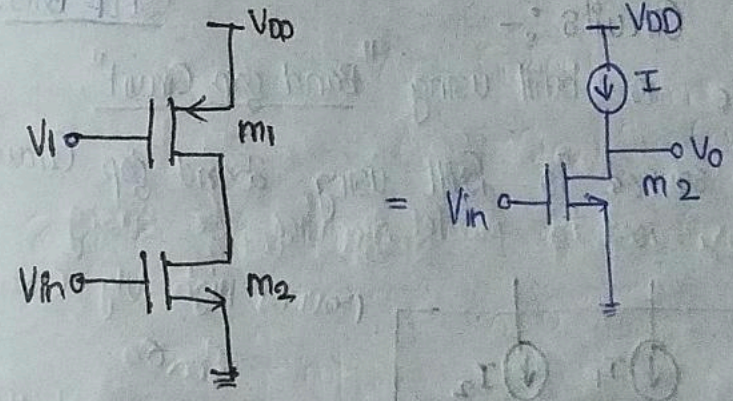
R_{out}

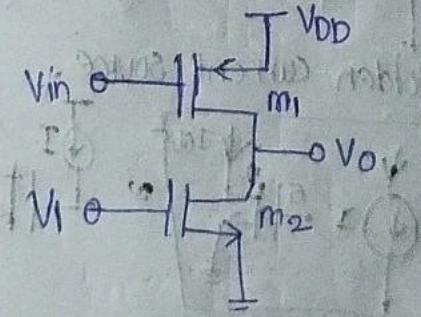


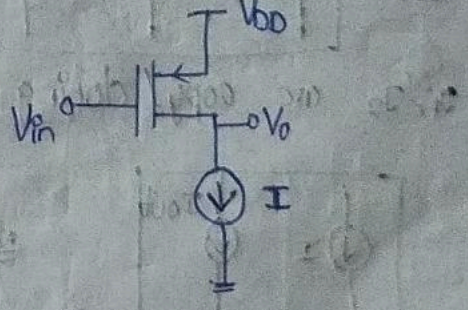
$R_{out} \| r_{d_3} \| r_{d_4}$

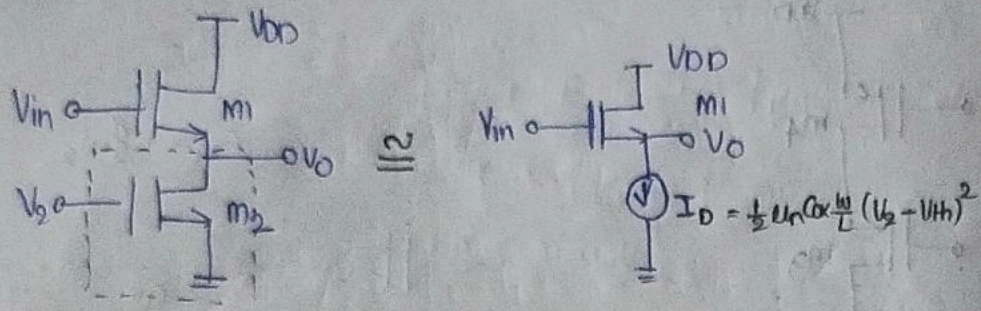
Need for Current Sources:-

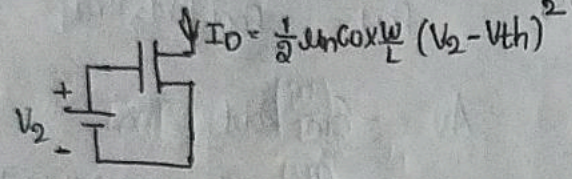
case(i)







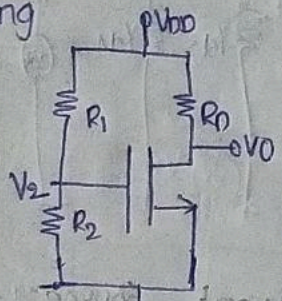




* μ_n → temperature dependent parameter
  V_{th} - temperature dependent parameter } I_D changes

* V_2 [V_{gs}] is supply dependent (V_{DD})
  to stable O.P self Biasing is provided which is supply dependent

* To supply proper biasing

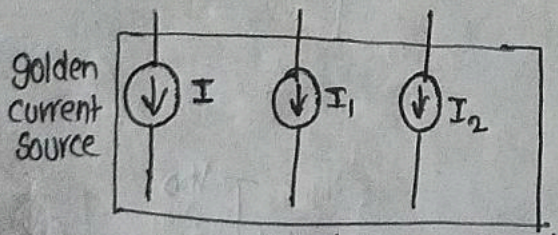


$\left(V_2 = V_{DD}\frac{R_2}{R_1+R_2}\right)$

Here V_2 is supply dependent
V_2 (overdrive vtg) for stabilizing operating point generated by "SELF BIAS".

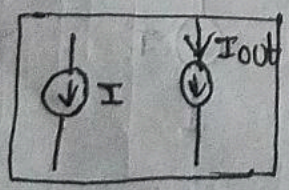
Current mirror Circuits :-

* A current source is built using "Band gap Circuit".
* A golden current source is built using Band gap Circuits
* Current mirrors are used in MOSfet Amplifier for Biasing

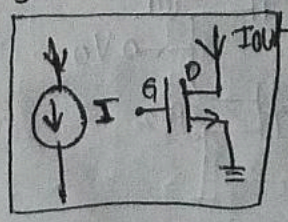


provides High, Vtg Gain
Error ≈ 0
improves Biasing Stability

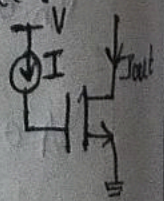
I_1, I_2 are copy / cloning of golden current source.

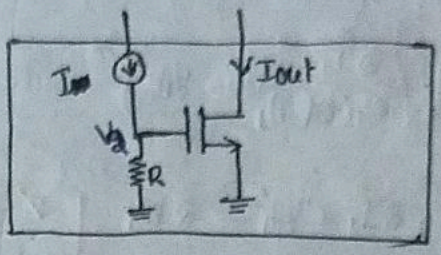


≅



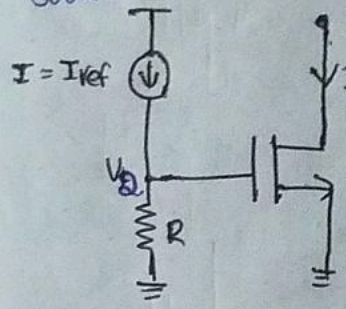
≅





Constant

* Let us build a constant current source using Band gap circuits
* we copy / clone this current source to built many other current sources



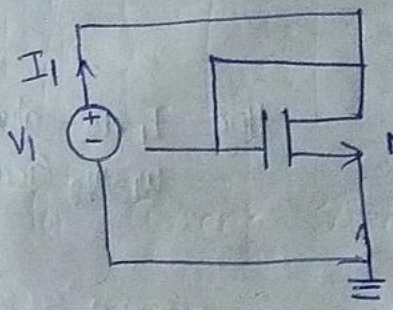
$I_{out} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_2 - V_{th})^2$

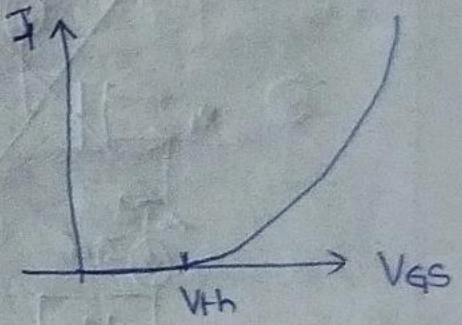
$I_{out} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(I_{ref}R - V_{th})^2$

↓

temperature dependent Resistors

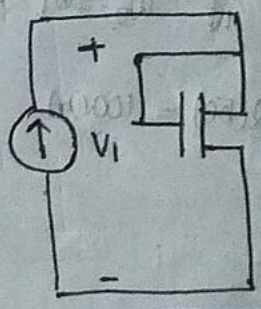
case i: diode connected device

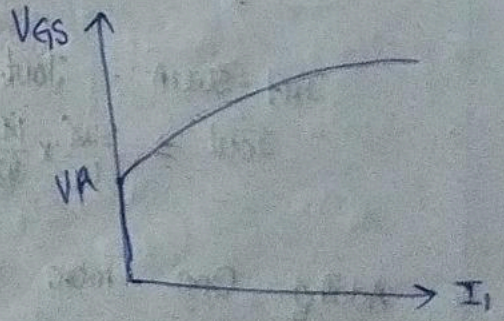




$I_1 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_1 - V_{th})^2$

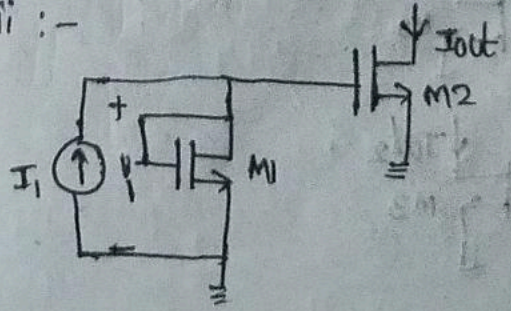
case ii :-

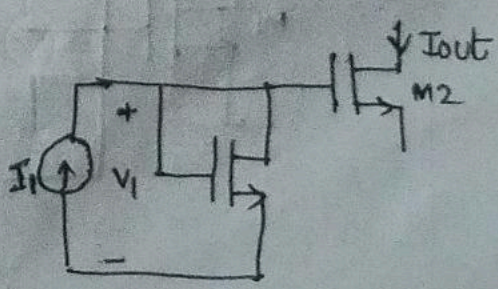




$$V_1 = \sqrt{\frac{2I_1}{\mu_n C_{ox}(W/L)_1}} + V_{th}$$

case iii :-





Iout =

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_1 - V_{th})^2$$

$$= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 \left[\sqrt{\frac{2I_1}{\mu_n C_{ox}(W/L)_1}} + V_{th} - V_{th}\right]^2$$

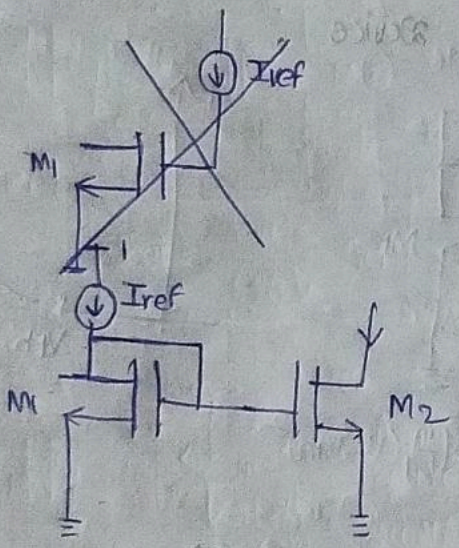
$$= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 \left[\frac{2I_1}{\mu_n C_{ox}(W/L)_1}\right]$$

$$I_{out} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} I_1$$

$$I_1 = I_{ref}$$

$$\boxed{I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{ref}}$$

Flipping :

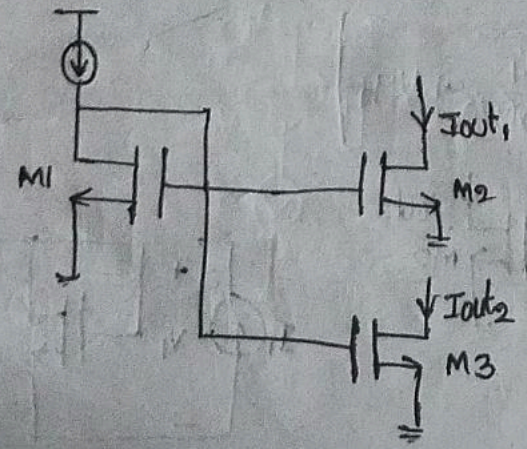


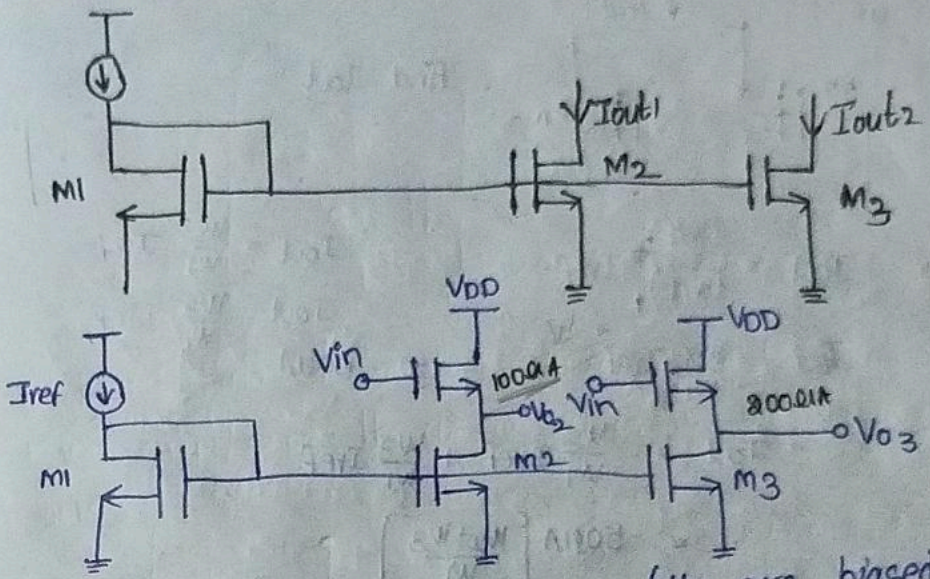
Here $L_1 = L_2$ = always
$W_1 = W_2$ (accordingly)

$I_{ref} = 50\mu A$ $I_{out} = 100\mu A$? if $W_2 = 2W_1$ $L_1 = L_2$ then $I_{out} = 100\mu A$

$$I_{out} = \frac{2W_1}{L_1} \times \frac{L_1}{W_1} [50] = 2(50) = 100\mu A$$

Adding One more stage :





A circuit includes 2 source followers biased at 100μAmps and 200μAmp. we have reference current of 50μA find width ratio of two source followers.

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{ref}$$

$$I_{out} = \frac{W_2}{W_1} I_{ref}$$

~~100μA = $\frac{W_1}{W_2}$ 50ref~~

$$100\mu A = \frac{2W_1}{W_1} 50$$

$$= 100\mu A$$

$$\frac{W_2}{W_1} =$$

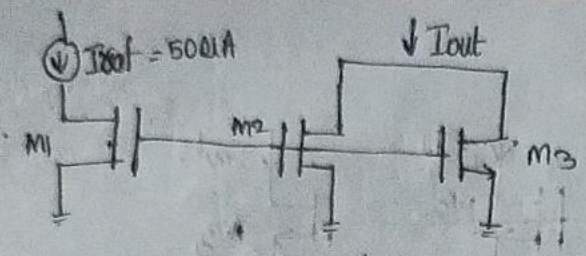
$$W_2 : W_1 = 2 : 1$$

$$200\mu A = \frac{W_3}{W_2} 50$$

$$= 4:1$$

$$W_3 : W_2 = 4:1$$

$W_1 : W_2$
1 : 2
$W_2 : W_3$
1 : 4



Find Iout.

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{ref}$$

$$I_{out} = \frac{W_2}{W_1} I_{ref}$$

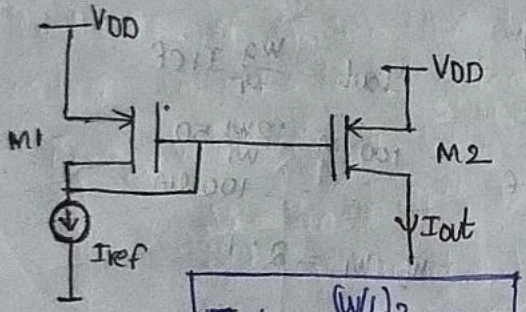
$$I_{out} = \frac{W_3}{W_1} I_{ref}$$

$$I_{out} = \frac{W_2}{W_1} I_{ref} \qquad \frac{2}{1} \times 50 = 100\mu A$$

$$I_{out} = \frac{W_2}{W_1} I_{ref} + \frac{W_3}{W_1} I_{ref}$$

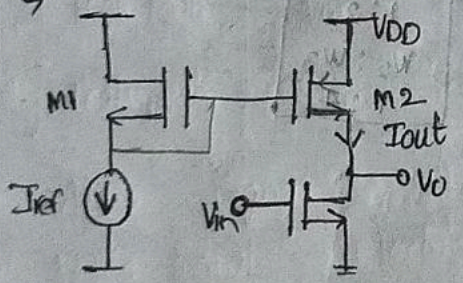
$$= 50\mu A \left[\frac{W_2 + W_3}{W_1}\right]$$

P type Current Mirrors



$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{ref}$$

Q)



An NMOS common source stage requires a load current source equal to 200μA we Iref = 400μA. Find the width ratio.

$L_1 = L_2$

$$I_{out} = \frac{W_2}{W_1} I_{ref}$$

$$200 = \frac{W_2}{W_1} 400$$

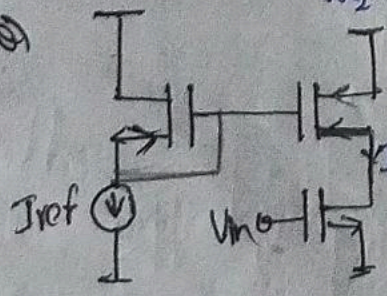
$$\frac{1}{2} = \frac{W_2}{W_1}$$

$$W_2 : W_1 = 1 : 2$$

$* W_2 : W_1 = 0.5 \qquad * W_2 = 0.5 W_1$

$$W_1 : W_2 = 2 : 1$$

Q)



$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{ref}$$ if L

$\frac{W_2}{W_1} = ?$

$$\frac{I_{ref}}{2} = \frac{W_2}{W_1} I_{ref}$$

$$\frac{(W/L)_2}{(W/L)_1} = \frac{1}{2} \qquad \frac{(W/L)_1}{(W/L)_2} = \frac{2}{1}$$

Q) if $I_{ref} = \frac{I_{ref}}{2}$ $I_{out} = 2I_{ref}$ then width ratio

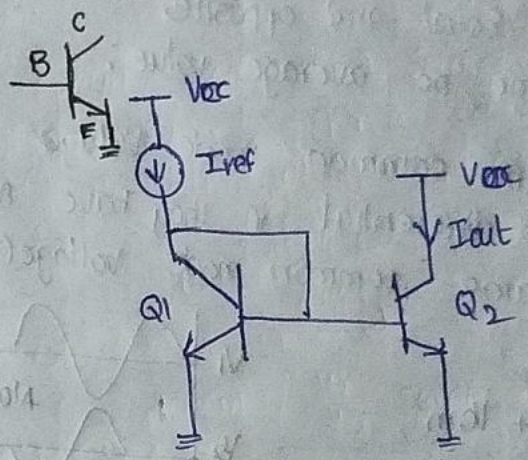
$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{ref}$$

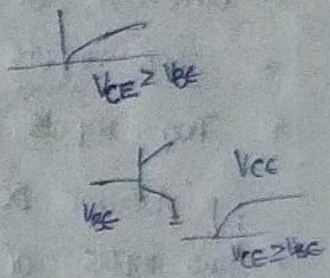
$$2I_{ref} = \frac{(W/L)_2}{(W/L)_1} \frac{I_{ref}}{2}$$

$$\frac{(W/L)_2}{(W/L)_1} = \frac{4}{1} \qquad (W/L)_1 : (W/L)_2 = 1:4$$

BJT CURRENT MIRROR CIRCUITS

CE - power gain high, signal out of phase.





① when transistor in forward region

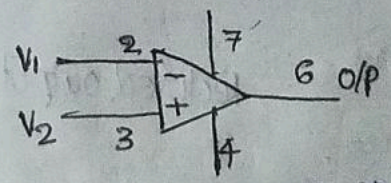
$$I_{C_2} = I_{S_2} e^{\frac{V_{BE}}{V_T}}$$ [In Active region (Reverse Bias)]

I_S - saturation Current
↳ Reverse

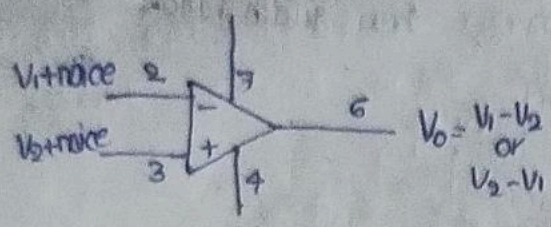
$$I_{C_1} = I_{S_1} e^{Vee/V_T}$$

$$\boxed{\frac{I_{C_2}}{I_{C_1}} = \frac{I_{S_2}}{I_{S_1}}}$$

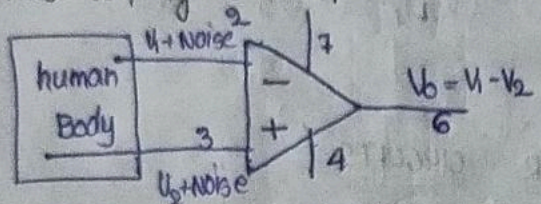
DIFFERENTIAL AMPLIFIER CIRCUITS

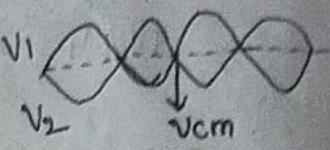


* Using common CS, CD, CC, there will be Noise carried from input to output [Noise cannot be rectified]
* Noise can be rectified using filters, Noise removing components.
* Differential Amplifiers are used to rectify Noise without using any noise removal components.



noise coupling : ECG - Electro Cardio Graphy



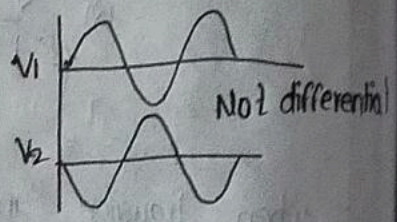


* Difference of two inputs gives differential output
* Two inputs must be Equal and opposite
* Two inputs have same DC average value.

Average DC value = V_{cm} = common mode voltage

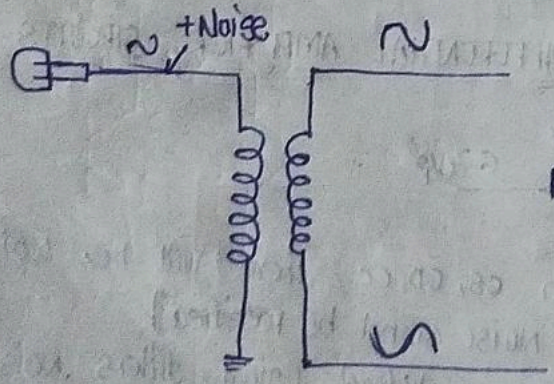
* Two inputs of OP-Amp are differential if they have equal & opposite voltage & have same common mode voltage (V_{cm})
* From value of V_1, V_2

$$V_1 = V_m \sin \omega t + V_{cm}$$
$$V_2 = -V_m \sin \omega t + V_{cm}$$



Peak value	V_1	V_2	$V_1 - V_2$
Peak-~~Peak~~	V_m	$-V_m$	$V_m - (-V_m) = 2V_m$
Peak-peak	$2V_m$	$-2V_m$	$2V_m - (-2V_m) = 4V_m$

* Audio signal - 20Hz to 20kHz
* Voice signal → Electrical signal [microphone]



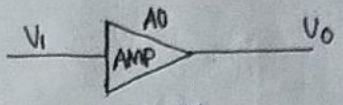
Case (i) :-

when single stage used, noise carried by input is also carried to output which doesn't get rectified output.

* To acheive this, another secordary transformer which carries two differential input signals, thus the output can be noise free

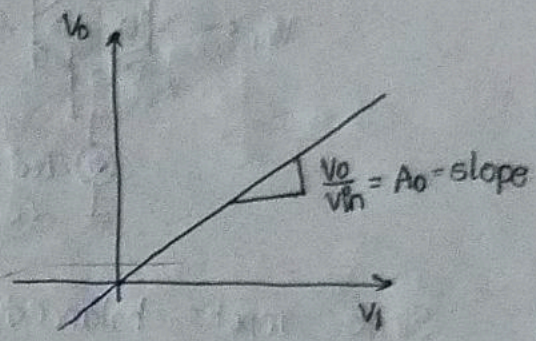
$$V_o = V_1 - V_2$$

case (i):



$$V_1 A_O = V_o$$

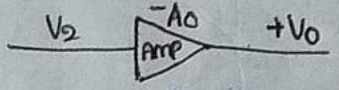
$$\boxed{A_O = \frac{V_o}{V_1}}$$



here we get linear graph

$$\boxed{\text{slope} = \text{Gain} = A_O}$$

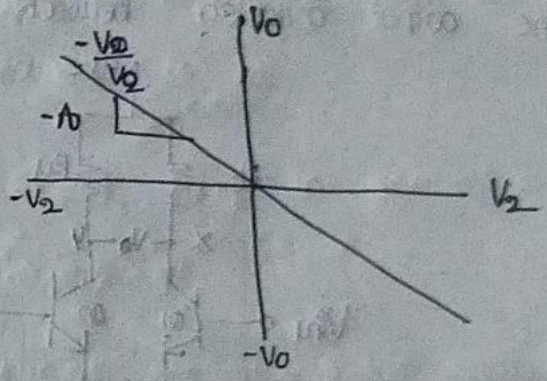
case (ii):



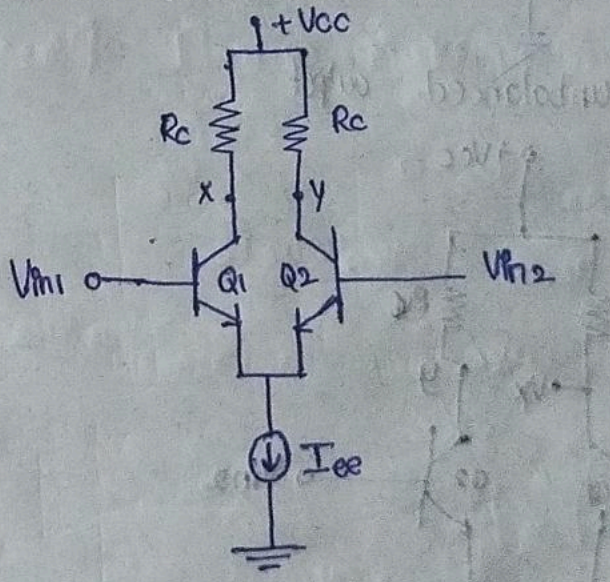
$$-A_O V_2 = V_O$$

$$A_O = \frac{-V_o}{V_2}$$

$$\text{slope} = \text{Gain} = A_O = \frac{-V_o}{V_2}$$



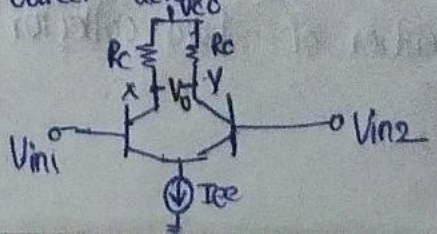
BJT DIFFERENTIAL AMPLIFIERS



Type of Differential Amplifiers:

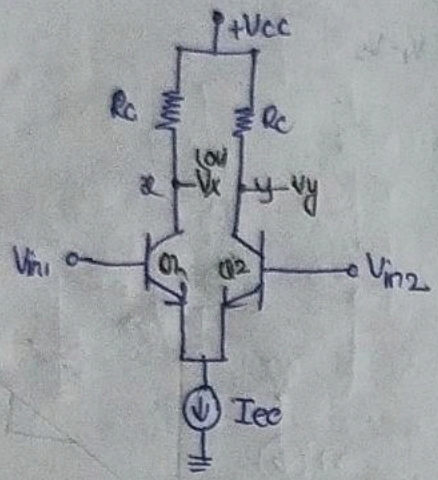
1) Dual Input Balanced Output differential Amplifier

output collect across two collector terminals.



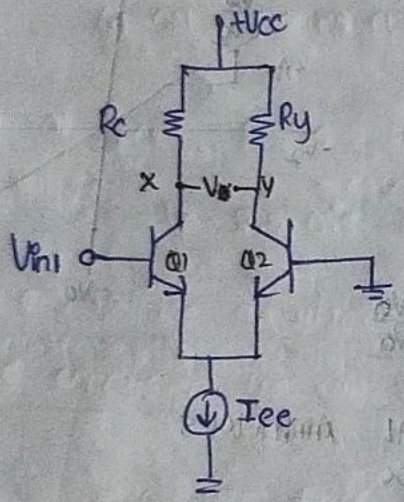
8) Dual input unbalanced output

output collected across either of two collector terminals(x,y)

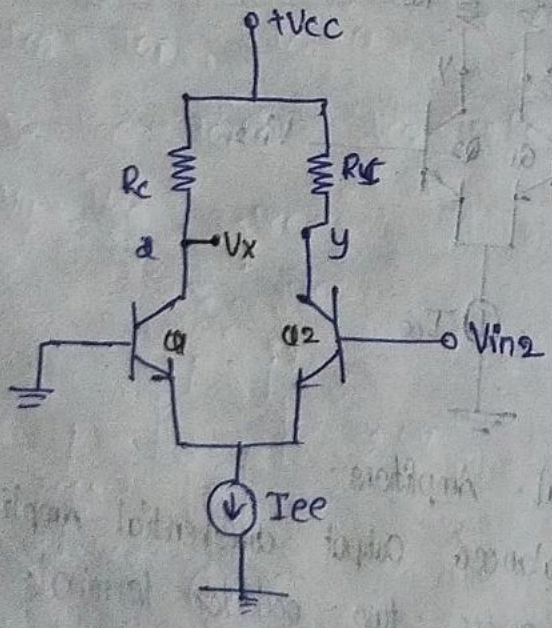


3) Single input balanced output

the output collected between two collectors terminals



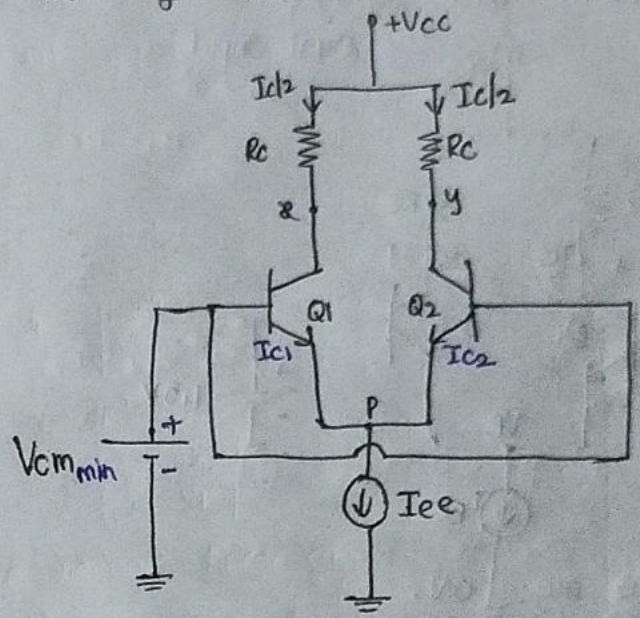
4) Single input unbalanced output



output collected at either of two collector termals.

Here Both Base terminals are short circuited & connected to Vcm.

case(i)



case(i) : Apply KCL at node P,

$$I_{ee} = I_{c_1} + I_{c_2}$$

since both transistors are identical

$$I_{c_1} = I_{c_2} = \frac{I_{ee}}{2}$$

Voltage across Rc (V) = IR = $\frac{I_{ee}}{2} R_c$.

Voltage across "x" point = $V_{cc} - V_{Rc}$

$$V_x = V_{cc} - \frac{I_{ee}}{2} R_c = V_y$$

$$V_x = V_y = V_{cc} - \frac{I_{ee}}{2} R_c$$

* If $V_{in1} - V_{in2} = 0$ then $V_x - V_y = 0$

Here V_{in1}, V_{in2} - differntial inputs

V_{o1}, V_{o2} - differential outputs

* Vcmmin is got Rejected by differential Amplifiers.

[common mode values]

Vcm - distoubances - pertubutation.

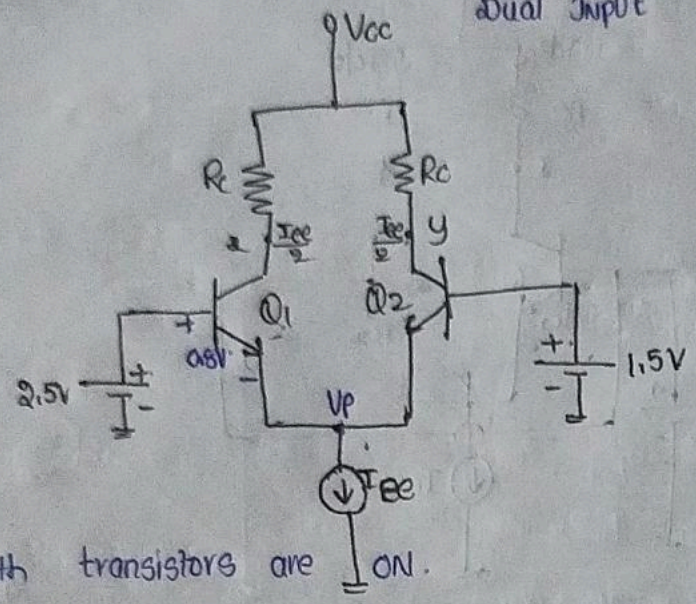
when $R_c + \Delta R$

then $V_x = V_{cc} - \frac{I_{ee}}{2} R_c$

$$V_y = V_{cc} - \frac{I_{ee}}{2}(R_c + \Delta R)$$

case ii) when different Base voltages

Dual Input



* wBoth transistors are ON.

⇒ Assume the trainstor Q1 is in condution mode.

Q1-ON [some current flows]

⇒ Voltage at point P is

$$V_p = 2.5 - 0.8 = 1.7V$$

⇒ from above, voltage available across emitter terminals are 1.7V

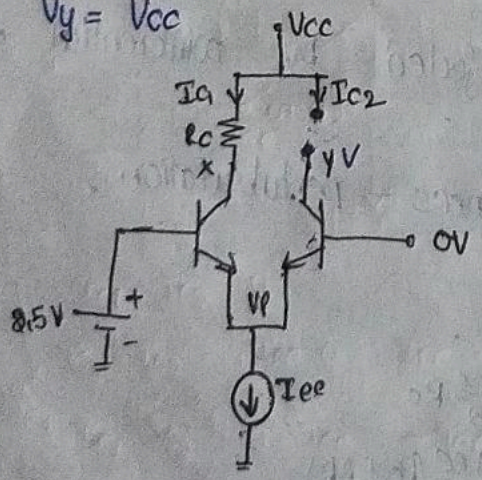
⇒ from above conclusion, we can say transistor Q2 in non conducting mode

∴ Q2-OFF [zero current] ∵[$V_{in_2} < V_p$]

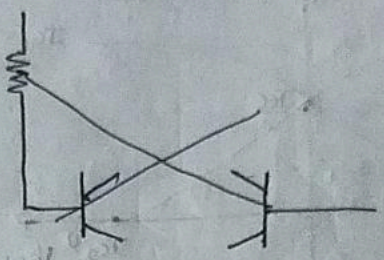
* $I_{ee} = I_{c_1}$ $I_{c_2} = 0$

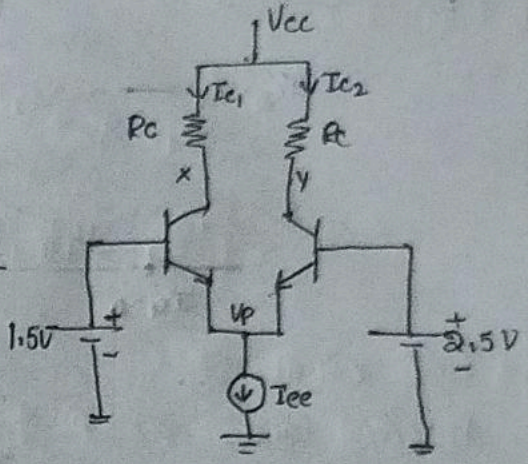
$V_x = V_{cc} - I_{c_1} R_c = V_{cc} - I_{ee} R_c$

$V_y = V_{cc}$



case (iii)





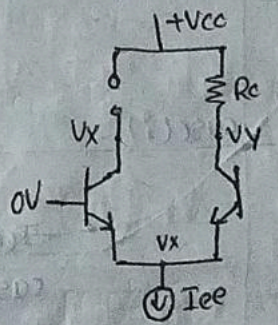
let Q_2 is in ON condition

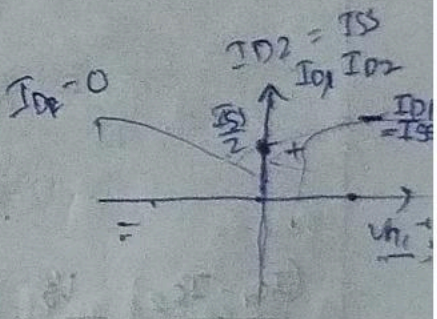
$\therefore V_p = 2.5 - 0.8 = 1.7V$

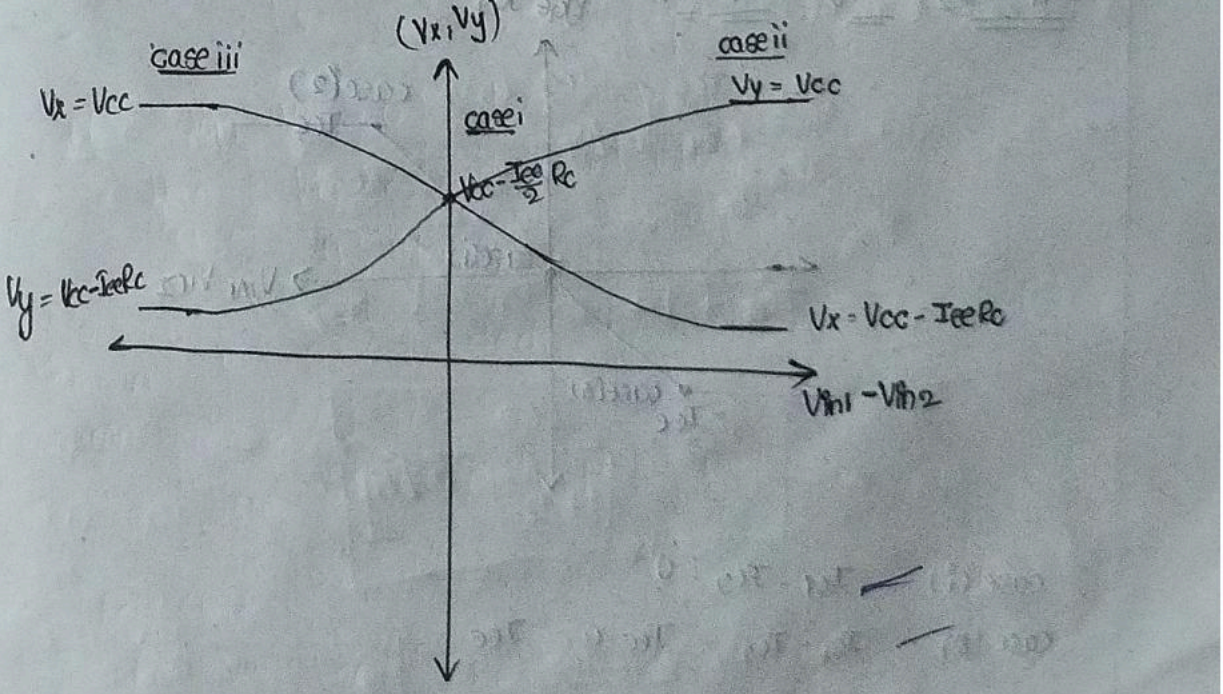
thus Q_1 is in OFF condition [$\because V_{in1} < V_p$]

$I_{C_1} = 0$

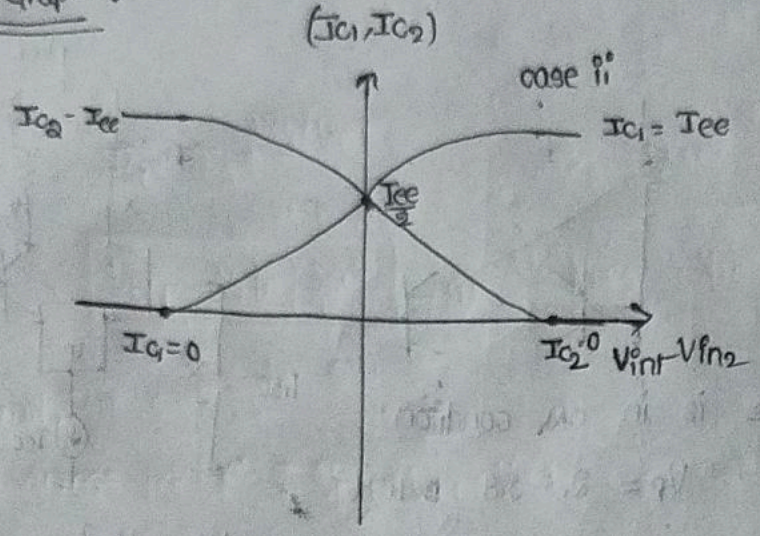
* $I_{C_2} = I_{ee}$
* $V_x = V_{cc}$ $\quad V_y = V_{cc} - I_{C_2}R_c = V_{cc} - I_{ee}R_c$



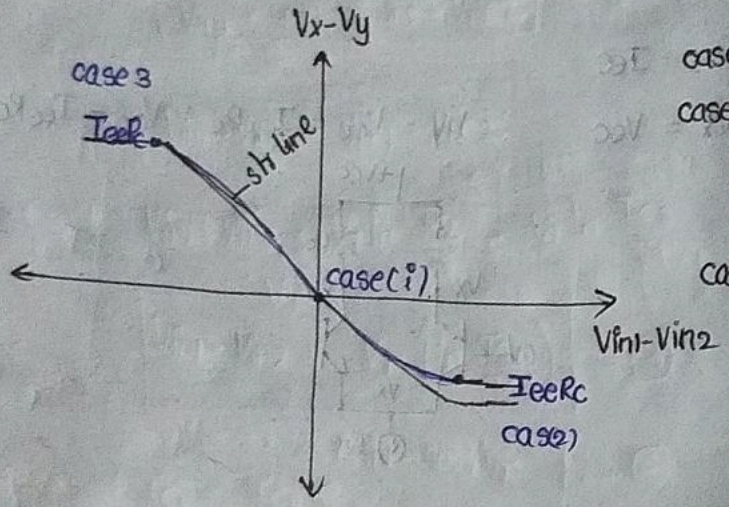




Current Graph :



(Vx - Vy) Vs Vin1 - Vin2 :



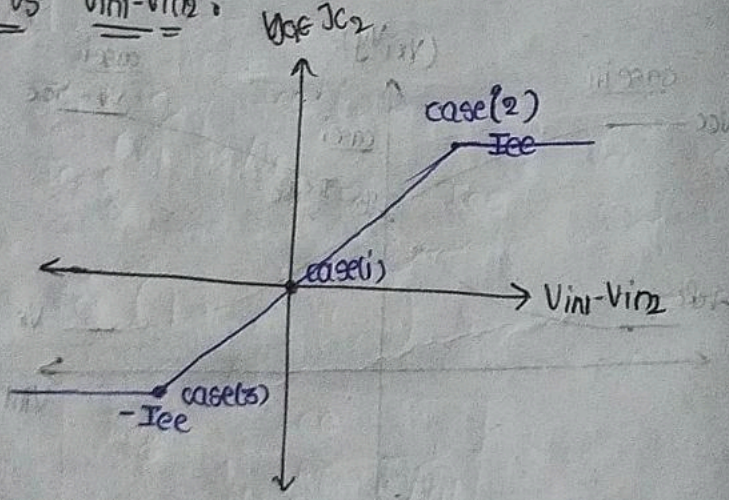
case i) Vx - Vy = 0

case ii) Vx - Vy = Vcc - IeeRc - Vcc

Vx - Vy = - IeeRc

case iii) Vx - Vy = + IeeRc

(Ic1 - Ic2) Vs Vin1 - Vin2 :



case (i) = $I_{c1} - I_{c2} = 0$

case (2) = $I_{c1} - I_{c2} = I_{ee} - 0 = I_{ee}$

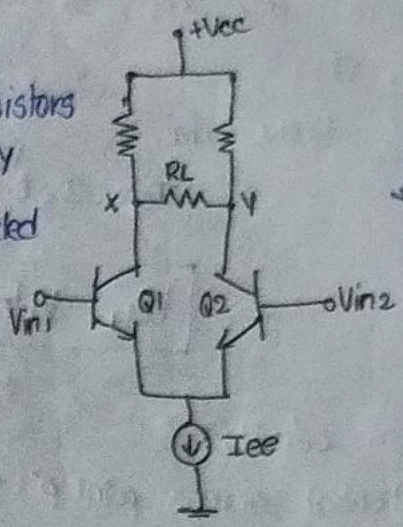
Case (3) = $I_{c1} - I_{c2} = 0 - I_{ee} = -I_{ee}$

case (i):

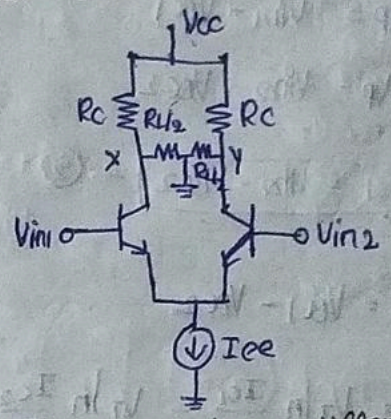
Consider two Identical transistors

R_L is connected between x & y

* analysis cote possible, since connected directly two main nodes

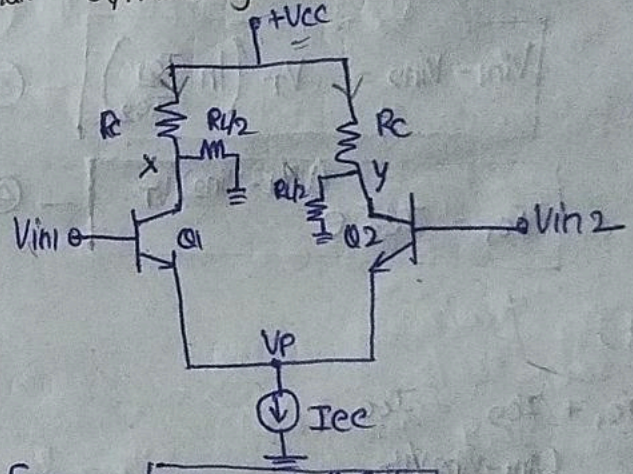


case (ii): Half differential circuit



R_L divided as $R_L/2$, $R_L/2$ since both are identical.

case (iii): Half symmetry differential circuit



Both are identical

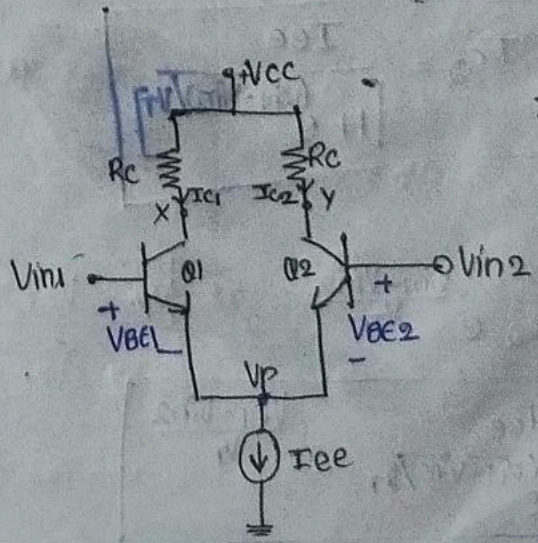
$R_L/2$ at x $R_L/2$ at y

here $R_{out} = R_c \parallel R_L/2$

we have $A_v = -g_m R_c$

$$A_v = -g_m (R_c \parallel R_L/2)$$

case (iv):



$I_{C_1} = \frac{I_{ee}}{2}$

$I_{C_2} = \frac{I_{ee}}{2}$

} Q1 Q2 identiacal

Derive I_{C_1}, I_{C_2}, V_x, V_y and $V_x - V_y$ in terms of input voltages $(V_{in1} - V_{in2})$

⇒ we know that

$$I_{C_1} = I_S e^{V_{BE_1}/V_T} \qquad I_{C_2} = I_S e^{V_{BE_2}/V_T}$$

$$\boxed{V_{BE_1} = V_T \ln\left(\frac{I_{C_1}}{I_S}\right)} - (1) \qquad \boxed{V_{BE_2} = V_T \ln\left(\frac{I_{C_2}}{I_S}\right)}$$

* From circuit,

Potential across point P : $V_p = V_{in1} - V_{BE1}$

also $V_p = V_{in2} - V_{BE2}$

$$\boxed{V_{in1} - V_{BE1} = V_{in2} - V_{BE2}} - (2)$$

$$V_{in1} - V_{in2} = V_{BE1} - V_{BE2}$$

$$V_{in1} - V_{in2} = V_T \ln \frac{I_{C_1}}{I_S} - V_T \ln \frac{I_{C_2}}{I_S}$$

$$\boxed{V_{in1} - V_{in2} = V_T \left(\ln \frac{I_{C_1}}{I_{C_2}}\right)} - (3)$$

$$\boxed{I_{C_1} = I_{C_2} e^{(V_{in1} - V_{in2})/V_T}} - (4)$$

* From circuit,

$$I_{C_1} + I_{C_2} = I_{ee}$$

$$I_{C_2} e^{(V_{in1} - V_{in2})/V_T} + I_{C_2} = I_{ee}$$

$$I_{C_2}\left(1 + e^{\frac{V_{in1} - V_{in2}}{V_T}}\right) = I_{ee}$$

$$\boxed{I_{C_2} = \frac{I_{ee}}{\left[1 + e^{(V_{in1} - V_{in2})/V_T}\right]}}$$

$$I_{C_1} = I_{C_2} e^{\frac{V_{in1} - V_{in2}}{V_T}}$$

$$\boxed{I_{C_1} = \frac{I_{ee}}{1 + e^{(V_{in1} - V_{in2})/V_T}} e^{\frac{V_{in1} - V_{in2}}{V_T}}}$$

$V_x = V_{cc} -$

$$I_{c_2} = \frac{I_{ee}}{e^{(V_{in1}-V_{in2})/V_T}\left[1+\frac{1}{e^{(V_{in1}-V_{in2})/V_T}}\right]}$$

$$I_{c_1} = \frac{I_{ee}}{1+e^{(V_{in2}-V_{in1})/V_T}} \qquad I_{c_2} = \frac{I_{ee}}{1+e^{(V_{in1}-V_{in2})/V_T}}$$

if Q1 Q2 are identical,

$$V_{in1} - V_{in2} = \frac{I_{ee}}{2}$$

$$I_{c_1} = \frac{I_{ee}}{1+e^{\frac{-I_{ee}}{2V_T}}} \qquad I_{c_2} = \frac{I_{ee}}{1+e^{\frac{I_{ee}}{2V_T}}}$$

$V_{in1} + V_{in2}$

$I_{C1} + I_{C2} = I_{ee}$

$I_{c_1} = \frac{I_{ee}}{1+e^{\frac{V_{in1}-V_{in2}}{V_T}}}$

$I_{c_2} = \frac{I_{ee}}{1+e^{\frac{V_{in2}-V_{in1}}{V_T}}}$

$$I_{c_1} = \frac{I_{ee}}{1+e^{(V_{in2}-V_{in1})/V_T}} = \frac{2(V_{in1}+V_{in2})}{1+e^{\frac{V_{in2}-V_{in1}}{V_T}}}$$

$$I_{c_2} = \frac{I_{ee}}{1+e^{(V_{in1}-V_{in2})/V_T}} = \frac{2(V_{in1}-V_{in2})}{1+e^{(V_{in1}-V_{in2})/V_T}}$$

$V_{in_1} - V_{in_2}$;

$V_x = V_{cc} - I_{c_1} R_c \qquad V_y = V_{cc} - I_{c_2} R_c$

$$V_x = V_{cc} - \frac{I_{ee} R_c}{1+e^{(V_{in2}-V_{in1})/V_T}}$$

$$V_y = V_{cc} - \frac{I_{ee} R_c}{1+e^{(V_{in1}-V_{in2})/V_T}}$$

$$V_x - V_y = V_{cc} - I_{c_1} R_c - V_{cc} + I_{c_2} R_c$$

$$V_x - V_y = R_c\left[I_{c_2} - I_{c_1}\right]$$

$$V_x - V_y = R_c\left[\frac{I_{ee}}{1+e^{(V_{in1}-V_{in2})/V_T}} - \frac{I_{ee}}{1+e^{(V_{in2}-V_{in1})/V_T}}\right]$$

$$V_x - V_y = I_{ee} R_c\left[\frac{1}{1+e^{\frac{V_{in1}-V_{in2}}{V_T}}} - \frac{1}{1+e^{(V_{in2}-V_{in1})/V_T}}\right]$$

$$V_x - V_y = -I_{ee}R_c \left[\frac{1}{1+e^{(V_{in1}-V_{in2})/V_T}} - \frac{1}{e^{(V_{in2}-V_{in1})/V_T}+1}\right]$$

$$V_x - V_y = -I_{ee}R_c \left[\frac{1}{1+e^{(V_{in1}-V_{in2})/V_T}} - \frac{e^{(V_{in1}-V_{in2})/V_T}}{1+e^{(V_{in1}-V_{in2})/V_T}}\right]$$

$$V_x - V_y = -I_{ee}R_c \frac{1-e^{\frac{V_{in1}-V_{in2}}{V_T}}}{1+e^{\frac{V_{in1}-V_{in2}}{V_T}}}$$

$$= -I_{ee}R_c \frac{1-e^{\frac{-I_{ee}}{2V_T}}}{1+e^{-I_{ee}/2V_T}}$$

$$= -I_{ee}R_c \frac{1-e^{-2\frac{I_{ee}}{4V_T}}}{1+e^{-2\frac{I_{ee}}{4V_T}}}$$

$$\boxed{V_x - V_y = -I_{EE}R_c \tanh\left(\frac{I_{ee}}{4V_T}\right)}$$

$\frac{e^x - e^{-x}}{e^x + e^{-x}}$

$\frac{e^{2x}-1}{e^{2x}+1}$

$V_{in1} - V_{in2} = c$

$V_{in2} - V_{in1} = \frac{I_{ee}}{2}$

$\tanh\theta = \frac{1-e^{-2\theta}}{1+e^{2\theta}}$

$$V_x - V_y = -I_{ee}R_c \tanh\left(\frac{V_{in1}-V_{in2}}{2V_T}\right)$$

$\frac{1}{\infty}$

Case(1)

$$I_{C_2} = \frac{I_{ee}}{1+e^{\frac{V_{in1}-V_{in2}}{V_T}}}$$

$$I_{C_1} = \frac{I_{ee}}{1+e^{-(V_{in1}-V_{in2})/V_T}}$$

Case i)

$V_{in1} = V_{in2}$ $\quad I_{C_2} = I_{ee}/2$

$I_{C_1} = I_{ee}/2$

Case ii) $V_{in1} - V_{in2}$ very large (+Ve)

$$I_{C_2} = \frac{I_{ee}}{1+e^{\infty}} = \frac{1}{\infty} = 0$$

$V_x = V_{cc} - I_{C_2}R_c$

$\boxed{V_x = V_{cc} - I_{ee}R_c}$

$$I_{C_1} = \frac{I_{ee}}{1+e^{-\infty}} = I_{ee}$$

one of transistor is in OFF condition

Case iii) $V_{in} - V_{in2} \Rightarrow -Ve$

$$I_{C_2} = \frac{I_{ee}}{1+e^{-\infty}} = I_{ee}$$

$\boxed{V_x = V_{cc} - I_{C_2}R_c}$

$$I_{C_1} = \frac{I_{ee}}{\infty} = 0$$

$\boxed{V_y = V_{cc} - I_{ee}R_c}$

Also says one of transistor is in OFF condition.

$$V_x - V_y = V_{cc} - I_{ee}R_c - V_{cc} + I_{ee}R_c = 0$$

$$V_x - V_y = V_{cc} - I_{c_1}R_c - V_{cc} + I_{c_2}R_c$$

$$= R_c\left[-I_{c_1} + I_{c_2}\right]$$

$$= R_c \frac{-I_{ee}}{1+e^{\frac{V_{in2}-V_{in1}}{V_T}}} + \frac{+I_{ee}}{1+e^{\frac{V_{in1}-V_{in2}}{V_T}}}$$

$$= -I_{ee}R_c\left[\frac{1}{1+e^{\frac{V_{in2}-V_{in1}}{V_T}}} - \frac{1}{1+e^{\frac{(V_{in1}-V_{in2})}{V_T}}}\right]$$

$$= -I_{ee}R_c\left[\frac{1}{1+\frac{1}{e^{\frac{V_{in1}-V_{in2}}{V_T}}}} - \frac{1}{1+e^{\frac{V_{in1}-V_{in2}}{V_T}}}\right]$$

$$= -I_{ee}R_c\left[\frac{e^{\frac{V_{in1}-V_{in2}}{V_T}} - 1}{e^{\frac{V_{in1}-V_{in2}}{V_T}} + 1}\right]$$

$$= -I_{ee}R_c \frac{1-e^{-\frac{(V_{in1}-V_{in2})}{V_T}}}{1+e^{-\frac{(V_{in1}-V_{in2})}{V_T}}}$$

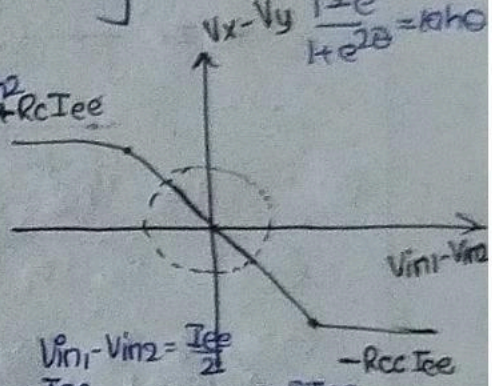
$V_{in1} - V_{in2} = \frac{I_{ee}}{2}$

$$= \frac{1-e^{-\frac{I_{ee}}{2V_T}}}{1+e^{-\frac{I_{ee}}{2V_T}}} = \frac{1-e^{-\frac{2I_{ee}}{4V_T}}}{1+e^{-\frac{2I_{ee}}{4V_T}}}$$

$$V_x - V_y = -I_{ee}R_c \tanh\left(\frac{I_{ee}}{4V_T}\right) = -I_{ee}R_c\left[\frac{V_{in_1}-V_{in_2}}{2V_T}\right]$$

$y = mx$

$\frac{1-e^{-2\theta}}{1+e^{2\theta}} = \tanh\theta$



what is slope of characteristic curve around or $V_{in1} - V_{in2} = 0$

$$V_x - V_y = -R_c I_{ee} \tanh\left(\frac{V_{in1}-V_{in2}}{2V_T}\right)$$

since $V_{in1} - V_{in2} = 0$

$$\tanh\left(\frac{V_{in1}-V_{in2}}{2V_T}\right) << 1$$

$$\therefore \tan\frac{V_{in1}-V_{in2}}{2V_T} = \frac{V_{in1}-V_{in2}}{2V_T}$$

$$V_x - V_y = -\frac{R_c I_{ee}}{2V_T}(V_{in1}-V_{in2})$$

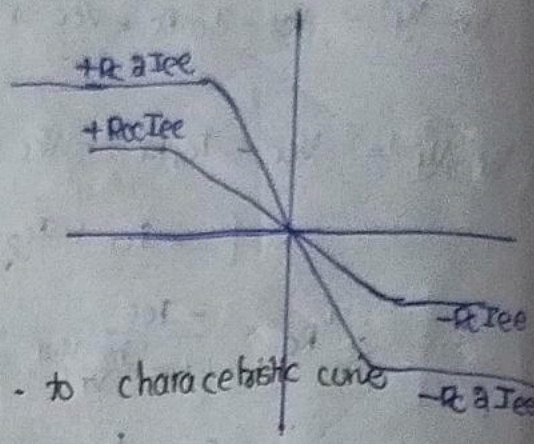
Slope :

$$\boxed{\frac{V_x - V_y}{V_{in1}-V_{in2}} = -\frac{R_{cc}I_{ee}}{2V_T}}$$

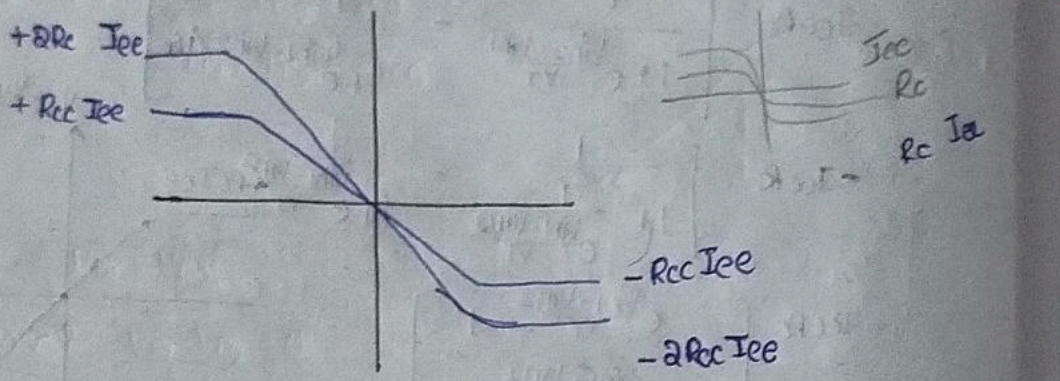
what happens to characteristic curve if Iee is doubles

Iee → 2Iee

graph/characteristic curve expands →

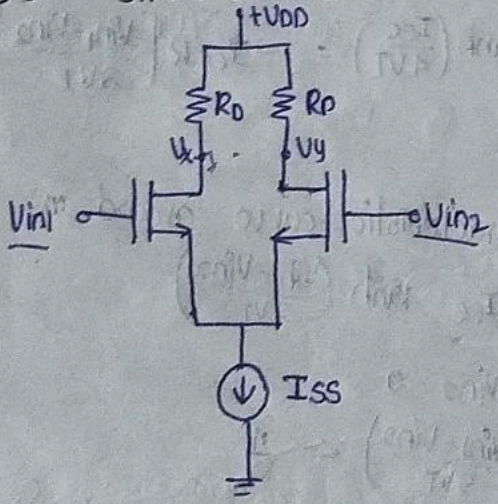


what happens if Rc doubled → to characteristic curve

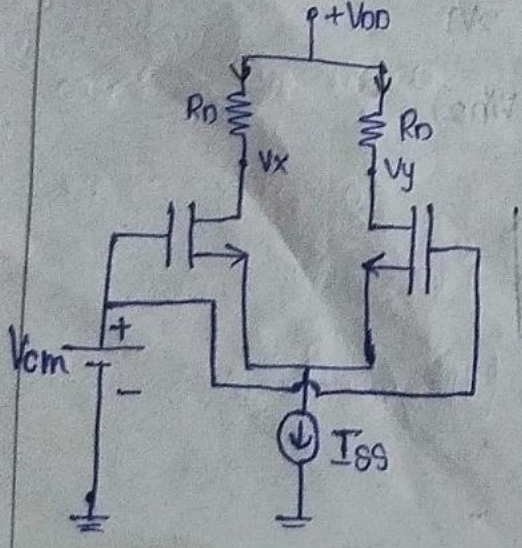


* Ambient temperature ↑, slope ↑

MOS DIFFERENTIAL PAIR AMPLIFIERS



case i) Both Vin1 & Vin2 are short circuit



$V_{in1} = V_{in2} = V_{cm}$

$I_{D1} = I_{D2} = \frac{I_{SS}}{2}$

$I_{D1} + I_{D2} = I_{SS}$

since both are identical

$\therefore I_{D1} = I_{D2} = \frac{I_{SS}}{2}$

$$\boxed{V_x = V_y = V_{DD} - \frac{I_{SS}}{2} R_D} \qquad I_{D1} = I_{D2} = \frac{I_{SS}}{2}$$

From the circuit,

V_{GS1} , $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS1} - V_{th})^2$

$$\frac{I_{SS}}{2} = \frac{\mu_n C_{ox} W/L}{2} (V_{GS1} - V_{th})^2$$

$$I_{SS} = \mu_n C_{ox} \frac{W}{L} (V_{GS1} - V_{th})^2$$

$$V_{GS1} = V_{GS2} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox} W/L}} + V_{th}$$

* If $V_{in1} = V_{in2}$, the differential pair under Equilibrium mode so that overdrive voltage is given by

↓ Biasing Equilibrium

$$V_{GS1} - V_{th} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox} W/L}} \qquad \sqrt{\frac{I_{SS}}{\mu_n C_{ox} W/L}}$$

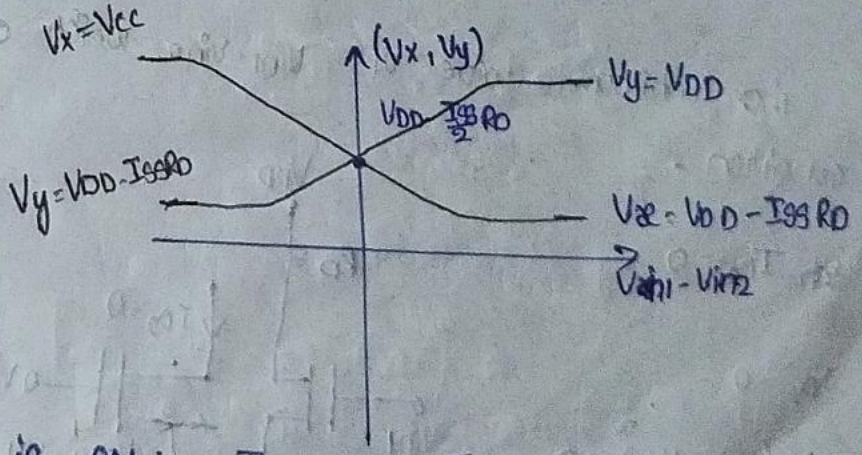
* If any changes made in $V_{cm\,min}$, the circuit parameters doesn't got affected.

Case 2: Differential Behaviour:

$I_{D1} =$

① Q_1 is in ON : $I_{D1} = I_{SS}$ $I_{D2} = 0$ $I_{D1} = I_{SS}/2$ $I_{D2} = \frac{I_{SS}}{2}$

$V_x = V_{DD} - I_{SS} R_D$ $V_y = V_{DD}$. $V_x = V_y = V_{DD} - \frac{I_{SS}}{2} R_D$



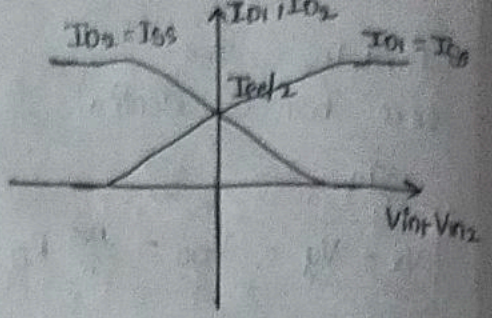
Q_2 is ON : $I_{D2} = I_{SS}$ $I_{D1} = 0$

$V_y = V_{DD} - I_{SS} R_D$ $V_x = V_{CC}$

① $I_{D2} - I_{D1} = I_{ee}/2$

Q1 ON: $I_{D1} = I_{ee}$ $I_{D2} = 0$

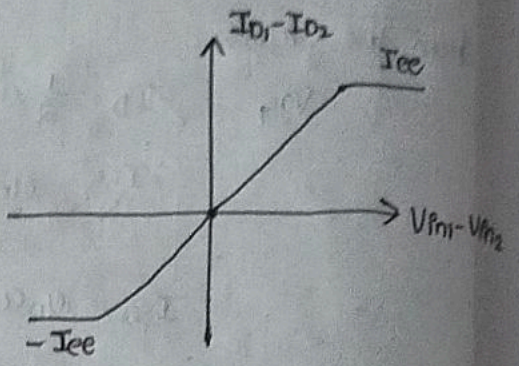
Q2 ON: $I_{D2} = I_{ee}$ $I_{D1} = 0$



② $I_{D1} - I_{D2}$

⇒ 1: $I_{D1} - I_{D2} = I_{ee}$

$I_{D1} - I_{D2} = -I_{ee}$

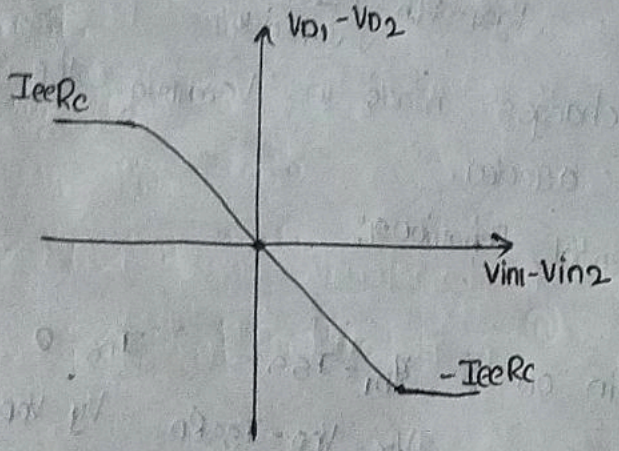


③ $V_{D1} - V_{D2}$

case i: $V_{D1} - V_{D2} = 0$

case ii: $V_{D1} - V_{D2} = V_{DD} - I_{ee}R_C - V_{DD} = -I_{ee}R_C$

case iii: $V_{D1} - V_{D2} = V_{DD} - V_{DD} + R_C I_{ee} = I_{ee}R_C$



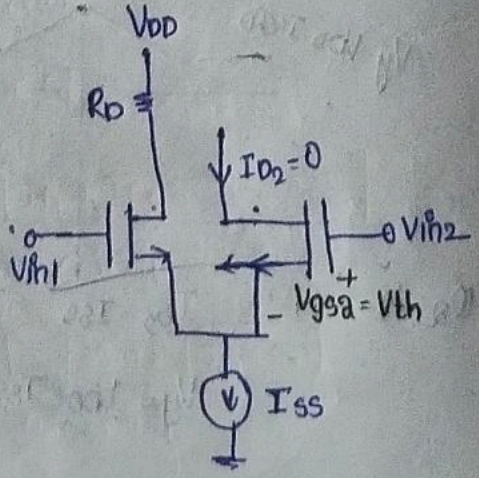
what is the minimum value of $V_{in1} - V_{in2}$ which one of mos is in off condition -

case i: $I_{D2} = 0$

we have $I_{D2} = 0$ -

$\frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{gs2} - V_{th})^2 = 0$

$\boxed{V_{gs2} = V_{th}}$

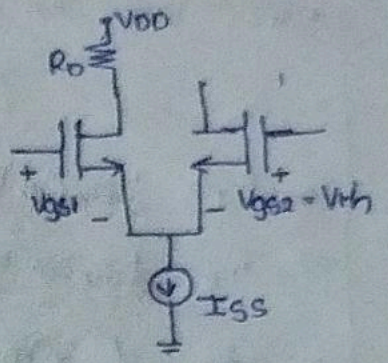


case ii) M1 is in ON mode

$I_{D1} = I_{SS}$

$I_{SS} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{gs1} - V_{th})^2$

$V_{gs1} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} W/L}} + V_{th}$.



case iii) $V_p = V_{in1} - V_{gs1} = V_{in2} - V_{gs2}$

$V_{in1} - V_{in2} = V_{gs1} - V_{gs2}$

$V_{in1} - V_{in2} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} W/L}} + V_{th} - V_{th}$

$$\boxed{V_{in1} - V_{in2} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} W/L}}}$$

the minimum value $V_{in1} - V_{in2}$ required to turn off one of mos is

$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} W/L}} \quad -①$$

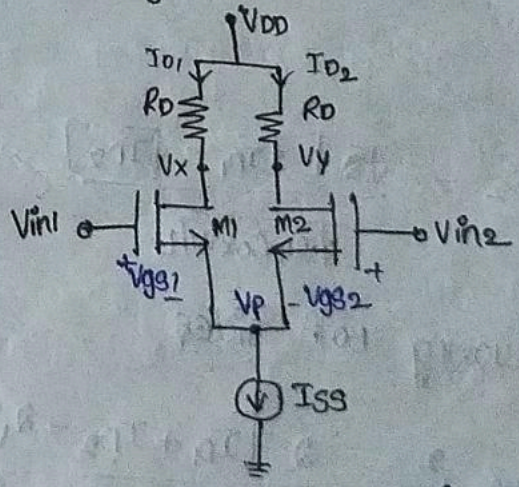
* we have $V_{gs1} - V_{th} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox} W/L}} \quad -②$

comparing ① and ②

$V_{in1} - V_{in2} = \sqrt{2}\,[V_{gs1} - V_{th}]$

$V_{in1} - V_{in2} = \sqrt{2}$ [Biasing overdrive voltage]

Large signal Analysis of mos Differential Amplifiers:-



When M1, M2 transistors are not identical,

$V_p = V_{in} - V_{gs1}$

$V_p = V_{in} - V_{gs2}$

$V_{in1} - V_{in2} = V_{gs1} - V_{gs2}$

* we know that Drain current Eqn is given by

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2 \quad \text{- saturation}$$

$$\Rightarrow I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs1}-V_{th})^2$$

$$\Rightarrow I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs2}-V_{th})^2$$

$$\Rightarrow V_{gs1} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} W/L}} + V_{th}$$

$$\Rightarrow V_{gs2} = \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} W/L}} + V_{th}$$

$$\Rightarrow V_{in1} - V_{in2} = V_{gs1} - V_{gs2}$$

$$= \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} W/L}} + V_{th} - \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} W/L}} - V_{th}$$

$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} W/L}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} W/L}} = \frac{\sqrt{2I_{D1}} - \sqrt{2I_{D2}}}{\sqrt{\mu_n C_{ox} W/L}}$$

$\Rightarrow$ From circuit,

$$I_{D1} + I_{D2} = I_{SS}$$

we have $V_x = V_{DD} - I_{D1}R_D$

$V_y = V_{DD} - I_{D2}R_D$

$$\boxed{V_x - V_y = -R_D[I_{D1} - I_{D2}]} \quad \text{---} \ (A)$$

consider

$$V_{in1} - V_{in2} = \frac{\sqrt{2}\left[\sqrt{I_{D1}} - \sqrt{I_{D2}}\right]}{\sqrt{\mu_n C_{ox} W/L}}$$

squaring both sides

$$(V_{in1} - V_{in2})^2 = \frac{2\left[I_{D1} + I_{D2} - 2\sqrt{I_{D1}I_{D2}}\right]}{\mu_n C_{ox} W/L}$$

$$(V_{in1} - V_{in2})^2 = \frac{2\left[I_{SS} - 2\sqrt{I_{D1}I_{D2}}\right]}{\mu_n C_{ox} W/L}$$

$$\frac{2\sqrt{I_{D1}I_{D2}}}{\mu_n C_{ox} W/L} = \frac{2I_{SS}}{\mu_n C_{ox} W/L} - (V_{in}-V_{in2})^2$$

$$\frac{4 I_{D1}I_{D2}}{(\mu_n C_{ox} W/L)^2} = \frac{4I_{SS}}{(\mu_n C_{ox} W/L)^2} + (V_{in}-V_{in2})^2 - \frac{4 I_{SS}}{\mu_n C_{ox} \frac{W}{L}} V_{in_1} - V_{in_2}$$

$$4 I_{D1} I_{D2} = 4 I_{SS} + \frac{(V_{in_1} - V_{in_2})^2}{\mu_n C_{ox} W/L}$$

$$4 I_{D_1} I_{D_2} = 4 I_{SS} + (\mu_n C_{ox} W/L)^2 (V_{in_1} - V_{in_2})^2 - 4 I_{SS}(V_{in_1} - V_{in_2})(\mu_n C_{ox} W/L)$$

$$V_{in1} - V_{in2} = \frac{\sqrt{2}}{\mu_n C_{ox} \frac{W}{L}} V_{gs_1} - V_g\left(\sqrt{I_{D_1}} - \sqrt{I_{D_2}}\right)$$

$$(V_{in_1} - V_{in_2})^2 = \frac{2}{\mu_n C_{ox} \frac{W}{L}} \left(I_{D_1} + I_{D_2} - 2\sqrt{I_{D_1} I_{D_2}}\right)$$

$$\frac{\mu_n C_{ox} W/L}{2} (V_{in} - V_{in2})^2 = I_{SS} - 2\sqrt{I_{D_1} I_{D_2}}$$

$$2\sqrt{I_{D_1} I_{D_2}} = I_{SS} - \frac{\mu_n C_{ox} W/L}{2} (V_{in_1} - V_{in_2})^2$$

$$4 I_{D_1} I_{D_2} = I_{SS}^2 + \left(\frac{\mu_n C_{ox} W/L}{2}\right)^2 (V_{in_1} - V_{in_2})^4 - I_{SS} \mu_n C_{ox} \frac{W}{L} (V_{in_1} - V_{in_2})^2$$

$$4 I_{D_1} I_{D_2} = (I_{D_1} + I_{D_2})^2 - (I_{D_1} - I_{D_2})^2$$

$$(I_{D_1} - I_{D_2})^2 = I_{SS}^2 - 4 I_{D_1} I_{D_2}$$

$$= I_{SS}^2 - I_{SS}^2 + 2 I_{SS} \mu_n C_{ox} \frac{W}{L} (V_{in_1} - V_{in_2})^2 - \left(\frac{\mu_n C_{ox} W/L}{2}\right)^2 (V_{in} - V_{in2})^4$$

$$= \frac{1}{4} (\mu_n C_{ox} W/L)^2 (V_{in_1} - V_{in_2})^2 \left[\frac{4 I_{SS}}{\mu_n C_{ox} W/L} - (V_{in_1} - V_{in_2})^2 \right]$$

$$I_{D_1} - I_{D_2} = \sqrt{\frac{1}{4} (\mu_n C_{ox} \frac{W}{L})^2 (V_{in_1} - V_{in_2})^2 \cdot \frac{4 I_{SS}}{\mu_n C_{ox} W/L} - (V_{in_1} - V_{in_2})^2}$$

$$I_{D_1} - I_{D_2} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in_1} - V_{in_2}) \sqrt{\frac{4 I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - (V_{in_1} - V_{in_2})^2}$$

$$I_{D_1} - I_{D_2} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in_1} - V_{in_2}) \sqrt{\frac{4 I_{SS}}{\mu_n C_{ox} W/L} - (V_{in_1} - V_{in_2})^2}$$

Condition 1: $V_{in1} = V_{in2}$

$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox} W/L (V_{in1} - V_{in2}) \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - (V_{in1} - V_{in2})^2}$$

$$I_{D1} - I_{D2} = 0 \qquad [\because V_{in1} = V_{in2}]$$

$$I_{D1} = I_{D2}$$

from above,

$$I_{D1} = I_{D2} \qquad [\because M1, M2 \text{ short circuit}]$$

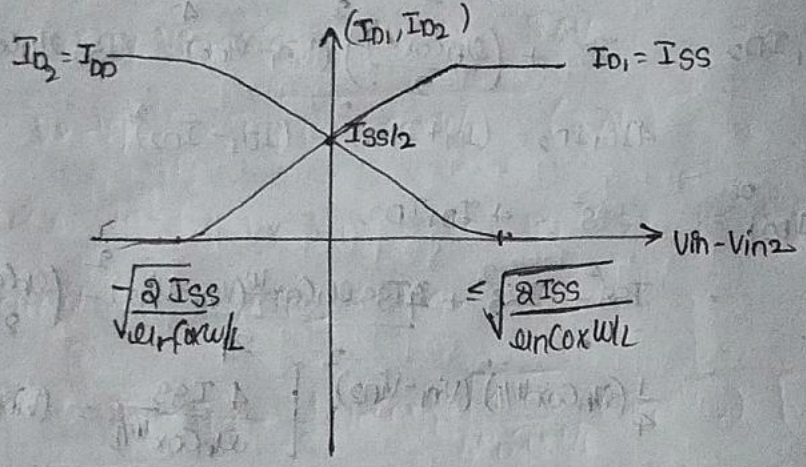
Above Equation is valid is only when Both M1 & M2 are ON conditions at the edge of saturation is turning off upto.

$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} W/L}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} W/L}}$$

this Equation $[I_{D1} - I_{D2}]$ is valid only if $V_{in1} - V_{in2} \leq$ $\sqrt{2}$(overdrive voltage)

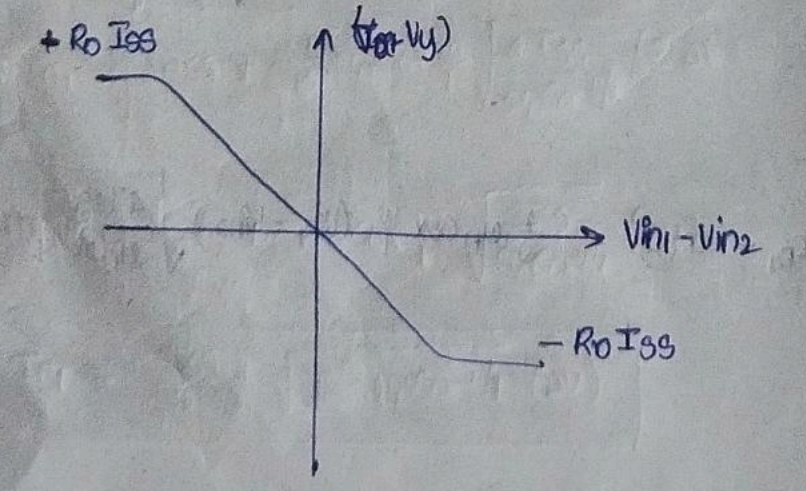
$V_{in1} = V_{DD} - I_{SS}R_D$
$- V_{DD}$
$- I_{SS}R_D$

$$V_{in1} - V_{in2} \leq \sqrt{2}\left(\sqrt{\frac{I_{SS}}{\mu_n C_{ox} W/L}}\right.$$



Differential output voltage is given by

$$V_x - V_y = -\frac{R_D}{2}\left[\mu_n C_{ox} W/L (V_{in1} - V_{in2}) \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} W/L} - (V_{in1} - V_{in2})^2}\right]$$



* case :

$(V_{in1} - V_{in2})^2 \ll\ll \frac{4 I_{SS}}{\mu_n C_{ox} W/L}$

$I_{D1} - I_{D2} =$

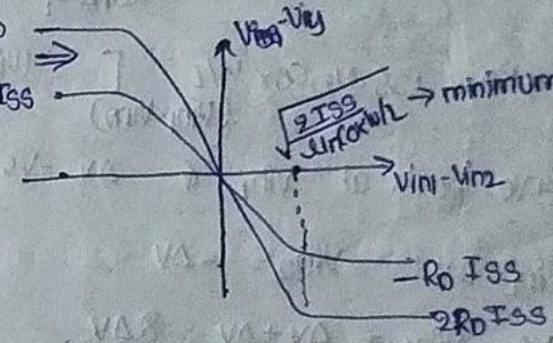
$V_x - V_y = -R_D \frac{1}{2} \mu_n C_{ox} W/L \sqrt{\frac{4 I_{SS}}{\mu_n C_{ox} W/L}}$

$$\boxed{V_x - V_y = -R_D \sqrt{I_{SS} \mu_n C_{ox} W/L}\ (V_{in1} - V_{in2})}$$

* what happens to characteristic curve if I_{SS} is doubled.

$Gain = slope = \frac{V_x - V_y}{V_{in1} - V_{in2}} = -R_D \sqrt{I_{SS} \mu_n C_{ox} W/L}$

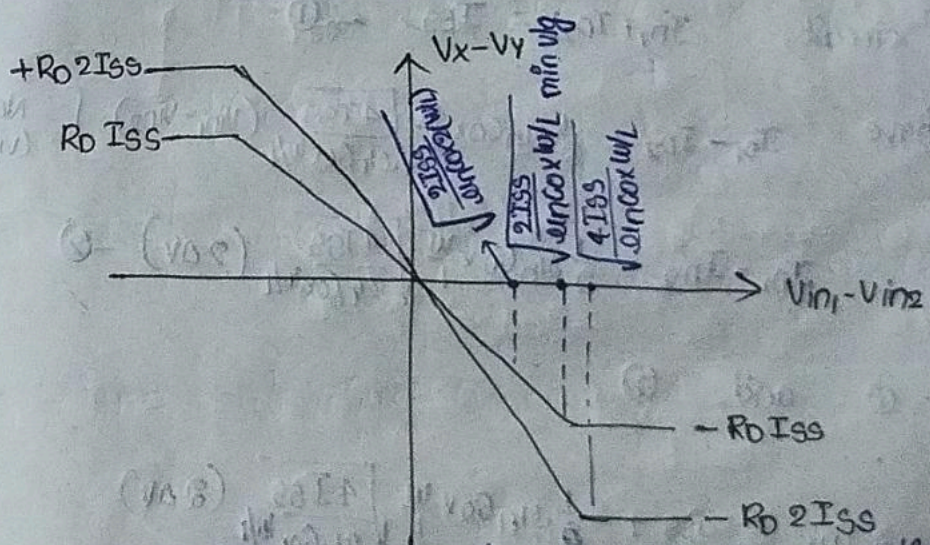
$I_{D1} - I_{D2}$



If $(\frac{W}{L})$ is doubled is what happens to ~~$I_{D1} - I_D$~~ $V_x - V_y$

$V_x - V_y = -\frac{R_D}{2} \mu_n C_{ox} \frac{W}{L} \sqrt{\frac{4 I_{SS}}{\mu_n C_{ox}} - (V_{in} - V_{in2})^2}\ (V_{in1} - V_{in2})$

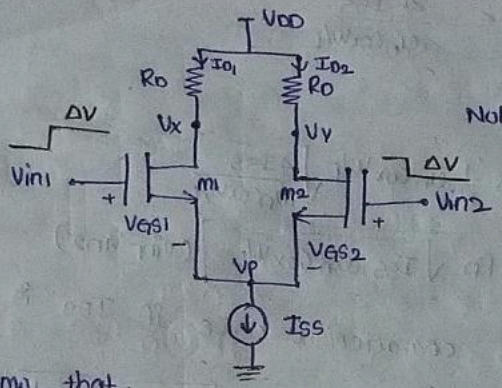
$V_x - V_y = -R_D \sqrt{I_{SS} \mu_n C_{ox} (\frac{W}{L})}$



here when $(\frac{W}{L})$ is doubled, the cure is more linear than normal curve of $V_x - V_y$

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Small Signal Analysis of mosfet differential Amplifier



* we know that,

$$V_x - V_y = -\frac{R_D}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1}-V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1}-V_{in2})^2}$$

$$V_x - V_y = -R_D\sqrt{I_{SS}\mu_n C_{ox}\frac{W}{L}}\left[\because (V_{in1}-V_{in2})^2 < \frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}}\right]$$

* applying ΔV +ve peak at V_{in1} & ΔV -ve peak at V_{in2}

$$V_{in1} = \Delta V \qquad V_{in2} = -\Delta V$$

$$V_{in1} - V_{in2} = \Delta V + \Delta V = 2\Delta V$$

$$V_x - V_y = -R_D\sqrt{I_{SS}\mu_n C_{ox}\frac{W}{L}}\,(2\Delta V)$$

* we know that $V_x - V_y = -R_D(I_{D1} - I_{D2})$
* From circuit, $I_{D1} + I_{D2} = I_{SS}$ —①
* we have $I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}(V_{in1}-V_{in2})$ [∵ Neglect $(V_{in1}-V_{in2})^2$]

$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}(2\Delta V) \quad -②$$

Solving ① and ②

$$2I_{D1} = I_{SS} + \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}(2\Delta V)$$

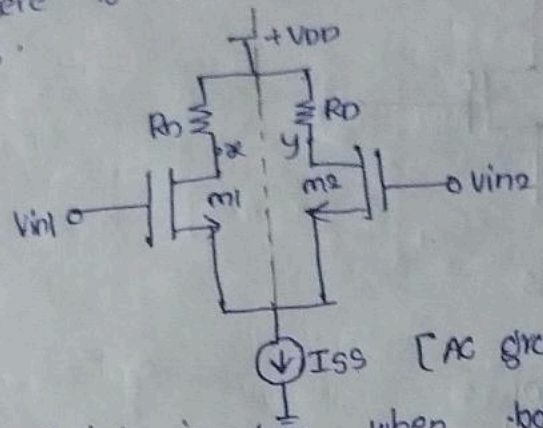
$$I_{D1} = \frac{I_{SS}}{2} + \mu_n C_{ox}\frac{W}{L}\sqrt{\frac{I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}(\Delta V)$$

$$\boxed{I_{D1} = \frac{I_{SS}}{2} + \sqrt{I_{SS}\mu_n C_{ox}\frac{W}{L}}\,(\Delta V)}$$

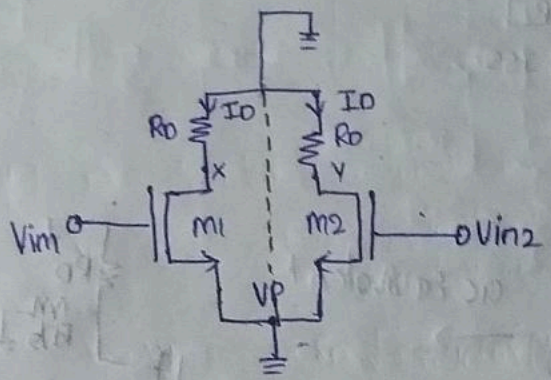
comparing with $I_D = I_0 + g_m V_{GS}$

$$g_m = \sqrt{I_{SS}\mu_n C_{ox} W/L}$$

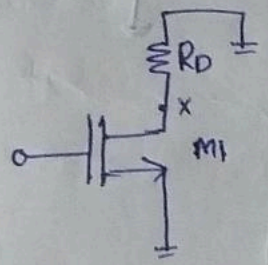
* there is no effect on Up point due to change in differential inputs.



* [AC ground in small signal Analysis]
* All Analysis is done when both MOSFETS are "identical"
* Consider M1, M2 are identical, draw a line of symmetry as shown and do small signal Analysis on one of transistor.



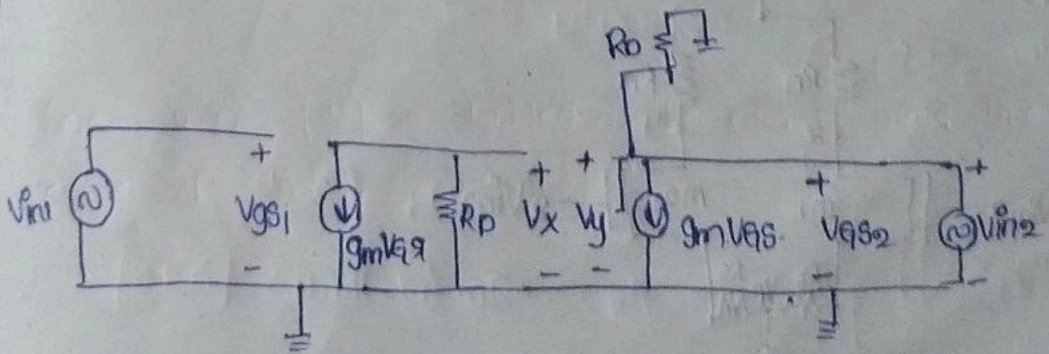
Ac Equivalent Circuit :



$A_V = -g_m R_D [(\lambda = 0)]$

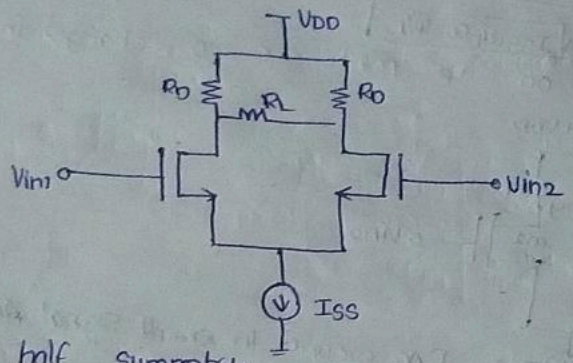
$A_V = -g_m (R_D \| r_o) [(\lambda \neq 0)]$

from circuit $A_V = \frac{V_x}{V_{in_1}} = \frac{V_x - V_y}{V_{in_1} - V_{in_2}} = -g_m R_D$

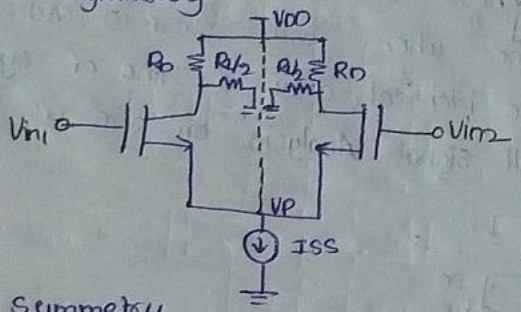


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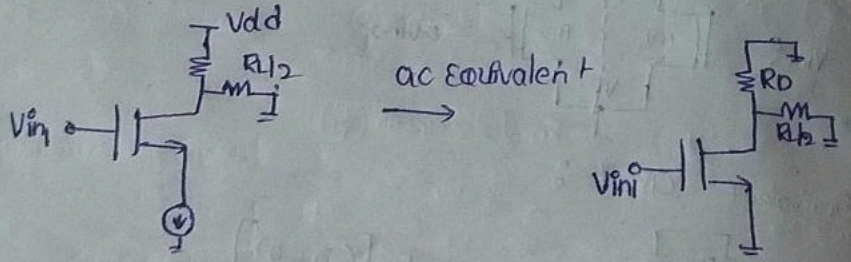
case (i) Half Symmetry Circuit :-



using half symmetry



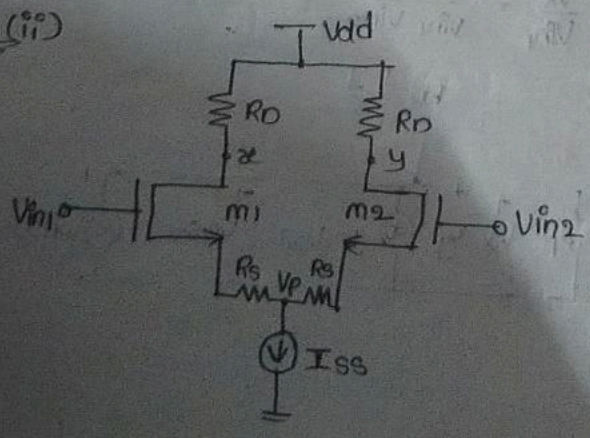
using symmetry



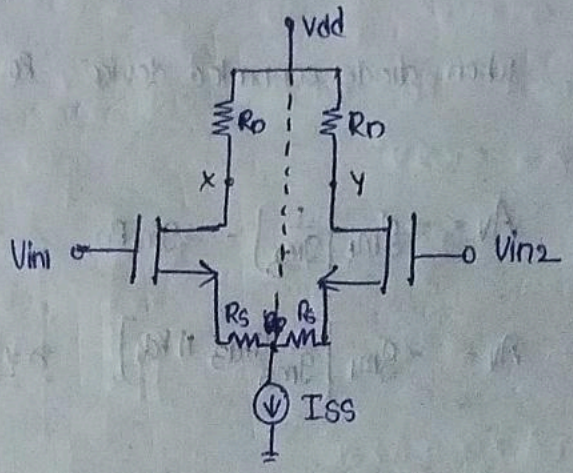
* $\lambda = 0 \Rightarrow A_V = -g_m\left(R_{OD} \| \frac{R_L}{2}\right)$

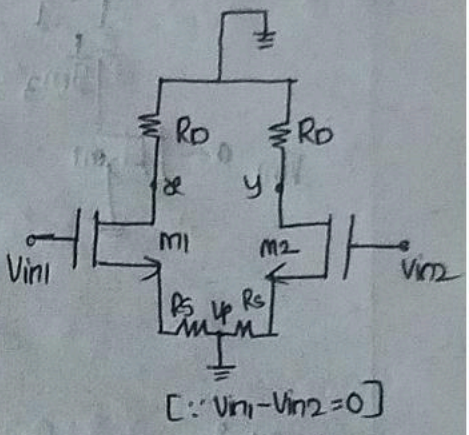
* $\lambda \neq 0 \Rightarrow A_V = -g_m\left(R_{OD} \| \frac{R_L}{2} \| R_d\right)$

case (ii)



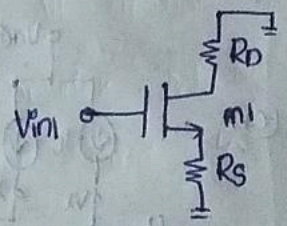
using symmetry line we have





$[\because V_{in1} - V_{in2} = 0]$

draw Ac Equivalent for one of symmetry

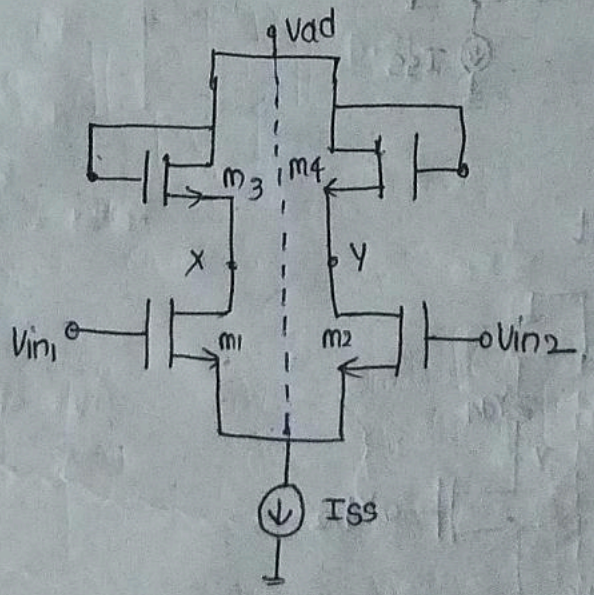


$$A_V = \frac{-g_m R_D}{1+g_m R_S} \quad [\lambda = 0]$$

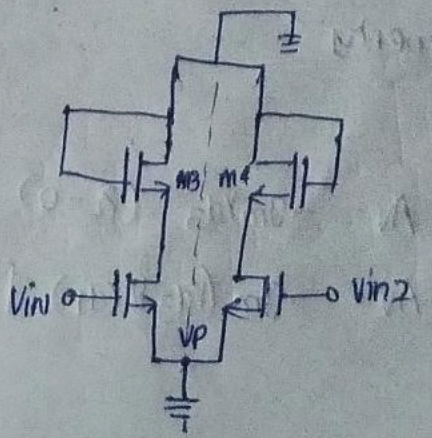
$$A_V = \frac{-g_m (R_D \| r_d)}{1+g_m R_S} \quad (\lambda \neq 0)$$

Diode Connected device as load :

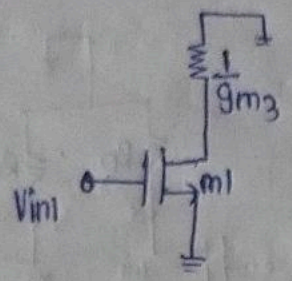
Case (iii)



ac Equivalent Circuit :



Consider one of load,



when diode connected device $R_D = 1/g_m$ $\lambda = 0$

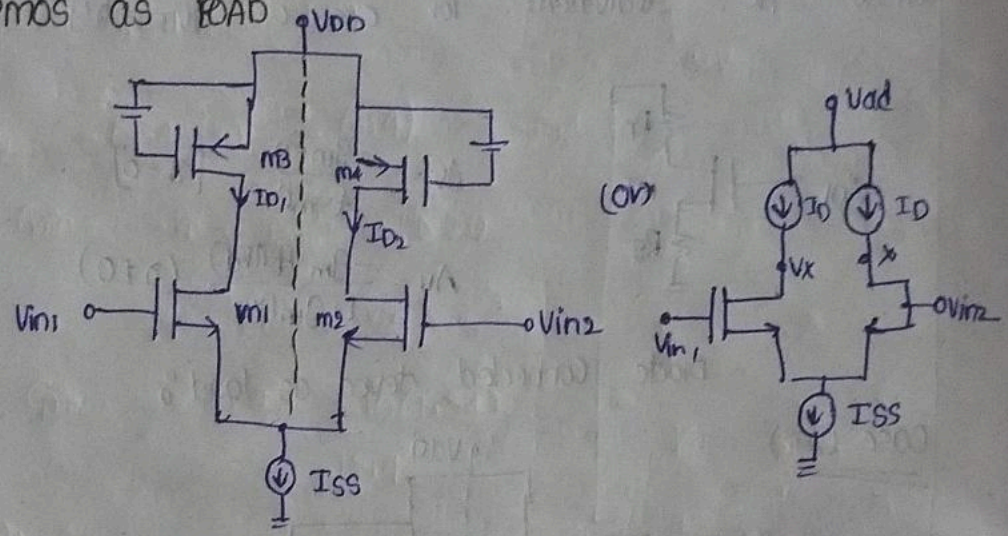
$\frac{1}{g_m} \| r_d$ $\lambda \neq 0$

$$A_V = -g_{m_1}\left[\frac{1}{g_{m_3}}\right] = -g_{m_1}R_D = \frac{-g_m}{g_{m_3}}$$

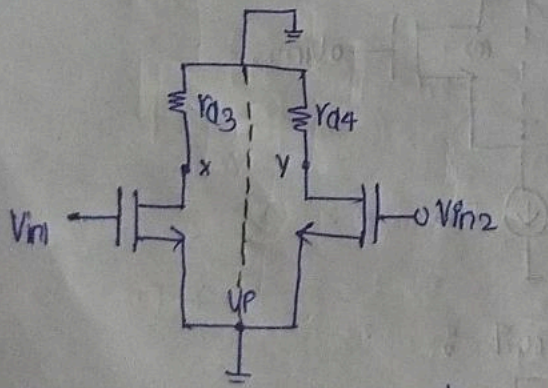
$$A_V = -g_{m_1}\left[\frac{1}{g_{m_3}} \| r_{d_3} \| r_{d_1}\right] \quad \lambda \neq 0.$$

case(iv) :

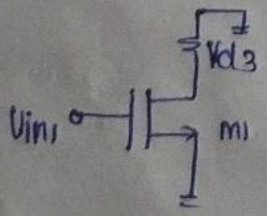
* PMOS as LOAD



AC Equivalent Circuit



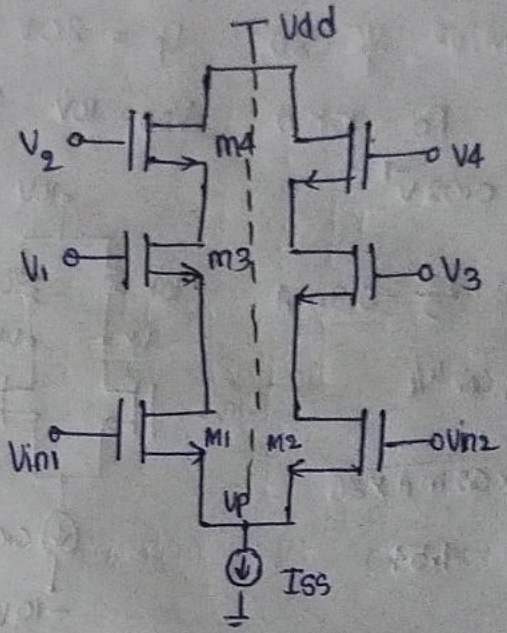
consider one of symmerty

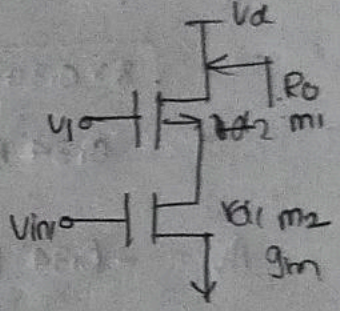


$$A_V = -g_m r_{d_3} \quad (\lambda = 0)$$

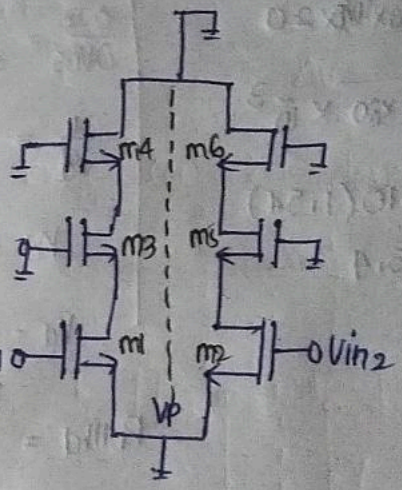
$$A_V = -g_m (r_{d_3} \| r_{d_1}) \quad [\lambda \neq 0]$$

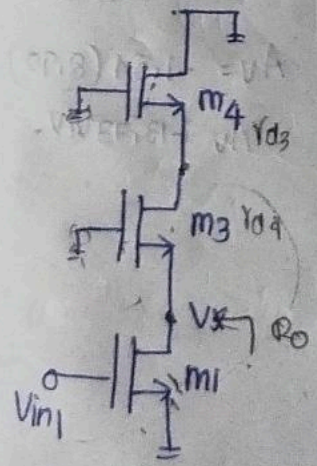
case 5) cascode Amplifier as load [telescope circuit]





ac Equivalent circuit :



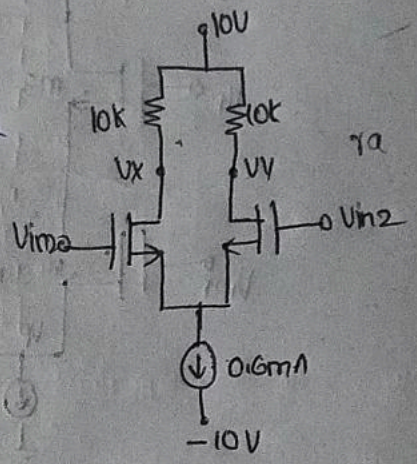


$Av = -g_m (r_{d1} \| \cdots$

$Av = -g_{m1} (g_{m3} r_{d3} r_{d1}) \| r_{d4}$

Find the differential gain of differential mos Amplifier with follow spec: $\mu_n C_{ox} = 0.2 mA/V^2$ $\frac{W}{L} = 20$ $V_p = 20V$ find $\lambda = 0$ $\lambda \neq 0$

$I_{SS} = 0.6mA$ $R_D = 10K\Omega$ $V_{DD} = 10V$ $V_{SS} = -10V$ Both are identical $\lambda = 0.02 V^{-1}$



$A_v = -g_m R_D$ $\frac{I_{SS}}{2} = 0.3mA$

$g_m = \sqrt{2 I_{Dmax} \mu_n C_{ox} W/L}$

$= \sqrt{2 \times 0.3mA \times 0.2mA \times 20}$

$= 0.34\ mS$ 1.54

$A_v = -(0.34)(10) = -(3.4) = -15.4$

$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$

$\frac{\partial I_D}{\partial V_{DS}} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 (\lambda)$

$\frac{1}{r_d} = I_D \lambda$

$r_d = \frac{1}{\lambda I_D}$

$r_d = \frac{1}{0.02 (0.6)}$ K

$83.33K$

$R_D \| r_d = \frac{83.33 \times 10}{83.33 + 10}$

$= 8.92\ K$

$A_v = -1.54 (8.92)$

$A_v = -13.73\ V/V$

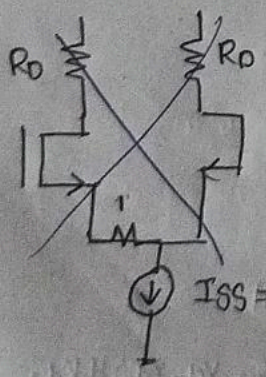
Gain $= -R_D \sqrt{I_{SS} \mu_n C_{ox} W/L \times 20}$

$= -10K \sqrt{0.6 \times 0.2 \times 20} \times 10^{-3}$

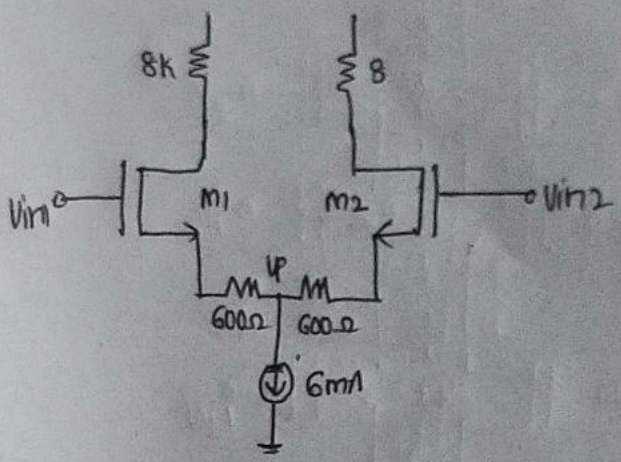
Gain $= -3.4$ $-10(1.54)$

$= -15.4$

Find A_v :



Find Av :



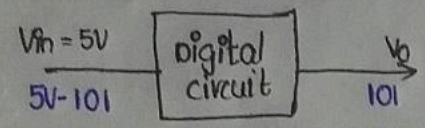
UNIT - 4

Complementary Metallic Oxide Semiconductors [CMOS]

TTL - Transistor / Transistor Logic

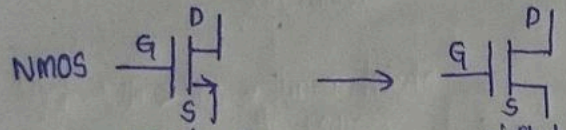
MOS (0.8 - 1.8) ms

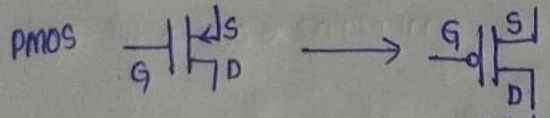
* CMOS is used for Digital representation
* CMOS has less power consumtion, high packing density.
* BJT requires more speed bcoz it requeqers more power consumption than mos & CMOS.
* BJT has high gm value.
* more speed - BJT
* CMOS logic family — less power consoumption
* → high packing density (i.e millions of transistors are fabricated on a single wafer.



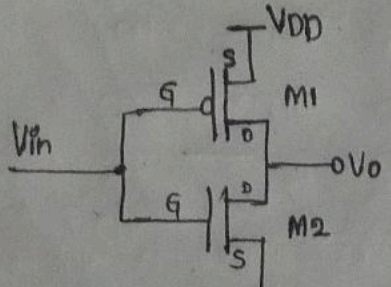
Logic 0 - LOW - 0V [analog]
Logic 1 - HIGH - 5V [analog]

* CMOS is cascading of PMOS and NMOS.



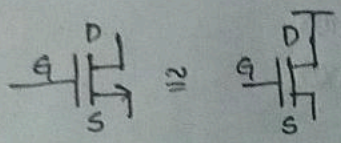


* Body of Nmos should be connected to less power supply [ground]
* Body of Pmos should be connected to Highest power supply [VDD]



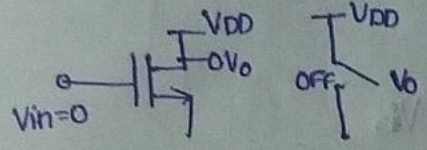
* com CMOS circuit acts as INVERTER(NOT)

NMOS :



case(i) :-

* Vin = 0

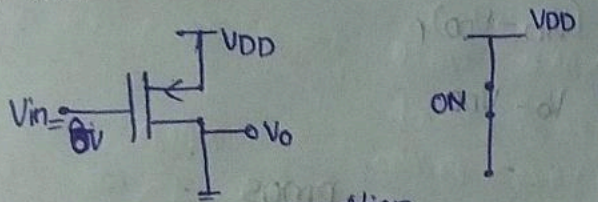


$V_o = V_{DD}$

0 - OFF switch

* Current flowing from drain to source

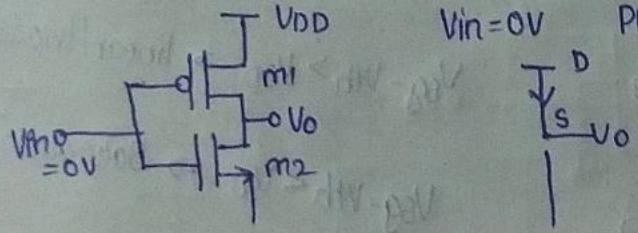
case (ii) Vin = 0



$V_o = 0V$

* 0V - Pmos ON condition.
* Current flows from source to drain

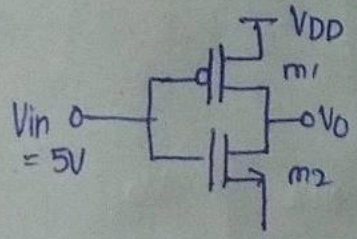
case (i) : Vin = 0V



Vin = 0V Pmos - ON NMOS - OFF

$V_o = V_{DD}$

case (ii) : Vin = 5V



Vin = 5V Pmos - OFF NMOS - ON



$V_o = 0V$

Pmos : Vin = 0 M1 → ON current : S → D → S.C → ON

Vin = 5V M1 → OFF curent : S → D → O.C → OFF

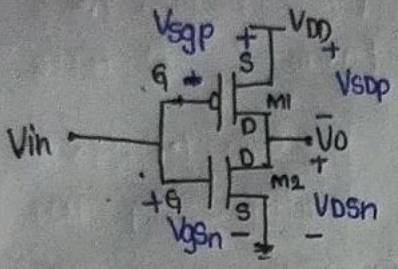
NMOS : Vin = 0 M2 → OFF current : D → S → O.C

vin = 5V M2 - ON current : D → S → S.C

Vin	M1	M2	Vo
0V	ON	OFF	VDD
5V	OFF	ON	0

CMOS INVERTER VOLTAGE TRANSFER CHARACTERISTICS

+Vth - Nmos
-Vth - pmos



$V_{gsn} = (V_g - V_s)_n = (V_{in} - 0)_n = V_{in}$

$V_{dsn} = (V_o - V_s)_n = (V_o - 0)_n = V_o$

$V_{gsp} = (V_g - V_s)_p = (V_{in} - V_{DD})_p$

$V_{dsp} = (V_D - V_s)_p = V_o - V_{DD}$

NOMOS

$V_{gsn} < V_{th}$ - OFF [cutoff]

$V_{gsn} > V_{th}$ - linear region saturation

$V_{gsn} - V_{th} > V_{ds}$ → linear/triode region

$V_{gs} - V_{th} < V_{ds}$ → saturation

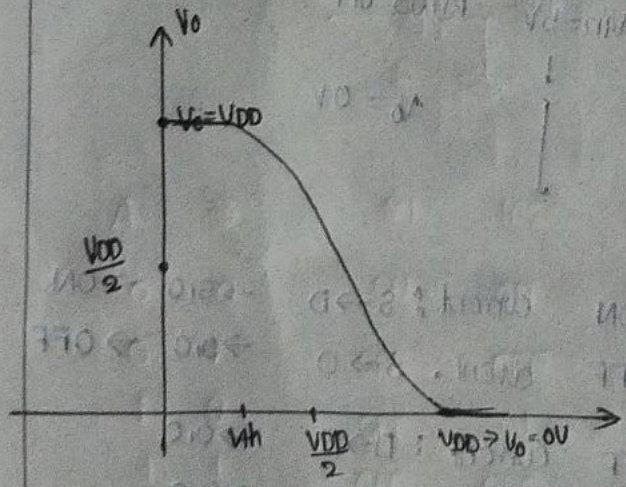
PMOS

$V_{gsp} < V_{th}$ - ON

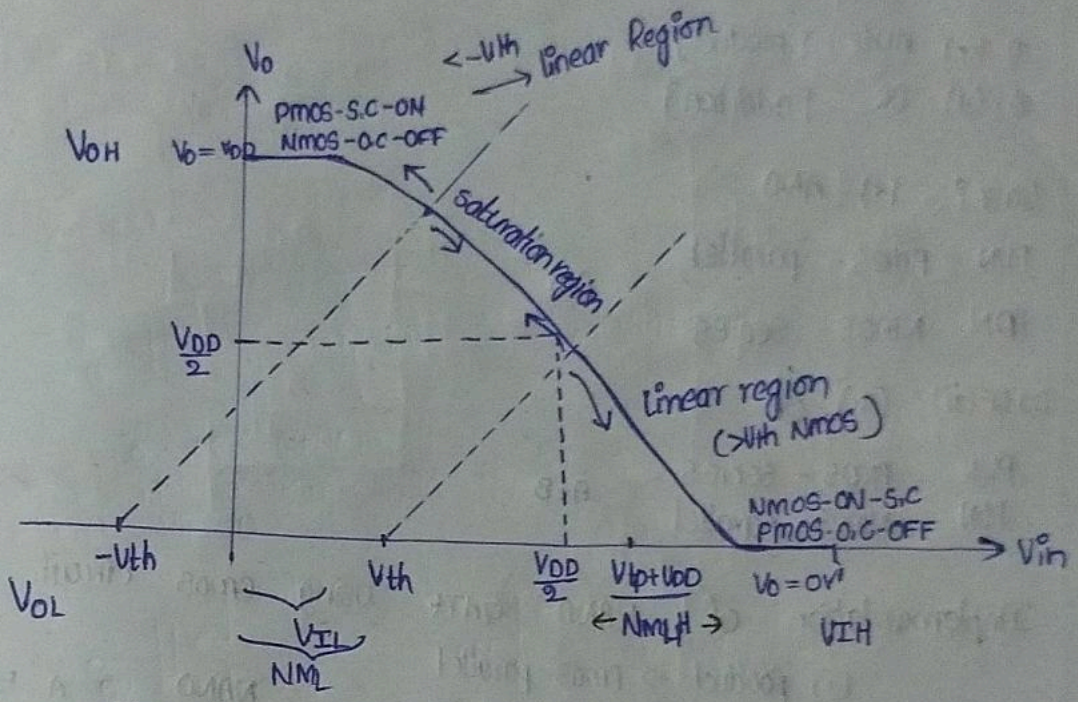
$V_{gsp} > V_{th}$ - cutoff

$V_{sg} - V_{th} > V_{SD}$ → linear/triode

$V_{sg} - V_{th} < V_{SD}$ → Saturation

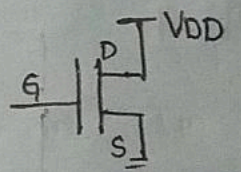


Vtg transfer characteristics of CMOS INVERTER

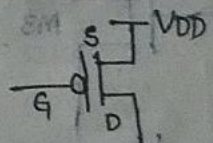


* V_{OH} - output vtg at high level
V_{OL} - output vtg at low level
V_{IL} - input vtg at low level
V_{IH} - input vtg at High level
N_{ML} → Noise module at low level [<Vth] Vin less → High performance of CMOS
N_{MH} → Noise module at High level [

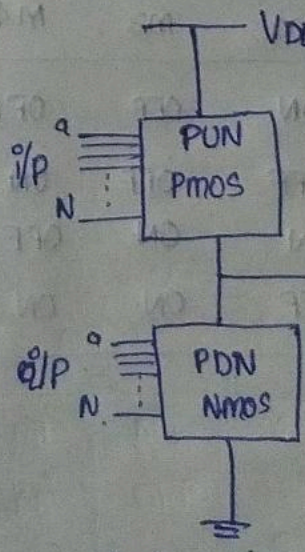
CMOS LOGIC CIRCUIT DESIGN RULES :-



$V_G = 0V$ O.C → OFF $V_{DD} = 5V$
$= 1V$ S.C → ON $V_{DD} = 0V$



$V_G = 0V$ S.C → ON → $V_{DD} = 5$
$V_G = 1V$ O.C → OFF → $V_{DD} = 0$



Pmos transistor easily passes logic HIGH

Nmos transistor easily passes logic LOW.

Block diagram

* cmos logic circuit can perform two tasks

1) (·) AND [product]
2) (+) OR [addition]

Case i :- (·) AND

PUN Pmos - parallel

PDN Nmos - series

A·B

case(ii): (+) OR

PUN Pmos - series

PDN Nmos - parallel

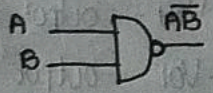
A+B

Implementation of NAND GATE using cmos circuit

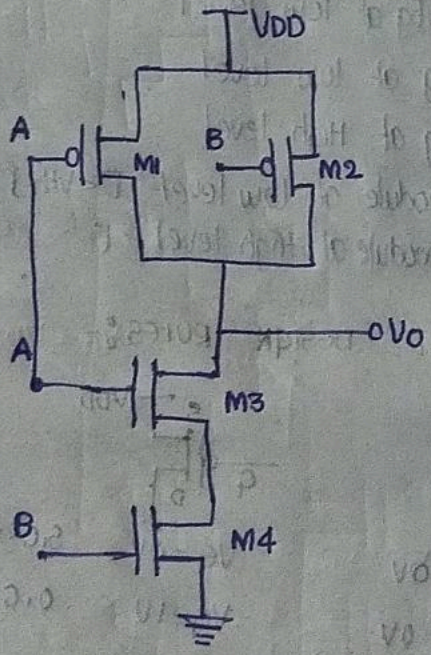
(·) product → Pmos- parallel

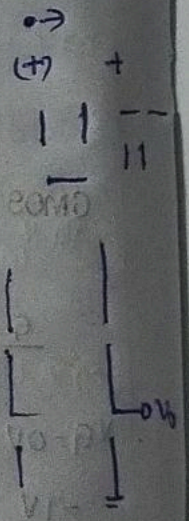
→ Nmos → series.

NAND



A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

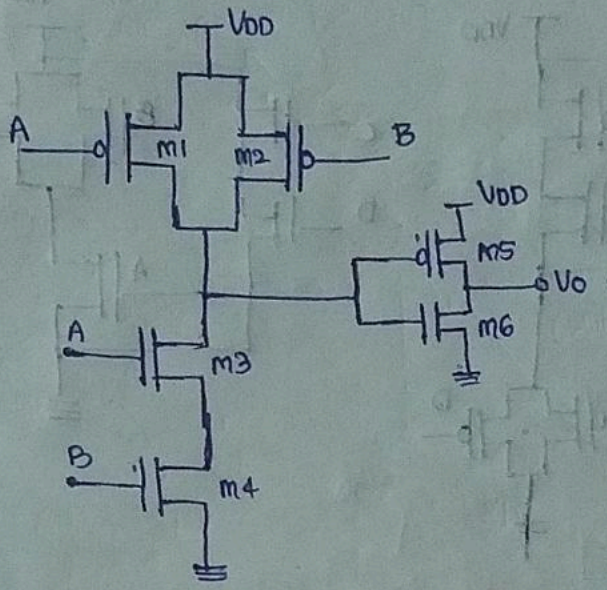




A	B	M1	M2	M3	M4	Vo
0	0	ON	ON	OFF	OFF	VDD
0	1	ON	OFF	OFF	ON	VDD
1	0	OFF	ON	ON	OFF	VDD
1	1	OFF	OFF	ON	ON	0

Implementation of AND GATE USING CMOS circuit

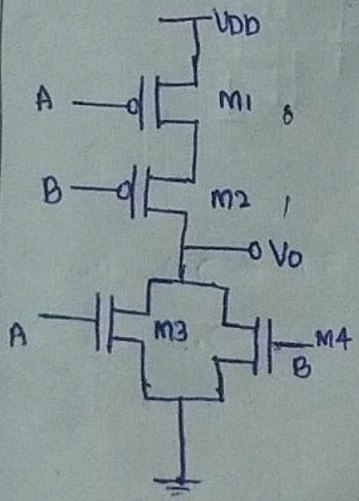
pmos- parallel
Nmos- series



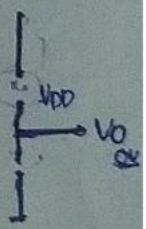
A	B	M1	M2	M3	M4	M5	M6	Vo
0	0	ON	ON	Off	Off	OFF	ON	0
0	1	ON	OFF	OFF	ON	OFF	ON	0
1	0	OFF	ON	ON	OFF	OFF	ON	0
1	1	OFF	OFF	ON	ON	ON	OFF	VDD

Implementation of NOR using cmos

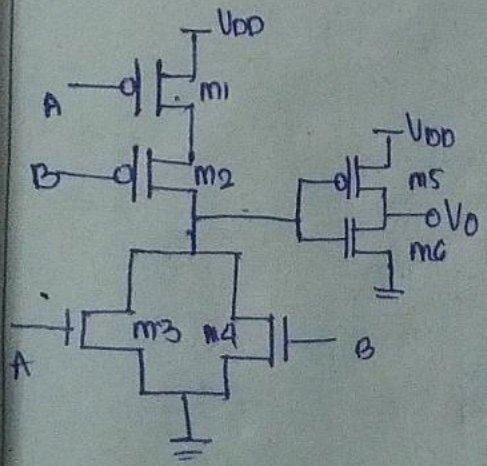
OR- Pmos- series
Nmos- parallel



A	B	m1	m2	m3	m4	Vo
0	0	ON	ON	OFF	OFF	VDD
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

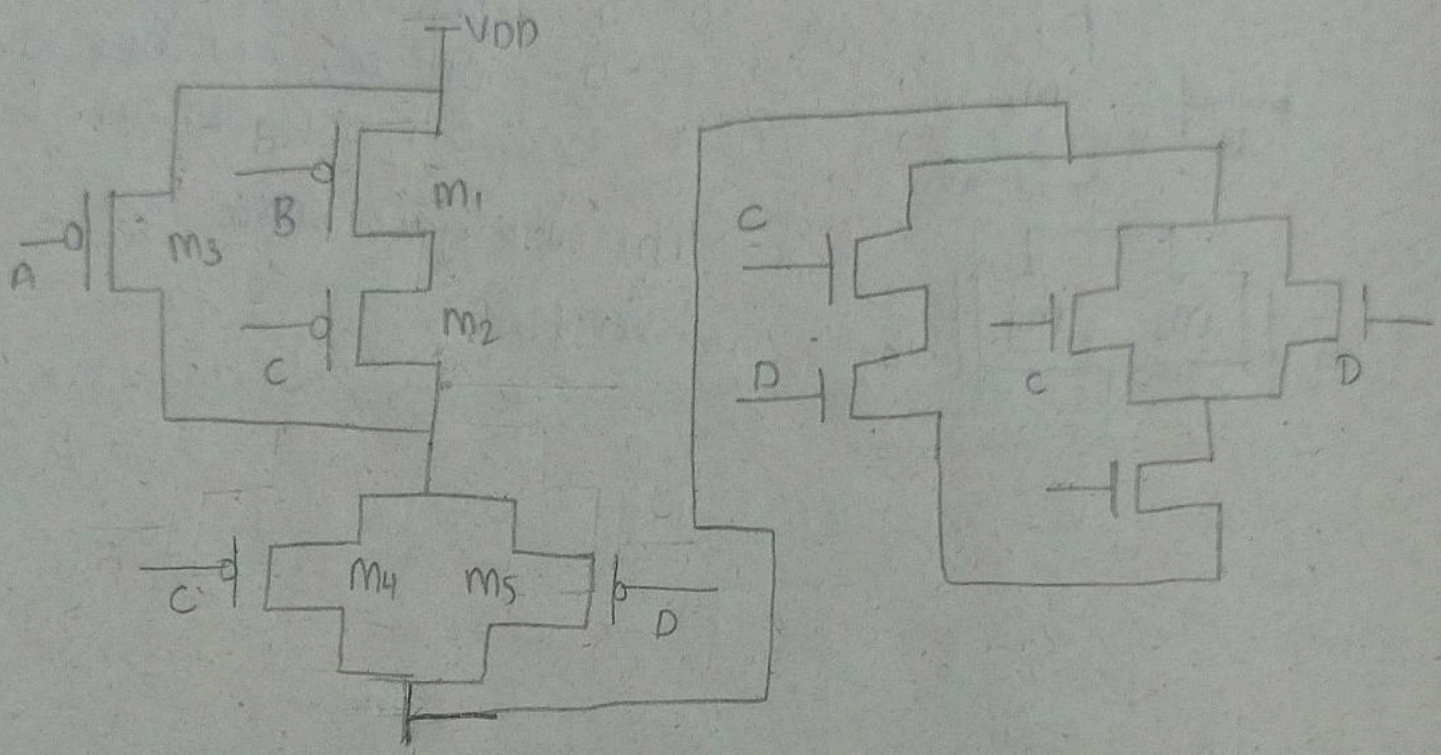


OR GATE :-



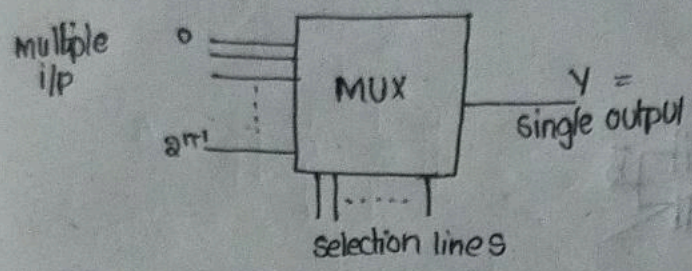
A	B	M1	M2	M3	M4	M5	M6	Vo
0	0	ON	ON	OFF	OFF	OFF	ON	0
0	1	ON	OFF	OF	ON	ON	OFF	1
1	0	OFF	ON	ON	OFF	"	"	1
1	1	OFF	OFF	ON	ON	"	"	1

$Y = (A \cdot (B + C)) + CD$



Implementation 2x1 multiplexer :

$2^n : 1$



* parallel - to - series
* many - to - one circuit
* data selector
* data combiner

