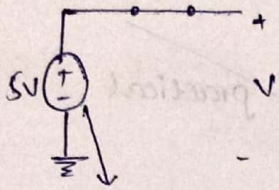
7/12/21

Ideal voltage source

1. Internal resistance is zero.

Modelling:



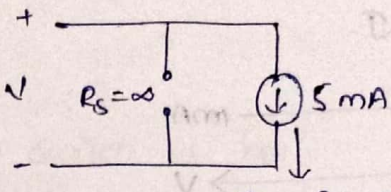
An ideal voltage source of magnitude 5V.

In modelling
Internal resistance comes in series with voltages sources.

Ideal Current Source

1. Internal resistance is infinite.

Modelling



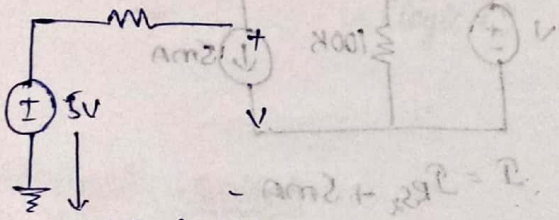
An ideal current source of magnitude 5 mA.

In modelling:
Internal resistance comes in parallel with the current source.

Practical voltage source

Internal resistance is finite

$R_s \neq 0$

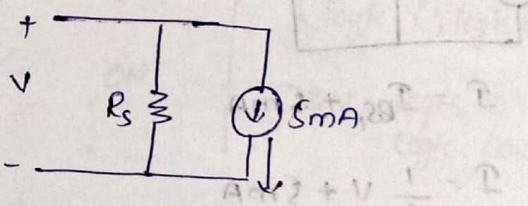


practical voltage source.

Practical Current Source

Internal resistance is finite

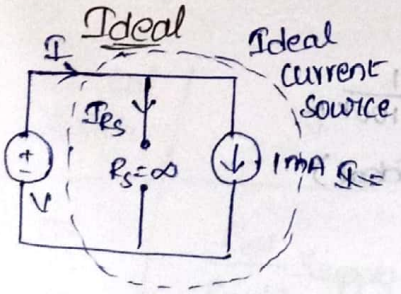
$(R_s \neq \infty)$



Practical current source.

Drawing the I-V characteristics of ideal current source & practical current source.

Ideal



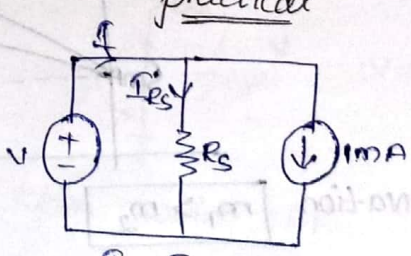
$I = I_{Rs} + 1mA$

$= \frac{V}{\infty} + 1mA$

$= 0 + 1mA$

$I = 1mA \cdot (y = c)$

practical



$I = I_{Rs} + 1mA$

$= \frac{V}{R_s} + 1mA$

$I = \frac{1}{R_s} V + 1mA$

$y = mx + c$

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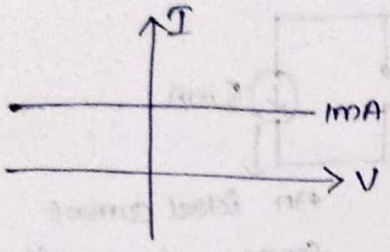
$I \to y$; $V \to x$

$I = 1mA$

$I = 0.V + 1mA$

$y = mx + C$

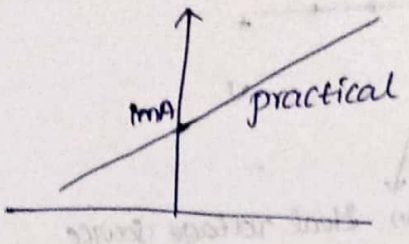
slope, $m = 0$



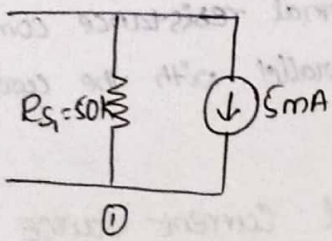
$I = \frac{1}{R_s} V + 1mA$

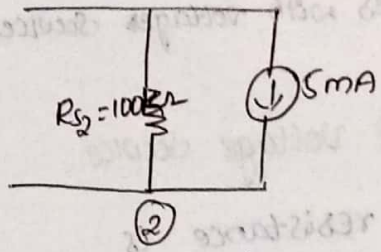
$y = mx + C$

slope, $m = \frac{1}{R_s}$

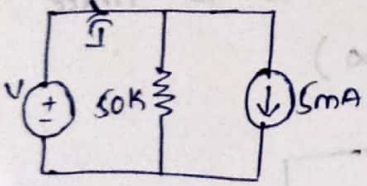


Q. Among the following current sources as shown in fig. below which is a better current source?





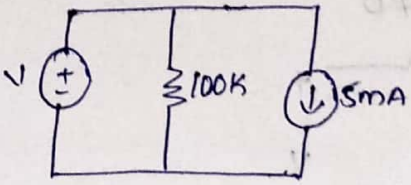
By observation, both are of same magnitude.



$I = I_{RS_1} + 5mA$

$I = \frac{1}{R_{S_1}} V + 5mA$

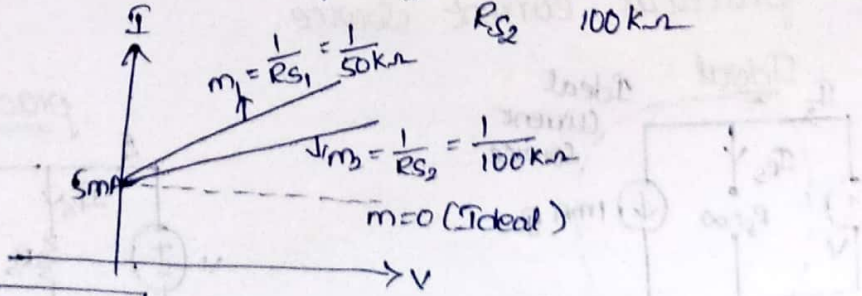
slope, $m_1 = \frac{1}{R_{S_1}} = \frac{1}{50K\Omega}$



$I = I_{RS_2} + 5mA$

$I = \frac{1}{R_{S_2}} V + 5mA$

slope, $m_2 = \frac{1}{R_{S_2}} = \frac{1}{100K\Omega}$



By observation $\boxed{m_1 > m_2}$

⇒ The I-V characteristics of current source '2' is closer to ideal current source characteristics compared to the I-V characteristics of current source '1'.

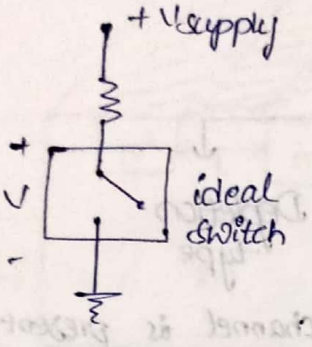
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$\therefore m_1 > m_2$

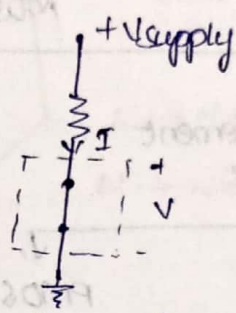
$\Rightarrow \frac{1}{R_{S_1}} > \frac{1}{R_{S_2}} \Rightarrow \boxed{R_{S_2} > R_{S_1}}$

* Whatever current source is having higher internal resistance will be considered as a better current source.

Ideal Switch



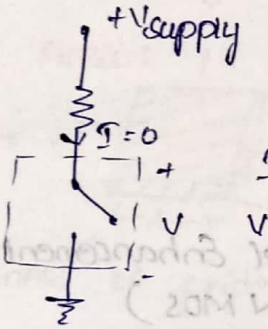
* When switch is 'ON'.



By observation; V = 0 (logic 0)

$I = \frac{V_{supply}}{R}$

* When switch is 'OFF'

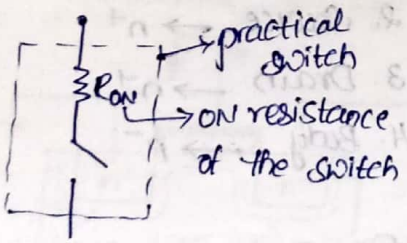


I = 0

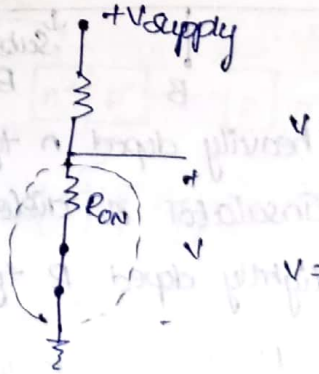
V = Vsupply (logic 1)

Ideal Switch	V
OFF	Vsupply (V) (logic '1', logic high
ON	0V logic '0' logic Low

Practical Switch



* When switch ON



$V = \frac{R_{ON}}{R_{ON}+R} V_{supp}$

$V \neq 0$

practical switch	V
ON	$\frac{R_{ON}}{R_{ON}+R} V_{supply}$ logic '0' logic 'low'
OFF	V_{supply} logic '1' logic 'high'.

* When switch OFF

$V = V_{supply}$.

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* ON resistance of an ideal switch is $R_{ON} = 0\,\Omega$

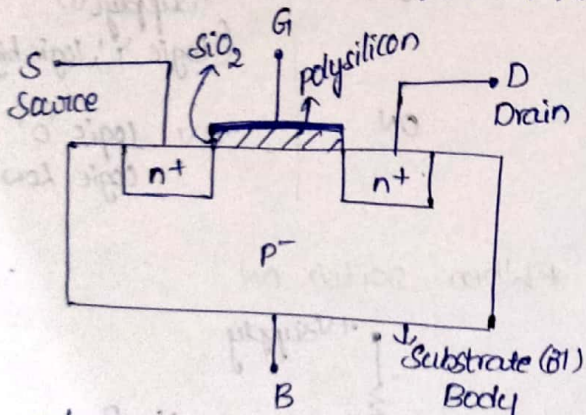
* A MOSFET can act as switch, current source, resistor, capacitor by operating in different regions.

8/12/21

MOSFET :- Metal Oxide Semiconductor Field Effect transistor
↓ polysilicon. (small)

MOSFET
- Enhancement Type
  - NMOS → n-channel Enhancement type MOSFET
  - PMOS → P channel Enhancement type Mosfet.
- Depletion type → channel is present at time of fabrication.

Construction of MOSFET (N-channel Enhancement type (or) NMOS)

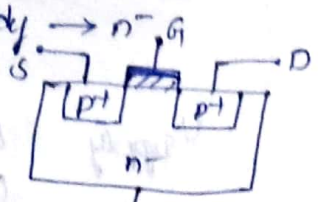


4 terminals
1. Gate → polysilicon
2. Source → n^+
3. Drain → n^+
4. Body → P^-

n^+ → heavily doped n type
SiO_2 → Insulator or dielectric
P^- → lightly doped P type.

	NMOS	PMOS
Source	n^+	p^+
Drain	n^+	p^+
Body	P^-	n^-
☆	$V_D > V_S$	$V_S > V_D$

* For P channel Enhancement type PMOS
1. Gate → polysilicon
2. Source → p^+
3. Drain → p^+
4. Body → n^-

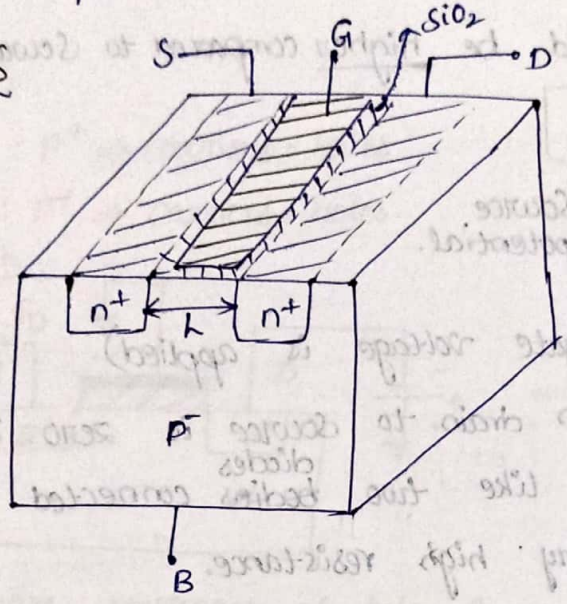


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* Source terminal : From this terminal carries will start (Bowler) ↓ e^- or holes.

* Drain terminal : the carriers coming from source will reach (Wicket keeper) drain.

NMOS

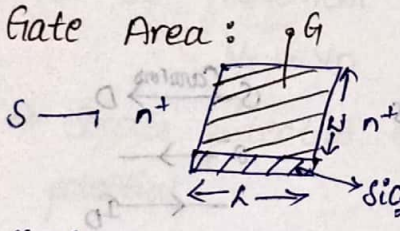


Cross sectional view

L → channel length of NMOS

W → width of NMOS

* Gate Area :



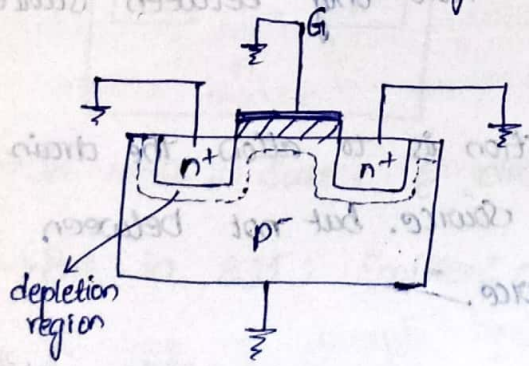
total gate Area = W.L

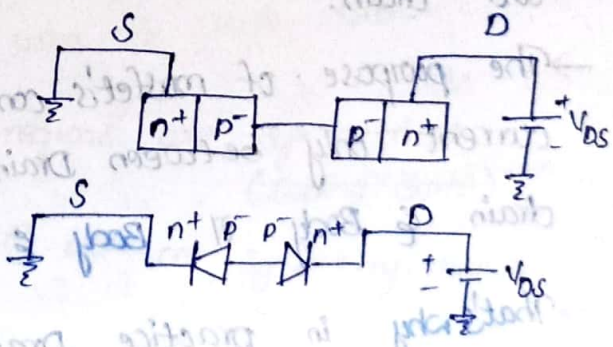
* thickness of oxide layer (SiO_2) is from 2 mm to 50 mm

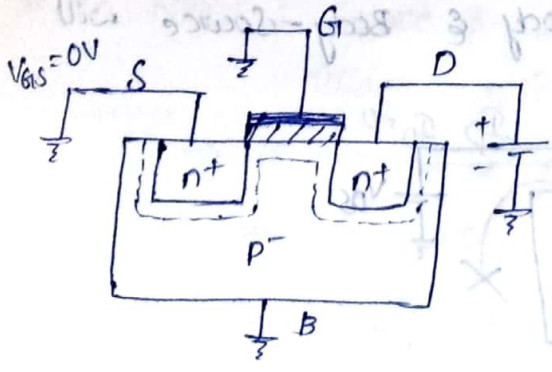
* Designer has a control over W & L of a MOSFET.

* What happens when no gate voltage is applied.

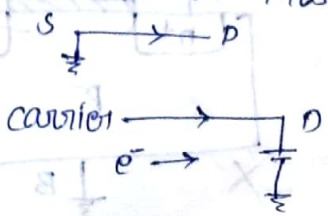
Gate to source voltage i.e., $V_{GS} = 0V$.







* In order to have current flow in MOSFET



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* Source $n^+ \longrightarrow$ Carriers (e^-s)

  Drain $n^+ \longrightarrow$ Carriers (e^-s)

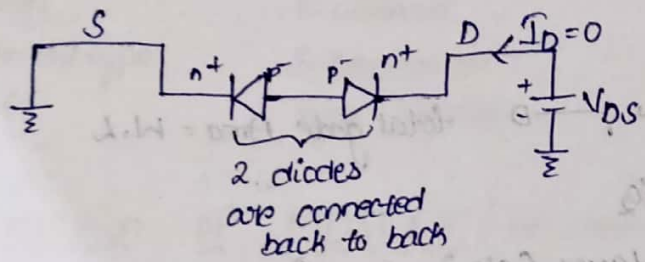
* For the carriers to start from source and to reach drain.

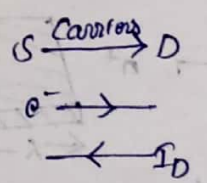
* Drain potential should be higher compared to source potential

* In NMOS: $V_D > V_S$

  V_D → Drain potential; V_S → Source potential.

* If $V_{GS} = 0V$ (NO gate voltage is applied) then the current from drain to source is zero. Bcz, as shown in fig. It is like two diodes bodies connected back to back which offers very high resistance.





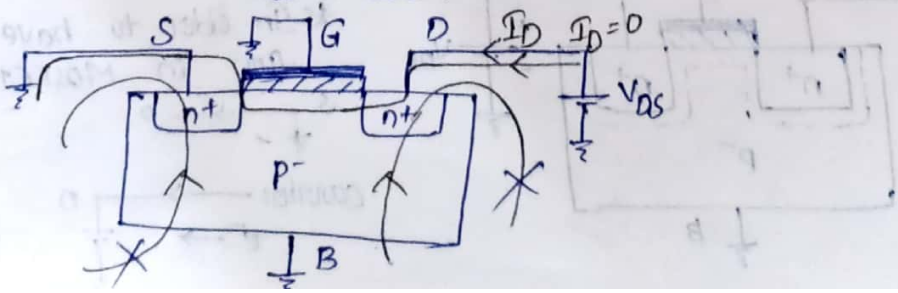
* NO channel Exists $\therefore I_D = 0$

Remember:

* We want our drain current to flow only between source and drain.

→ The purpose of mosfet's construction is to allow the drain current only between Drain & Source. But not between drain & Body & Body & Source.

→ That's why in practice Drain-Body & Body-Source will always be in reverse biased.



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* If $V_{GS} = 0V$ & $V_{DS} = 1V \Rightarrow I_D = ?$

i.e., Current shouldn't flow through

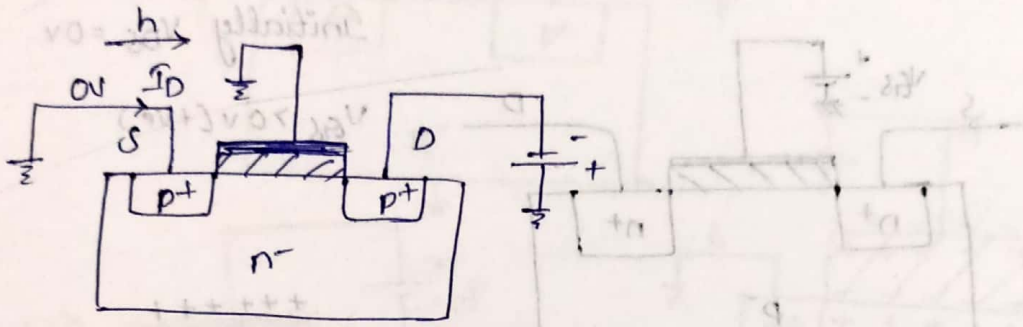
1. Body & Source regions 2. Body & drain regions.

$I_D = 0$ (NO channel)

P-MOS

Source : $P^+ \Rightarrow$ carriers = holes

Drain : $P^+ \Rightarrow$ carriers = holes.

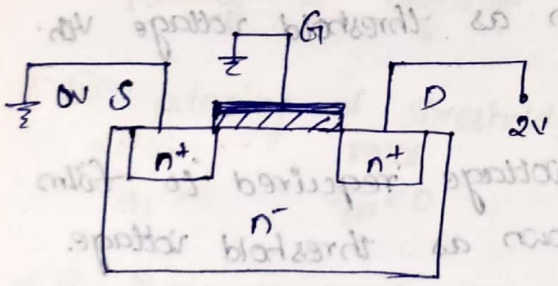


* For the movement of holes from source to drain,

$V_S > V_D$

$\Rightarrow$ Source potential should be more compared to drain potential.

* What if in NMOS substrate is also n^-



NMOS

$V_D > V_S$

→ In NMOS; Source & drain regions are symmetrical. (Doping same).

→ But in BJT; Emitter & collector are not symmetry.

* In NMOS; Source & drain are defined based on the voltage applied.

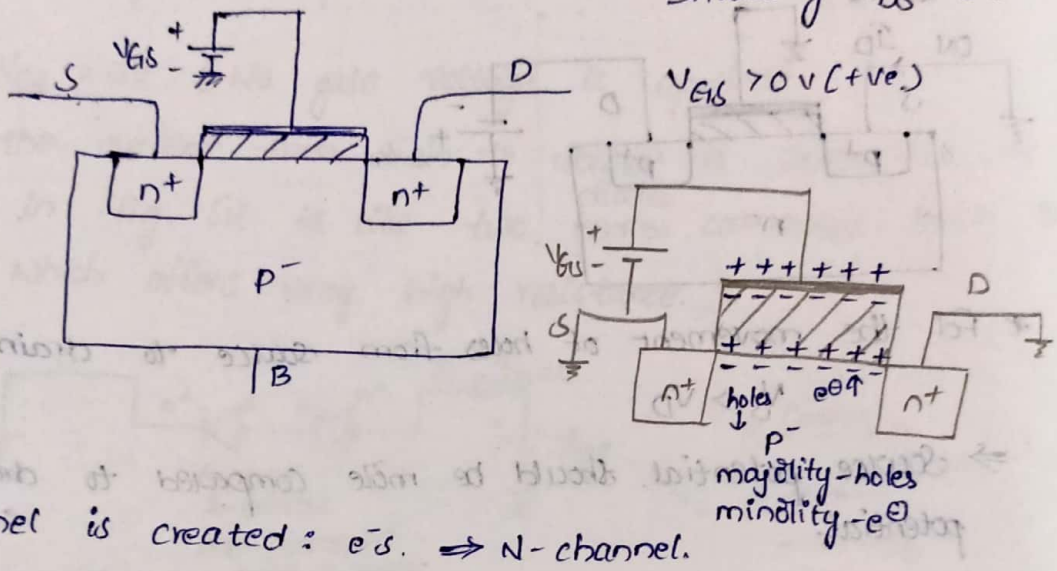
$\Rightarrow$ if terminal ① potential is more compared to ② then in NMOS; terminal ① is drain ($\because V_D > V_S$) terminal ② is source.

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* In PMOS; if terminal ① potential is more compared to terminal ②
then, terminal ① is source.
terminal ② is Drain.

14/2/21

* What HOW to create a n-channel in an N-MOS

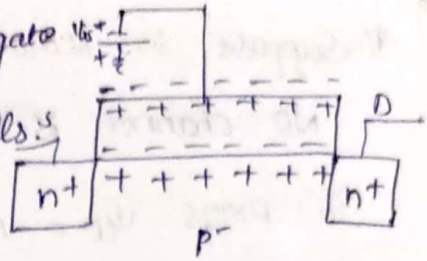


* channel is created : e⁻s. ⇒ N-channel.
* The minimum gate to source voltage V_{GS} applied so as to create a channel is known as threshold voltage V_{th}.
(or)
* The minimum gate to source voltage required to form an inversion layer is also known as threshold voltage.
* In NMOS: the polarity of threshold voltage is "positive."
* N-channel consists of e⁻s.
* The charge density in the channel depends on gate to source voltage.
⇒ More the V_{GS} ⇒ more the charge present in channel.
* If we apply $V_{GS} = -ve$ in an NMOS. Will there be any N-channel?
NO; N-channel is created. as we applying -ve to the gate

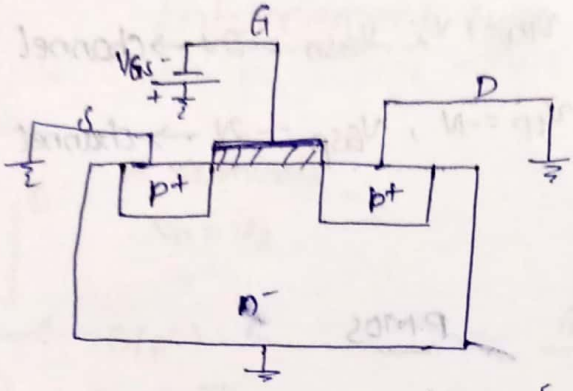
Scanned with CamScanner

then holes will get attracted to gate

⇒ No channel is created b/w n+ wells.

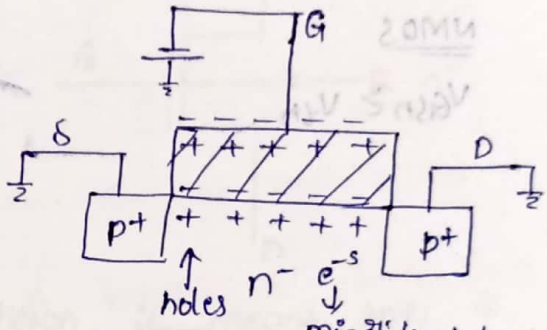


* How to create P-channel in a P-MOS.



$V_{SD} = 0V$

$V_{GS} < 0V$ (-ve)



⇒ P-channel of inversion layer is formed b/w S and D.

minority: holes
majority: e⁻

* The minimum gate to source voltage V_{GS} applied so as to create an inversion layer is known as threshold voltage V_{tp}.

→ Polarity is "negative." (PMOS)

* If polarity of threshold voltage in NMOS & PMOS.

NMOS PMOS

$V_{th} > 0$; $V_{tp} < 0$

* In order to create a channel in NMOS & PMOS what should be the condition of polarity of gate to source voltage in both transistors.

NMOS, $V_{GSn} > 0$ $V_{GSn} \geq V_{tn}$

PMOS, $V_{GSP} < 0$ $V_{GSP} \leq V_{tp}$

SG SG

* For N-channel to exists : $V_{GSn} \geq V_{tn}$ (+ve)

P-channel to exists : $V_{GSP} \leq V_{tp}$ → (-ve)

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* Suppose in NMOS $V_{th} = 1V$, $V_{GSn} = 0.7V$

NO channel is ~~formed~~. ($V_{GSn} \geq V_{th}$)

In PMOS $V_{tp} = -1V$, $V_{GSp} = -0.7V$

NO channel is ~~formed~~. ($V_{GSp} \leq V_{tp}$)

* Suppose in NMOS $V_{th} = 1V$, $V_{GSn} = 2V \rightarrow$ channel creats.

PMOS $V_{tp} = -1V$, $V_{GSp} = -2V \rightarrow$ channel creates.

* channel to create

NMOS

$V_{GSn} \geq V_{th}$

PMOS

$V_{GSp} \leq V_{tp}$

$V_{GSp} - V_{SP} \leq V_{tp}$

$-(V_{GP} - V_{SP}) \geq -V_{tp}$ ($V_{tp} = -ve$)

$V_{SP} - V_{GP} \geq |V_{tp}|$ (+ve)

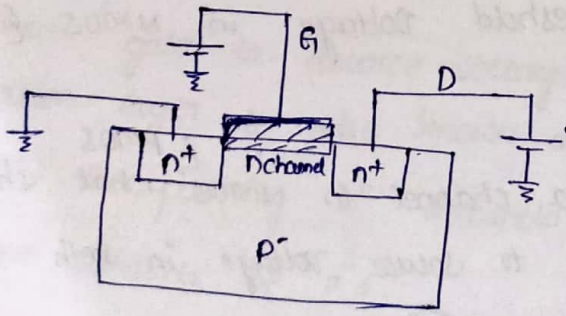
$V_{SGP} \geq |V_{tp}|$ → condition for channel to exists in PMOS

* NMOS : $V_{GSn} \geq V_{th}$

PMOS : $V_{GSp} \leq V_{tp}$ (-ve)

$V_{SGp} \geq |V_{tp}|$

*



$V_{GS} > V_{th}$ → channel creates

$V_{DS} = 0V$ → No potential difference.

$\Rightarrow I_D = 0$

* Why the name Enhancement?

Before applying V_{GS} ; no channel is present.

After applying $V_{GSn} \geq V_{th}$ (NMOS) & $V_{GSp} \geq |V_{tp}|$ (PMOS) an inversion layer & channel has been created. That's y this name came Enhancement type.

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* What is Depletion type MOSFET

A channel is already existing even if $V_{GS} = 0V$.

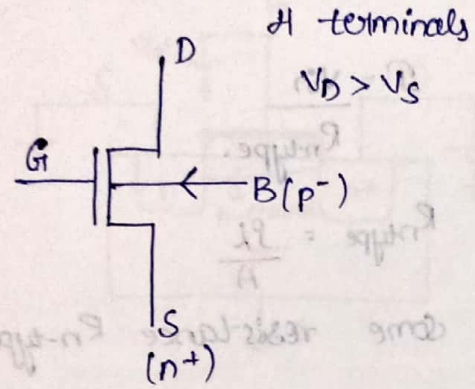
that's why it is depletion type

15/12/21

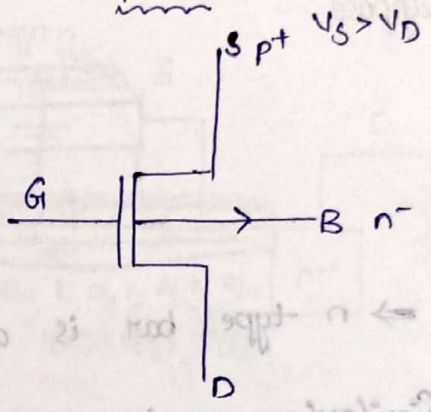
Symbols.

Enhancement type MOSFET

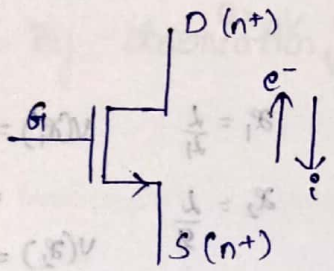
NMOS

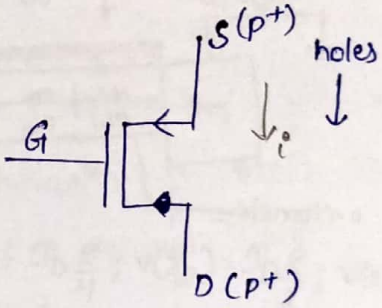


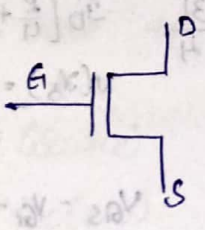
PMOS

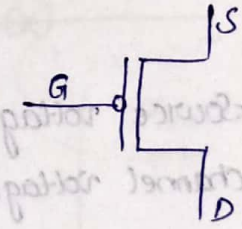


When only 3 terminals are shown, it means body is tied to source.





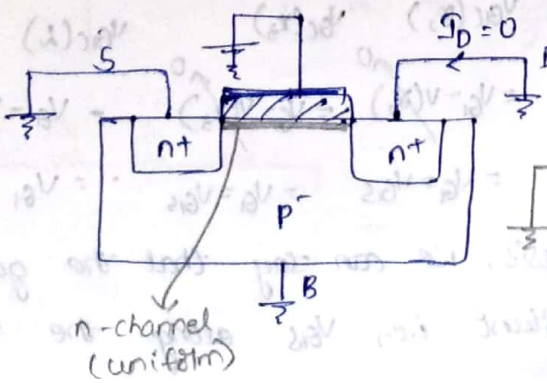


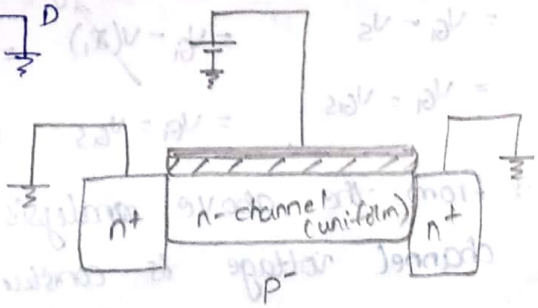


Uniform channel :-

let's take NMOS

$V_{GSn} \geq V_{th}$ & $V_{DS} = 0 \Rightarrow I_D = 0$





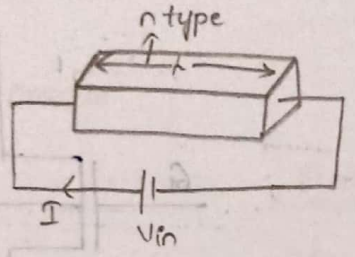
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* The charge density or charge depth is constant throughout the length of the channel from Source to Drain is uniform channel.

* The charge present in channel depends on the gate to source voltage.

If V_{GS} is more ⇒ charge present in channel is also more.

* Suppose

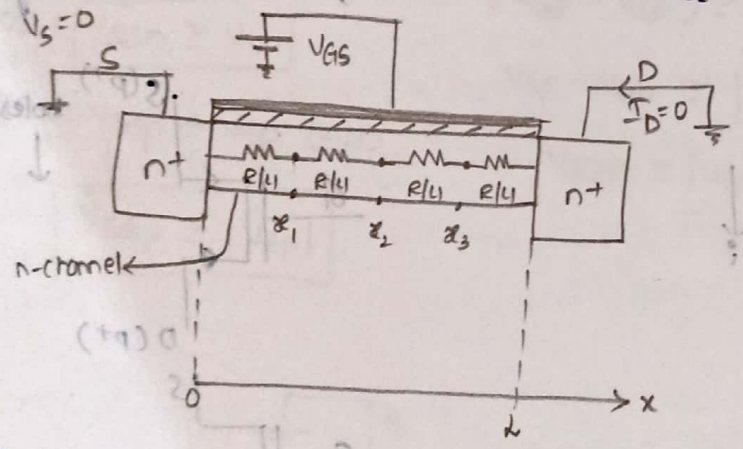


$$I = \frac{V_{in}}{R_{n\text{-type}}}$$

$$R_{n\text{type}} = \frac{\rho L}{A}$$

⇒ n type bar is also having some resistance $R_{n\text{-type}}$.

* Similarly n-channel is also modelled as a resistance 'R'



$x_1 = \frac{L}{4}$ $\quad V(x_1) = I_D \frac{R}{4} = 0$

$x_2 = \frac{L}{2}$ $\quad V(x_2) = I_D\left[\frac{R}{4} + \frac{R}{4}\right] = 0$

$x_3 = \frac{3L}{4}$ $\quad V(x_3) = I_D\left(3\frac{R}{4}\right) = 0$

→ Gate to Source voltage = V_{GS}

→ Gate to channel voltage = $V_{GC}(x) = V_G - V(x)$

$V_{GS} = V_G - V_S$

$= V_G$

→ $V_{GC}(x)$:

$x = 0$ (Source)	x_1	x_2	x_3	$x = L$ (Drain)
$V_{GC}(0)$	$V_{GC}(x_1)$	$V_{GC}(x_2)$	$V_{GC}(x_3)$	$V_{GC}(L)$
$= V_G - V_S$	$= V_G - V(x_1)$	$= V_G - V(x_2)$	$= V_G - V(x_3)$	$= V_G - V_D$
$= V_G = V_{GS}$	$= V_G = V_{GS}$	$= V_G = V_{GS}$	$= V_G = V_{GS}$	$= V_G = V_{GS}$

* From the above analysis, we can say that the gate to channel voltage is constant i.e., V_{GS} along the length of

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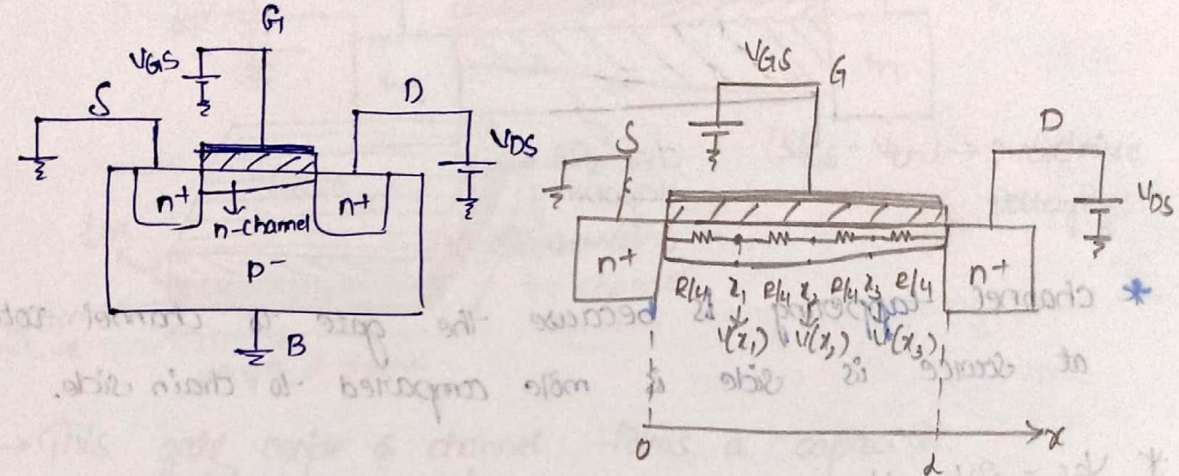
channel from source towards drain.

⇒ The charge depth is also constant throughout the length of the channel.

⇒ This is known as "uniform channel."

* What happens if $V_{GS} \geq V_{tn}$ & $V_{DS} > 0$

⇒ channel is created & $I_D > 0$



⇒ Here also channel is modelled with a resistor 'R'.

By observation, $V_S = 0$

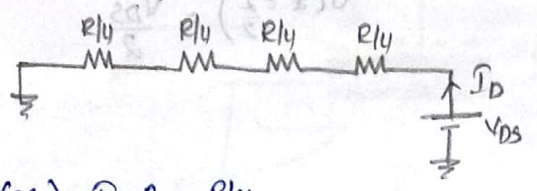
$\Rightarrow V_{GS} = V_G - V_S = V_G$

$\Rightarrow V_G = V_{GS}$

$V_D = V_{DS}$; $V(x_1) = I_D \frac{R}{4}$; $V(x_2) = I_D \frac{R}{2}$; $V(x_3) = I_D \frac{3R}{4}$

⇒ Gate to channel voltage $V_{GC}(x)$

$x = 0$ (Source)	x_1	x_2	x_3	$x = L$ (Drain)
$V_{GC}(x=0)$	$V_{GC}(x_1)$			
$= V_G - V_S$	$= V_G - V(x_1)$	$= V_G - V(x_2)$	$V_G - V(x_3)$	$V_{GS} - V_{DS}$
$= V_G = V_{GS}$	$= V_G - \frac{V_{DS}}{4}$	$= V_G - \frac{V_{DS}}{2}$	$= V_G - \frac{3V_{DS}}{4}$	
$V_{GC}(x=0) = V_{GS}$	$V_{GC} = V_{GS} - \frac{V_{DS}}{4}$	$V_{GC} = V_{GS} - \frac{V_{DS}}{2}$	$V_{GC} = V_{GS} - \frac{3V_{DS}}{4}$	$V_{GC} = V_{GS} - V_{DS}$

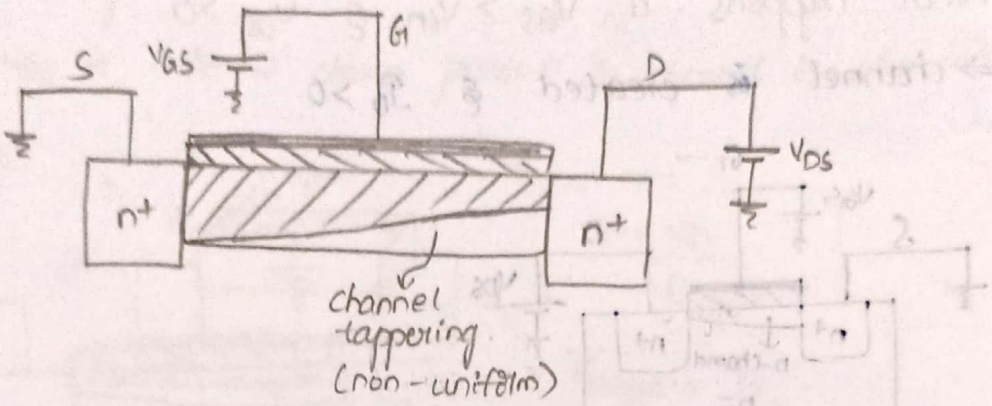


$V(x_1) = I_D \cdot \frac{R}{4} = \frac{R/4}{R} \times V_{DS} = \frac{V_{DS}}{4}$; $V(x_2) = \frac{V_{DS}}{2}$; $V(x_3) = \frac{3V_{DS}}{4}$

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* By observation, the gate to channel voltage keeps on decreasing as we move from source towards drain.

⇒ the channel depth is more at source side compared to drain side. This is known as "channel tappering."



* channel tappering is because the gate to channel voltage at source is side is more compared to drain side.

* $V_{GS} = 2V$, $V_{th} = 1V$, $V_{DS} = 0$ NMOS

Gate to channel voltage at $x = \frac{L}{2} = ?$

By observation: $I_D = 0$

⇒ Gate to channel voltage is constant throughout the channel $= V_{GSn}$

$= 2V$

$V_{GC}(x=0) = V_{GC}(x=\frac{L}{4}) = V_{GC}(x=\frac{L}{2}) = V_{GC}(\frac{3L}{4}) = V_{GC}(L) = 2V.$

⇒ Uniform channel.

* $V_{GSn} = 3V$, $V_{th} = 1V$, $V_{DSn} = 1V$

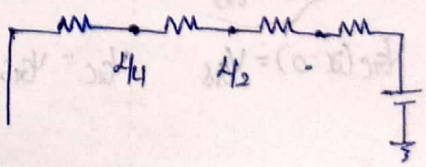
$V_{GC}(x=\frac{L}{2}) = ?$

$V_{GC}(x=\frac{L}{2}) = V_G - V(x=\frac{L}{2})$

$= V_{GS} - \frac{V_{DS}}{2}$

$= 3 - \frac{1}{2}$

$= 2.5\ V$



$V(x=\frac{L}{2}) = \frac{V_{DS}}{2}$

$V_{GC}(x=L) = V_{GS} - V_{DS} = 3V - 1V = 2V$ (Drain)

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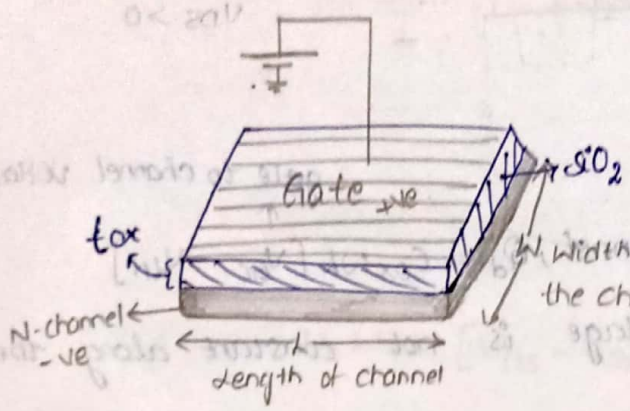
$V_{GC}(x=0) = V_{GS} = 3V$. (source)

$\Rightarrow$ Non-Uniform $\Rightarrow$ channel tapering.

16/12/21

Derive the

Gate Oxide Capacitance



$(V_{GS} - V_{th})$ → overdrive voltage

→ This gate oxide & channel forms a capacitor.
(+ve) ↓ dielectric (-ve) ↓

→ Total gate area = W×L ; t_{ox} = thickness of oxide layer = 2nm to 50nm.

→ Total gate oxide capacitance,

$$C = \frac{\epsilon A}{d}$$

$A = W \times L$

$d = t_{ox}$

$$C = \frac{\epsilon_{ox}\epsilon_0 WL}{t_{ox}} \quad (F)$$

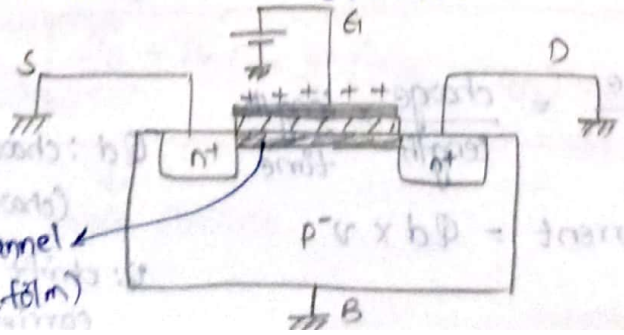
$\epsilon = \epsilon_r \epsilon_0$

capacitance per unit Area length, $\frac{C}{WL} = \frac{\epsilon_{ox}\epsilon_0}{t_{ox}}$

$$C_{ox} = \frac{\epsilon_{ox}\epsilon_0}{t_{ox}} \quad (F/m^2)$$

total gate oxide capacitance, $C = C_{ox} \times WL$

Derive the drain current I_D equation in an N-channel Enhancement type MOSFET



$V_{GS} > V_{th}$

$(V_{GS} - V_{th})$ → overdrive voltage.

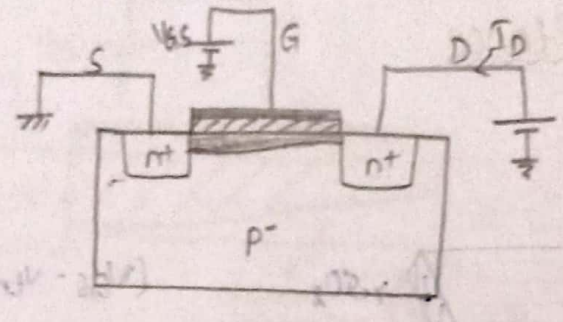
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Total charge present in an uniform channel:

$$Q = C_{ox} W L [V_{GS} - V_{tn}]$$

(as we know $Q = CV$)

charge per unit length, $Q_d = \frac{Q}{L} = WC_{ox}[V_{GS} - V_{tn}]$



$V_{GS} > V_{tn}$

$V_{DS} > 0$

gate to channel voltage.

total charge present in channel, $Q_d = C_{ox} W L [V_{GC} - V_{tn}]$

→ Here gate to channel voltage is not constant along the length of the channel.

$V_{GC}(x=0) = V_{GS}$ (source)

$V_{GC}(x=L) = V_{GS} - V_{DS}$ Drain

Charge per unit length, $Q_d(x) = \frac{Q}{L} = WC_{ox}[V_{GS} - V(x) - V_{tn}]$

$\because V_{GC}(x) = V_G - V(x)$

$= V_{GS} - V(x)$

[n-channel carriers: e⁻s]

$Q_d(x) = \frac{Q}{L} = WC_{ox}[(V_{GS} - V_{tn}) - V(x)]$

units: $\frac{\text{columbs}}{\text{meter}}$.

C_{ox}: gate oxide capacitance per unit area

W: width of the channel.

$V(x)$: potential of channel at point 'x'.

$(V_{GS} - V_{tn})$: Overdrive voltage.

as per def:

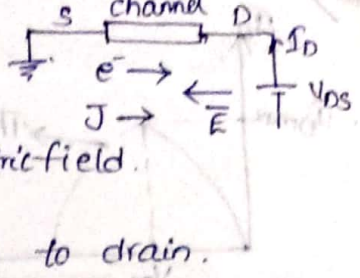
$$\text{current} = \frac{\text{charge}}{\text{time}} = \frac{\text{charge}}{\text{length}} \times \frac{\text{length}}{\text{time}}$$

$$\text{current} = Q_d \times v$$

Q_d: charge density (charge/ unit length)

v: drift velocity of carriers.

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$\therefore$ Drain current, $I_D = Q_d \times v$

drift velocity, $\vec{v} = -\mu_n \vec{E}$ → Electric field.

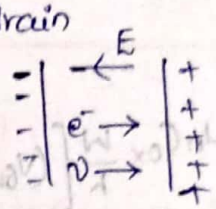
→ the direction of e's is from source to drain.

$\therefore$ the drift velocity of e's is also from source to drain.

⇒ Electric field E is from source to drain

$\Rightarrow \vec{v} = -\mu_n \vec{E}$ $\left[\because E = -\frac{dV}{dx}\right.$

$\Leftrightarrow v = \mu_n \frac{dV}{dx}$

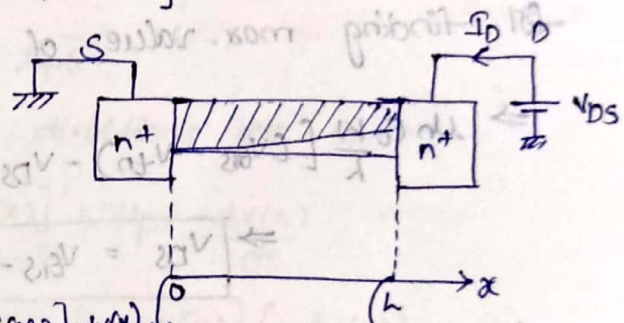


$I_D = Q_d(x) \cdot \mu_n \frac{dV(x)}{dx}$ $\quad \therefore I_D$ is constant throughout the length of the channel.

$I_D dx = \mu_n W C_{ox} [V_{GS} - V_{th} - V(x)] dV(x)$

range x : 0 to L

$V(x)$: 0 to V_{DS}



Integrate on B.S

$$\int_{x=0}^{L} I_D dx = \mu_n \int_{V(x)=0}^{V_{DS}} W C_{ox} [V_{GS} - V_{th} - V(x)] dV(x)$$

$V_c(x=0) = 0V$ $\quad V(x=L) = V_{DS}$

$\therefore I_D$ is constant throughout the length of the channel

$$I_D \int_0^L dx = \mu_n W C_{ox} \left[\int_0^{V_{DS}} (V_{GS} - V_{th}) dV(x) - \int_0^{V_{DS}} V(x) dV(x) \right]$$

$$I_D [x]_0^L = \mu_n W C_{ox} \left[(V_{GS} - V_{th}) \int_0^{V_{DS}} dV(x) - \frac{V^2(x)}{2} \Big|_0^{V_{DS}} \right]$$

$$I_D [L - 0] = \mu_n W C_{ox} \left[(V_{GS} - V_{th}) V(x) - \frac{1}{2} [V_{DS}^2 - 0^2] \right]$$

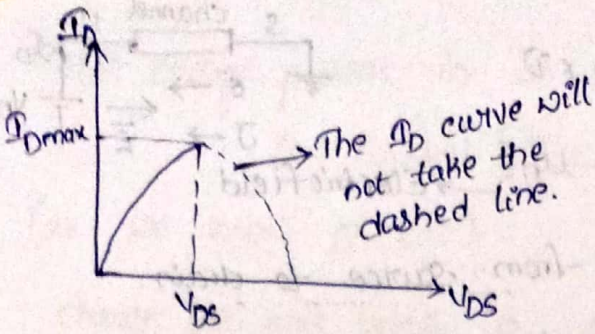
$$I_D = \mu_n \frac{W}{L} C_{ox} \left[(V_{GS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$\boxed{I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]}$$

↓

Drain Current.

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$I_D \rightarrow y$

$V_{DS} \rightarrow x$

$y = k_1 x - k_2 x^2$ (parabola)

finding max. value of I_D:

$y = f(x)$

for finding max. value of y

$\frac{dy}{dx} = 0$

$$\therefore \frac{\partial I_D}{\partial V_{DS}} = 0$$

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$\frac{\partial I_D}{\partial V_{DS}} = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{th}).1 - \frac{1}{2}.2 V_{DS}\right]$$

$$\frac{\partial I_D}{\partial V_{DS}} = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{th}) - V_{DS}\right]$$

for finding max. value of I_D, $\frac{\partial I_D}{\partial V_{DS}} = 0$

$$\Rightarrow \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{th}) - V_{DS}\right] = 0$$

$$\Rightarrow \boxed{V_{DS} = V_{GS} - V_{th}}$$

at $V_{DS} = V_{GS} - V_{th}$, I_D will reach its max. value.

to find I_{Dmax} put $V_{DS} = V_{GS} - V_{th}$ in I_D Eq.

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{th})(V_{GS} - V_{th}) - \frac{1}{2}(V_{GS} - V_{th})^2\right]$$

$$= \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{th})^2 - \frac{1}{2}(V_{GS} - V_{th})^2\right]$$

$$= \mu_n C_{ox} \frac{W}{L} \cdot \frac{1}{2}(V_{GS} - V_{th})^2$$

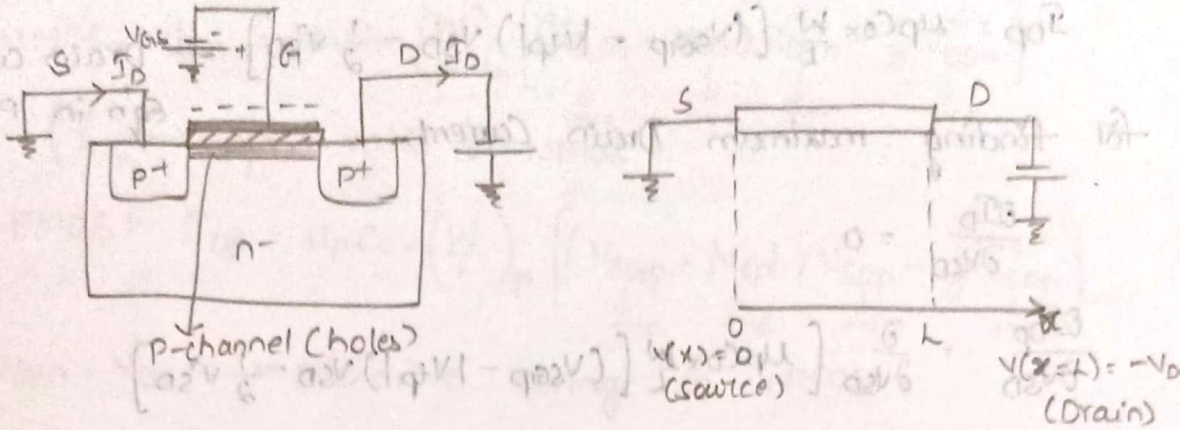
$$\boxed{I_{D(max)} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})^2}$$

$$\boxed{I_{D(max)} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}[V_{OV}]^2}$$

V_{OV} : overdrive voltage $= V_{GS} - V_{th}$

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Derive I_D Eqn in PMOS



Charge present in the channel, $Q = C_{ox} W L (V_{GC} - V_{tp})$

$$Q_d = \frac{Q}{L} = W C_{ox} [V_{GSp} - V(x) - V_{tp}]$$

$V_{GC}\big|_{x=0} = V_{GS} - 0 = V_{GS}$

$V_{GC}\big|_{x=L} = V_{GS} + V_{DS}$

Drain current, $I_{Dp} = Q_d \times v$

$\bar{v} = \mu_p \bar{E}$

→ Both holes & electric field directions are same.

$$I_{Dp} = W C_{ox} [V_{GSp} - V_{tp} - V(x)] \times \mu_p x \frac{-dV(x)}{dx}$$

$$I_{Dp}\, dx = -\mu_p C_{ox} W [V_{GSp} - V_{tp} - V(x)] (-dV(x))$$

$$I_{Dp} dx = -\mu_p C_{ox} W [V_{GSp} - V_{tp} - V(x)]\, dV(x)$$

$$\int_0^L I_{Dp} dx = -\mu_p C_{ox} W \left[\int_0^{-V_{DS}} (V_{GSp} - V_{tp})\, dV(x) - \int_0^{-V_{DS}} V(x)\, dV(x) \right]$$

$$I_{Dp}\, x\Big]_0^L = -\mu_p C_{ox} W \left[(V_{GSp} - V_{tp})(-V_{DS}) - \frac{V^2(x)}{2} \Big]_0^{-V_{DS}} \right)$$

$$I_{Dp} = \mu_p C_{ox} \frac{W}{L} \left[-(V_{GSp} - V_{tp})(-V_{DS}) - \frac{V_{DS}^2}{2} \right]$$

$V_{GSp} = V_{Gp} - V_{Sp} = -(V_{Sp} - V_{Gp}) = -V_{SGp}$

$$\boxed{V_{SGp} = -V_{GSp}}$$

$V_{DS} = V_D - V_S = -(V_S - V_D) = -V_{SD}$

$$\boxed{V_{SD} = -V_{DS}}$$

$-V_{tp} = |V_{tp}|$

PMOS:
- $V_{GSp} = -ve$
- $V_{SGp} = +ve$
- $V_{DS} \to -ve$
- $V_{SD} \to +ve$

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$$\Rightarrow I_{Dp} = \mu_p C_{ox} \frac{W}{L}\left[-(-V_{SGip} + |V_{tp}|)V_{SD} - \frac{1}{2}V_{SD}^2\right]$$

$$I_{Dp} = \mu_p C_{ox} \frac{W}{L}\left[(V_{SGip} - |V_{tp}|)V_{SD} - \frac{1}{2}V_{SD}^2\right] \rightarrow \text{Drain current Eq'n in PMOS}$$

for finding maximum Drain Current,

$$\frac{\partial I_D}{\partial V_{SD}} = 0$$

$$\frac{\partial I_{Dp}}{\partial V_{SD}} = \frac{\partial}{\partial V_{SD}}\left[\mu_p C_{ox} \frac{W}{L}\left[(V_{SGip} - |V_{tp}|)V_{SD} - \frac{1}{2}V_{SD}^2\right]\right]$$

$$0 = \mu_p C_{ox} \frac{W}{L}\left[(V_{SGip} - |V_{tp}|) - V_{SD}\right]$$

$$(V_{SGip} - |V_{tp}|) - V_{SD} = 0$$

$$V_{SD} = V_{SGip} - |V_{tp}|$$

at $V_{SD} = V_{SGip} - |V_{tp}|$ I_D will be maximum.

put $V_{SD} = V_{SGip} - |V_{tp}|$ in I_D Eq'n.

$$I_{Dp(max)} = \mu_p C_{ox} \frac{W}{L}\left[(V_{SGip} - |V_{tp}|)(V_{SGip} - |V_{tp}|) - \frac{1}{2}(V_{SGip} - |V_{tp}|)^2\right]$$

$$= \mu_p C_{ox} \frac{W}{L} \frac{1}{2}(V_{SGip} - |V_{tp}|)^2$$

$$\therefore I_{Dp(max)} = \frac{1}{2}\mu_p C_{ox} \frac{W}{L}\left[V_{SGip} - |V_{tp}|\right]^2$$

17/12/21

$\frac{W}{L}$ → Aspect ration

V_{DSn} - Drain to Source voltage (NMOS)

$I_D = (\mu_n C_{ox})\left(\frac{W}{L}\right)(V)^2$

I_D → A, V^2

$\mu_n C_{ox}$ = Amp/(Volt)^2 $\qquad \mu_n C_{ox} = \frac{A}{V^2}$

* In NMOS, given $\mu_n C_{ox} = 2\ mA/V^2$, $\left(\frac{W}{L}\right)_n = 2$, $V_{GSn} = 2V$, $V_{th} = 1V$, $V_{DSn} = 1V$ find I_{Dn}

$$I_{Dn} = \mu_n C_{ox}\left[\frac{W}{L}\right]\left[(V_{GSn} - V_{th})(V_{DSn}) - \frac{1}{2}V_{DSn}^2\right]$$

$$= 2m \times 2\left[(2V - 1V)1V - \frac{1}{2}1V\right]$$

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$I_{Dn} = 2\ mA$

* NMOS :- $I_{Dn} = \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[(V_{GSn} - V_{tn}) V_{DSn} - \frac{1}{2} V_{DSn}^2\right]$

(V_{GSn}: +ve, V_{tn}: +ve, V_{DSn}: +ve, V_{DSn}^2: +ve)

$\left(\frac{W}{L}\right)_n \rightarrow$ Aspect ratio of NMOS

* PMOS :- $I_{Dp} = \mu_p C_{ox} \left(\frac{W}{L}\right)_p \left[(V_{SGp} - |V_{tp}|) V_{SDp} - \frac{1}{2} V_{SDp}^2\right]$

(V_{SGp}: +ve, $|V_{tp}|$: +ve, V_{SDp}: +ve, V_{SDp}^2: +ve)

$V_{GSn} - V_{tn} \rightarrow$ Overdrive voltage in NMOS.

$V_{SGp} - |V_{tp}| \rightarrow$ Overdrive voltage in PMOS

$V_{DS} = V_{GSn} - V_{tn}$ at I_{Dmax} in NMOS.

When $V_{DSn} < V_{GSn} - V_{tn}$; what happens to the gate to channel voltage at drain side?,

$V_{GC}(x = L) = V_G - V(x = L)$

$= V_{GSn} - V_D$

$= V_{GSn} - V_{DSn}$

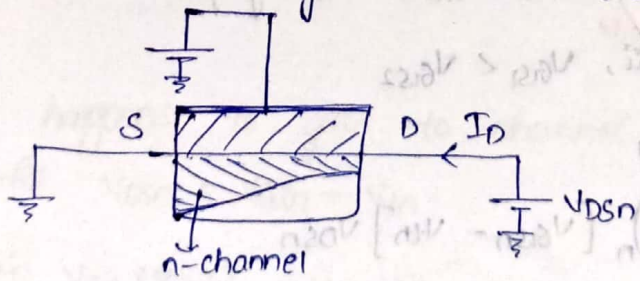
Eg: $V_{GSn} = 2V$, $V_{tn} = 1V$, $V_{DSn} = 0.5\ V$

$V_{DSn} < V_{GSn} - V_{th}$

$0.5 < 2 - 1 \Rightarrow 0.5 < 1V$ $\quad [V_{tn} < V_{GC}]$

$V_{GC}(x = L) > V_{tn}$

When $V_{DSn} < V_{GSn} - V_{tn} \Rightarrow$ the gate to channel voltage at drain side is greater than the threshold voltage.



$I_{Dn} = \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[\underbrace{(V_{GSn} - V_{th}) V_{DS}}_{①} - \underbrace{\frac{1}{2} V_{DS}^2}_{②}\right]$

If $(V_{GSn} - V_{tn}) V_{DS} = \frac{1}{2} V_{DS}^2$

$V_{DS} << 2 V_{GSn} - V_{tn}$

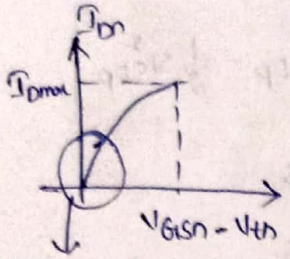
If this condition is true then we can neglect the second older term

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$\therefore I_{Dn} = \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[(V_{GSn} - V_{th})\right] V_{DSn}$; $V_{DS} << 2(V_{GSn} - V_{th})$

$R_{ON} = \frac{V_{DSn}}{I_{DSn}} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{GSn} - V_{th})}$

Here RON is on resistance of NMOS;



Here I_D is varying linearly with V_{DSn}

It means in this region, MOSFET behaves as a variable resistor

Here MOSFET behaves as a resistor in 'deep triode region.'

R_{ON} : ON resistance.

Q:- $\mu_n C_{ox} = 2mA/V^2$ (for $V_{DSn} << 2V_{OV}$)

$\left(\frac{W}{L}\right)_n = 2$

$V_{GSn} = 2V$

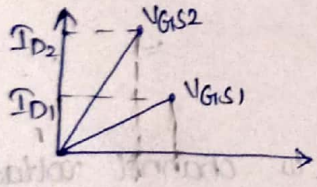
$V_{th} = 1V$

$R_{ON} = ?$

$R_{ON} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{GSn} - V_{th})}$

$= \frac{1}{2(2)(2-1)} = \frac{1}{4} = 0.250\,\Omega$

Problem:-



for $V_{DSn} << 2V_{OV}$

Here I_{D2} more than I_{D1}

1. Which is true for above from the graph.

i, $V_{GS1} > V_{GS2}$ ✓ ii, $V_{GS1} < V_{GS2}$

Sol:- for $V_{DSn} << 2V_{OV}$

$I_{Dn} = \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[V_{GSn} - V_{th}\right] V_{DSn}$

If V_{GSn} is more then I_D also more (directly proportional)

$\boxed{V_{GS1} < V_{GS2}}$

2. Which is true?

i, R_{ON} @ V_{GS1} > R_{ON} @ V_{GS2}

ii, R_{ON} @ V_{GS1} < R_{ON} @ V_{GS1}

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Sol $R_{ON} \propto \frac{1}{V_{GS} - V_D}$

* If $V_{GS} \uparrow$, $R_{ON} \downarrow$

here $V_{GS1} < V_{GS2}$ then $R_{ON1} > R_{ON2}$

or

If V_{GS} is more $\Rightarrow I_D$ is more $\Rightarrow R_{ON}$ is low.

Eg:- $\mu_n C_{ox} = 2m A/V^2$

$V_{tn} = 1V$, $\left(\frac{W}{L}\right)_n = 2$

case i, $V_{GSn} = 2V$

$$R_{ON} = \frac{1}{2 \times 2 \times (2-1)} = \frac{1}{4} = 250\Omega$$

case ii, $V_{GSn} = 3V$

$$R_{ON} = \frac{1}{2 \times 2 \times (3-1)} = \frac{1}{8} = 125\Omega$$

** $\Rightarrow R_{ON} \downarrow$ with $\uparrow$ in V_{GS}

$\Rightarrow R_{ON} \downarrow$ with $\uparrow$ in $\frac{W}{L}$.

ON Resistance :-

NMOS :- $$R_{ON} = \frac{V_{DSn}}{I_{Dn}} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{GSn} - V_{tn})}$$;

$V_{DSn} << 2(V_{GSn} - V_{tn})$

PMOS :- $$R_{ON} = \frac{V_{SDP}}{I_{DP}} = \frac{1}{\mu_p C_{ox} \left(\frac{W}{L}\right)_p (V_{SGp} - |V_{tp}|)}$$;

$V_{SDP} << 2(V_{SGp} - |V_{tp}|)$

* What happens to gate to channel voltage at the drain side for $V_{DSn} = V_{GSn} - V_{tn}$.

NMOS:- $V_{GC}(x = L) = V_G - V_D$

$= V_{GSn} - V_{DSn}$

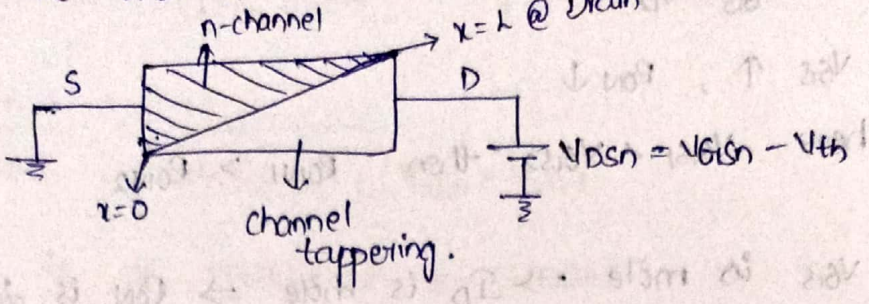
$= V_{GSn} - (V_{GSn} - V_{tn})$

$V_{GC}(x = L) = V_{tn}$

$\Rightarrow$ Gate to channel voltage at drain side is equal to threshold voltage V_{tn} for $V_{DSn} = V_{GSn} - V_{tn}$

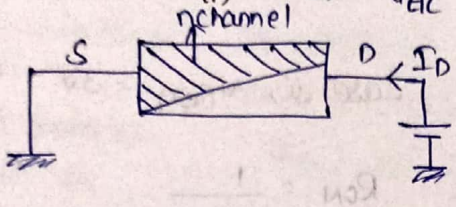
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⇒ Now the channel looks like



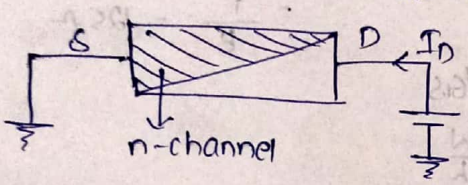
Channel's state at different Conditions :-

i, $V_{DSn} < V_{GSn} - V_{th}$ ⇒ V_{GC} (at drain) > V_{th}



triode

ii, $V_{DSn} = V_{GSn} - V_{th}$ ⇒ V_{GC} (@ drain) = V_{th}



Edge

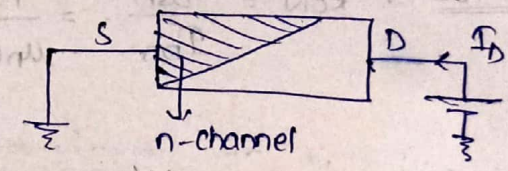
iii, $V_{DSn} > V_{GSn} - V_{th}$

$V_{GC}(x=L) = V_G - V(x=L)$

$= V_G - V_D$

$= V_{GSn} - V_{DSn}$

V_{GC} (@ drain) < V_{th}



saturation.

Eg:- $V_{GSn} = 2V$, $V_{th} = 1V$, $V_{DSn} = 1.5V$ $V_{DSn} > V_{GSn} - V_{th}$

$V_{GC}(x=L) = V_{GSn} - V_{DSn}$

$= 2 - 1.5V$

$= 0.5V$

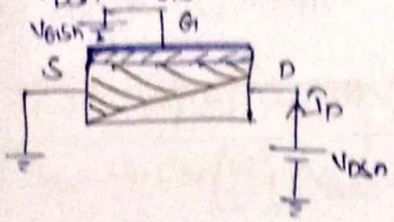
$V_{GC}(x=L) < V_{th}$ at drain.

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triode

$V_{DSn} < V_{GSn} - V_{tn}$



$V_{DSn} < V_{GSn} - V_{tn}$

$\Rightarrow V_{GSn} - V_{DSn} > V_{tn}$

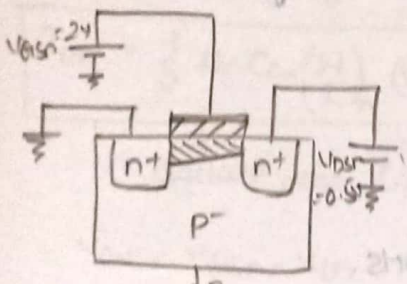
$V_G - V_S - (V_D - V_S) > V_{tn}$

$V_G - V_D > V_{tn}$

$V_{GD} > V_{tn}$

$\Rightarrow$ channel is present at the drain for $V_{GD} > V_{tn}$

$V_{tn} = 1V$



$V_{GSn} > V_{tn}$

By observation:

$V_{GSn} = V_G - V_S$

$= 2 - 0$

$= 2V$

$V_{GD} = V_G - V_D$

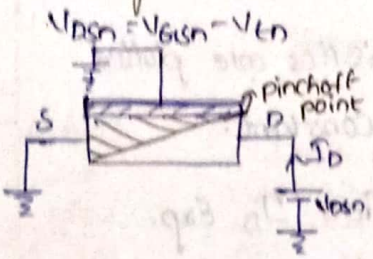
$= V_{GS} - V_{DS}$

$= 2 - 0.5 = 1.5V$

$(V_{GD} = 1.5V) > V_{tn}$

Edge of Sat

$V_{DSn} = V_{GSn} - V_{tn}$



$V_{DSn} = V_{GSn} - V_{tn}$

$\Rightarrow V_{GSn} - V_{DSn} = V_{tn}$

$V_G - V_S - (V_D - V_S) = V_{tn}$

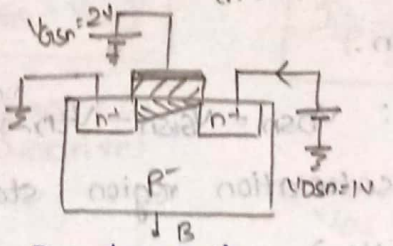
$V_G - V_D = V_{tn}$

$V_{GD} = V_{tn}$

$\Rightarrow$ gate to drain potential is just equal to threshold voltage.

$\Rightarrow$ Charge carriers depleted at drain side.

$V_{tn} = 1V$



By observation:

$V_{GSn} = V_G - V_S$

$= 2 - 0 = 2V.$

$V_{GSn} > V_{tn}$

$V_{GD} = V_G - V_D$

$= 2 - 1V$

$= 1V$

$V_{GD} = V_{tn}$

$V_{GS} - V_{DS} = V_{tn}$

$V_{DSn} = V_{GSn} - V_{tn}$

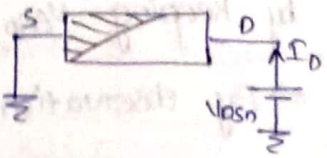
↓

Pinchoff voltage.

* at this voltage I_D remains constant.

Saturation

$V_{DSn} > V_{GSn} - V_{tn}$



$V_{DSn} > V_{GSn} - V_{tn}$

$\Rightarrow V_{GSn} - V_{DSn} < V_{tn}$

$V_G - V_S - (V_D - V_S) < V_{tn}$

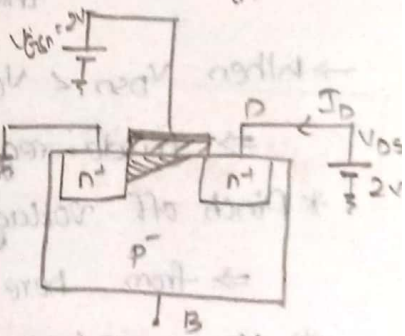
$V_G - V_D < V_{tn}$

$V_{GD} < V_{tn}$

$\Rightarrow$ No channel is present at drain.

$\because V_{GD} < V_{tn}$

$V_{tn} = 1V$



By observation

$(V_{GSn} = 2V) > V_{tn}$

$V_{GD} = 2 - 2$

$= 0V$

$V_{GD} < V_{tn}$

$\Rightarrow$ @ drain no channel.

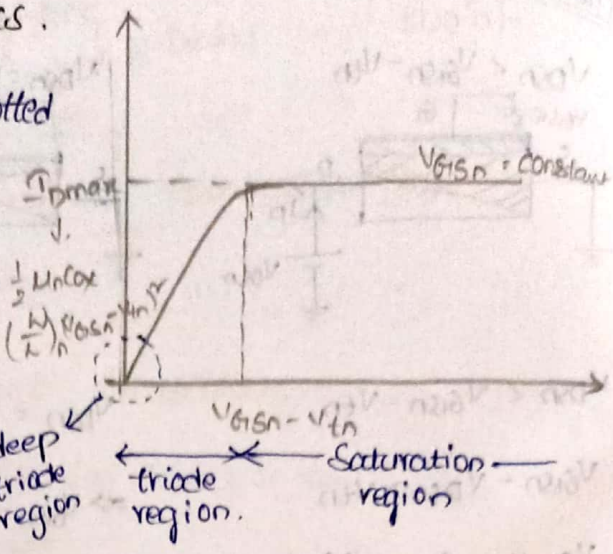
$\Rightarrow V_{GSn} - V_{DSn} < V_{tn}$

$\Rightarrow V_{DSn} > V_{GSn} - V_{tn}.$

In this, pinch off point will move from drain towards source.

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* I_D Vs V_{DS} characteristics.



the above characteristics are plotted by keeping V_{GSn} = constant.

⇒ By observation from I_D Exp. $\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSn} - V_{tn})^2$

$V_{GS} \uparrow \Rightarrow I_D \uparrow$.

⇒ For constant $V_{GSn} > V_{tn}$; I_D increases with V_{DS}.

→ When $V_{DSn} = V_{GSn} - V_{tn}$ then I_{Dn} reaches to a maximum value and it remains constant.

$$I_{Dn(max)} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSn} - V_{tn})^2$$

→ When $V_{DSn} \geq V_{GSn} - V_{tn}$

⇒ I_{Dn} remains constant.

therefore, this region is known as Saturation Region.

this is current Saturation Region.

→ When $V_{DSn} < V_{GSn} - V_{tn}$

⇒ triode region.

* Pinch off voltage: $V_{DSn} = V_{GSn} - V_{tn}$

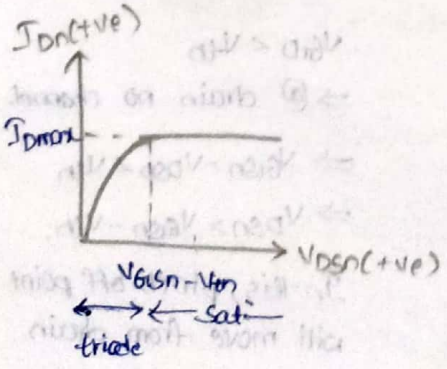
⇒ from here saturation region starts.

* $V_{DSn} << 2(V_{GSn} - V_{tn})$

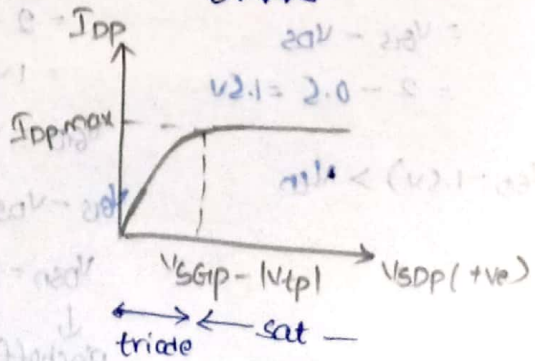
⇒ deep triode region. → MOSFET acts as a resistor.

* at pinchoff voltage, pinchoff points exactly at drain.

NMOS



PMOS



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triode region:-

$V_{DSn} < V_{GSn} - V_{tn}$

triode region current (drain)

$$I_{Dn} = \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[(V_{GSn} - V_{tn}) V_{DSn} - \frac{1}{2} V_{DSn}^2\right]$$

Saturation region:-

$V_{DSn} \geq V_{GSn} - V_{tn}$

Drain Current Eq

$I_{Dn} = I_{Dn\,max}$ | $@\, V_{DSn} = V_{GSn} - V_{tn}$

$$= \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[(V_{GSn} - V_{tn})(V_{GSn} - V_{tn}) - \frac{1}{2}(V_{GSn} - V_{tn})^2\right]$$

$$= \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[(V_{GSn} - V_{tn})^2 - \frac{1}{2}(V_{GSn} - V_{tn})^2\right]$$

$$I_{Dn} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{GS} - V_{tn})^2$$

↓ Square law. (dependent on overdrive).

$V_{ov} = V_{GSn} - V_{tn}$

Cutoff region

$V_{GSn} < V_{tn} \Rightarrow$ NO channel

$\Rightarrow I_D = 0$

$\Rightarrow$ NMOS OFF

triode region:-

$V_{SDp} < V_{SGp} - |V_{tp}|$

Drain Current in triode region

$$I_{Dp} = \mu_p C_{ox} \left(\frac{W}{L}\right)_p \left[(V_{SGp} - V_{tp}) V_{SDp} - \frac{1}{2} V_{SDp}^2\right]$$

Saturation region:-

$V_{SDp} \geq V_{SGp} - |V_{tp}|$

Drain Current Eq.

$I_{Dp} = I_{Dp\,max}$ | $@\, V_{DSp} = V_{SGp} - |V_{tp}|$

fly.

$$I_{Dp} = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_p \left[V_{SGp} - |V_{tp}|\right]^2$$

$V_{ov} = V_{SGp} - |V_{tp}|$

Cutoff region

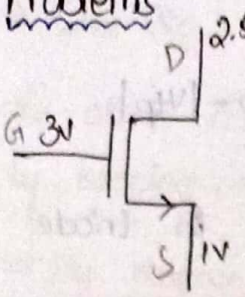
$V_{SGp} < |V_{tp}| \Rightarrow$ NO channel

$\Rightarrow I_D = 0$

$\Rightarrow$ PMOS OFF

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Problems



Given: $V_{tn} = 1V$

$V_{tp} = -1V$

$\mu_n C_{ox} = 1 mA/V^2$

$\mu_p C_{ox} = 0.5 mA/V^2$

$\frac{W}{L} = 2$

Find

i, Which MOSFET (NMOS/PMOS)

ii, Mark the terminals

iii, Region of operation

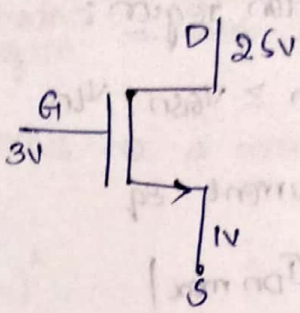
iv, Direction of I_D

v, I_D = ?

i, By observation from symbol : NMOS

ii, In NMOS : $V_D > V_S$

$\Rightarrow 2.5V \rightarrow D \; ; \; 1V \rightarrow S.$



iii, Region of operation

$V_{DSn} < V_{GSn} - V_{tn} \Rightarrow$ Triode

$V_{DSn} \geq V_{GSn} - V_{tn} \Rightarrow$ Sat

$V_{GSn} < V_{tn} \Rightarrow$ cutoff.

By observation

$V_G = 3V$, $V_S = 1V$ $\Big\}$ $V_{GSn} = V_G - V_S = 3 - 1$

$V_{GS} = 2V$

$V_D = 2.5V$

$V_{GSn} > V_{tn} \quad (2 > 1)$

$V_{DSn} = V_D - V_S$

$V_{GSn} - V_{tn} = 1V$

$= 2.5 - 1V = 1.5V$

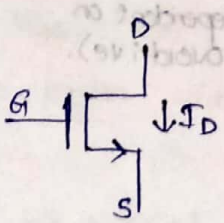
$V_{DSn} > V_{GSn} - V_{tn} \quad (1.5 > 1V)$

$\Rightarrow$ Saturation Region

iv, Direction of I_D

In NMOS : D $\longrightarrow$ S

I_D



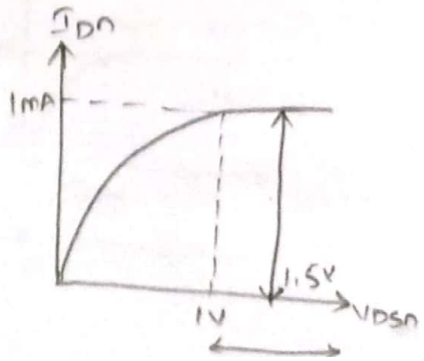
v, Drain Current

$\because$ NMOS is in Saturation region.

$$I_{Dn} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n [V_{GSn} - V_{tn}]^2$$

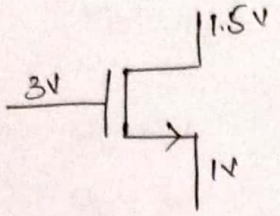
$$= \frac{1}{2} \times 1m \times 2 \times [2 - 1]^2$$

$$\boxed{I_{Dn} = 1mA}$$



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Problem:- Repeat the above problem for the MOS transistor as shown below. Take the data given in above problem.



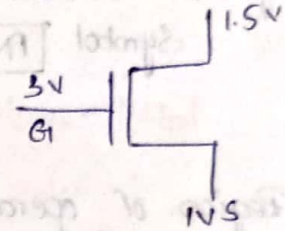
i, By observation from symbol "NMOS"

ii, Mark the terminals

NMOS: $V_D > V_S$

D → 1.5

S → 1V



iii, Region of operation

By observation:

$V_G = 3V$, $V_S = 1V$, $V_D = 1.5V$

$V_{GSn} = V_G - V_S = 3 - 1V = 2V$

$\Rightarrow V_{GSn} > V_{tn}$ $(2 > 1)$

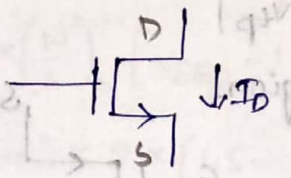
$V_{GSn} - V_{tn} = 1V$

$V_{DSn} = V_D - V_S = 1.5V - 1V = 0.5V$

$V_{DSn} < V_{GSn} - V_{tn} \Rightarrow$ triode region.

iv, direction of I_D

NMOS: $D \xrightarrow{I_D} S$

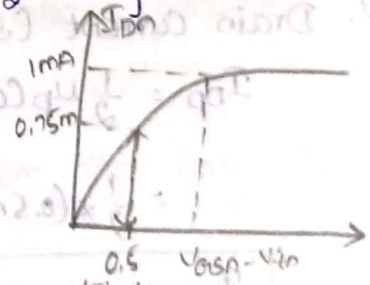


v, Drain current (triode region)

$$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[(V_{GSn} - V_{tn}) V_{DSn} - \frac{1}{2} V_{DSn}^2\right]$$

$$= 1m \times 2 \times \left[(2V - 1V)\,0.5 - \frac{1}{2} \times \frac{1}{4}\right]$$

$$I_D = 0.75\,mA$$

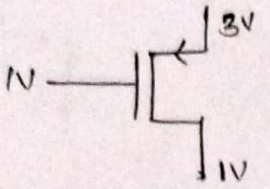


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N180119
M. Surya kumari.

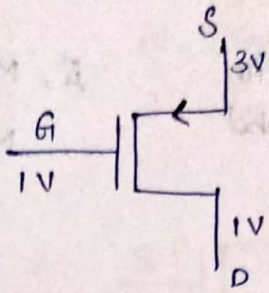
Problem

i, Repeat the above problem.



i, By observation : By Symbol PMOS

ii,



In PMOS

$V_S > V_D$

$V_D < V_S$

iii, Region of operation

$V_G = 1V$

$V_S = 3V$

$V_D = 1V$

$V_{SG} = V_S - V_G$

$= 3 - 1$

$= 2$

$V_{tp} = -1$

$|V_{tp}| = 1$

$V_{SGp} > |V_{tp}| \quad (2 > 1)$

$V_{SDp} = V_S - V_D$

$= 3 - 1$

$V_{SDp} = 2$

$V_{SGp} - |V_{tp}| = 2 - 1$

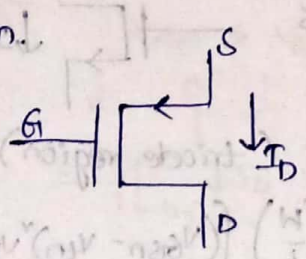
$V_{SGp} - |V_{tp}| = 1V$

$V_{SDp} > V_{SGp} - |V_{tp}|$

$\Rightarrow$ Saturation region.

iv, direction of I_D

S to D.



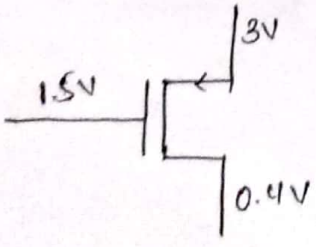
v, Drain current (saturation region)

$$I_{Dp} = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_p \left[V_{SGp} - |V_{tp}|\right]^2$$

$$= \frac{1}{2} \times (0.5m) \times 2 \left[2 - 1\right]^2$$

$$\boxed{I_{Dp} = 0.5 \text{ mA}}$$

ii,



i, By observation :-

By Symbol

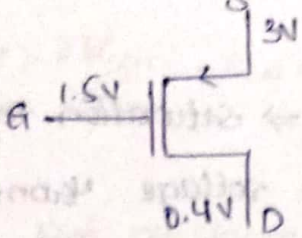
it is 'PMOS'

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ii, In PMOS

$V_S > V_D$

$V_D < V_S$



iii, $V_G = 1.5V$

$V_S = 3V$

$V_D = 0.4V$

$V_{SG} = V_S - V_G$

$= 3 - 1.5$

$V_{SGp} = 1.5V$

$V_{SDp} = V_S - V_D$

$= 3 - 0.4$

$= 2.6V$

$V_{SGp} - |V_{tp}|$

$= 1.5 - 1$

$= 0.5$

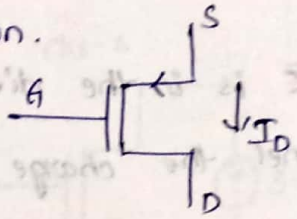
$V_{SGp} > |V_{tp}|$ (1.5 > 1)

$V_{SDp} > V_{SGp} - |V_{tp}|$ (2.6 > 0.5)

$\Rightarrow$ Saturation region.

iv, direction of I_D

S to D



v, Drain Current (Saturation region)

$$I_{Dp} = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_p [V_{SGp} - |V_{tp}|]^2$$

$$= \frac{1}{2} \times (0.5m) \times 2 \times [1.5 - 1]$$

$$\boxed{I_{Dp} = 0.125 \text{ mA}}$$

* How much is gate current in above problem?

$I_G = 0$

Because, the gate is insulated from the body by an insulator or dielectric

$\Rightarrow$ No current will flow from the gate.

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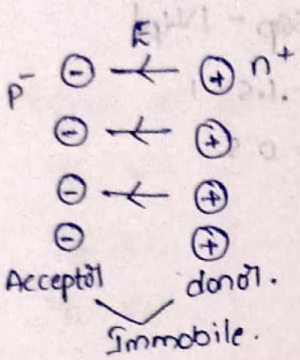
22/12/2

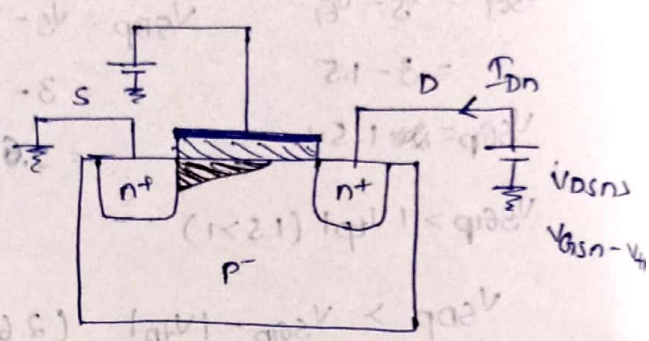
Doubt :- If $V_{DSn} > V_{GSn} - V_{tn}$ ⇒ saturation region.

then gate to drain voltage $V_{GDn} < V_{tn}$

⇒ No channel is present i.e., the carriers are depleted @ drain side.

⇒ If there is no channel at the drain then how does I_D will flow?





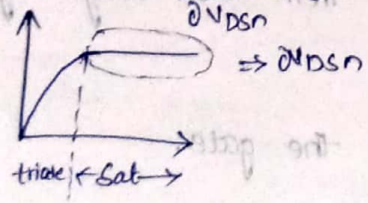
→ This Electric field $\bar{E}$ is in the direction of drain current I_{Dn} which will tunnel the charge carriers (e⁻s). therefore I_{Dn} will flow.

→ In saturation region, drain current I_{Dn} will be constant but ⇒ Hence MOSFET acts as a current source in saturation region.

*

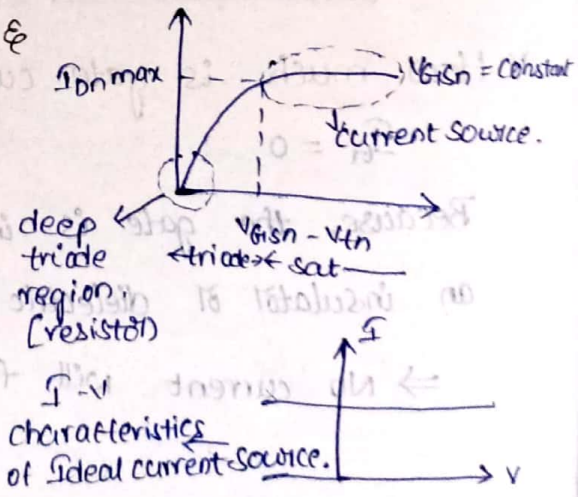
Q. In which region, among triode & saturation MOSFET is having higher resistance in ?

Sol triode.



$\frac{\partial I_{Dn}}{\partial V_{DSn}} = 0$

$\Rightarrow \partial V_{DSn}$



channel resistance $= \frac{\partial V_{DSn}}{\partial I_{DSn}} = \frac{1}{\frac{\partial I_{DSn}}{\partial V_{DSn}}} \simeq \frac{1}{0} = \infty$ [saturation region]

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channel resistance, $\frac{\partial V_{DSn}}{\partial I_{Dn}} = r_{ON} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSn} - V_{th})}$ = finite.

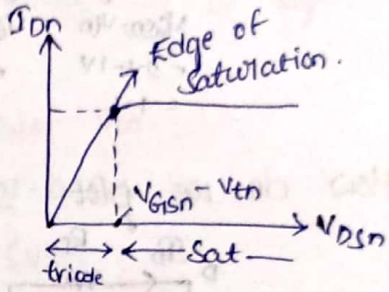
⇒ NMOS offers high resistance in saturation region.
(current source has infinite resistance)

⇒ In saturation, there is no dependendence of I_D on V_{DS} but in practical I_{Dn} will depend on V_{DS}.

* What is edge of Saturation

If a NMOS is in edge of saturation then

$$V_{DSn} = V_{GSn} - V_{th}$$



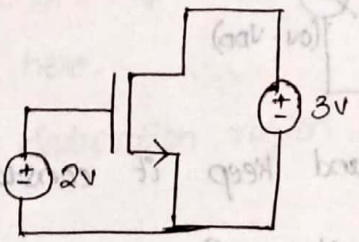
* Eg:- Given $V_{th} = 1V$

$\mu_n C_{ox} = 1 mA/V^2$

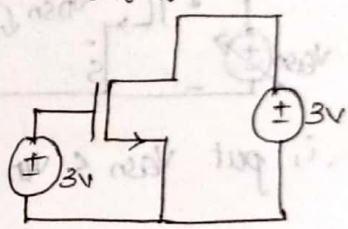
$\left(\frac{W}{L}\right)_n = 2$

$I_{Dn} = ?$

Ckt-1

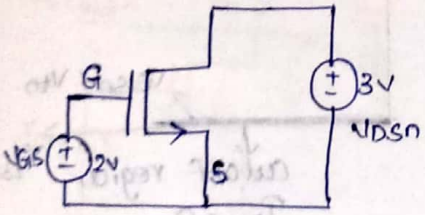


Ckt-2



Ckt-1

1. Mark the terminals



2. Region of operation

$V_{GSn} = 2$, $V_{th} = 1$

⇒ $V_{GSn} > V_{th}$

$V_{GSn} - V_{th} = 2 - 1 = 1V$ (V_{ov})

$V_{DSn} = 3V$

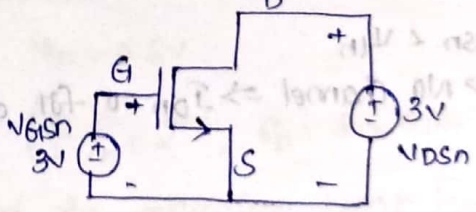
$V_{DSn} > V_{GSn} - V_{th}$

⇒ Saturation region.

$I_{Dn} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{ov}]^2$

Ckt-2

1. Mark the terminals.



2. Region of operation

$V_{GSn} = 3$, $V_{th} = 1V$

⇒ $V_{GSn} > V_{th}$

$V_{GSn} - V_{th} = 3 - 1 = 2V$ (V_{ov})

$V_{DSn} = 3V$

$V_{DSn} > V_{GSn} - V_{th}$

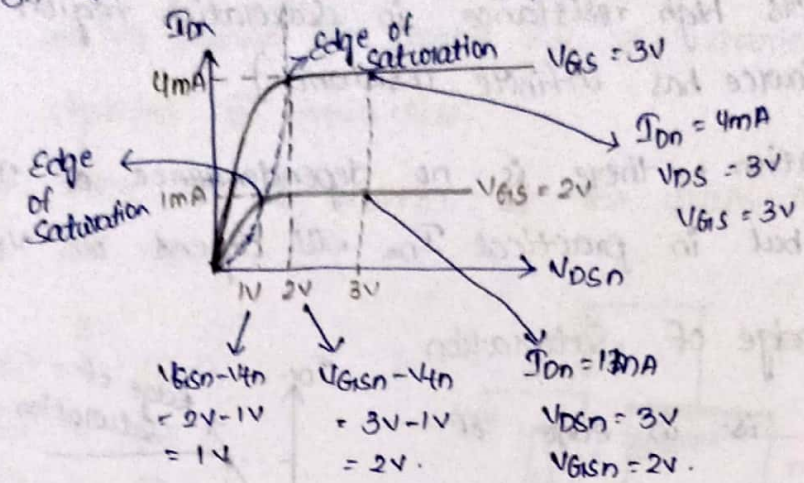
⇒ Saturation region.

$I_{Dn} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{ov}]^2$

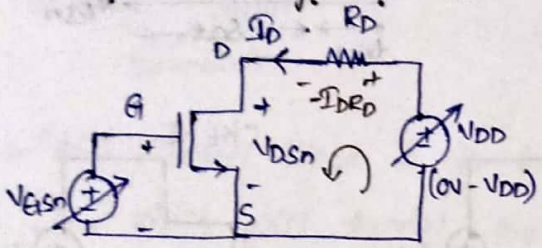
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$= \frac{1}{2} \times 1m \times 2 \times 1^2$ $= \frac{1}{2} \times 1m \times 2 \times 2^2$

$I_{Dn} = 1\,mA$ @ $V_{GSn} = 2V$ $I_{Dn} = 4mA$ @ $V_{GSn} = 3V$



* How do we plot I_{Dn} Vs V_{DSn} ie, output char. of MOSFET.



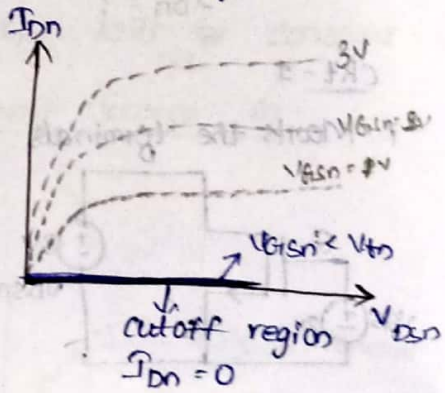
$V_{tn} = 1V$

i, put $V_{GSn} < V_{tn}$ and keep it constant. then vary V_{DD};

$$-V_{DD} + I_DR_D + V_{DSn} = 0$$

$$I_D = -\frac{1}{R_D} V_{DSn} + \frac{V_{DD}}{R_D}$$

[$V_{GSn} < V_{tn}$
⇒ No channel ⇒ $I_{Dn} = 0$ for all V_{DD}]



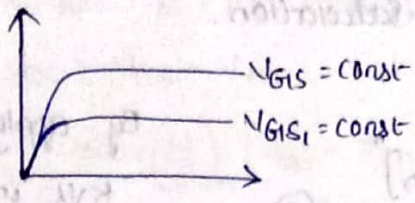
ii, put $V_{GSn} = 2V$ and keep it constant and then vary V_{DD}.

$$I_D = -\frac{1}{R_D} V_{DSn} + \frac{V_{DD}}{R_D}$$

put $V_{GSn} = 3V$ and keep it constant and then vary V_{DD}: note corresponding I_{Dn} & V_{DSn} values.

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Problem :-



Which is true?

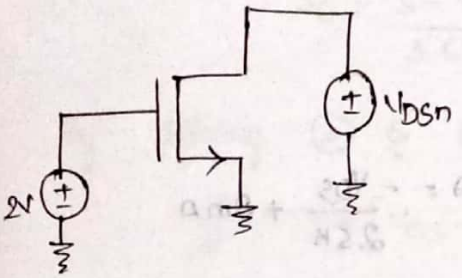
i) $V_{GS_1} > V_{GS2}$

ii) $V_{GS_1} < V_{GS2}$

$V_{GS_1} < V_{GS2}$ $\left[\because I_D \propto V_{ov}^2\right]$; $V_{ov} = V_{GSn} - V_{tn}$

In saturation if V_{GS} is more then I_D is also more.

Problem :- Given NMOS is at edge of saturation. $V_{tn} = 0.5V$, What is value of V_{DSn}?



Given that NMOS is at edge of operation.

$\Rightarrow V_{DSn} = V_{GSn} - V_{tn}$

$= 2V - 0.5V$

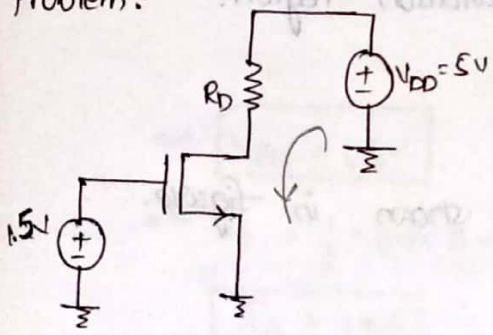
$V_{DSn} = 1.5V$.

Is $I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n [V_{ov}]^2$

Yes, it is valid here.

$\because$ NMOS is in saturation region.

Problem :-



Given:

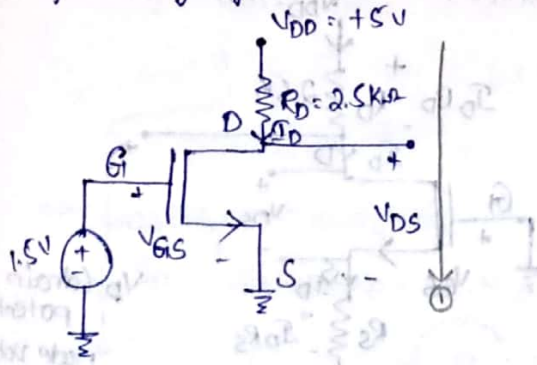
$\mu_n C_{ox} = 1 mA/V^2$

$V_{tn} = 0.5V$

$\left(\frac{W}{L}\right)_n = 2$, $R_D = 2.5 K\Omega$

Find the operating point $[V_{DS}, I_D]$ and gate current

Operating point means the value of V_{DS} & I_D ; $I_G = 0$



Apply KVL at outerloop

$-5 - V_{DD} + I_D R_D + V_{DS} = 0$

$\left[-5 + I_D(2.5 K\Omega) + V_{DS} = 0\right]$

$I_D = -\frac{1}{R_D} V_{DS} + \frac{V_{DD}}{R_D}$ → ①

I_D, V_{DS} → two variables.

$\Rightarrow$ We don't know the region of operation.

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Assume NMOS MOS in Saturation.

$\Rightarrow V_{DS} \geq V_{GS} - V_{th}$

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS} - V_{th}]^2 \rightarrow (2)$$

$$I_D = \frac{1}{2} \times 1m \times 2 [1.5 - 0.5]^2$$

$$\boxed{I_D = 1mA}$$

By applying KVL in loop ①

$-1.5V + V_{GS} = 0$

$V_{GS} = 1.5V$

Substitute $I_D = 1mA$ in Eq ①

$$I_D = -\frac{1}{R_D} V_{DS} + \frac{V_{DD}}{R_D}$$

$$1mA = -\frac{1}{2.5K} V_{DS} + \frac{5}{2.5K} \Rightarrow 1mA = -\frac{V_{DS}}{2.5K} + 2mA$$

$$\frac{V_{DS}}{2.5K} = 2mA - 1mA \Rightarrow V_{DS} = 1mA(2.5K\Omega)$$

$$\boxed{V_{DS} = 2.5V}$$

⇒ Now justify our assumption:

In Saturation, $V_{DS} > V_{GS} - V_{th}$

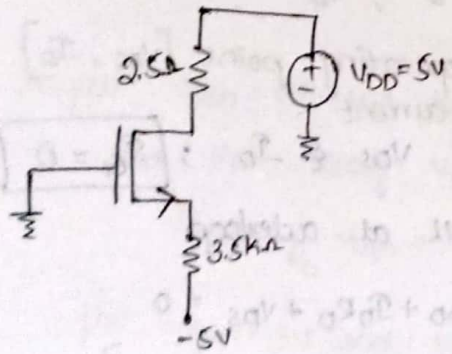
$2.5 > 1.5 - 0.5$

Indeed MOSFET is in Saturation region.

∴ Operating point (2.5V, 1mA)

Problem :-

Find V_D & I_D for the NMOS circuit shown in figure.



$V_{th} = 0.5V$

$\left(\frac{W}{L}\right)_n = 2$

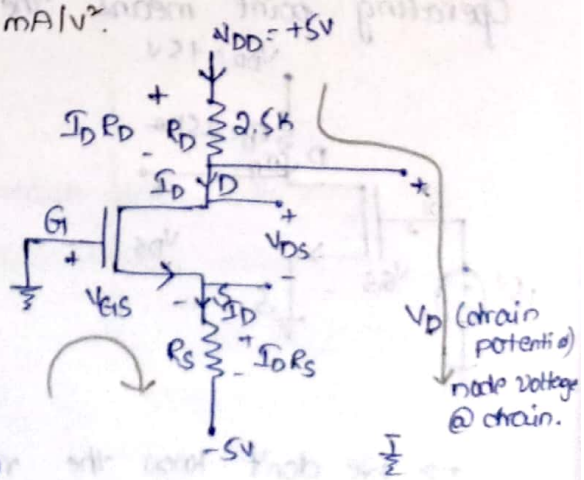
$\mu_n C_{ox} = 1mA/V^2$

Sol: Which transistor: NMOS

Apply KVL at outer loop,

$V_{DD} = I_D R_S + V_D$

$$I_D = -\frac{1}{R_D} V_D + \frac{V_{DD}}{R_D} \rightarrow (1)$$



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Assume NMOS is in saturation.

$$V_{DS} \geq V_{GS} - V_{tn}$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[V_{GS} - V_{tn}\right]^2$$

① : variables I_D, V_D

$$I_D = \frac{1}{2} \times 1m \times 2 \left[V_{GS} - 0.5V\right] \longrightarrow ②$$

② : variables, I_D, V_{GS}

Apply KVL in input loop.

$$V_{GS} + I_D R_S - 5V = 0$$

$$I_D = \frac{5 - V_{GS}}{3.5K\Omega} \longrightarrow ③$$

③ variables I_D, V_{GS}

By solving ② & ③

$$\frac{1}{2} \times 1m \times 2 \left[V_{GS} - 0.5V\right]^2 = \frac{5 - V_{GS}}{3.5K}$$

$$5 - V_{GS} = 3.5 \left[V_{GS} - 0.5V\right]^2$$

$$5 - V_{GS} = \frac{7}{2} \left[V_{GS}^2 + 0.25 - V_{GS}\right]$$

$$7V_{GS}^2 - 7V_{GS} + \frac{7}{4} = 10 - 2V_{GS}$$

$$7V_{GS}^2 - 5V_{GS} - 10 + \frac{7}{4} = 0$$

$$7V_{GS}^2 - 5V_{GS} - \frac{33}{4} = 0$$

$$V_{GS} = 1.5V, \; -0.785V$$

this value not possi

$-0.785V < V_{tn}$

$$\Rightarrow \boxed{V_{GS} = 1.5V}$$

$$\Rightarrow I_D = \frac{1}{2} \times 1m \times 2 \times \left[1.5 - 0.5\right]^2$$

$$\boxed{I_D = 1mA}$$

$$V_D = V_{DD} - I_D R_D = 5V - 1m \times 2.5K$$

$$= 5V - 2.5V$$

$$\boxed{V_D = 2.5V}$$

⇒ Justify assumption

In saturation : $V_{DS} \geq V_{GS} - V_{tn}$

$$V_D - V_S \geq V_G - V_S - V_{tn}$$

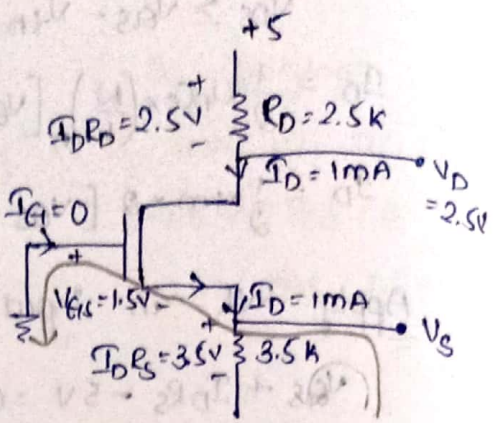
$$2.5 \geq 0 - 0.5$$

$$2.5 > -0.5$$

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∴ MOSFET is in saturation.

$V_D = 2.5V$, $I_D = 1mA$



Problem:-

Find V_S.

$-V_S + (-V_{GS}) = 0$

$V_S = -V_{GS}$

$\boxed{V_S = -1.5V}$

(or)

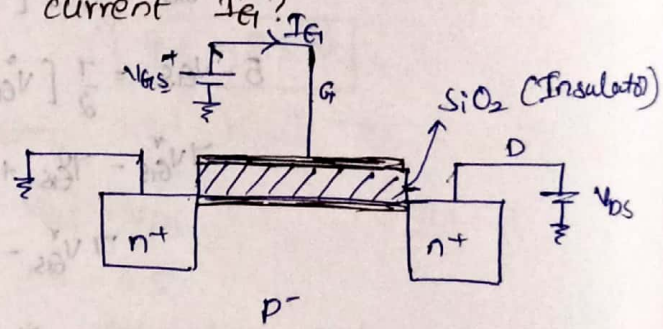
$V_S = I_D R_S - 5V$

$V_S = 3.5V - 5V$

$\boxed{V_S = -1.5V}$

23/12/21

* How much is the gate current I_G?



⇒ Because of the presence of SiO_2 (insulator); gate current will be of order of 10^{-15}

⇒ $I_G = 0$.

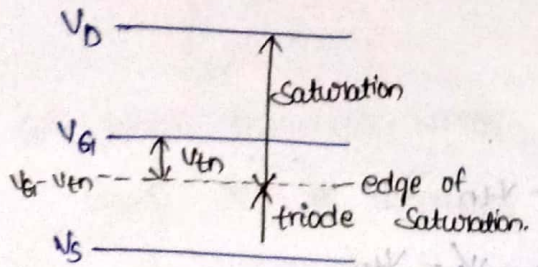
Condition for Saturation

NMOS

$V_{DSn} \geq V_{GSn} - V_{tn}$

$V_D - V_S \geq V_G - V_S - V_{tn}$

$V_D \geq V_G - V_{tn}$



PMOS

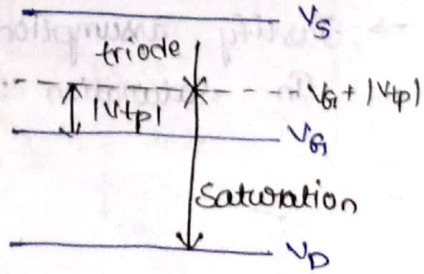
Condition for Sat based on V_D & V_G & MOS is ON

$V_{SDp} \geq V_{SGp} - |V_{tp}|$

$V_S - V_D \geq V_S - V_G - |V_{tp}|$

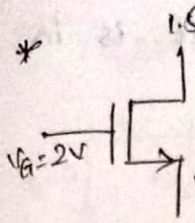
$-V_D \geq -V_G - |V_{tp}|$ x(-)

$V_D \leq V_G + |V_{tp}|$



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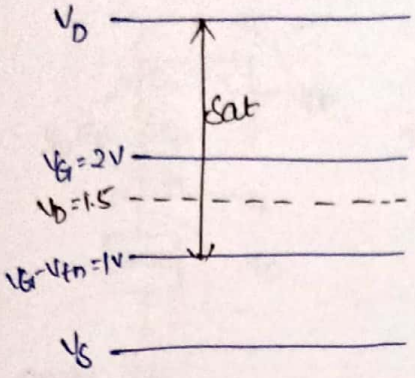
*



Assume $V_{GS} > V_{tn}$

$V_{tn} = 1V$

region of operation = ?



⇒ saturation region.

$V_{tn} = 0.5$

$V_D = 3V \longrightarrow$ sat

$V_D = 2V \longrightarrow$ sat

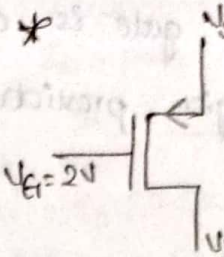
$= 1.5V \longrightarrow$ sat

$= 1V \longrightarrow$ edge of sat

$= 0.95 \longrightarrow$ triode region.

$= 0.95 \longrightarrow$ triode region.

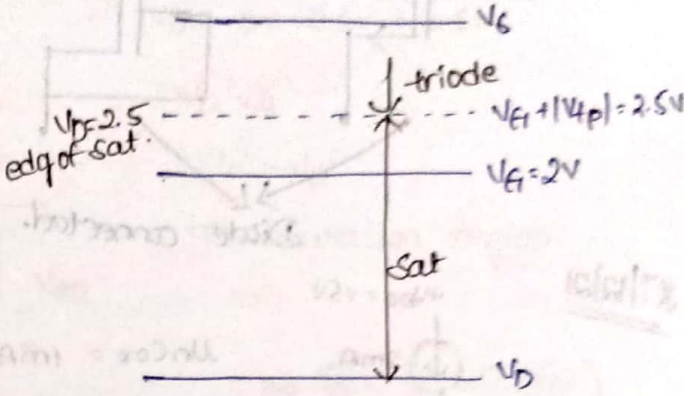
*



$V_{tp} = -0.5V$

Assume $V_{SGp} > |V_{tp}|$

⇒ PMOS : ON.



$V_D = 3V \longrightarrow$ triode

$= 2.6V \longrightarrow$ triode

$= 2.5V \longrightarrow$ Sat (Edge)

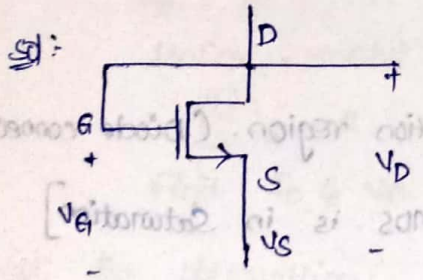
$= 2V \longrightarrow$ Sat

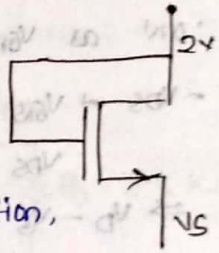
$= 1V \longrightarrow$ Sat

* Region of operation ?

Given $V_{GSn} > V_{tn}$; $V_{tn} = 1V$

Sol:





By observation,

$V_G = V_D = 2V$

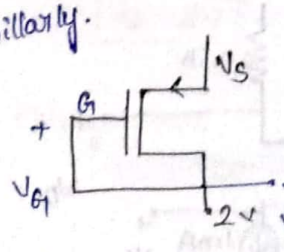
$2V > 2 - 1$

$2 > 1$ ⇒ Saturation.

⇒ If a gate terminal is shorted to drain terminal then NMOS is in <u>saturation region</u> provided <u>$V_{GSn} > V_{tn}$</u>

i.e, <u>NMOS : ON.</u>

Similarly.



Given $V_{tp} = -1V$;

$V_{GSp} > |V_{tp}|$

⇒ PMOS : ON

Region of operation?

By observation

$V_G = V_D = 2V$

$V_D < V_G + |V_{tp}|$

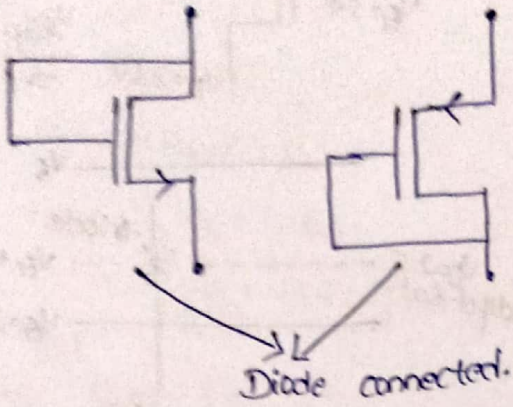
$2 < 2 + 1$

$2 < 3V$ ⇒ Saturation region.

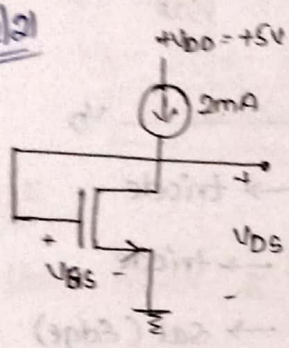
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⇒ In PMOS; if gate is connected to drain then it is in Saturation region provided $V_{GSp} > |V_{tp}|$

*



27/12/21



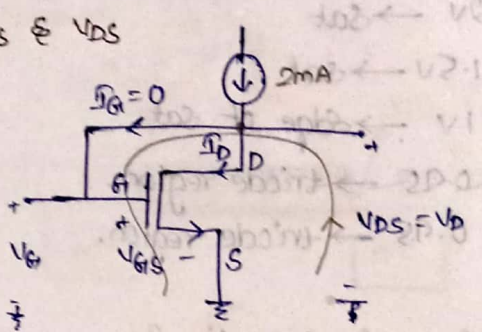
$\mu_n C_{ox} = 1mA/V^2$

$V_{tn} = 0.5V$

$\left(\frac{W}{L}\right)_n = 2$

Find V_{GS} & V_{DS}

By Observation: NMOS.



From KCL

$2mA = I_G + I_D$

$I_D = 2mA$

⇒ NMOS : ON as $V_{GS} > V_{tn}$

Apply KVL $\quad -V_{DS} + V_{GS} = 0$

$V_{DS} = V_{GS}$

$\Rightarrow V_D - V_S = V_G - V_S$

$V_D = V_G$ ⇒ Saturation region. (Diode connected)

$\therefore I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS} - V_{tn}]^2$ [∵ MOS is in Saturation]

$V_{GS} = V_{tn} + \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n}} = 0.5V + \sqrt{\frac{2\times 2m}{1m\times 2}}$

$V_{GS} = 0.5V + \sqrt{2} = 1.914V.$

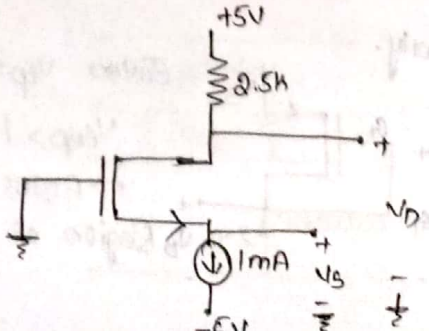
⇒ $\boxed{V_{DS} = V_{GS} = 1.914V}$

Problem 2: $\mu_n C_{ox} = 1mA/V^2$

$V_{tn} = 1V$

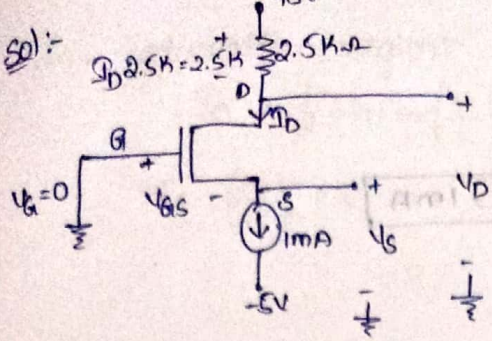
$\left(\frac{W}{L}\right)_n = 2$

Find V_D & V_S



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Sol:-



By Observation:

$I_D = 1mA$

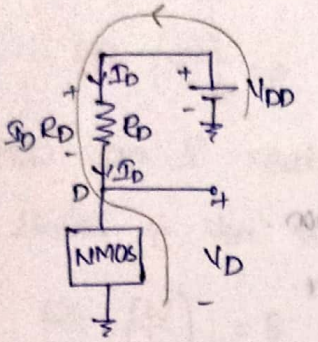
$V_G = 0$

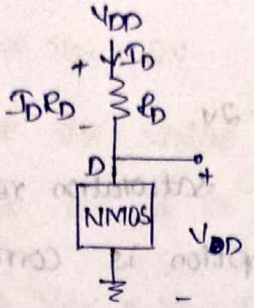
Apply KVL:

$5V = I_D (2.5K\Omega) + V_D$

$5V = 1m \times 2.5K + V_D$

$V_D = 5V - 2.5V = 2.5V$





$V_G = 0$

$V_D > V_G$

$\Rightarrow$ Saturation region.

Apply KVL:

$-V_{DD} + I_D R_D + V_D = 0$

$V_D = V_{DD} - I_D R_D$

Apply KVL:

$V_{DD} = I_D R_D + V_D$

$\Rightarrow I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n [V_{GS} - V_{th}]^2$

$\Rightarrow V_{GS} = V_{th} + \sqrt{\frac{2 I_D}{\mu_n C_{ox} \left(\frac{W}{L}\right)_n}}$

$= 1V + \sqrt{\frac{2 \times 1m}{1m \times 2}}$

$V_{GS} = 2V$

Apply KVL in inner loop:

$-V_S - V_{GS} = 0$

$\Rightarrow \boxed{V_S = -V_{GS} = -2V}$

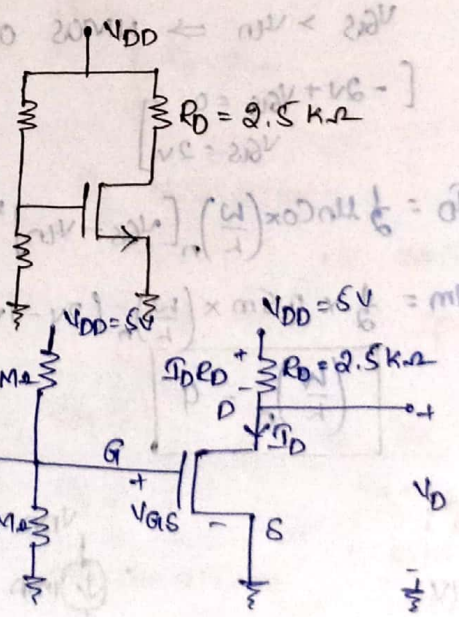
Problem 3:

$V_{th} = 1V$

$\mu_n C_{ox} = 1mA/V^2$

$\left(\frac{W}{L}\right)_n = 2$

Find I_D & V_D



Sol: By observation:

$V_G = \frac{2M\Omega}{2M\Omega + 3M\Omega} \times 5V$

$= \frac{2M}{5M} \times 5V$

$\Rightarrow \boxed{V_G = 2V}$

Apply KVL

$-V_G + V_{GS} = 0$

$\boxed{V_{GS} = V_G = 2V}$

Apply KVL

$V_{DD} = I_D R_D + V_D$

$V_D = V_{DD} - I_D R_D$

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Assume NMOS is in saturation

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS} - V_{th}]^2$$

$$= \frac{1}{2} \times 1m \times 2 \times [2-1]^2 \Rightarrow \boxed{I_D = 1mA}$$

$$\Rightarrow V_D = V_{DD} - I_D R_D$$

$$= 5 - 1m \times 2.5K \Rightarrow \boxed{V_D = 2.5V}$$

Justify our assumption:

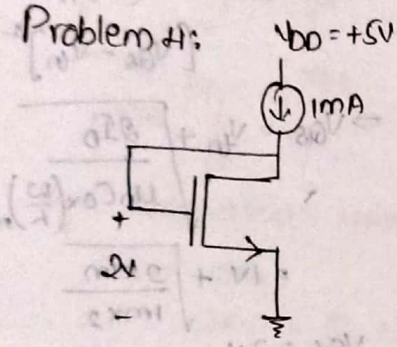
$V_D = 2.5V$; $V_G = 2V$

$V_D > V_G \Rightarrow$ saturation region.

$\therefore$ Our assumption is correct.

$I_D = 1mA$; $V_D = 2.5V$

Problem 4:

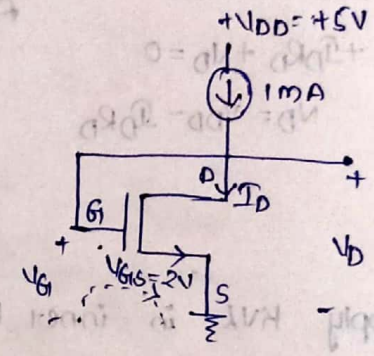


Given

$V_{th} = 1V$,

$\mu_n C_{ox} = 0.5 mA/V^2$

$\left(\frac{W}{L}\right)_n = ?$



$\therefore 1mA = I_G + I_D$

$I_D = 1mA$

By observation: $I_D = 1mA$

i, $V_{GS} = 2V$; $V_{th} = 1V$.

$V_{GS} > V_{th} \Rightarrow$ NMOS ON.

$[-2V + V_{GS} = 0$

$V_{GS} = 2V]$

ii, $V_G = V_D$

$\Rightarrow$ Saturation region

(Diode connected)

$\therefore I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS} - V_{th}]^2$

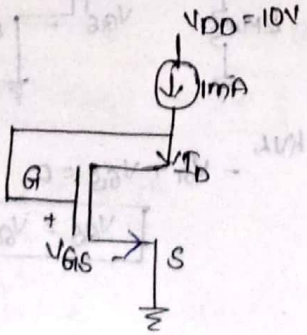
$1m = \frac{1}{2} \times 0.5m \times \left(\frac{W}{L}\right)_n [2V - 1V]^2$

$\boxed{\left(\frac{W}{L}\right)_n = 4}$

Problem 5:

$V_{th} = 1V$

$\mu_n C_{ox} = 1mA/V^2$



By observation:

$I_D = 1mA$; MOSFET : ON

$\Rightarrow V_G = V_D$

$\Rightarrow$ Saturation region

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In Saturation region:

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS} - V_{tn}]^2$$

If $\left(\frac{W}{L}\right)_n = 2 \Rightarrow V_{GS} = V_{tn} + \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n}}$

$= 1V + \sqrt{\frac{2 \times 1m}{1m \times 2}} = 2V$

For $\left(\frac{W}{L}\right)_n = 2 \Rightarrow V_{GS} = 2V$

How can I realize the value of V_{GS} by keeping $I_D = 1mA$?

$\mu_n C_{ox}$ & V_{tn} value is not in hands of designer (Technology parameters)

For $\left(\frac{W}{L}\right)_n = 8 \Rightarrow V_{GS} = V_{tn} + \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n}}$

$= 1V + \sqrt{\frac{2 \times 1m}{1m \times 8}} = 1V + 0.5V = 1.5V$

For $\left(\frac{W}{L}\right)_n = 8 \Rightarrow V_{GS} = 1.5V$

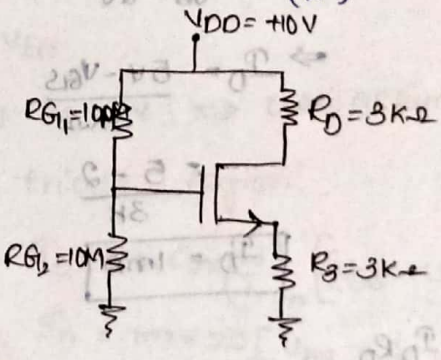
* $\Rightarrow$ For having I_D = constant, If $\left(\frac{W}{L}\right)$ ↑es $\Rightarrow V_{GS}$ ↓es

Problem 6:

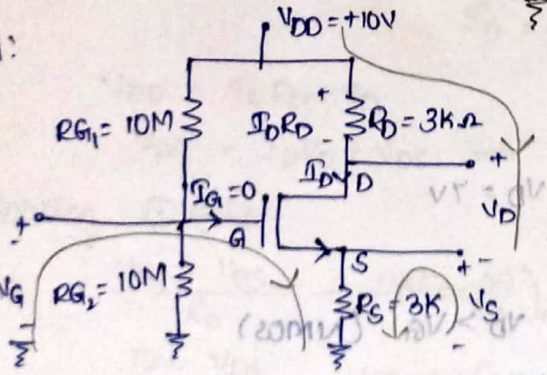
$V_{tn} = 1V$

$\mu_n C_{ox} = 1mA/V^2$

$\left(\frac{W}{L}\right)_n = 2$

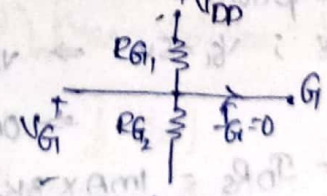


Sol:



By observation:

$V_G = 5V$; we don't know V_{GS} & region of operation.



resister divider

$V_G = \frac{R_{G2}}{R_{G1} + R_{G2}} \times V_{DD}$

$= \frac{10M}{10M + 10M} \times 10$

$V_G = 5V$

Apply KVL:

$-V_G + V_{GS} + I_D R_S = 0$

$I_D = \frac{V_G - V_{GS}}{R_D}$

$\boxed{I_D = \frac{5V - V_{GS}}{3K\Omega}} \rightarrow (1)$

Apply KVL in outer

$V_{DD} = I_D R_D + V_D$

$V_D = V_{DD} - I_D R_D$

another KVL

$-V_S + I_D R_S = 0 \Rightarrow \boxed{V_S = I_D R_S}$

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In order to find I_D, we need to know the region of operation.

∴ Assume MOSFET is in saturation region.

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS} - V_{tn}]^2 \longrightarrow (2)$$

Solve (1) & (2)

$$\frac{5V - V_{GS}}{3K\Omega} = \frac{1}{2} \times 1m \times 2 [V_{GS} - 1V]^2$$

$$5V - V_{GS} = 3[V_{GS} - 1]^2$$

$$5V - V_{GS} = 3V_{GS}^2 - 6V_{GS} + 3$$

$$3V_{GS}^2 - 6V_{GS} + V_{GS} - 2 = 0$$

$$3V_{GS}[V_{GS} - 2] + 1[V_{GS} - 2] = 0$$

$$[V_{GS} - 2][3V_{GS} + 1] = 0$$

$V_{GS} = 2$ $\quad 3V_{GS} = -1$

$V_{GS} = 2V$ $\quad \Rightarrow V_{GS} = -\frac{1}{3}V$ (Not possible)

$$\Rightarrow I_D = \frac{5V - V_{GS}}{3K\Omega}$$

$$= \frac{5 - 2}{3K}$$

$$\boxed{I_D = 1mA}$$

$$\Rightarrow V_D = V_{DD} - I_D R_D$$

$$= 10 - 1m \times 3K\Omega$$

$$= 10 - 3V \Rightarrow 7 \Rightarrow V_D = 7V$$

Justify our assumption:

$V_D = 7V$; $V_G = 5V \Rightarrow V_D > V_G$ (NMOS)

$\Rightarrow$ our assumption is correct.

$$V_S = I_D R_S = 1mA \times 3K\Omega = 3V$$

Check: $V_{GS} = 2V$

$V_G - V_S = 2V$

$5V - 3V = 2V$

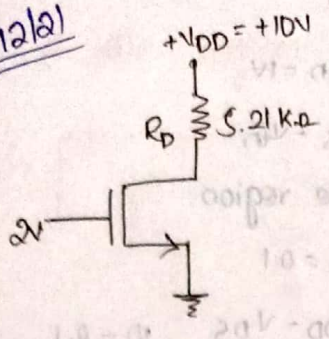
$2V = 2V$

$V_D = V_D - V_S = 7V - 3V = 4V$

$V_{GS} = 2V$
$I_D = 1mA$
$V_D = 7V$
$V_S = 3V$
$V_{DS} = 4V$

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28/12/21



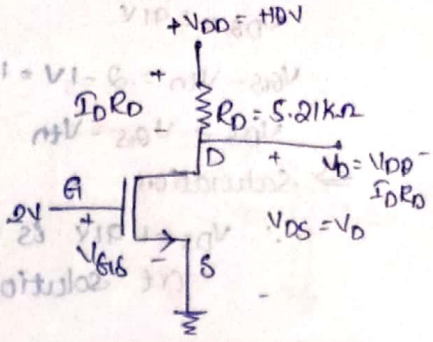
Given

$\mu_n C_{ox} = 1 mA/V^2$

$V_{tn} = 1V$

$\left(\frac{W}{L}\right)_n = 20$

Find I_D



Sol: By observation:

$V_G = V_{GS} = 2V$

$V_D = V_{DS}$

Assume NMOS is in saturation region.

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS} - V_{tn}]^2$$

$$= \frac{1}{2} \times 1m \times 20 [2V - 1V]^2$$

$I_D = 10mA$

$\Rightarrow V_D = V_{DD} - I_D R_D = 10 - 10mA(5.21K)$

$\Rightarrow V_D = -42.1V$

Justify our assumption,

$V_D < V_G - V_{tn}$

$-42.1V < 2V - 1V = 1V \Rightarrow$ our assumption is wrong.

$\Rightarrow$ MOSFET is in triode region!

∴ In triode region: $I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)_n \left[(V_{GS} - V_{tn})V_{DS} - \frac{1}{2}V_{DS}^2\right] \rightarrow ①$

$$I_D = 1m \times 20\left[V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$V_{DD} = I_D R_D + V_D$

$V_{DD} = I_D R_D + V_{DS} \Rightarrow I_D = \frac{V_{DD} - V_{DS}}{R_D} \rightarrow ②$

Solving ① & ②

$$\frac{V_{DD} - V_{DS}}{R_D} = \mu_n C_{ox}\left(\frac{W}{L}\right)_n \left[(V_{GS} - V_{tn})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$\frac{10V - V_{DS}}{5.21K} = 1m \times 20\left[V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$10V - V_{DS} = 5.21 \times 10\left[\frac{2V_{DS} - V_{DS}^2}{2}\right]$$

$$10V - V_{DS} = 52.1\left[2V_{DS} - V_{DS}^2\right]$$

$$52.1V_{DS}^2 - 104.2V_{DS} - V_{DS} + 10V = 0$$

$$52.1V_{DS}^2 - 105.2V_{DS} + 10V = 0$$

$V_{DS} = 1.91V$ & $0.1V$

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$V_{DS} = 1.91V$

$V_{GS} - V_{th} = 2 - 1V = 1V$

$V_{DS} > V_{GS} - V_{th}$

$\Rightarrow$ Saturation

$\therefore V_{DS} = 1.91V$ is not crt solution

$V_{DS} = 0.1V$

$V_{GS} - V_{th} = 1V$

$V_{DS} < V_{GS} - V_{th}$

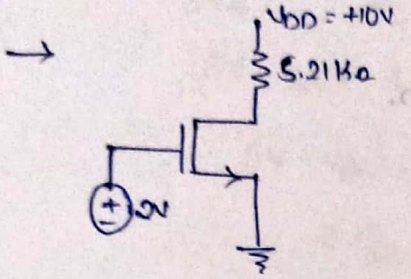
$\Rightarrow$ triode region

$\therefore V_{DS} = 0.1$

$\Rightarrow I_D = \frac{V_{DD} - V_{DS}}{R_D} = \frac{10 - 0.1}{5.21K}$

$\Rightarrow \boxed{I_D = 1.90\,mA}$

$\boxed{I_D = 1.90mA \text{ & } V_{DS} = 0.1V}$



$V_{DS} << 2[V_{GS} - V_{th}]$

$0.1 << 2[2 - 1V]$

$0.1 << 2V$

$\Rightarrow$ Deep triode region

$\Rightarrow$ MOSFET is acts as resistor.

$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[[V_{GS} - V_{th}] V_{DS} - \frac{1}{2} V_{DS}^2\right]$

$R_{eq} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_n [V_{GS} - V_{th}]}$ Since $V_{DS} << 2[V_{GS} - V_{th}]$

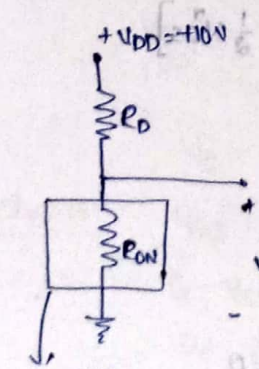
$\Rightarrow I_D = \mu_n C_{ox} \left(\frac{W}{L}\right)_n [V_{GS} - V_{th}] V_{DS}$; $\frac{1}{2} V_{DS}^2$ is neglected.

$\Rightarrow R_{ON} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_n [V_{GS} - V_{th}]}$

$\Rightarrow R_{ON} = \frac{1}{1m \times 20 \times [2V - 1V]}$

$R_{ON} = \frac{1}{1m \times 20} = 50\Omega$

$\boxed{R_{ON} = 50\Omega}$



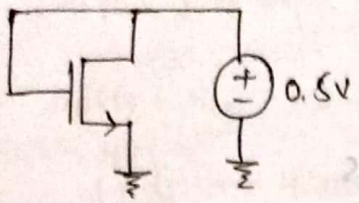
$V_{DS} = \frac{R_{ON}}{R_{ON} + R_D} \times V_{DD} = \frac{50\Omega}{50\Omega + 5.21K} \times 10$

$\boxed{V_{DS} = 0.1V}$

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Find the region of operation

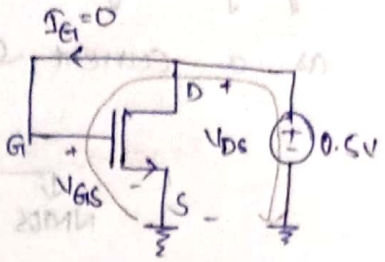
i)



$V_{tn} = 1V$

$\mu_n C_{ox} = 1 mA/V^2$

$\left(\frac{W}{L}\right)_n = 2$



Applying KVL

$-V_{GS} + 0.5V = 0$

$V_{GS} = V_{GS} 0.5$

By observation

gate & drain are shorted

$V_G = V_D$

$\Rightarrow$ Not in Saturation since $V_{GS} < V_{tn}$

$\Rightarrow$ cut-off region. MOSFET OFF.

$\Rightarrow I_D = 0$

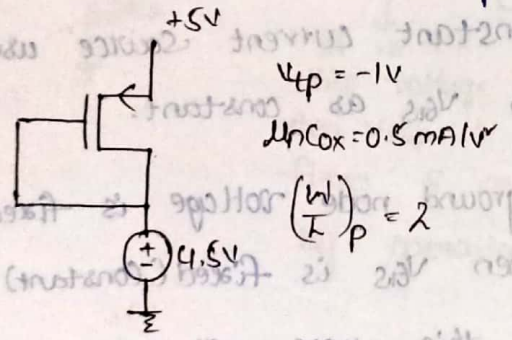
* In 'diode connected' if $V_{GS} \geq V_{tn} \Rightarrow$ Saturation

MOSFET : ON.

if $V_{GS} < V_{tn} \Rightarrow$ cut off region.

* Triode region is not possible in diode connection.

ii)



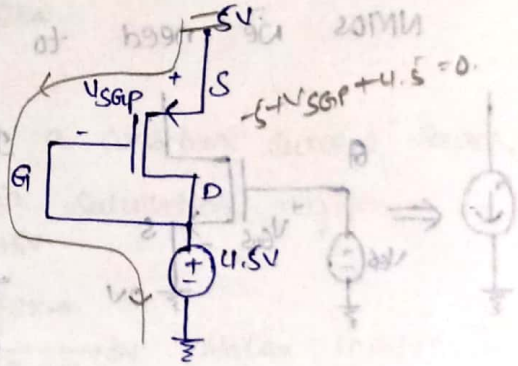
By observation,

gate & drain are shorted

$\Rightarrow V_G = V_D$ [PMOS]

$\Rightarrow$ Saturation

Not correct ✗



Apply KVL,

$+5V = +V_{SGp} + 4.5V$

$V_{SGp} = 5 - 4.5$

$V_{SGp} = 0.5V$

$V_{SGp} < |V_{tp}|$

$\Rightarrow$ PMOS OFF

$\Rightarrow$ Cut off region.

* Note:

In diode connected, using PMOS if

$V_{SGp} \geq |V_{tp}| \Rightarrow$ Saturation (CMOS = ON)

$V_{SGp} < |V_{tp}| \Rightarrow$ cut-off (CMOS = OFF)

triode region is not possible.

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* By operating MOSFET in Saturation region, it will acts as a current source.

MOSFET
↓ NMOS
↓ PMOS

* Using NMOS as a current source this can be done by operating NMOS in saturation region.

In saturation:

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS} - V_{tn}]^2$$

* $\mu_n C_{ox}$ & V_t are technology parameters.

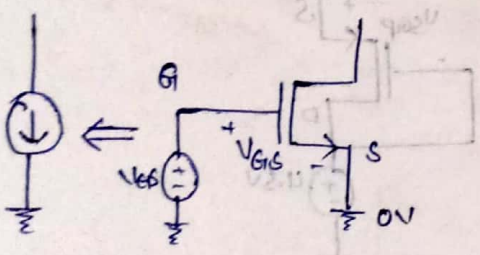
It means they are not in the hands of designer.

* $\left(\frac{W}{L}\right)_n$ & V_{GS} are in the hands of designer.

$\mu_n C_{ox}$, V_t → fixed (constant)

$\left(\frac{W}{L}\right)_n$ → fixed (constant)

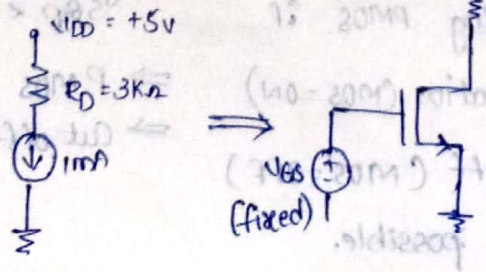
⇒ In order to realize a constant current source using NMOS we need to keep V_{GS} as constant.



If ground node voltage is fixed (constant) then V_{GS} is fixed (constant) then this NMOS will acts as a constant current source.

Note:- Suppose we want to realize a current source which is nearer to least power supply or ground then this can be done using NMOS by connecting its source to least power supply or ground.

It means:



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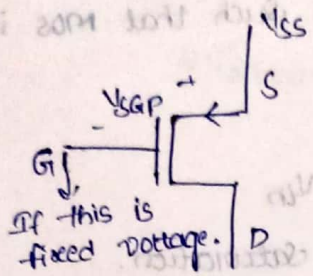
Similarly for PMOS

$$I_{Dp} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p \left[V_{SGp} - |V_{tp}|\right]^2$$

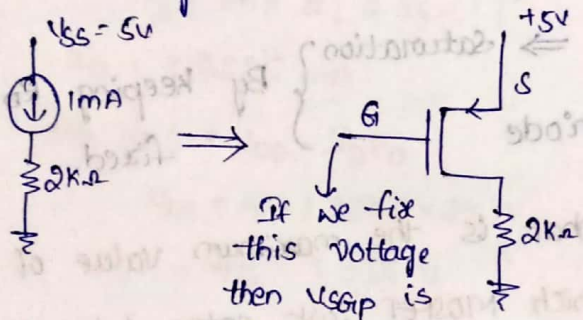
$\mu_p C_{ox}$, V_{tp} → technology parameters (Constant)

$\left(\frac{W}{L}\right)_p$ → fixed by designer.

for having constant current source, we have to fix V_{SGp}.

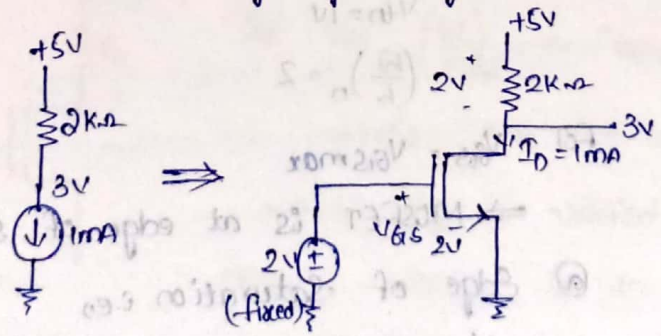


Typically current source which are nearer to highest power supply are realized using PMOS(by operating in Saturation region).



by operating in Saturation region.

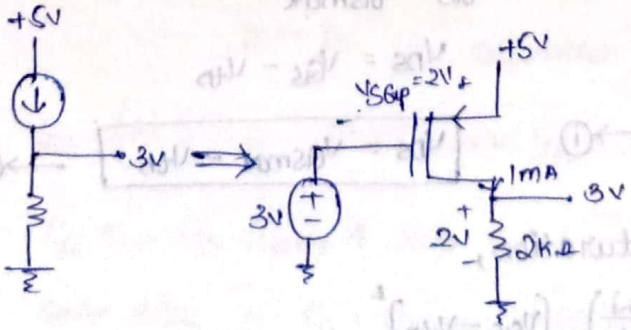
Eg:-



$\mu_n C_{ox} = 1\text{mA/V}^2$

$\left(\frac{W}{L}\right)_n = 2$

$V_{tn} = 1V$



$\mu_p C_{ox} = 0.5\text{mA/V}^2$

$\left(\frac{W}{L}\right)_p = 4$

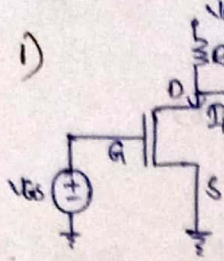
$V_{tp} = -1V$

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Observations:-

1)



$\left(\frac{W}{L}\right)_n$ → fixed (constant)

$\mu_n C_{ox}$, V_{th} → technology parameters (fixed)

Further more assume MOSFET in Saturation [i.e., we have taken R_D such that MOS is in Sat]

* If V_{GS} ↑,

$\Rightarrow I_D$ ↑

$\Rightarrow I_D R_D$ ↑ $\Rightarrow V_D$ ↓

⇒ For some value of $V_{GS\,max}$, $V_{DS} = V_{GS} - V_{th}$

i.e., Edge of saturation.

⇒ For $V_{GS} > V_{GS\,max}$, $V_{DS} < V_{GS} - V_{th}$

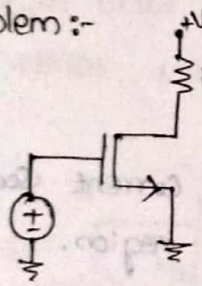
⇒ MOSFET will enter into triode region.

⇒ $V_{th} \le V_{GS} \le V_{GS\,max}$ ⇒ Saturation

$V_{GS} > V_{GS\,max}$ ⇒ triode

} By keeping R_D, $\left(\frac{W}{L}\right)_n$ fixed.

Problem:-



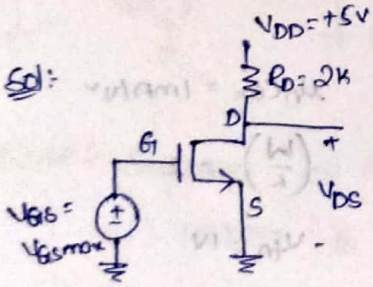
What is the maximum value of V_{GS} for which MOSFET just enter into triode region.

Given $\mu_n C_{ox} = 1mA/V^2$

$V_{th} = 1V$

$\left(\frac{W}{L}\right)_n = 2$

Sol:-



For $V_{GS} = V_{GS\,max}$

⇒ MOSFET is at edge of saturation.

@ Edge of Saturation i.e.,

$V_{GS} = V_{GS\,max}$

$V_{DS} = V_{DD} - I_D R_D$

$\boxed{V_{DS} = 5 - I_D\,2K\Omega}$ → (1)

$V_{DS} = V_{GS} - V_{th}$

$\boxed{V_{DS} = V_{GS\,max} - V_{th}}$ → (2)

at Edge of Saturation,

$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n \left[V_{GS} - V_{th}\right]^2$

$I_D = \frac{1}{2} \times 1m \times 2 \left[V_{GS} - 1\right]^2$

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$\Rightarrow V_{DS} = 5V - 1m\,[V_{GSmax} - 1]^2 2k\Omega$

$V_{DS} = 5V - 2[V_{GSmax} - 1]^2 \longrightarrow (3)$

Eq (2) & (3) are having 2 unknowns. (V_{DS}, V_{GSmax})

solve (2) & (3)

$V_{GSmax} - 1 = 5V - 2[V_{GSmax} - 1]^2$

$V_{GSmax} - 1 = 5V - 2V^2_{GSmax} + 4V_{GSmax} + 2$

$2V^2_{GSmax} - 3V_{GSmax} - 4 = 0$

$V_{GSmax} = 2.35$ & -0.85 (not possible).

$\therefore V_{GSmax} = 2.35V$

$\Rightarrow$ If $V_{GS} > V_{tn}$ Saturation,

$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n [V_{GS} - V_{tn}]^2$

$= \frac{1}{2} \times 1m \times 8 [2.35 - 1]^2$

$I_D = 1.8225\ mA$

$\Rightarrow V_{DS} = V_{DD} - I_D R_D$

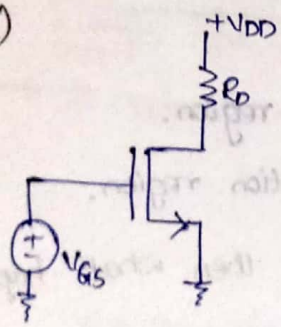
$V_{DS} = 5 - 1.8225 \times 2k\Omega$

$V_{DS} = 1.355\ V$

$V_{GSmax} - V_{tn} = 1.35V$

$\Rightarrow V_{DS} = V_{GSmax} - V_{tn} \Rightarrow$ Edge of Saturation.

2)



If V_{GS}, $\left(\frac{W}{L}\right)_n \longrightarrow$ fixed

$\mu_n C_{ox}$, $V_{tn} \longrightarrow$ tech. parameters.

$\rightarrow$ if R_D is varied.

Assume MOSFET is in Saturation,

(i.e., we have taken a value of R_D such that it is in saturation).

$\Rightarrow$ If V_{GS}, $\left(\frac{W}{L}\right)_n$ is fixed $\Rightarrow I_D$ is fixed.

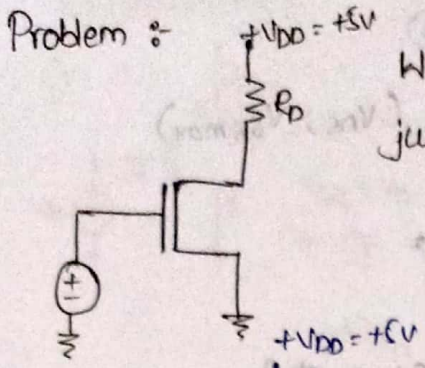
$\Rightarrow$ If $R_D \uparrow$, $\Rightarrow I_D R_D \uparrow \Rightarrow V_{DS} \downarrow$

$\Rightarrow$ for some value of $R_D = R_{Dmax}$, MOSFET will just enters into Edge of Saturation.

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$\Rightarrow$ If $R_D > R_{Dmax} \Rightarrow$ MOSFET will Enters into triode region.

Problem :- What is the max value of R_D such that MOS just enters into Triode region.

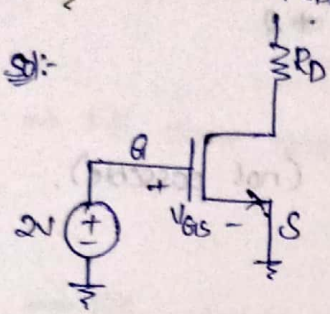


given $\mu_n C_{ox} = 1 mA/V^2$

$V_{tn} = 1V$

$\left(\frac{W}{L}\right)_n = 2$

N180119
M. Sanjakumar



Sol:-

By observation:

$V_{GS} = 2V$

@ $R_D = R_{Dmax} \Rightarrow$ MOSFET is at Edge of Saturation.

@ Edge of saturation,

$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n [V_{GS} - V_{tn}]^2$

$I_D = 1mA$

$V_{DS} = V_{DD} - I_D R_D$

@ Edge of saturation: $V_{DS} = V_{DD} - I_D R_{Dmax}$

$V_{DS} = 5 - I_D R_{Dmax}$

$V_{DS} = 5V - 1mA\, R_{Dmax} \longrightarrow (1)$

@ Edge of saturation: $V_{DS} = V_{GS} - V_{tn}$

$V_{DS} = 2 - 1 = 1V \longrightarrow (2)$

from (1) & (2)

$1V = 5V - 1m R_{Dmax}$

$R_{Dmax} = 4 k\Omega$

If $R_D > R_{Dmax} \Rightarrow$ MOSFET is in triode region.

$R_D \leq R_{Dmax} \Rightarrow$ MOSFET is in saturation region.

For the above problem if $\left(\frac{W}{L}\right)_n$ is doubled then what happens to R_{Dmax}. $\left(\frac{W}{L}\right)_n = 4$

$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n [V_{GS} - V_{tn}]^2$

$= \frac{1}{2} \times 1m \times 4 [2-1]^2 = 2mA \Rightarrow \boxed{I_D = 2mA}$

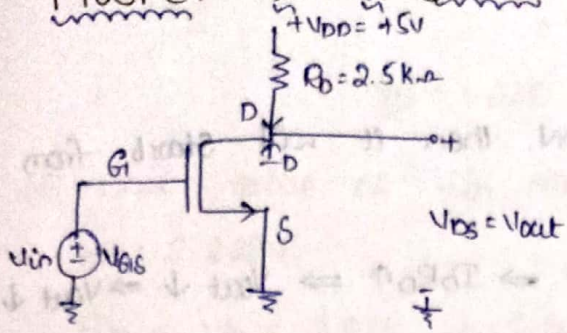
$V_{DS} = 5V - 2mA\, R_{Dmax}$; $V_{DS} = V_{GS} - V_{tn} \Rightarrow V_{DS} = 1V$

$\Rightarrow 1V = 5V - 2mA R_{Dmax}$

$R_{Dmax} = \frac{4}{2mA} \Rightarrow \boxed{R_{Dmax} = 2 k\Omega}$

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MOSFET as a switch:



Digital switch

digital i/p: 0V, V_{DD}

↓ logic '0' ↓ low — ↓ logic '1' ↓ High.

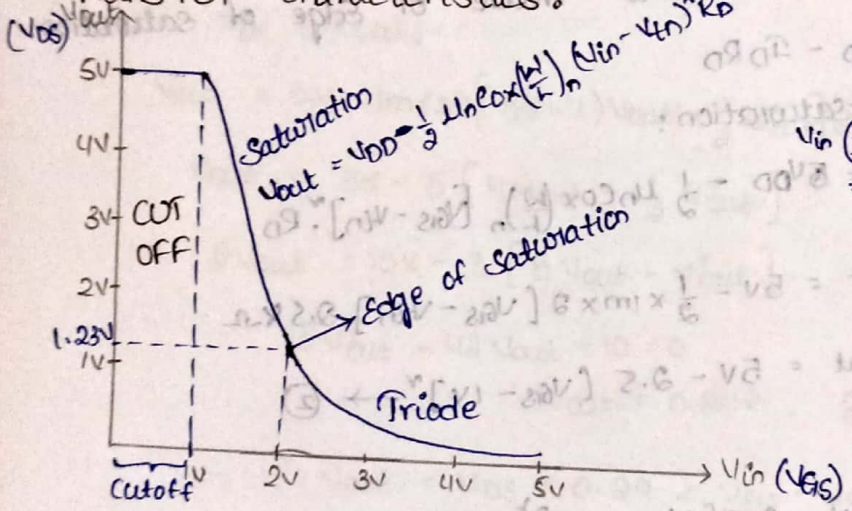
→ for MOSFET to acts as a switch, what is the input V_{GS} of the MOSFET.

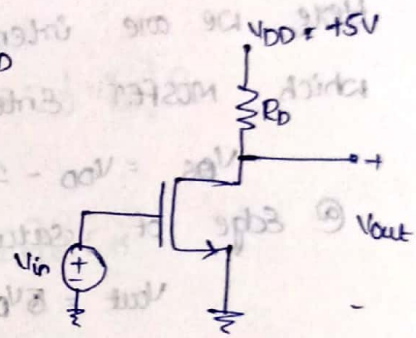
A: $V_{GS} = 0V$ [logic '0'] or $V_{GS} = V_{DD}$ [logic '1']

By observation: $V_{in} = V_{GS}$

$V_{out} = V_{DS} = V_{DD} - I_D R_D$

Transfer characteristics:-





$V_{tn} = 1V$

$\mu_n C_{ox} = mA/V^2$

$\left(\frac{W}{L}\right)_n = 2$

→ If $V_{in} = 0V \Rightarrow V_{in} = V_{GS} = 0V \leq V_{tn} \Rightarrow$ MOSFET : OFF.

$\Rightarrow I_D = 0$

$\Rightarrow V_{out} = V_{DD} - I_D R_D$

$V_{out} = V_{DD} = 5V$

$0 \leq V_{in} < V_{tn} \Rightarrow$ MOSFET OFF $\Rightarrow I_D = 0 \Rightarrow V_{out} = V_{DD} = 5V$

cut-off region.

$\Rightarrow$ cut-off region $\Rightarrow$ MOSFET OFF

$\Rightarrow$ Switch OFF. $\Rightarrow I_D = 0$

By observation:

Slope $= \frac{\partial V_{out}}{\partial V_{in}} = 0$ (cut off) $\because V_{out} = V_{DD}$

→ If V_{in} is just greater than $V_{tn} = 1V \Rightarrow I_D$ will be very less

MOSFET ON $\Rightarrow V_{out} = V_{DD} - I_D R_D$

$= 5V -$ (neglected)

V_{out} nearer to $V_{DD} = 5V$

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$\therefore V_{DS} > V_{GS} - V_{th}$

$\Rightarrow$ Saturation

* As MOSFET just turns ON then it will start from saturation region.

* $\Rightarrow$ If $V_{in} \uparrow \Rightarrow V_{GS} \uparrow \Rightarrow I_D \uparrow \Rightarrow I_D R_D \uparrow \Rightarrow V_{out} \downarrow \Rightarrow V_{out} \downarrow$

if $V_{out} \downarrow \Rightarrow V_{DS} \downarrow$

for some value of $V_{in} = V_{GS} \Rightarrow$ MOSFET will comes at Edge of saturation.

@ Edge of saturation

$$V_{DS} = V_{GS} - V_{th}$$

$$V_{out} = V_{GS} - 1V \longrightarrow (1)$$

Here we are intend to findout the value of V_{in} for which MOSFET Enters into Triode @ Edge of saturation.

$V_{GS} = V_{DD} - I_D R_D$

@ Edge of saturation:

$$V_{out} = 5V_{DD} - \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n [V_{GS} - V_{th}]^2 \cdot R_D$$

$$V_{out} = 5V - \frac{1}{2} \times 1m \times 2 [V_{GS} - V_{th}] 2.5K\Omega$$

$$V_{out} = 5V - 2.5 [V_{GS} - 1V]^2 \longrightarrow (2)$$

from (1) & (2)

$$V_{GS} - 1V = 5V - 2.5[V_{GS} - 1V]^2$$

$$V_{GS} - 1V = 5V - 2.5V_{GS}^2 + 5V_{GS} - 2.5$$

$$2.5V_{GS}^2 - 4V_{GS} - 3.5 = 0$$

$V_{GS} = 2.228V$, $V_{GS} = -0.628$ ×

$\Rightarrow V_{in} = 2.228 > V_{th}$ is correct answer.

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n [V_{GS} - V_{th}]^2$$

$$I_D = \frac{1}{2} (1m)(2)(1.228)^2 = 1.502mA$$

$$V_{DS} = V_{out} = V_{DD} - I_D R_D = 5 - 1.502m \times 2.5K$$

$$V_{DS} = V_{out} = 1.23K$$

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@ Edge of saturation, $V_{GS} = V_{th}$

$= 2.228 - 1 = 1.228$

$V_{GS} = 1.228 \Rightarrow$ same as above.

for what value of V_{in} MOSFET enters into triode region.

$\Rightarrow 2.228V$

$V_{th} \leq V_{in} < 2.228 \Rightarrow$ Saturation region.

for $V_{in} = V_{DD} \Rightarrow$ MOSFET is in triode region. $= 5V$.

In triode region,

$$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[(V_{GS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}^2\right] R_D$$

$$V_{DS} = V_{DD} - I_D R_D$$

In triode,

$$V_{DS} = V_{DD} - \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[(V_{GS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}^2\right] R_D$$

But $V_{DS} = V_{out}$,

$$V_{out} = 5V - 1m(2)\left[(5V - 1)V_{out} - \frac{1}{2} V_{out}^2\right] 2.5K$$

$$V_{out} = 5V - 5\left[4V_{out} - \frac{1}{2} V_{out}^2\right]$$

$$2V_{out} = 10V - 5\left[8V_{out} - V_{out}^2\right]$$

$$.5V_{out}^2 - 42V_{out} + 10 = 0$$

$V_{out} = 0.24V$, $8.15V \times$ $[V_{DS} < V_{GS} - V_t$

$V_{out} = V_{DS} = 0.29 < V_{GS} - V_{th}(4V)$

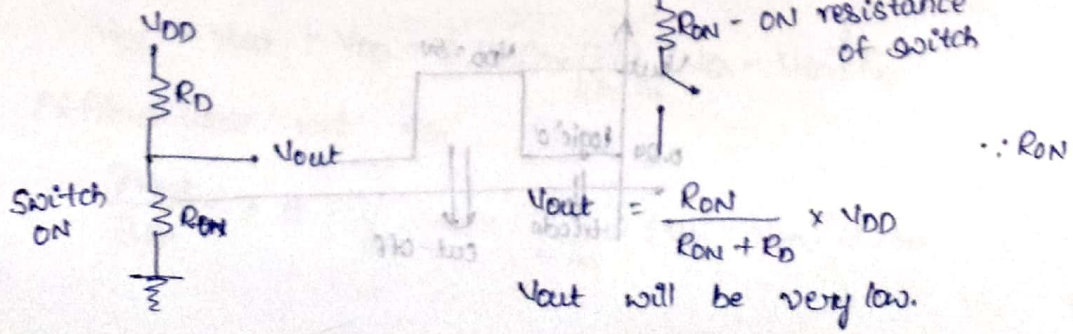
$$I_D = \frac{V_{DD} - V_{DS}}{R_D} = \frac{5 - 0.24}{2.5K} = 1.9mA$$

$V_{in} = V_{DD} = 5V \Rightarrow V_{out} = 0.24V$ & $I_D = 1.9mA$

$\Rightarrow$ MOSFET ON.

Practical Switch:-

ON Switch:



$\therefore R_{ON}$

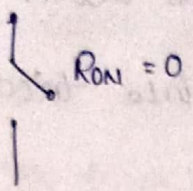
$$V_{out} = \frac{R_{ON}}{R_{ON} + R_D} \times V_{DD}$$

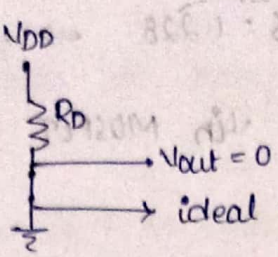
V_{out} will be very low.

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* If the switch is ON, Vout will be very less.

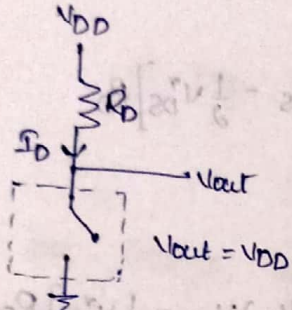
Ideal Switch





Practical Switch

OFF Switch:



If the switch is OFF

$V_{DD} = V_{out}$

So far, in cut-off region

$V_{in} = 0V$

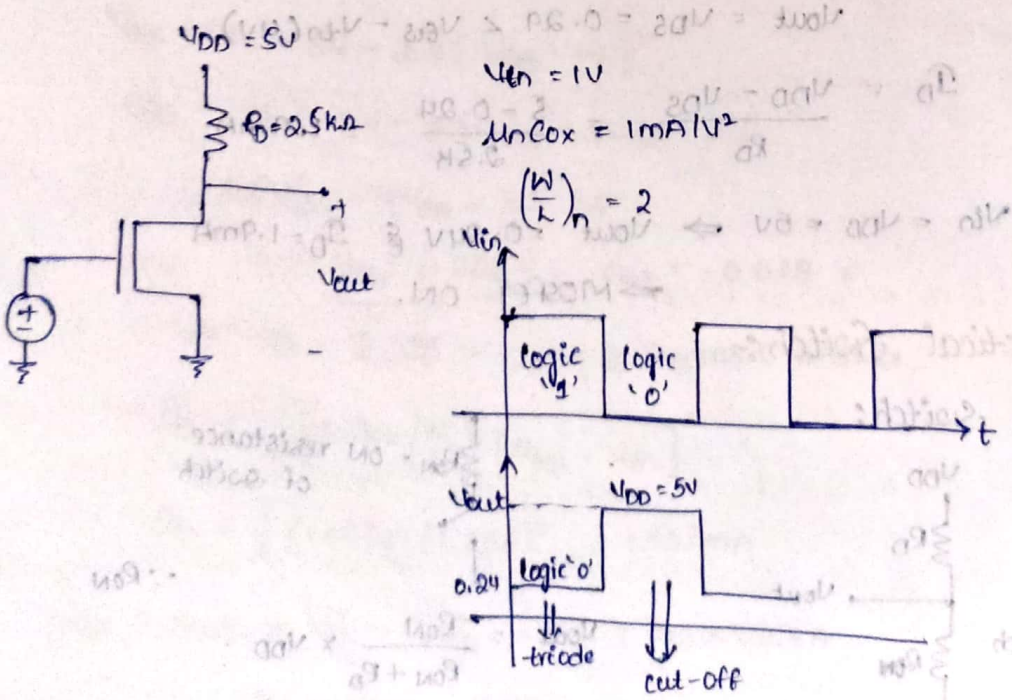
$\Rightarrow V_{out} = V_{DD} = 5V \Rightarrow$ OFF switch.

* In triode region $\Rightarrow V_{out} = 0.24V \Rightarrow$ ON switch (Low value)

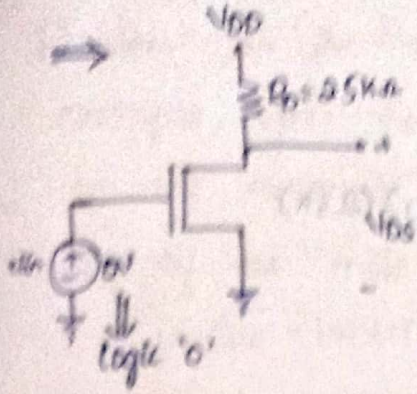
$V_{in} = V_{DD} = 5V$

$\Rightarrow$ Slope $\frac{\partial V_{out}}{\partial V_{in}}$ in cut-off Region is zero.

$\Rightarrow$ Slope $\frac{\partial V_{out}}{\partial V_{in}}$ in triode Region is less.



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Given,

$V_{th} = 1V$

$\mu_n C_{ox} = 1mA/V^2$

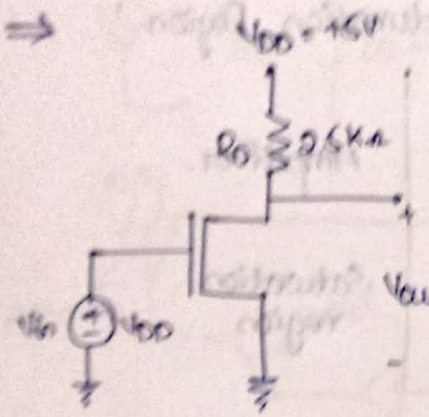
$\left(\frac{W}{L}\right)_n = 2$

i/p → logic '0'

o/p → logic '1'.

V_{in} - control voltage

It is in cut-off region (OFF switch)



V_{in} - control voltage

It is in triode region (ON)

i/p → logic '1'

o/p → logic '0'.

$\Rightarrow 0V \leq V_{in} < V_{th} \Rightarrow$ cut-off region.

$V_{th} \leq V_{in} \leq 2.228V \Rightarrow$ Saturation Region.

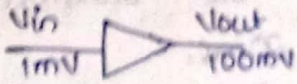
$2.228 < V_{in} \leq V_{DD} \Rightarrow$ Triode region.

Here we want to find slope in saturation region.

at $V_{in} = 1.814V \left(\frac{1+2.228}{2}\right)$

Slope = $\frac{\partial V_{out}}{\partial V_{in}} = \frac{\text{change in o/p}}{\text{change in i/p}}$ = Gain = voltage gain.

= no units = volt/volt



$\frac{V_{out}}{V_{in}} = \frac{100mA}{1mA} = 100$

We know $V_{out} = V_{DD} - I_D R_D$

In sat,

$V_{DS} = V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{in} - V_{th})^2 R_D$

Differentiate wrt V_{in},

$\frac{\partial V_{out}}{\partial V_{in}} = 0 - \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n 2(V_{in} - V_{th})^{2-1} R_D$

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$$\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{in} - V_{tn}) R_D$$

Now, $\left.\frac{\partial V_{out}}{\partial V_{in}}\right|_{\text{at } V_{in} = 1.614V} = -1m \times 2(1.614 - 1)(2.5K)$

$= -3.07$ V/V

$$\left|\frac{\partial V_{out}}{\partial V_{in}}\right| = 3.07 \text{ V/V} > 1$$

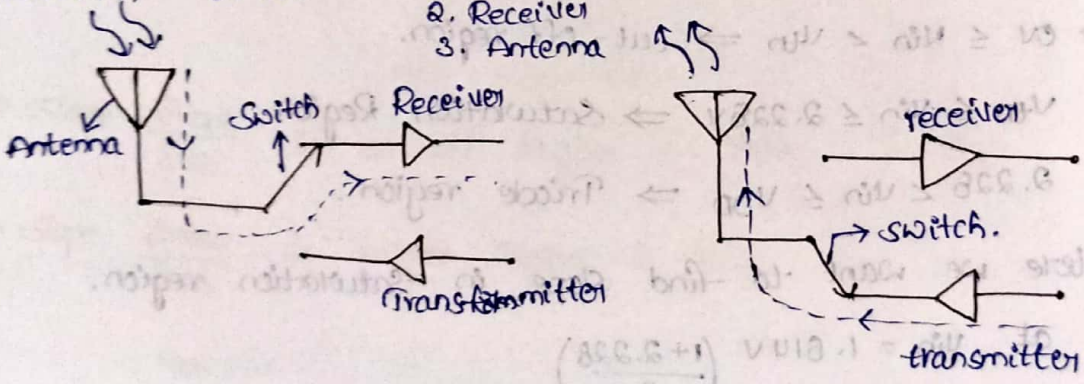
This is nothing but Amplification.
Amplification is done by Amplifier.

* MOSFET acts as Amplifier in 'Saturation Region.'

MOSFET	V_{in} = logic '1' ON Switch	V_{in} = logic '0' OFF Switch	Amplifier.
Region of Operation	Triode region	cut-off region	Saturation region

Cordless Phone :

1. Transmitter
2. Receiver
3. Antenna



⇒ The Antenna is alternatively connected to the receiver and the transmitter in regularly intervals.
Eg: 20ms.
That's why Electronic Antena switch is needed there.

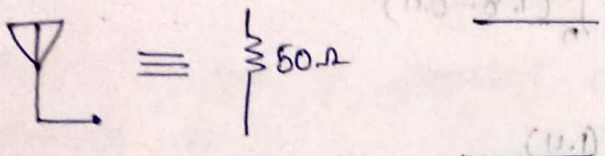
⇒ This cordless phone in the above example receives half of the time and transmitts for the other half.

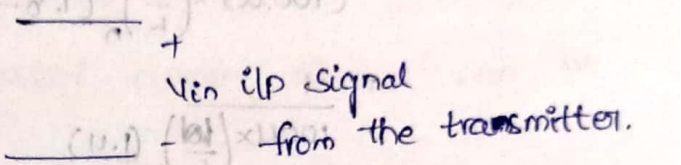
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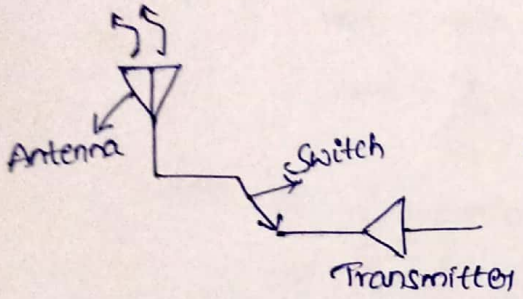
Problem :- In the cordless phone as shown in above example, here the switch is connecting the transmitter to the Antenna must negligibly attenuate the signal. Eg: by not more than 10% if $V_{DD} = 1.8V$

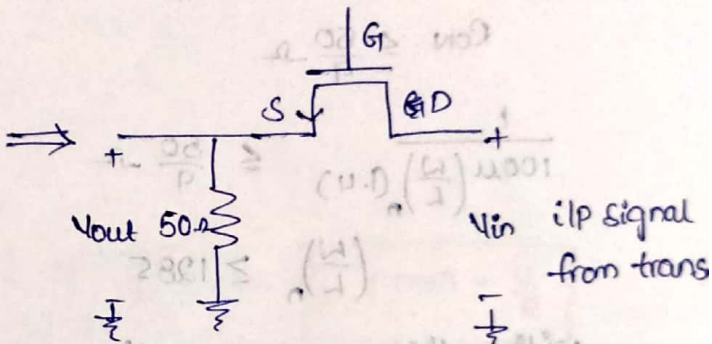
$\mu_n C_{ox} = 100 \mu A/V^2$, $V_{th} = 0.4V$. Determine the minimum required aspect ratio of switch.

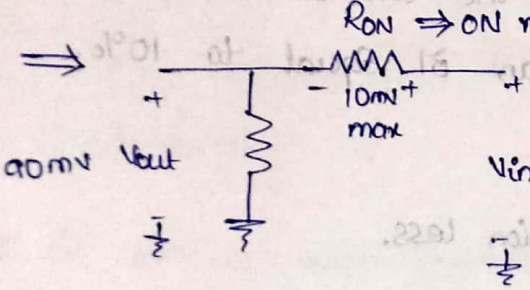
Assume the antena can be modelled as 50Ω resistor.











$\frac{V_{out}}{V_{in}} \geq 0.9$

* The purpose of switch to transfer the ilp signal from the transmitter to the Antenna with very less voltage drop across the switch.

From the given data, the switch can attenuate a maximum of 10% of the ilp signal from the transmitter.

$$\Rightarrow \frac{V_{out}}{V_{in}} \geq 0.9 \qquad V_{out} = \frac{50}{50 + R_{ON}} \times V_{in}$$

$$\frac{50\Omega}{50\Omega + R_{ON}} \geq 0.9$$

$$R_{ON} \leq \frac{50}{9}\Omega$$

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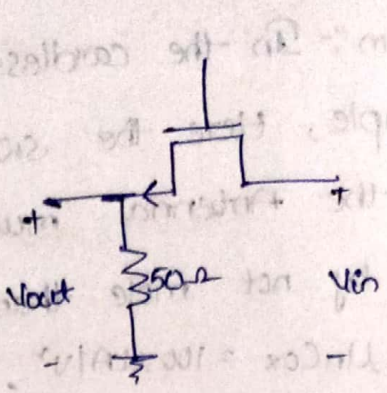
$$R_{ON} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS} - V_{tn})}$$

$V_{GS} = V_G - V_S$

$= V_{DD} - (\text{milli volts})$

$V_{GS} = 1.8V - (\text{mV}) \to 0$

$\boxed{V_{GS} \simeq 1.8V}$ $\boxed{V_S = V_{out}}$



$$\Rightarrow R_{ON} = \frac{1}{(100\mu) \times \left(\frac{W}{L}\right)_n (1.8 - 0.4)}$$

$$= \frac{1}{100\mu \times \left(\frac{W}{L}\right)_n (1.4)}$$

$$R_{ON} \leq \frac{50}{9}\ \Omega$$

$$\frac{1}{100\mu \left(\frac{W}{L}\right)_n (1.4)} \leq \frac{50}{9}\ \Omega$$

$$\left(\frac{W}{L}\right)_n \geq 1285$$

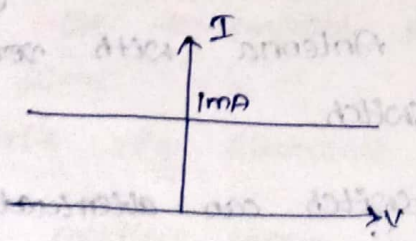
With this aspect ratio the attenuation is the switch will be less than or Equal to 10%.

$\Rightarrow \left(\frac{W}{L}\right)_n \uparrow \Rightarrow R_{ON} \downarrow$

$\Rightarrow$ Attenuation less.

31/12/21

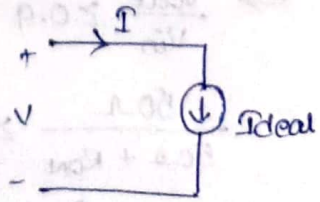
I-V char. of Ideal current source



$\Rightarrow$ There is no dependence of 'I' on 'V'

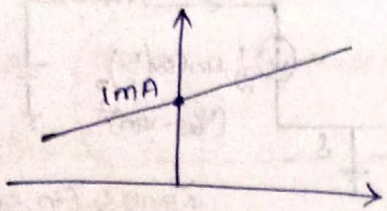
$\boxed{I = 1mA}$; for all 'V'.

This I-V char. of ideal current source can be modelled as



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I-V characteristics of practical source.



⇒ Here there is a dependence of 'I' on 'V'.

$$I = I_{mA} + K.V \quad ; \quad K > 0$$

i.e., for $V > 0 \Rightarrow I > I_{mA}$

$V < 0 \Rightarrow I < I_{mA}$

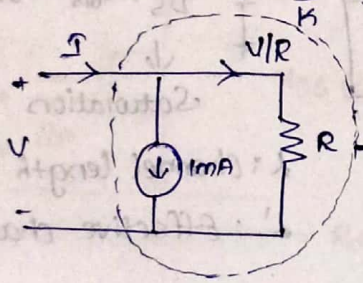
This IV char. of practical current source can be modelled as

$$I = I_{mA} + K.V$$

$$= I_{mA} + \frac{V}{\left(\frac{1}{K}\right)}$$

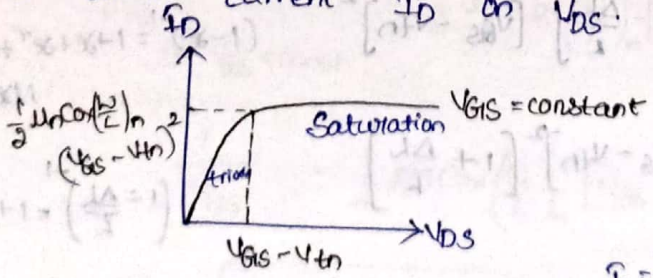
unit of $\frac{1}{K}$: ohms

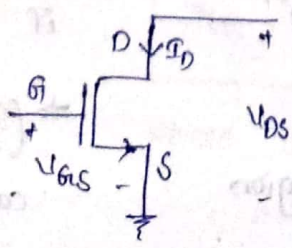
Let $R = \frac{1}{K} \Rightarrow K = \frac{1}{R} \Rightarrow$ $\boxed{I = I_{mA} + \frac{V}{R}}$

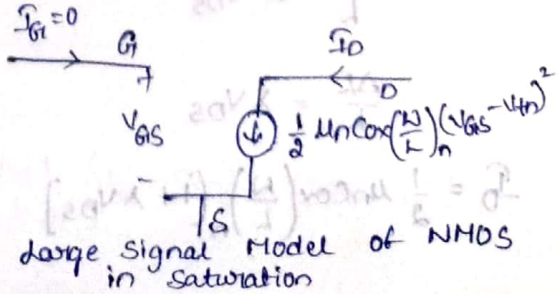


→ practical current source.

* So far, we have assumed when $V_{DS} = V_{DS\,sat} = V_{GS} - V_{th}$ then MOSFET Enters saturation & it acts as a constant current source. i.e., there is no dependence of drain current I_D on V_{DS}.

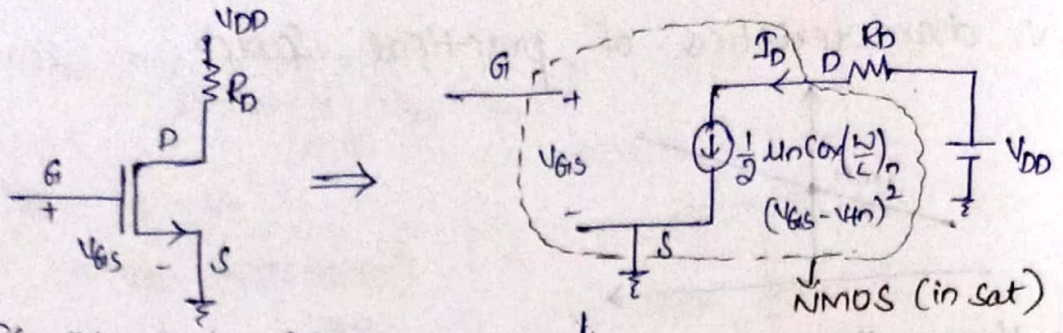






large signal Model of NMOS in saturation

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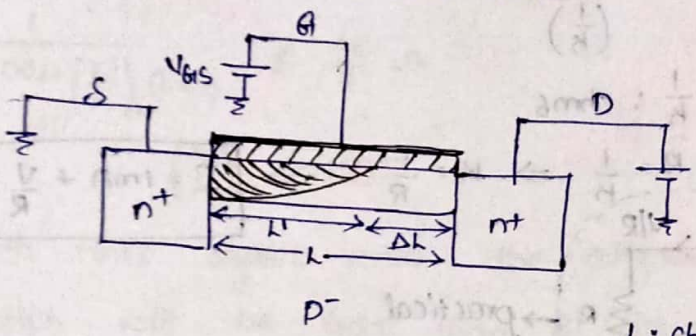


If this is in Saturation ⇒ this will be Equivalent Circuit.

⇒ But in practical, there is a dependency of drain current I_D on V_{DS}.

When $V_{DS} = V_{DS,sat} = V_{GS} - V_{tn}$ ⇒ pinch off occurs.
⇒ pinch off

When $V_{DS} > V_{GS} - V_{tn}$ ⇒ pinch off point will move towards source side.



$V_{DS} > V_{GS} - V_{tn}$
↓
Saturation

L : Channel length
L' : Effective channel length.

In Saturation,

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L'}\right)\left[V_{GS} - V_{tn}\right]^2$$

$L = L' + \Delta L$

$L' = L - \Delta L$

$L' = L\left[1 - \frac{\Delta L}{L}\right]$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L\left(1-\frac{\Delta L}{L}\right)}\left[V_{GS} - V_{tn}\right]^2$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[1 - \frac{\Delta L}{L}\right]^{-1}\left[V_{GS} - V_{tn}\right]^2$$

$(1-x)^{-1} = 1 + x + x^2 + \cdots$; $|x| < 1$

$$= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left[V_{GS} - V_{tn}\right]^2\left[1 + \frac{\Delta L}{L}\right]$$

$\left(1 - \frac{\Delta L}{L}\right)^{-1} = 1 + \frac{\Delta L}{L} + \left(\frac{\Delta L}{L}\right)^2 + \cdots$

$\frac{\Delta L}{L} \propto V_{DS}$

unit of λ : V^{-1}

$\frac{\Delta L}{L} = \lambda V_{DS}$

if $\frac{\Delta L}{L} << 1$

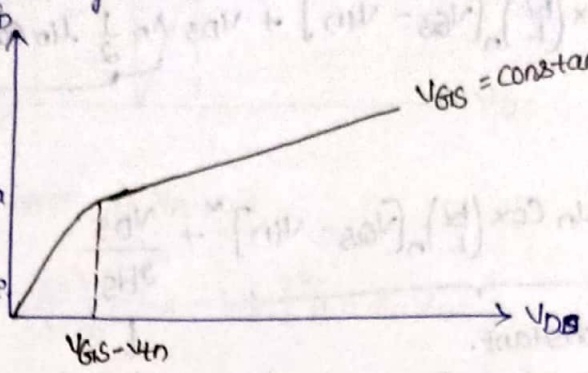
⇒ $\left(\frac{\Delta L}{L}\right)^2, \left(\frac{\Delta L}{L}\right)^3, \cdots$ can be neglected

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n\left[1 + \lambda V_{DS}\right]$$ Saturation region

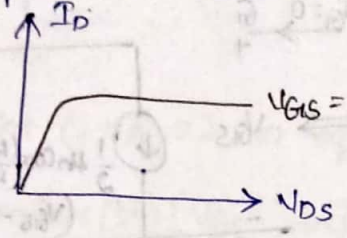
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From the above eq'n, we can say that drain current I_D has linear dependence on V_{DS}.

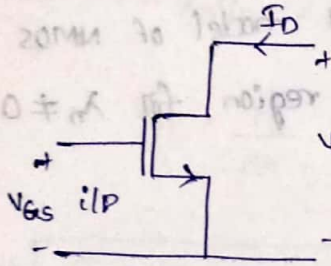
From this I_D-V_D char. we can say MOSFET acts as a current source with finite o/p resistance



→ If $\lambda = 0$; MOSFET acts as ideal current source ie, having infinite output resistance in saturation region.



Now, we will find finite o/p resistance in practical



R_{ds} is defined as:

o/p resistance = R_{ds} ; $R_{ds} = \left.\frac{\partial V_{DS}}{\partial I_D}\right|_{@\ V_{GS}=\text{const}} = \frac{1}{\left(\frac{\partial I_D}{\partial V_{DS}}\right)}$

In Sat:

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n \left[V_{GS} - V_{tn}\right]^2 \left[1 + \lambda_n V_{DS}\right]$$

Differentiate wrt V_{DS}

$$\left.\frac{\partial I_D}{\partial V_{DS}}\right|_{@\ V_{GS}=\text{const}} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n \left[V_{GS} - V_{tn}\right]^2 \left[0 + \lambda_n\right]$$

$$\frac{1}{g_{ds}} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n \left[V_{GS} - V_{tn}\right]^2 \left[\lambda_n\right]$$

$$\boxed{g_{ds} = \frac{1}{\lambda_n I_D}}$$

where $I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n \left[V_{GS} - V_{tn}\right]^2$ when $\lambda_n = 0$

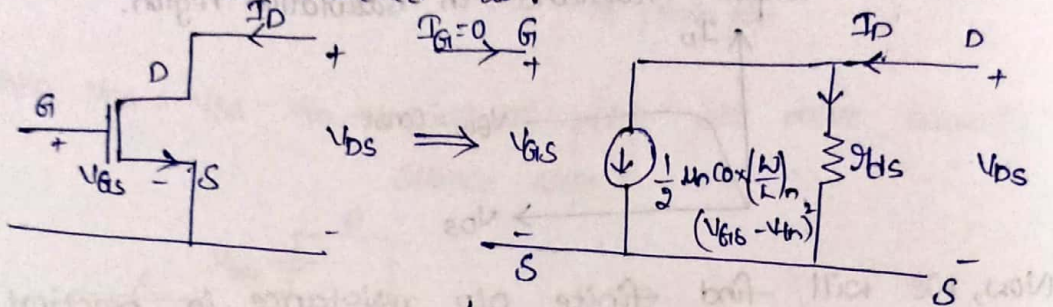
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$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS}-V_{tn})^2 [1+\lambda_n V_{DS}]$$

$$= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS}-V_{tn}]^2 + V_{DS}\lambda_n \underbrace{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS}-V_{tn})^2}_{g_{DS}}$$

$$\Rightarrow I_D = \underbrace{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS}-V_{tn}]^2}_{\text{constant. No dependence of } V_{DS}} + \underbrace{\frac{V_{DS}}{g_{DS}}}_{\text{dependence on } V_{DS}}$$

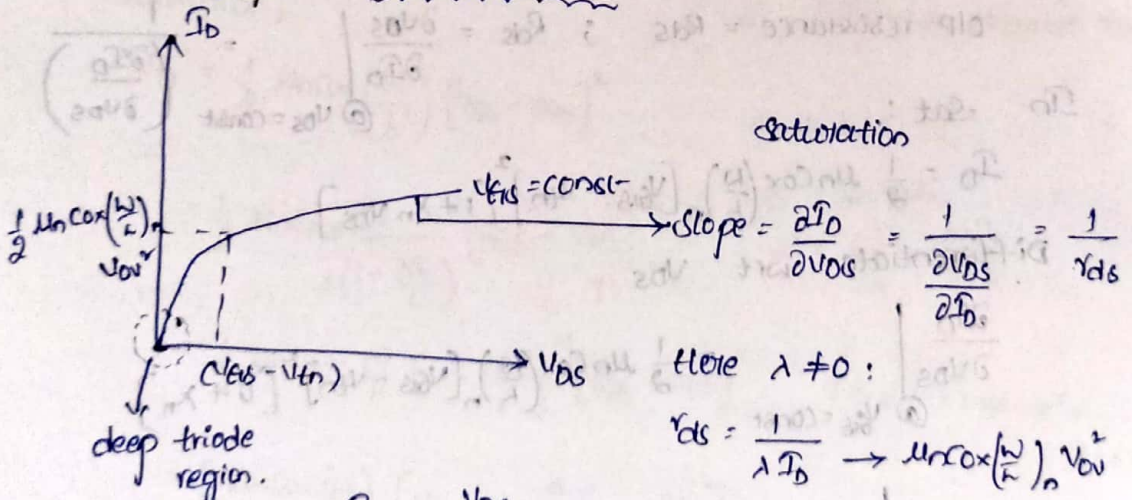
This can be modelled as :



Large signal model of NMOS in Saturation region for $\lambda_n \neq 0$

3/11/22.

NMOS Output characteristics :-



Here $\lambda \neq 0$:

$$r_{ds} = \frac{1}{\lambda I_D} \rightarrow \mu_n C_{ox}\left(\frac{W}{L}\right)_n V_{ov}^2$$

$$R_{ON} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS}-V_{tn})}$$

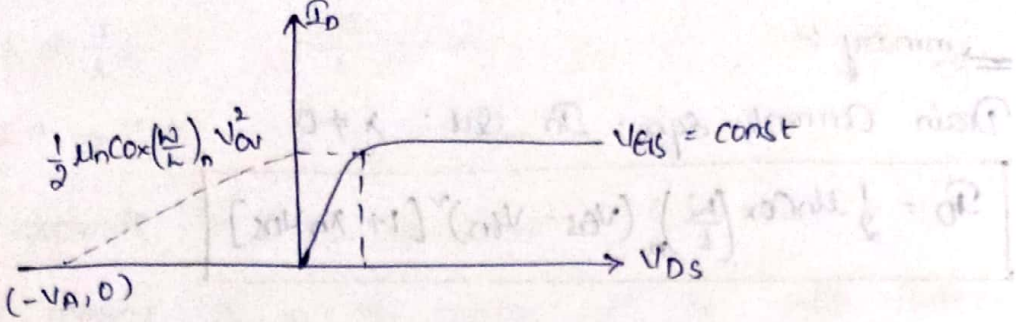
if $\lambda = 0$: $r_{ds} = \frac{1}{0 \cdot I_D} = \infty$

In Sat :

i.e., $\lambda_n \neq 0$

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS}-V_{tn}]^2 [1+r_{ds}^2]$$

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eqn (1) = 0 point $(-V_A, 0)$

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS} - V_{tn}]^2 [1 + \lambda_n V_{DS}] \quad (1)$$

$(-V_A, 0)$

$$0 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS} - V_{tn}]^2 [1 + \lambda_n] V_{DS}$$

$$V_{DS} = -\frac{1}{\lambda_n}$$

Substitute point $(-V_A, 0)$ in eq(1)

$$0 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS} - V_{tn}]^2 [1 + \lambda_n(-V_A)]$$

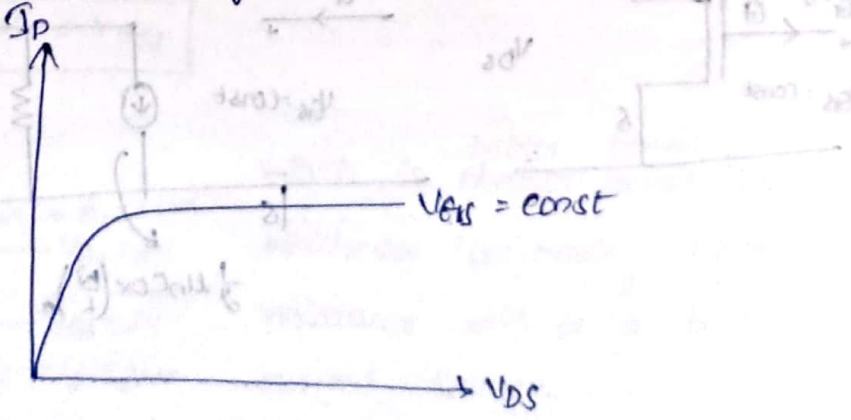
$$1 - \lambda_n V_A = \frac{0}{(1)}$$

V_A : Early voltage : $V_A > 0$

$$V_A = \frac{1}{\lambda_n} \Rightarrow \boxed{\lambda_n = \frac{1}{V_A}}$$

$$\Rightarrow \boxed{I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS} - V_{tn}]^2 \left[1 + \frac{V_{DS}}{V_A}\right]}$$

→ In problems : if it gives as no channel length modulation it means $\lambda = 0$ (or) $V_A = \infty$ i.e., no dependence of I_D (or) V_{DS} in Saturation region.



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Summary :-

Drain Current Eqn : I_D Sat : $\lambda \neq 0$

$$\boxed{I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS} - V_{tn})^2 [1 + \lambda_n V_{DS}]}$$

$$= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS} - V_{tn})^2 \left[1 + \frac{V_{DS}}{V_A}\right]$$

Similarly in PMOS

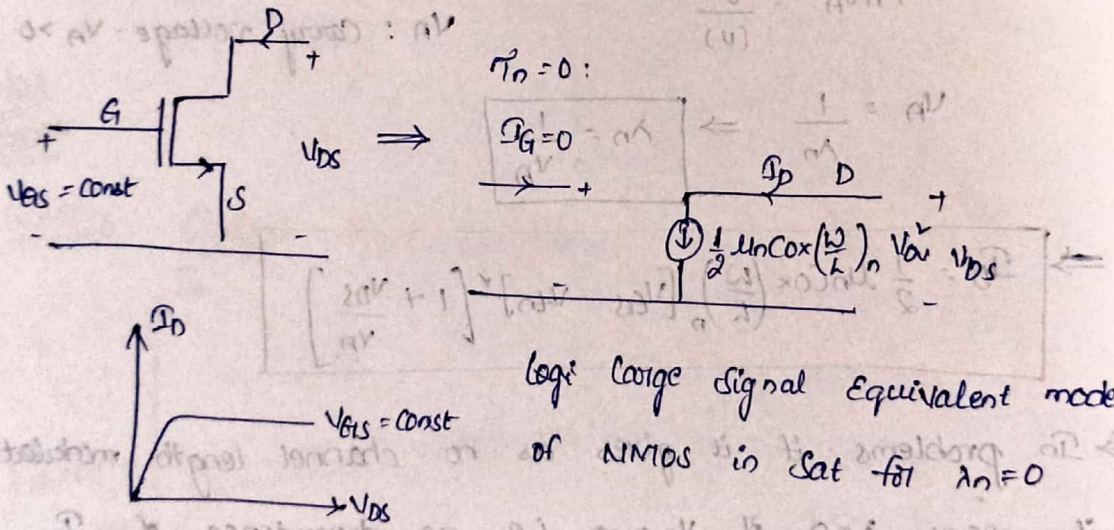
$$I_{Dp} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p [V_{SGp} - |V_{tp}|^2][1 + \lambda_p |V_{SDp}]$$

$$= \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p [V_{SGp} - |V_{tp}|^2]\left[1 + \frac{V_{SDp}}{|V_A|}\right]$$

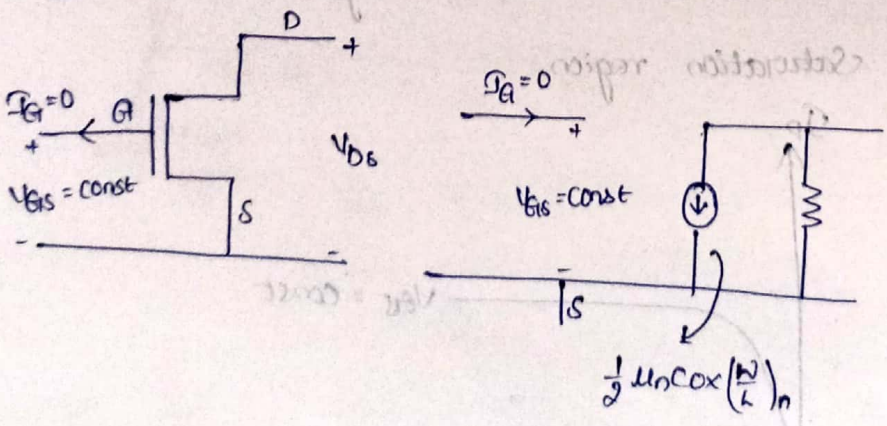
Observation :-

$\lambda_n \longrightarrow +ve$

$I_p \longrightarrow -ve$



Logic Large signal Equivalent model of NMOS in Sat for $\lambda_n = 0$



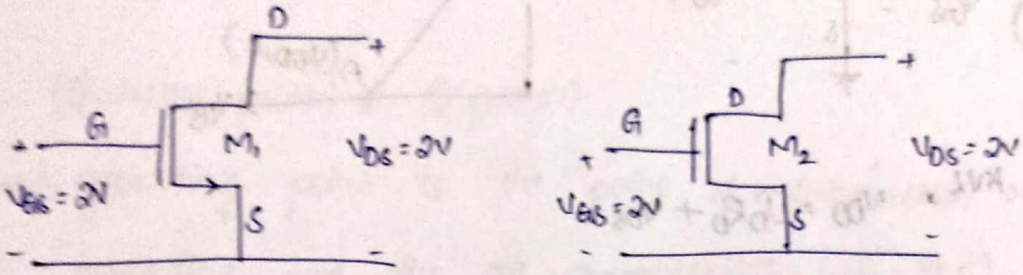
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$\Rightarrow \lambda \propto \frac{1}{L}$ $\qquad \frac{\Delta L}{L} \propto V_{DS}$

if $L \uparrow \Rightarrow \lambda \downarrow$ $\qquad \frac{\Delta L}{L} = \lambda V_{DS}$

$\Rightarrow I_D$ depends on V_{DS} decreases

$\Rightarrow$ It means I_D vs V_{DS} curve will be more flatter in saturation region.



$V_{tn} = 1V$ $\qquad$ By observation $\qquad$ $V_{tn} = 1V$

$\frac{W_1}{L_1} = \frac{2\mu m}{1\mu m}$ $\qquad$ Both M_1, M_2 are in sat $\qquad$ $\frac{W_2}{L_2} = \frac{4\mu m}{2\mu m}$

$\mu_n C_{ox} = 1 mA/V^2$ $\qquad$ $V_{DS} = V_{GS}$ $\qquad$ $\mu_n C_{ox} = 1 mA/V^2$

$\lambda_{n_1} \neq 0$ $\qquad$ $\lambda_{n_2} \neq 0$

Moreover

$\mu_n C_{ox}$, V_{tn}, $\frac{W}{L}$ same

$\therefore I_D$ is also same.

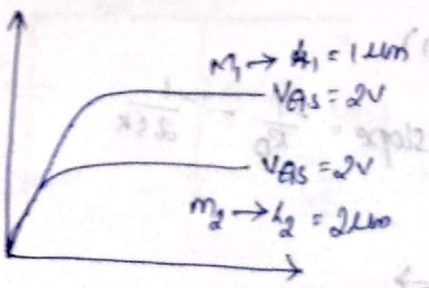
By observation: $L_1 < L_2 \Rightarrow$ from Eqn (2) $\Rightarrow \boxed{\lambda_{n_1} > \lambda_{n_2}}$

$\Rightarrow \boxed{r_{ds1} < r_{ds2}}$

$r_{ds1} = \frac{1}{\lambda_{n_1} I_D} = r_{ds2} = \frac{1}{\lambda_{n_2} I_D}$

$\boxed{r_{ds1} < r_{ds2}}$

*



Which is better current source?

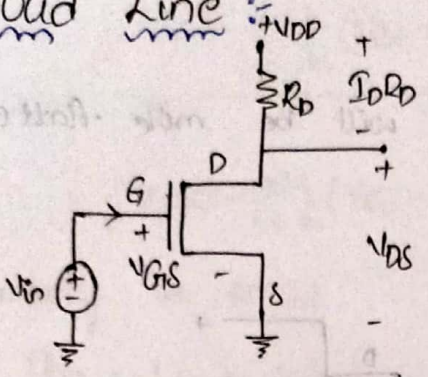
Whichever is having higher r_{ds} resistance will be a better current source.

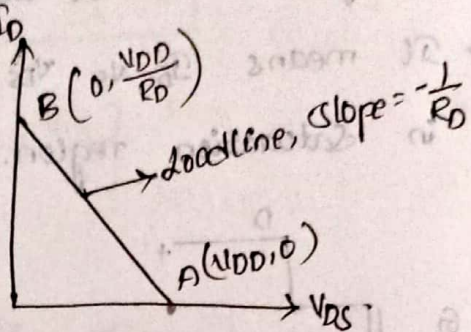
$\Rightarrow M_2$ acts as better current source than M_1

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⟹ Longer channel MOSFET has lower λ_n & higher r_{ds}.

Load Line :-





Apply KVL, $V_{DD} = I_D R_D + V_{DS}$

$I_D = -\frac{1}{R_D} V_{DS} + \frac{V_{DD}}{R_D}$ → load line.

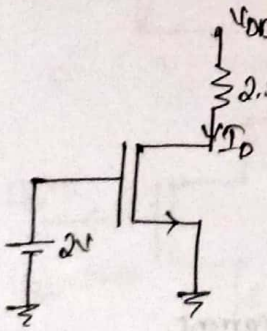
$y = mx + c$ ⇒ Straight line with slope $m = \frac{-1}{R_D}$ & y-intercept $= \frac{V_{DD}}{R_D}$

This lets x-axis & y-axis at A & B point

x-axis :- put $y = 0 \Rightarrow I_D = 0 \Rightarrow 0 = -\frac{1}{R_D} V_{DS} + \frac{V_{DD}}{R_D} \Rightarrow \boxed{V_{DS} = V_{DD}}$

y-axis :- put $x = 0 \Rightarrow V_{DS} = 0 \Rightarrow I_D = -\frac{1}{R_D}(0) + \frac{V_{DD}}{R_D} \Rightarrow I_D = \frac{V_{DD}}{R_D}$

Problem :- i, Draw the load line for the ckt shown below.



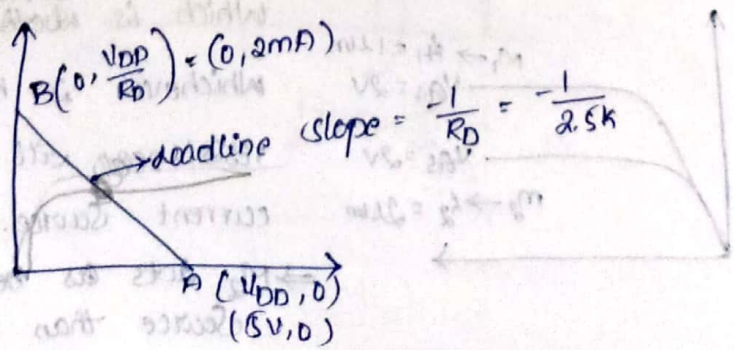
Given

$V_{th} = 1V$

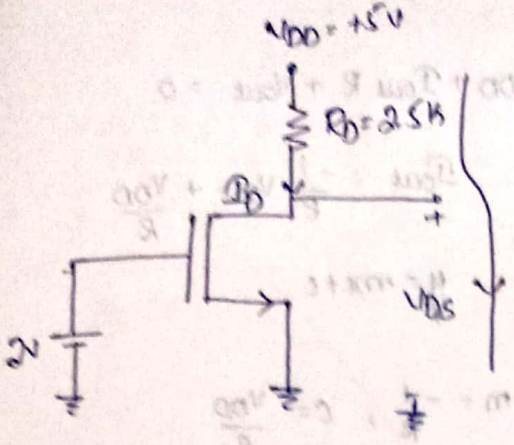
$\left(\frac{W}{L}\right)_n = 2$

$\mu_n C_{ox} = 1mA/V^2$

ii, find the operating point (Q) (V_{DSQ}, I_{DQ})



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Apply KVL in outer loop

$$V_{DD} = I_D R_D + V_{DS}$$

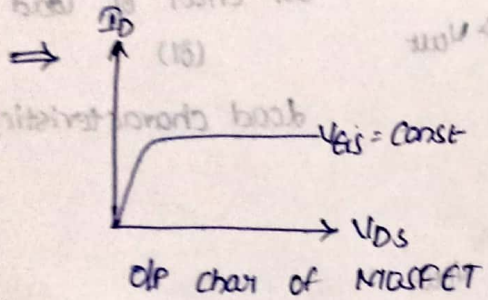
$$I_D = -\frac{1}{R_D} V_{DS} + \frac{V_{DD}}{R_D}$$

$$y = mx + c$$

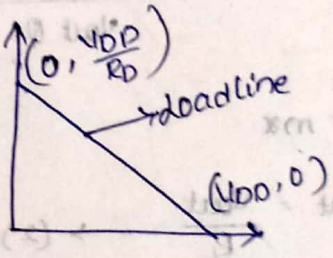
(Quiscent point) or (Q.point)

⟹ operating point is the point of intersection of load line and the o/p characteristics ($I_D - V_{DS}$) of a MOSFET

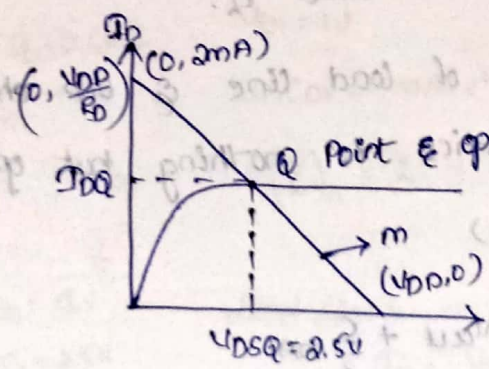
Q.Point $[V_{DSQ}, I_{DQ}]$



o/p char of MOSFET

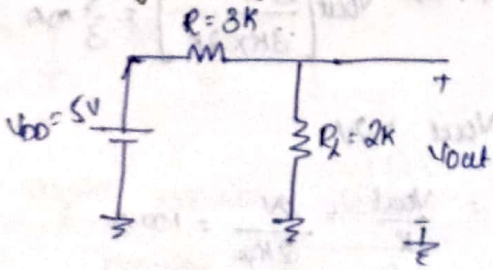


⟹

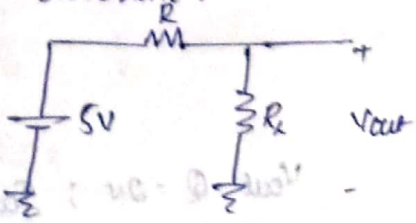


$$m = -\frac{1}{R_D} = -\frac{1}{2.5K}$$

Explaining :- Q.point concept using a simple resistive divider.



Loadline :



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$V_{out} = \frac{R_L}{R+R_L} \times 5V$

$V_{out} = 2V$

$I_{out} = \frac{5}{R+R_L} = 1mA$

Q. point : operating point

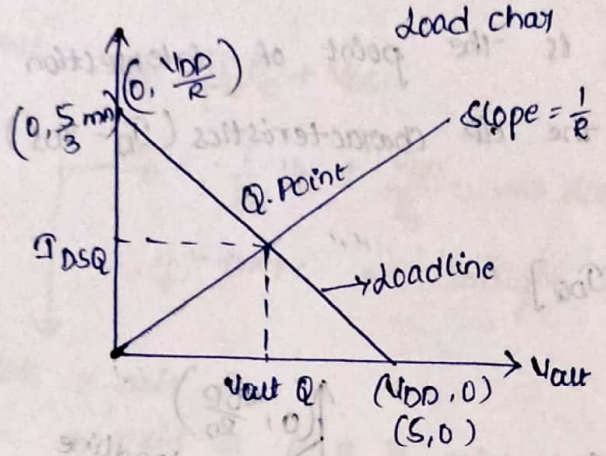
$(2V, 1mA)$

$-V_{DD} + I_{out} R + V_{out} = 0$

$I_{out} = -\frac{1}{R} V_{out} + \frac{V_{DD}}{R}$

$\therefore y = mx + c$

$m = -\frac{1}{R}, \quad c = \frac{V_{DD}}{R}$



$I_{out} = -\frac{1}{3K} V_{out} + \frac{5}{3}mA$ → (1)

load line Eqn

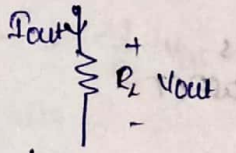
OIP char of load

(or)

load characteristics

$y = mx$

$I_{out} = \frac{V_{out}}{R_L}$ → (2)



load char (or) OIP char of load R_L.

⇒ point of intersection of load line & OIP char of load or load characteristics is nothing but operating point (Q) from (1) & (2)

$\frac{V_{out}}{2K\Omega} = -\frac{1}{3K\Omega} V_{out} + \frac{5}{3}mA$

$V_{out}\left[\frac{1}{2K} + \frac{1}{3K}\right] = \frac{5}{3}mA \Rightarrow V_{out}\left[\frac{5K}{3K \times 2K}\right] = \frac{5}{3}mA$

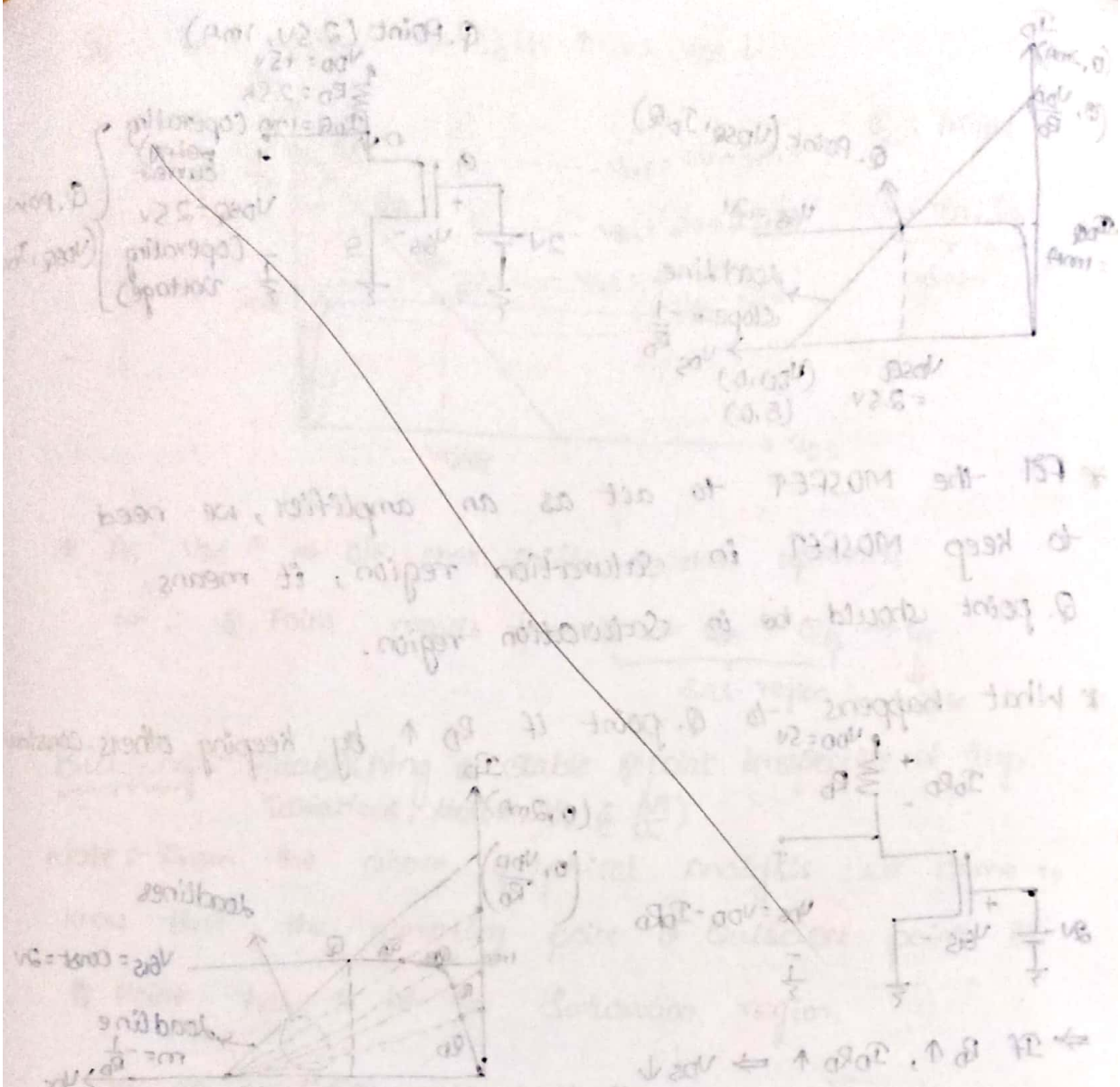
$\Rightarrow V_{out} = 2V$

$I_{out} = \frac{V_{out}}{R} = \frac{2V}{2K\Omega} = 1mA$

$V_{out}\ Q = 2V \; ; \; I_{out}\ Q = 1mA$

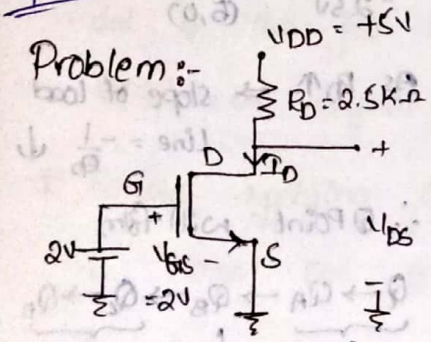
$Q\ (V_{out}\ Q, I_{out}\ Q) = (2V, 1mA)$

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4/1/22

Problem :-

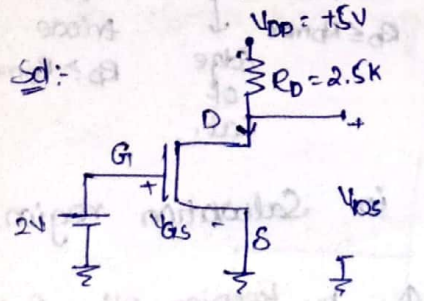


$V_{th} = 1V$

$\mu_n C_{ox} = 1mA/V^2$

$\left(\frac{W}{L}\right)_n = 2$

Sol :-



Load Line :

$$I_D = \frac{V_{DD} - V_{DS}}{R_D}$$

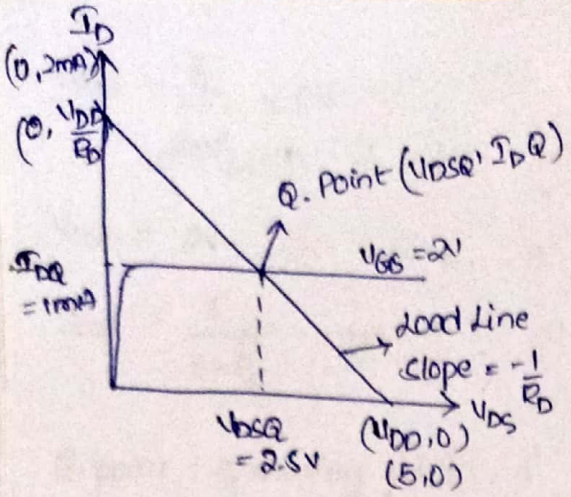
$$I_D = -\frac{1}{R_D} V_{DS} + \frac{V_{DD}}{R_D}$$

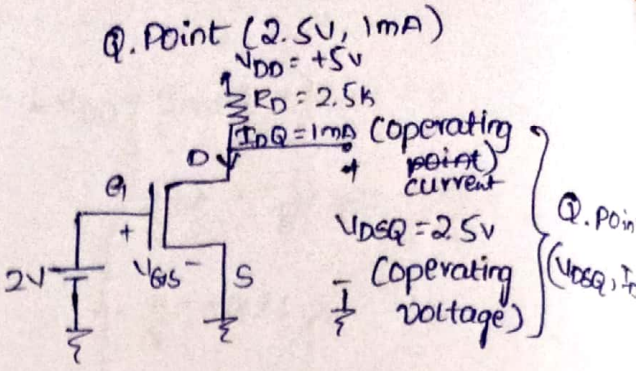
Slope $= -\frac{1}{R_D}$, y intercept $= \frac{V_{DD}}{R_D} = 2mA$

$= -\frac{1}{2.5K}$

asper previous solved problem $\boxed{I_D = 1mA}$

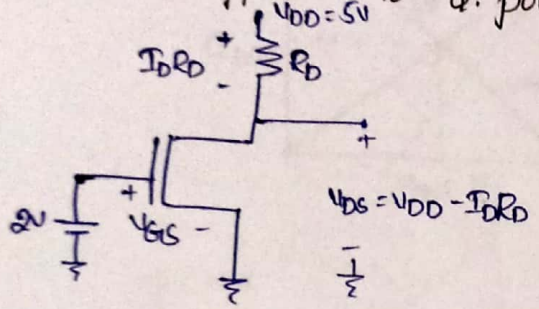
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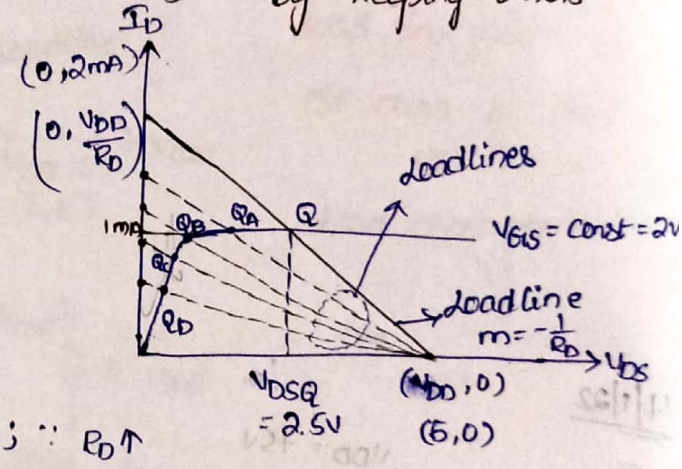




* For the MOSFET to act as an amplifier, we need to keep MOSFET in saturation region, it means Q. point should be in saturation region.

* What happens to Q. point if R_D ↑ by keeping others consta





⇒ If R_D ↑, I_DR_D ↑ ⇒ V_{DS} ↓

⇒ Here only load line changes ; ∵ R_D ↑

⇒ O/P char. fixed ; ∵ V_{GS} = Constant

As R_D ↑ ⇒ slope of load line = $-\frac{1}{R_D}$ ↓

∴ Q Point will form

$Q \rightarrow Q_A \rightarrow Q_B \rightarrow Q_C \rightarrow Q_D$

$Q \rightarrow Q_A$: $R_D \leq R_{Dmax}$

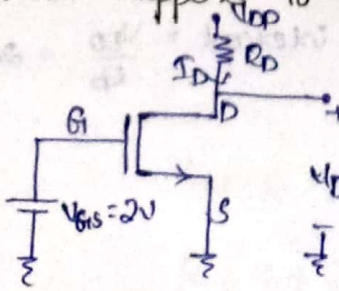
Q_B : Edge of Sat.

$Q_C \rightarrow Q_D$: triode $R_D > R_{Dmax}$

* If $R_D > R_{Dmax}$ then Q. Point will move into triode region. therefore MOSFET will not acts as an amplifier in this region.

That's why we want to keep Q. Point in Saturation region.

* What happens to the Q. Point if V_{GS} ↑, by keeping other Const.



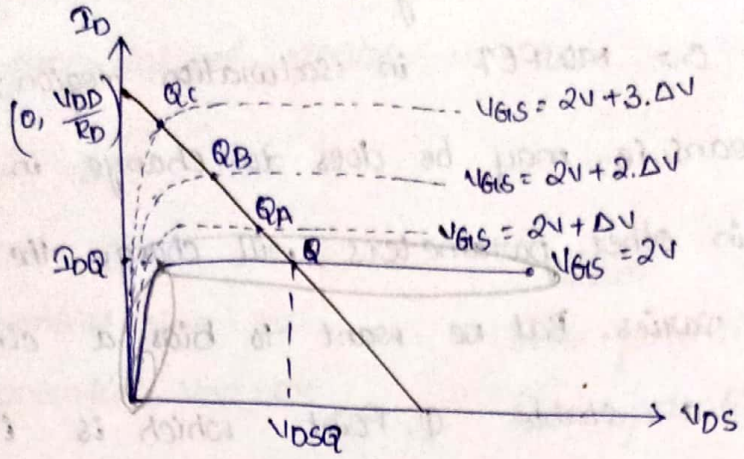
By observation:

i, Load line doesn't change since R_D is fixed.

ii, O/P char. changes because V_{GS} ↑

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If $V_{GS} \uparrow \Rightarrow I_D \uparrow \Rightarrow I_D R_D \uparrow \Rightarrow V_{DS} \downarrow$



Q_C : triode

Q, Q_A, Q_B — Sat.

* As $V_{GS} \uparrow \Rightarrow$ O/P char. shifts towards upwards

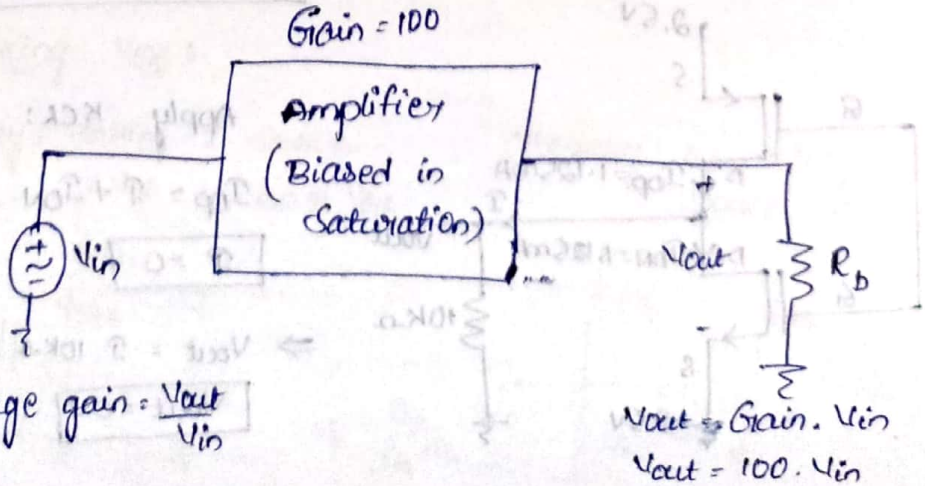
$\Rightarrow \therefore$ Q. Point moves from $Q \rightarrow Q_A \rightarrow Q_B \rightarrow Q_C$ (Sat. region; Q_C ↓ triode)

Biasing :- Establishing a stable Q.point irrespective of temp. variations, $\mu_n C_{ox}$, V_t & $(\frac{W}{L})$

Note :- From the above graphical Analysis we came to know that the operating point or Quiscient point or Q. Point has to be in Saturation region.

* In an amplifier, we basically give input as ac sinosoidal & the job of an amplifier is to amplify the input ac signal.

* Before applying ac input to the amplifier, we have to keep our Q. Point in Saturation. Keeping Q. Point in Saturation region is known as Biasing



Voltage gain = $\frac{V_{out}}{V_{in}}$

$V_{out} = Gain . V_{in}$

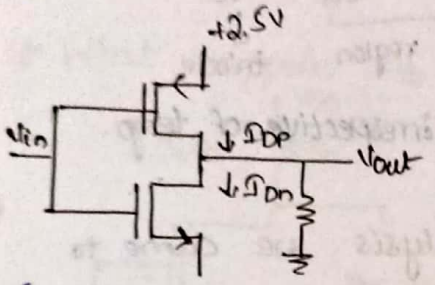
$V_{out} = 100 . V_{in}$

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* What is stable of Biasing?

If we keep our MOSFET in saturation region; By some means ie, may be does to change in temp. & changes in other parameters will change the Q. Point & Q. Point varies. But we want to bias a circuit so as to have a stable Q. Point which is irrespective of temperature, ageing etc.

5/1/22



Given

$V_{tn} = 1V$; $V_{tp} = -1V$

$\mu_n C_{ox}\left(\frac{W}{L}\right)_n = \mu_p C_{ox}\left(\frac{W}{L}\right)_p = 1mA/V^2$

find I_{DP}, I_{DN} for $V_{in} = 0V = 2.5V = -2.5V$.

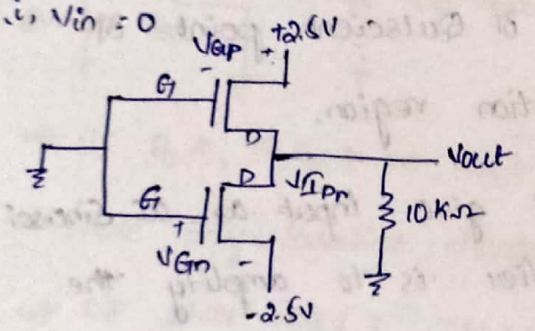
By observation:

$V_{SGP} = 2.5V$, $V_{SGn} = 2.5V$

PMOS: ON NMOS: ON

$|V_{tp}| = 1V$; $V_{tn} = 1V$

i) $V_{in} = 0$



$\mu_p C_{ox}\left(\frac{W}{L}\right)_p = 1mA/V^2$, $\mu_n C_{ox}\left(\frac{W}{L}\right)_n = 1mA/V^2$

Assume NMOS is in Sat:

$I_{DN} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GSn} - V_{tn}]^2$

$= \frac{1}{2} \times 1m \times 1.5^2$

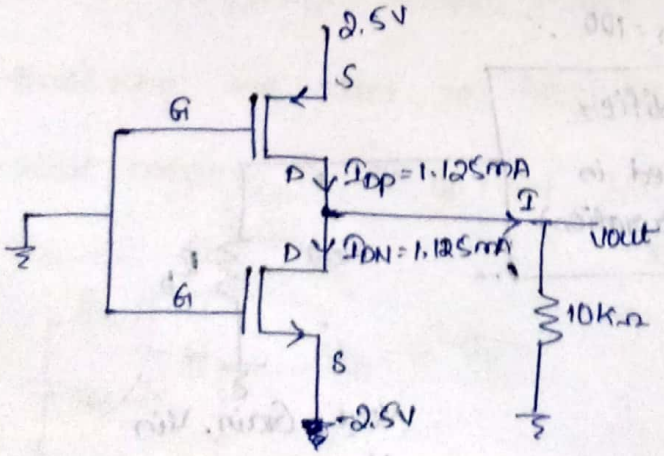
$I_{DN} = 1.125\,mA$

Assume PMOS is in Sat

$I_{DP} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_p [V_{SGp} - V_{tp}]$

$= \frac{1}{2} \times 1mA \times 1.5^2$

$I_{DP} = 1.125\,mA$



Apply KCL:

$I_{DP} = I + I_{DN}$

$I = 0$

$\Rightarrow V_{out} = I.10K\Omega$

$V_{out} = 0V$

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Drain potential of PMOS = 0V = V_{DP}

Drain potential of NMOS = 0V = V_{DN}

Check for sat:

PMOS:

Gate potential, V_{GP} = 0V

Drain potential, V_{DP} = 0V

$V_D = V_G \Rightarrow$ Saturation

Our assumptions r true.

$\therefore I_{DP} = 1.125mA = I_{DN}$

NMOS

Gate potential, V_{GN} = 0V

Drain potential, V_{DN} = 0V

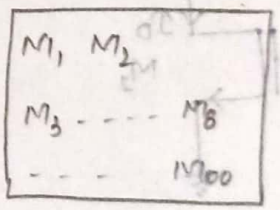
$V_D = V_G \Rightarrow$ Saturation.

Biasing Techniques:

1. Biasing by fixing V_{GS}:

Here biasing means establishing a stable operating point i.e., maintaining constant drain current irrespective of variations in temp, & etc.

In a packet of MOSFET i.e., from same manufacturer & same type



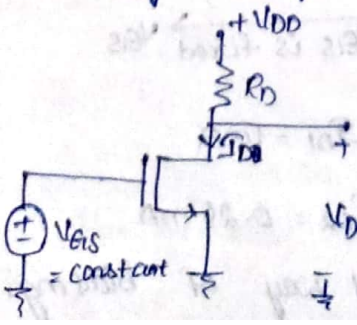
Packet
same manufacturer,
same type,
same number.

$\Rightarrow$ All MOSFET's don't have same threshold voltage V_{th}; $\left(\frac{W}{L}\right)$, & Cox

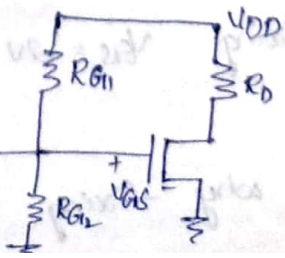
$\Rightarrow$ Further more μ_n & V_{th} are dependent on temperature.

By fixing V_{GS}:

One way: taking 2 sources: V_{DD} & V_{GS}



Otherway: by taking single source V_{DD}.



$V_G = \frac{R_{G2}}{R_{G1}+R_{G2}} \cdot V_{DD}$

$V_G = V_{GS}$

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M_1 :

$\mu_n C_{ox} = 1mA/V^2$

$V_{tn1} = 1V$ & $\left(\frac{W}{L}\right)_1 = 2$

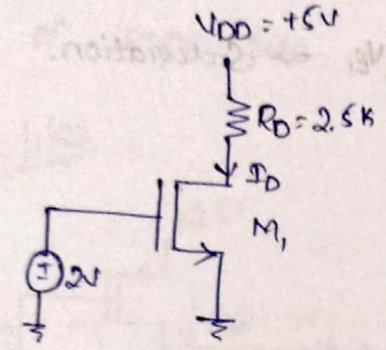
M_2 :

$\mu_n C_{ox} = 1mA/V^2$

$V_{tn2} = 1.5V$ & $\left(\frac{W}{L}\right)_2 = 2$

⇒ Here our aim is to establish an operating current of 1mA.

I have taken M_1 transister:



"V_{GS} fixed"

Assume M_1 is in saturation.

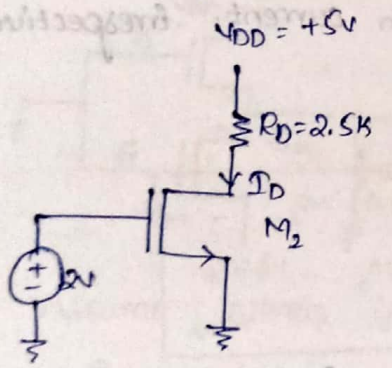
$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)[V_{GS} - V_{tn}]^2$$

$$= \frac{1}{2} \times 1m \times 2 \times 1^2$$

$$\boxed{I_D = 1mA}$$

$V_{DS} = V_{DD} - I_D R_D$

Now, inplace M_1 take M_2 transister. then,



"V_{GS} is fixed"

Assume M_2 in Saturation:

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2[V_{GS} - V_{tn}]^2$$

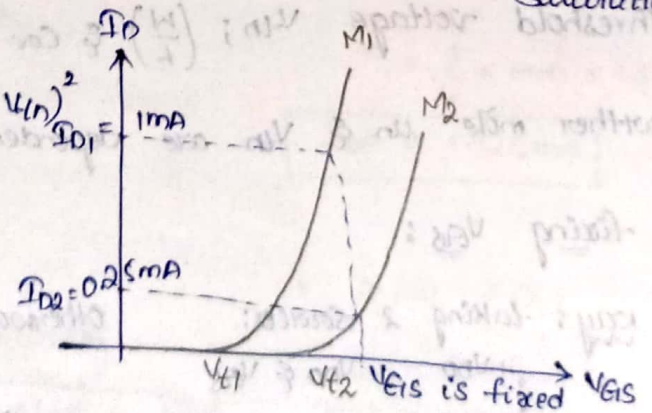
$$= \frac{1}{2} \times 1m \times 2\,[2V - 1.5V]^2$$

$$= 1m \times 0.25$$

$$\boxed{I_D = 0.25\,mA}$$

M_2 also in Saturation.

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{tn})^2$$



⇒ By fixing $V_{GS} = 2V$, M_1 has given $I_{D1} = 1mA$

M_2 has given $I_{D2} = 0.25\,mA$

⇒ That's why fixing V_{GS} is not a good way of biasing.

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$V_{GS} = 2V$

$M_1 \Rightarrow I_{D1} = 1mA$

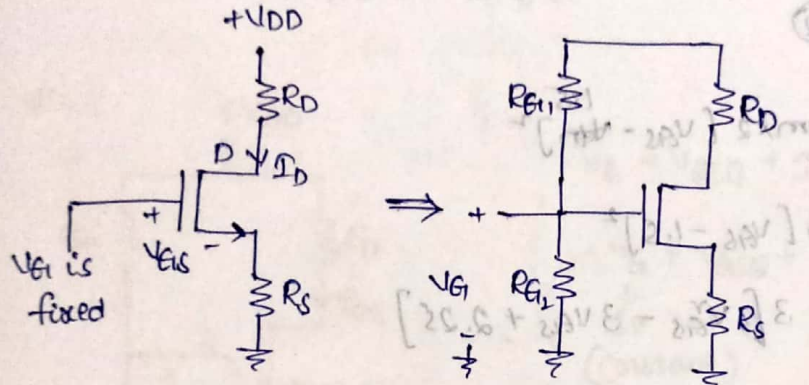
$M_2 \Rightarrow I_{D2} = 0.25mA$

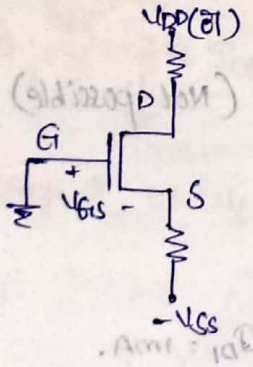
$\Rightarrow I_D$ is varying from one to one.

M_3

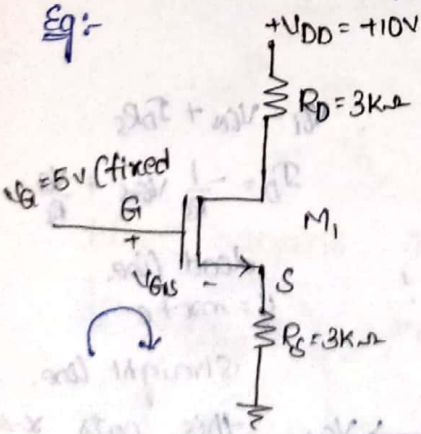
Since Q. Point is changing from device to device & also if there is a change in temp which leads to change in threshold voltage.

2. Fixing V_G & corresponding a resister R_S in series with source. (voltage divider bias)





Eg:-



M_1 : $\mu_n C_{ox} = 1mA/V^2$

$V_{t1} = 1V$ $\left(\frac{W}{L}\right)_{n1} = 2$

By doing the Analysis for finding I_D :

$V_G = V_{GS} + I_D R_S$

$5 = V_{GS} + I_D \cdot 3K$

$I_D = \frac{5V - V_{GS}}{3K} \rightarrow (1)$

$I_D = \frac{1}{2} \times 1 \times 2 \times [V_{GS} - 1]^2 \rightarrow (2)$

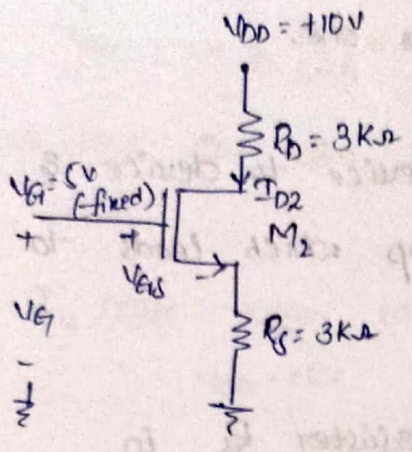
① & ②

After solving we get

$I_D = 1mA.$

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For the same



M_2 : $\mu_n C_{ox} = 1 mA/V^2$,

$V_{tn} = 1.5V$, $\left(\frac{W}{L}\right)_2 = 2$

Assume M_2 is in sat:

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{tn})^2 \longrightarrow (1)$$

$$V_G = V_{GS} + I_{D2}R_S$$

$$I_{D2} = \frac{5V - V_{GS}}{3K\Omega} \longrightarrow (2)$$

Solving (1) & (2)

$$\frac{5V - V_{GS}}{3K} = \frac{1}{2} \times 1m \times 2 \left[V_{GS} - 1.5\right]^2$$

$$5V - V_{GS} = 3\left[V_{GS} - 1.5\right]^2$$

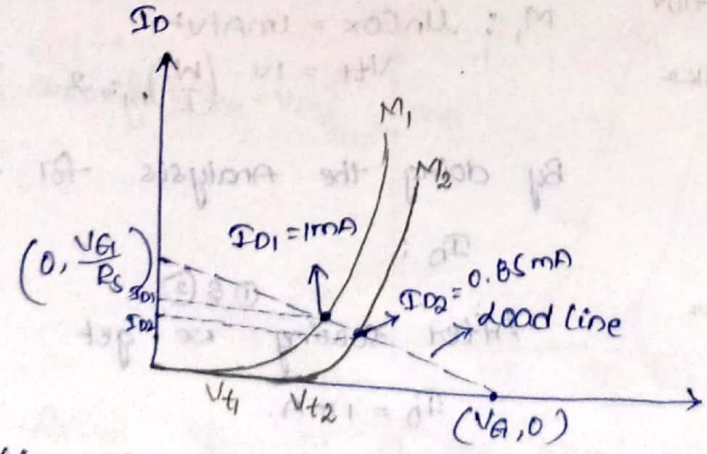
$$5V - V_{GS} = 3\left[V_{GS}^2 - 3V_{GS} + 2.25\right]$$

$$3V_{GS}^2 - 8V_{GS} + 1.75 = 0$$

$V_{GS} = 2.43V$ & $0.2VV$ (Not possible)

$$I_{D2} = \frac{5V - 2.43V}{3K\Omega}$$

$$\boxed{I_{D2} = 0.85\,mA}$$ nearer to $I_{D1} = 1mA$.



$V_G = V_{GS} + I_D R_S$

$I_D = -\frac{1}{R_S} V_{GS} + \frac{V_G}{R_S}$

Load line.

$y = mx + c$

Straight line.

this cuts x-axis at ($y = 0$ put)

$\Rightarrow V_{GS} = V_G$

cuts y axis at ($x = 0$)

ie, $V_{GS} = 0$ $\boxed{I_D = \frac{V_G}{R_S}}$

∴ this brings biasing technique gives a stable Q. point compared to biasing using constant V_{GS}.

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⇒ The nearer for this stability in this biasing techq. is because of the presence of R_S. Here R_S gives negative feedback.

* What has happened actually?

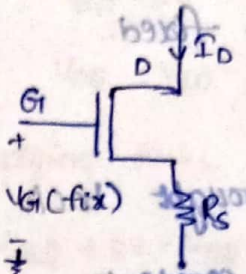
$V_G = V_{GS} + I_D R_S$

By some means

$5 = V_{GS} + I_D\ 3k\Omega$

V_t has increased i.e., from 1V to 1.5V

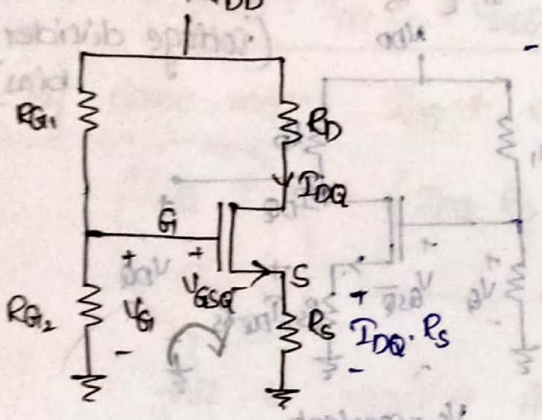
$\Rightarrow V_t \uparrow \Rightarrow I_D \downarrow \Rightarrow I_D R_S \downarrow$



$\therefore V_G$ is fixed

$5 = V_{GS} + (I_D R_S)\downarrow$

*



$-V_G + V_{GSQ} + I_{DQ} \cdot R_S = 0$

$V_G = V_{GSQ} + I_{DQ} R_S$

V_G ↓ 5V (constant)

If temp ↑ $\Rightarrow V_t \uparrow \Rightarrow$ $I_{DQ}\downarrow$ $\Rightarrow (I_{DQ} \cdot R_S)\downarrow \Rightarrow V_{GSQ}\uparrow$

$I_{DQ}\uparrow$

this is negative feedback action.

negative feedback is provided by R_S.

What happens if $I_{DQ} \uparrow$ by some means?

$I_{DQ}\uparrow \Rightarrow (I_{DQ} \cdot R_S)\uparrow \Rightarrow V_{GSQ}\downarrow$

$I_{DQ}\downarrow$

this is negative feedback action because of R_S.

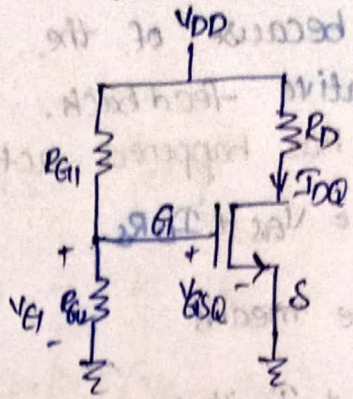
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By some means I_{DQ} ↓ then what happens

- $V_G + V_{GS} = 0$

$V_{GSQ} = V_G = 2V$ (constant)

$V_{GSQ} = 2V \Rightarrow$ fixed.



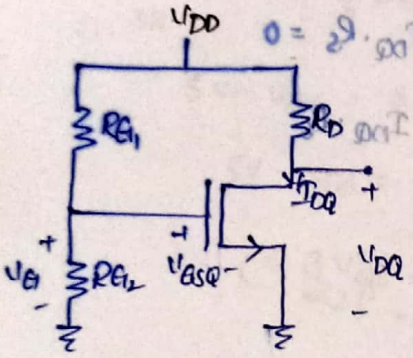
Here if I_{DQ} ↓,

it can't be brought back to provided value

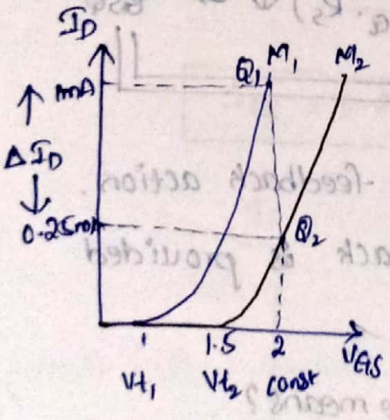
Since V_{GSQ} = constant

∴ No negative feedback is present.

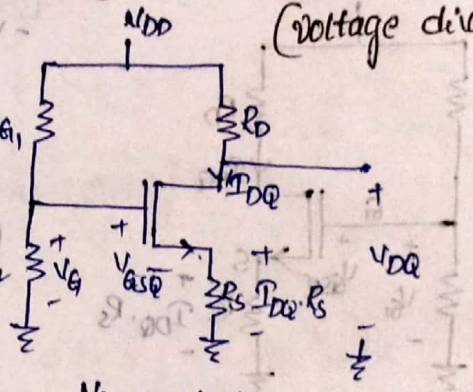
Biasing using constant V_{GS}



$V_G = V_{GSQ}$ = constant = 2V



Biasing using a constant V_G & R_S in series with Source. (voltage divider bias)

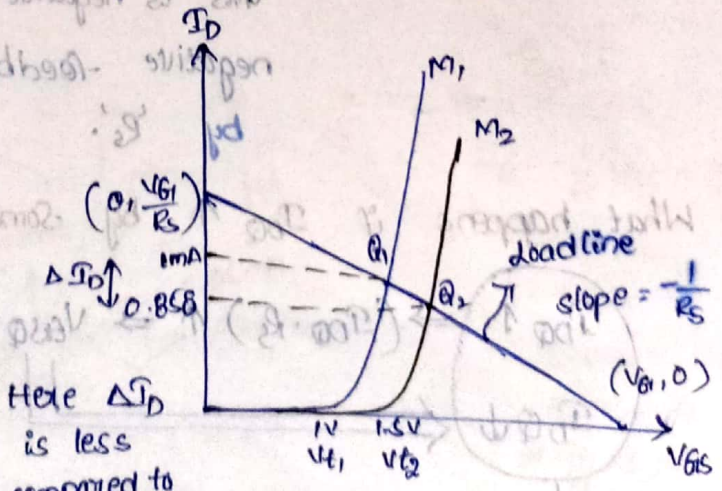


V_G = constant

Apply KVL: $V_G = V_{GSQ} + I_{DQ} \cdot R_S$

Load line $I_{DQ} = -\frac{1}{R_S} V_{GSQ} + \frac{V_G}{R_S}$

$y = mx + c$



Here ΔI_D is less compared to biasing using constant V_{GS}

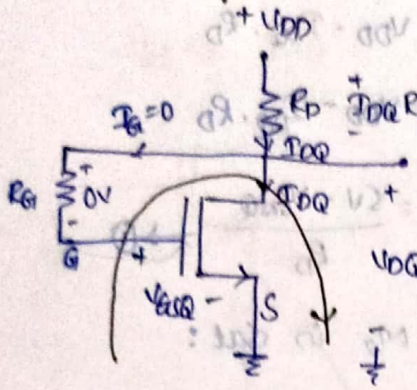
$V_G = 5V$

$V_G / R_S = \frac{5}{3}$ mA

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25/1/22

3. Biasing Using Drain to Gate feedback resistor.



By observation

$V_{GD} = 0V$

$V_{DQ} = V_{DD} - I_{DQ} R_D \rightarrow (1)$

Applying KVL,

$-V_{GSQ} + 0V + V_{DQ} = 0$

$\Rightarrow V_{GSQ} = V_{DQ}$.

$\Rightarrow$ Rewriting above Eq. (1)

$V_{DD} = I_{DQ} R_D + V_{DQ}$

$$\boxed{V_{DD} = I_{DQ} R_D + V_{GSQ}}$$

By some means $I_{DQ} \uparrow$ what happens?

$I_{DQ} \uparrow \Rightarrow (I_{DQ} \cdot R_D) \uparrow \Rightarrow V_{GSQ} \downarrow$

$I_{DQ} \downarrow$

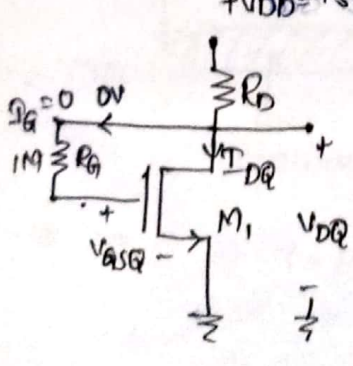
this is negative feedback action

negative feedback is given by feedback resistor 'R_G'

$\Rightarrow$ Typically we take R_G in Mega Ohms

$\Rightarrow$ Drawback in this biasing technique is reduced voltage savings since $V_{GD} = 0V$.

Explanation :-

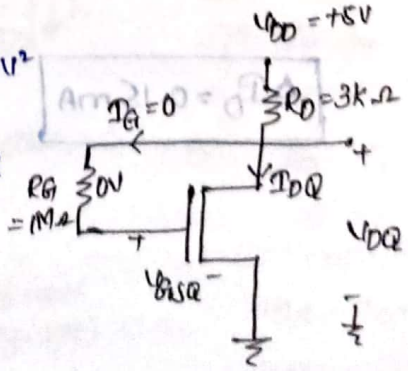


$\mu_n C_{ox} = 1\ mA/V^2$

$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 2$

$V_{t1} = 1V$

$V_{t2} = 1.5V$



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By Observation

$V_{GSQ} = V_{DQ}$

$V_{DQ} = V_{DD} - I_{DQ} \cdot R_D$

$I_{DQ} = \dfrac{5V - V_{GSQ}}{R_D} \rightarrow (1)$

Assume M_1 in sat:

$I_{DQ} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{GSQ} - V_t)^2 \rightarrow (2)$

from (1) & (2)

$\dfrac{5 - V_{GSQ}}{3K} = \frac{1}{2} \times 1m \times 2 [V_{GSQ} - 1]^2$

$5V - V_{GSQ} = 3 [V_{GSQ}^2 - 2V_{GSQ} + 1]$

$3V_{GSQ}^2 - 5V_{GSQ} - 2 = 0$

$V_{GSQ} = 2V \;\&\; -\frac{1}{3}V$

✓ ×

$I_{DQ} = \dfrac{5V - V_{GSQ}}{3K\Omega}$

$= \dfrac{5V - 2V}{3K\Omega}$

$I_{DQ} = 1mA$

$V_{GD} = 0$

$\Rightarrow V_D = V_G$

$\Rightarrow$ Indeed 'sat'.

By Observation

$V_{GSQ} = V_{DQ}$

$V_{DQ} = V_{DD} - I_{DQ} \cdot R_D$

$V_{GSQ} = V_{DD} - I_{DQ} \cdot R_D$

$I_{DQ} = \dfrac{5V - V_{GSQ}}{R_D} \rightarrow (1)$

Assume M_2 in sat:

$I_{DQ} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_2 (V_{GSQ} - V_{tn})^2 \rightarrow (2)$

from (1) & (2)

$\dfrac{5V - V_{GSQ}}{3K} = \frac{1}{2} 1m \times 2 \cdot [V_{GSQ} - 1.5]^2$

$5V - V_{GSQ} = 3 [V_{GSQ}^2 - 3V_{GSQ} + 2.25]$

$3V_{GSQ}^2 - 8V_{GSQ} + 1.75 = 0$

$V_{GSQ} = 2.43V \;\&\; 0.24V$

✓ ×

$I_{DQ} = \dfrac{5V - 2.43V}{3K\Omega}$

$\approx 0.85mA$

$V_{GD} = 0$

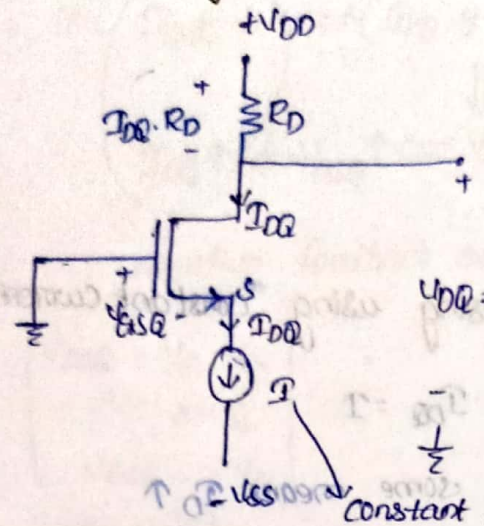
$\Rightarrow V_D = V_G$

$\Rightarrow$ Indeed sat.

$\boxed{\Delta I_D = 0.15mA}$

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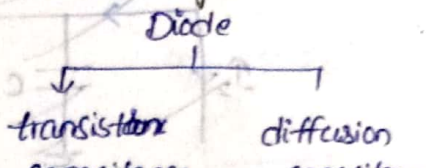
4. Biasing Using Constant Current Source



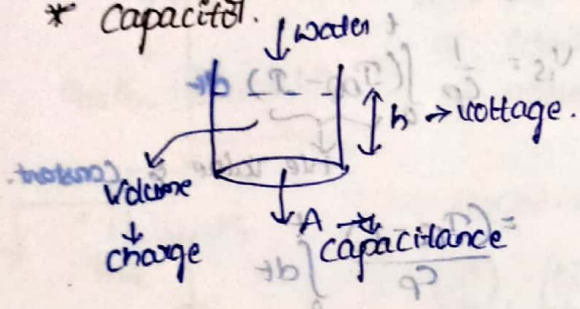
$V_{DQ} = V_{DD} - I_{DQ} \cdot R_D$

(parasitic capacitance)

* Diode capacitance.



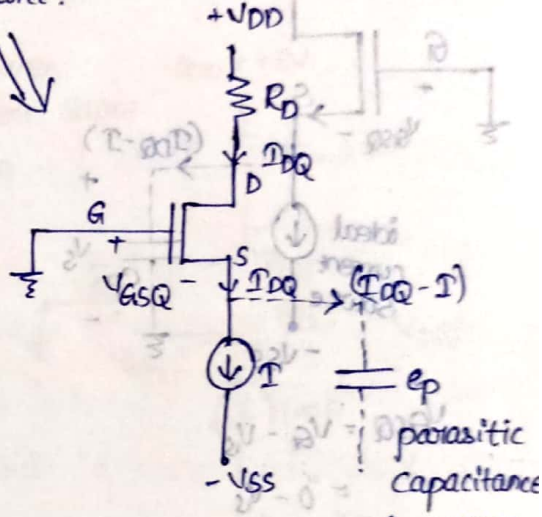
* Capacitor.



Area of cross section → capacitance 'C'

height → voltage 'V'

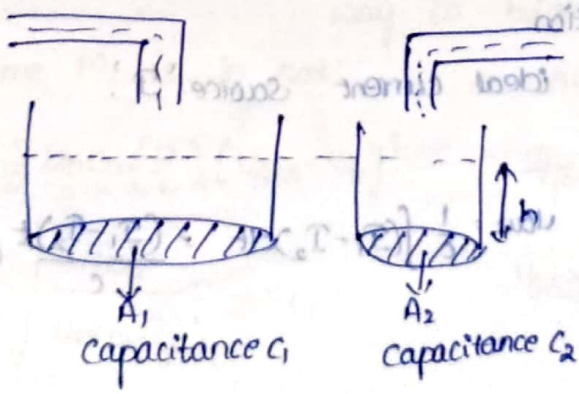
Volume → charge 'Q'.



In Cylinder:

Volume = A × h

$Q = C \cdot V \Rightarrow C = \frac{Q}{V}$



Rate of flow is same in both cylinders. which will take more time to fill height 'h' in both cylinders.

Ans C_1 $[\because C_1 > C_2]$

* $C \uparrow \Rightarrow \tau = RC \uparrow$

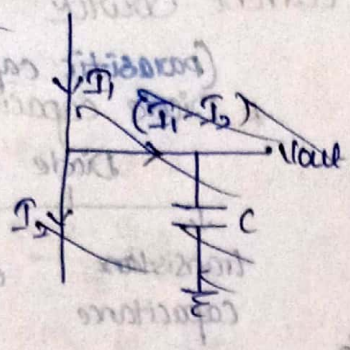
time constant $\Rightarrow$ Speed $\downarrow$

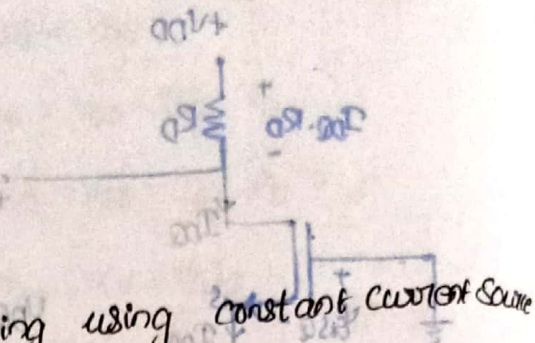
time $\Rightarrow 5\tau \uparrow$ (taken to reach study state)

* If capacitance is more then speed is less.

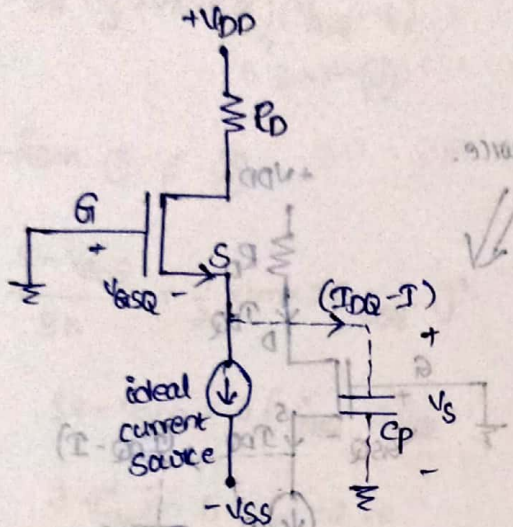
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Note:-





What happens if I_{DQ} ↑ in biasing using constant current source



$V_{GSQ} = V_G - V_S$

$= 0 - V_S$

$V_{GSQ} = -V_S$

Initially $I_{DQ} = I$

but by some means I_D ↑

$\Rightarrow I_{DQ} - I > 0$

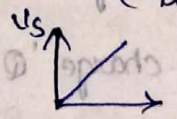
$\Rightarrow V_S = \frac{1}{C_P}\int_0^t (I_{DQ} - I)\,dt$

(+ve value & constant.)

$= \frac{(I_{DQ} - I)}{C_P}\int_0^t dt$

$V_S = \frac{I_{DQ} - I}{C_P}\,t$; as t ↑ $\Rightarrow V_S$ ↑

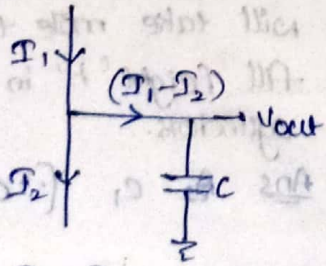
$\therefore$ If I_{DQ} ↑ $\Rightarrow (I_{DQ} - I)$ ↑ $\Rightarrow V_S$ ↑



* If I_{DQ} ↑ $\Rightarrow V_S$ ↑ $\Rightarrow V_{GSQ}$ ↓ $\Rightarrow I_{DQ}$ ↓

this is negative feedback action provided by the ideal current source 'I'.

Note:-



$V_{out} = \frac{1}{C}\int (I_1 - I_2)\,dt = \frac{(I_1 - I_2)t}{C}$ (ramp)

i, if $I_1 > I_2$ $\Rightarrow (I_1 - I_2) > 0$ $\Rightarrow V_{out}$ ↑

ii, if $I_1 < I_2$ $\Rightarrow I_1 - I_2 < 0$ $\Rightarrow V_{out}$ ↓

iii, if $I_1 = I_2$ $\Rightarrow I_1 - I_2 = 0$ $\Rightarrow V_{out}$ remains Constant.

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* What happens if I_{DQ} ↓ in previous example.

if I_{DQ} ↓ $\Rightarrow (I_{DQ} - I)$ ↓

$\Downarrow$

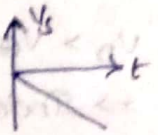
I_{DQ} ↑ $\Leftarrow V_{GSQ}$ ↑ $\Leftarrow V_S$ ↓

↓

negative feedback action

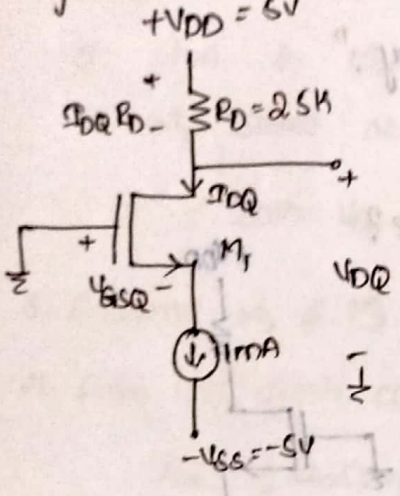
$$V_S = \frac{I_{DQ} - I}{C_p} t$$

$I_{DQ} - I < 0$



$$\begin{bmatrix} V_{GSQ} = V_G - V_S \\ 0 - V_S \\ V_{GSQ} = -V_S \end{bmatrix}$$

Explaination:-



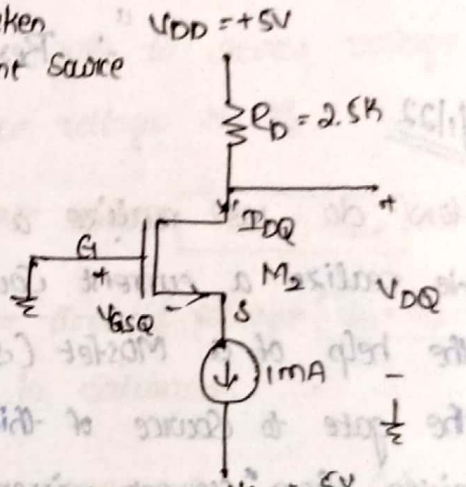
Here we have taken an ideal current source of value 1mA

$\mu_n C_{ox} = 1mA/V^2$

$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 2$

$V_{t1} = 1V$;

$V_{t2} = 1.5V$



By observation:

$I_{DQ} = 1mA$

By observation:

$I_{DQ} = 1mA$

$\Delta I_D = 0$

∴ that's why this technique is best way in biasing techniques.

Assume M_1 is in sat:

$$I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 [V_{GSQ} - V_{t1}]^2$$

$$V_{GSQ} = \sqrt{\frac{2I_{DQ}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{t1}$$

$$= \sqrt{\frac{2 \times 1mA}{1m \times 2}} + 1V$$

$V_{GSQ} = 2V$ & $V_G = 0$

Assume M_2 is in sat:

$$I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 [V_{GSQ} - V_{t2}]^2$$

$$V_{GSQ} = \sqrt{\frac{2I_{DQ}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_2}} + V_{t2}$$

$$= \sqrt{\frac{2 \times 1mA}{1mA \times 2}} + 1.5V$$

$V_{GSQ} = 2.5V$ & $V_G = 0$

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$V_{DQ} = V_{DD} - I_{DQ} \cdot R_D$

$= 5V - 1m(2.5K\Omega)$

$V_{DQ} = 2.5V$

$\therefore V_D > V_G$

$\Rightarrow$ Indeed Saturation

$Q(V_{DQ}, I_{DQ}) = (2.5V, 1mA)$

$V_{DQ} = V_{DD} - I_D R_D$

$= 5V - 1m(2.5K\Omega)$

$V_{DQ} = 2.5V$

$\therefore V_D > V_G$

$\Rightarrow$ Indeed saturation.

$Q(V_{DQ}, I_{DQ}) = (2.5V, 1mA)$

$\Rightarrow$ Here Q Point is very much ~~State~~ Stable

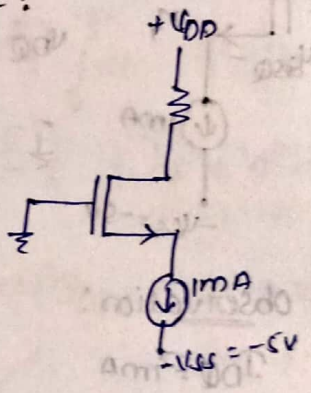
"$\therefore$ Best Biasing way."

26/1/22

How do we realize a current source?

We realize a current source with the help of a Mosfet (saturation region) the gate to source of this Mosfet is given from "current mirror circuit."

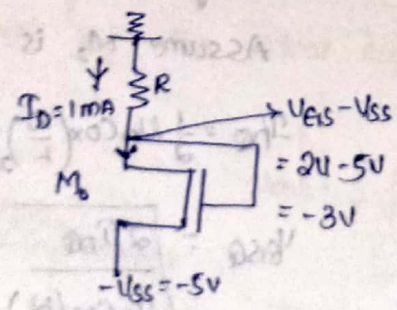
threshold voltage of all transistors is same $V_t = 1V$

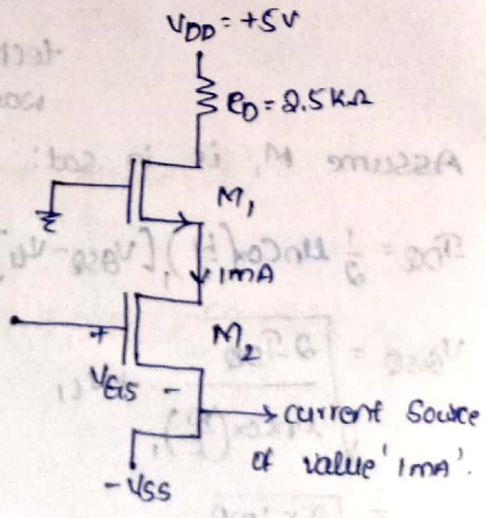


M_0:

$\mu_n C_{ox} = 1mA/V^2$

$\left(\frac{W}{L}\right)_0 = 2$, $V_{t0} = V_{t1} = V_{t2} = 1V$





By observation:

$I_D = 1mA$ & $V_{GD} = 0$, $V_D = V_G$ (diode connected) (Sat)

for $I_D = 1mA$, $V_{GS} = ?$

$I_D = \frac{0 - (-3)}{R} \Rightarrow R = \frac{3}{1m} = 1K\Omega$

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$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_0 (V_{GS} - V_{tn})^2$$

$$V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_0}} + V_{to}$$

$$= \sqrt{\frac{2\times 1m}{1m\times 2}} + 1V = 2V$$

$R = 3K\Omega$

If we keep the value $R = 3K\Omega$ then the current flowing through M_0 is 1mA.

In order to realize a current source of value 1mA using Mosfet M_2.

1. We have to operate M_2 in saturation region.
2. Since we have already generated a reference current of 1mA in M_0, then give the gate to source voltage of M_0 same as gate to source voltage of M_2.

$\therefore$ Both V_{GS} of M_0 & M_2 are same $\boxed{V_{GS0} = V_{GS2}}$

3. Assume M_0 & M_2 are having same threshold voltage $\boxed{V_{t0} = V_{t2} = V_t}$
4. From the drain current expression in saturation

$$I_{D0} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_0 (V_{GS0} - V_{t0})^2$$ current through M_0 (drain)

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{t2})^2$$ current through M_2 (drain)

as $V_{GS0} - V_{t0} = V_{GS2} - V_{t2}$ & $\mu_n C_{ox}$ is same

$$\Rightarrow \frac{I_{D2}}{I_{D0}} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_0}$$

M_0 always sate region diode connected.

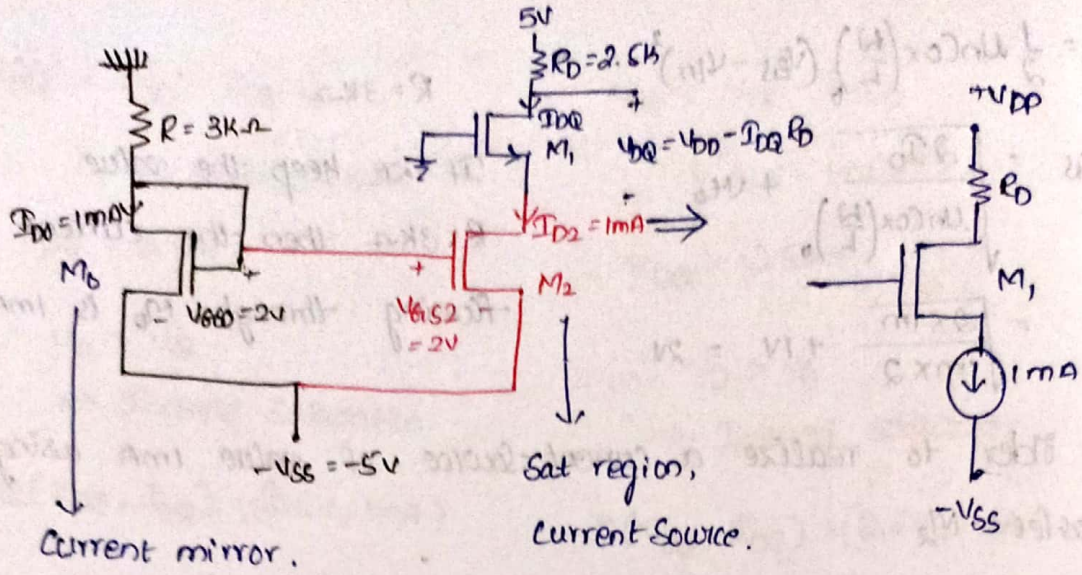
$$\boxed{I_{D2} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} I_{D0}}$$

We want $I_{D2} = 1mA$, given $I_{D0} = 1mA$

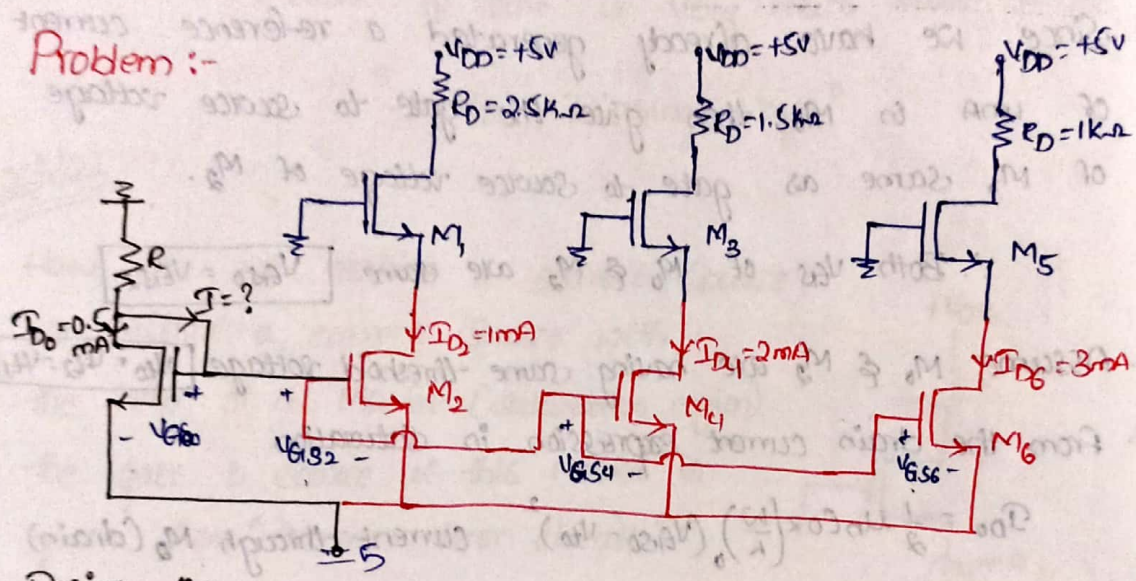
$$1mA = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_0} \cdot 1mA \Rightarrow \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_0$$

$$\Rightarrow \boxed{\left(\frac{W}{L}\right)_2 = 2}$$

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Problem :-



Design the current mirror circuit and find $\left(\frac{W}{L}\right)_2, \left(\frac{W}{L}\right)_4, \left(\frac{W}{L}\right)_6$.
Given $\mu_n C_{ox} = 1mA/V^2$ is constant for all Mosfets. threshold voltage $V_t = 1V$ for all Mosfets.

Sol: Designing means choosing the proper values of components so as to meet the designed specification.

ie., we need to find the values of R & $\left(\frac{W}{L}\right)_0$ for having $I_{D0} = 0.5mA$; this I_{D0} has to be mirred in M_2, M_4 & M_6. (therefore we have to find the corresp) as 1mA, 2mA, 3mA respectively. for this to happen, we have to find the corresponding values of & $\left(\frac{W}{L}\right)_2, \left(\frac{W}{L}\right)_4, \left(\frac{W}{L}\right)_6$.

By Observation :- $I = I_{G0} + I_{G2} + I_{G4} + I_{G6}$

$V_{GS0} = V_{GS2} = V_{GS4} = V_{GS6}$; $V_t = V_{t1}, V_{t2} \cdots V_{t6} = 1V$

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Since M_0 is carrying a drain current $I_{D0} = 0.5\,mA$ & $V_D = V_G \Rightarrow M_0$ is in saturation region.

Assume $\left(\frac{W}{L}\right)_0 = 2$

In sat :-

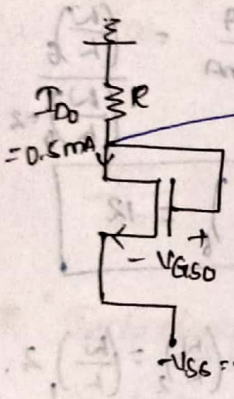
$$I_{D0} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_0 (V_{GS0} - V_{t0})^2$$

$$V_{GS0} = \sqrt{\frac{2I_{D0}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_0}} + V_{t0} = \sqrt{\frac{2\times 0.5m}{1m\times 2}} + 1V$$

$$= 0.707 + 1V$$

$$V_{GS0} = 1.707\,V$$

$$\therefore V_{GS0} = V_{GS2} = V_{GS4} = V_{GS6} = 1.707\,V$$



Now, $I_{D0} = \frac{0V - (-3.293V)}{R}$

$$R = \frac{+3.293V}{0.5\,mA}$$

$$R = 6.586\,k\Omega$$

⇒ Since all the gate terminals of MOSFET's don't know any gate current i.e., Gate current = 0

$\Rightarrow I = 0$

$$I_{G0} = I_{G2} = I_{G4} = I_{G6} = 0$$

⇒ By taking $R = 6.586\,k\Omega$ & $\left(\frac{W}{L}\right)_0 = 2$; we have generated a reference current in M_0. ($I_{D0} = 0.5\,mA$)

Now this I_{D0} will mirror this currents in M_2, M_4 & M_6.

Given

$I_{D0} = 0.5\,mA$; $I_{D2} = 1mA$; $I_{D4} = 2mA$; $I_{D6} = 3mA$

Assuming M_2, M_4 & M_6 are in saturation region:-

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In sat :-

$$I_{D0} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_0 (V_{GS0} - V_{t0})^2$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{t2})^2$$

$$I_{D4} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_4 (V_{GS4} - V_{t4})^2$$

$$I_{D6} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_6 (V_{GS6} - V_{t6})^2$$

V_{GS} & V_t is same for M_0, M_2, M_4 & M_6

$$\frac{I_{D2}}{I_{D0}} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_0}$$

$$\frac{1mA}{0.5mA} = \frac{\left(\frac{W}{L}\right)_2}{2}$$

$$\boxed{\left(\frac{W}{L}\right)_2 = 4}$$

$$\frac{I_{D4}}{I_{D0}} = \frac{\left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_0}$$

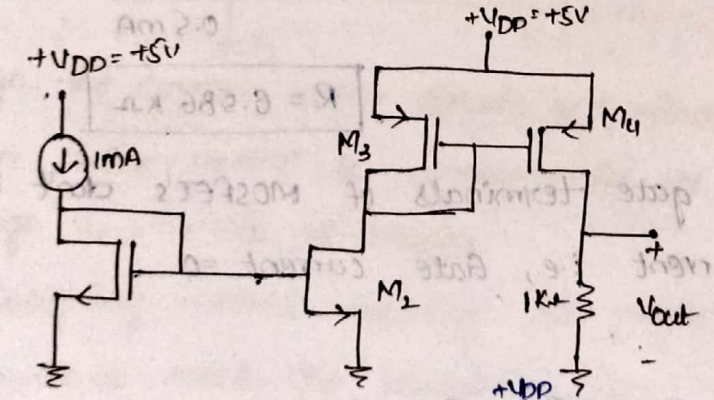
$$\frac{2mA}{0.5mA} = \frac{\left(\frac{W}{L}\right)_4}{2}$$

$$\boxed{\left(\frac{W}{L}\right)_4 = 8}$$

$$\frac{I_{D6}}{I_{D0}} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_0}$$

$$\frac{3mA}{0.5mA} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_0 = 2}$$

$$\boxed{\left(\frac{W}{L}\right)_6 = 12}$$



$\lambda = 0$; $\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_1 2$.

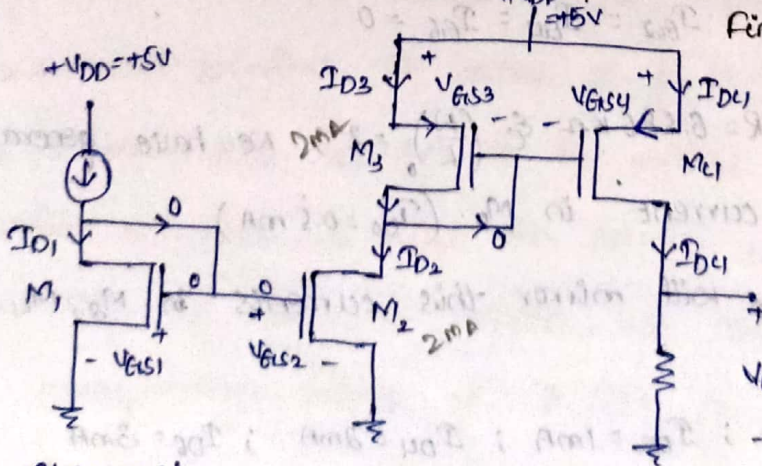
$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4$

$V_{tn} = 1V$, $V_{tp} = -1V$

$\mu_n C_{ox} = 1mA$, $\mu_p C_{ox} = 0.5m$

All MOSfets are in sat

Find V_{out} ?



By Observation:

$V_{GS1} = V_{GS2}$ — M_1 & M_2 are NMOS

$V_{GS3} = V_{GS4}$ — M_3 & M_4 are PMOS

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$I_{D1} = 1mA$, $I_{D3} = I_{D2}$

$V_{out} = I_{D4} \cdot R$

Given, $\left(\frac{W}{L}\right)_2 = 2.\left(\frac{W}{L}\right)_1 \Rightarrow \frac{I_{D2}}{I_{D1}} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}$

$\left(\because \text{all are in sat}\right) \Rightarrow I_{D2} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} \times I_{D1} = \frac{2}{1} \times 1mA = 2mA$

$\boxed{I_{D2} = 2mA}$

$\Rightarrow I_{D3} = I_{D2} = 2mA.$

M_3 will mirror I_{D3} in M_4 as I_{D4}

$V_{GS3} = V_{SG4}$; $|V_{tp3}| = |V_{tp4}|$

$\frac{I_{D4}}{I_{D3}} = \frac{\left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_3}$

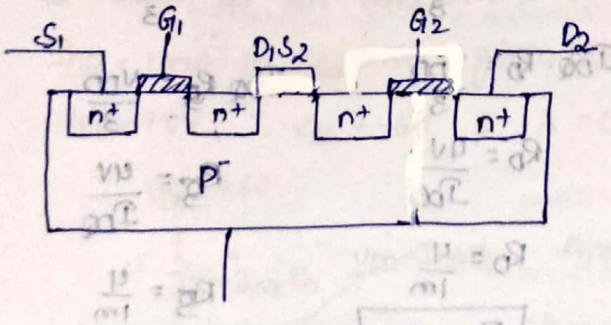
$I_{D4} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_4 [V_{SG4P4} - |V_{tp4}|]^2$

$I_{D3} = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_3 [V_{SG4P3} - |V_{tp3}|]^2$

$\frac{I_{D4}}{2mA} = 1 \Rightarrow \boxed{I_{D4} = 2mA}$

* "Technology" means :-

We have designed an IC (integrated circuit) in 0.18 μm technology.



NMOS & PMOS which is fabricated in this technology will be having a

$L_{min} = 0.18 \mu m$ (minimum channel length)

↓

180 nm.

180 nm ⟶ L = 90 nm (not possible) L = 250 nm L = 1 μm

technology possible possible

90 nm ⟶ L = 135 nm L = 65 nm L = 32 nm

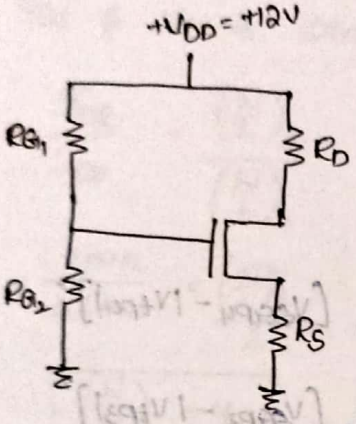
technology ✓ ✗ ✗

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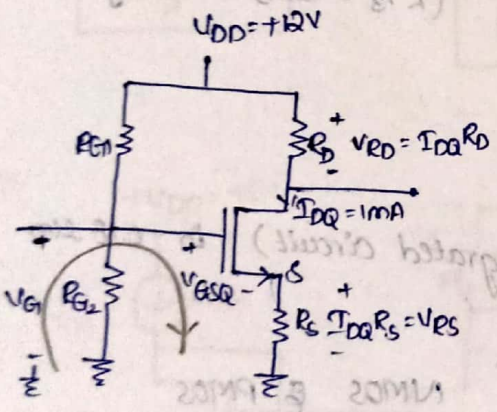
27/1/22

* for current mirroring we should take same type (NMOS or PMOS)
* for diff Mosfets like NMOS & PMOS we can't do mirroring.

Q. Design a voltage divider bias ckt as shown in fig (which is used as an amplifier) such that bias current $I_{DQ}=1mA$ given $\mu_n C_{ox} = 1mA/V^2$, $V_{tn}=1V$; $\left(\frac{W}{L}\right)_n = 2$ & $V_{DD}=12V$



Sol:- Here design means finding appropriate values of components R_D, R_S, R_{G1} & R_{G2} & R_{G2} such that bias current $I_D = 1mA$.



As a rule a thumb:

Voltage across R_D = $V_{RD} = I_{DQ} R_D$

Voltage across R_S = $V_{RS} = I_{DQ} \cdot R_S$

$V_{RD} = V_{RS} = \frac{V_{DD}}{3} = 4V$

$\Rightarrow V_{RD} = \frac{V_{DD}}{3}$ $\Rightarrow V_{RS} = \frac{V_{DD}}{3}$

$I_{DQ} \cdot R_D = \frac{V_{DD}}{3}$ $I_{DQ} \cdot R_S = \frac{V_{DD}}{3}$

$R_D = \frac{4V}{I_{DQ}}$ $R_S = \frac{4V}{I_{DQ}}$

$R_D = \frac{4}{1m}$ $R_S = \frac{4}{1m}$

$R_D = 4K\Omega$ $R_S = 4K\Omega$

Now,

Apply KVL:

$-V_G + V_{GSQ} + I_{DQ} \cdot R_S = 0$

$V_G = V_{GSQ} + 4V$ → (1)

$V_G = \frac{R_{G2}}{R_{G1}+R_{G2}} V_{DD}$ → (2)

In saturation region

$I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSQ} - V_{tn})^2 \Rightarrow V_{GSQ} = \sqrt{\frac{2I_{DQ}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n}} + V_{tn}$

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$$V_{GSQ} = \sqrt{\frac{2 \times 1m}{1m \times 2}} + 1V = 2V \Rightarrow \boxed{V_{GSQ} = 2V}$$

from ① $\Rightarrow V_G = V_{GSQ} + 4V$

$\Rightarrow V_G = 2V + 4V = 6V \Rightarrow \boxed{V_G = 6V}$

from ⑤ $\Rightarrow V_G = \frac{R_{G2}}{R_{G1}+R_{G2}} V_{DD}$

$$6V = \frac{R_{G2}}{R_{G1}+R_{G2}} \times 12V$$

$$R_{G1} + R_{G2} = 2R_{G2} \Rightarrow \boxed{R_{G1} = R_{G2}}$$

Let $R_{G1} = 1M\Omega$, $R_{G2} = 1M\Omega$

Typically we take values of R_{G1} & R_{G2} in Mega ohms for having high input resistances.

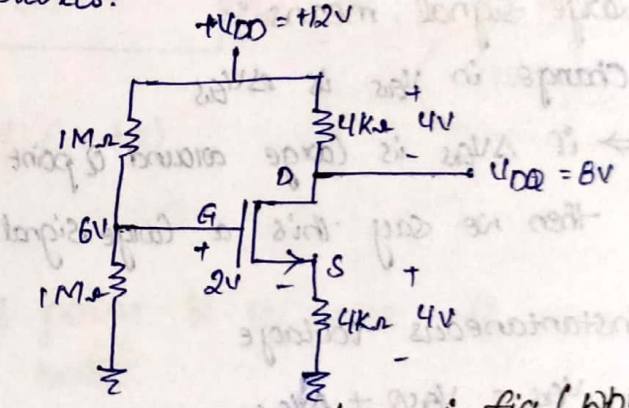
Final design values

$R_{G1} = 1M\Omega$

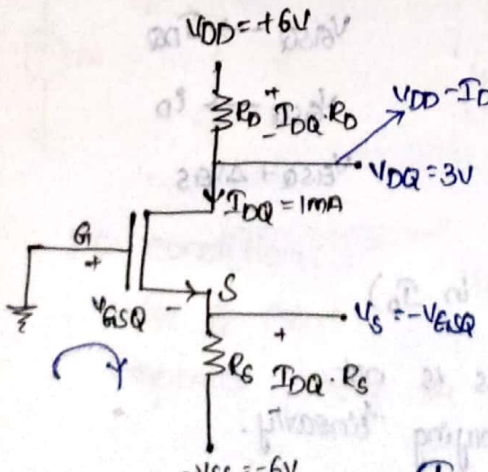
$R_{G2} = 1M\Omega$

$R_D = 4K\Omega$

$R_S = 4K\Omega$



Q. Design a dual supply biasing circuit as shown in fig (which is used as an amplifier) in order to establish a bias current $I_{DQ} = 1mA$ & $V_{DQ} = 3V$. given $\mu_n C_{ox} = 1mA/V^2$, $V_{tn} = 1V$, $\left(\frac{W}{L}\right)_n = 2$, $V_{DD} = +6V$, $-V_{SS} = -6V$ & $\lambda = 0$



Applying KVL,

$V_{GSQ} + I_{DQ}R_S - V_{SS} = 0$

$2V + 1mA \cdot R_S - 6 = 0$

$1mA R_S = 4V$

$\Rightarrow \boxed{4K\Omega = R_S}$

$$R_S = \frac{V_S - (-V_{SS})}{I_{DQ}}$$

$$= \frac{-2V + 6V}{1mA}$$

$\boxed{R_S = 4K\Omega}$

In Sat :-

$$I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GSQ} - V_{tn}]^2$$

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$$V_{GSQ} = \sqrt{\frac{2 I_{DQ}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n}} + V_{tn}$$

$$= \sqrt{\frac{2 \times 1m}{1m \times 2}} + 1V$$

$$\boxed{V_{GSQ} = 2V}$$

$V_{DQ} = 3V$

$V_{DD} - I_{DQ} R_D = 3V$

$$R_D = \frac{V_{DD} - 3V}{I_{DQ}} = \frac{6V - 3V}{1mA} = 3K\Omega \Rightarrow \boxed{R_D = 3K\Omega}$$

Large signal Expression in saturation:-

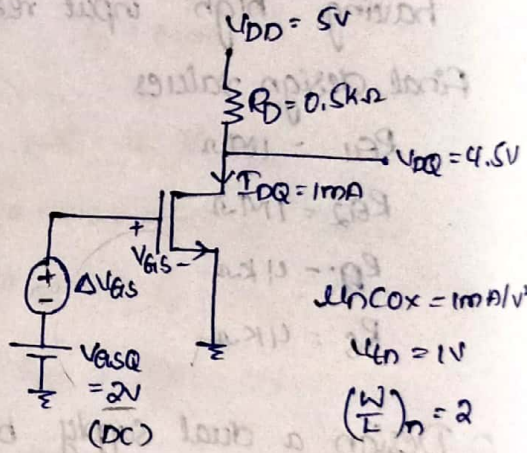
$$I_{DQ} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n [V_{GSQ} - V_{tn}]^2$$

⇒ Large signal expression is non-linear (∵ square term)

Large signal means :-

Change in V_{GS} is ΔV_{GS}

⇒ if ΔV_{GS} is large around Q point then we say this a large signal.



instantaneous voltage v_{gs}

$V_{GS} = V_{GSQ} + \Delta V_{GS}$

ΔV_{GS}	V_{GS} ($V_{GSQ}+$)	$i_D = I_{DQ} + \Delta I_D$ (instantaneous drain current $= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS} - V_{tn})^2$
0V	2V	1mA
200mV (0.2V)	2.2V	1.44mA ; $\Delta I_D = 0.44mA$
400mV (0.4V)	2.4V	1.96mA ; $\Delta I_D = 0.96mA$
600mV (0.6V)	2.6V	2.56mA ; $\Delta I_D = 1.56mA$

$V_{GSQ} \rightarrow I_{DQ}$

$V_{GSQ} \rightarrow i_D$

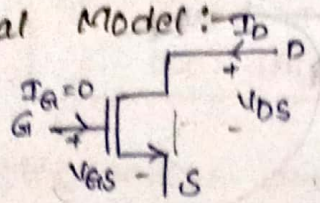
$V_{GSQ} + \Delta V_{GS}$

(Change in V_{GS}) ΔV_{GS}		ΔI_D (change in I_D)	
Linear signal	200mV	0.44mA	This is not varying linearly.
	400mV	0.96mA	
	600mV	1.56mA	

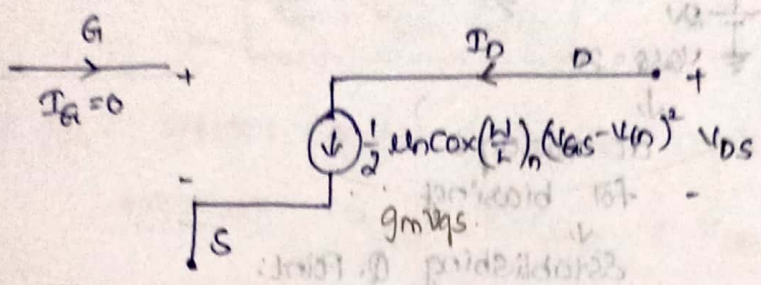
⇒ Large signal model is Non-linear.

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*Large signal model is an Exact model.

Large Signal Model:- 

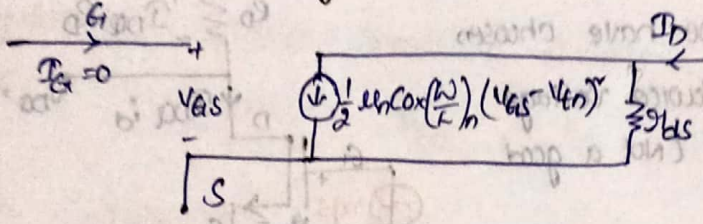
⇒ Modelled as below



Large Signal Model for $\lambda = 0$

$\lambda = 0$
No channel length modulation
$g_{ds} = \frac{1}{\lambda I_D} = \infty$

for $\lambda \neq 0$ considering channel length modulation.

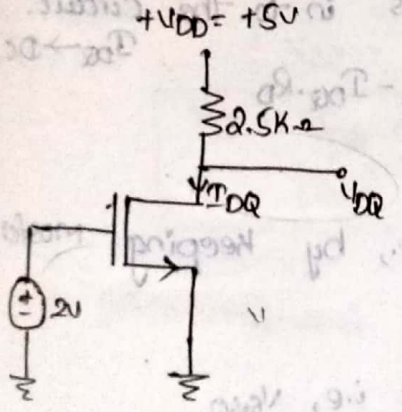


Large signal model ($\lambda \neq 0$)

$\lambda \neq 0$
$g_{ds} = \frac{1}{\lambda I_D}$

31/1/22

*What is the operating point or Q. point for the biasing ckt as shown below.



Given:

$\mu_n C_{ox} = 1mA/V^2$

$V_{th} = 1V$

$\left(\frac{W}{L}\right)_n = 2$

By observation:

MOS in Sat

$I_{DQ} = 1mA$

$V_{DQ} = V_{DD} - I_{DQ} \cdot R_D$

$= 2.5V$

Q.Point $= (V_{DQ}, I_{DQ})$

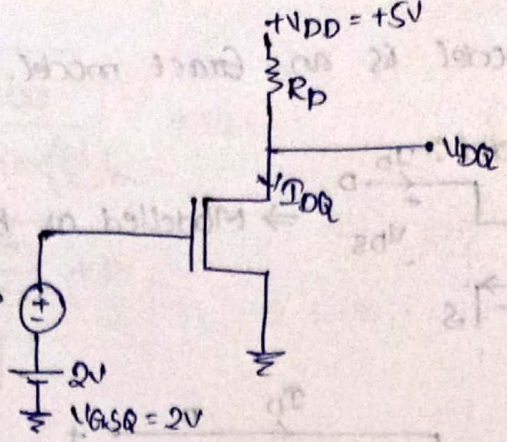
$= (2.5V, 1mA)$

DC condition:

@ Q. Point $V_G = 2V$, $I_{DQ} = 1mA$, $V_{DQ} = 2.5V$

depends purely on 'dc' parameter.

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if PK-PK ac input high comparing with $V_{GSQ} = 2V$ then it is large signal.

ac i/p

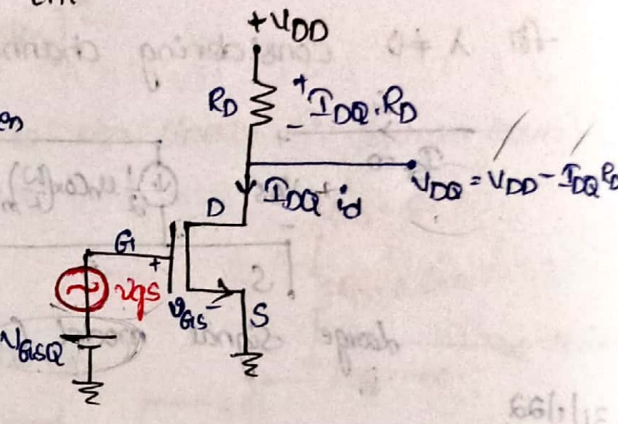
if PK-PK ac i/p is very small comparing with small signal.

dc voltage for biasing

↓

Establishing Q. Point.

We want to use this biasing ckt as an Amplifier.



1. For Simplicity, we have choosen constant gate to source voltage biasing technique. (Not a good way of biasing)

* 1. Kept V_{GSQ} so as to establish desired Q. point.

$V_{GSQ} \longrightarrow DC$

2. Because of $V_{GSQ} > V_{th} \Rightarrow I_{DQ}$ flows in to the circuit.

$I_{DQ} \rightarrow DC$

$\Rightarrow V_{DQ} = V_{DD} - I_{DQ} \cdot R_D$

$V_{DQ} \rightarrow DC$

Therefore Q. point is established. i.e., by keeping Mosfet in Saturation.

3. Now, we super impose ac input v_{gs} on dc i.e, V_{GSQ}

$v_{gs} \longrightarrow ac$

2.5

$\Rightarrow$ instantaneous gate to source voltage

$$v_{GS} = V_{GSQ} + v_{gs}$$
$$(DC) \quad (AC)$$

$\Rightarrow$ Bcz of v_{gs} ; we get i_d (ac)

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⇒ instantaneous drain current,

$$i_D = I_{DQ} + i_d$$
(DC) (AC)

⇒ instantaneous drain voltage,

$$v_D = V_{DD} - i_D R_D$$

Pure dc :- letter : Capital & Suffix : Capital.

Notation: V_{GSQ} ; I_{DQ} ; V_{DQ} → pure dc

Pure ac :- letter : Cap Small & Suffix : Small

Notation: v_{gs} ; i_d ; v_{ds} → pure ac

instantaneous :- letter : Small & Suffix : Capital
(dc+ac)

Notation: v_{GS} , i_D , v_D → instantaneous

* In Saturation:

$$i_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[v_{GS} - V_{tn}\right]^2$$

$$v_D = V_{DD} - i_D R_D$$

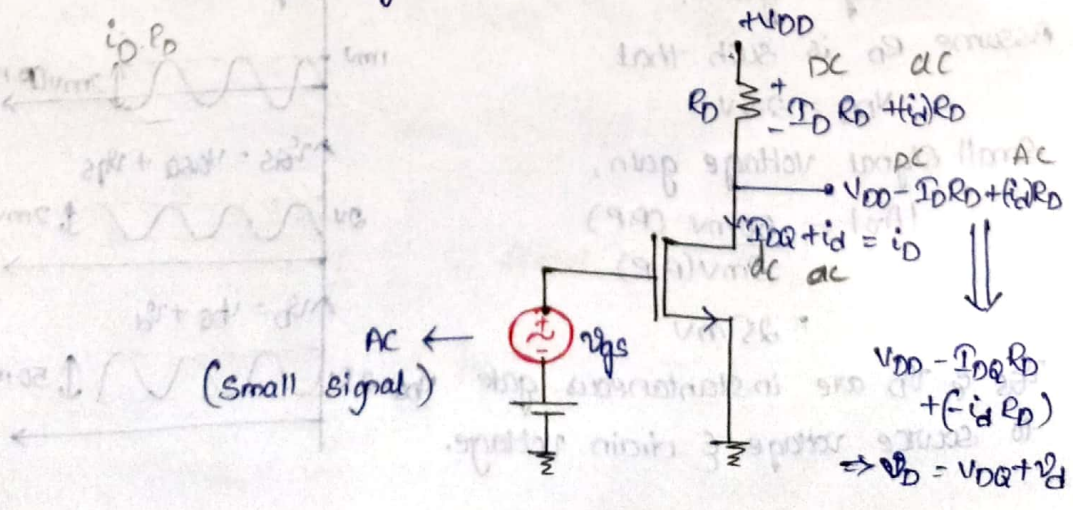
$$v_D = V_{DD} - (I_{DQ} + i_d) R_D$$

$$= V_{DD} - I_{DQ} R_D + (-i_d R_D)$$

v_d

$$v_D = V_{DQ} + v_d$$
(DC) (Ac.)

⇒ Instantaneous voltage drop across 'R_D' is $i_D \cdot R_D$



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Amplifier:

Voltage gain = $\frac{\text{o/p Peak to peak voltage (ac)}}{\text{i/p Peak to Peak voltage (ac)}}$

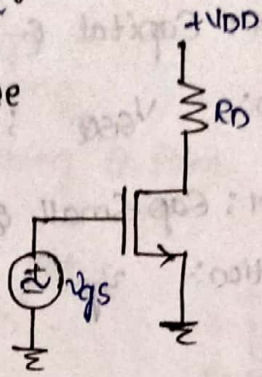
(No units)

$$A_v = \frac{v_o(P\text{-}P)}{v_{gs}(P\text{-}P)}$$

Note:- In order to find A_v, we need to get a relation b/w

Small Signal Operation :-

A student has forgot to give 'dc' gate to source voltage 'V_{GSQ}' and no he has given an ac i/p 'v_{gs}'. will this work as an amplifier.



≙ In an Amplifier, before applying an ac input i.e., v_{gs}. First of all, we have to establish Q. Point

⇒ Q. Point is established by provided dc gate to Source voltage V_{GSQ}.

⇒ In above case, Q-point has not been established.

⇒ Therefore, this will not work as Amplifier.

Student Doubt :-

How do we find Smallsignal voltage gain?

Assume R_D is such that

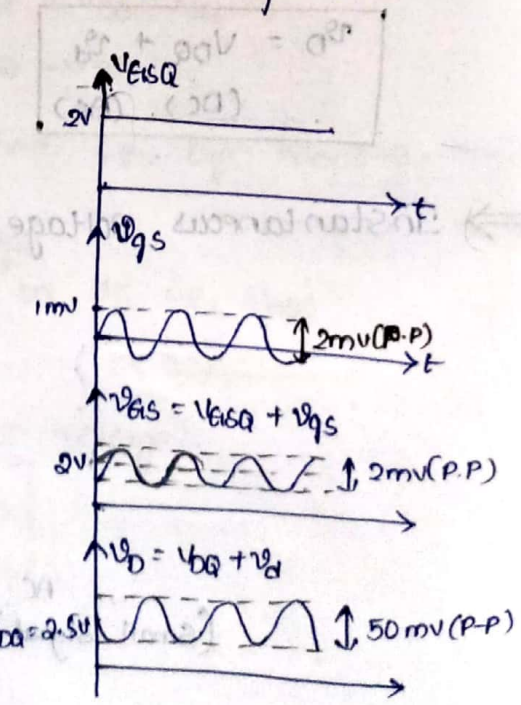
$V_{DQ} = 2.5V$

Small Signal voltage gain,

$$|A_v| = \frac{50mV\ (P\text{-}P)}{2mV\ (P\text{-}P)}$$

$$= 25$$

v_{GS} & v_D are instantaneous gate to source voltage & drain voltage.

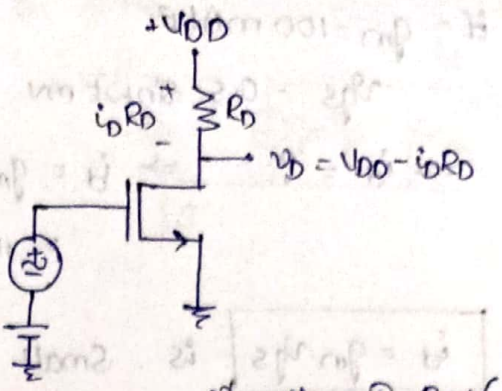


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Small Signal Operation

In Sat :-

Instantaneous drain current



$$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [v_{GS} - V_{tn}]^2$$

$$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GSQ} + v_{gs} - V_{tn}]^2$$

$$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [(V_{GSQ} - V_{tn}) + v_{gs}]^2$$

$$= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [(V_{GSQ} - V_{tn})^2 + 2(V_{GSQ} - V_{tn})v_{gs} + v_{gs}^2]$$

$$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSQ} - V_{tn})^2 + \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [2(V_{GSQ} - V_{tn})v_{gs} + v_{gs}^2]$$

$$I_{DQ} + i_d = I_{DQ} + \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [2(V_{GSQ} - V_{tn})v_{gs} + v_{gs}^2]$$

that $\boxed{v_{gs} : \text{Small signal.}}$ ← v_{gs} is very small compared to Q point 'V_{GSQ}'.

$$v_D = V_{DD} - I_{DQ}R_D + (-i_d R_D)$$
$$= V_{DQ} + v_d$$

Approximate :- If v_{gs} is small $\Rightarrow v_{gs}^2$ is very smaller

$$v_{gs}^2 << 2\underbrace{[V_{GSQ} - V_{tn}]}_{V_{ov}: \text{overdrive voltage.}} \cdot v_{gs}$$

$$\Rightarrow v_{gs} << 2[V_{GSQ} - V_{tn}]$$

then we can neglect v_{gs}^2 term in above eqn.

$$\Rightarrow i_d = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n 2[V_{GSQ} - V_{tn}]v_{gs}$$

$$i_d = \underbrace{\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSQ} - V_{tn})}_{\text{constant if } V_{GSQ} \text{ \& } \frac{W}{L} \text{ is fixed}} v_{gs}$$

$$\Rightarrow i_d = g_m v_{gs} \quad ; \quad g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSQ} - V_{tn})$$

(AC) (AC) = $g_m \times 1\text{mV}$

units : mA/V = mho = conductance = Trans

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if $g_m = 100\ mA/V^2$

$v_{gs} = 0.5 \sin \omega t\ mV$

$\Rightarrow i_d = ?$ $\Rightarrow i_d = g_m \times v_{gs}$

$= 100 \times 0.5 \sin \omega t = 50 \sin \omega t\ \mu A.$

* $\boxed{i_d = g_m \cdot v_{gs}}$ is small signal expression.

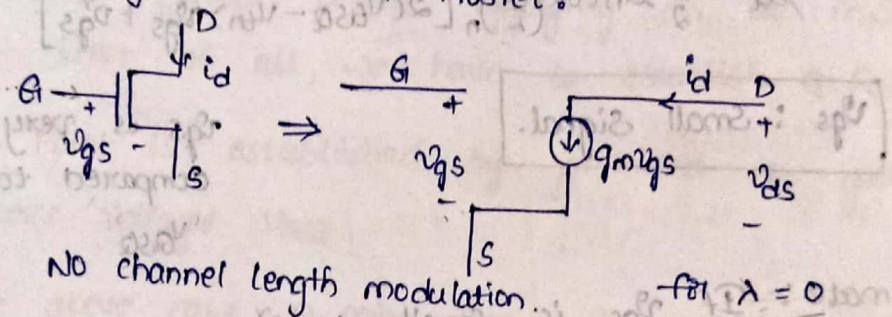
* 1. Small signal expression is linear.

2. Small signal expression is having approximation.

$v_{gs} << 2[V_{GSQ} - V_{th}]$

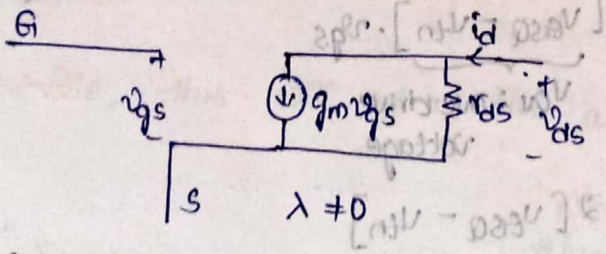
that's why small signal model is an approximated model.

3. Small signal model of Mosfet :-

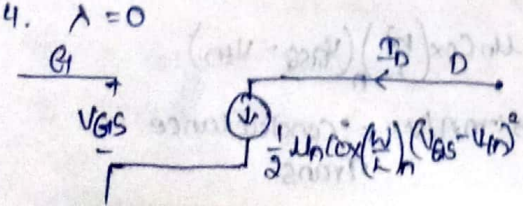
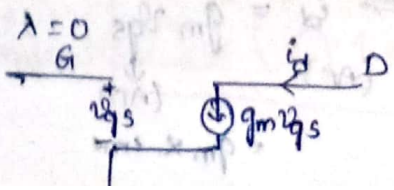


No channel length modulation. for $\lambda = 0$

$\lambda \neq 0$

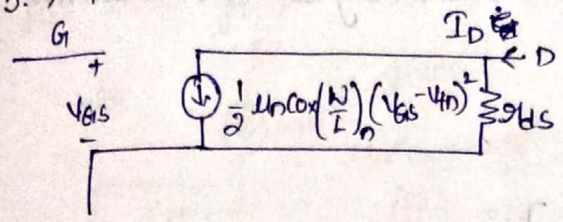


Comparision b/w large signal & small signal model

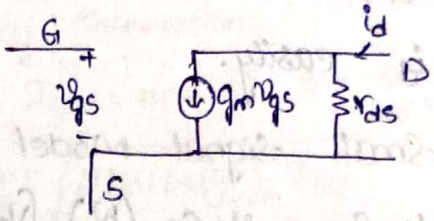
	Large Signal	Small Signal
1.	Expression: $I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)[V_{GS} - V_{th}]^2$	1. $i_d = g_m v_{gs}$
2.	Non-linear	2. Linear
3.	Exact model	3. Approximate model
4.	$\lambda = 0$ 	4. $\lambda = 0$ 

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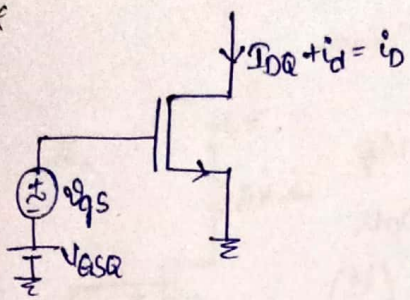
5. $\lambda \neq 0$



5. $\lambda \neq 0$



*



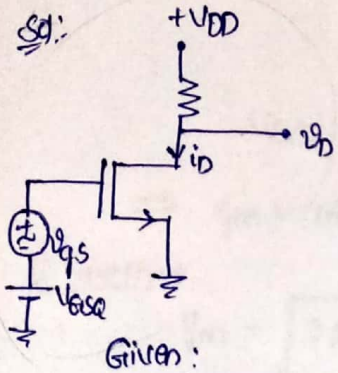
$\lambda = 0$

V_{GSQ}	v_{gs}	$v_{GS} = V_{GSQ} + v_{gs}$	I_{DQ}	$i_d = g_m v_{gs}$	$i_D = I_{DQ} + i_d$
2	0	2 V	1mA	0	1 mA
2V	1mV	2.001 V	1mA	2μA	1.002mA

1/2/22

*What is the need to go small signal model?

Sol:



$V_{GSQ} = 2V$; $v_{gs} = 1mV \Rightarrow i_d \rightarrow$ change in drain current.

$i_D = I_{DQ} + i_d$

$V_{GSQ} = 2V \Rightarrow I_{DQ} = 1mA$

$i_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n \left[v_{GS} - V_{tn}\right]^2$

$= \frac{1}{2} \times 1m \times 2 \times [1.001]^2$

$i_D = 1.002\ mA$

$v_{GS} = V_{GSQ} + v_{gs}$

$= 2.001\ V$

Given:

$\mu_n C_{ox} = 1mA/V^2$

$V_{tn} = 1V$

$\left(\frac{W}{L}\right)_n = 2$

$I_{DQ} + i_d = 1.002mA \Rightarrow i_d = 0.002mA = 2\mu A.$

* For finding i_d we have used square law eqn.

Alternate:

Since $v_{gs} = 1mA$ (Small signal)

We can use

Small signal Expr. $= i_d = g_m v_{gs}$

$= 2mA/V \times 1mV$

$= 2\mu A$

$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_n V_{ov}$

$= 1m \times 2 \times 1\ V$

$= 2mA/V$

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⇒ From this we can calculate small signal drain current i_d easily.

* Small signal Model

1. $g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GSQ} - V_{tn}] \rightarrow ①$

In sat:

$$I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GSQ} - V_{tn}]^2$$

$$(V_{GSQ} - V_{tn}) = \sqrt{\frac{2I_{DQ}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n}}$$

Substitute in eqn ①

$$\Rightarrow g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_n \sqrt{\frac{2I_{DQ}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n}}$$

2. $$\boxed{g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_n I_{DQ}}}$$

In sat :-

$$I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSQ} - V_{tn})^2$$

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n = \frac{I_{DQ}}{(V_{GSQ} - V_{tn})^2}$$

Substitute above eqn in ①

$$g_m = \frac{2I_{DQ}}{(V_{GSQ} - V_{tn})^2} \times (V_{GSQ} - V_{tn})$$

3. $$\boxed{g_m = \frac{2I_{DQ}}{V_{GSQ} - V_{tn}}}$$

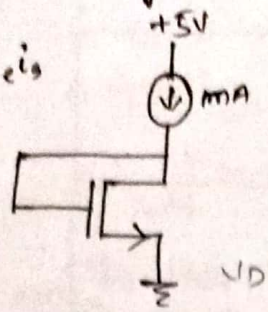
Finally :- Expression for g_m (transconductance) in Saturation

1. $g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSQ} - V_{tn})$
2. $g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_n I_{DQ}}$
3. $g_m = \frac{2I_{DQ}}{V_{GSQ} - V_{tn}}$

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Eg:- Find g_m of Mosfets

(i)



given

$\mu_n C_{ox} = 1mA/V^2$

$\left(\frac{W}{L}\right)_n = 8$

$V_D = V_G$

$\Rightarrow$ sat

By Observation:

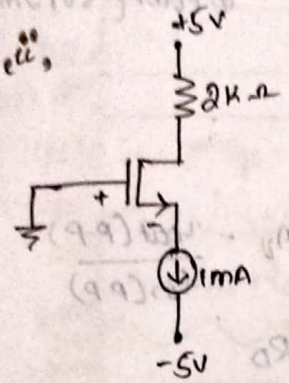
$I_{DQ} = 1mA$; $V_{GD} = 0$ (sat)

$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_n I_{DQ}}$

$= \sqrt{2 \times 1m \times 8 \times 1mA}$

$\boxed{g_m = 4\,mA/V}$

(ii)



given:

$\mu_n C_{ox} = 1mA/V^2$

$\left(\frac{W}{L}\right)_n = 8$

$V_{th} = 1V$

By observation:-

$I_{DQ} = 1mA$; $V_{DQ} = 5V - 1m \times 2K$

$= 3V$

$V_D > V_G \Rightarrow$ sat.

I st method.

$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSQ} - V_{th})$

$V_{GSQ} = ?$

In sat, $I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSQ} - V_{th})^2$

$V_{OV} = \sqrt{\frac{2I_{DQ}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n}} = \sqrt{\frac{2 \times 1mA}{1m \times 8}} = \frac{1}{2} = 0.5V$

$V_{GSQ} = 0.5V + 1V = 1.5V$

$\Rightarrow g_m = 1m \times 8 \times 0.5 = 4mA/V$. $\boxed{g_m = 4mA/V}$

II method.

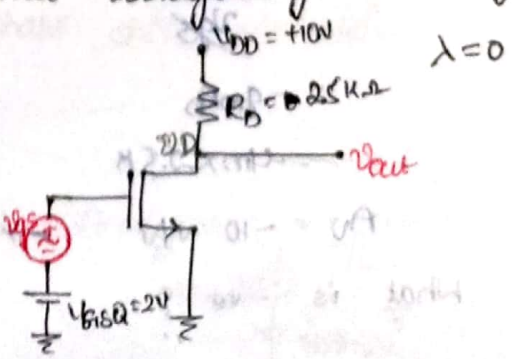
$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_n I_{DQ}} = \sqrt{2 \times 1m \times 8 \times 1mA} \Rightarrow \boxed{g_m = 4mA/V}$

III method:

$g_m = \frac{2I_{DQ}}{V_{GSQ} - V_{th}} = \frac{2 \times 1mA}{0.5m} \Rightarrow \boxed{g_m = 4\,mA/V}$

* How do we find small signal voltage gain using Small Signal Analysis?

Sol: Initially we are not using small signal Analysis for finding Small Signal voltage gain A_v.



$\lambda = 0$

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1. We have to find Q. point

Assume Mosfet is is sat

$\Rightarrow I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSQ} - V_{tn})^2$

$\boxed{I_{DQ} = 2mA}$

$V_{DQ} = V_{DD} - I_{DQ} \cdot R_D$

$= 10 - 2mA(2.5K)$ $\Rightarrow \boxed{V_{DQ} = 5V}$ Q. Point (5V, 2mA)

DC conditions :

$V_{GSQ} = 2V$, $I_{DQ} = 2mA$, $V_{DQ} = 5V$

2. For finding small signal voltage gain $A_v = \frac{v_{out}(P\text{-}P)}{v_{in}(P\text{-}P)}$

v_{out}, v_{in} → AC quantities.

$v_D = V_{DQ} + v_d$

$5V \quad -i_d R_D$

$v_D = V_{DD} - i_D R_D$

$= (V_{DD} - I_{DQ} R_D) + (-i_d R_D)$

$V_{DD} - (I_{DQ} + i_d) R_D$

$V_{DD} - I_{DQ} R_d - i_d R_D$

Now, $A_v = \frac{v_{out}}{v_{in}}$

By observation :

$v_{out} = v_d$ (small signal o/p ac signal)

$v_d = -i_d R_D$

$v_{in} = v_{gs}$

from small signal expression

$i_d = g_m v_{gs}$

$\Rightarrow g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSQ} - V_{tn}) = 1mA/V^2 \times 4 \times 1V$

$g_m = 4mA/V$

$\Rightarrow i_d = g_m v_{gs}$.

$A_v = \frac{-i_d R_D}{v_{gs}}$ $\left[\frac{v_{out}}{v_{in}} = \frac{-i_d R_D}{v_{gs}}\right]$

$= \frac{-g_m v_{gs} R_D}{v_{gs}}$

$= -g_m R_D$

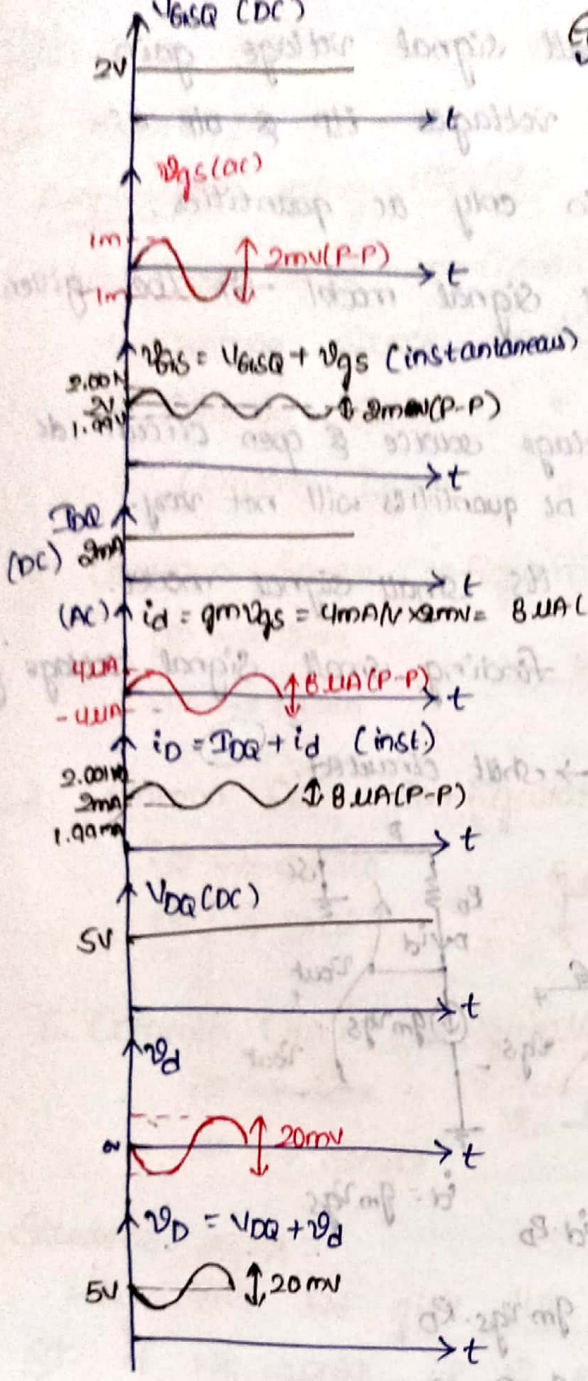
$= -4m \times 2.5K$

$A_v = -10$ V/V → small signal voltage gain.

What is -ve ?

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Graphical Approach.



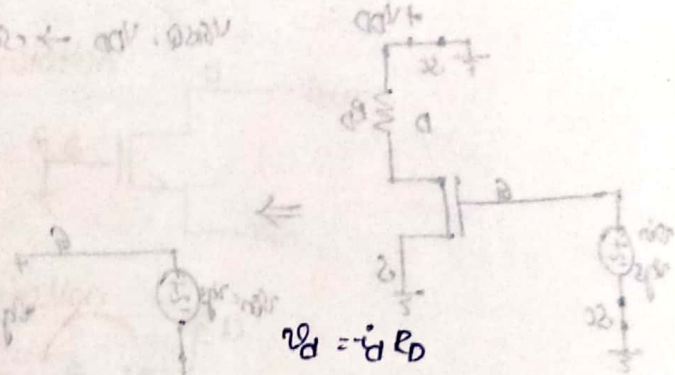
(v_{gs}) ↑ in ⇒ v_{GS} ↑

⇓

i_D ↑

⇓

v_D ↓ ⇐ $i_D R_D$ ↑



$v_d = -i_d R_D$

$= -8\mu A(P-P) \times 25k\Omega$

$= -20mV\ (P-P)$

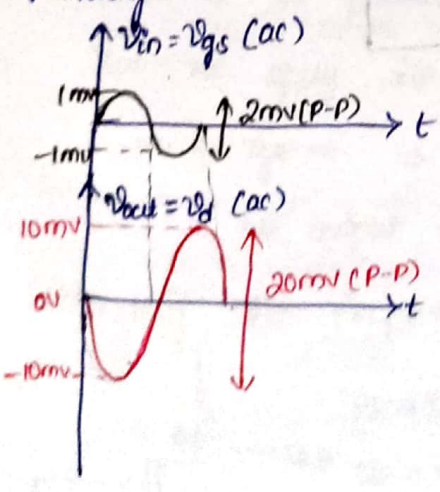
$A_v = \frac{v_{out}}{v_{in}} = \frac{v_d\ (P-P)}{v_{gs}\ (P-P)}$

$= \frac{-20mV\ (P-P)}{2mV\ (P-P)} = -10V/V$

$\boxed{A_v = -10V/V}$

180°

Finally :-

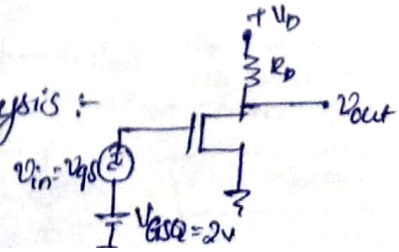


-ve means i/p & o/p are 180° out of phase.

i.e., i/p & o/p are having a phase shift of 180°.

NOW we use Small Signal Analysis :-

$A_v = \frac{v_{out}\ (P-P)\ (ac)}{v_{in}\ (P-P)\ (ac)}$



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Since for calculating small signal voltage gain, we need peak to peak voltages i/p & o/p ac.

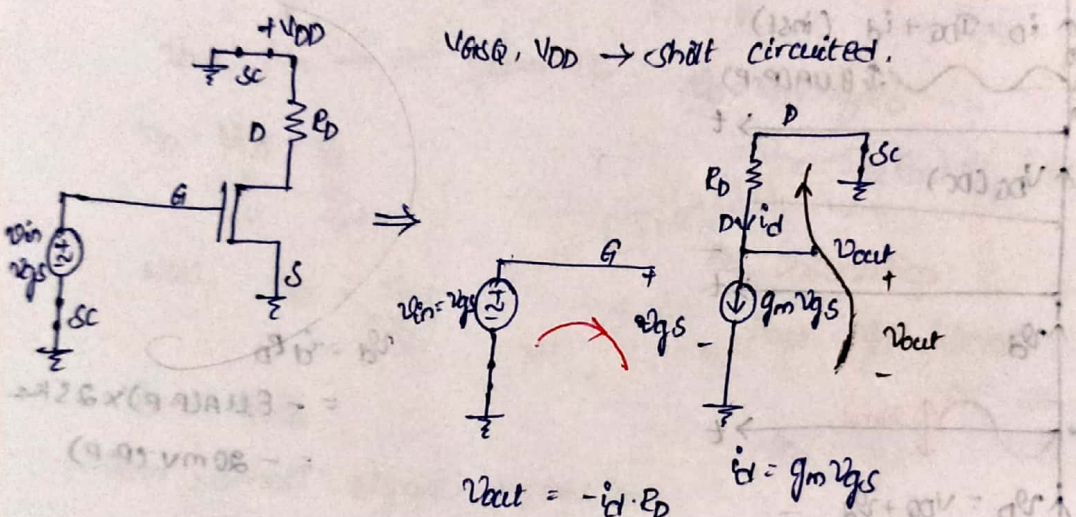
i.e., we are intrested in only ac quantities.

Now, we will apply small signal model for the given circuit.

Step 1 :- We short circuit dc voltage source & open circuit dc current sources. since DC quantities will not vary.

Step 2 : Replace Mosfet with its small signal model.

Step 3 : Do the analysis for finding small signal voltage gain



V_{GSQ}, V_{DD} → short circuited.

$v_{out} = -i_d \cdot R_D$

$= -g_m v_{gs} \cdot R_D$

$v_{out} = -g_m R_D \cdot v_{in}$

$$A_v = \frac{v_{out}}{v_{in}} = -g_m R_D$$

$\Rightarrow A_v = -4mA/V \times 2.5K = -10\ V/V$

$A_v = -10\ V/V$

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2/2/22

In Mosfet :-

Amplifiers using Mosfet :-

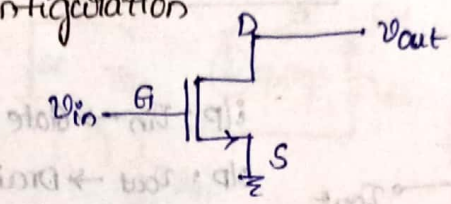
There are three configurations

1. Common Source configuration (CS)
2. Common Gate " (CG)
3. Common Drain " (CD)

1. Common Source Configuration

i/p → Gate

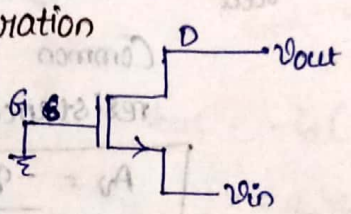
o/p → Drain



2. Common Gate Configuration

i/p → Source

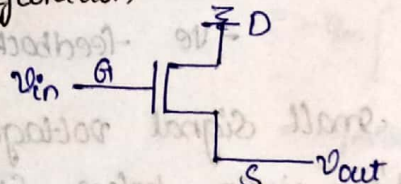
o/p → Drain



3. Common Drain Configuration

i/p → Gate

o/p → Source



Student doubt :-

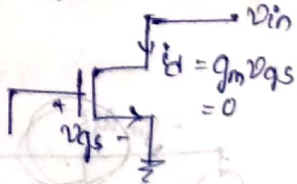
Why don't we give i/p @ drain?

Sol: if we apply i/p @ either gate or source then we will be having "v_{gs}" ⇒ $g_m v_{gs}$ current is generated and it is passed through the load for having v_{out}.

But we apply i/p v_{in} @ drain we don't $v_{gs} = 0$

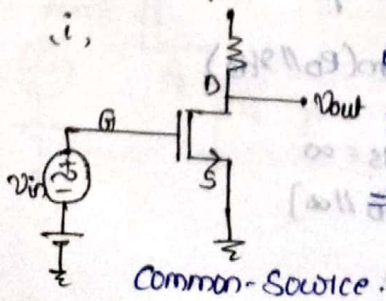
⇒ $g_m v_{gs} = 0$ ⇒ $v_{out} = 0$

∴ No output voltage ⇒ gain = 0.



Identify the Amplifiers wrt their Configurations.

i,



i/p → v_{in} @ gate

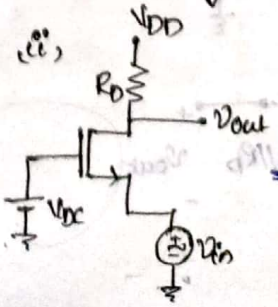
o/p → v_{out} @ drain

No feedback

⇒ Common Source.

Common-Source. $A_v = -g_m R_D$

ii,



i/p : v_{in} @ Source

o/p : v_{out} @ drain

No feedback

⇒ Common Gate

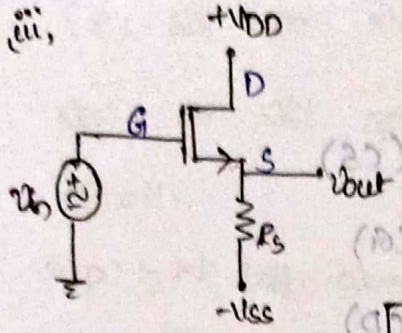
$A_v = +g_m R_D$

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* In CS amplifier ; i/p & o/p are 180° out of phase

* In CG amplifier ; i/p & o/p are same phase (0°).

(iii)



i/p → @ Gate

o/p → @ Source

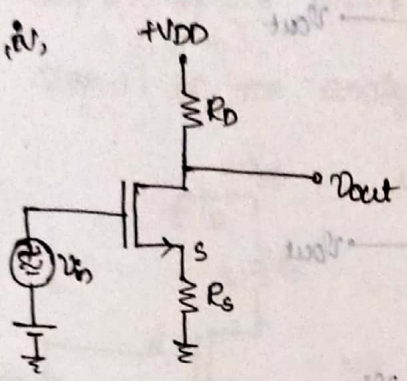
Common Drain Amplifier or (CD)

-ve feedback is present. due to R_S.

$$A_v = \frac{+g_m R_S}{1+g_m R_S}$$

⇒ In CD amplifier, i/p & o/p are same phase.

(iv)



i/p : V_{in} → Gate

o/p : V_{out} → Drain

Common Source Amplifier with degenerated resistance R_S

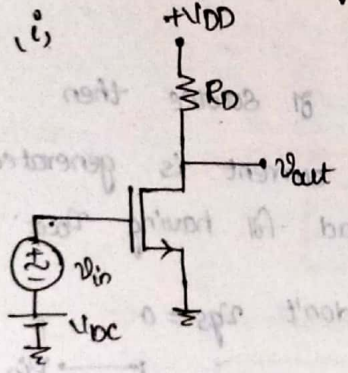
$$A_v = \frac{-g_m R_D}{1+g_m R_S}$$

Here i/p & o/p are 180° out of phase.

-ve feedback is present.

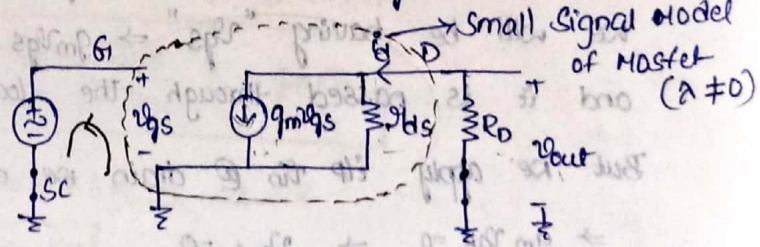
Derive the small signal voltage gain expression for the following ckt's given below. [λ ≠ 0]

(i)



By observation

Common Source Configuration.



$V_{in} = V_{gs}$

Both r_{ds} & R_D are in parallel

i.e., $r_{ds} \,//\, R_D$

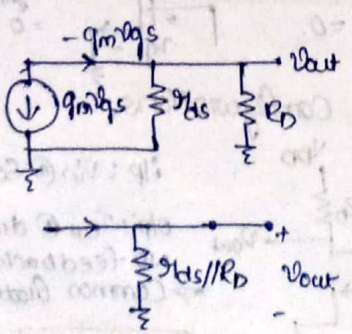
$V_{out} = -g_m V_{gs} \times r_{ds} \,//\, R_D$

$$\frac{V_{out}}{V_{in}} = A_v = -g_m (R_D \,//\, r_{ds})$$

If $\lambda = 0 \Rightarrow r_{ds} = \infty$

$\Rightarrow A_v = -g_m [R_D \,//\, \infty]$

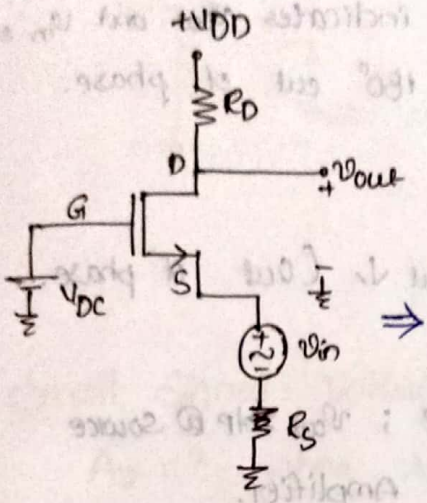
$A_v = -g_m R_D$



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Q. Repeat the above problem for the CG, CD & CS with degeneration resistance R_S.

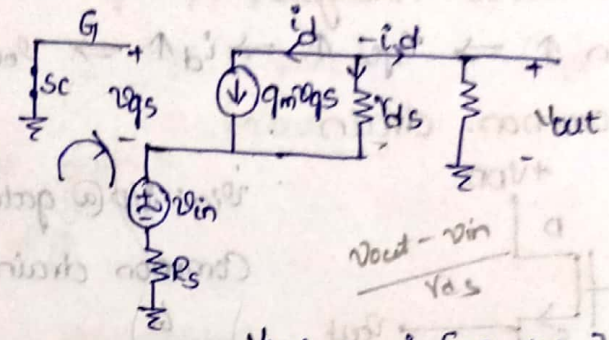
(i) Common Gate



v_{in} : i/p ⇒ Source

v_{out} : o/p ⇒ Drain.

Common Gate Amplifier. ($\lambda \neq 0$)



$\frac{v_{out}}{v_{in}}$

NOW Apply KVL,

$v_{gs} + v_{in} + i_d R_S = 0$

$v_{in} = -v_{gs} - i_d R_S$

$v_{in} = -v_{gs} - g_m v_{gs} R_S$

$v_{gs} = \frac{-v_{in}}{1+g_m R_S}$

NOW, $\frac{v_{out}}{v_{in}} = \frac{+g_m}{1+g_m R_S} [r_{ds} // R_D]$

'+' indicates v_{out} and v_{in} are in phase.

-ve feedback provided by R_S.

$v_{out} = -i_d [r_{ds} // R_D]$

$= -g_m v_{gs} [r_{ds} // R_D]$

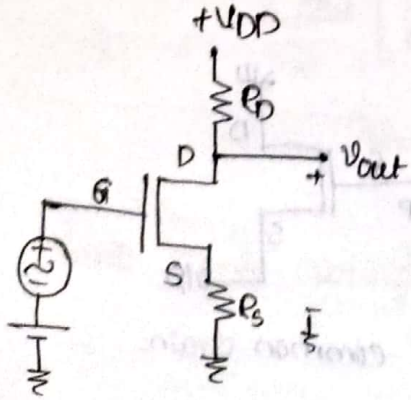
$= -g_m \left[\frac{-v_{in}}{1+g_m R_S}\right] [r_{ds} // R_D]$

$= \frac{g_m v_{in}}{1+g_m R_S} [r_{ds} // R_D]$

Qualitative Analysis:-

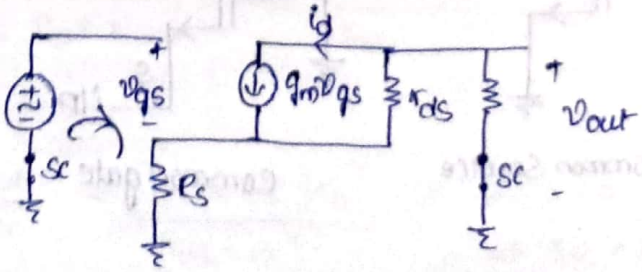
$v_{in} \uparrow \Rightarrow v_{gs} \downarrow \Rightarrow i_d \downarrow \Rightarrow v_{out} \uparrow$

(ii) Common ~~drain~~ Source



v_{in} : i/p @ Gate ; v_{out} : o/p @ drain

Common Source Amplifier.



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$-v_{in} + v_{gs} + i_d R_s = 0$

$v_{in} = v_{gs} + g_m v_{gs} R_s$

$\frac{v_{in}}{1+g_m R_s} = v_{gs}$

$v_{out} = -i_d [R_D // r_{ds}]$

$v_{out} = -g_m v_{gs} [r_{ds} // R_D]$

$v_{out} = -g_m \frac{v_{in}}{1+g_m R_s} [r_{ds} // R_D]$

Now, $\boxed{\frac{v_{out}}{v_{in}} = -\frac{g_m}{1+g_m R_s} [r_{ds} // R_D]}$

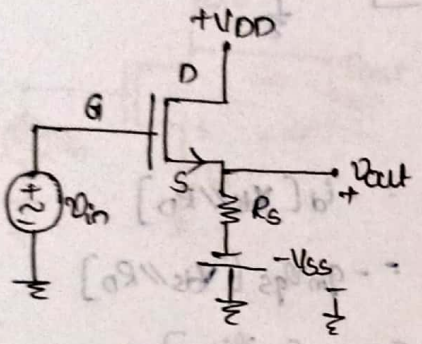
'-' indicates v_{out} and v_{in} are 180° out of phase.

'-' ve feedback provided by R_s

Qualitative Analysis :-

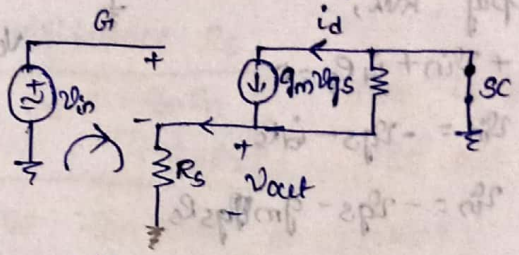
$v_{in} \uparrow \Rightarrow v_{gs} \uparrow \Rightarrow i_d \uparrow \Rightarrow v_{out} \downarrow$ (Out of phase.

(iii) Common drain



v_{in}: i/p @ gate ; v_{out} : o/p @ source

Common drain Amplifier.



$-v_{in} + v_{gs} + i_d R_s = 0$

$v_{in} = v_{gs} + g_m v_{gs} R_s$

$v_{gs} = \frac{v_{in}}{1+g_m R_s}$

$v_{out} = i_d R_s$

$v_{out} = g_m v_{gs} R_s$

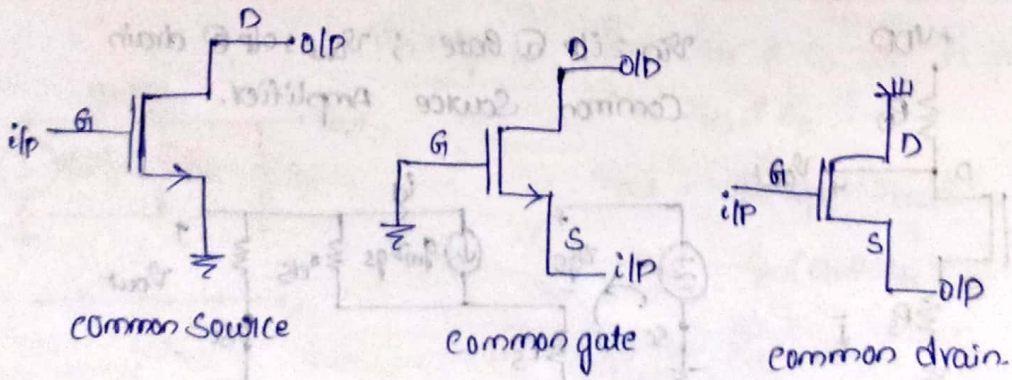
$v_{out} = g_m \cdot \frac{v_{in}}{1+g_m R_s} \cdot R_s$

$\boxed{\frac{v_{out}}{v_{in}} = +\frac{g_m R_s}{1+g_m R_s}}$

Here '+' indicates v_{out} & v_{in} are in phase.

R_s provides -ve feedback.

3/2/22

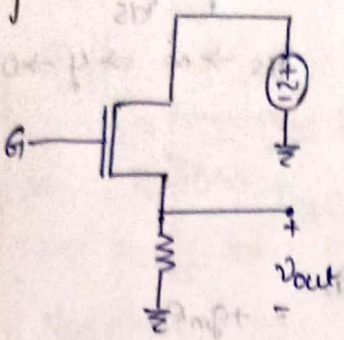


common source common gate common drain.

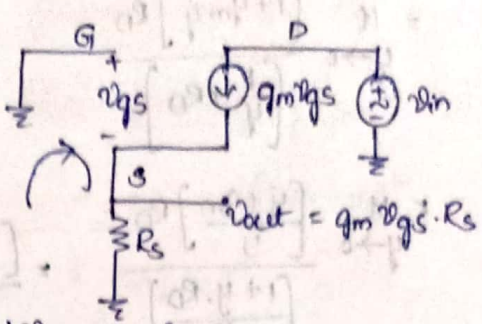
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Note :- We don't apply V_{in} at drain because $v_{gs} = 0$

Explanation :-



AC Analysis:



$+v_{gs} + g_m v_{gs} R_s = 0$

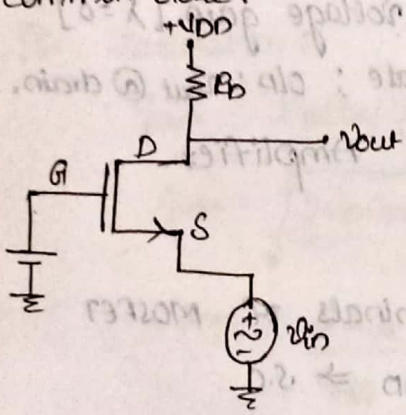
$v_{gs}[1 + g_m R_s] = 0 \quad [v_{gs} = 0]$

$\boxed{v_{out} = 0}$

Small Signal Voltage gain :-

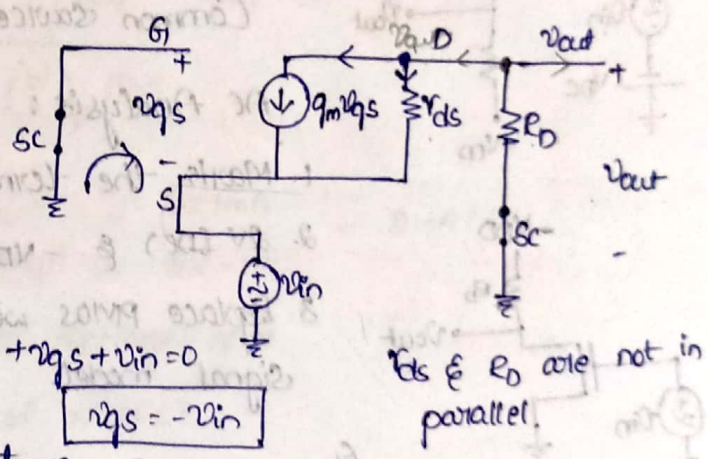
$A_v = ?$ when $\lambda \neq 0$

Common Gate :-



AC Analysis :

DV (DC) & V_{DD} ⇒ short circuit.



$+v_{gs} + v_{in} = 0$

$\boxed{v_{gs} = -v_{in}}$

r_{ds} & R_D are not in parallel.

Apply Nodal Analysis at v_{out}

$$\frac{v_{out} - 0}{R_D} + \frac{v_{out} - v_{in}}{r_{ds}} + g_m v_{gs} = 0$$

$$v_{out}\left[\frac{1}{R_D} + \frac{1}{r_{ds}}\right] = \frac{v_{in}}{r_{ds}} + g_m v_{in}$$

$$v_{out}\left[\frac{r_{ds} + R_D}{R_D \times r_{ds}}\right] = \frac{v_{in}[1 + g_m r_{ds}]}{r_{ds}}$$

Small Signal Voltage gain,

$$A_v = \frac{v_{out}}{v_{in}} = \frac{[1 + g_m r_{ds}] R_D}{[r_{ds} + R_D]}$$

if $\lambda = 0$

$\Rightarrow r_{ds} = \infty$

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$$A_v = \lim_{r_{ds}\to\infty} \frac{[1+g_m r_{ds}]R_D}{[r_{ds}+R_D]}$$

let $r_{ds} = \frac{1}{y}$

$\Rightarrow y = \frac{1}{r_{ds}}$

$r_{ds} \to \infty \Rightarrow y \to 0$

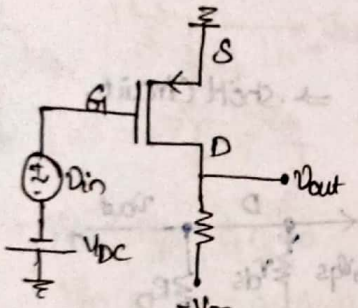
$$= \lim_{y\to 0} \frac{\left[1+g_m\frac{1}{y}\right]R_D}{\left[\frac{1}{y}+R_D\right]}$$

$$= \lim_{y\to 0} \frac{\left[\frac{y+g_m}{y}\right]R_D}{\left[\frac{1+y.R_D}{y}\right]} = \frac{[0+g_m]R_D}{1+0.R_D} = +g_m R_D$$

$$\boxed{A_v = +g_m R_D}$$

From Derivation of Small Signal Model of PMOS.

⇒ We have found out that small signal model of PMOS is same as small signal model of NMOS.



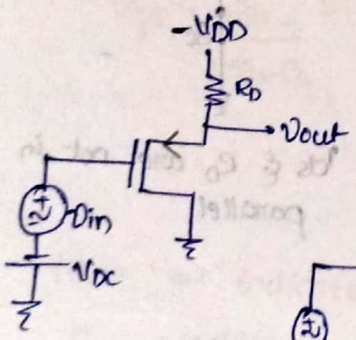
Small Signal voltage gain. [$\lambda = 0$]

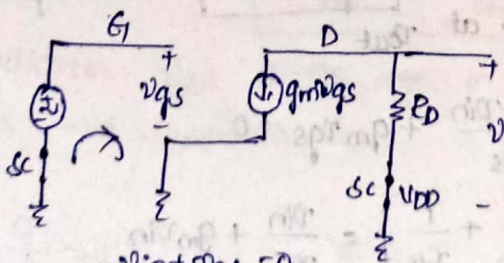
i/p : v_{in} @ gate ; o/p : v_{out} @ drain.

Common source Amplifier.

AC Analysis :

1. Mark the terminals of MOSFET
2. 2V (DC) & -VDD ⇒ S.C
3. Replace PMOS with its equivalent small signal model.





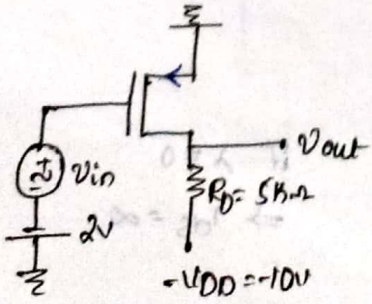
$-v_{in} + v_{gs} = 0$

$$\boxed{v_{gs} = v_{in}}$$

$v_{out} = -g_m v_{gs}(R_D)$

$$\boxed{\frac{v_{out}}{v_{in}} = A_v = -g_m R_D}$$

Problem :-



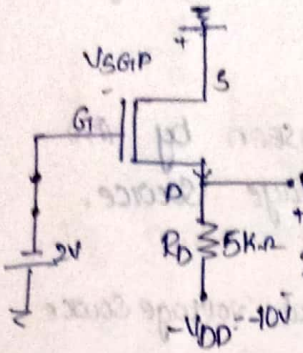
$\mu_n C_{ox} = 0.5mA/V^2$, $\left(\frac{W}{L}\right)_p = 4$ $V_{tp} = -1V$.

find $A_v = \frac{V_{out}}{V_{in}}$ $\lambda = 0$

1. Finding the Q. point from there we can calculate g_m (based on DC).

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While finding Q point (DC) we remove ac sources.



We don't know the region of operation

Assume PMOS is in Saturation:

$I_{DQ} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p [V_{SGP} - |V_{tp}|]^2$ [I_{DQ} S→D]

$= \frac{1}{2} \times 0.5 \times 4 [2V - 1V]^2$

$= 1m[1V]^2$

$= 1mA.$

$V_{DQ} = I_{DQ} \cdot R_D - V_{DD} = 1mA(5K) - 10V \Rightarrow V_{DQ} = -5V$

$V_{DQ} = -5V$

$V_{GQ} = -2V$

$V_D < V_G \Rightarrow$ Saturation

$\Rightarrow$ Assumption true.

Q. Point (-5V, 1mA)

In Saturation:

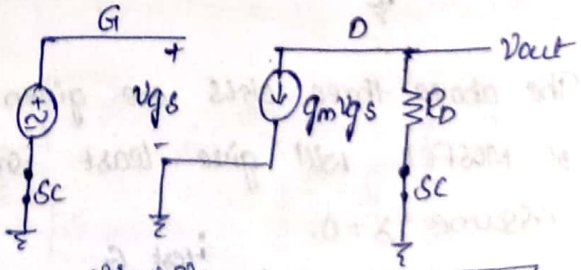
$$g_{mp} = \mu_p C_{ox}\left(\frac{W}{L}\right)_p [V_{GSQ} - |V_{tp}|]^2$$

$$g_{mp} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_p I_{DQ}}$$

$$g_{mp} = \frac{2I_{DQ}}{V_{GSQ} - |V_{tp}|} = \frac{2 \times 1mA}{2V - 1V} = 2mA/V$$

Now find Small Signal Voltage gain

1. Mark the terminals of MOSFET
2. Short Circuit DC voltage Source & Open Circuit DC current Source.
3. Replace MOSFET with its Small Signal Model.
4. Do the Analysis.



$-V_{in} + V_{gs} = 0 \Rightarrow \boxed{V_{gs} = V_{in}}$

$V_{out} = g_m V_{gs} \cdot R_D$

$V_{out} = -g_m V_{in} R_D$

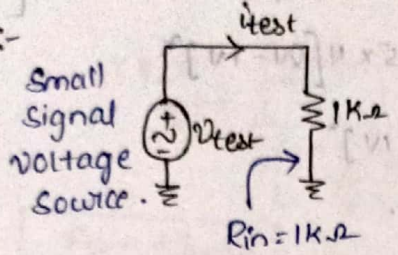
Small Signal voltage gain, $A_V = \frac{V_{out}}{V_{in}} = -g_m R_D$

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* So-far, we have calculated small signal voltage gain, Now, we start small signal resistances.

Small Signal Resistance:- The resistance seen by the small signal voltage source.

Eg:-



v_{test} = Small signal voltage source

i_{test} = Small signal current.

R_{in} → Small signal resistance seen by v_{test}

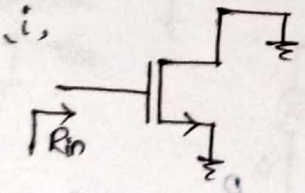
$$R_{in} = \frac{v_{test}}{i_{test}} = 1K\Omega \quad [-v_{test} + i_{test} 1K\Omega = 0]$$

For finding Small signal resistances.

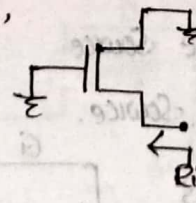
1. Draw the small signal model of the circuit.
   - (i) Mark the terminals
   - (ii) DC voltage sources ⇒ short circuited
     DC current " ⇒ open circuited.
   - (iii) Replace MOSFET with small signal model.
2. Connect a test source v_{test} at the terminal which is desired & i_{test} is the current coming out of v_{test}

   ⇒ Small signal resistance $R_{in} = \frac{v_{test}}{i_{test}}$

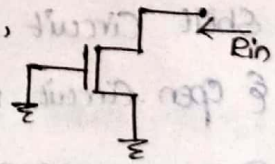
(i)



(ii)



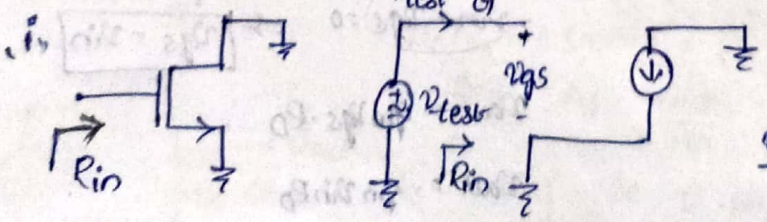
(iii)



The above three ckts are given to as to find which terminal of MOSFET will give least small signal resistance

Assume $\lambda = 0$.

(i)



By observation:

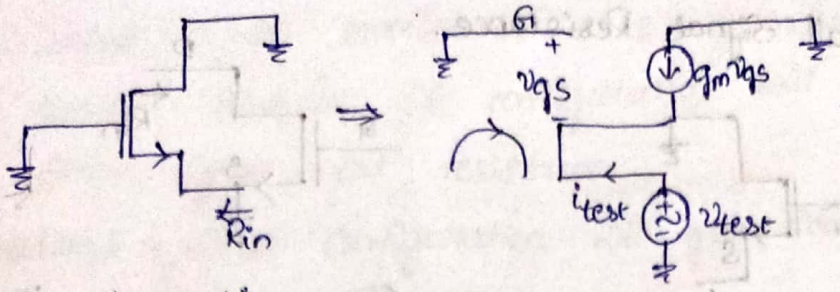
$i_{test} = 0$

$$\frac{v_{test}}{i_{test}} = \frac{v_{test}}{0} = \infty$$

Small signal resistance seen into Gate, $R_{in} = \infty$

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(ii)



$+v_{gs} + v_{test} = 0$

$v_{gs} = -v_{test}$.

By observation,

$$i_{test} = -g_m v_{gs} = -g_m(-v_{test}) = g_m v_{test}.$$

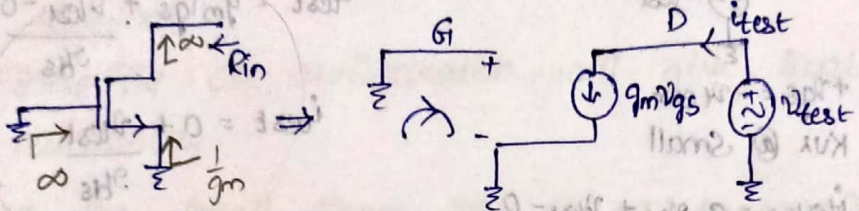
$$R_{in} = \frac{v_{test}}{i_{test}} = \frac{v_{test}}{g_m v_{test}} = \frac{1}{g_m}$$

if $g_m = 10mA/V$

$R_{in} = \frac{1}{10m} = 100\Omega$

Small signal resistance seen into source, $R_{in} = \frac{1}{g_m}$

(iii)



By observation $v_{gs} = 0$

$$i_{test} = g_m v_{gs} \Rightarrow i_{test} = 0$$

$$R_{in} = \frac{v_{test}}{i_{test}} = \infty$$

Small signal resistance seen into drain, $R_{in} = \infty$.

Note :- By comparing all 3 cases, Small signal resistance seen into source will give least resistance i.e.,

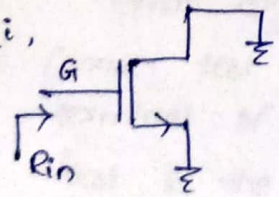
$R_{in} = \frac{1}{g_m}$.

* Typically r_{ds} is high.

4/2/22

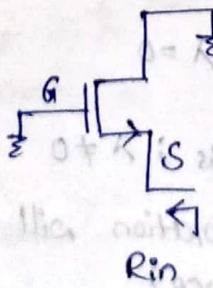
$\lambda = 0$ Small signal Resistance.

(i)



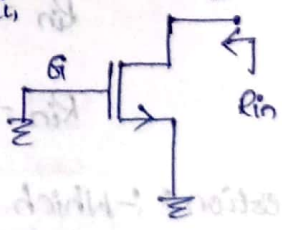
$R_{in} = \infty$

(ii)



$R_{in} = \frac{1}{g_m}$

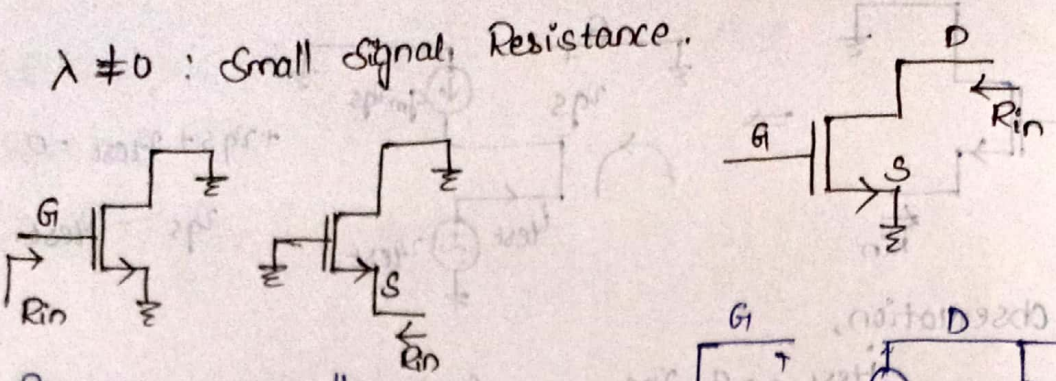
(iii)



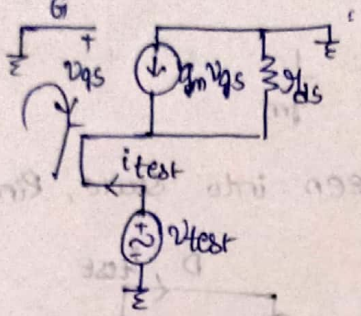
$R_{in} = \infty$

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$\lambda \neq 0$: Small Signal Resistance.



$R_{in} = \infty$



$+v_{gs} = -v_{test}$

KVL @ Small

$$i_{test} = -g_m v_{gs} + \frac{v_{test} - 0}{r_{ds}}$$

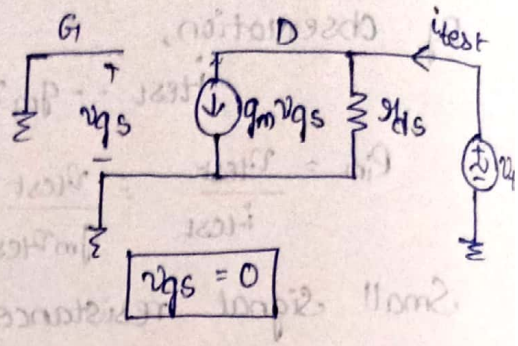
$$= +g_m v_{test} + \frac{v_{test}}{r_{ds}}$$

$$v_{test}\left[g_m + \frac{1}{r_{ds}}\right] = i_{test}$$

$$\frac{v_{test}}{i_{test}} = \frac{r_{ds}}{1 + g_m r_{ds}} = \frac{r_{ds}}{g_m\left[r_{ds} + \frac{1}{g_m}\right]}$$

$$R_{in} = \frac{v_{test}}{i_{test}} = \frac{1/g_m \cdot r_{ds}}{\frac{1}{g_m} + r_{ds}} = \frac{1}{g_m} // r_{ds}$$

$$R_{in} = \frac{1}{g_m} // r_{ds}$$



$$i_{test} = g_m v_{gs} + \frac{v_{test} - 0}{r_{ds}}$$

$$i_{test} = 0 + \frac{v_{test}}{r_{ds}}$$

$$R_{in} = \frac{v_{test}}{i_{test}} = r_{ds}$$

* Typically r_{ds} will be in terms of kilograms.

⇒ Therefore source terminal will give least small signal resistance.

$$R_{in} = \frac{1}{g_m} \; ; \; \lambda = 0$$

$$R_{in} = \frac{1}{g_m} // r_{ds} \; ; \; \lambda \neq 0$$

Question 1 :- Which configuration will give least small signal input resistance?

Sol:- Common Source Configuration : i/p @ gate

" Gate " : i/p @ Source

" Drain " : i/p @ gate

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∵ Input in CG configuration is given at source terminal. Therefore CG configuration will give least small signal input resistance.

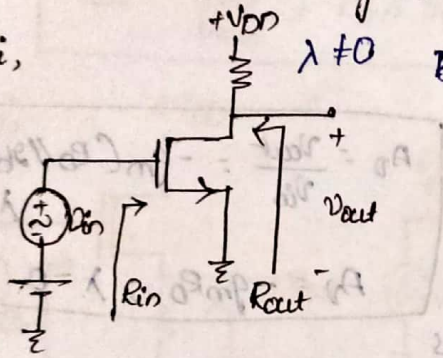
Question 2 :- What configuration will give least small signal output resistance.

Sol:- Common Source Configuration: o/p @ Drain
" Gate " : o/p @ Drain
" Drain " : o/p @ Source.

∵ In common drain configuration: o/p is taken at source terminal.
Therefore CD configuration will give least small signal o/p resistance.

Find the small signal i/p & o/p resistance for following

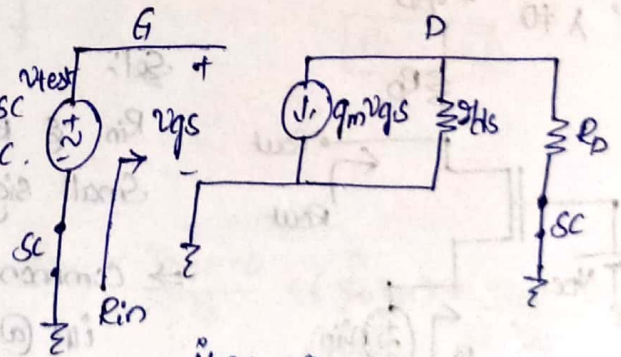
i,



By observation:
Common Source Amplifier
(or)
Common Source Configuration.

Finding Rin (Small Signal)

1. Apply AC Analysis
   i, Mark the terminals
   ii, DC voltage source → SC
   DC current " → OC.
   iii, Replace MOSfet with small signal model



2. Connect test source at terminal of our intrest
   itest is the current flowing out of Vtest. (Small signal current)
   Shut circuit the i/p Small signal voltage sources.

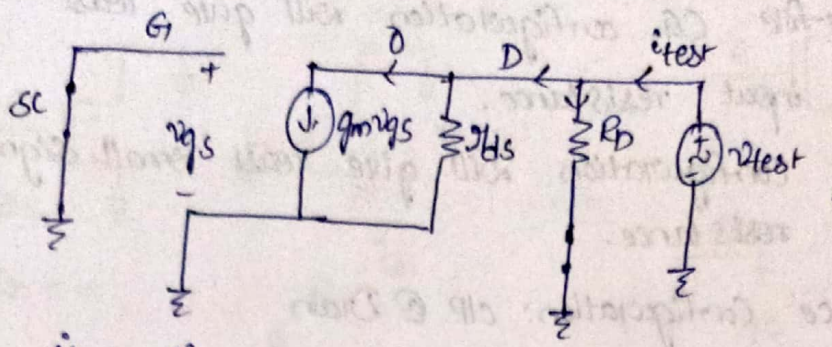
itest = 0

$\Rightarrow R_{in} = \frac{V_{test}}{i_{test}}$

$R_{in} = \infty$

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finding Small Signal Resistance R_{out}.



$v_{gs} = 0$

$\Rightarrow g_m v_{gs} = 0$

$$i_{test} = \frac{v_{test} - 0}{R_D} + \frac{v_{test} - 0}{r_{ds}}$$

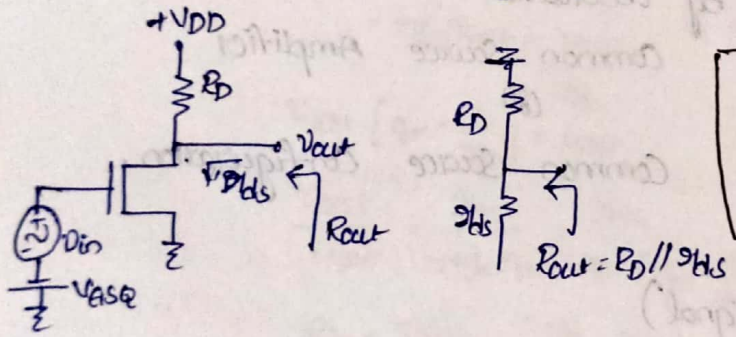
$$= v_{test}\left[\frac{1}{R_D} + \frac{1}{r_{ds}}\right] = v_{test}\left[\frac{r_{ds} + R_D}{R_D r_{ds}}\right]$$

$$R_{out} = \frac{v_{test}}{i_{test}} = \frac{R_D r_{ds}}{R_D + r_{ds}} = R_D \,//\, r_{ds}$$

$\Rightarrow \boxed{R_{out} = R_D // r_{ds}}$

if $\lambda = 0 \Rightarrow r_{ds} = \frac{1}{\lambda I_D} = \infty$

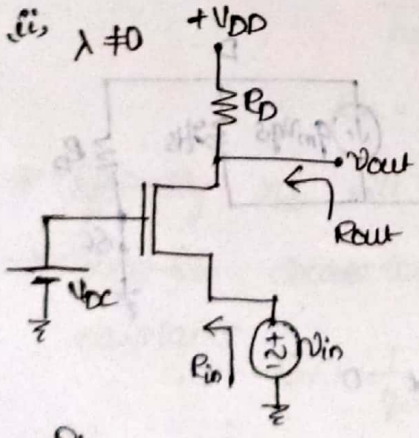
$\Rightarrow R_{out} = R_D // \infty = R_D \quad (\lambda = 0)$



$$A_v = \frac{v_{out}}{v_{in}} = -g_m(R_D // r_{ds}) \quad \lambda \neq 0$$

$$A_v = -g_m R_D, \quad \lambda = 0$$

ii) $\lambda \neq 0$



Sol:

R_{in} & R_{out} :

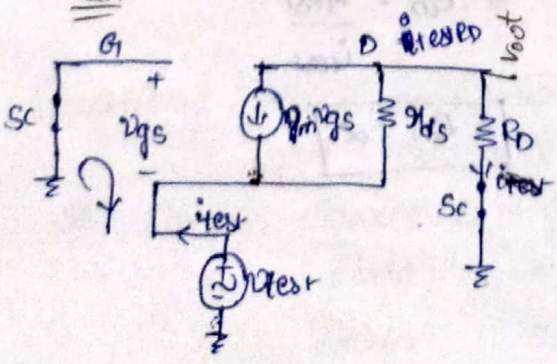
Small signal i/p & o/p resistances.

$\Rightarrow$ Common Gate Configuration

i/p @ source

o/p @ drain.

R_{in}



$\boxed{+v_{gs} = -v_{test}}$

$$i_{test} = -g_m v_{gs} + \frac{v_{test} - i_{test} R_D}{r_{ds}}$$

$$= +g_m v_{test} + \frac{v_{test} - i_{test} R_D}{r_{ds}}$$

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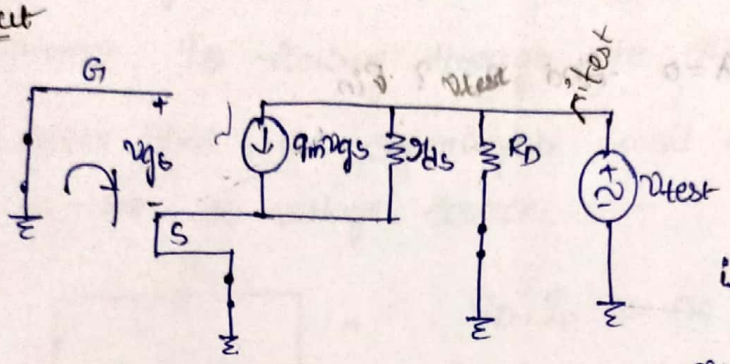
$$i_{test}\left[1+\frac{R_D}{r_{ds}}\right] = \frac{v_{test}\left[g_m+\frac{1}{r_{ds}}\right]}{g_m+\frac{1}{r_{ds}}}$$

If $\lambda = 0 \Rightarrow r_{ds} = \infty$

$$\Rightarrow R_{in} = \frac{1+\frac{R_D}{\infty}}{g_m+\frac{1}{\infty}} = \frac{1}{g_m}$$

$$\Rightarrow \frac{v_{test}}{i_{test}} = R_{in} = \frac{1+\frac{R_D}{r_{ds}}}{g_m+\frac{1}{r_{ds}}}$$

R_{out}



$v_{gs} = 0$

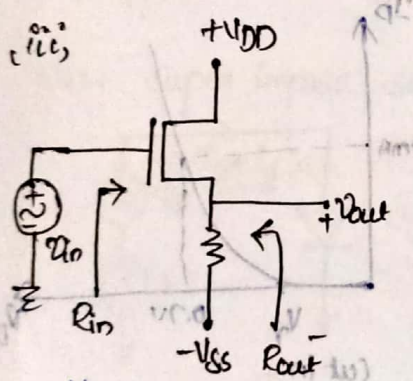
$\Rightarrow g_m v_{gs} = 0$.

$$i_{test} = \frac{v_{test}-0}{R_D} + \frac{v_{test}-0}{r_{ds}}$$

$$\frac{v_{test}}{i_{test}} = \frac{R_D r_{ds}}{R_D + r_{ds}}$$

$$R_{out} = \frac{v_{test}}{i_{test}} = R_D \,//\, r_{ds}$$

(iii)

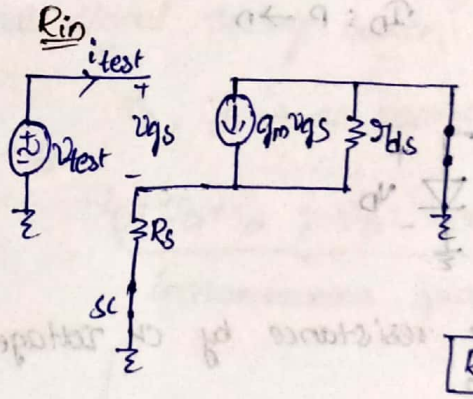


i/p @ Gate,

o/p @ Source

⇒ Common Drain.

R_{in}

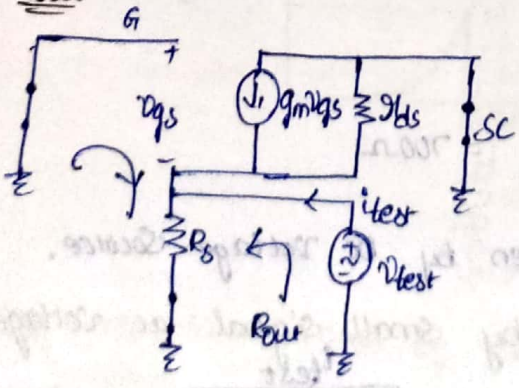


$i_{test} = 0$

$$\Rightarrow R_{in} = \frac{v_{test}}{i_{test}} = \infty$$

$$R_{in} = \infty$$

R_{out}



$$i_{test} = \frac{v_{test}-0}{R_S} + (-g_m v_{gs}) + \frac{v_{test}-0}{r_{ds}}$$

$(+g_m v_{test})$

$$i_{test} = v_{test}\left[\frac{1}{R_S}+\frac{1}{r_{ds}}+g_m\right]$$

$$= v_{test}\left[\frac{1}{R_S}+\frac{1}{r_{ds}}+\frac{1}{1/g_m}\right]$$

$+v_{gs} + v_{test} = 0$

$$v_{gs} = -v_{test}$$

$$\frac{v_{test}}{i_{test}} = \frac{1}{\frac{1}{1/g_m}+\frac{1}{r_{ds}}+\frac{1}{R_S}}$$

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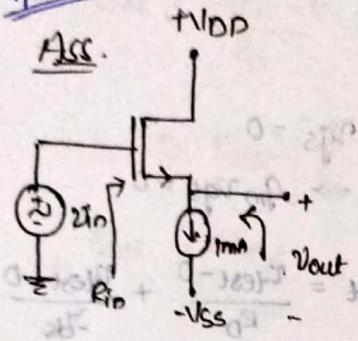
$$\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}=\frac{1}{R_1 // R_2 // R_3}$$

$$\Rightarrow \frac{v_{test}}{i_{test}}=\frac{1}{\frac{1}{1/g_m // r_{ds} // R_S}}$$

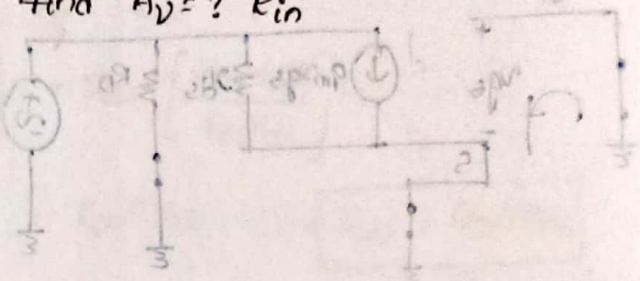
$$R_{out}=\frac{1}{g_m} // r_{ds} // R_S$$

9/2/22

Ass.



$\lambda = 0$ find $A_V = ?$ R_{in}

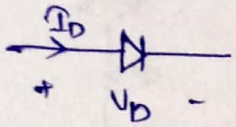


Voltage Buffer.

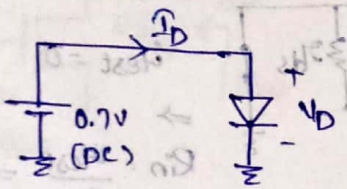
$\Rightarrow A_V = 1$

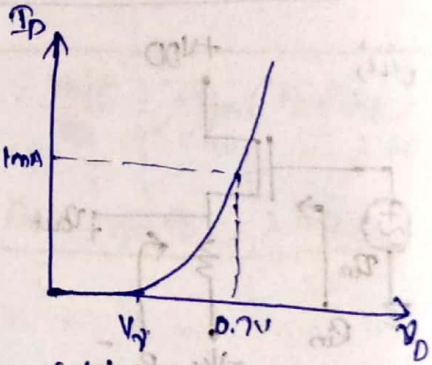
Static & Dynamic Resistance.

$\Rightarrow$ (AC)



$I_D : P \rightarrow n$





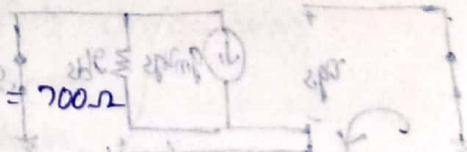
Cut in voltage.

Q: What is the resistance by DC voltage source 0.7V?

Sol:- $V_D = 0.7V$, $I_D = 1mA$

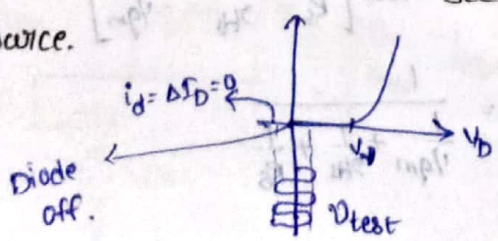
$\therefore$ Static resistance $= \frac{V_D}{I_D}$

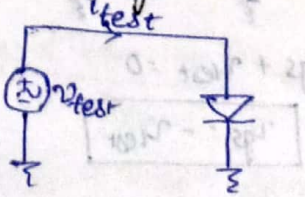
Here i/p dc voltage is static. $= \frac{0.7V}{1mA} = 700\Omega$



Static Resistance :- Resistance seen by DC voltage source.

Q: What is the resistance seen by small signal ac voltage source.





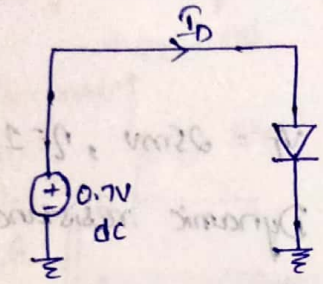
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⇒ We can't apply small signal voltage source directly across a diode. Bcz diode will be off.

then, how to give small signal voltage source across a diode.

Sol:- First of all; we will switch on the diode by applying DC voltage source so as to have desired diode current I_D flowing through the diode.

⇒ After this, we superimpose small signal voltage source on the dc voltage source.

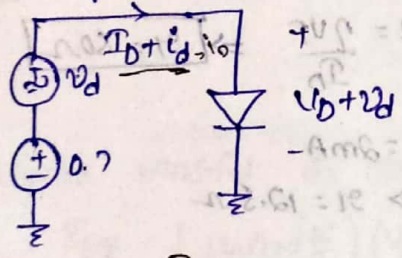


$V_D, I_D \Rightarrow$ DC quantities.

from the $I_D - V_D$ char, the resistance seen by dc voltage source is

Static resistance $= \frac{V_D}{I_D} = \frac{0.7}{1mA} = 700\Omega$

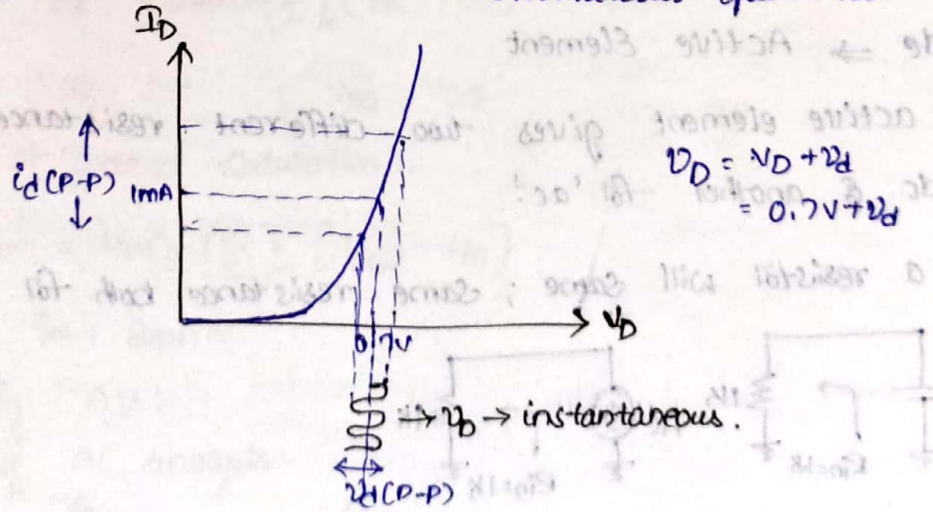
Now super impose small signal voltage source.



$v_D, i_d \Rightarrow$ ac quantities.

$i_D = I_D + i_d$; $v_D = V_D + v_d$

instantaneous quantities.



$v_D = V_D + v_d$
$= 0.7V + v_d$

The resistance seen by small signal voltage source is nothing but dynamic or resistance or AC resistance.

Dynamic resistance $= r_d = \frac{dV}{dI} = \frac{v_d(P-P)}{i_d(P-P)}$

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$I_D = I_0 \left[e^{V_D/\eta V_T} - 1 \right]$ I_0 : reverse saturation current

$I_D = I_0 e^{V_D/\eta V_T} - I_0$ → neglected compared to first term

$I_D = I_0 e^{V_D/\eta V_T}$

Diff. wrt 'V_D'

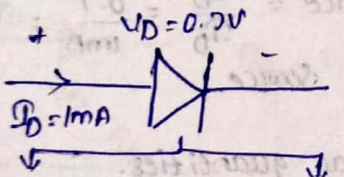
$\frac{dI_D}{dV_D} = I_0 e^{V_D/\eta V_T} \cdot \frac{1}{\eta V_T}$

$\frac{dI_D}{dV_D} = \frac{I_D}{\eta V_T} \Rightarrow r = \frac{dV_D}{dI_D} = \frac{1}{\left(\frac{dI_D}{dV_D}\right)} = \frac{1}{\frac{I_D}{\eta V_T}}$

Dynamic resistance $\boxed{r = \frac{\eta V_T}{I_D}}$

⇒ In Ckt Case, $I_D = 1mA$ & Assume $V_T = 25mV$, $\eta = 1$

$r = \frac{1 \times 25mV}{1mA} \Rightarrow \boxed{r = 25\Omega}$ Dynamic resistance.



Static 700Ω (DC)

Dynamic 25Ω (AC)

If $I_D = 0.5mA$

$r = \frac{\eta V_T}{I_D} \Rightarrow \boxed{r = 50\Omega}$

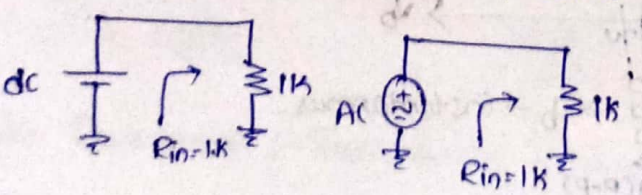
if $I_D = 2mA$

$\Rightarrow r = 12.5\Omega$

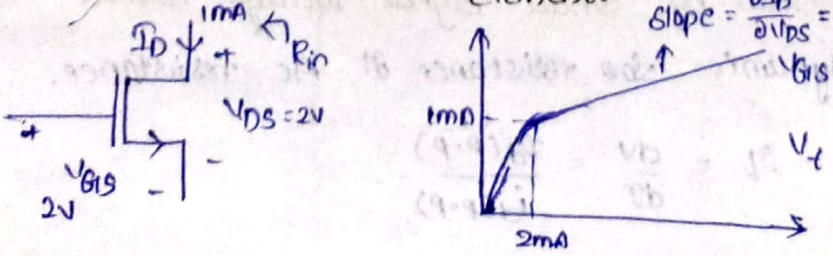
* Diode ⇒ Active Element

⇒ An active element gives two different resistance one for dc & another for 'ac'

⇒ But a resistor will same ; same resistance both for dc & ac



Eg:- MOSfet is an Active element.



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Resistance seen by dc voltage source

@ Drain = $\frac{V_{DS}}{I_D} = \frac{2V}{1mA} = 2K\Omega$

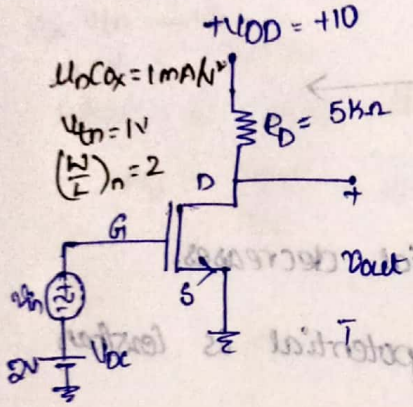
Resistance seen by small signal voltages source

@ drain = $\frac{\partial V_{DS}}{\partial I_D} = r_{ds} = 100K\Omega$

$r_{ds} = \frac{1}{\text{slope}}$

$= \frac{1}{\left(\frac{\partial I_D}{\partial V_{DS}}\right)} = \frac{\partial V_{DS}}{\partial I_D}$

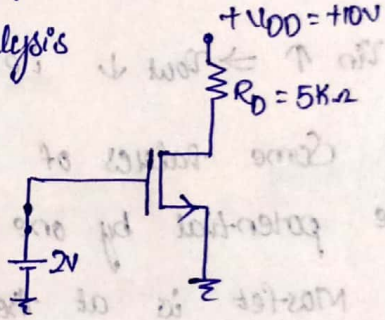
Voltage Swings :-



[Assume the small signal voltage gain $A_v = -100\ V/V$]

Here. Q. Point :-

DC Analysis



Assume Mosfet in sat :

$I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS} - V_{tn})^2 = 1mA$

$V_{DQ} = 5V$; $V_{DQ} > V_{GIQ}$

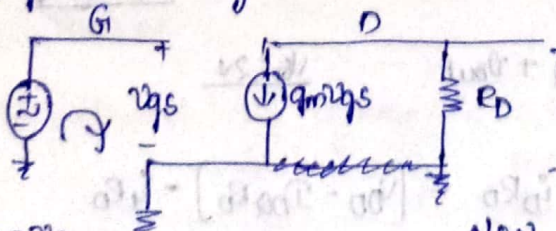
$\Rightarrow$ Indeed Saturation.

$\Rightarrow g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GSQ} - V_{tn}]$

$g_m = 2mA/V$

finding A_V :-

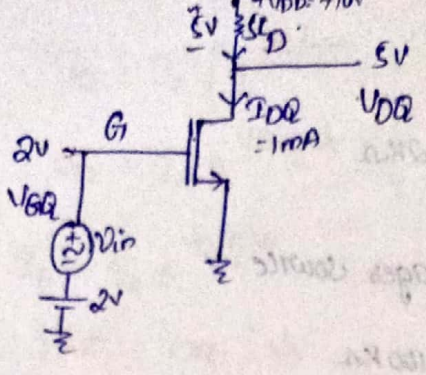
Apply AC analysis :-



NOW, $\frac{v_{out}}{v_{in}} = A_v = -g_m R_D$

$A_v = -2mx\ 5K\Omega = -10\ V/V$

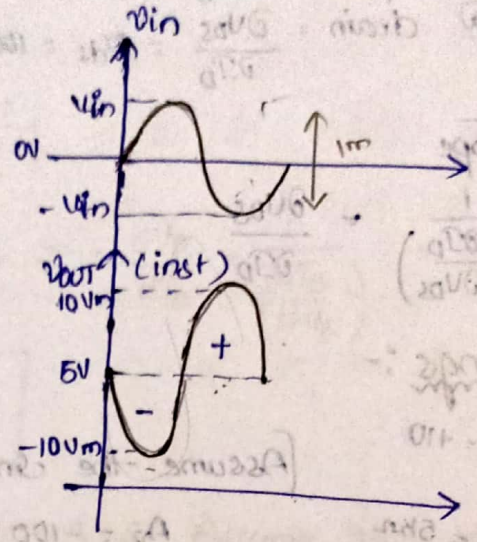
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$v_{in} = v_m \sin \omega t$

$A_v = \frac{v_{out}}{v_{in}} = -10 V/V$

$\boxed{v_{out} = -10 v_{in}}$



By observation:-

if $v_{in} < 0$ (-ve half)

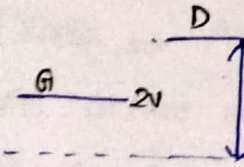
$\Rightarrow v_{out} \uparrow$

if $v_{in} \uparrow \Rightarrow v_{out}$ (P-P) $\uparrow$

$\Rightarrow$ if $v_{in} \uparrow \Rightarrow v_{out} \downarrow$ i.e., drain potential decreases.

$\Rightarrow$ for some values of v_{in}; drain potential is lesser than gate potential by one threshold voltage.

i.e., Mosfet is at the edge of saturation.



Allowed o/p negative peak (swing) @ o/p = 4V.

$V_G - V_{th} = 2V - 1V = 1V$ ↑ triode.

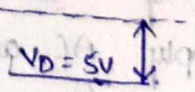
Allowed output negative swing

Note:- We have to operate MOS in saturation.

Allowed o/p +ve swing

if $v_{in} \downarrow \Rightarrow v_{out} \uparrow$

for some value of $v_{in} \Rightarrow v_{out}$ reaches to a max of $V_{DD} = 10V$. How?



Instantaneous $v_{OUT} = V_{OUTQ} + v_{out}$ $\quad V_{GS} = 2V$

$= 5V + v_{out}$

$v_{OUT} = V_{DD} - i_D R_D = [V_{DD} - I_{DQ} R_D] - i_d R_D$

$v_{in} \downarrow \Rightarrow v_{GS} \downarrow \Rightarrow i_D \downarrow$

(cut-off) at one value of v_{in}, $i_D = 0 \Rightarrow v_{OUT} = V_{DD}$

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$I_{DQ} + i_d = 0$ When $v_{out} = V_{DD}$

$\Rightarrow i_d = -I_{DQ}$ $\Rightarrow$ MOSfet = cutoff.

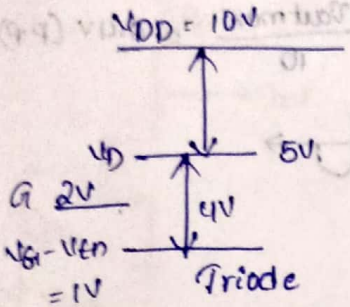
$\Rightarrow$ Allowed o/p positive swing = 5V

Allowed o/p negative swing = 4V

$\Rightarrow$ Allowed o/p symmetrical swing = 8V (P-P) (Here MOS will be in sat)

↓

Positive & negative should be same.



Allowed o/p symmetrical o/p swing = 8V (P-P)

What is max. allowed i/p signal?

$A_v = \frac{v_{out}}{v_{in}} = -10 V/V \Rightarrow |A_v| = 10$

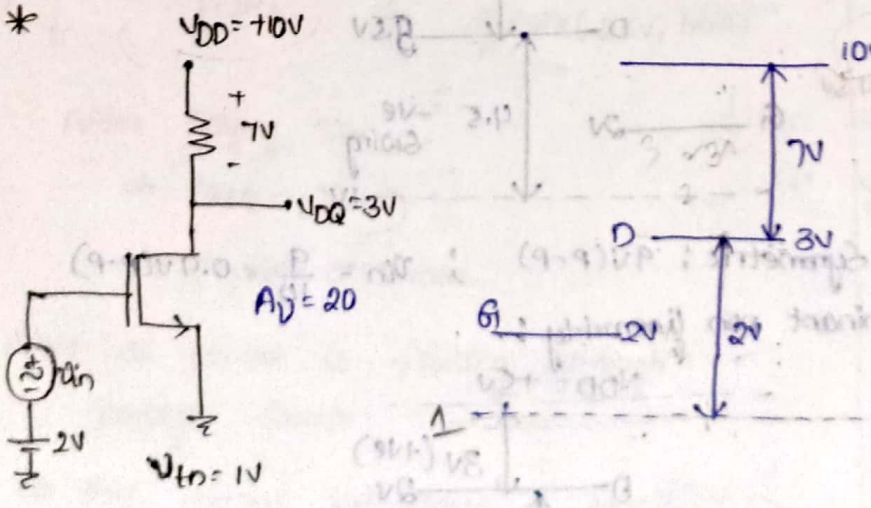
$\Rightarrow \frac{v_{out\,max}}{v_{in\,max}} = 10$

$\Rightarrow v_{in\,max} = \frac{v_{out\,max}}{10} = \frac{8V(P-P)}{10} =$

MOSfet : Sat $\leftarrow$ $v_{in\,max} = 0.8V$ (P-P)

$\Rightarrow$ Dominant Non-linear :- Triode.

*

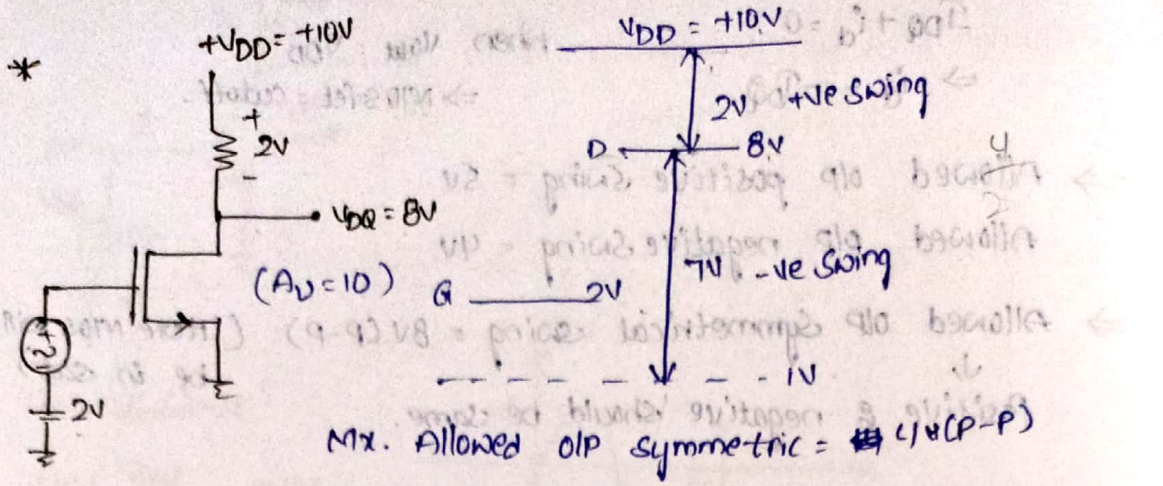


Mx. allowed o/p symmetric = 4V (P-P)

" " i/p swing = $\frac{4V}{20}$ (P-P) = 0.2V (P-P)

Dominant Non-Linearity : Triode.

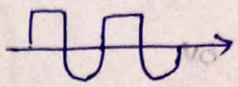
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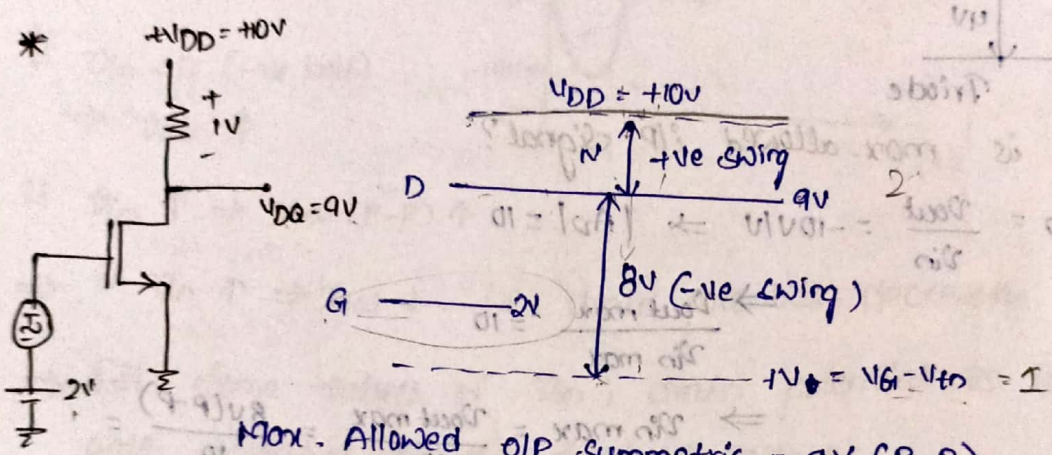


Max. Allowed o/p symmetric = 4 V(P-P)

Max. allowed i/p swing = $\frac{V_{out\,max}}{10}$ = 0.4V (P-P)

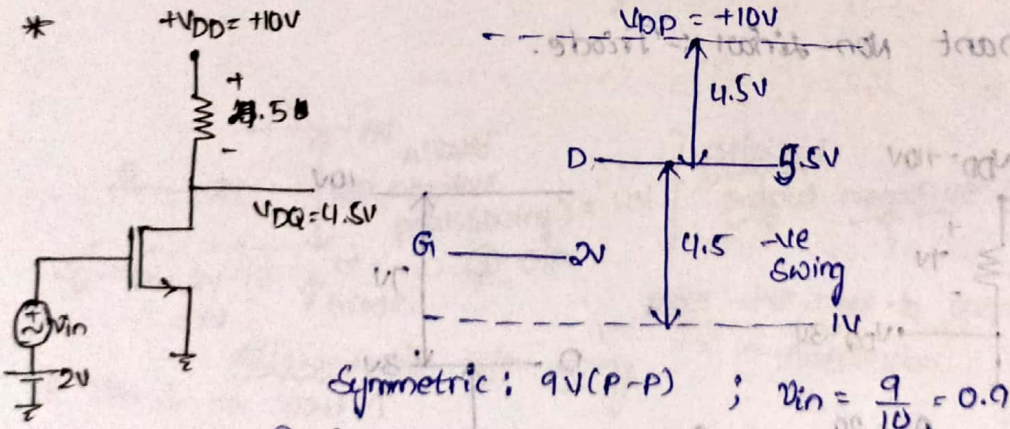
$V_{in} > 0.4V$ (P-P) → cut-off.





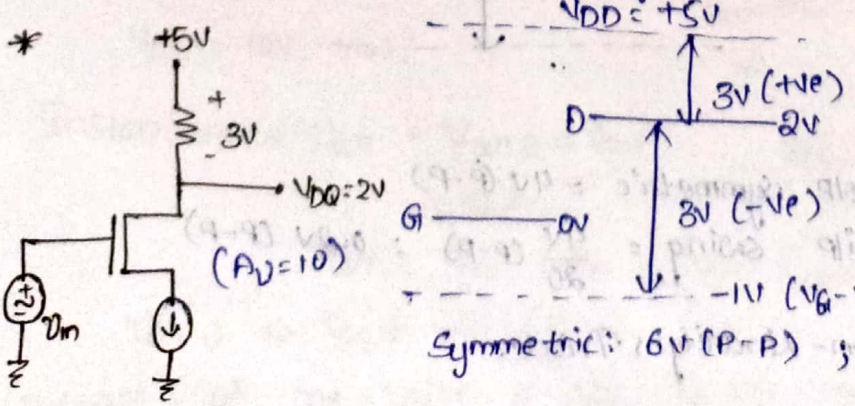
Max. Allowed o/p symmetric = 1V (P-P)

Dominant : cut-off. i/p swing = $\frac{2}{20}$ =



Symmetric : 9V(P-P) ; $V_{in} = \frac{9}{10} = 0.9\,V(P\text{-}P)$

Dominant non linearity :



Symmetric : 6V (P-P) ; i/p = $\frac{6V}{10}$ = 0.6V

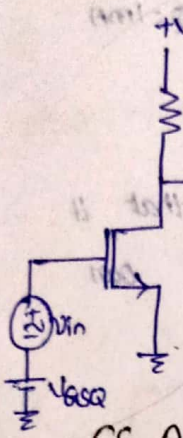
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$V_{in} < max.V_{in} \Rightarrow$ Sat.

10/2/22

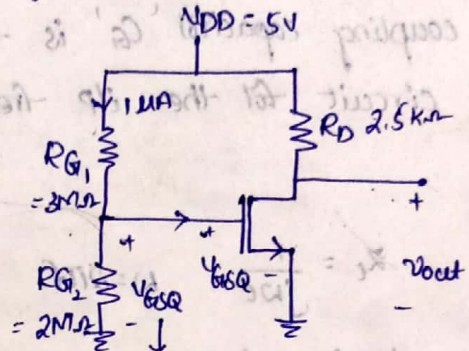
* In an Amplifier; After biasing i.e, when Q. point is established then we apply small signal voltage source.

Question: How do we apply Small Signal voltage Source?



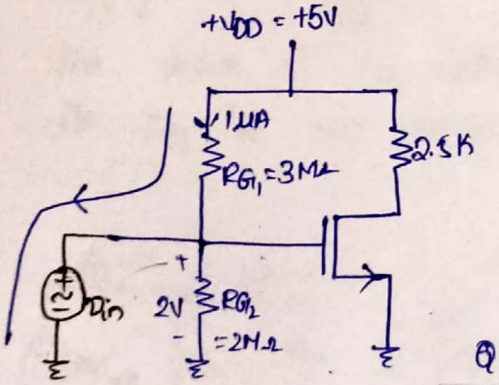
CS Amplifier

We can get desired V_{GSQ} with the help of single power supply V_{DD}.



$\frac{R_{G_2} \times V_{DD}}{R_{G_1} + R_{G_2}} = 2V$

In this, how do we connect V_{in}?



$I_{DQ} = 1mA$

$V_{DQ} = V_{DD} - I_{DQ}R_D$

$V_{DQ} = 2.5V$

Q.Point (2.5V, 1mA)

After Aplying V_{in}

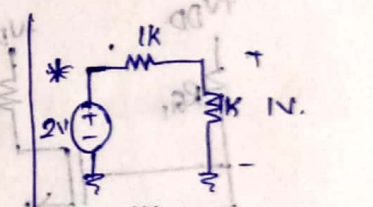
$\Rightarrow V_{GSQ} = V_{in}$

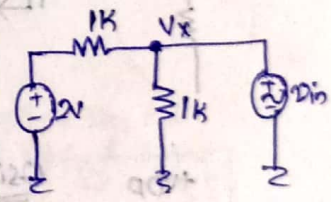
$\Rightarrow$ Q-point disturbed.

Since dc current is flowing through voltage source V_{in}.

$\Rightarrow$ this means we have to block dc current flowing into voltage source V_{in}.

$\Rightarrow$ Basically capacitor blocks 'dc' & allows 'ac'.

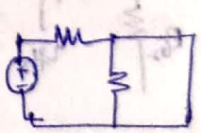




using superposition

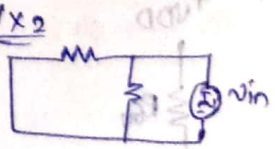
$V_x = V_{x_1} + V_{x_2}$

V_{x_1}



$\Rightarrow V_{x_1} = 1V$

V_{x_2}



$\Rightarrow V_{x_2} = V_{in}$

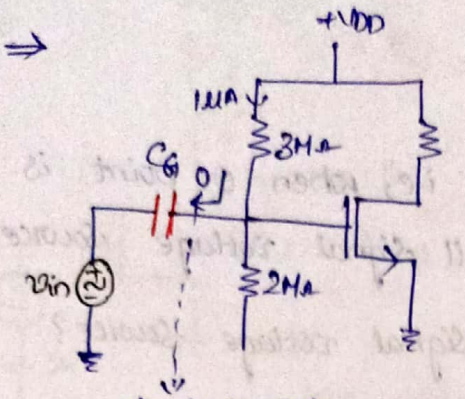
$\Rightarrow V_x = 0 + V_{in}$

$= V_{in}$

1 V dc is disturbed.

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⇒



Coupling :- which connects v_{in} with the circuit Amplifier.

⇒ Hence Q. point will not get disturbed.

∴ $V_{GSQ} = 2V \Rightarrow I_{DQ} = 1mA$

$\Rightarrow V_{DQ} = 25V.$

NO dc current flows through coupling capacitor.

⇒ The value of coupling capacitor 'C_G' is taken such that it acts as short circuit for the i/p frequencies of our intrest

DC - O.P

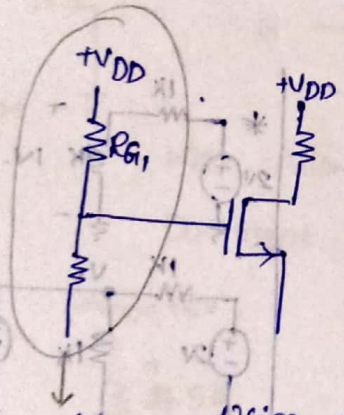
A.C - S.C

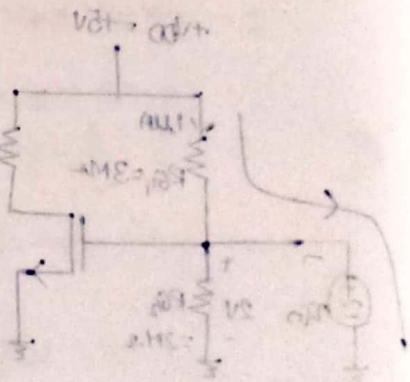
let $C = 100\ \mu F$

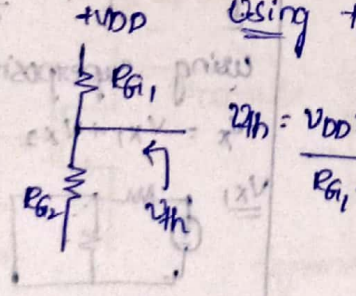
$f = 1\ KHz$

$$Z_c = \frac{1}{j\omega C} \qquad \omega = 2\pi f$$

$$|Z_c| = \frac{1}{2\pi f.C} = \frac{1}{2\pi \times 10^3 \times 100 \times 10^{-6}} = \frac{10}{2\pi} = 1.59$$

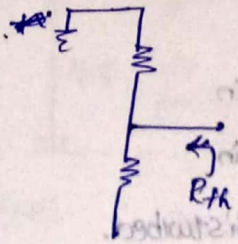




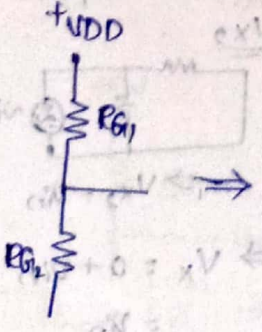


Using thevenin.

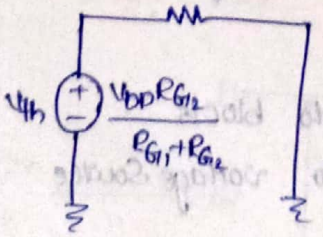
$$V_{th} = \frac{V_{DD} \times R_{G2}}{R_{G1} + R_{G2}}$$



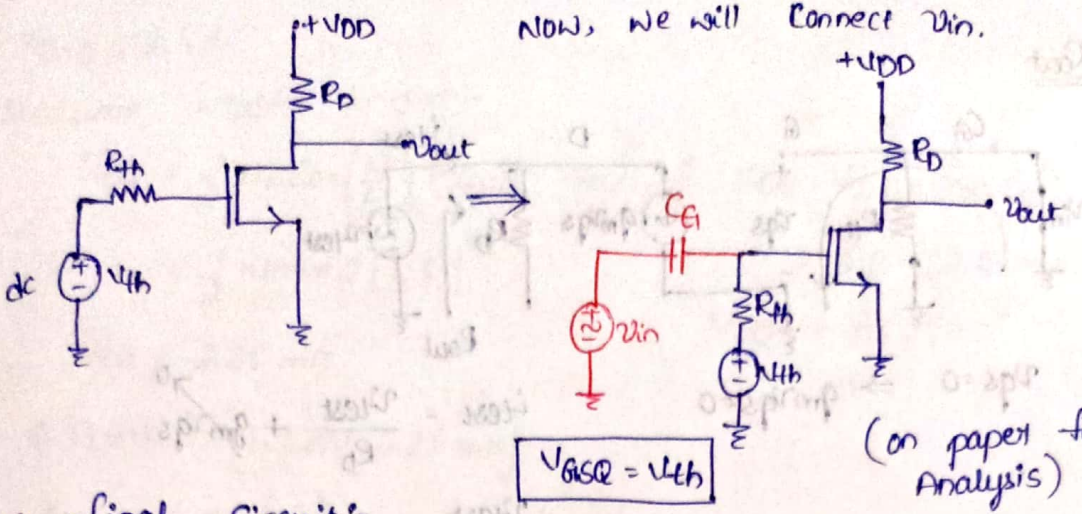
$R_{th} = R_{G1} // R_{G2}$



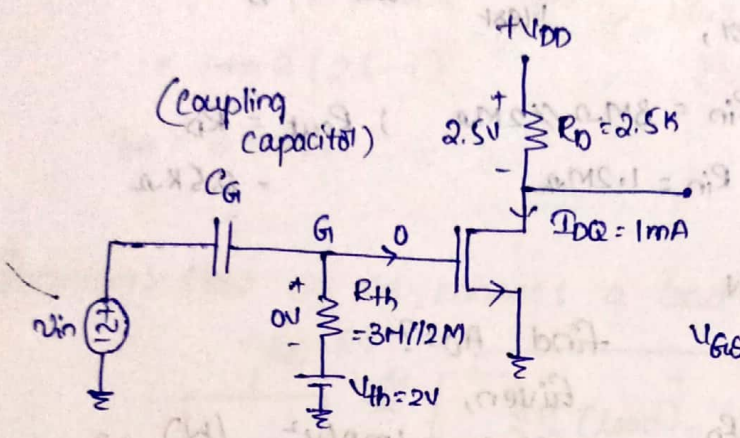
$R_{th} = R_{G1} // R_{G2}$



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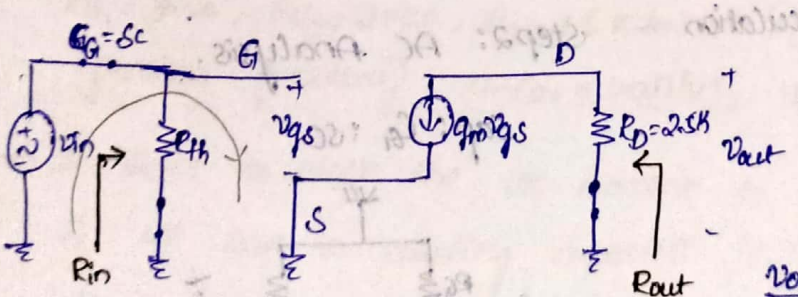
Now final Circuit:-



Small Signal gain A_v = ?

Apply AC Analysis:-

The value of C_G taken such that it is shorted for i/p freq. of our intrest.



$-V_{in} + V_{gs} = 0$

$V_{in} = V_{gs}$

$V_{out} = -g_m V_{gs} R_D$

$\frac{V_{out}}{V_{in}} = A_V = -g_m R_D$

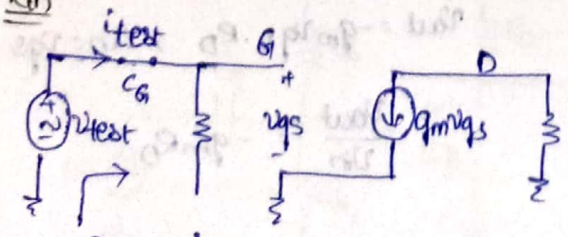
Now, $g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{GSQ} - V_{th})$

$g_m = 1m \times 2 \times (2V - 1) \Rightarrow g_m = 2mA/V$

$\Rightarrow A_V = -2 \times 2.5$

$A_V = -5\ V/V$

Rin

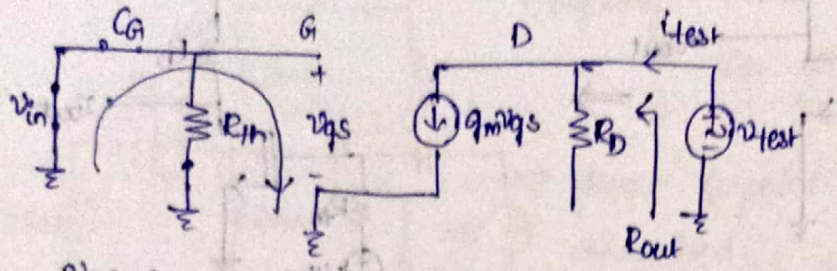


$R_{in} = \frac{V_{test}}{i_{test}} = R_{th} = R_{G_1} // R_{G_2}$

$\Rightarrow$ In order to have higher i/p small signal res. we take R_{G_1} & R_{G_2} in Mega ohms.

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R_{out}



$v_{gs} = 0 \Rightarrow g_m v_{gs} = 0$

$i_{test} = \frac{v_{test}}{R_D} + g_m v_{gs}$ ($g_m v_{gs} \to 0$)

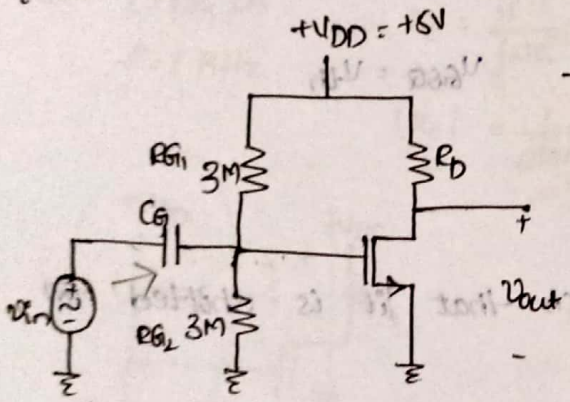
$R = \frac{v_{test}}{i_{test}} = R_{out} = R_D$

$\Rightarrow$ For above Amplifier,

$A_v = -5$ v/v ; $R_{in} = 3M\Omega // 2M\Omega$; $R_{out} = R_D$

$R_{in} = 1.2M\Omega$ $= 2.5K\Omega$

Question:-



find A_v = ?

Given,

$\mu_n C_{ox} = 1mA/V^2$, $\left(\frac{W}{L}\right)_n = 2$

$V_{tn} = 1V$, $R_D = 1.5K\Omega$

* The value of C_G is taken such that it acts as short circuit

Sol: Step 1: Q. Point calculation

$\Rightarrow$ DC Analysis

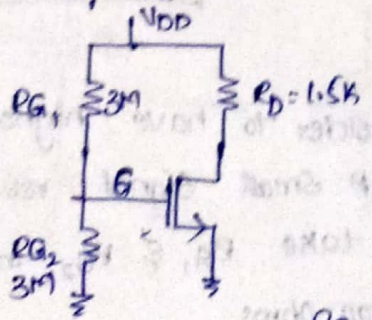
$\Rightarrow$ Q. Point:

DC Analysis:-

for DC: $\omega = 0$

$\Rightarrow |Z_c| = \frac{1}{0.C} = \infty$

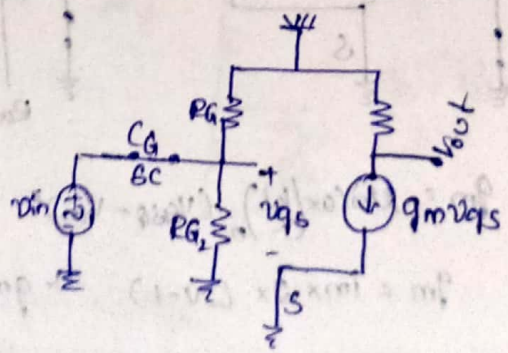
$\Rightarrow$ cap: C_G = O.C



$V_{GSQ} = V_{GQ} = \frac{R_{G_2}}{R_{G_1} + R_{G_2}} \times V_{DD}$

Step 2: AC Analysis.

cap: C_G : SC



$v_{out} = -g_m v_{gs} \cdot R_D$; $v_{in} = v_{gs}$

$\frac{v_{out}}{v_{in}} = -g_m R_D$

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$V_{GSQ} = 2.5V$

Assume Mosfet in sat :-

$$I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSQ} - V_{th})^2 \quad \& \quad V_{DQ} = V_{DD} - (I_{DQ} R_D)$$

$$= \frac{1}{2} \times 1m \times 2 [1.5]^2 \qquad = 5V - [2.25m \times 1.5K]$$

$I_{DQ} = 2.25\ mA$ $\qquad V_{DQ} = 1.625V$

Q. Point = $[1.625V, 2.25\ mA]$

$$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GSQ} - V_{th})$$

$$= 1m \times 2 (2.5 - 1)$$

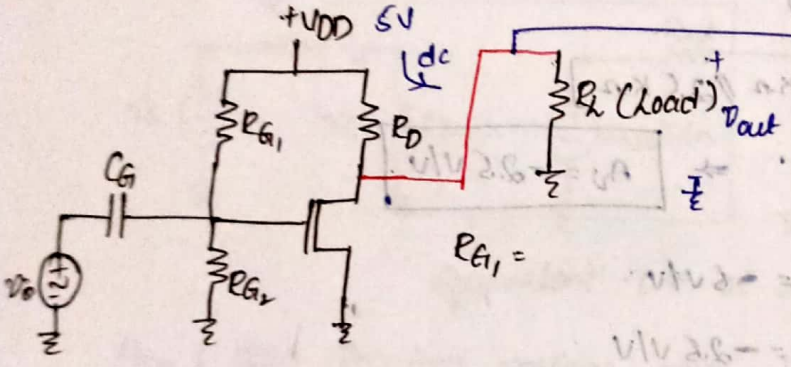
$g_m = 3\ mA/V$

Now,

$$A_V = \frac{v_{out}}{v_{in}} = -g_m R_D = 3mA/V \times 1.5K$$

$$\boxed{A_V = 4.5\ V/V}$$

Question:- How do we connect a load to an Amplifier.



this connection will draw some current into load R_L.

$\Rightarrow I_{DQ}$ disturbs

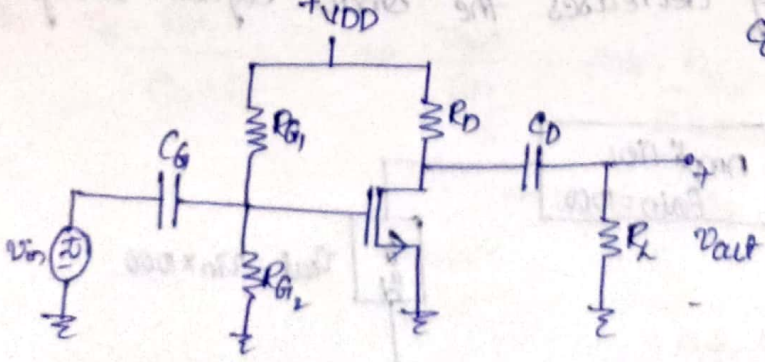
$\Rightarrow$ Q. Point disturbs.

$R_{G_1} = 3M\Omega$, $R_{G_2} = 2M\Omega$, $R_D = 2.5K\Omega$ $\Rightarrow I_{DQ} = 1\ mA$ & $V_{DQ} = 2.5V$ $\quad g_m = 2mA/V$

(previous problem) $\mu_n C_{ox} = 1mA/V^2$, $V_{th} = 1V$ & $\left(\frac{W}{L}\right)_n = 2$.

$\Rightarrow$ In order to block the dc current to pass through load R_L we use a coupling capacitor 'C_D' which intern blocks dc & allows ac.

$\Rightarrow$ the ckt will be



C_G & C_D $\Rightarrow$ Coupling capacitors.

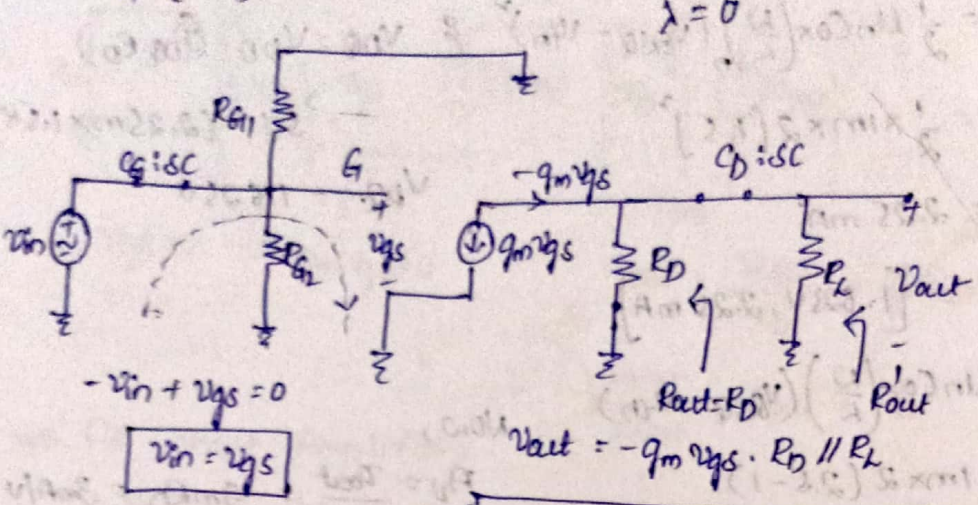
Here C_G & C_D values are chosen that they are shorted for our freq. of interest.

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find A_v :-

C_G & C_D are SC.

$\lambda = 0$



$-v_{in} + v_{gs} = 0$

$\boxed{v_{in} = v_{gs}}$

$v_{out} = -g_m v_{gs} \cdot R_D // R_L$

$$\boxed{\frac{v_{out}}{v_{in}} = A_v = -g_m (R_D // R_L)}$$

Let $R_L = 2.5\,K\Omega$

$A_v = -g_m (R_D // R_L)$

$= -2mA/v\ [2.5K\Omega // 2.5K\Omega]$

$A_v = -2m\ [1.25K]$ $\Rightarrow$ $\boxed{A_v = -2.5\ v/v}$

without R_L $\Rightarrow$ $A_v = -6\ v/v$

with R_L $\Rightarrow$ $A_v = -2.6\ v/v$

$\Rightarrow$ A_v decreases because of loading.

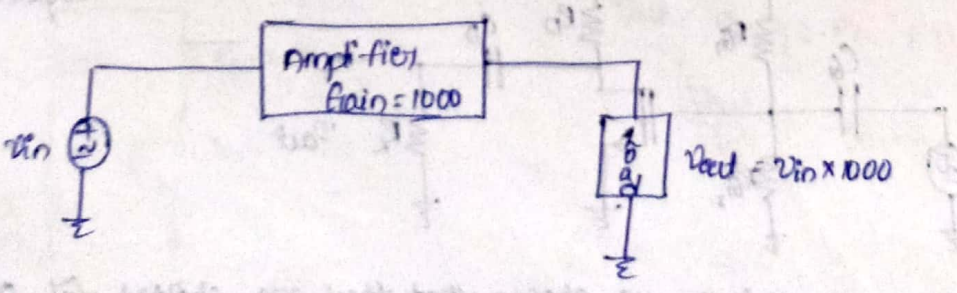
$\Rightarrow$ Amplifier o/p resistance R_{out} has come in parallel with R_L.

$R'_{out} = R_{out} // R_L = R_D // R_L = 2.5K // 2.5K$

$= 1.25K\Omega$.

Therefore loading decreases the small signal voltage gain.

*



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By observation: Without $R_L \Rightarrow R_L = \infty \Rightarrow A_v = -5\ v/v$

With $R_L = 2.5K\Omega \Rightarrow A_v = -2.5\ v/v$

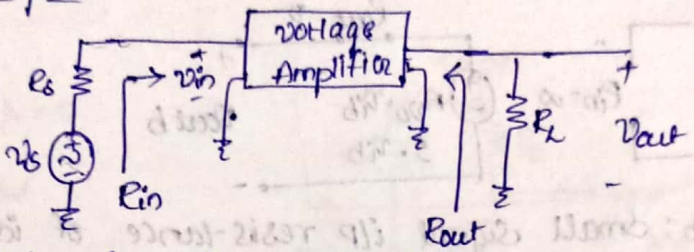
This decrease in A_v is because of loading.

How to avoid loading? (Avoid reducing gain)

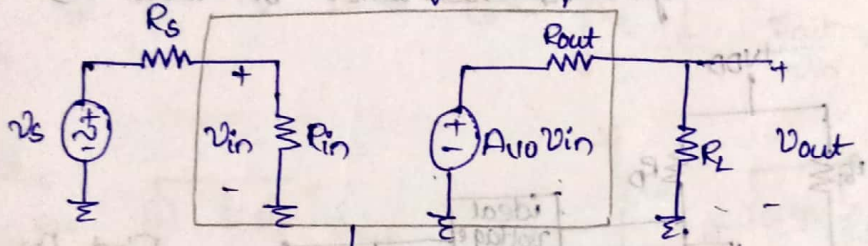
It can be done using ideal voltage Buffer.

Equivalent ckt of ideal voltage Buffer.

Voltage Amplifier



Equivalent ckt of voltage Amplifier.



Equivalent ckt of a voltage Amplifier.

A_{vo} : open circuited voltage gain (means $R_L = \infty$)

$$A_{vo} = \frac{v_{out}}{v_{in}}\Big|_{@ R_L = \infty}$$

$$v_{out} = A_{vo} \cdot v_{in} \times \frac{R_L}{R_{out} + R_L}$$

$$\boxed{A_v = \frac{v_{out}}{v_{in}} = A_{vo} \cdot \frac{R_L}{R_{out} + R_L}} \Rightarrow \text{if } R_L = \infty \Rightarrow \boxed{A_v = A_{vo}}$$

$$v_{in} = v_s \cdot \frac{R_{in}}{R_{in} + R_s} \Rightarrow \frac{v_{out}}{v_{in}} = A_{vo} \cdot \frac{R_L}{R_L + R_{out}}$$

$$\Rightarrow v_{out} = A_{vo} \cdot \frac{R_L}{R_L + R_{out}} \cdot v_{in}$$

$$= A_{vo} \cdot \frac{R_L}{R_L + R_{out}} \cdot \frac{v_s \cdot R_{in}}{R_{in} + R_s}$$

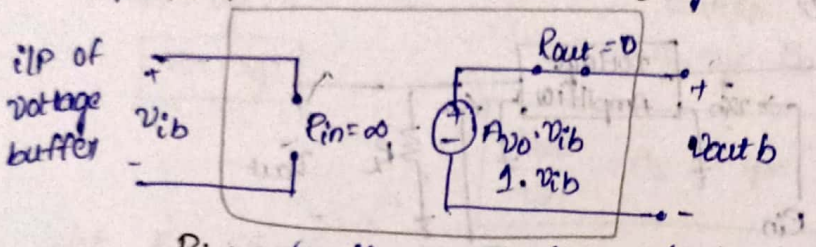
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$$\Rightarrow A_{vs} = \frac{v_{out}}{v_s} = A_{vo} \cdot \frac{R_L}{R_L + R_{out}} \cdot \frac{R_{in}}{R_{in} + R_s}$$

* For a good voltage Amplifier : $R_{in} >> R_s$ & $R_{out} << R_L$

Ideally $R_{in} = \infty$; $R_{out} = 0$ → voltage Amplifier.

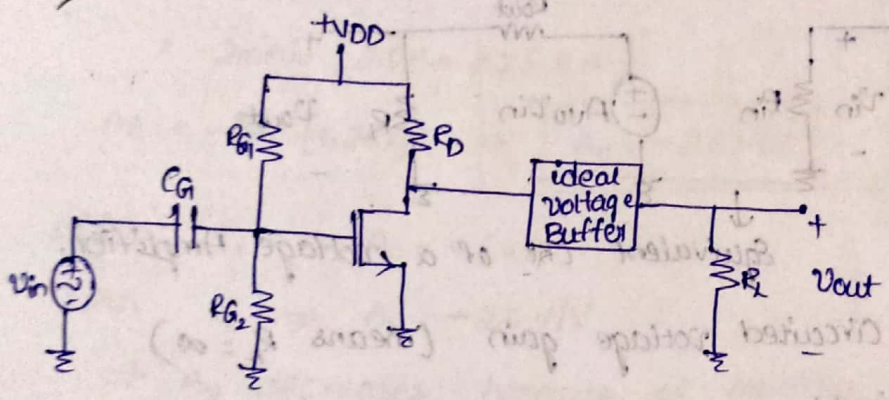
* Equivalent Ckt of ideal voltage Buffer [$A_v = 1$]



R_{inb} : Small signal i/p resistance of ideal V.B

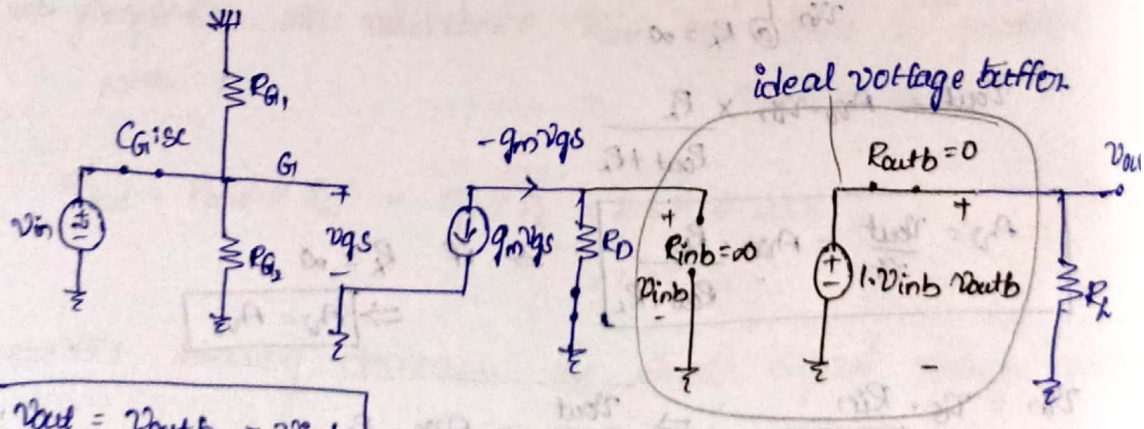
R_{outb} : Small signal o/p resistance of ideal V.B

$\Rightarrow$



Find A_v.

Sol:-



$v_{out} = v_{outb} = v_{inb}$

$v_{in} = v_{gs}$

$v_{inb} = -g_m v_{gs} R_D$

$\Rightarrow v_{out} = -g_m v_{gs} R_D$

$\Rightarrow \frac{v_{out}}{v_{in}} = -g_m R_D = -2m \times 2.5K$

[A_v not depending on R_L i.e., avoiding loading]

$\frac{v_{out}}{v_{in}} = A_v = -5\,V/V.$

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⇒ In order to avoid loading, we have to use voltage Buffer.

⇒ CD configuration acts as voltage Buffer.

15/2/22

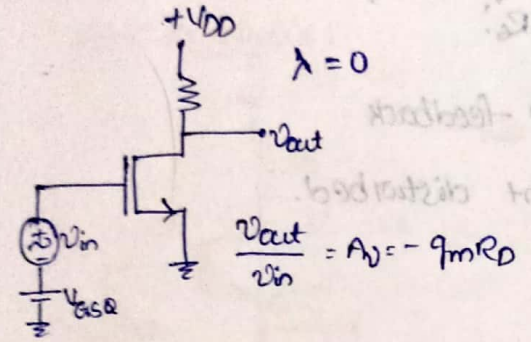
Coupling Capacitor: Blocks dc & Allows AC

⇓

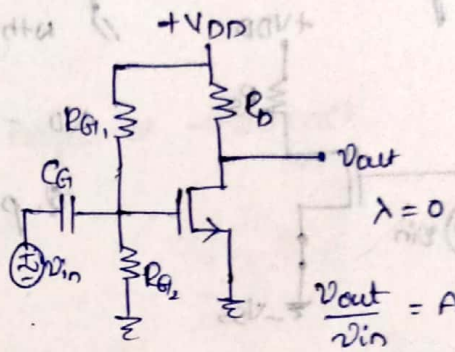
Q.point does not disturbed.

(Q.point is stable).

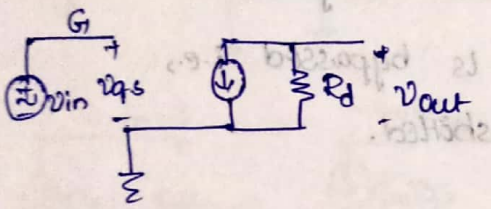
Recap

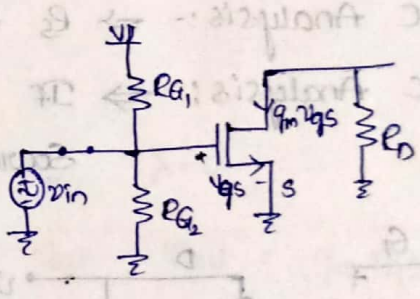


$\frac{V_{out}}{V_{in}} = A_V = -g_m R_D$

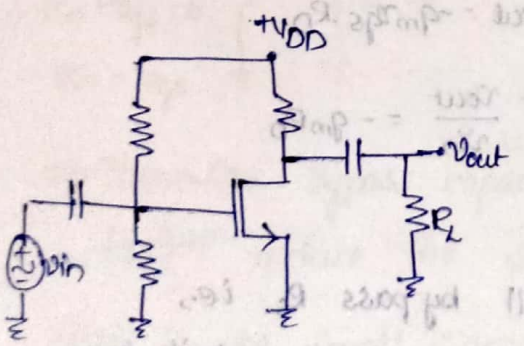


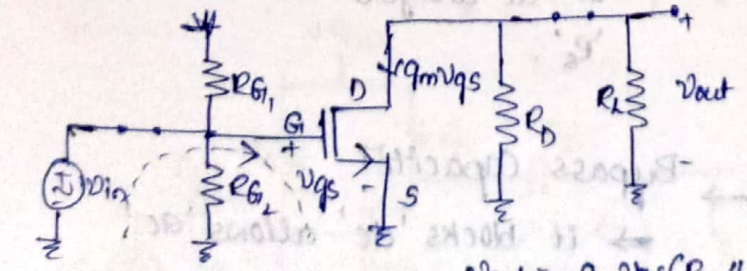
$\frac{V_{out}}{V_{in}} = A_V = -g_m R_D$





$V_{in} = V_{gs}$.





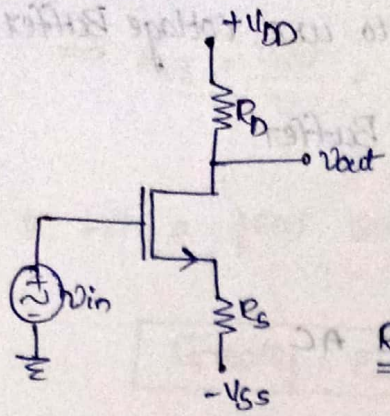
$-V_{in} + V_{gs} = 0$

$V_{gs} = V_{in}$

$V_{out} = -g_m V_{gs} (R_D \| R_L)$

$\frac{V_{out}}{V_{in}} = A_V = -g_m (R_D \| R_L)$

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$$A_v = \frac{-g_m R_D}{1 + g_m R_S}$$

here $A_v \downarrow$ due to -ve feedback.

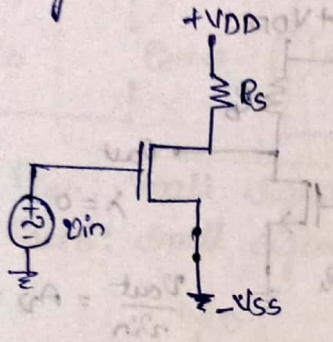
provided by 'R_S'

R_S : (i) Gives -ve feedback.

(ii) Stable Q. point.

→ What should be done so as not to disturb & decrease the gain?

By keeping a bypass capacitor C_S in // with 'R_S'.

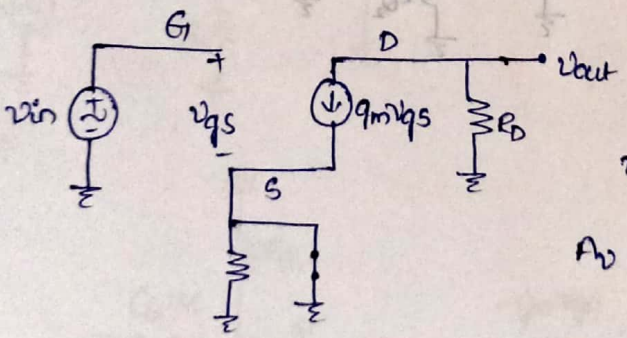


No -ve feedback

Q. point disturbed.

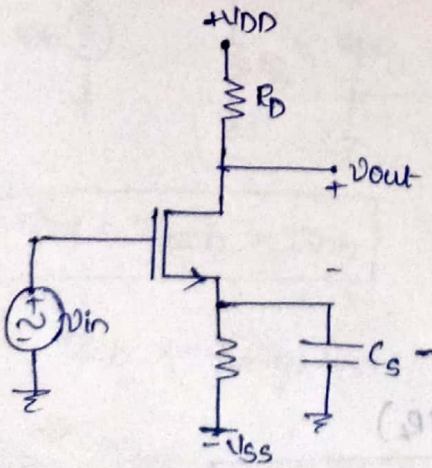
In DC Analysis :- ⇒ R_S should be present.

In AC Analysis : ⇒ If R_S is bypassed i.e., Source shorted.



$$V_{out} = -g_m V_{gs} . R_D$$

$$A_v = \frac{V_{out}}{V_{in}} = -g_m R_D$$



C_S will bypass R_S i.e., in ac analysis we don't have 'R_S'.

Bypass capacitor

⇒ it blocks 'dc' allows 'ac'

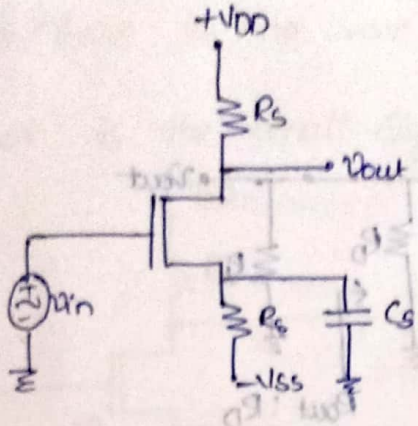
⇒ R_S It bypasses 'R_S'

⇒ A_v doesn't decrease.

→ It doesn't change Q. point.

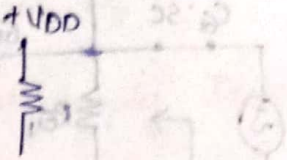
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Question:- Is there any negative feedback for DC?



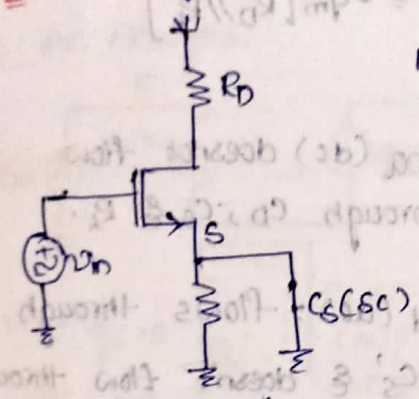
Sol:- DC Analysis:

C_S : OC, V_{in} : SC

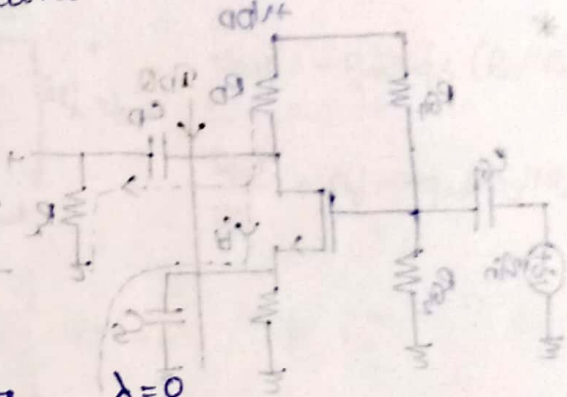


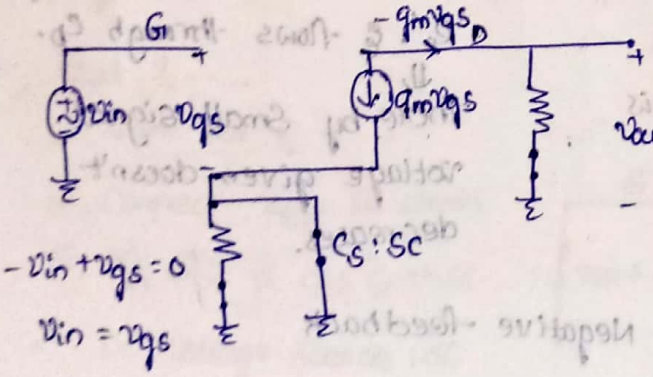
Yes, negative feedback is present.

AC Analysis:



No negative feedback





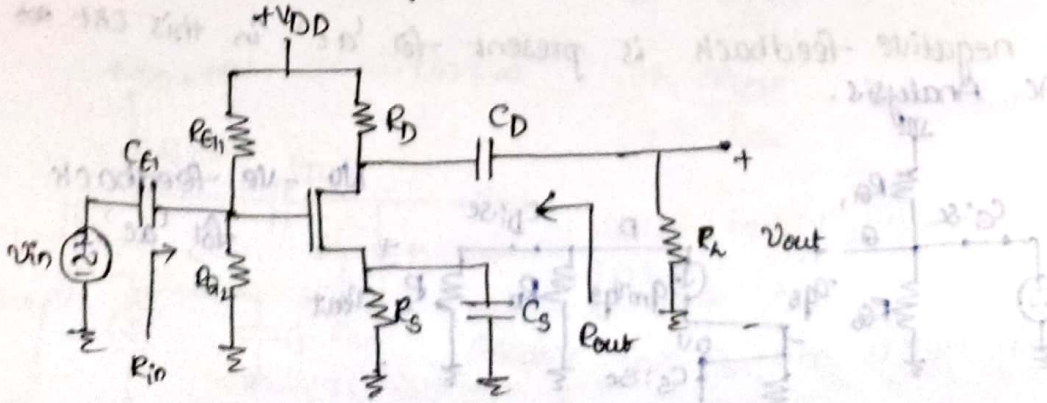
$\lambda = 0$

$V_{out} = -g_m v_{gs} \cdot R_D$

$\frac{V_{out}}{V_{in}} = A_V = -g_m R_D$

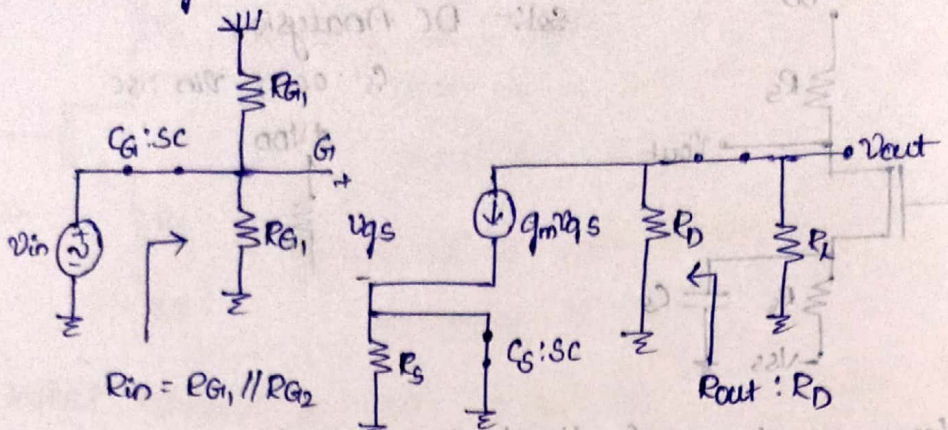
⇒ Therefore Bypass capacitor 'C_S' bypasses 'R_S' which intern doesn't reduce the small signal voltage gain A_V.

What is the Small Signal voltage gain A_V?



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Sol:- AC Analysis:-



$R_{in} = R_{G_1} // R_{G_2}$

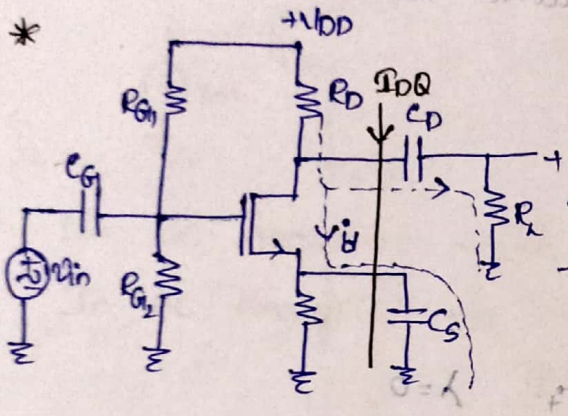
$R_{out} : R_D$

$v_{in} = v_{gs}$

$v_{out} = -g_m v_{gs} [R_D // R_L]$

$$A_v = \frac{v_{out}}{v_{in}} = -g_m [R_D // R_L]$$

*



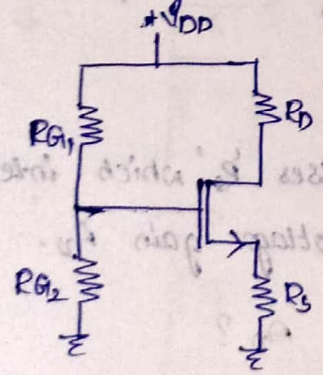
⇒ I_{DQ} (dc) doesnot flow through C_D; C_S & R_L.

⇒ i_d (ac): flows through 'C_S' & doesn't flow through 'R_S'. & flows through C_D.

∴ there by Small signal voltage given doesn't decreases.

Q: Is Negative feedback is present for DC?

Sol: DC Analysis:



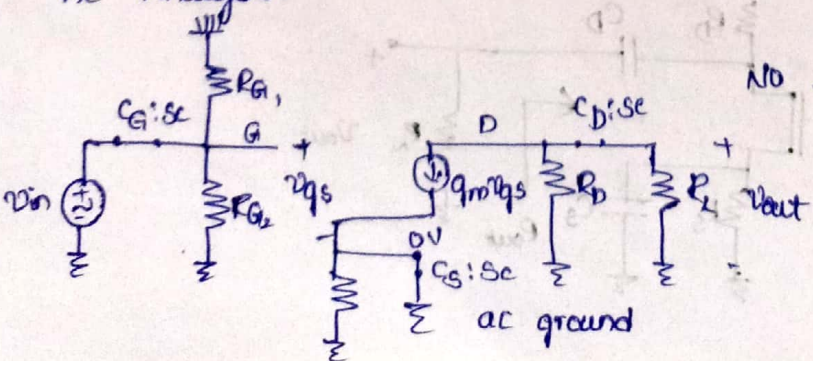
Yes, Negative feedback is present.

Here 'R_S' provides -ve feedback

⇒ Stable Q. point.

Q. Is negative feedback is present for 'ac' in this CKt.

AC Analysis.



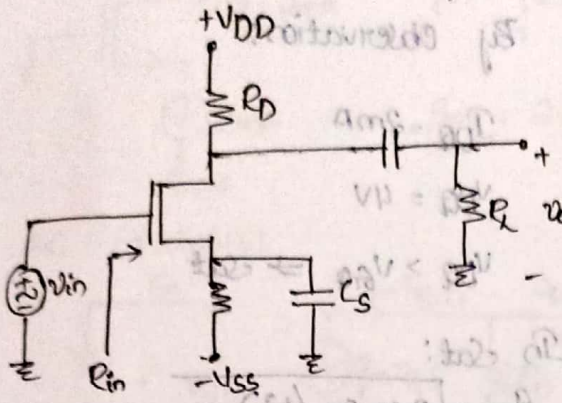
No -ve feedback for 'ac'.

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Here R_S is bypassed. No current flows through 'R_S'.

$\Rightarrow$ There is no -ve feedback for ac.

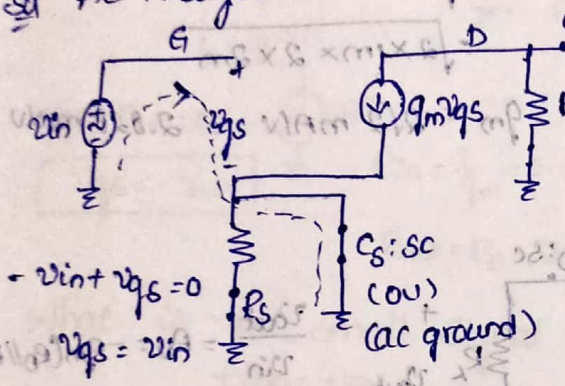
What is the small signal voltage gain A_v?



Dual Supply Design.

Assume C_D & C_S are shorted for our frequencies of intrest.

AC Analysis:



$v_{out} = -g_m v_{gs} (R_D // R_L)$

$\frac{v_{out}}{v_{in}} = A_v = -g_m (R_D // R_L)$

Rout ?

i, take out 'R_L'

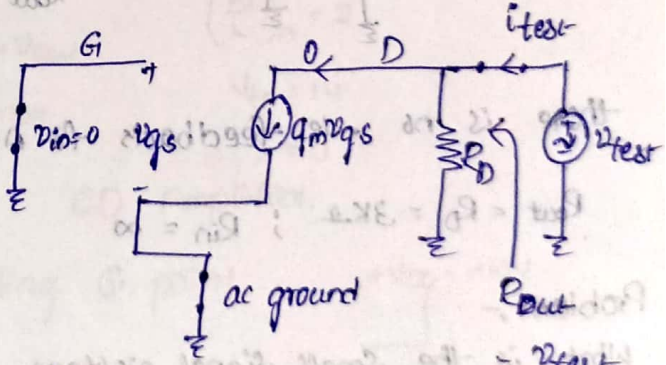
ii, Connect v_{test} @ drain

iii, $v_{in} \Rightarrow$ SC & C_D & $C_S \Rightarrow$ SC

iv, DC voltage sources : SC

DC current " : OC

v, Replace MOSfet with small signal model.

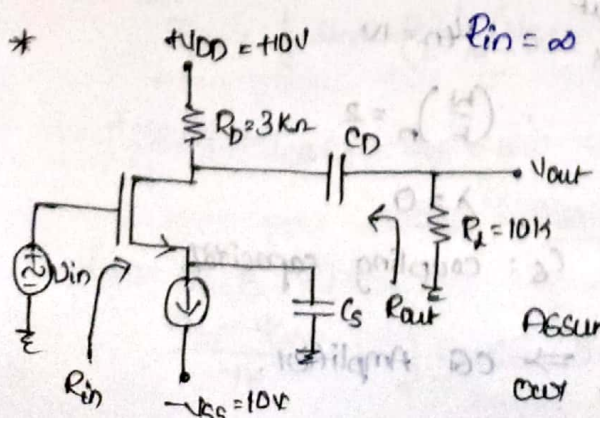


$R_{out} = \frac{v_{test}}{i_{test}}$

$v_{gs} = 0 \Rightarrow g_m v_{gs} = 0$

$\Rightarrow i_{test} = \frac{v_{test}}{R_D}$

$\Rightarrow \frac{v_{test}}{i_{test}} = R_D = R_{out}$

* 

$R_{in} = \infty$

$\mu_n C_{ox} = 1mA/V^2$, $V_{tn} = 1V$,

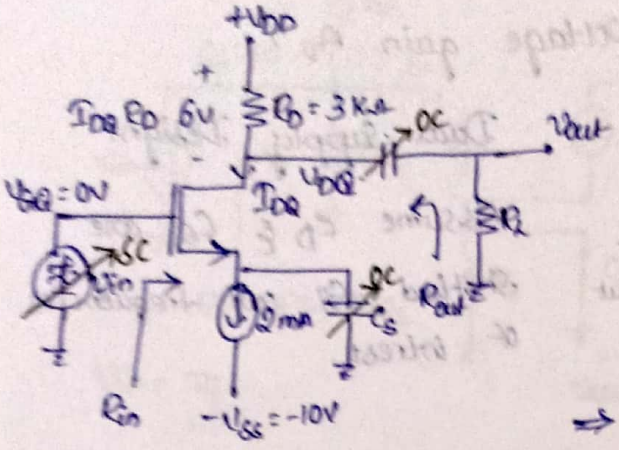
$\left(\frac{W}{L}\right)_n = 2$ $\lambda = 0$

Assume C_D & C_S are shorted for our freq. of intrest.

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Sol:- First, we have to find Q.point

This is done using DC Analysis ⇒ CS & CD : OC & Vin : SC



By observation:

$I_{DQ} = 2mA$

$V_{DQ} = 4V$

$V_{DQ} > V_{GQ} \Rightarrow$ sat

⇒ In sat:

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_n I_{DQ}}$$

$$= \sqrt{2 \times 1m \times 2 \times 2m}$$

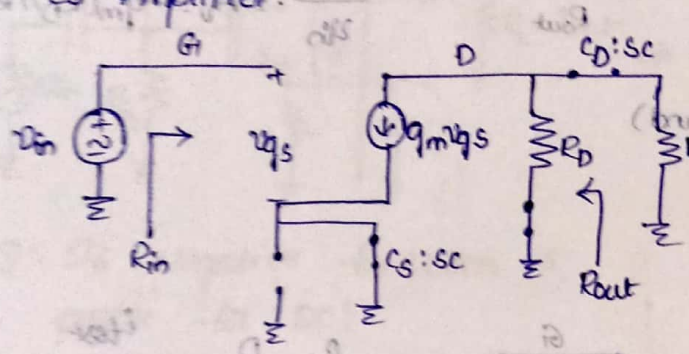
$$g_m = 2\sqrt{2}\ mA/V = 2.828\ mA/V$$

for finding A_V:

AC Analysis:

2mA dc (C.S) → 0.C

CS Amplifier.



$\frac{V_{out}}{V_{in}} = A_V = -g_m(R_D // R$

$= -2.828(3k // 0$

$A_V = -6.526\ V/V$

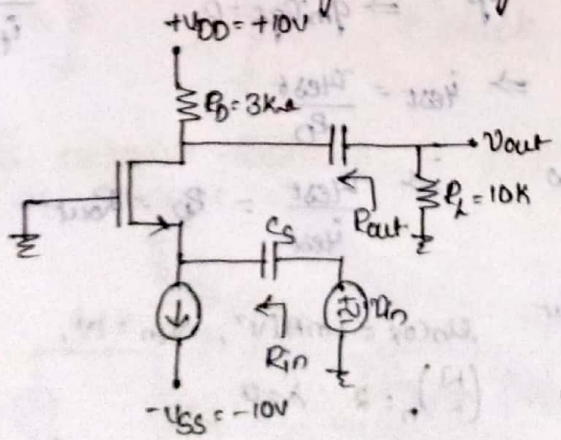
i/p & o/p are 180° out of phase.

there is no -ve feedback for AC.

$R_{out} = R_D = 3K\Omega$; $R_{in} = \infty$

Problem:-

What is the Small Signal voltage gain A_V.



$\mu_n C_{ox} = 1mA/V^2$

$V_{tn} = 1V$

$\left(\frac{W}{L}\right)_n = 2$

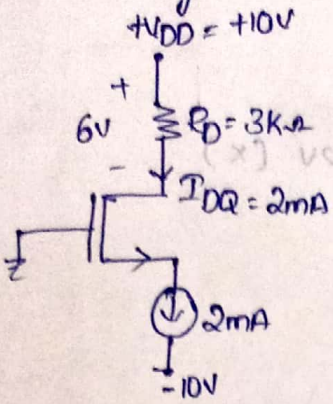
$\lambda = 0$.

C_S : coupling capacitor.

i/p @ S & o/p @ drain ⇒ CG Amplifier.

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DC Analysis:



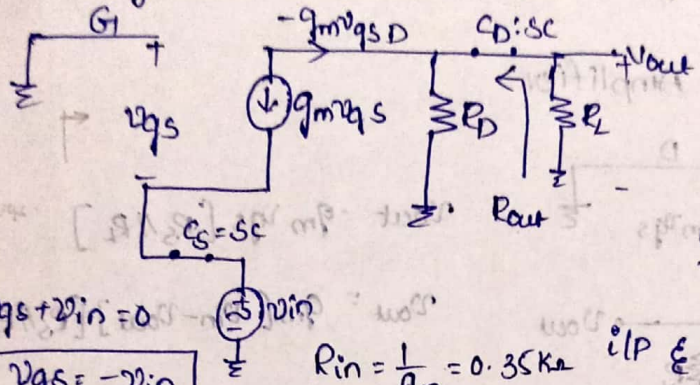
$V_{DQ} = 4V > (V_{GQ} = 0V)$

$\Rightarrow$ Sat

$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_n I_{DQ}}$

$g_m = 2.828\ mA/V.$

AC Analysis:



$v_{gs} = -v_{in}$

$R_{in} = \frac{1}{g_m} = 0.35K\Omega$

$R_{out} = R_D = 3K\Omega$

$v_{out} = -g_m v_{gs}(R_D // R_L)$

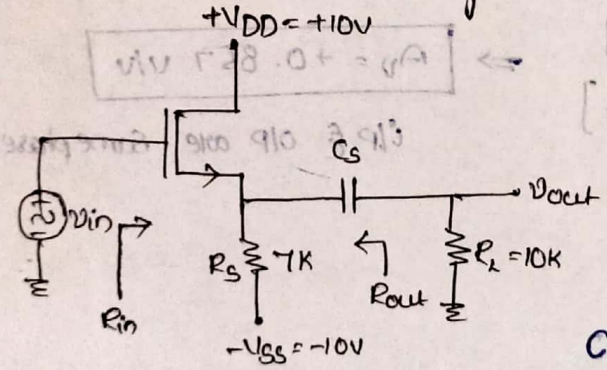
$v_{out} = g_m v_{in}(R_D // R_L)$

$\frac{v_{out}}{v_{in}} = g_m(R_D // R_L) = A_v$

i/p & o/p are same phase.

$A_v = +6.526\ V/V$

What is the small signal voltage gain A_v.



$\mu_n C_{ox} = 0.5mA/V^2$

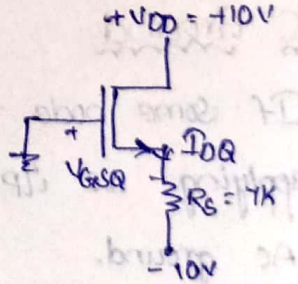
$\left(\frac{W}{L}\right)_n = 2$

$V_{tn} = 1V$

$\lambda = 0$

CD Amplifier.

Sol:- DC Analysis for finding Q. point



$C_S = OC$, $v_{in} = SC$

$V_G = 0V$, $V_D = 10$ $\Rightarrow$ saturation

In Sat:

$I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSQ} - V_{tn})^2 \rightarrow (1)$

$+V_{GSQ} + I_{DQ}R_S - V_{SS} = 0$

$I_{DQ} = \frac{V_{SS} - V_{GSQ}}{R_S} \rightarrow (2)$

from (1) & (2)

$\frac{10V - V_{GSQ}}{7K} = \frac{1}{2} \times 0.5m \times 2\,[V_{GSQ} - 1]^2$

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$$20V - 2V_{GSQ} = 7\left[V_{GSQ}^2 - 2V_{GSQ} + 1\right]$$

$$7V_{GSQ}^2 - 12V_{GSQ} - 13 = 0$$

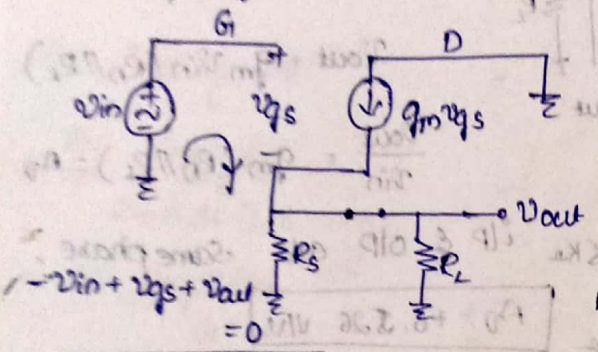
$$V_{GSQ} = 2.467V \;,\; -0.752V \;(\times)$$

$$\Rightarrow V_{GSQ} = 2.467V$$

$$I_{DQ} = \frac{V_{SS} - V_{GSQ}}{R_S} = \frac{10 - 2.467}{7k} = 1.07mA$$

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_n I_{DQ}} = \sqrt{2 \times 0.5m \times 2 \times 1.07m} = 1.46 \text{ mA/V}$$

AC Analysis: CD Amplifier:



$v_{out} = g_m v_{gs} [R_S // R_L]$

$v_{out} = g_m [v_{in} - v_{out}] [R_S // R_L]$

$$A_V = \frac{v_{out}}{v_{in}} = \frac{g_m(R_S // R_L)}{1 + g_m(R_S // R_L)}$$

$v_{gs} = v_{in} - v_{out}$

$$\Rightarrow A_V = \frac{1.46m\,[7K // 10K]}{1 + [1.46m(7K // 10K)]}$$

$$\Rightarrow \boxed{A_V = +0.857 \text{ V/V}}$$

i/p & o/p are same phase.

$R_{in} = \infty$

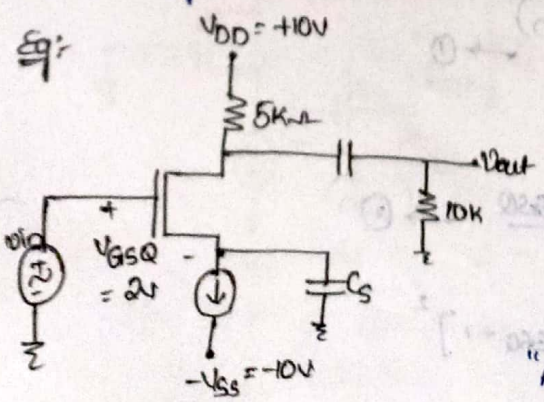
$R_{out} = R_L // R_S // \frac{1}{g_m} // R_S$

16/2/22

AC ground

→ If some node voltage is not varying even after applying ac i/p signal then it is known as an AC ground.

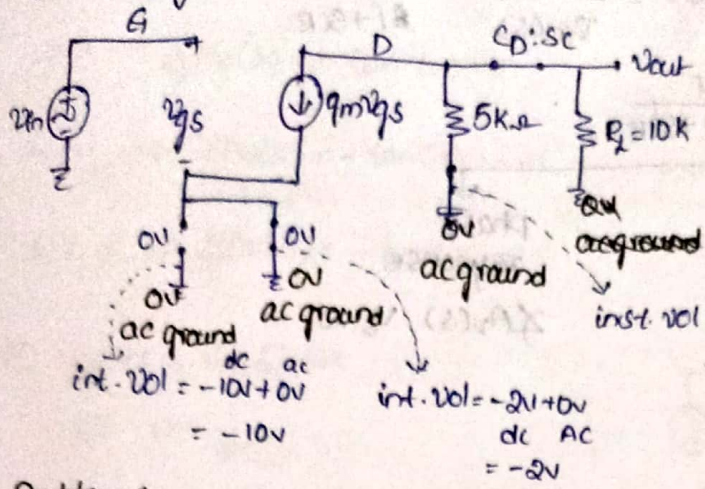
Eg:



Here V_{DD} node voltage = 10V not varying even after applying V_{in}(ac) That's why in ac analysis we will ground this node. Here this is an "Ac ground."

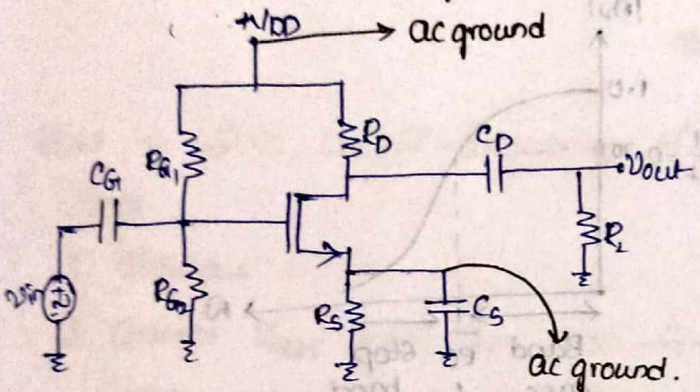
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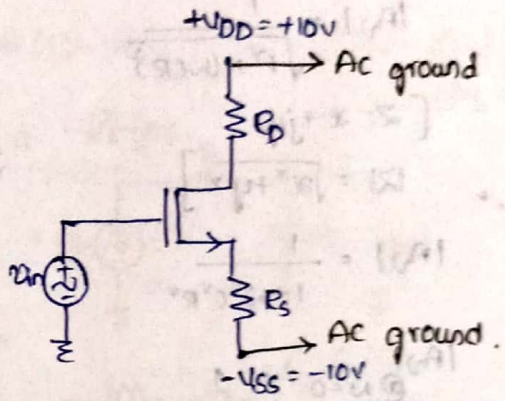
AC Analysis:-



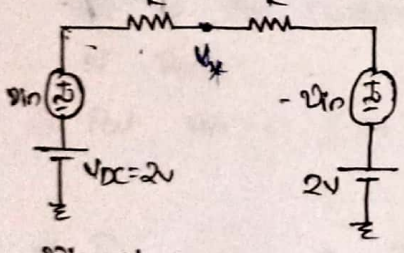
Problem:

Whic nodes are ac ground.





Problem:



$v_{in} = V_m \sin \omega t$

Is Node V_x an ac ground?

Apply Nodal at V_x:

$$\frac{V_x - (v_{in}+2)}{R} + \frac{V_x - (-v_{in}+2)}{R} = 0$$

$$\frac{2V_x}{R} - \frac{v_{in}}{R} - \frac{2V}{R} + \frac{v_{in}}{R} - \frac{2V}{R} = 0$$

$$V_x = \frac{2V+2V}{2} = 2V \Rightarrow V_x = 2V$$

'DC' ⇒ not varying

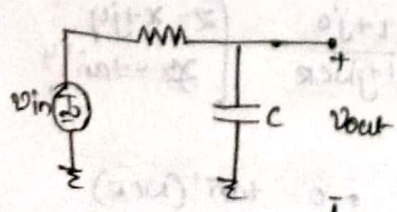
⇒ AC ground.

⇒ Even after applying 'ac' V_x is not varying.

⇒ Instantaneous voltage @ $V_x = 2V$.

R-C Circuits:

Low Pass Filter



$$Z_c(s) = \frac{1}{sC}$$

$s = j\omega$

$$v_{out}(s) = \frac{Z_c(s)}{R + Z_c(s)} v_{in}(s)$$

$$\frac{v_{out}(s)}{v_{in}(s)} = \frac{1/sC}{R + 1/sC} = \frac{1/sC}{\frac{1+sCR}{sC}}$$

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Transfer function (A) $A_v(s) = \frac{v_{out}(s)}{v_{in}(s)} = \frac{1}{1+sCR}$

$$A_v(s) = \frac{1}{1+sCR}$$

- Magnitude response: $|A_v|$ vs ω
- phase response: $\angle A_v(s)$ vs ω

Magnitude Response:

$$|A_v| = \frac{1}{|1+j\omega CR|}$$

$$|A_v| = \frac{1}{\sqrt{1^2+(\omega CR)^2}}$$

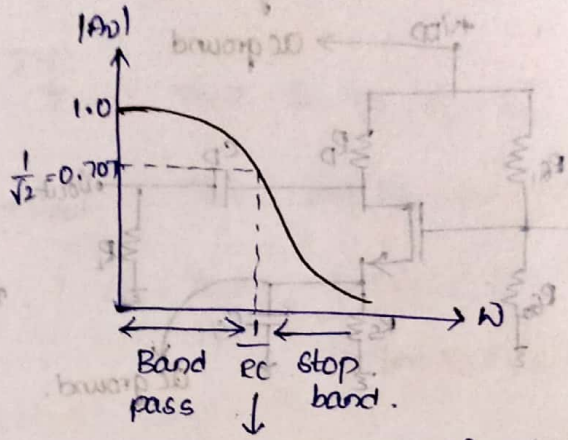
[$z = x+jy$, $|z| = \sqrt{x^2+y^2}$]

$$|A_v| = \frac{1}{1+\omega^2C^2R^2}$$

$|A_v|_{@\omega=0} = 1$ (dc)

$|A_v|_{@\omega=\frac{1}{RC}} = \frac{1}{\sqrt{1+\frac{1}{R^2C^2}\cdot R^2C^2}} = \frac{1}{\sqrt{2}}$

$|A_v|_{@\omega=\infty} = 0$



ω_H = cutoff frequency.

* As $\omega \uparrow \Rightarrow A_v \downarrow$

⇒ This is allowing low frequency signals & attuating high frequency singal.

⇒ low pass filter.

⇒ Cutoff frequency, $\omega_H = \frac{1}{RC}$ rad/sec

$f_H = \frac{1}{2\pi RC}$ Hz.

Phase Response

$\angle A_v$ vs ω $\quad A_v(s) = \frac{1}{1+sCR} \Rightarrow A_v(s) = \frac{1+j0}{1+j\omega CR}$ $\quad [z = x+jy,\ \angle z = \tan^{-1}\frac{y}{x}$

$$A_v(s) = \frac{1}{1+sCR} \Rightarrow \angle A_v(s) = \frac{\tan^{-1}(\frac{0}{1})}{\tan^{-1}(\frac{\omega CR}{1})} = 0 - \tan^{-1}(\omega CR)$$

$$\frac{1}{(1+j\omega CR)}$$

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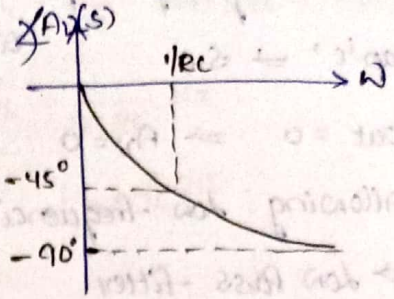
$\angle A_v(s) = -\tan^{-1} \omega CR$

$\omega = 0 \Rightarrow \angle A_v(s) = -\tan^{-1}(0) = 0$

$\omega = \frac{1}{RC} \Rightarrow \angle A_v(s) = -\tan^{-1}(1) = -45^\circ$

$\omega = \infty \Rightarrow \angle A_v(s) = -\tan^{-1}\infty = -90^\circ$

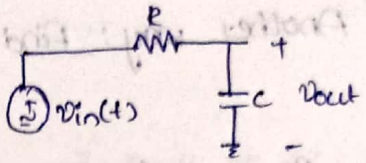
(pole, $s = -\frac{1}{RC}$; $\tan^{-1}(0) = 0$



* $v_{in}(t) = V_m \sin \omega t$

For $\omega = \frac{1}{RC}$

$v_{out}(t) = \frac{1}{\sqrt{2}} \cdot V_m \sin(\omega t - 45^\circ)$

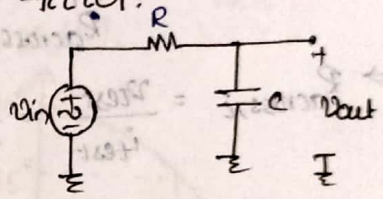


Generalized:

$v_{in}(t) = V_m \sin \omega_0 t$

$v_{out}(t) = |A_v|_{\omega=\omega_0} \cdot V_m \sin[\omega_0 t + \angle A_v|_{@\omega=\omega_0}]$

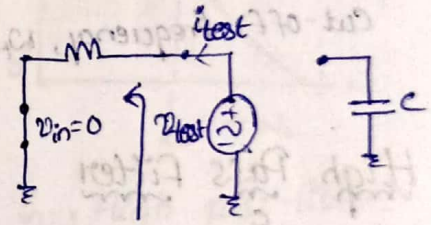
How to find cutoff frequency of a filter.



Steps:

1. Take out 'C'.
2. Connect v_{test} across the node from
3. where we want to find $R_{across,C}$.

i_{test} is the current carrying out of v_{test}.



$R_{across,C}$

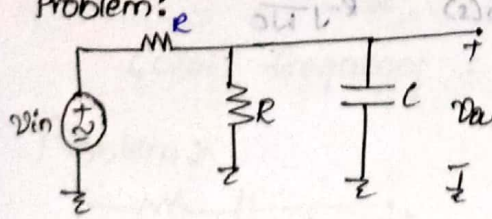
Small signal res. seen by capacitor.

3. Put $v_{in} = 0$ i.e., ac v.source = sc, ac c.source = oc.

4. $R_{across,C} = R = \frac{v_{test}}{i_{test}}$

5. Cutoff freq. $= \frac{1}{R_{across,C} \cdot C}$ rad/sec

Problem:

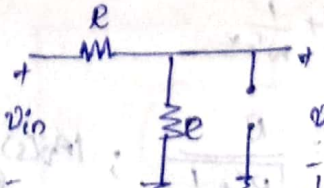


i, Whic filter?

ii, Find the cut-off frequency.

i, $\omega = 0$ (dc) → zero-frequency, low freq.

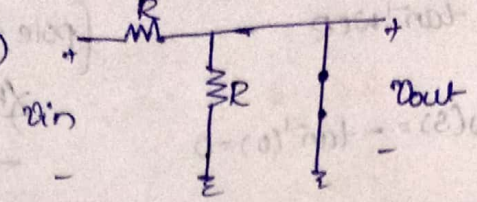
for dc ⇒ cap 'C' is OC



$A_v = \frac{v_{out}}{v_{in}} = \frac{R}{R+R} = \frac{R}{2R} = \frac{1}{2}$

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$\omega = \infty$ (very high-freq)



Cap 'c' ⇒ S.C

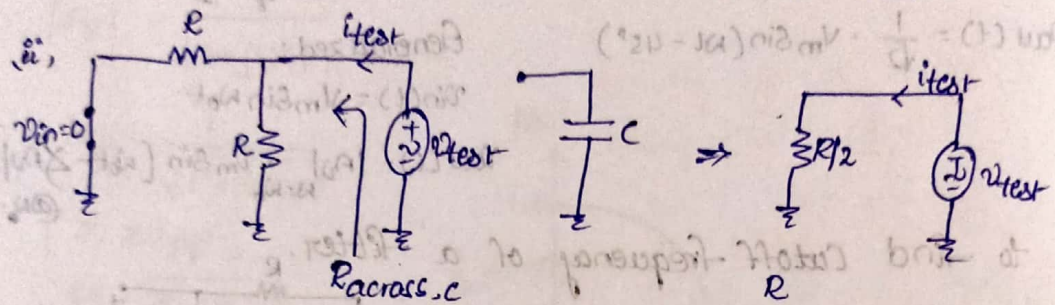
$v_{out} = 0 \Rightarrow A_v = 0$

⇒ Allowing low frequencies & Attuating high freq.

⇒ Low Pass filter.

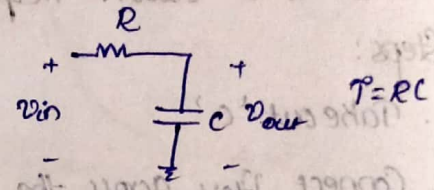
Note :- Another way : Find T.F(s) (or) $A_v(s)$ & then put $\omega = 0$ & $\omega = \infty$ in $|T.F(s)|$

ii)



$R_{across,C}$

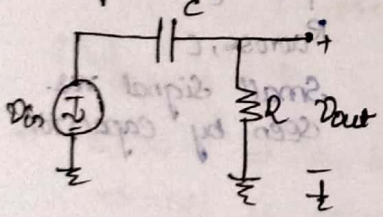
$\Rightarrow R_{across,C} = \frac{v_{test}}{i_{test}} = \frac{R}{2}$



$\tau = RC$

Cut-off frequency, $\omega_H = \frac{1}{R_{across,C} \cdot C} = \frac{1}{\frac{R}{2} \cdot C}$

High Pass Filter



$\frac{v_{out}(s)}{v_{in}(s)} = \frac{sCR}{1+sCR}$ (zero) (Pole)

$\frac{v_{out}(s)}{v_{in}(s)} = \frac{R}{R+\frac{1}{sC}}$

$T.F(s) = A_v = \frac{R}{R+\frac{1}{j\omega C}} \cdot \frac{j}{j}$ $\quad j = \pm$

$A_v(s) = \frac{v_{out}(s)}{v_{in}(s)} = \frac{R}{R - j\frac{1}{\omega C}}$

Magnitude Response

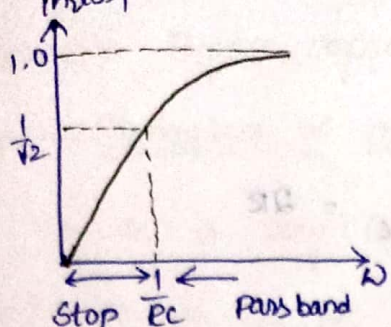
$|A_v(s)|$ Vs ω

$|A_v(s)| = \frac{R}{\sqrt{R^2 + \frac{1}{\omega^2 C^2}}}$

$|A_v(s)|_{@\omega=0 \text{ (dc)}} = \frac{R}{\sqrt{R^2 + \frac{1}{\omega^2 C^2}}}$; $|A_v(s)|_{@\omega=\frac{1}{RC}} = \frac{R}{\sqrt{R^2 + \frac{1}{R^2C^2} \cdot C^2}} = \frac{R}{\sqrt{2R^2}} = \frac{1}{\sqrt{2}}$

$|A_v(s)|_{@\omega=\infty} = \frac{R}{R} = 1$

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$\omega_L = \frac{1}{RC}$ rad/sec

$f_L = \frac{1}{2\pi RC}$ Hz

$\omega_L = f_L 2\pi$

ω_L = Lower cutoff frequency.

Phase Response

$\angle A_V(s)$ Vs ω

$A_V(s) = \frac{R}{R - j\frac{1}{\omega C}} = \frac{R+j0}{R - j\frac{1}{\omega C}}$

$z = x - jy \Rightarrow \angle z = -\tan^{-1} y/x$

$\Rightarrow \angle A_V(s) = 0 - \left(-\tan^{-1}\frac{1}{\omega CR}\right)$

$\angle A_V(s) = \tan^{-1}\frac{1}{\omega CR}$

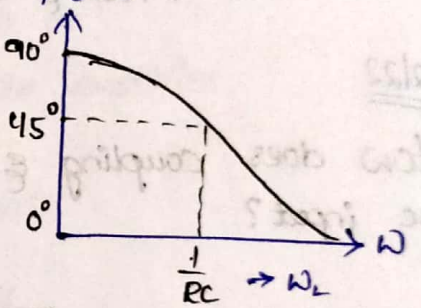
$\angle A_V(s) = \frac{\tan^{-1}\left(\frac{0}{R}\right)}{\tan^{-1}\left(\frac{\frac{1}{\omega C}}{R}\right)} = \frac{0^\circ}{-\tan^{-1}\frac{1}{\omega R}}$

$\omega = 0 \Rightarrow \angle A_V(s) = \tan^{-1}(\infty) = 90^\circ$

$\omega = \infty \Rightarrow \angle A_V(s) = \tan^{-1}(0) = 0^\circ$

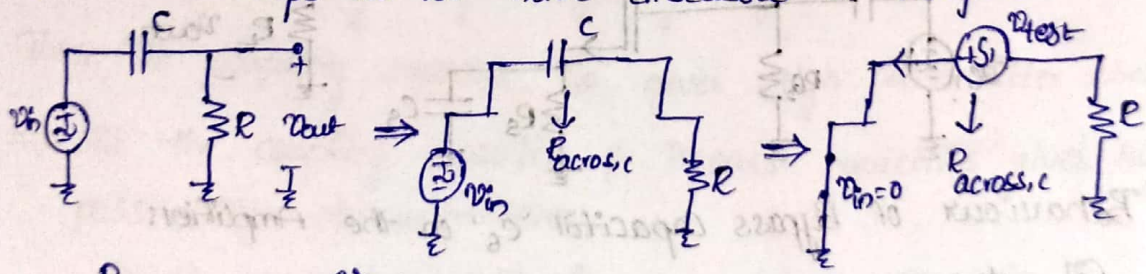
$\omega = \frac{1}{RC} \Rightarrow \angle A_V(s) = \tan^{-1}(1) = 45^\circ$

$|A_V(s)|$



How do we find cutoff frequency in high pass filter?

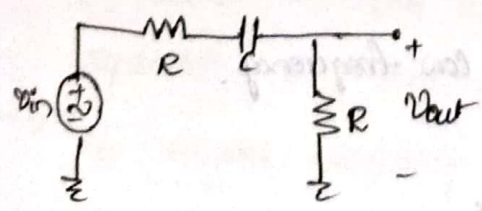
Sol:- Same steps as we have discussed in lowpass filter.



$R_{across,C} = \frac{v_{test}}{i_{test}} = R$

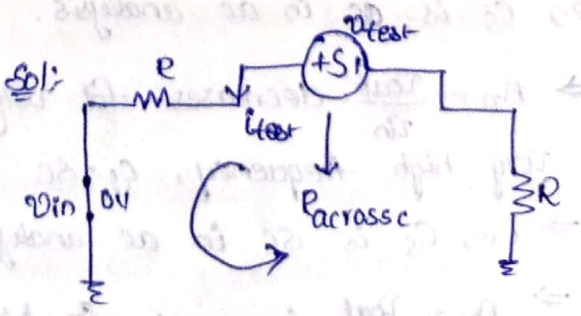
Cutoff frequency $= \frac{1}{R_{across,C} C} = \frac{1}{RC}$

Problem:-



Find cutoff freq.

Sol:-



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$-v_{test} + i_{test}R + i_{test}R = 0$

$v_{test} = 2\, i_{test} R$

$\frac{v_{test}}{i_{test}} = R_{across,C} = 2R$

$\Rightarrow \omega_c = \frac{1}{R_{across,C}\, C} = \frac{1}{2RC}$

for dc: $\omega = 0 \Rightarrow$ cap: OC $\Rightarrow \frac{v_{test}}{i_{test}} = 0$

for $\omega = \infty \Rightarrow$ cap: SC $\Rightarrow \frac{v_{test}}{i_{test}} = \frac{1}{2}$

lower frequency $\Rightarrow$ stopping ; higher freq $\Rightarrow$ Allowing.

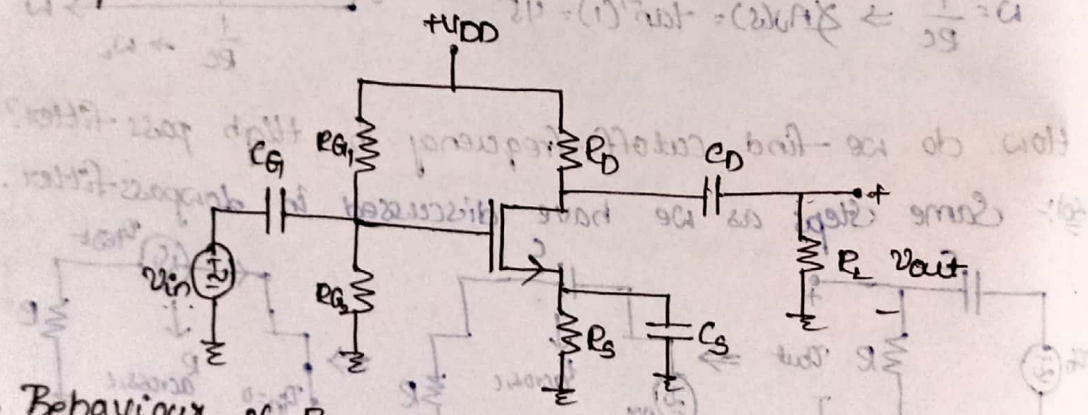
$\Rightarrow$ High Pass filter.

Note:- Alternate Method:

Find T.F(s) & substite $\omega = 0$ & $\omega = \infty$ in |T.F(s)|

17/2/22

How does coupling & Bypass capacitor behaviour with ac input?



i, Behaviour of Bypass capacitor 'C_S' on the Amplifier:

For dc: $\omega = 0 \Rightarrow C_S$ = OC

i.e., if we are applying frequencies (ac) nearer to dc ($\omega = 0$)

Very low freq signal "v_{in}" then C_S will be O.C.

i.e., C_S is oc in ac analysis.

$\Rightarrow A_V = \frac{v_{out}}{v_{in}}$ decreases for very low frequency.

For very high frequency, C_S: SC

$\Rightarrow$ i.e., C_S is SC in ac analysis.

$\Rightarrow A_V = \frac{v_{out}}{v_{in}}$ increases for high frequencies.

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Therefore Bypass capacitor 'C_S' gives high pass filter chars.

ii) Behaviour of coupling capacitor 'C_D' is an Amplifier.

If v_{in} is a very low-freq. signal which is nearer to

dc ($\omega=0$) $\Rightarrow$ C_D : OC $\Rightarrow$ $v_{out}=0$

$\Rightarrow$ Not allowing low freq. signal.

If v_{in} is a very high freq. signal which is '∞'

$\Rightarrow$ C_D : SC $\Rightarrow$ $\frac{v_{out}}{v_{in}} = -g_m(R_D // R_L)$

$\Rightarrow$ Allowing high freq. signal.

Therefore coupling capacitor 'C_D' gives high pass filter chars.

iii) Behaviour of coupling capacitor 'C_G' an Amplifier:

For v_{in} = Very low-frequency nearer to 'dc'

$\Rightarrow$ C_G : OC $\Rightarrow$ NO v_{in} goes to the amplifier.

$\Rightarrow$ $v_{out}=0$

$\Rightarrow$ Not allowing low-freq. signals.

For v_{in} = high freq. ($\omega=\infty$) $\Rightarrow$ C_G : SC

$\Rightarrow$ $\frac{v_{out}}{v_{in}} = -g_m(R_D // R_L)$

$\Rightarrow$ Allowing high frequency signal.

Therefore coupling capacitor 'C_G' gives high pass filter chars.

$\Rightarrow$ All the coupling capacitors & Bypass capacitors gives high pass filter characteristics.

$\Rightarrow$ ω_L $\rightarrow$ lower cutoff frequency of an Amplifier is decided by C_S, C_G & C_D.

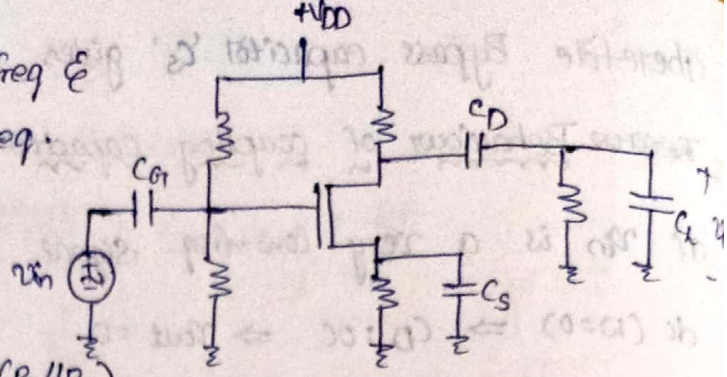
$\rightarrow$ Basically we design an Amplifier for having some gain & Bandwidth = $(f_H - f_L)$; f_L is decided by coupling & Bypass capacitors i.e., they give high pass filter characteristics.

$\rightarrow$ f_H : Higher frequency cut-off frequency f_H is decided by 'C_L' which intern is connected parallel to the load.

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C_L ⇒ Allowing low freq & Stopping high freq.

⇒ Low pass filter.



assume C_{G1}, C_S, C_D : SC

[for dc: C_L : OC

$\frac{V_{out}}{V_{in}} = -g_m(R_D \| R_L)$

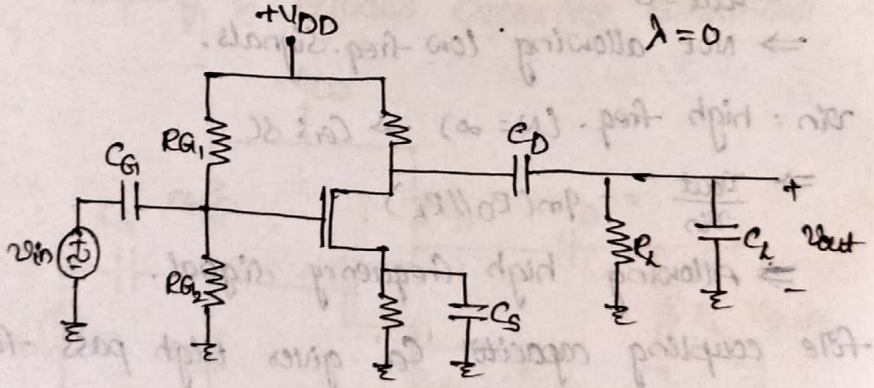
for $\omega = \infty$, C_L : SC

⇒ $V_{out} = 0$ ⇒ $A_V = 0$]

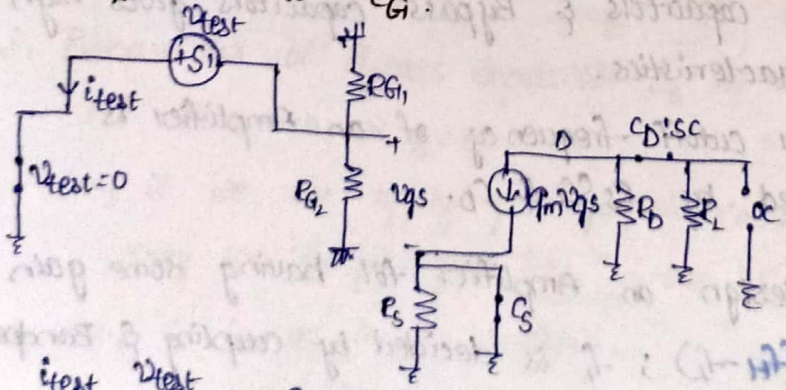
Summary:-

* Coupling & bypass capacitors gives high pass filter chars & C_L gives low pass filter chars.
* For a high pass filter, there will be a lower cut-off freq. ω_L or F_L. Each capacitor (C_{G1}, C_D & C_S) will give 'F_L' based on the values of "$R_{across,C}$ & C".

How to find lower cut off frequency 'F_L'?

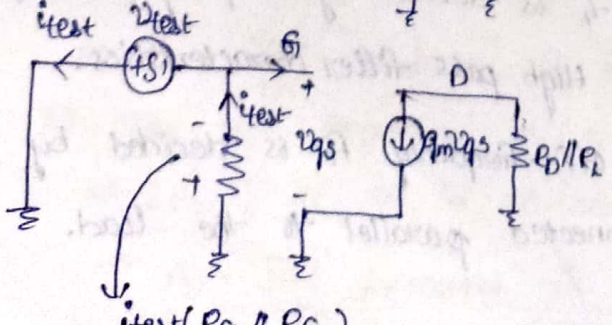


i) 'F_L' due to 'C_{G1}'.



Steps:

1. Take out C_{G1}
2. ~~Repeat~~ Replace C_{G1} connect V_{test}, i_{test} is coming out & DO the ac analysis.
3. $V_{in} = 0$ & dc voltage source ⇒ SC current sources ⇒ OC
4. C_D & C_S ⇒ SC, C_L ⇒ OC
5. Replace mosfet with small signal model, find $R_{across,C}$



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$\Rightarrow -v_{test} + i_{test}(R_{G_1} // R_{G_2}) = 0$

$R_{across,C_G} = \frac{v_{test}}{i_{test}} = R_{G_1} // R_{G_2}$

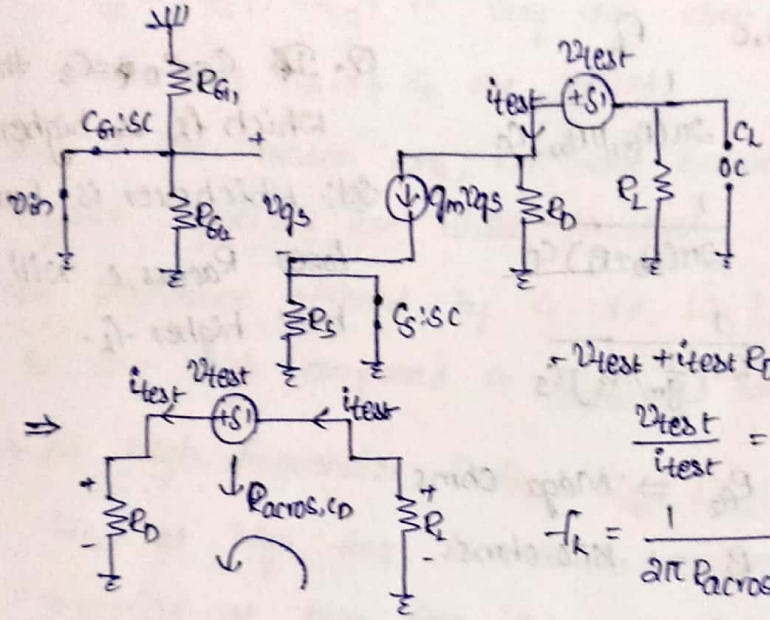
$\omega_L = \frac{1}{R_{across,C_G} \cdot C_G} = \frac{1}{(R_{G_1} // R_{G_2}) \cdot C_G}$

$f_L = \frac{1}{2\pi R_{across,C_G} \cdot C_G} = \frac{1}{2\pi (R_{G_1} // R_{G_2}) \cdot C_G}$ due to C_{G_1}.

6. Find $R_{across,C} = \frac{v_{test}}{i_{test}}$ & $\omega_L = \frac{1}{R_{across,C_G} \cdot C_G}$ or $f_L = \frac{1}{2\pi R_{across,C} \cdot C_G}$

ii, 'f_L' due to capacitor 'C_D'.

$C_S, C_G \Rightarrow SC$ & $C_L \Rightarrow OC$



$v_{in} = v_{gs} = 0$

$\Rightarrow g_m v_{gs} = 0$

$-v_{test} + i_{test} R_D + i_{test} R_L = 0$

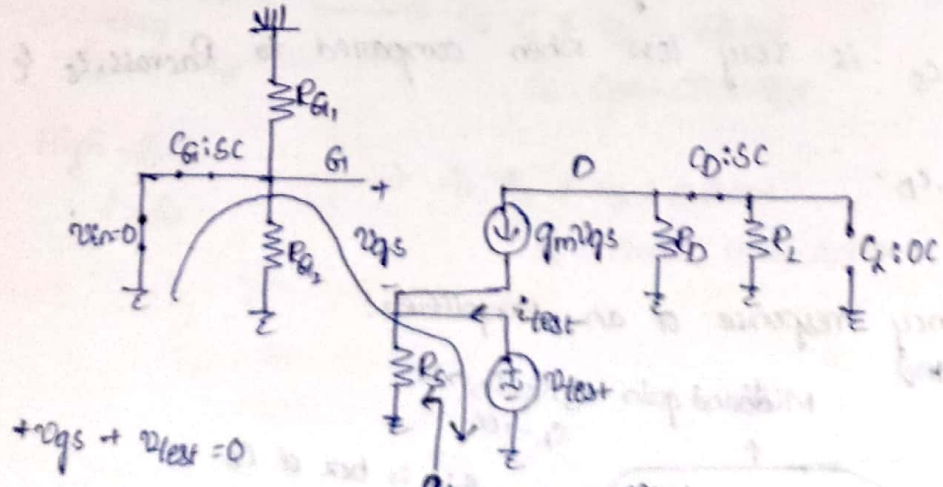
$\frac{v_{test}}{i_{test}} = R_{across,C_D} = R_D + R_L$

$f_L = \frac{1}{2\pi R_{across,C_D} \cdot C_D} = \frac{1}{2\pi (R_D + R_L) C_D}$

due to C_D.

iii, 'f_L' due to Bypass capacitor 'C_S':-

$C_G, C_D \Rightarrow SC$ & $C_L \Rightarrow OC$



$+v_{gs} + v_{test} = 0$

$v_{gs} = -v_{test}$

$R_{across,C_S} = \frac{v_{test}}{i_{test}}$

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Applying nodal @ source

$$i_{test} = \frac{v_{test}}{R_S} - g_m v_{gs} = \frac{v_{test}}{R_S} + g_m v_{test}$$

$$i_{test} = v_{test}\left[\frac{1}{R_S} + \frac{1}{1/g_m}\right]$$

$$\frac{v_{test}}{i_{test}} = \frac{1}{\frac{1}{R_S} + \frac{1}{1/g_m}} = \frac{1}{g_m} /\!/ R_S = R_{across,C_S}$$

$$f_L = \frac{1}{2\pi R_{across,C_S} \cdot C_S} = \frac{1}{2\pi\left(\frac{1}{g_m} /\!/ R_S\right) C_S}$$ due to C_S.

Note:-

Due to	$R_{across,C}$	f_L
C_G	$R_{G_1} /\!/ R_{G_2}$	$\frac{1}{2\pi(R_{G_1} /\!/ R_{G_2}) C_G}$
C_D	$R_D + R_L$	$\frac{1}{2\pi(R_D+R_L) C_D}$
C_S	$\frac{1}{g_m} /\!/ R_S$	$\frac{1}{2\pi\left(\frac{1}{g_m} /\!/ R_S\right) C_S}$

Q. If $C_G = C_D = C_S$ then which f_L is higher?

Sol:- whichever is having lower $R_{across,C}$ will have higher f_L.

* Typically R_{G_1} & R_{G_2} ⇒ Mega ohms

R_D & R_L ⇒ Kilo ohms.

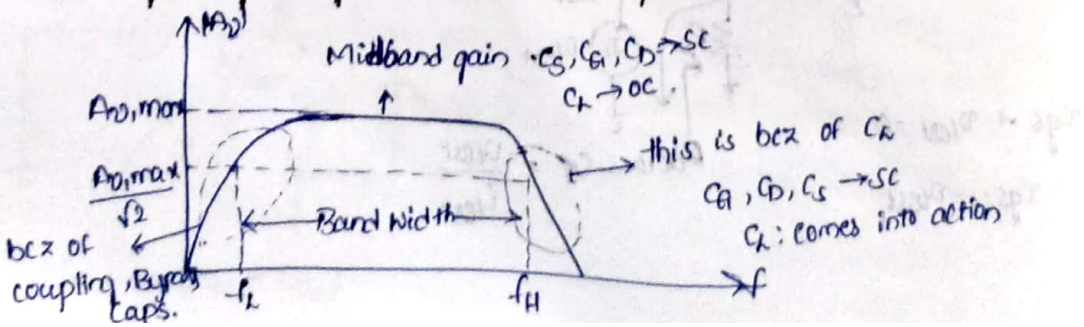
Eg:- If $g_m = 10\,mA/V \Rightarrow \frac{1}{g_m} = 100\,\Omega$

$\Rightarrow \left(\frac{1}{g_m} /\!/ R_S\right)$ ⇒ low value.
(R_S ↓ K-Ω)

⇒ f_L due to 'C_S' is higher when $C_G = C_D = C_S$ since R_{across,C_S} is very low when compared to R_{across,C_G} & R_{across,C_D}.

18/2/22

* Frequency response of an Amplifier:



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(at f_L) at these frequencies

$\Rightarrow$ coupling & Bypass caps comes into action.

* Why C_L should be OC:

→ At low frequencies i.e., in the vicinity of $f_L (f < f_L)$ the impedence offered by the C_G, C_S & C_D are in mole in comparision with $R_{across,C}$ C_G, C_S & C_D respectivly.

That's why C_G, C_S & C_D comes into action at these frequencie impedence offered by C_L is very high comp to $R_{across,C_L} \Rightarrow C_L$: OC

→ In midband frequencies i.e., $f > f_L$; the impedence $|Z_{C_G}|$, $|Z_{C_S}|$, $|Z_{C_D}|$ is very less comp to. R_{across,C_G,C_S,C_D} that's why C_G C_S & C_D are shorted.

This is the reason why, we have assumed the coupling & Bypass capacitors are short circuited.

The impedence offered by C_L i.e., $|Z_{C_L}|$ at midband freq. is very high compared to $R_{across,C_L} \Rightarrow C_L$: OC.

→ At high frequencies $f > f_H$; $|Z_{C_G}|$, $|Z_{C_S}|$ & $|Z_{C_D}|$ are shorted. $|Z_{C_L}|$ at high freq. is now in comparision with R_{across,C_L} therefore at high freq. 'C_L' comes into action.

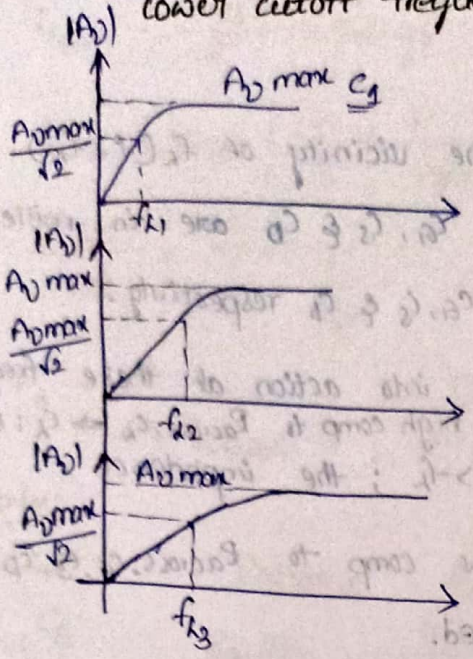
low frequencies $f < f_L$ ⟶ C_G, C_S & C_D : comes into action
C_L : Open circuit.

Midband freq. $f_L < f < f_H$ ⟶ C_G, C_S & C_D : shorted
C_L : Open Circuited.

High freq. $f > f_H$ ⟶ C_G, C_S & C_D : shorted.
C_L : Comes into action.

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Question:- If $f_{L1} < f_{L2} < f_{L3}$ then which is the dominant lower cutoff frequency?

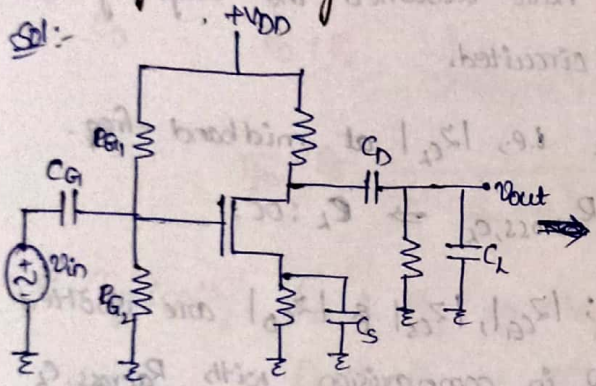


f_{L3} is the dominant lower cutoff frequency.

⇒ All frequency greater than f_{L3}; All the three capacitors are short circuits.

Finding the higher cutoff frequency due to 'C_L'.

Sol:-



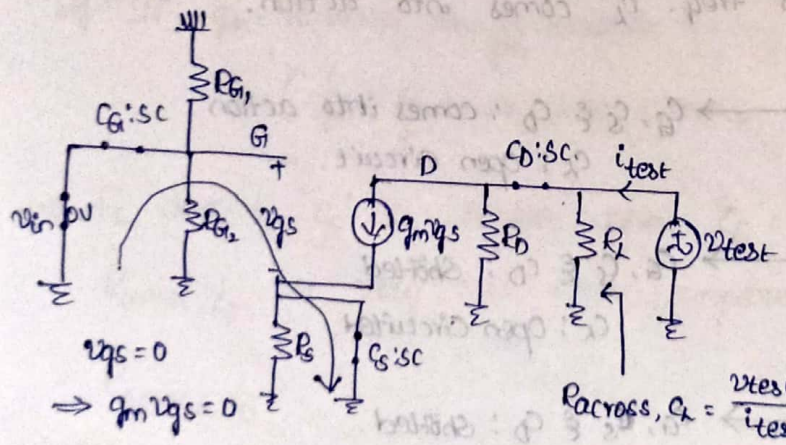
Apply Nodal @ drain

$$i_{test} = 0 + \frac{v_{test}}{R_D} + \frac{v_{test}}{R_L}$$

$$i_{test} = v_{test}\left[\frac{1}{R_D} + \frac{1}{R_L}\right]$$

$$\frac{v_{test}}{i_{test}} = \frac{R_D R_L}{R_D + R_L} = R_D \| R_L$$

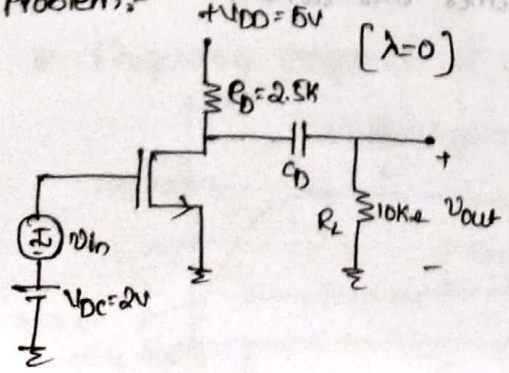
$$f_H \text{ due to } C_L = \frac{1}{2\pi R_{across\ C_L} \cdot C_L}$$



$$R_{across,\ C_L} = \frac{v_{test}}{i_{test}}$$

$$f_H = \frac{1}{2\pi (R_D \| R_L) C_L}$$

Problem:-

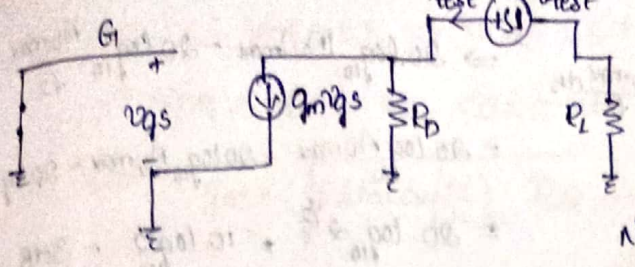


i, Presence of 'C_D' gives which filter characteristic?

High Pass Filter.

ii, In order to have a lower cutoff freq. f_L = 100Hz for the amplifier as shown in fig. What should be the value of 'C_D'.

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Given: $f_L = 100\,Hz$

$R_D = 2.5\,K\Omega$

$R_L = 10\,K\Omega$

$v_{gs} = 0 \Rightarrow g_m v_{gs} = 0$

$\frac{v_{test}}{i_{test}} = R_{across,C_D} = R_D + R_L$

$R_{across,C_D} = 2.5K + 10K$

$= 12.5\,K\Omega$

Now, $f_L = \frac{1}{2\pi R_{across,C_D} \cdot C_D}$

$C_D = \frac{1}{2\pi R_{across} C_D \cdot f_L}$

$C_D = \frac{1}{2\pi \times 12.5K \times 100}$

$C_D = 0.0127 \times 10^{-5}$

$\boxed{C_D = 0.127\,\mu F}$

Why "decibels"?

Suppose we want to plot voltage gain values from 1 V/V to 10^5 V/V w.r.t frequency. This cannot be done using a linear scale.

Thats why use decibels i.e, dB's

* Voltage gain $dB = 20 \log_{10} A_v$

Current gain $dB = 20 \log_{10} A_I$

$\frac{P_{out}}{P_{in}}$ = Power gain $dB = 10 \log_{10} \frac{P_{out}}{P_{in}}$

Suppose, $A_v = 10^5$ V/V (nominal values)

In dB's $\Rightarrow |A_v|_{dB} = 20 \log_{10} |A_v| = 20 \log_{10} 10^5$

$= 20 \times 5 \log_{10} 10$

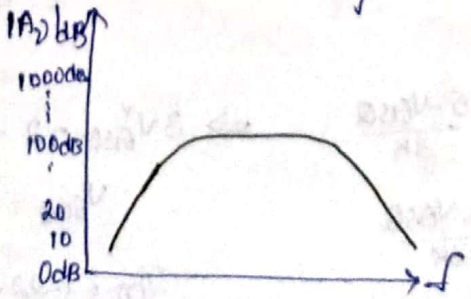
$|A_v| = 10^5 V/V = |A_v|_{dB} = 100\,dB$

$A_v = 1 V/V$ (nominal value)

In dB's $\Rightarrow |A_v|_{dB} = 20 \log_{10} |A_v| = 20 \log_{10} 1 = 0\,dB.$

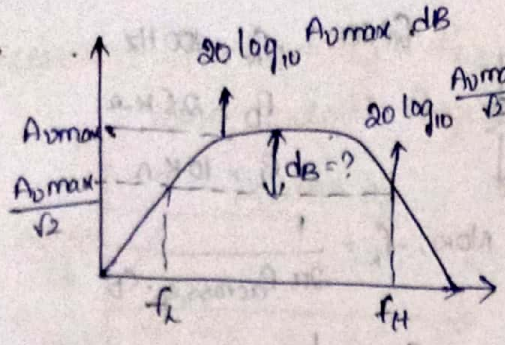
$A_v = 1 V/V \Rightarrow |A_v|_{dB} = 0\,dB.$

$\Rightarrow$ Now using decibels we can plot $|A_v|_{dB}$ Vs freq.



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*



$\Rightarrow 20\log_{10}|A_v|_{max} - 20\log_{10}\frac{A_{v\max}}{\sqrt{2}}$

$= 20\log_{10} A_{v\max} - 20\log_{10} A_{v\max} - 20\log_{10}\sqrt{2}$

$= 20\log_{10} 2^{1/2} = 10\log_{10} 2 = 3\text{dB}$

$\Rightarrow$ "3 dB cut-off frequency."

19/8/22

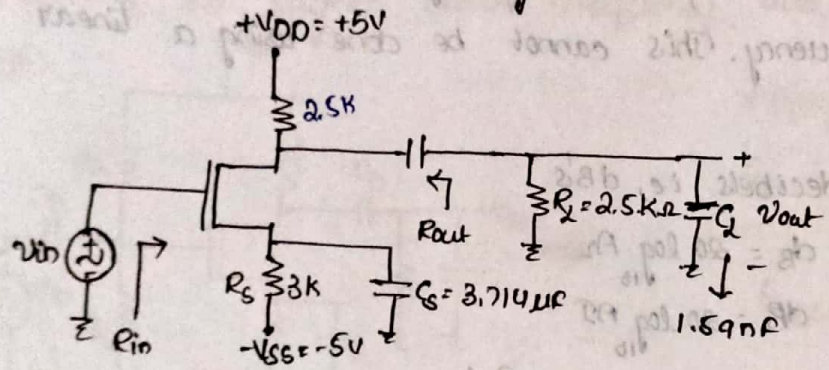
* If A_v in dB is -ve then A_v is less than 1.

Eg: $A_v = 0.1\ V/V \Rightarrow |A_v|_{dB} = 20\log|A_v|$

$= 20\log_{10} 10^{-1}$

$= -20\text{ dB}.$

* Find f_L, f_H & Midband gain of Amplifier as shown.



Given $\mu_n C_{ox} = 1m A/V^2$

$\left(\frac{W}{L}\right)_n = 2$

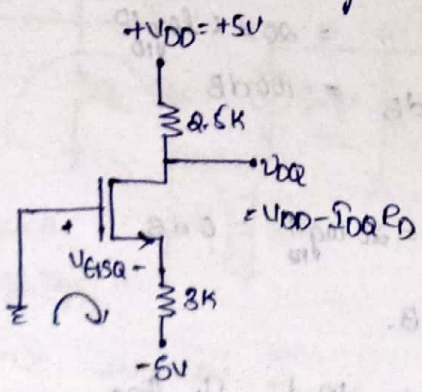
$V_{tn} = 1V$

$\lambda = 0$

Sol: In mid band $\Rightarrow$ C_S & C_D : SC ; C_L : OC

Mid band gain $\Rightarrow$ Small Signal voltage gain.

1. Find Q. Point using dc analysis & then calculate g_m.



Assume mos in sat:

$I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSQ} - V_{tn})^2$

$I_{DQ} = \frac{1}{2} \times 1m \times 2[V_{GSQ} - V_{tn}]^2 \rightarrow (1)$

$V_{GSQ} + I_{DQ} 3K - 5 = 0$

$I_{DQ} = \frac{5 - V_{GSQ}}{3k} \rightarrow (2)$

from (1) & (2)

$V_{GSQ}^2 + V_{tn}^2 - 2V_{GSQ} = \frac{5 - V_{GSQ}}{3K}$

$V_{GSQ}^2 + 1 - 2V_{GSQ} = \frac{5 - V_{GSQ}}{3K}$

$3V_{GSQ}^2 + 3 - 6V_{GSQ} = 5 - V_{GSQ}$

$\Rightarrow 3V_{GSQ}^2 - 2 - 5V_{GSQ} = 0$

$V_{GSQ} = 1.33, -1$

$I_{DQ} = 1.22\text{ mA} = 1\text{mA}.$

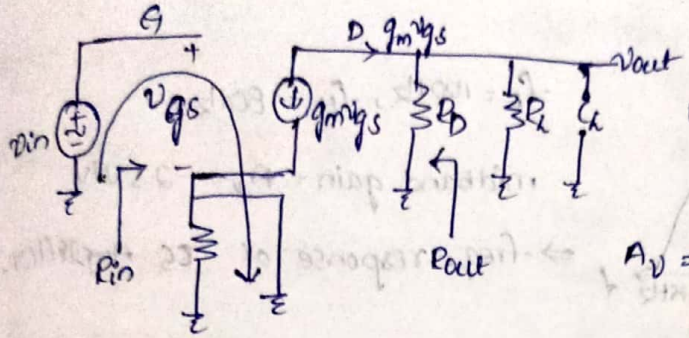
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$\Rightarrow V_{DQ} = 5 - 1m(2.5) \Rightarrow V_{DQ} = 2.5V$

$\Rightarrow V_{DQ} > V_{tQ} \Rightarrow$ saturation.

In sat: $g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_n I_{DQ}} = \sqrt{2 \times 1m \times 2 \times 1m} = 2mA/V.$

Mid band gain :- Small signal voltage gain.



$v_{gs} = v_{in}$

Nodal

$v_{out} = -g_m v_{gs} (R_D \| R_L)$

$A_v = \frac{v_{out}}{v_{in}} = -g_m (R_D \| R_L)$

$= -2m (2.5K \| 2.5K)$

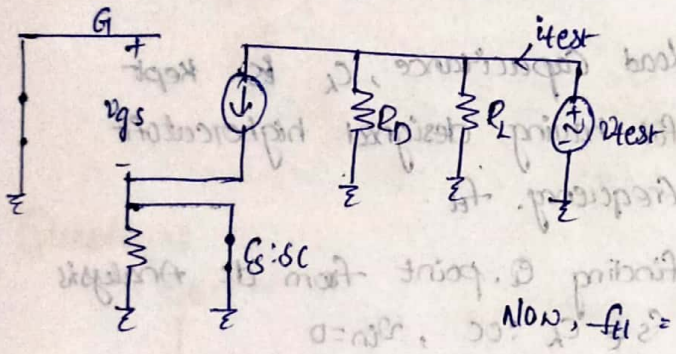
$= -2m (1.25K)$

$A_v = -2.5 V/V$

$R_{in} = \infty$

$R_{out} = R_D = 2.5K\Omega$

f_H : Higher cutoff frequency. Bcz of 'C_L'.



$v_{gs} = 0 \Rightarrow g_m v_{gs} = 0$

$\frac{v_{test}}{i_{test}} = R_{across, C_L} = R_D \| R_L$

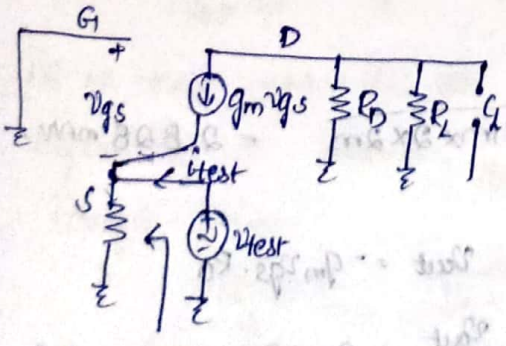
$R_{across, C_L} = 1.25K.$

Now, $f_H = \frac{1}{2\pi R_{across, C_L} \cdot C_L} = \frac{1}{2\pi \times 1.25K \times 1.5n}$

$f_H = 80 KHz$

f_L :- Lowest cutoff frequency Bcz of C_S & C_D.

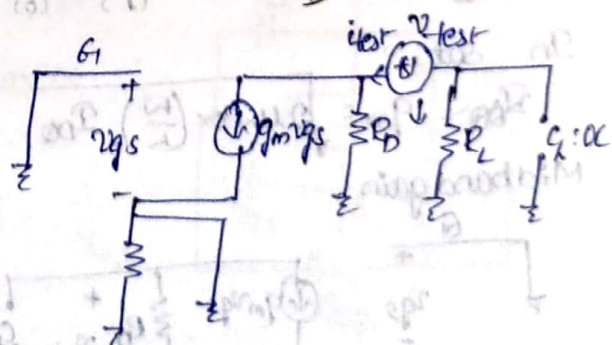
R_{across, C_S}



$R_{across, C_S} = \frac{1}{g_m} \| R_S$

$= 0.5K \| 3K = 0.428K\Omega$

R_{across, C_D}



$R_{across, C_D} = R_D + R_L = 2.5K + 2.5K$

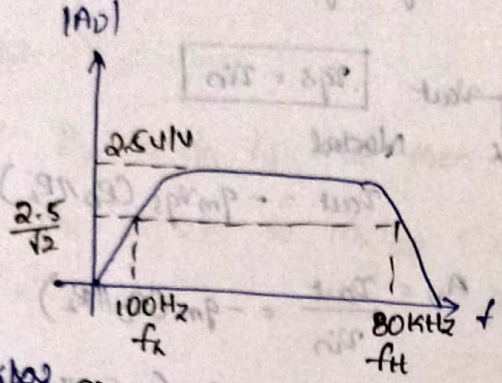
$R_{across, C_D} = 5K\Omega$

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$f_{L,C_S} = \frac{1}{2\pi R_{across,C_S} \cdot C_S}$ $f_{L,C_D} = \frac{1}{2\pi R_{across,C_D} \cdot C_D}$

$= \frac{1}{2\pi \times 0.428K \times 371.4\mu}$ $= \frac{1}{2\pi \times 5K \times 0.3175\mu}$

$f_{L,C_S} = 100Hz$. $f_{L,C_D} = 100Hz$

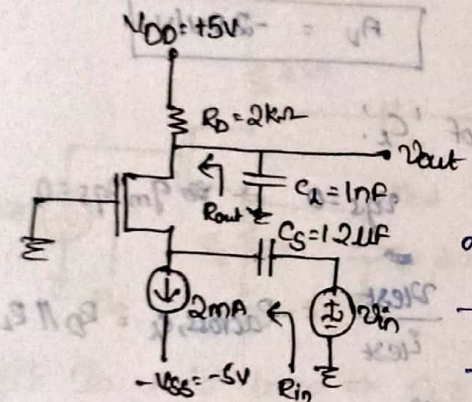


$f_L = 100Hz$, $f_H = 80Hz$

midband gain = $A_V = -2.5 V/V$

⇒ freq. response of CS Amplifier.

Problem Find the midband gain, f_L & f_H of the Amplifier as shown $\mu_n C_{ox} = 1mA/V^2$, $V_{th} = 1V$, $\left(\frac{W}{L}\right)_n = 2$ $\lambda = 0$



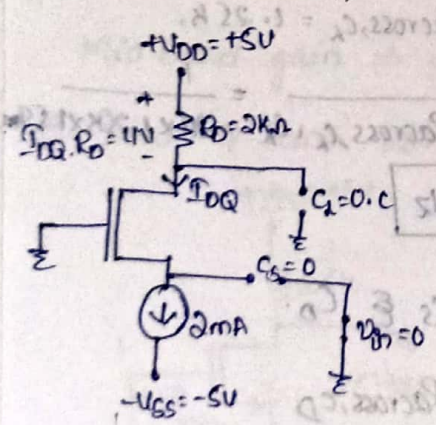
By observation:

ip @ source
op @ Drain
} CG Amplifier.

Load capacitance, C_L is kept for having designed higher cutoff frequency. f_H.

1. finding Q. point from dc Analysis

C_S & C_L : OC, $v_{in} = 0$



By observation

$I_{DQ} = 2mA \Rightarrow I_{DQ} \cdot R_D = 4V$.

$V_{DQ} = 5 - 4V \Rightarrow V_{DQ} = 1V$

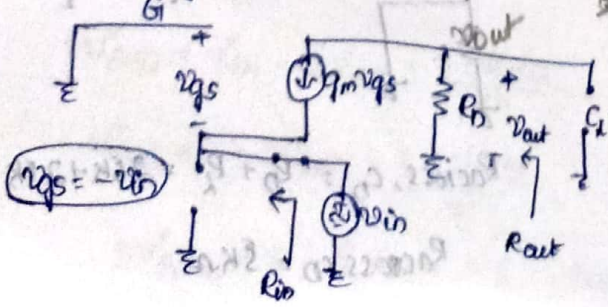
$V_{DQ} > V_{GQ} \Rightarrow$ saturation.

(1) (0)

In sat:

$I_{DQ} = g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_n I_{DQ}} = \sqrt{2 \times 1m \times 2 \times 2m} = 2.828 mA/V$.

Midband gain



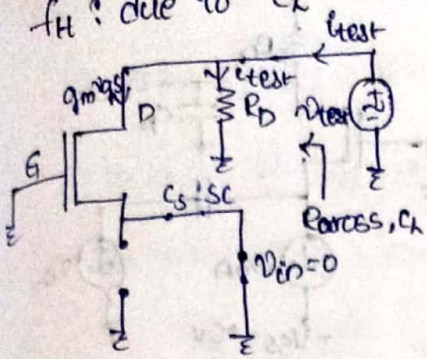
$v_{out} = -g_m v_{gs} \cdot R_D$

$\frac{v_{out}}{v_{in}} = A_V = g_m R_D = 2.828 \times 2$

$A_V = 5.65 V/V$

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f_H : due to C_L



$v_g = 0 \Rightarrow g_m v_{gs} = 0$

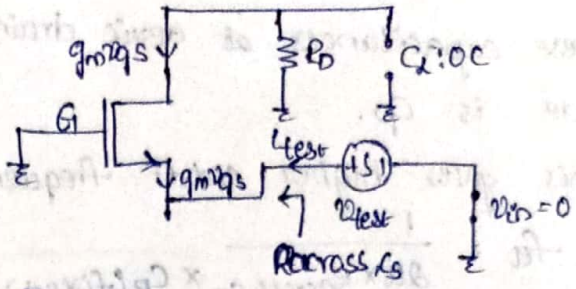
$$R_{across, C_L} = \frac{v_{test}}{i_{test}} = R_D$$

$\Rightarrow R_{across, C_L} = 2K\Omega$

$$f_H = \frac{1}{2\pi \times 2K \times 1nF}$$

$$\boxed{f_H = 79.5\ KHz}$$

f_L : due to C_S



$v_{gs} + v_{test} = 0$

$v_{gs} = -v_{test}$

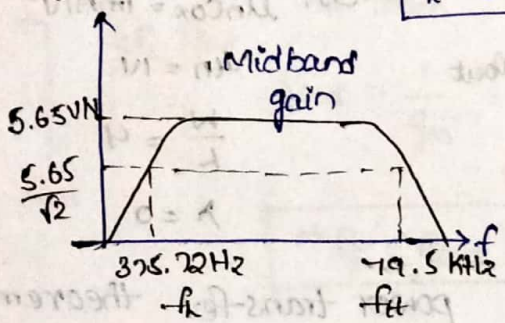
$i_{test} = -g_m v_{gs} = g_m v_{test}$

$$\frac{v_{test}}{i_{test}} = R_{across, C_S} = \frac{1}{g_m} = \frac{1}{2.828\ mA/V}$$

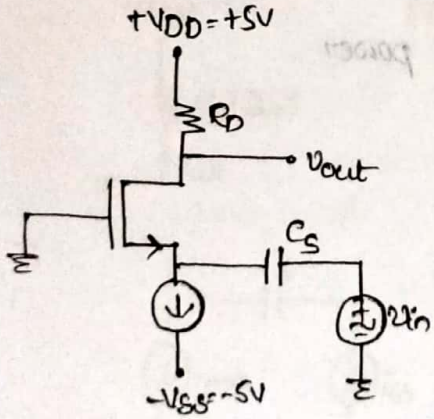
$\Rightarrow R_{across, C_S} = 0.353K\Omega$

$$f_L = \frac{1}{2\pi \times 0.353K \times 1.2\mu} = 375.72\ Hz$$

$$\Rightarrow \boxed{f_L = 375.72\ Hz}$$

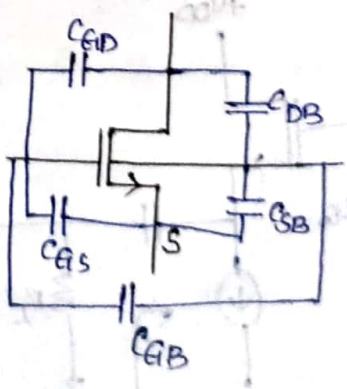


Question:



Will there be any higher cutoff freq?

Sol:- Even though we haven't connected any load capacitance 'C_L' but still we will have higher cutoff frequency because of parasetic capacitor @ drain node.



All of these capacitors are parasitic capacitors of Mosfet.

Ranges from

10^{-15} F ↓ femto farads to 10^{-18} F ↓ Atto farads.

These capacitors are kept from externally, these are all device capacitance.

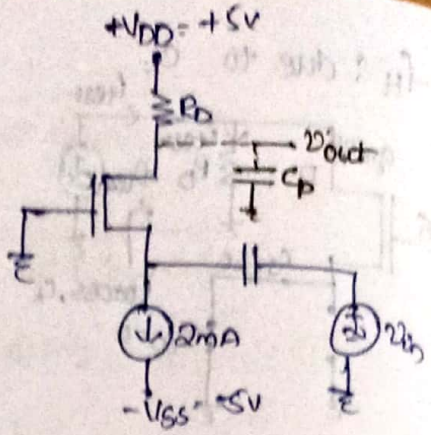
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Therefore, the effect of all of these capacitances at device drain node is C_p.

This gives higher cutoff frequency.

$$f_H = \frac{1}{2\pi \times R_{across,C_p} \times C_p \text{ (fixed)}}$$

$$\boxed{f_H = \frac{1}{2\pi \times R_D \times C_p}}$$

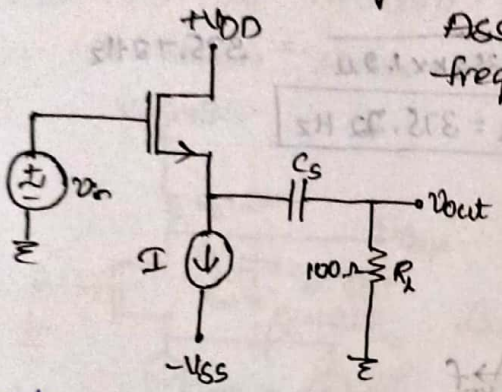


22/2/22

Problem:

What should be the value of current source 'I' for which maximum power is delivered to the load R_L.

Assume C_S is shorted for our freq. of intrest.



Given: $\mu_n C_{ox} = 1mA/V^2$

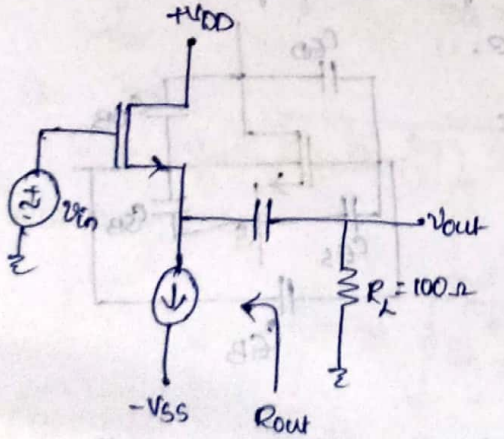
$V_{tn} = 1V$

$\frac{W}{L} = 4$

$\lambda = 0$

Sol: As per Maximum power transfer theorem; i.e., when v_{in} is kept constant & R_L is varied & corresponding P_{R_L} is power max. power

In our Cas; $R_L = R_{out}$



$$R_{out} = \frac{1}{g_m} \| r_o$$

$$R_{out} = \frac{1}{g_m}$$

$$\therefore R_{out} = R_L$$

$$\frac{1}{g_m} = 100$$

$$g_m = 10 \text{ mA/V}$$

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In Sat:

$$\sqrt{2\mu_n C_{ox}\frac{W}{L} I_{DQ}} = 10m$$

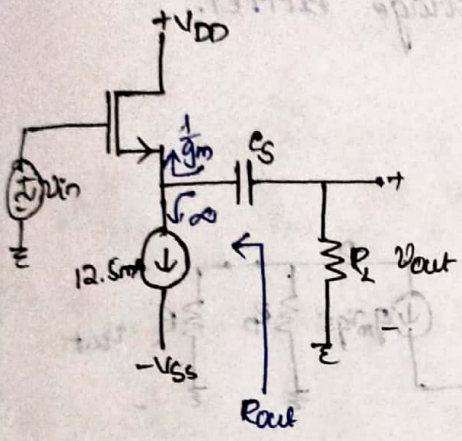
$$2\times\mu_n C_{ox}\frac{W}{L} I_{DQ} = 10\times 10m$$

$$2\times 1m\times 4\times I_{DQ} = 10m\times 10m$$

$$I_{DQ} = \frac{50m}{4} \Rightarrow \boxed{I_{DQ} = 12.5mA}$$

For what value of R_L, max. power is delivered to the load. Assume C_S is S.C for our freq. of intrest.

Given $\mu_n C_{ox} = 1mA/V^2$, $V_{tn} = 1V$, $\left(\frac{W}{L}\right)_n = 4$, $\lambda = 0$



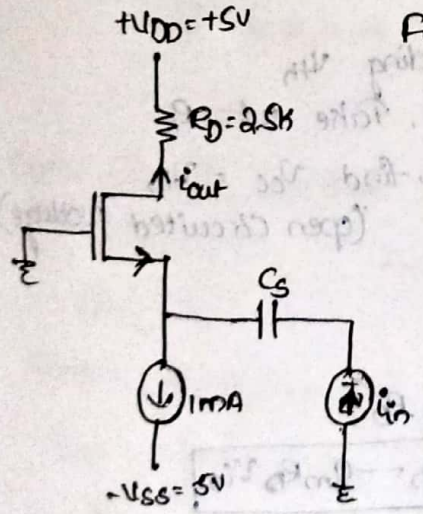
AS per max. power transfer theorem,

$R_L = R_{out}$ for max. power delivered to load.

$$R_{out} = \frac{1}{g_m} = \frac{1}{\sqrt{2\mu_n C_{ox}\frac{W}{L}\cdot I_{DQ}}} = \frac{1}{10m}$$

$$\Rightarrow \boxed{R_L = R_{out} = 100\,\Omega}$$

Question:



Find small signal current gain

$A_I = \frac{i_{out}}{i_{in}}$ Given $\mu_n C_{ox} = 1mA/V^2$

$V_{tn} = 1V$

$\left(\frac{W}{L}\right)_n = 2$, $\lambda = 0$

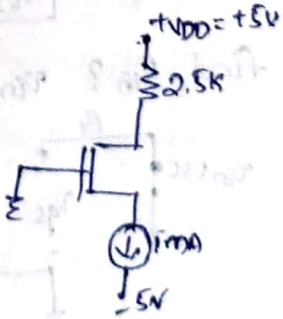
Here C_S is shorted for our freq. of intrest.

Use AC analysis for finding A_I.

By Observation:

$I_{DQ} = 1mA$, $V_{DQ} = V_{DD} - I_{DQ}\cdot R_D = 2.5V$

$V_{GIQ} = 0 \Rightarrow V_{DQ} > V_{GIQ} \Rightarrow$ Saturation.

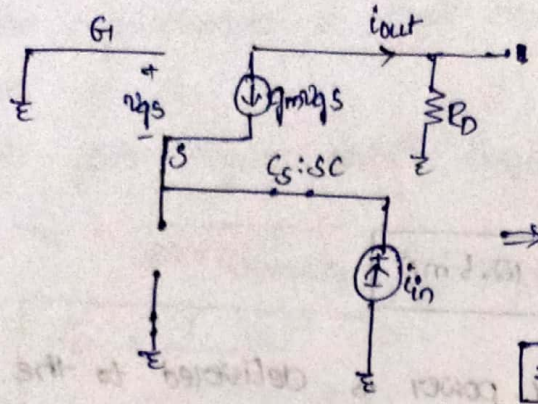


In Sat:

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) I_{DQ}} = \sqrt{2\times 1m\times 2\times 1mA} = 2mA/V.$$

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AC Analysis



$i_{out} = -g_m v_{gs}$.

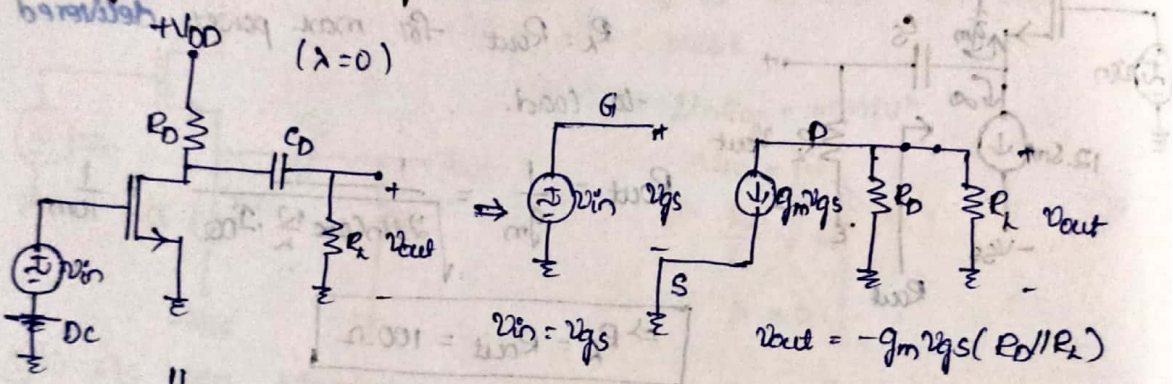
$i_{in} = -g_m v_{gs}$

$\Rightarrow \frac{i_{out}}{i_{in}} = 1$

$\Rightarrow A_V = 1$

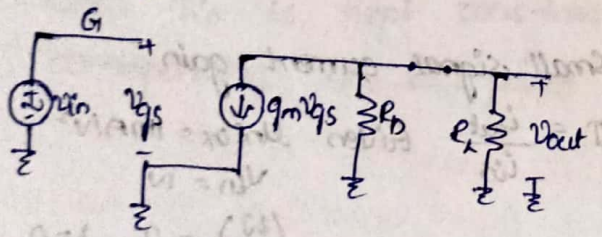
* 'CG' Comp configuration is used as Current Buffer.
* 'CD' configuration is used as voltage Buffer.

Using Thevinin's Equivalent :-



$v_{out} = -g_m v_{gs}(R_D \| R_L)$

$A_V = \frac{v_{out}}{v_{in}} = -g_m(R_D \| R_L)$

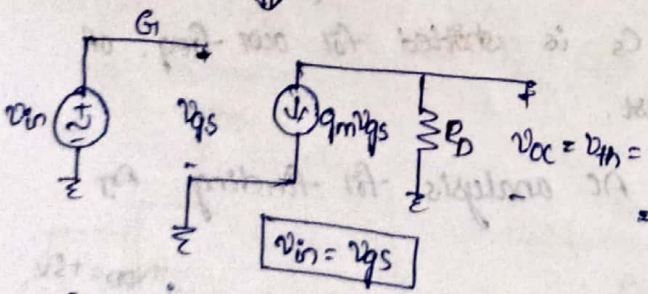


finding v_{th}

i, take out R_L

ii, find $v_{oc} = v_{th}$

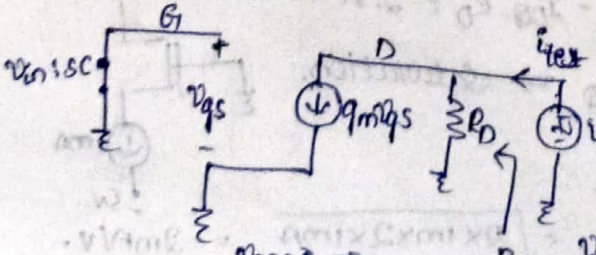
(open circuited voltage)



$v_{oc} = v_{th} = -g_m v_{gs} \cdot R_D$

$\Rightarrow v_{th} = -g_m R_D v_{in}$

find R_{th} ? $v_{in} = 0$

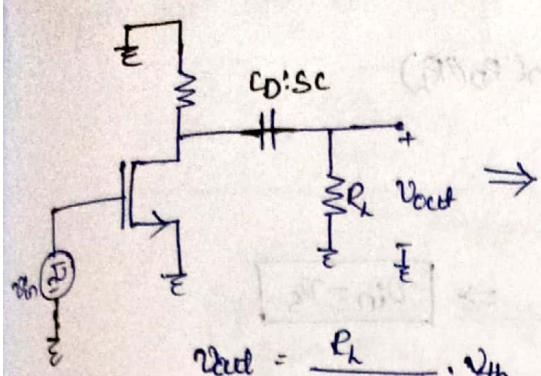


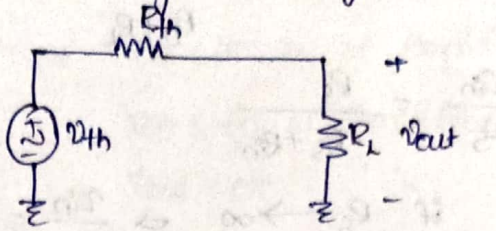
$\frac{v_{out}}{i_{test}} = R_{th} = R_D$

$v_{gs} = 0 \Rightarrow g_m v_{gs} = 0$ $R_{th} = \frac{v_{test}}{i_{test}}$

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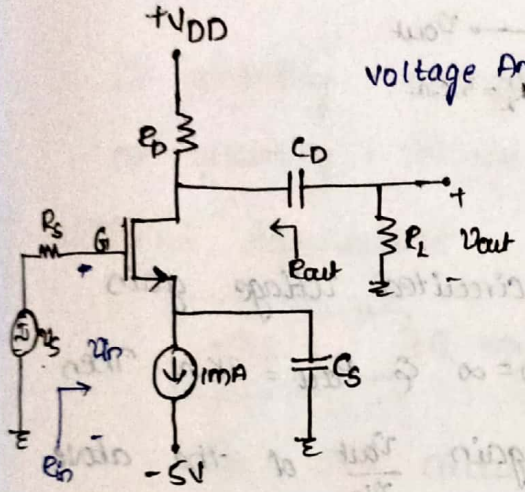
Thevinin equivalant Model for Small Signal Analysis.



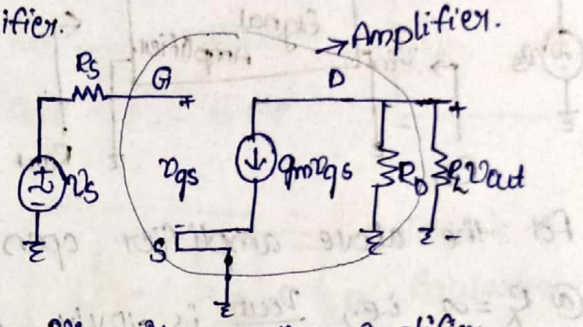


$$v_{out} = \frac{R_L}{R_L + R_{th}} \cdot v_{th} = \frac{R_L}{R_L + R_D} \cdot -g_m R_D \cdot v_{in}$$

$$A_v = \frac{v_{out}}{v_{in}} = -g_m \frac{R_D \cdot R_L}{R_D + R_L} \Rightarrow \boxed{A_v = -g_m (R_D // R_L)}$$



Voltage Amplifier.



→ Amplifier.

v_{in}: i/p of the Amplifier.

v_S : Source signal

R_S : Source resistance.

R_{in}: i/p resistance of Amplifier.

R_{out} : o/p resistance of Amplifier.

v_{out} : o/p of Amplifier.

$R_{in} = \infty$, $R_{out} = R_D$

$$A_v = \frac{v_{out}}{v_{in}}\Big|_{@ R_L = \infty} \Rightarrow$$ (open Circuited voltage gain).

Small Signal res.

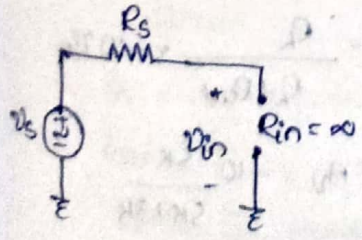
Open Circuit voltage gain,

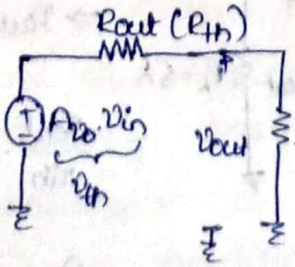
$$A_v = \frac{v_{out}}{v_{in}}\Big|_{@ R_L = \infty}$$

@ $R_L = \infty$

$v_{out} = -g_m v_{gs} \cdot R_D$

$v_{out} = -g_m v_{in}$ $\Rightarrow \frac{v_{out}}{v_{in}} = A_{vo} = -g_m R_D$





$v_{oc} = v_{th} = -g_m R_D \cdot v_{in}$

$v_{th} = A_{vo} \cdot v_{in}$

voltage Divider.

$$\Rightarrow v_{out} = \frac{R_L}{R_L + R_{out}} A_{vo} v_{in}$$

$$\Rightarrow \frac{v_{out}}{v_{in}} = A_v = A_{vo} \cdot \frac{R_L}{R_{out} + R_L}$$

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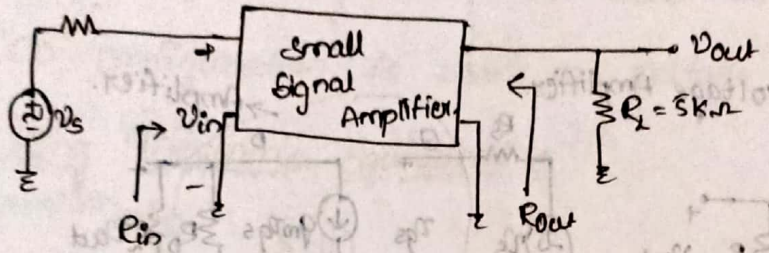
$$\Rightarrow A_V = -g_m R_D \cdot \frac{R_L}{R_D + R_L} = -g_m (R_D \| R_L)$$

$$\frac{v_{in}}{v_s} = \frac{R_S}{R_S + R_{in}}$$

if $R_S \longrightarrow \infty \Rightarrow \frac{v_{in}}{v_s} = 1 \Rightarrow \boxed{v_{in} = v_s}$

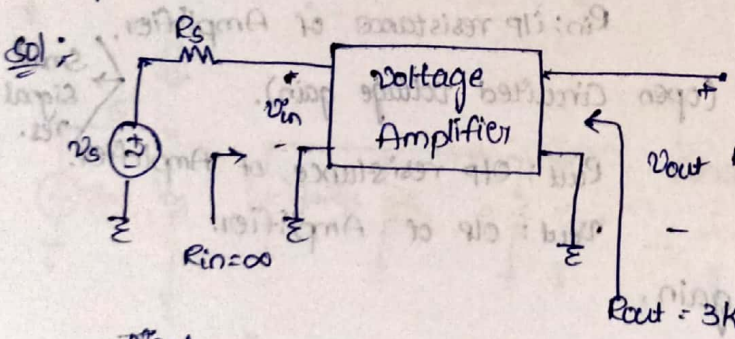
$$\Rightarrow A_{VS} = \frac{v_{out}}{v_s} = \frac{v_{out}}{v_{in}} = A_V = A_{V_0} \frac{R_L}{R_L + R_O}$$

Problem:



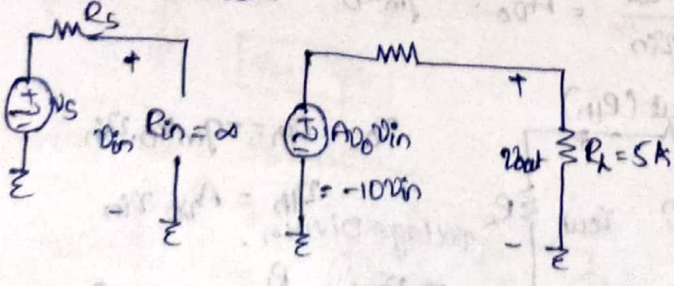
For the above amplifier open circuited voltage gain @ $R_L = \infty$ i.e., $\frac{v_{out}}{v_{in}}$ is $-10 V/V$, $R_{in} = \infty$ & $R_{out} = 3k\Omega$. Then find the small signal voltage gain $\frac{v_{out}}{v_{in}}$ of the above Amplifier.

Sol:



$\frac{v_{out}}{v_{in}} = A_{V_0} = -10 V/V$ (open circuited voltage gain)

The above voltage amplifier equivalent circuit is modelled as:



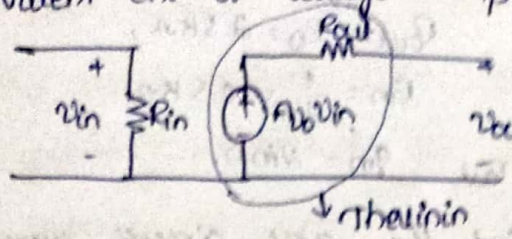
$$\Rightarrow v_{out} = \frac{R_L}{R_L + R_{out}} \times -10 v_{in}$$

$$\frac{v_{out}}{v_{in}} = A_V = -10 \cdot \frac{5k}{5k + 3k}$$

$$A_V = -10 \cdot \frac{5}{8} \Rightarrow \boxed{A_V = -6.25 V/V}$$

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Equivalent ckt of voltage Amplifier.



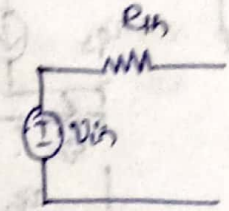
Rout : o/p res. of Amplifier } Small Signal
Rin : i/p res of Amplifier
Vin : i/p of Amplifier
Vout : o/p " "

$A_{Vo} = \left.\frac{V_{out}}{V_{in}}\right|_{R_L=\infty}$ ← [Open Circuited voltage gain @ $R_L = \infty$]

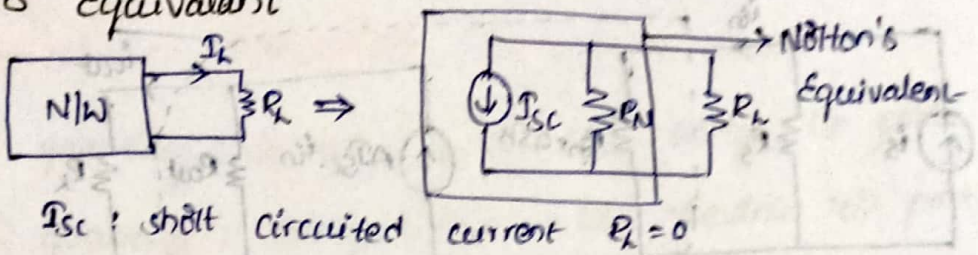
Thevinin model is taken @ output since the o/p quantity is voltage quantity → for a voltage Amplifier

$A_V = \frac{V_{out}}{V_{in}}$

i/p quantity : voltage V_{in} → ∴ @ i/p
o/p quantity : voltage V_{out} → ∴ @ o/p



Norton's Equivalent



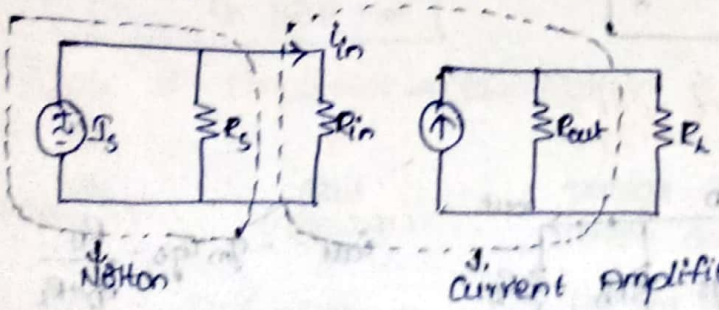
I_{sc} : short circuited current $R_L = 0$

$I_L \approx I_{sc}$ @ $R_L = 0$, R_N is similar to R_{th}

Current Amplifier

A_I = current gain = $\frac{i_{out}}{i_{in}}$

i/p quantity : current i_{in} → Use Norton Equivalent @ i/p
o/p quantity : current i_{out} → Use Norton " @ o/p.

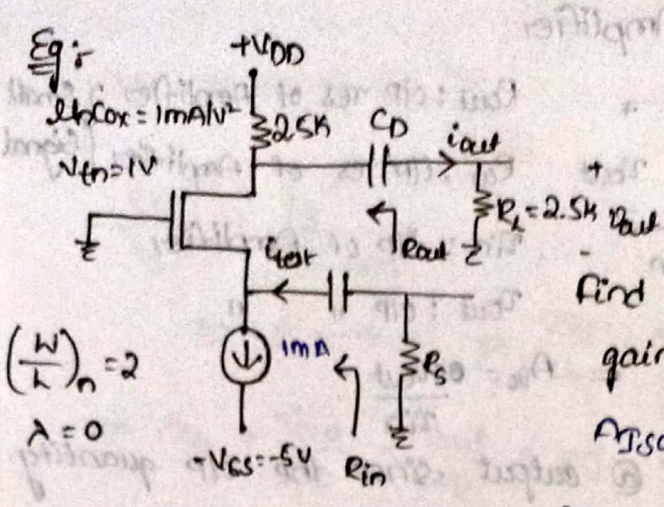


i_{in} = i/p current of the Amplifier
i_{out} = o/p current flowing through R_L.
R_{in} = i/p ~~current~~ resistance of Amplifier.
R_{out} = o/p resi. of Amplifier.

$A_{Isc} = \left.\frac{i_{out}}{i_{in}}\right|_{@R_L=0}$ Short Circuited current gain.

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Eg:



$\mu_n C_{ox} = 1mA/V^2$

$V_{th} = 1V$

$\left(\frac{W}{L}\right)_n = 2$

$\lambda = 0$

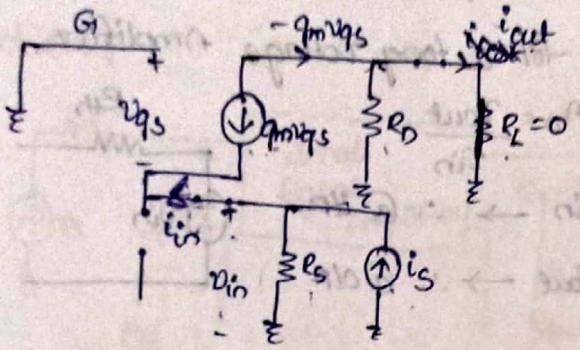
$R_{out} = R_D = 2.5k\Omega$,

$R_{in} = \frac{1}{g_m} = 0.5k\Omega$

$g_m = 2mA.$

Find the short circuit current gain?

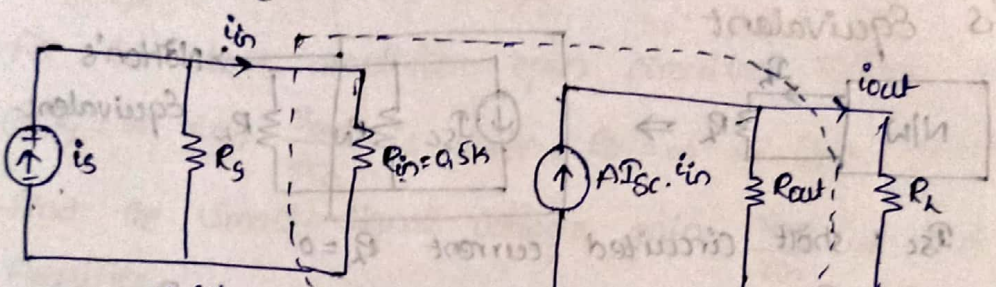
$A_{ISC} = \left.\frac{i_{out}}{i_{in}}\right|_{@ R_L = 0}$



$i_{out} = -g_m v_{gs}$

$i_{in} = -g_m v_{gs}$.

$\frac{i_{out}}{i_{in}} = 1 \Rightarrow \boxed{A_{ISC} = 1}$



Current Divider.

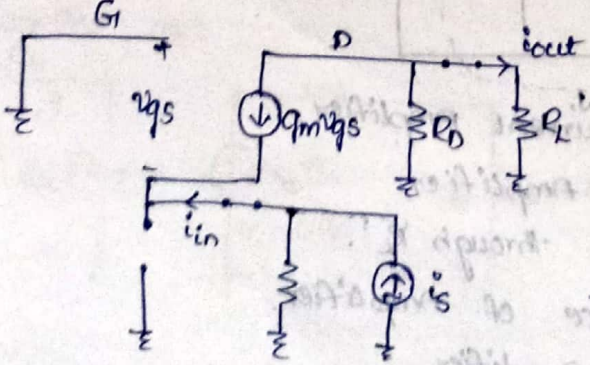
Current Amplifier.

$i_{out} = \frac{R_{out}}{R_L + R_{out}} \cdot A_{ISC}\, i_{in}$

$\frac{i_{out}}{i_{in}} = A_{ISC} \cdot \frac{R_{out}}{R_L + R_{out}} = 1 \times \frac{2.5K}{2.5K + 2.5K} = \frac{1}{2}$

$\Rightarrow \boxed{\frac{i_{out}}{i_{in}} = A_I = \frac{1}{2}}$

n/o using equivalant ckt:-



$i_{out} = -g_m v_{gs} \cdot \frac{R_D}{R_D + R_L}$

$= i_{in} \cdot \frac{R_D}{R_D + R_L}$

$\frac{i_{out}}{i_{in}} = A_I = \frac{R_D}{R_D + R_L}$

$i_{in} = -g_m v_{gs}$

$\boxed{A_I = \frac{1}{2}}$

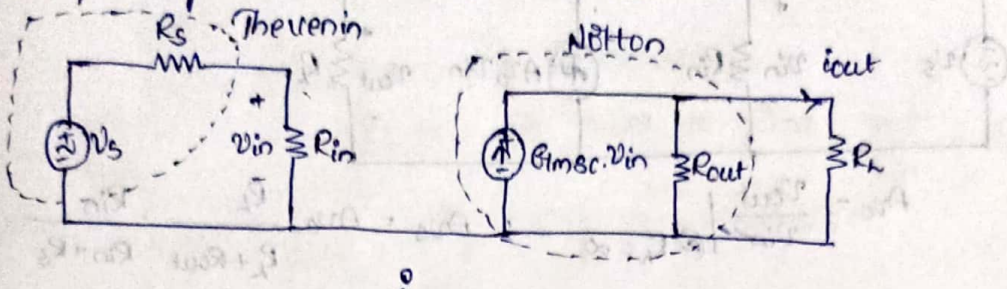
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Transconductance Amplifier (G_m)

'G_m' → transconductance gain.

ilp quantity → voltage 'v_{in}' → Use thevinin ilp part

olp quantity → current 'i_{out}' → Use Norton olp part.



$$G_{MSC} = \frac{i_{out}}{v_{in}}\Big|_{@R_L=0}$$

thevinin - Norton
v_{in} i_{out}

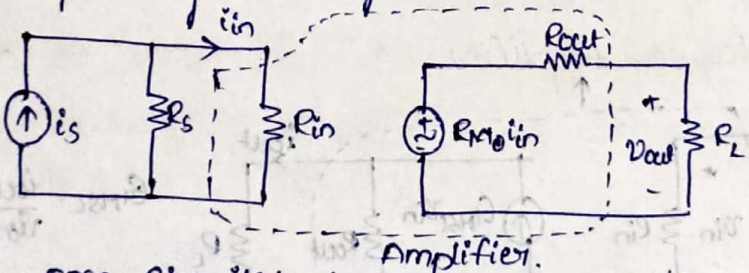
short circuit transconductance gain

R_{in}, R_{out} ⇒ ilp & olp resistance of Amplifier.

Transresistance Amplifier (R_m)

ilp quantity : Current i_{in} → Use Norton ilp part

olp quantity : Voltage v_{out} → Use thevinin olp part.



R_{MO} = open circuited trans resistance gain

$$R_{mo} = \frac{v_{out}}{i_{in}}\Big|_{@R_L=\infty}$$

R_{in} & R_{out} → ilp & olp res. of Amp.

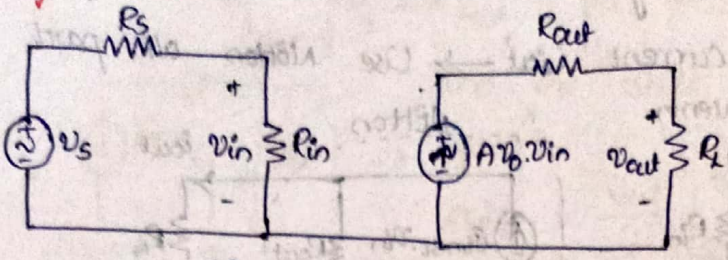
4 types of Amplifier → Classification is based on ilp & olp qtn.

ilp	olp	Amplifier.
v_{in} (thevinin)	v_{out} (Thevinin)	voltage Amplifier control source $A_{vo}.v_{in}$ ⇒ $A_{vo} = \frac{v_{out}}{v_{in}}$ @ $R_L=\infty$
i_{in} (Norton)	i_{out} (Norton)	Current Amplifier control source $A_{ISC}.i_{in}$ ⇒ $A_{ISC} = \frac{i_{out}}{i_{in}}$ @ $R_L=0$
v_{in} (Thevenin)	i_{out} (Norton)	Transconductance Amplifier control source $G_{MSC}v_{in}$ ⇒ $G_{MSC} = \frac{i_{out}}{v_{in}}\Big\|_{@R_L=0}$
i_{in} (Norton)	v_{out} (thevinin)	Transresistance Amplifier. control source $R_{MO}\,i_{in}$ ⇒ $R_{mo} = \frac{v_{out}}{i_{in}}\Big\|_{@R_L=\infty}$

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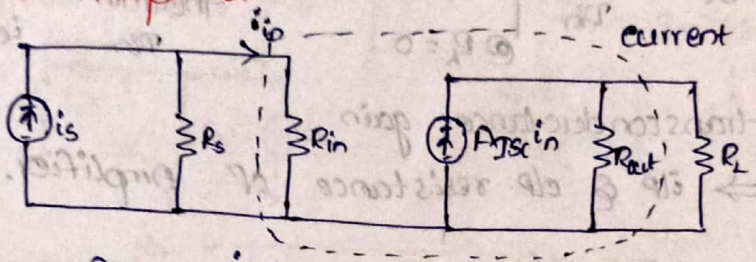
Equivalent ckts Backside.

Voltage Amplifier



$$A_{Vo} = \frac{V_{out}}{V_{in}}\Big|_{@R_L=\infty} \quad ; \quad A_{Vs} = A_{Vo} \cdot \frac{R_L}{R_L + R_{out}} \cdot \frac{R_{in}}{R_{in} + R_s}$$

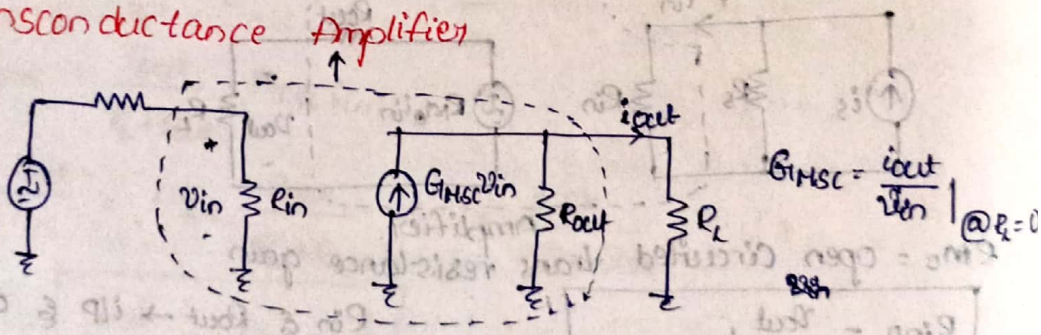
Current Amplifier



$$A_{ISC} = \frac{i_{out}}{i_{in}}\Big|_{@R_L=0}$$

$$A_{IS} = A_{ISC} \frac{R_{out}}{R_{out} + R_L} \cdot \frac{R_s}{R_s + R_{in}}$$

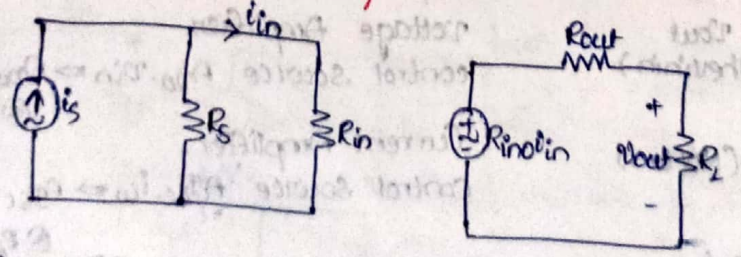
transconductance Amplifier



$$G_{mSC} = \frac{i_{out}}{V_{in}}\Big|_{@R_L=0}$$

$$\frac{i_{out}}{V_{in}} = G_{mSC} \cdot \frac{R_{out}}{R_{out} + R_L} \cdot \frac{R_{in}}{R_{in} + R_s}$$

transresistance Amplifier



$$R_{mo} = \frac{V_{out}}{i_{in}}\Big|_{@R_L=\infty}$$

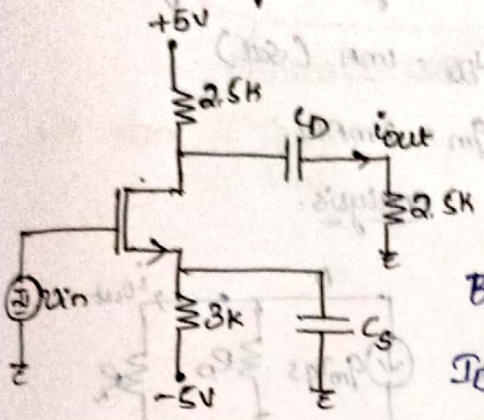
$$\frac{V_{out}}{i_{in}} = R_{ms} = R_{mo} \cdot \frac{R_L}{R_{out} + R_L} \cdot \frac{R_s}{R_s + R_{in}}$$

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23/12/22

Find the transconductance gain of the Amplifier as shown in fig. Assume C_D, C_S are sc for our freq. of intrest.

$\mu_n C_{ox} = 1mA/V^2$, $V_{tn} = 1V$, $\frac{W}{L} = 2$



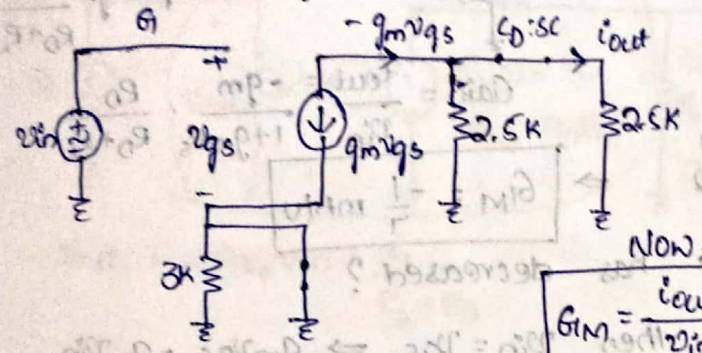
By Observation,

We have to find $\frac{i_{out}}{v_{in}} = G_M$ - A/V

By using dc Analysis:

$I_{DQ} = 1mA$, $g_m = 2mA/V$.

Using ac Analysis:



$-v_{in} + v_{gs} = 0$

$v_{in} = v_{gs}$

$i_{out} = -\frac{g_m v_{gs}}{\lambda}$

NOW,

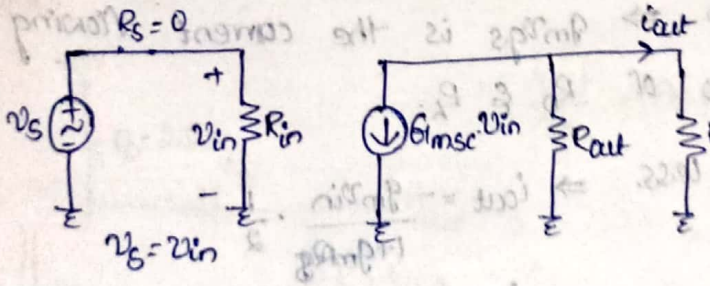
$$G_M = \frac{i_{out}}{v_{in}} = -\frac{g_m}{\lambda} = -1mA/V$$

ii, Write the above ckt into its Equivalent form two port nw.

Transconductance Amplifier.

ilp : v_{in} olp : i_{out}

$i_{out} = -\frac{G_{msc} v_{in} . R_{out}}{R_{out} + R_L}$



$\frac{i_{out}}{v_{in}} = G_{msc} \frac{R_{out}}{R_{out} + R_L}$

$= -2m \times \frac{2.5k}{2.5k + 2.5k}$

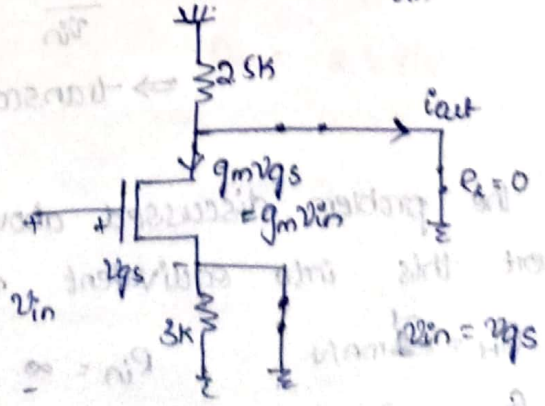
$G_M = \frac{i_{out}}{v_{in}} = -1mA/V$

$G_{msc} = \frac{i_{out}}{v_{in}}$ @ $R_L = 0$

Short circuit transconductance gain

$i_{out} = -g_m v_{gs}$.

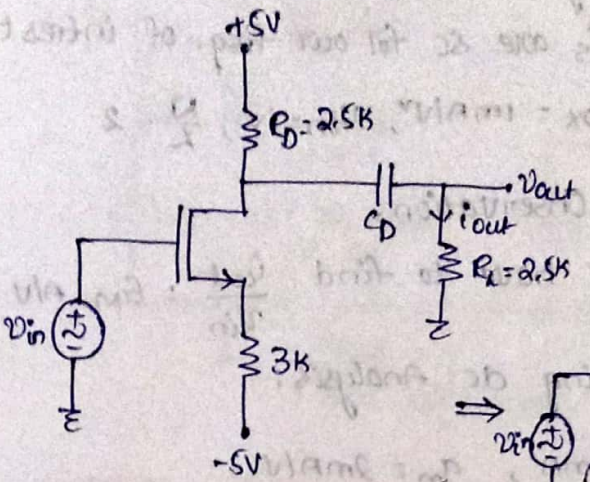
$G_{msc} = \frac{i_{out}}{v_{in}} = -g_m$



$v_{in} = v_{gs}$

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Problem: For the above problem if C_S is removed? then transconductance gain?

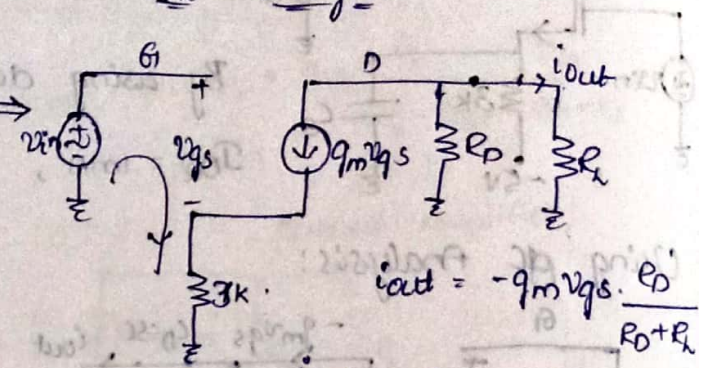


By doing DC Analysis:

I_{DQ} = 1mA (Sat)

g_m = 2 mA/V.

AC Analysis.



$v_{in} = v_{gs} + g_m v_{gs} \cdot R_S$

$v_{gs} = \frac{v_{in}}{1+g_m R_S}$

$i_{out} = -g_m v_{gs} \cdot \frac{R_D}{R_D+R_L}$

$Gain = \frac{i_{out}}{v_{in}} = \frac{-g_m}{1+g_m R_S} \cdot \frac{R_D}{R_D+R_L}$

$\Rightarrow G_M = \frac{-2m}{1+2m\times 3K} \cdot \frac{1}{2}$ $\Rightarrow$ $\boxed{G_M = -\frac{1}{7}\ mA/V}$

Why transconductance has decreased?

$\Rightarrow$ If 'C_S' is present then $v_{in} = v_{gs} \Rightarrow g_m v_{gs} = g_m v_{in}$ flows through the parallel combo of R_D & R_L.

$\Rightarrow$ When 'C_S' is removed then $v_{gs} = \frac{v_{in}}{1+g_m R_S} \Rightarrow v_{gs} < v_{in}$

$\Rightarrow g_m v_{gs} < g_m v_{in} \Rightarrow g_m v_{gs}$ is the current flowing the parallel combo of R_D & R_L.

Hence i_{out} is less. $\Rightarrow i_{out} = -\frac{g_m v_{in}}{1+g_m R_S} \cdot \frac{1}{2}$

$\Rightarrow \frac{i_{out}}{v_{in}}$ is less

$\Rightarrow$ transconductance decreases.

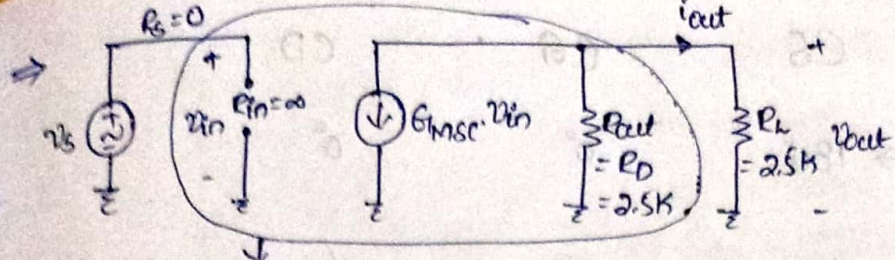
Note:-

* For the problem discussed above which includes 'C_S' convert this into equivalent voltage Amplifier.

Sol:- $G_M = -\frac{1}{7}\ mA/V$, $R_{in} = \infty$

$G_{MSC} = -2\ mA/V$ $R_{out} = R_D = 2.5\ K\Omega$

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transconductance Amplifier.

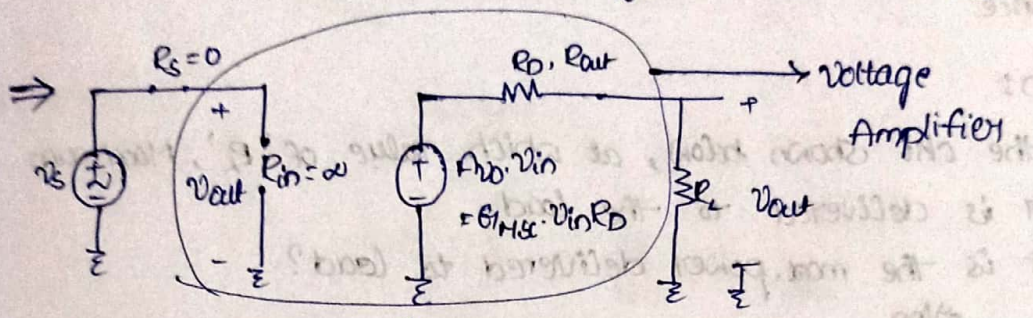
We want $\frac{v_{out}}{v_{in}}$.

@ $R_L = \infty \Rightarrow i_{out} = 0 \Rightarrow v_{out} = -G_{mSC} v_{in} R_D$

$$A_{v_0} = \left.\frac{v_{out}}{v_{in}}\right|_{@ R_L = \infty}$$

$$A_{v_0} = -G_{mSC} \cdot R_D$$

$$A_{v_0} = +2m \times 2.5K \Rightarrow \boxed{A_{v_0} = 5\ V/V}$$

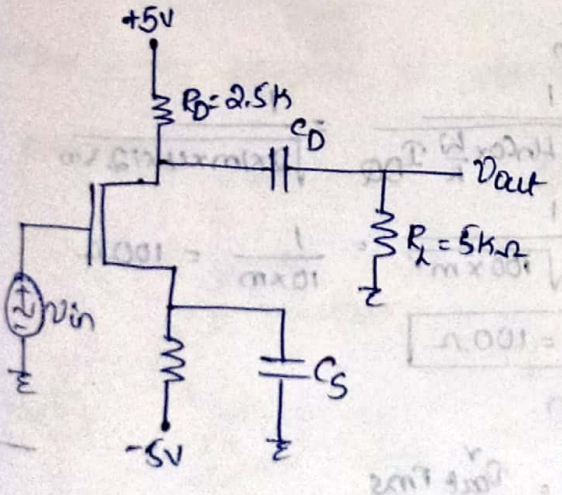


$$v_{out} = -A_{v_0} v_{in} \times \frac{R_L}{R_L + R_D}$$

$$\frac{v_{out}}{v_{in}} = -A_{v_0} \cdot \frac{R_L}{R_L + R_D}$$

$$\boxed{A_v = -5/2 = -2.5\ V/V}$$

Check:-



$$\frac{v_{out}}{v_{in}} = A_v = -g_m (R_D \| R_L)$$

$$= -2m [2.5K \| 2.5K]$$

$$= -2m [1.25K]$$

$$A_v = -2.5\ V/V$$

$\Rightarrow$ Hence verified.

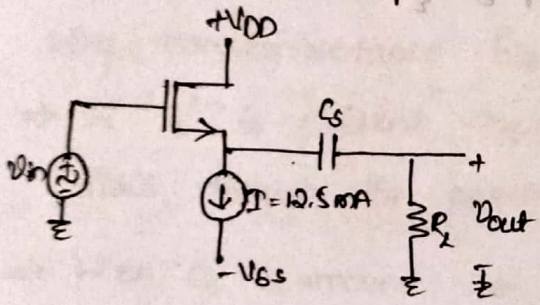
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	CS	CG	CD
i/p & o/p phase shift	180°	0°	0°
Voltage Buffer	×	×	✓
Current Buffer	×	✓	×
least i/p resistance	×	✓ Source terminal	×
least o/p resistance	×	×	✓ Source

Problem:

i, For the ckt shown below, at which value of 'R_L', Maximum power is delivered to the load.

ii, What is the max. power delivered to load?



Given $\mu_n C_{ox} = 1mA/V^2$

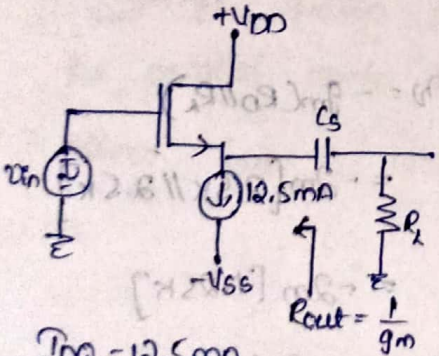
$V_{tn} = 1V$

$\frac{W}{L} = 2$

$\lambda = 0$

$V_{in} = 0.5 \sin \omega t$ volts.

Sol: i, Max. power delivered to R_L is when $R_L = R_{out}$.



$R_L = \frac{1}{g_m}$

$R_L = \frac{1}{\sqrt{2 \mu_n C_{ox} \frac{W}{L} I_{DQ}}} = \frac{1}{\sqrt{2 \times 1m \times 2 \times 12.5m}}$

$= \frac{1}{\sqrt{100 \times m^2}} = \frac{1}{10 \times m} = 100\Omega$

$I_{DQ} = 12.5mA$

$V_{DQ} = 10V$, $V_{GSQ} = 0 \Rightarrow$ Saturation.

$\Rightarrow \boxed{R_L = 100\Omega}$

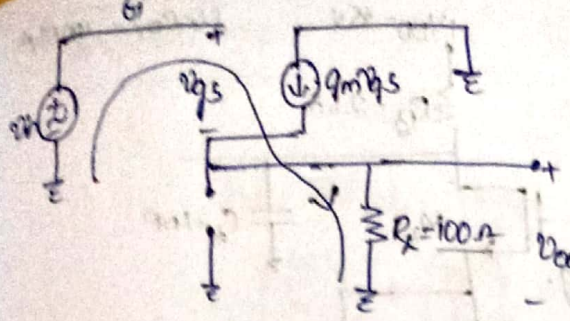
ii, Max. power dissipated in $R_L = \frac{V_{out\,rms}^2}{R_L}$

We have to find $V_{out\,rms} = \frac{V_{out}}{\sqrt{2}}$

Now doing AC analysis:

$g_m = \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_{DQ}} = 10mA/V.$

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$v_{out} = g_m v_{gs} \cdot R_L$

$v_{out} = \frac{g_m R_L}{1+g_m R_L} \cdot v_{in}$

$\Rightarrow v_{out} = \frac{10m \times 100}{1+10m \times 100} \cdot v_{in}$

$\Rightarrow v_{out} = \frac{1}{1+1} v_{in}$

$v_{out} = \frac{1}{8} v_{in}$

$v_{out} = \frac{1}{8} \times 0.5 \sin \omega t$ volts

$v_{out} = \frac{1}{4} \sin \omega t$

$v_{out\,rms} = \frac{V_m}{\sqrt{2}} = \frac{\frac{1}{4}}{\sqrt{2}} = \frac{1}{4\sqrt{2}}$

$-v_{in} + v_{gs} + g_m v_{gs} R_L = 0$

$v_{gs} = \frac{v_{in}}{1+g_m R_L}$

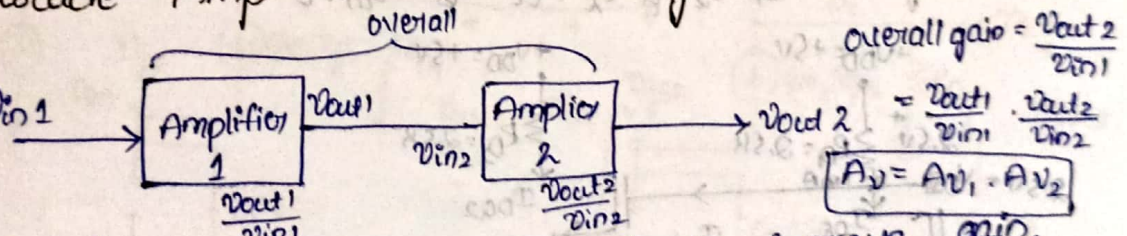
$\frac{10m \times 100}{1+10m \times 10V}$

Max. power dissipated in R_L $= \frac{v_{out\,rms}^2}{R_L}$

$= \frac{\left(\frac{1}{4\sqrt{2}}\right)^2}{100} = \frac{\frac{1}{32}}{100} = \frac{1}{3200}$

∴ Max. power delivered to $R_L = 0.312$ mW

Cascade Amplifier & Multistage Amplifier.



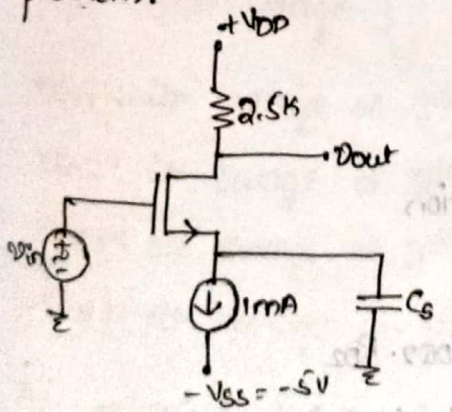
overall gain $= \frac{v_{out\,2}}{v_{in1}}$

$= \frac{v_{out1}}{v_{in1}} \cdot \frac{v_{out2}}{v_{in2}}$

$A_V = A_{V_1} \cdot A_{V_2}$

The main purpose of cascading is to improve gain.

problem:



Given. $\mu_n C_{ox} = 1mA/V^2$; $V_{tn} = 1V$

$\frac{W}{L} = 2$, $\lambda = 0$

By doing dc Analysis

$I_{DQ} = 1mA$; $V_{DQ} = 2.5V$

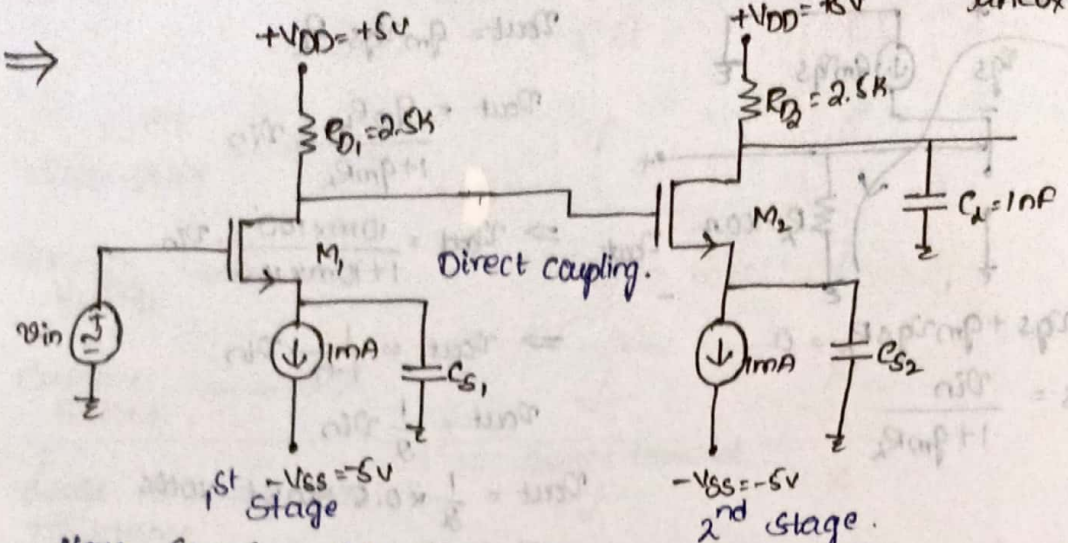
$V_{GQ} = 0V$ ⇒ Saturation

$A_V = \frac{v_{out}}{v_{in}} = -g_m R_D = -5 V/V$

If two such above amplifiers are cascaded then what is the overall gain?

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$\mu_n C_{ox} = 1mA/V^2$

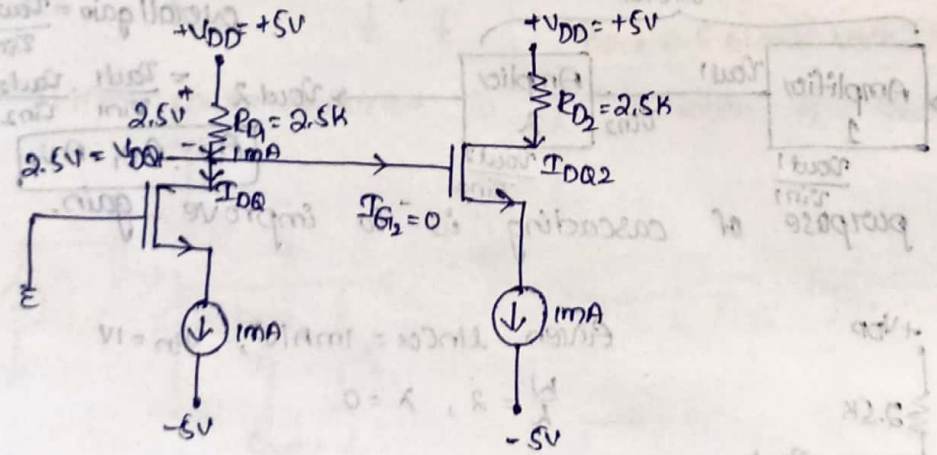


Here $C_{S1} = C_{S2} = 3.71\ \mu F$

→ While finding overall voltage gain

1. DO DC Analysis then find Q. point in both the stages & calculate g_{m1} & g_{m2}
   - g_{m1} ↓ transconductance of M_1
   - g_{m2} ↓ transconductance of M_2.
2. For Amplification: MOS-fets M_1 & M_2 has to be in saturation region.

DC Analysis: C_{S1}, C_{S2} & C_L : OC & $v_{in} = 0$



By observation:

$I_{DQ1} = 1mA$

$V_{DQ1} = V_{DD} - I_{DQ1} R_{D1}$

$= 5V - 1m(2.5K)$

$V_{DQ1} = 2.5V$

$g_{m1} = \sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right)_1 I_{DQ1}}$

$= \sqrt{2 \times 1m \times 2 \times 1m}$

By observation

$I_{DQ2} = 1mA$

$V_{DQ2} = V_{DD} - I_{DQ2} \cdot R_{D2}$

$= 5V - 1m(2.5K)$

$V_{DQ2} = 2.5V$

$V_{DQ2} = V_{DQ2} = 2.5V$

$g_m = \sqrt{2 \mu_n C_{ox} \left(\frac{W}{L}\right)_2 I_{DQ2}}$

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$g_{m_1} = 2mA/V$

$g_m = \sqrt{2 \times 1m \times 2 \times 1m}$

$g_{m_2} = 2mA/V$

$I_{D1} = I_{D2} = 1mA$

$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 2$ (Given

* While calculating overall voltage gain, we have to start from last stage & moves towards 1st stage.

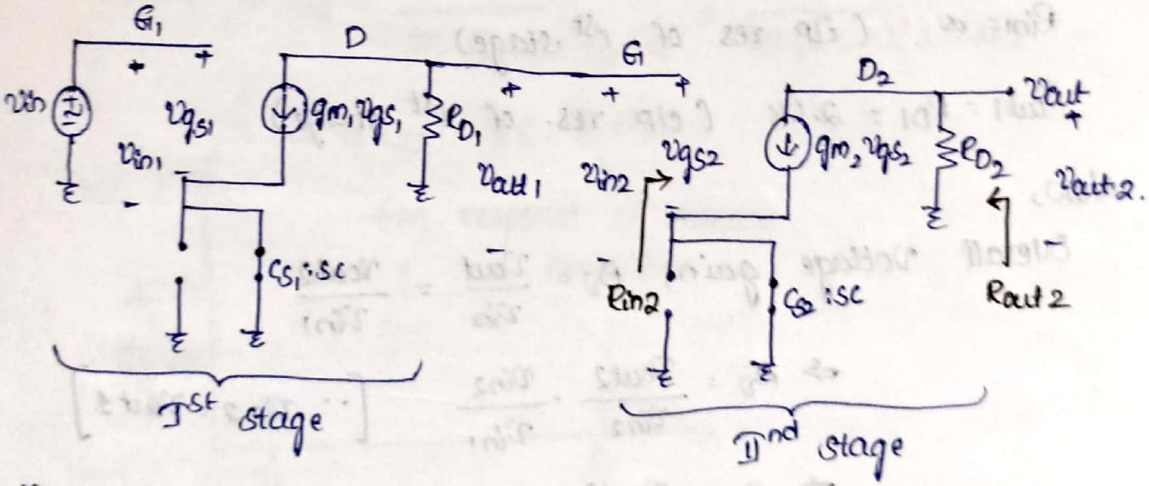
Eg:- If 3 stages are cascaded

⇒ Start from 3rd ⇒ 2nd ⇒ 1st stage.

This is because second & 3rd stage may load 2nd & simultaneously 2nd stage may load 1st stage.

i.e., while calculating the 1st stage gain we need to know the i/p res. of second stage.

AC Analysis:



v_{in1} : i/p voltage of I st stage

v_{in2} : i/p voltage of II nd stage

v_{out1} : o/p voltage of I st stage

v_{out2} : o/p voltage of II nd stage.

By observation:

$v_{out1} = v_{in2}$

$v_{in} = v_{in1} = v_{gs1}$

$v_{out} = v_{out2}$

By principle start from 2nd stage

By observation: $v_{in2} = v_{gs2}$ (2nd stage)

$v_{out2} = -g_{m2} v_{gs2} \cdot R_{D2}$

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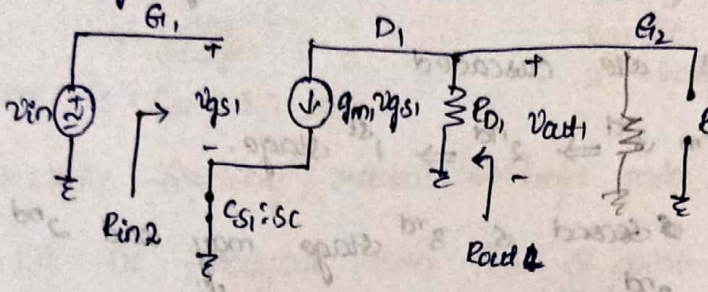
$$A_{V_2} = \frac{v_{out2}}{v_{in}} = -g_{m_2} \cdot R_{D2} = -2m(2.5K)$$

$$\Rightarrow \boxed{A_{V_2} = -5\,V/V}$$ 2nd stage voltage gain.

$R_{in2} = \infty$ → i/p res. of II nd stage

$R_{out2} = R_{D2} = 2.5K\Omega$ → o/p res. of II nd stage

I st stage



$R_{in1} = \infty$

$R_{out1} = R_{D1} = 2.5k$

By observation: $v_{in} = v_{in1} = v_{gs1}$

$$v_{out1} = -g_{m_1} v_{gs_1} R_{D1}$$

I st stage voltage gain $A_{V_1} = \frac{v_{out1}}{v_{in_1}} = -g_{m_1} R_{D1} = -5\,V/V$

Here II nd stage is not loading I st stage. $[\because R_{in2} = \infty]$

$R_{in1} = \infty$ (i/p res. of 1st stage)

$R_{out1} = R_{D1} = 2.5K$ (o/p res. of 1st stage)

Now,

Overall voltage gain, $A_V = \frac{v_{out}}{v_{in}} = \frac{v_{out2}}{v_{in1}}$

$$\Rightarrow A_V = \frac{v_{out2}}{v_{in2}} \cdot \frac{v_{in2}}{v_{in1}} \quad [\because v_{in2} = v_{out1}]$$

$$\Rightarrow A_V = \frac{v_{out2}}{v_{in2}} \cdot \frac{v_{out1}}{v_{in1}}$$

$$A_V = A_{V_2} \cdot A_{V_1}$$

$$\Rightarrow A_V = -5 \cdot -5V$$

$$\Rightarrow \boxed{A_V = +25\,V/V}$$

i/p & o/p are in same phase. Why?

1st stage —— 2nd stage $\Rightarrow$ 360° or 0°

180° 180° (same phase)

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Now, find f_H & f_L the given cascade connected mosfets.

$R_{across, C_L} = R_{D2} = 2.5\,K\Omega$

Now, f_H due to $C_L = \frac{1}{2\pi . R_{across.C_L} . C_L} = \frac{1}{2\pi (2.5K)(1nF)}$

f_H, due to $C_L = 63661\,Hz = 63.66\,KHz.$

Now,

$R_{across, C_{S1}} = \frac{1}{g_{m1}} = \frac{1}{2m} = 0.5K\Omega$

f_L, due to $C_{S1} = \frac{1}{2\pi . R_{across, C_{S1}} . C_{S1}} = \frac{1}{2\pi \times (0.5K)(3.7\mu)}$

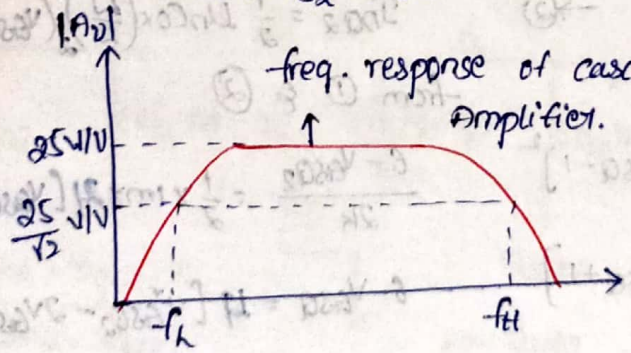
f_L due to $C_{S1} = 85.79\,Hz.$

Similarly,

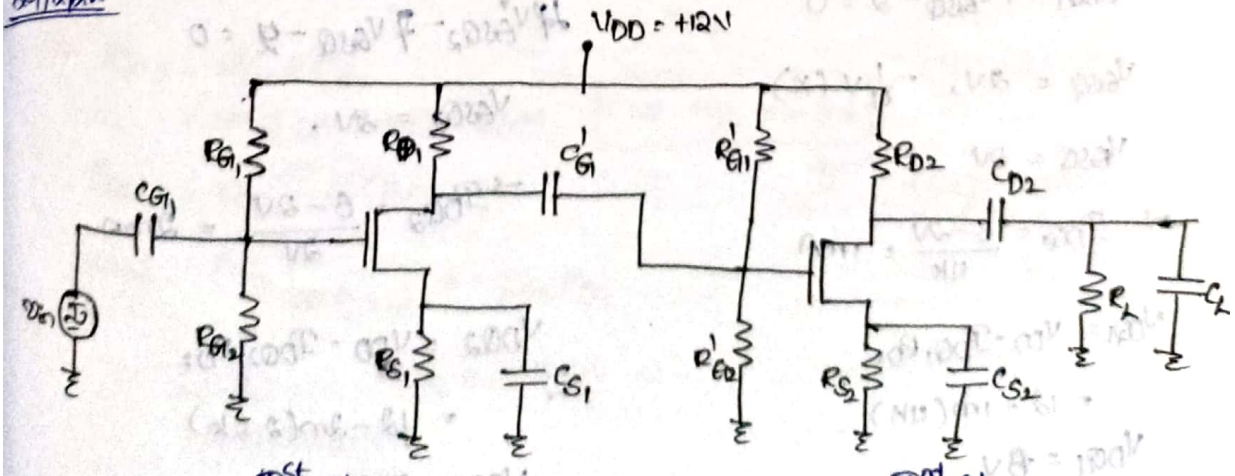
$R_{across, C_{S2}} = \frac{1}{g_{m2}} = \frac{1}{2m} = 0.5\,K\Omega$

f_L, due to $C_{S2} = \frac{1}{2\pi . R_{across, C_{S2}} . C_{S2}} = \frac{1}{2\pi (0.5K)(3.7\mu)}$

f_L due to $C_{S2} = 85.79\,Hz.$



21/2/22



RC-Coupled Amplifier.

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$R_{G_1} = R_{G_2} = 1M\Omega$, $R_{S_1} = 4K\Omega$ $R_{S_2} = 2K\Omega$ $V_{t1} = V_{t2} = 1V$

$R'_{G_1} = R'_{G_2} = 1M\Omega$ $R_{D_2} = 4K\Omega$ $R_{D_2} = 2.5K\Omega$ $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 2$

$\left(\frac{W}{L}\right)_2 = 4$

$R_L = 10K\Omega$, $C_{G_1} = C_{G_2} = C_{D_2} = \infty = C_{G_1}$ (very high) for low freq. of intrest these caps are

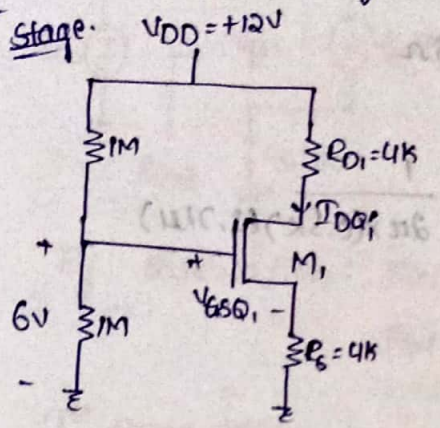
$C'_{G_1} = 0.01\mu F$, $C_L = 0.1nF$ find overall voltage gain.

Sol:- find Q. point of both stages.

* In DC analysis, all caps are o.c

1st Apply DC Analysis

I stage.



$-6 + V_{GSQ_1} + I_{DQ_1} \cdot 4K = 0$

$I_{DQ_1} = \frac{6 - V_{GSQ_1}}{4K} \rightarrow (1)$

In sat:-

$I_{DQ_1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GSQ_1} - V_{tn})^2 \rightarrow (2)$

from (1) & (2)

$\frac{6 - V_{GSQ_1}}{4K} = \frac{1}{2} \times 1m \times 2 [V_{GSQ} - 1]^2$

$6 - V_{GSQ_1} = 4[V^2_{GSQ} - 2V_{GSQ} + 1]$

$4V^2_{GSQ_1} - 7V_{GSQ} - 2 = 0$

$V_{GSQ} = 2V, -\frac{1}{4}V$ (X)

$V_{GSQ} = 2V$

$\Rightarrow I_{DQ_1} = \frac{6-2V}{4K} = 1mA$

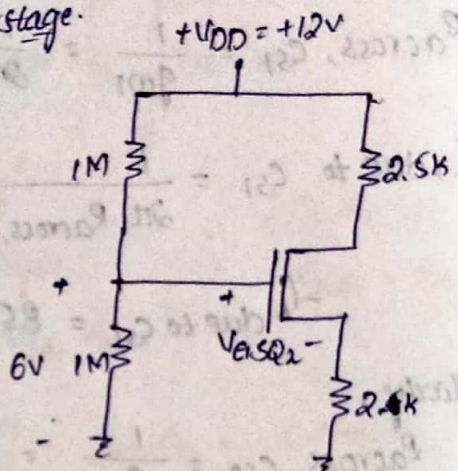
$V_{DQ_1} = V_{DD} - I_{DQ_1} R_{D_1}$

$= 12 - 1m(4K)$

$V_{DQ_1} = 8V$

$V_{GQ_1} < V_{DQ} \Rightarrow$ sat.

II nd stage.



$-6 + V_{GSQ_2} + I_{DQ_2} \cdot 2K = 0$

$I_{DQ_2} = \frac{6 - V_{GSQ_2}}{2K} \rightarrow (1)$

In sat:

$I_{DQ_2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GSQ_2} - V_{tn})^2 \rightarrow (2)$

from (1) & (2)

$\frac{6 - V_{GSQ_2}}{2K} = \frac{1}{2} \times 1m \times 2[V_{GSQ_2} - 1]^2$

$6 - V_{GSQ} = 2[V^2_{GSQ_2} - 2V_{GSQ_2} + 1]$

$2V^2_{GSQ_2} - 3V_{GSQ} - 4 = 0$

$V_{GSQ_2} = 2V.$

$\Rightarrow I_{DQ_2} = \frac{6-2V}{2V} = 2mA$

$V_{DQ_2} = V_{DD} - I_{DQ_2} R_{D_2}$

$= 12 - 2m(2.5K)$

$V_{DQ_2} = 7V$

$V_{GQ_2} < V_D \Rightarrow$ sat.

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In sat:

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{DQ1}}$$

$$\boxed{g_{m1} = 9\,mA/V}$$

In sat:

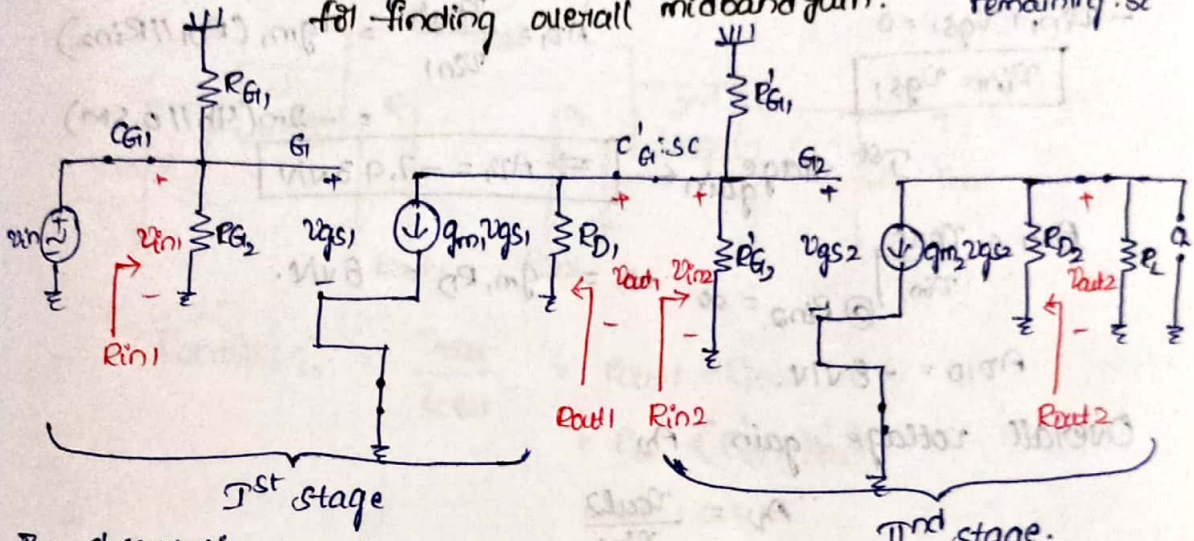
$$g_{m2} = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right) I_{DQ2}}$$

$$\boxed{g_{m2} = 4\,mA/V}$$

for finding voltage gain:

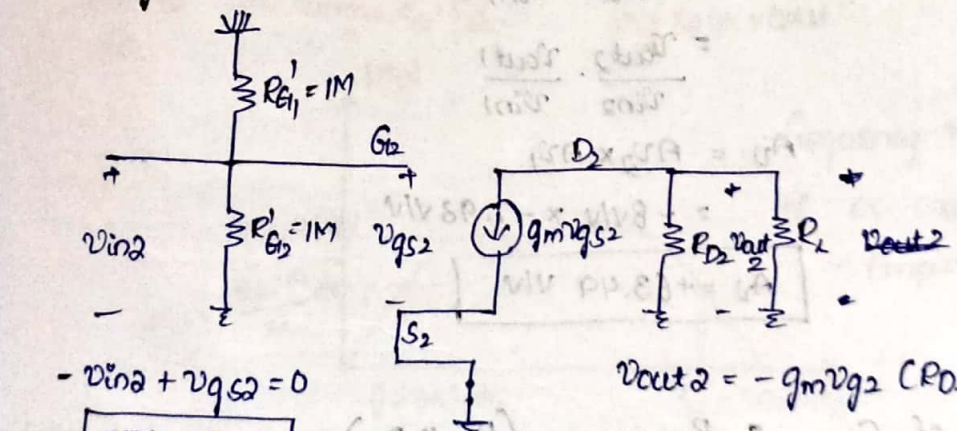
Start with last stage here it is second stage.

⇒ overall small signal model of Amplifier. for finding overall midband gain. C_d: OC, remaining: SC



By observation: $v_{out1} = v_{in2}$

II nd stage



$$-v_{in2} + v_{gs2} = 0$$

$$\boxed{v_{in2} = v_{gs2}}$$

$$v_{out2} = -g_m v_{g2} (R_{D2} \parallel R_L)$$

$$\Rightarrow \frac{v_{out2}}{v_{in2}} = A_{V2} = -g_m (R_{D2} \parallel R_L)$$

$$= -4m (2.5K \parallel 10K)$$

$$\Rightarrow A_{V2} = -8V$$

II nd stage gain

⇒ $R_{in2} = R'_{G1} \parallel R'_{G2}$

$= 1M \parallel 1M \Rightarrow R_{in} = 0.5M$

$R_{out2} = R_{D2} = 2.5K\Omega$

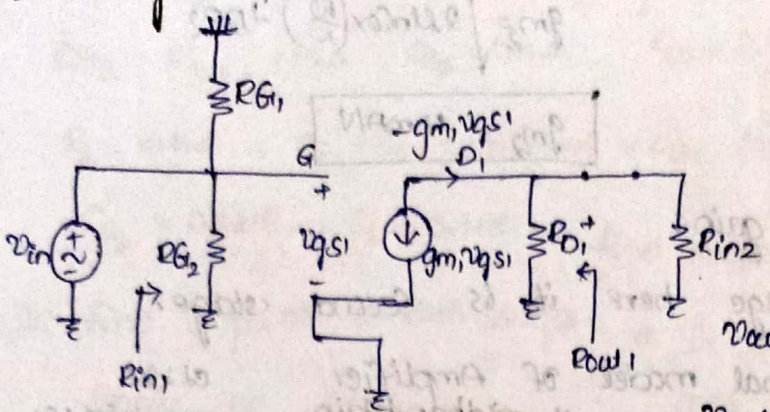
NOW, $A_{V2}\big|_{@R_L=\infty} = -g_{m2} R_{D2}$

$A_{V20} = -10\,V/V$

Open circuited voltage gain

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1st Stage.



$R_{in1} = R_{G1} // R_{G2} = 1M // 1M$

$R_{in1} = 0.5M\Omega$

$R_{out1} = R_{D1} = 4K\Omega$

$v_{out1} = -g_{m1} v_{gs1} (R_{D1} // R_{in2})$

$-v_{in1} + v_{gs1} = 0$

$\boxed{v_{in1} = v_{gs1}}$

$A_{v1} = \frac{v_{out1}}{v_{in1}} = -g_{m1} (R_{D1} // R_{in2})$

$= -2m(4K // 0.5M)$

1st stage gain $\Rightarrow \boxed{A_{v1} = -7.93 \text{ v/v}}$

$A_{v1} = \left.\frac{v_{out}}{v_{in}}\right|_{@R_{in2} = \infty} = -g_{m1} R_D = -8 \text{ v/v}.$

$A_{v10} = -8 \text{ v/v}.$

Overall voltage gain A_v

$$A_v = \frac{v_{out2}}{v_{in1}}$$

$$= \frac{v_{out2}}{v_{in2}} \cdot \frac{v_{in2}}{v_{in1}}$$

$$= \frac{v_{out2}}{v_{in2}} \cdot \frac{v_{out1}}{v_{in1}}$$

$A_v = A_{v2} \times A_{v1}$

$= -8 \text{ v/v} \times -7.93 \text{ v/v}$

$\boxed{A_v = +63.49 \text{ v/v}}$

f_H

f_H : B/c of C_L. & $R_{across, C_L} = (R_{D2} // R_L) = 2.5K // 10K = 2K$

$\Rightarrow f_H = \frac{1}{2\pi R_{across C_L} \cdot C_L} = \frac{1}{2\pi (R_{D2} // R_L) \cdot C_L}$

$= \frac{1}{2\pi (2K) \times 0.1nF} = 0.795 MHz = 795 kHz$

$\Rightarrow \boxed{f_H = 795 \text{ kHz}}$

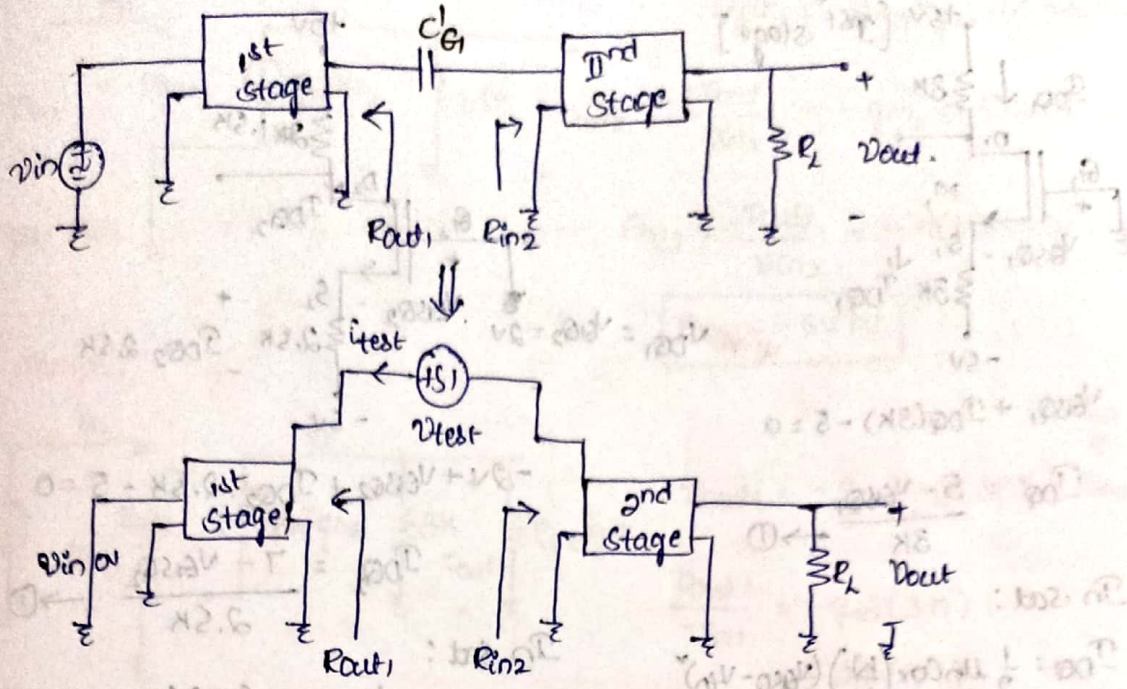
f_L

f_L : B/c of $C_{G1}, C_{G}, C_{S2}, C_{D1}, C'_{G}$ But $C_{G1}, C_{S1}, C_{S2}, C_{D2}$ are very very high.

$\Rightarrow f_L$ due to above caps near to zero.

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Hence here f_L is decided by C'_{G_1}.



$$R_{across, C'_{G_1}} = \frac{V_{test}}{i_{test}} = R_{out1} + R_{in2}$$

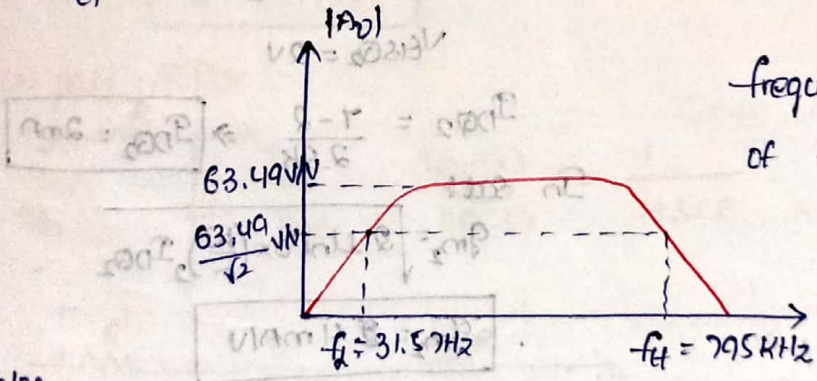
$$= R_{D1} + (R'_{G_1} \,//\, R'_{G_2})$$

$$= 4K + 0.5M$$

$$\simeq 504\ K\Omega$$

$$\Rightarrow f_L = \frac{1}{2\pi \cdot R_{across, C'_{G_1}} \cdot C'_{G_1}} = \frac{1}{2\pi \times 504K \times 0.01\mu} = 31.57\ Hz.$$

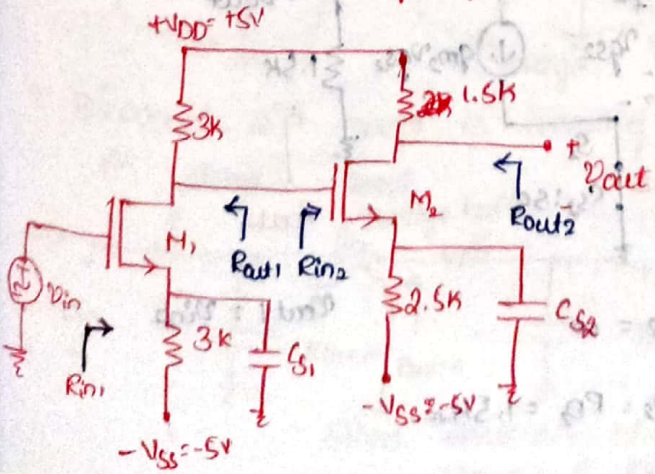
due to C'_{G_1}



frequency response of RC coupled Amplifier.

25/2/22

Find the overall voltage gain of cascaded Amplifier ~~& find f_L, f_H~~.



$\mu_n C_{ox}$ = 1mA/V²

μ_n = 1V

$\left(\frac{W}{L}\right)_1 = 2$

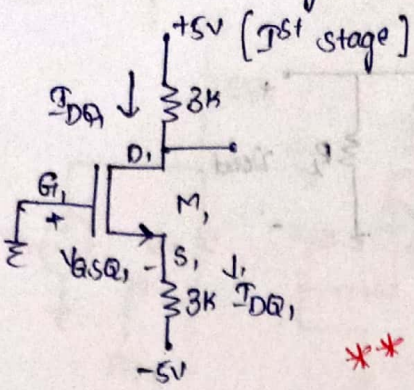
$\left(\frac{W}{L}\right)_2 = 4$

$\lambda = 0$

C_{S_1} & C_{S_2} are shorted for our freq. of intrest

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Sol: DC Analysis.



$V_{GSQ_1} + I_{DQ}(3K) - 5 = 0$

$$I_{DQ} = \frac{5 - V_{GSQ_1}}{3K} \rightarrow (1)$$

In sat:

$$I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GSQ} - V_{th})^2 \rightarrow (2)$$

from (1) & (2)

$I_{DQ_1} = 1mA$,

$V_{DQ} = 2V$

$V_{GD} = 0 \Rightarrow$ saturation.

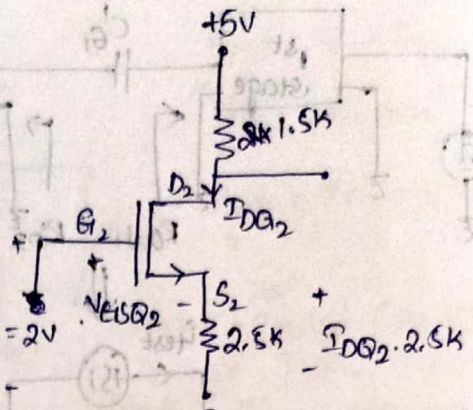
Sol:

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_{DQ_1}}$$

$$\boxed{g_{m_1} = 2mA/V}$$

$* V_{DQ_1} = V_{GSQ_2}$

II nd stage.



** $V_{DQ_1} = V_{GSQ_2} = 2V$

$-2V + V_{GSQ_2} + I_{DQ_2}.2.5K - 5 = 0$

$$I_{DQ_2} = \frac{7 - V_{GSQ_2}}{2.5K} \rightarrow (1)$$

In sat:

$$I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GSQ} - V_{th})^2 \rightarrow (2)$$

from (1) & (2)

$$\frac{7 - V_{GSQ_2}}{2.5K} = \frac{1}{2} 1m \times 4 (V_{GSQ_2} - V_{th})^2$$

$7 - V_{GSQ_2} = 5(V_{GSQ_2}^2 - 2V_{GSQ_2} + 1)$

$5V_{GSQ_2}^2 - 9V_{GSQ_2} - 2 = 0$

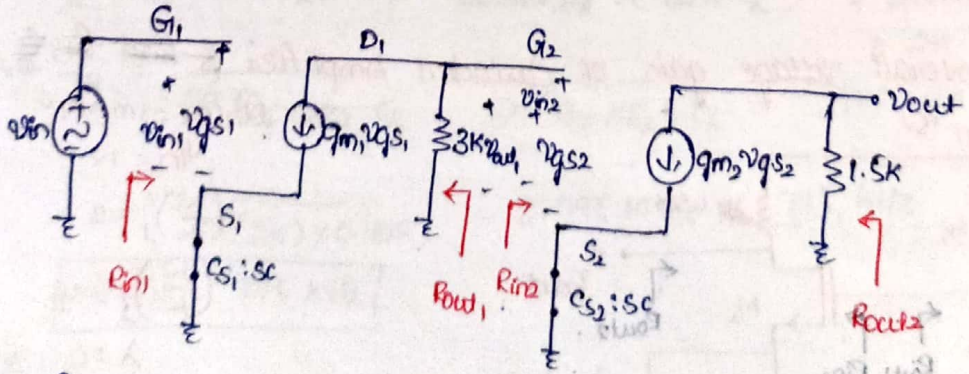
$V_{GSQ_2} = 2V$

$$I_{DQ_2} = \frac{7-2}{2.5K} \Rightarrow \boxed{I_{DQ_2} = 2mA}$$

In sat:

$$g_{m_2} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_2 I_{DQ_2}}$$

$$\boxed{g_{m_2} = 2.4 mA/V}$$



$R_{in_1} = \infty$

$R_{out_1} = R_{D_1} = 3K\Omega$

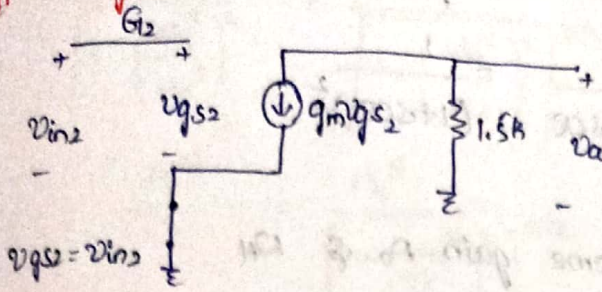
$R_{in2} = \infty$

$R_{out_2} = R_{D_2} = 1.5K\Omega$

$v_{out1} = v_{in2}$

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IInd stage:



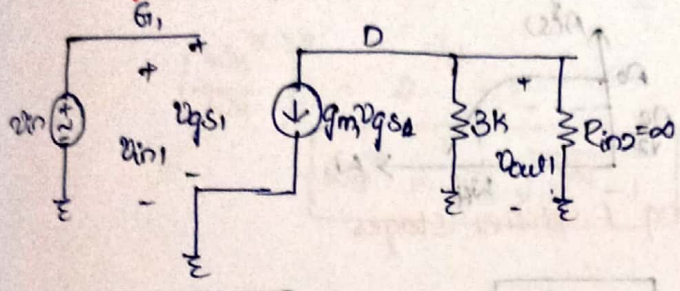
$v_{out_2} = -g_{m_2} v_{gs_2} \cdot 1.5k\Omega$

$\frac{v_{out}}{v_{in_2}} = -g_{m_2}(1.5k\Omega)$

$A_{V_2} = \frac{v_{out2}}{v_{in2}} = -4(1.5k\Omega)$

$\boxed{A_{V_2} = -6\,V/V}$

Ist stage:



$v_{out1} = -g_m v_{gs_1} (3K \,//\, R_{in_2})$ ($R_{in_2} \uparrow \infty$)

$\frac{v_{out1}}{v_{in1}} = -g_m(3K)$

$= -2m(3K)$

$v_{in1} = v_{in} = v_{gs1}$

$\boxed{\frac{v_{out1}}{v_{out1}} = A_{V_1} = -6\,V/V}$

overall voltage gain:

$A_V = \frac{v_{out2}}{v_{in2}} \cdot \frac{v_{in2}}{v_{in1}} = \frac{v_{out2}}{v_{in2}} \cdot \frac{v_{out1}}{v_{in1}}$

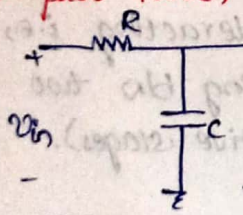
$\because v_{in} = v_{in1}$

$v_{out1} = v_{in2}$

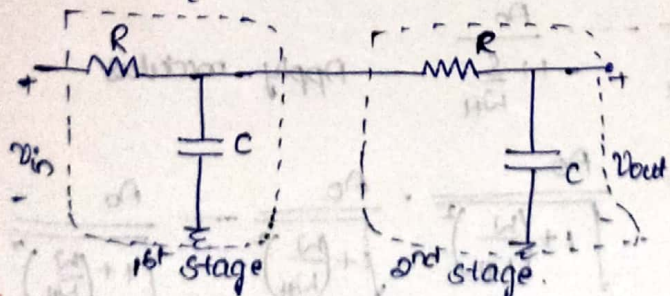
$A_V = -6\,V/V\,(-6\,V/V)$

$\boxed{A_V = 36\,V/V}$

Low pass filter



$\frac{v_{out(s)}}{v_{in(s)}} = \frac{1}{1+sCR}$



as we did earlier,

$A_V = A_{V1} \cdot A_{V2}$

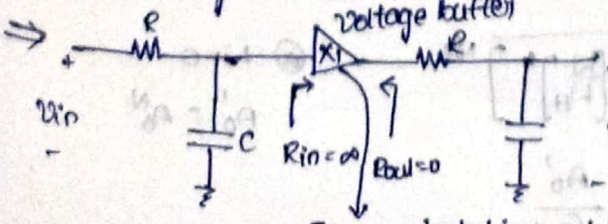
But here

$\frac{v_{out(s)}}{v_{in(s)}} \neq \frac{1}{1+sCR} \cdot \frac{1}{1+sCR}$

* Because 2nd stage is loading 1st stage.

$\Leftarrow \frac{v_{out(s)}}{v_{in(s)}} \neq \frac{1}{(1+sCR)^2}$

$\Rightarrow$ ideal voltage buffer



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i.e., Second stage is not loading first stage.

$$\Rightarrow \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{1+sCR} \cdot \frac{1}{1+sCR} = \frac{1}{(1+sCR)^2}$$

Similarly

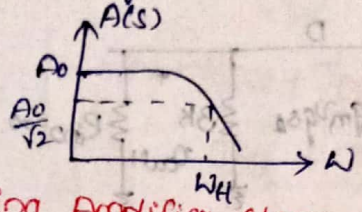
An Amplifier is having some gain A_0 & ω_H

$$A(s) = \frac{A_0}{1+\frac{s}{\omega_H}}$$

dc gain $\Rightarrow s=0 \Rightarrow A_0$

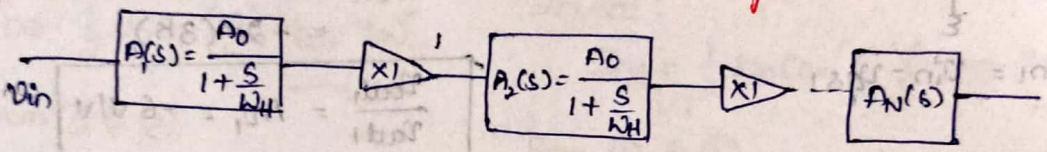
ω_H = Higher cutoff freq.

low pass filter char.



Cascade of

$\Rightarrow$ N-identical non-interacting Amplifier stages



$\Rightarrow$ non-interacting : the next stage is not loading the previous stage.

$A_0 \rightarrow$ dc gain of each stage.

$\omega_H \rightarrow$ Higher cutoff freq. of each stage.

then what is the higher cutoff freq. (ω_H^*) of overall cascade Amplifier.

$$\frac{V_{out}(s)}{V_{in}(s)} = A_1(s).A_2(s)\cdots A_N(s)$$ [$\because$ Non interacting i.e., no loading b/w two consecutive stages).

$$A_N(s) = A_1(s).A_2(s)\cdots A_N(s)$$

$$\frac{A_0'}{1+\frac{s}{\omega_H^*}} = \frac{A_0}{1+\frac{s}{\omega_H}} \cdot \frac{A_0}{1+\frac{s}{\omega_H}} \cdots \frac{A_0}{1+\frac{s}{\omega_H}}$$ Apply modulus

$$|A_N(s)| = \frac{A_0'}{\sqrt{1+\left(\frac{\omega}{\omega_H^*}\right)^2}} = \underbrace{\frac{A_0}{\sqrt{1+\left(\frac{\omega}{\omega_H}\right)^2}} \cdot \frac{A_0}{\sqrt{1+\left(\frac{\omega}{\omega_H}\right)^2}} \cdots \frac{A_0}{\sqrt{1+\left(\frac{\omega}{\omega_H}\right)^2}}}_{N \text{ terms}}$$

$$\frac{A_0'}{\sqrt{1+\left(\frac{\omega}{\omega_H^*}\right)^2}} = \frac{A_0^N}{\left[1+\left(\frac{\omega}{\omega_H}\right)^2\right]^{N/2}}$$

@ $\omega = 0$

$A_0' = A_0^N$

@ $\omega = \omega_H^* \Rightarrow A_N(s) = \frac{A_0'}{\sqrt{2}}$

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$$\frac{A_0}{\sqrt{1+\left(\frac{\omega_H^*}{\omega_H^*}\right)^2}} = \frac{A_0^N}{\left[1+\left(\frac{\omega_H^*}{\omega_H}\right)^2\right]^{N/2}}$$

$$\frac{A_0^N}{\sqrt{2}} = \frac{A_0^N}{\left[1+\left(\frac{\omega_H^*}{\omega_H}\right)^2\right]^{N/2}}$$

$$\left[1+\left(\frac{\omega_H^*}{\omega_H}\right)^2\right]^{N/2} = 2^{1/2} \Rightarrow \left[1+\left(\frac{\omega_H^*}{\omega_H}\right)^2\right] = 2^{1/N}$$

$$\left(\frac{\omega_H^*}{\omega_H}\right)^2 = 2^{1/N} - 1$$

$$\boxed{\omega_H^* = \omega_H \sqrt{2^{1/N}-1}}$$

Higher cutof freq. of overall cascade Amplifier.

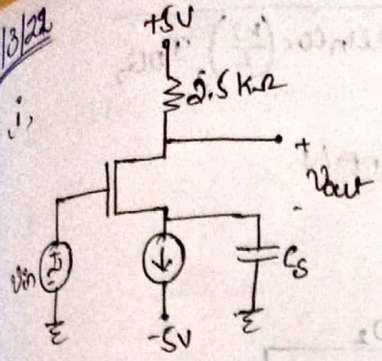
Assignment

N180119
M. Surya kumari.

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2/3/22

i)



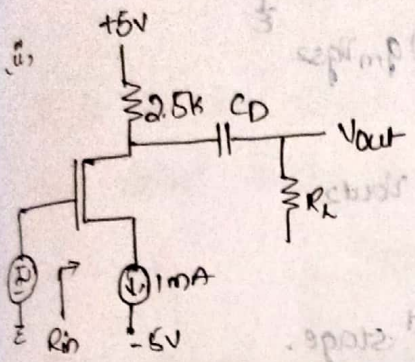
given $\mu_n C_{ox} = 1mA/V^2$

$V_{tn} = 1V$

$\left(\frac{W}{L}\right)_n = 2, \lambda = 0.$

Sol:- $A_v = -g_m R_D = -2m \times 2.5K = -5 V/V.$

ii)



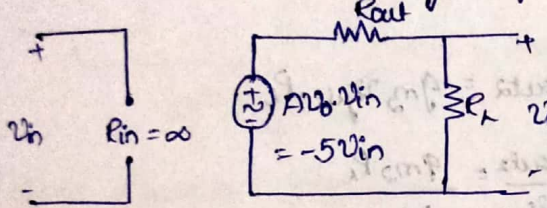
$A_v = ?$

$\frac{V_{out}}{V_{in}} = A_v = -g_m(R_D // R_L)$

$= -2m(2.5K // 2.5K)$

$A_v = -2.5 V/V$

Here R_L is the loading amplifier.

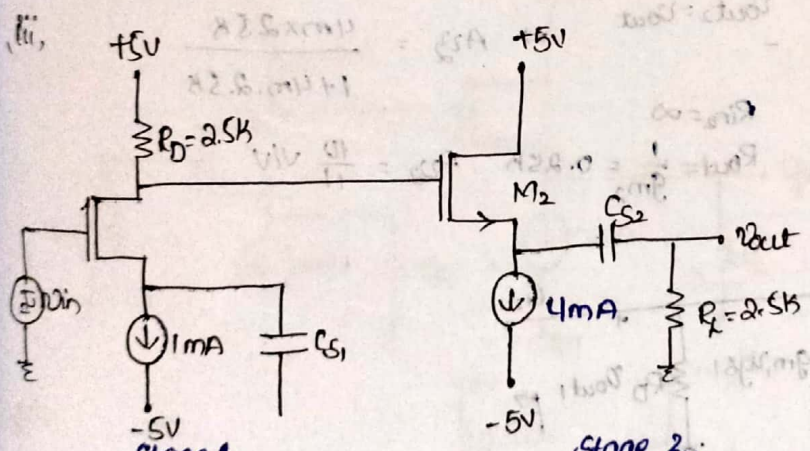


$V_{out} = -5V_{in} \cdot \frac{R_L}{R_L + R_{out}}$

$V_{out} = -2.5 V_{in}$

$\frac{V_{out}}{V_{in}} = -2.5 V/V.$

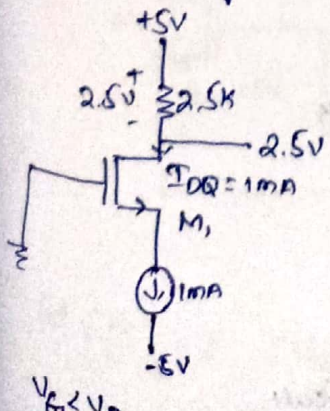
iii)



Stage 1 Stage 2.

DC Analysis

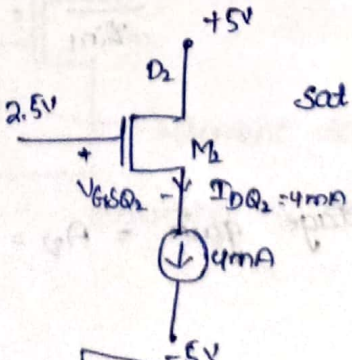
First stage



$V_{G1} < V_D$

$\Rightarrow$ Sat.

second stage



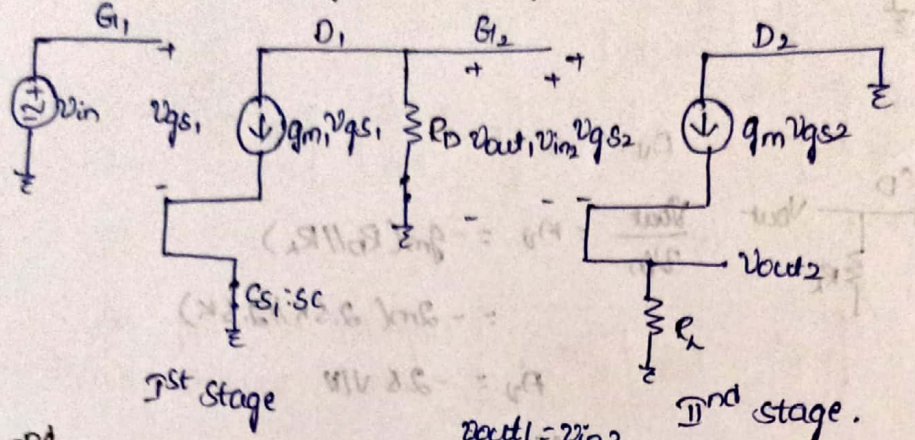
$V_{GSQ_2} = \sqrt{\frac{2I_{DQ_2}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n}} + V_{t2} = 1V + 1V = 2V$

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$g_{m_1} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_{DQ_1}}$ $\quad$ $g_{m_2} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_2 I_{DQ_2}}$

$g_{m_1} = 2mA/V$ $\quad$ $g_{m_2} = 4mA/V$

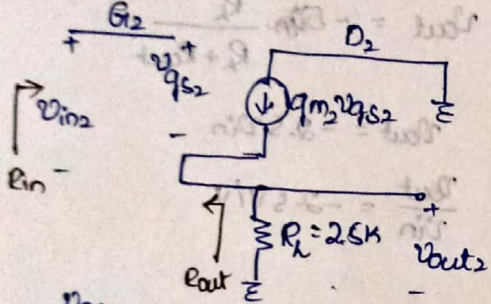
finding small signal voltage gain.



1st stage $\quad$ 2nd stage

$v_{out1} = v_{in2}$

2nd stage



$v_{gs2} = v_{in2} - v_{out2}$

$v_{out2} = g_{m_2} v_{gs2} \cdot R_L$

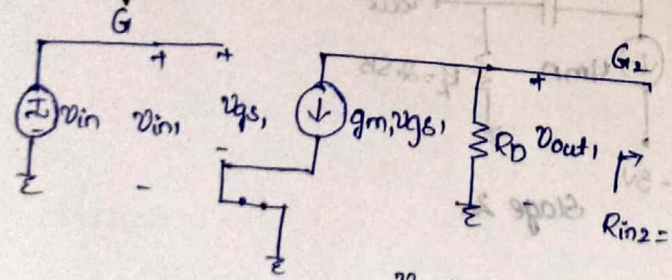
$\frac{v_{out2}}{v_{in2}} = \frac{g_{m_2} R_L}{1 + g_{m_2} R_L}$

$\Rightarrow A_{V_2} = \frac{4m \times 2.5K}{1 + 4m.2.5K}$

$R_{in_2} = \infty$

$R_{out} = \frac{1}{g_{m_2}} = 0.25K$ $\quad$ $A_{V_2} = \frac{10}{11}$ V/V

1st stage



$v_{in} = v_{in_1} = v_{gs_1}$

$v_{out1} = -g_{m_1} v_{gs_1} \cdot R_D$

$\frac{v_{out1}}{v_{in_1}} = A_{V_1} = -g_{m_1} R_D$

$= -2m \times 2.5K$

$\Rightarrow A_{V_1} = -5$ V/V.

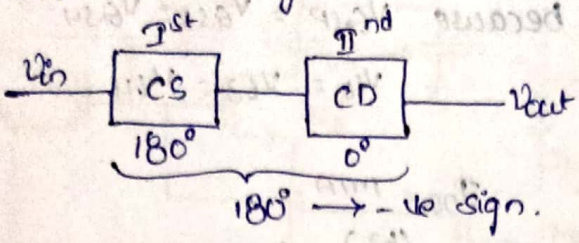
Overall voltage gain $= A_V = \frac{v_{out}}{v_{in}} = \frac{v_{out2}}{v_{in1}}$

$= \frac{v_{out2}}{v_{in2}} \cdot \frac{v_{out1}}{v_{in1}}$

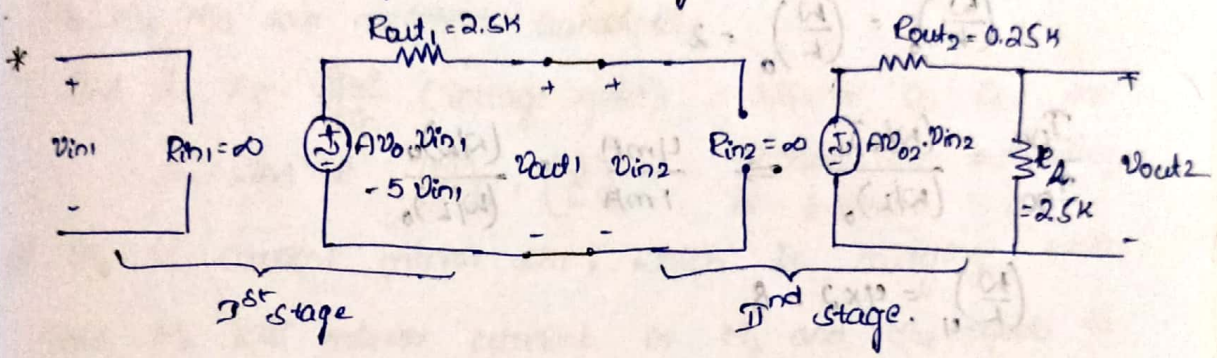
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$A_V = A_{V_1} \cdot A_{V_2} = \frac{10}{11} \cdot -5 = \frac{-50}{11} = -4.54 V/V$

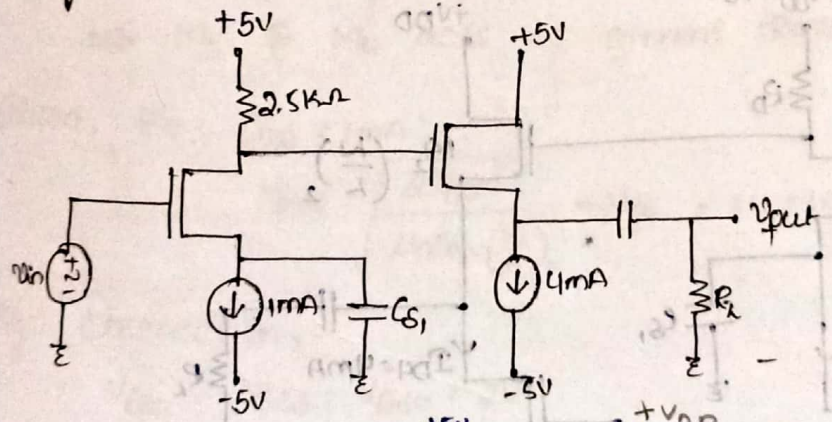
In order to avoid loading due to R_L, we have used voltage buffer i.e., CD configuration.



It is not an ideal buffer, then only we didn't get exact Vout value after putting a voltage buffer also.



Using Current Mirror.



given

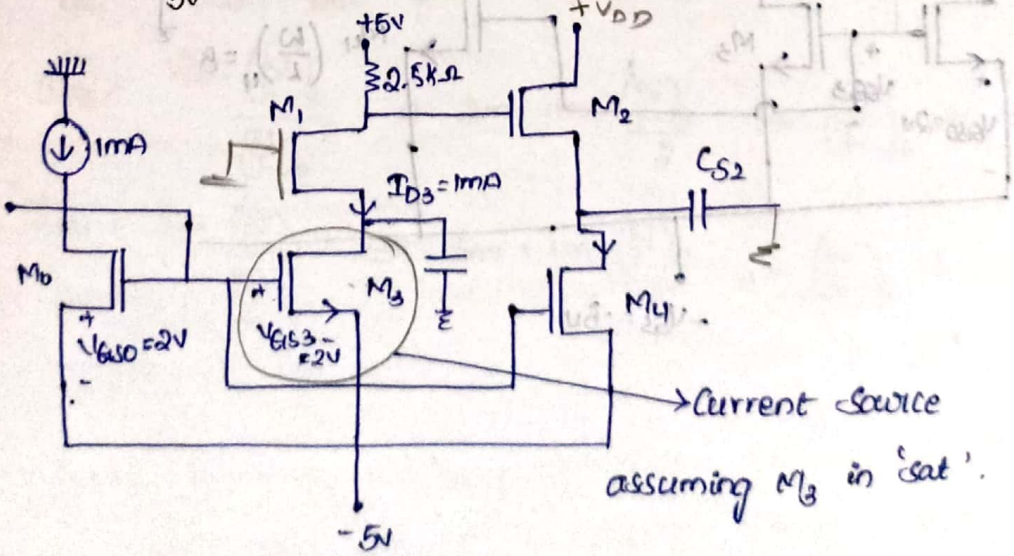
$\mu_n C_{ox} = 1 mA/V^2$

$\left(\frac{W}{L}\right)_n = 2$

$V_{tn} = 1V$

$\lambda = 0$

Sol:-



Let $\left(\frac{W}{L}\right)_0 = 2$, $V_{GS0} = 2V$

M_0 & M_3 are matched transistors,

$\mu_n C_{ox}$, V_{tn} are same.

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In sat,

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_{tn})^2$$

$$\frac{I_{D3}}{I_{D0}} = \frac{(W/L)_3}{(W/L)_0} \quad \Big| \quad \text{because } V_{GSP} = V_{GS3} = V_{GS4}$$

$$V_{t0} = V_{t3} = V_{t4}$$

$$I_{D3} = I_{D0}\cdot\frac{(W/L)_3}{(W/L)_0}$$

$I_{D0} = 1mA$

$\left(\frac{W}{L}\right)_0 = 2$

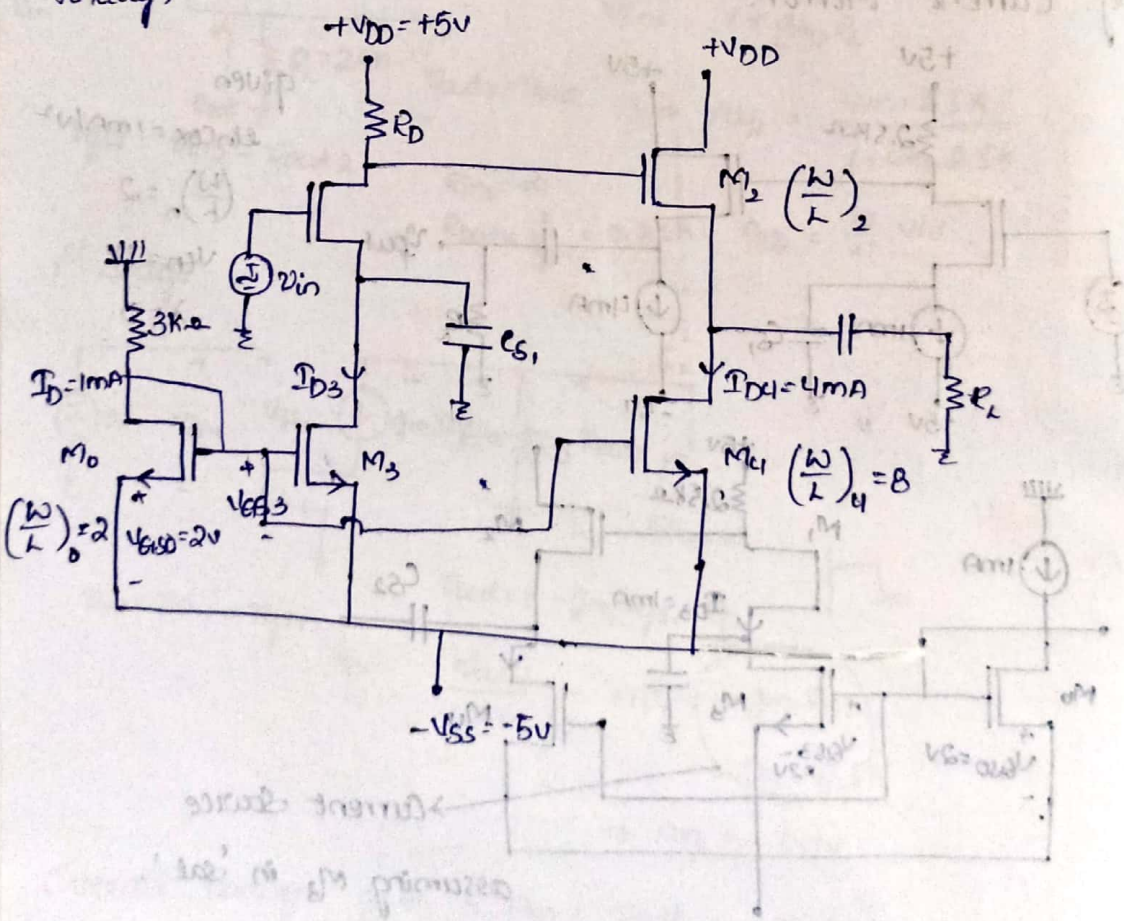
for having $I_{D3} = 1mA$

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_0 = 2$$

$$\frac{I_{D4}}{I_{D0}} = \frac{(W/L)_4}{(W/L)_0} \Rightarrow \frac{4mA}{1mA} = \frac{(W/L)_4}{(W/L)_0}$$

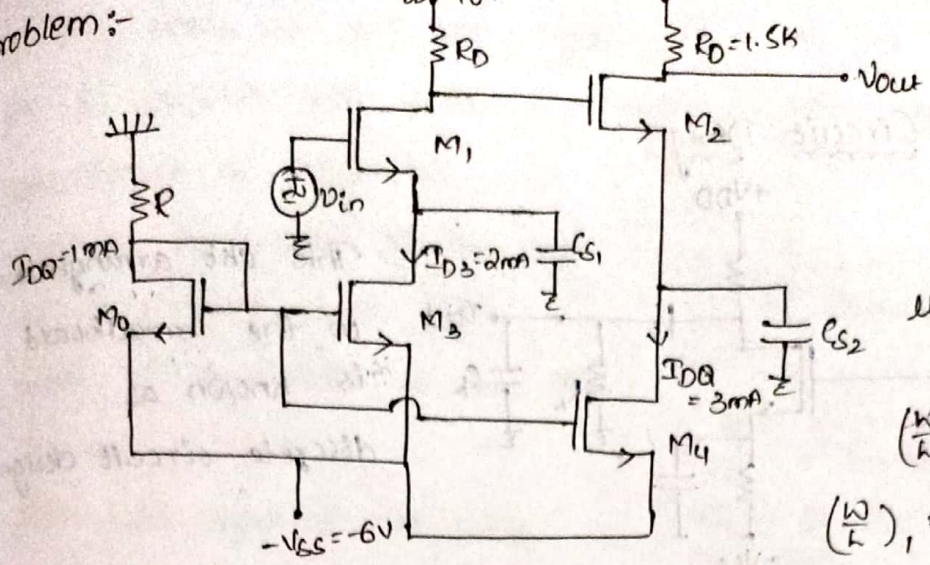
$$\left(\frac{W}{L}\right)_4 = 4\times 2 = 8$$

finally,



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problem :-



given,

$\mu_n C_{ox} = 1mA/V^2$

$\gamma_n = 1$ for all

$\left(\frac{W}{L}\right)_0 = 2$

$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$

M_0, M_3, M_4 are matched transistors.

find i, $A_v = \frac{V_{out}}{V_{in}}$ (voltage gain) ; assume C_{S1}, C_{S2} are

ii, find 'R'; $\left(\frac{W}{L}\right)_3$, $\left(\frac{W}{L}\right)_4$ shorted for our freq of interest.

M_0 is current mirror ckt, which is carrying 1mA.

This M_0 will mirror current in M_3 and M_4 equals to 2mA, 3mA respectively.

$\Rightarrow$ M_3 & M_4 acts as current sources.

Given, M_0 : $I_{DO} = 1mA$

$$V_{GSO} = \sqrt{\frac{2I_{DO}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_0}} + V_{to} = 1V + 1V = 2V$$

By observation,

$$V_{GSO} = V_{GS3} = V_{GS4} = 2V$$

$$I_{D3} = \frac{I_{DO}\cdot\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_0} \Rightarrow 2m = 1mA\cdot\frac{\left(\frac{W}{L}\right)_3}{2} \Rightarrow \left(\frac{W}{L}\right)_3 = 4$$

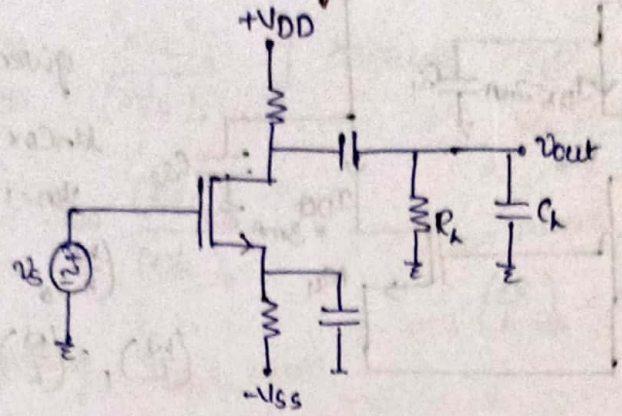
$$I_{D4} = I_{DO}\cdot\frac{\left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_0} \Rightarrow 3m = 1m\cdot\frac{\left(\frac{W}{L}\right)_4}{2} \Rightarrow \left(\frac{W}{L}\right)_4 = 6$$

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11:30

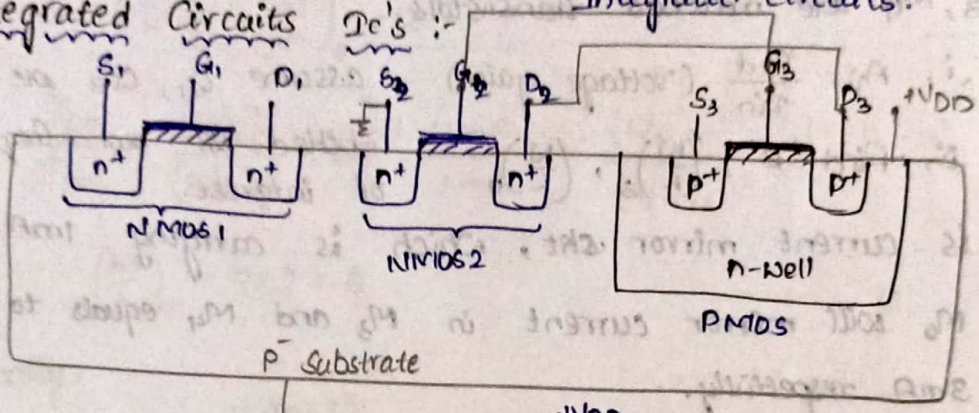
Discrete Circuit Design :-

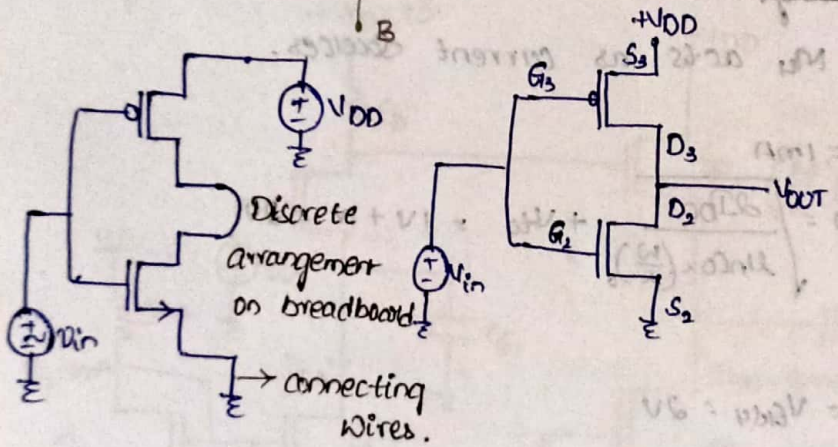
Eg:



This ckt arrangement on the breadboard is known as discrete circuit design.

Integrated Circuits Ic's :-





In an IC, all MOSfets are on single substrate i.e., integrated circuit

* In an amplifier design, we have been given Bandwith f_L & f_H and also gain of the Amplifier.

⟹ this means the amplifier has to amplify signals from f_L to f_H with a gain specified by the designer.

Eg:- A student is designing a video amplifier i.e, B.W of video amplifier $f_L = 0$ Hz & f_H = few Mega Hzts.

This means the given video amplifier has to amplify the signals near to 'dc'. It requires very huge bypass capa. i.e

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at freq. nearer to dc, these bypass caps has to be shifted. This is possible only when the value of the bypass capacitance is very low.

→ Therefore the main disadvantage is fabricating such high value of capacitors on an IC is not possible.

Even 1 μF capacitor also takes very huge area on IC.

$$f_L = \frac{1}{2\pi R_{across,C_S} C_S}$$

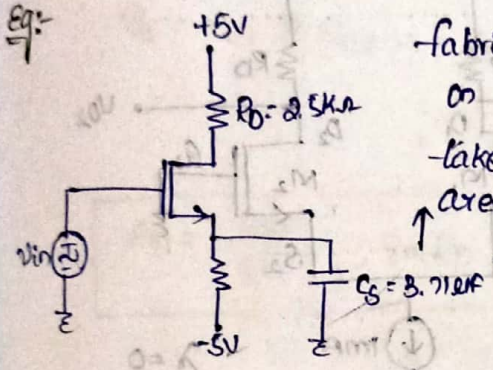
↓ 0Hz

$$C_S = \frac{1}{2\pi R_{across,C_S} \cdot f_L}$$

↓ has to be very high.

Then what is the alternate to design the below amplifier on an IC?

Eg:-

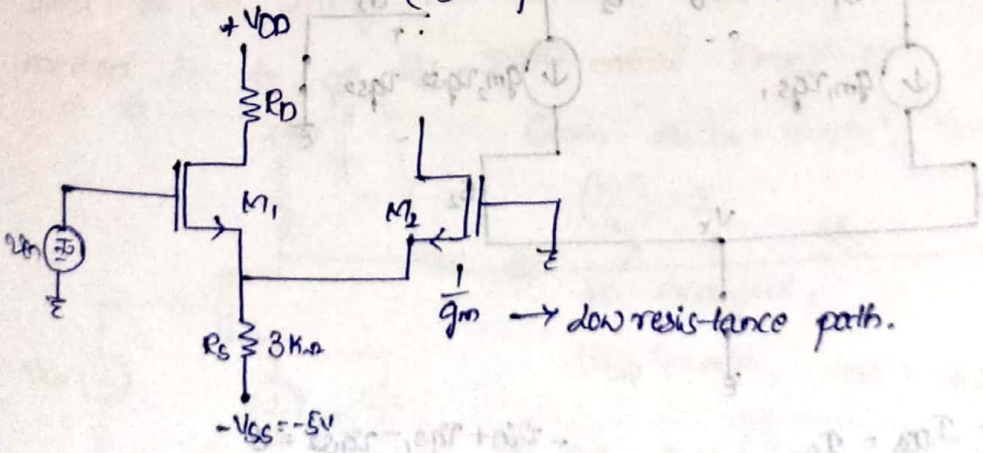


fabricating this cap on an IC will take very huge area.

⇒ then what is the alternate design the above amplifier on an IC?

Sol:- The purpose of bypass capacitor is to provide low resistance path i.e., all of the ac current will flow through 'Cs' compared to 'Rs'.

(R_S replaces with I_D = 1mA)



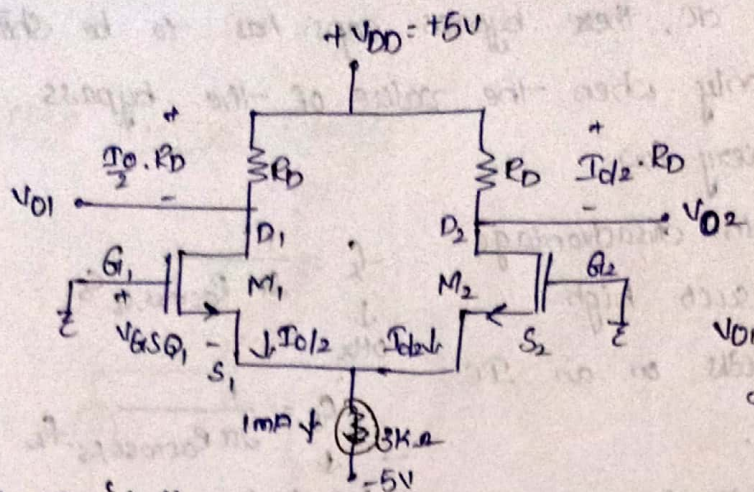
$\frac{1}{g_m}$ → low resistance path.

M_1 & M_2 both are identical means,

$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$, $\mu_n C_{ox}$, V_{th} are same.

By observation, $V_{GSQ_1} = V_{GSQ_2}$

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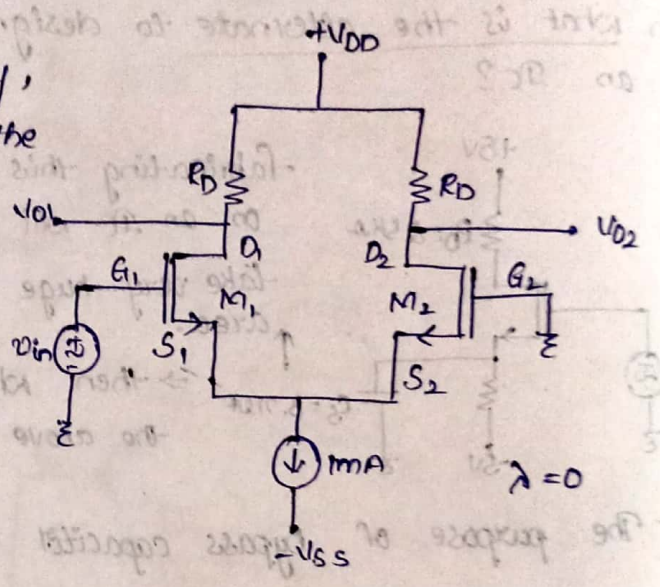
V_{O1} & V_{O2} having same potential.

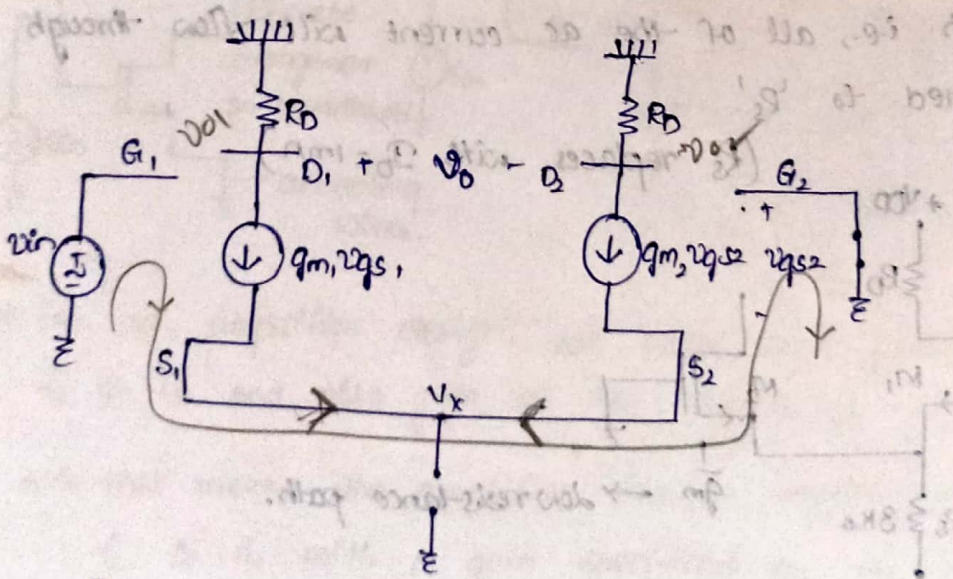
⇒ 1 mA 'tail current' gets equally divided among M_1 & M_2

→ for having symmetry, we connect R_D at the drain of 'M_2' i.e.,

$V_{DQ1} = V_{DD} - \frac{I_D}{2} R_D$

$V_{DQ2} = V_{DD} - \frac{I_D}{2} R_D$





$I_{DQ1} = I_{DQ2} = \frac{I_D}{2}$

$g_{m1} = g_{m2}$

$-v_{in} + v_{gs1} - v_{gs2} = 0$

$v_{in} = v_{gs1} - v_{gs2}$ → ①

Apply nodal @ V_x ⇒ $g_{m1} v_{gs1} = -g_{m2} v_{gs2}$

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$\Rightarrow v_{gs1} = -v_{gs2}$ $\left[\because g_{m1} = g_{m2}\right.$

$v_{gs1} + v_{gs2} = 0 \longrightarrow (2)$

$v_{gs1} + v_{gs2} = 0$

$v_{gs1} - v_{gs2} = 0$

$2v_{gs1} = 0.$

from (1) & (2)

$2v_{gs1} = v_{in} \Rightarrow v_{gs1} = \frac{v_{in}}{2}, \quad v_{gs2} = -\frac{v_{in}}{2}$

$v_{o1} = -g_m v_{gs1} R_D$

$v_{o1} = -g_{m1} \cdot \frac{v_{in}}{2} \cdot R_D$

$\left[\because g_{m1} = g_{m2} = g_m\right]$

$\Rightarrow v_{o1} = -g_m R_D \cdot \frac{v_{in}}{2}$

$v_{o2} = -g_{m2} v_{gs2} R_D$

$v_{o2} = -g_m \left(-\frac{v_{in}}{2}\right) R_D$

$v_{o2} = +g_m R_D \frac{v_{in}}{2}$

$v_o = v_{o1} + v_{o2} = -g_m R_D \frac{v_{in}}{2} - g_m R_D \frac{v_{in}}{2}$

$= -g_m R_D v_{in}$

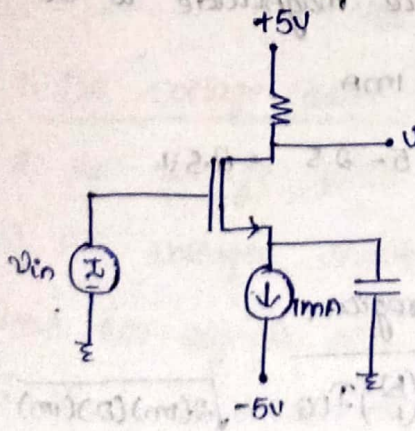
$$A_D = \frac{v_{out}}{v_{in}} = -g_m R_D$$

without using bypass caps we got the small signal voltage gain.

3/3/22

Summary :-

1. Fabricating capacitors of microfarad range will take huge area on an Integrated Circuits, that why the alternate method is to go for Differential Amplifier.



Given $\mu_n C_{ox} = 1mA/V^2$, $V_{th} = 1V$,

$\left(\frac{W}{L}\right)_1 = 2$

Sol:-

DC Analysis,

$I_{DQ} = 1mA, \quad V_{DQ} > V_{GQ}$

In sat, $g_m = \sqrt{2 \mu_n C_{ox} \left(\frac{W}{L}\right) I_{DQ}}$

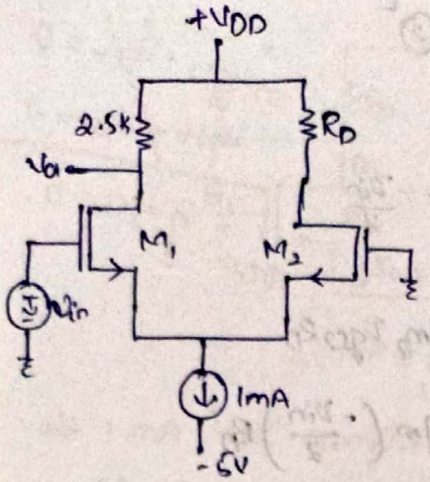
$g_m = \sqrt{2(1m)(2)(1m)} = 2mA/V$

$g_m = 2mA/V.$

By replacing C_s with mosfet.

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⇒ Differential amplifiers:



DC Analysis.

$v_{in} \rightarrow$ SC, $I_D = 1mA$

M_1, M_2 are identical

means having $\mu_n, \left(\frac{W}{L}\right), \mu_n C_{ox}$ will same

$V_{D1} = V_{DD} - \frac{I_D}{2} \cdot R_D$

$= 5 - \frac{1}{2}(2.5K) = 3.75V$

$V_{D1} = V_{D2} = 3.75V$

Both drains are having same dc voltage.

⇒ Each mosfet will carry 0.5 mA current.

$I_{DQ1} = I_{DQ2} = \frac{I_D}{2} = 0.5mA.$

$V_{DQ1} = V_{DQ2} = 3.5V$

$V_{GQ1} = V_{GQ2} = 0V$

$V_{DQ} > V_{GQ} \Rightarrow$ Saturation Region.

g_m of each mosfet:

$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) I_{DQ}} = \sqrt{2(1m)(2)\cdot\frac{1}{2}m}$

$g_m = 1.414\ mA/V.$

Small signal voltage gain,

$A_v = \frac{v_{out}}{v_{in}} = -g_m R_D = -1.414 \times 2.5K$

$\boxed{A_v = -3.535\ V/V}$

If we take the tail current source magnitude to be

$2I_D = 2mA \Rightarrow I_{DQ1} = I_{DQ2} = \frac{I_D}{2} = 1mA$

$V_{DQ1} = V_{DD} - \frac{I_D}{2} R_D = 5 - 2.5 = 2.5V$

$V_{DQ2} = 2.5V$

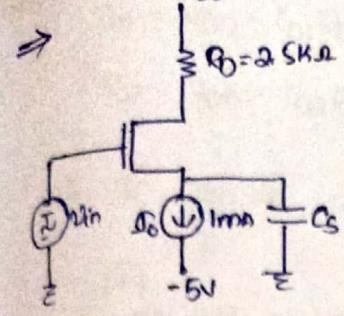
$V_{DQ} > V_{GQ} \Rightarrow$ saturation region.

'g_m' of each mosfet, $g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) I_{DQ}} = \sqrt{2(1m)(2)(1m)}$

$g_m = 2\ mA/V$

$A_v = -g_m R_D = -2m(2.5K) \Rightarrow \boxed{A_v = -5V/V}$

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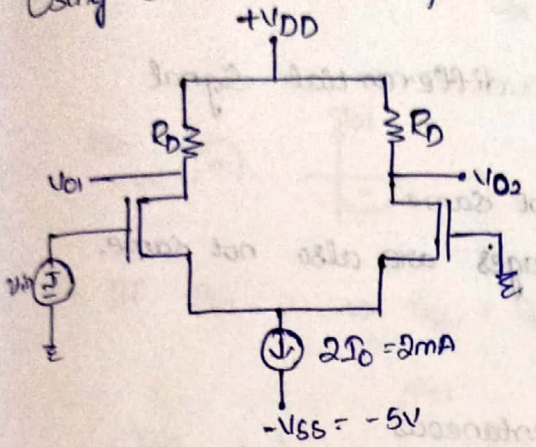
$\lambda = 0$, $\frac{v_{out}}{v_{in}} = -5\,V/V$

total power delivered, $= V_{DD} I_D + (-V_{SS})(-I_D)$

$= 5V(1m) + (-5V)(-1m)$

$= 10mW.$

Using differential amplifier: $\frac{v_{out}}{v_{in}} = -5V/V$



power dissipation due to V_{DD} and V_{SS} for same gain as in an CS amplifier.

$\Rightarrow V_{DD} \cdot 2I_D + V_{SS}(2I_D)$

$= 5(2m) + 5(2m)$

$= 20\,mW.$

Disadvantages :- For implementing same gain using differential amplifier we have to burn twice the power compared to CS Amplifier.

Advantage :- The main advantage is we don't need any bypass capacitor which will occupy huge area on IC. Swings, noises will be eliminated.

Differential Amplifiers :- The main ~~action~~ purpose is to simplify differential signal.

Differential signal means:

$$V_{in1} = V_{DC} + V_{in} \sin \omega t$$

$$V_{in2} = V_{DC} - V_{in} \sin \omega t$$

1. DC voltage same in V_{in1}, V_{in2}
2. AC voltage peak to peak has be same.
3. AC voltages should be 180° (out of phase)

These two signals are differential signals

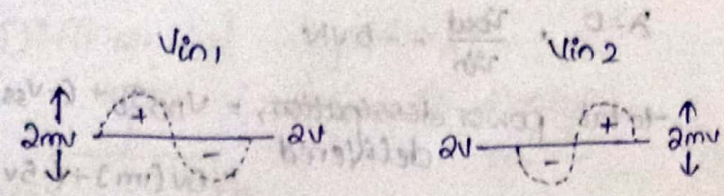
i, $V_{in1} = 2V + \sin \omega t\, mV$

$V_{in2} = 2V - \sin \omega t\, mV$

- DC Same
- ac P.P same
- 180° out of phase

} So differential signals.

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Same dc voltage = 2V

Same Peak to Peak ac = 2mV

V_{in1} & V_{in2} are 180° out of phase.

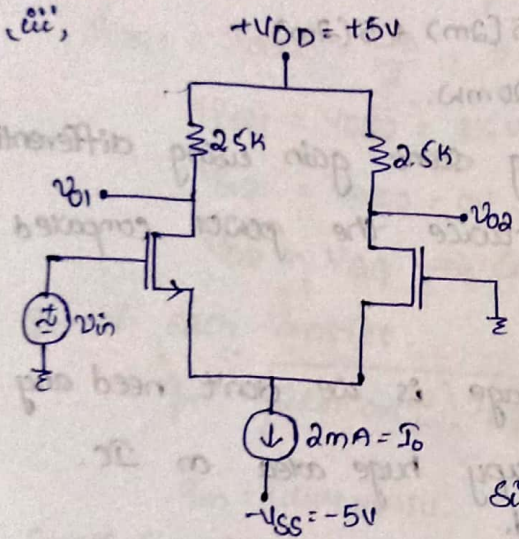
(ii) $V_{in1} = 2V + \sin\omega t\ mV$

$V_{in2} = 2V - 2\sin\omega t\ mV$ } ⇒ Not differential signal

Reason: (i) DC voltages are not same

(ii) Peak to Peak voltages are also not same.

(iii)



Instantaneous

$v_{o1} = dc + ac$

$V_{DD} - \frac{I_0}{2} R_D$ $\quad -g_m R_D \frac{v_{in}}{2}$

$5V - (1m \times 2.5K)$ $\quad -2m \times 2.5K \cdot \frac{v_{in}}{2}$

$= 2.5V$

$v_{o1} = 2.5V - 2.5\ v_{in} \rightarrow (1)$

Similarly

$v_{o2} = 2.5V + 2.5\ v_{in} \rightarrow (2)$

g_m of each Mosfet:

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{DQ}}$$

$$= \sqrt{2 \times 1m \times 2 \times 1m} = 2mA/V$$

⇒ from (1) & (2)

⇒ Both v_{o1} & v_{o2} are differential signals.

v_{o1} :



v_{o2} :



Observation

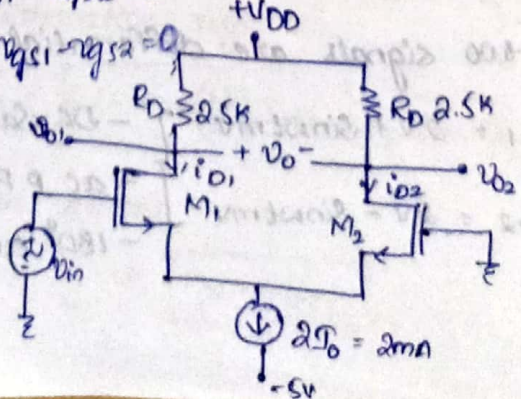
$-V_{in} + V_{gs1} - V_{gs2} = 0$

(i) If $v_{in} = 0 \Rightarrow V_{GS1} = V_{GS2}$ $\quad V_{gs1} - V_{gs2} = 0$

$\Rightarrow i_{D1} = i_{D2} \Rightarrow (1)$

$i_{D1} + i_{D2} = 2I_0$

from (1) $i_{D1} = i_{D2} = I_0$



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$v_{O1} = V_{DD} - i_{D1}R_D = 2.5V$

$v_{O2} = V_{DD} - i_{D2}R_D = 2.5V$

$-v_{in} + v_{GS1} - v_{GS2} = 0$

$\boxed{v_{in} = v_{GS1} - v_{GS2}}$

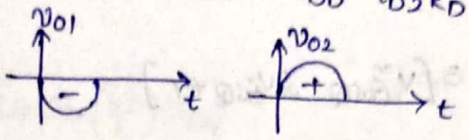
(ii) If $v_{in} > 0 \Rightarrow v_{GS1} > v_{GS2}$

$\Rightarrow i_{D1} > i_{D2}$ } $i_{D1} + i_{D2} = 2I_0$ $(i_{D1}R_D > i_{D2}R_D$

$\Rightarrow v_{O1} = V_{DD} - i_{D1}R_D$

$\Rightarrow v_{O2} = V_{DD} - i_{D2}R_D$ } $v_{O1} < v_{O2}$

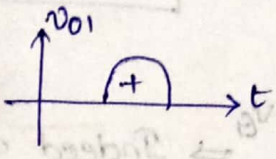
v_{in} +ve (+) $\Rightarrow$ +ve peak

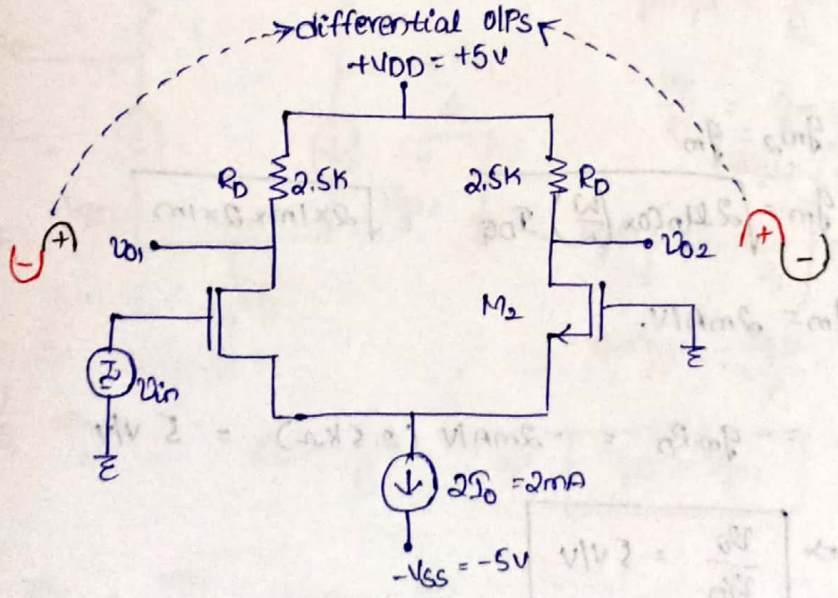


(iii) If $v_{in} < 0 \Rightarrow v_{GS1} < v_{GS2} \Rightarrow i_{D1} < i_{D2} \Rightarrow i_{D1}.R_D < i_{D2}.R_D$

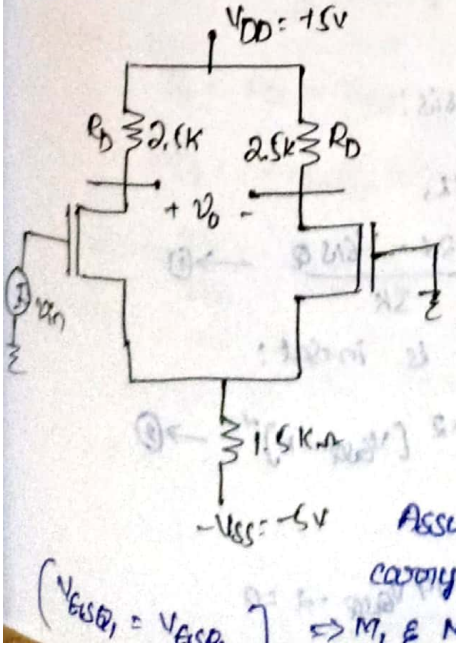
$\Rightarrow v_{O1} > v_{O2}$

v_{in} -ve (-)





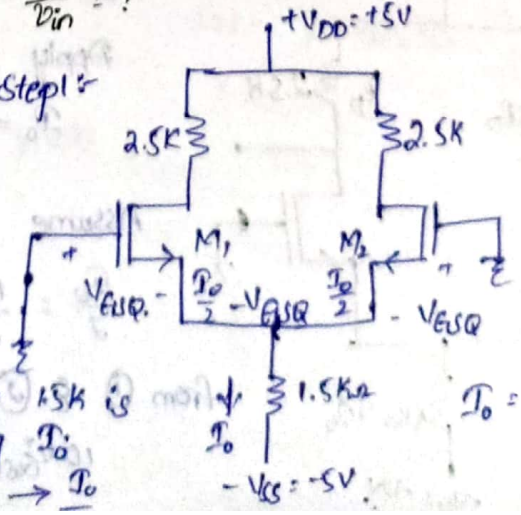
7/3/22



Given $\mu_n C_{ox} = 1mA/V^2$, $V_{tn} = 1V$, $\frac{W}{L} = 2$, $\lambda = 0$

$\frac{v_o}{v_{in}} = ?$

Step1 :-



Assume 1.5K is carrying I_0

$I_0 = \frac{-V_{GSQ} - (-V_{SS})}{1.5K}$

$(V_{GSQ1} = V_{GSQ2}$] $\Rightarrow M_1$ & $M_2 \rightarrow I_0$

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$$\Rightarrow I_D = \frac{5 - V_{GSQ}}{1.5K} \rightarrow (1)$$

Assume M_1 & M_2 $\Rightarrow$ Sat

$$\frac{I_D}{2} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{GSQ} - V_{tn})^2 \rightarrow (2)$$

from (1) & (2)

$$\frac{5 - V_{GSQ}}{1.5K} = 1m \times 2 [V_{GSQ} - 1]^2$$

$$5 - V_{GSQ} = 3[V_{GSQ}^2 - 2V_{GSQ} + 1]$$

$$3V_{GSQ}^2 - 5V_{GSQ} - 2 = 0$$

$$V_{GSQ} = 2V \Rightarrow \boxed{I_D = 2mA}$$

$V_{DQ1} = V_{DQ2} = 2.5V$

$V_{GQ1} = V_{GQ2} = 0V$

$V_D > V_G \Rightarrow$ Indeed sat.

In sat:

$g_{m1} = g_{m2} = g_m$

$$g_m = \sqrt{2 \mu_n C_{ox} \left(\frac{W}{L}\right) I_{DQ}} = \sqrt{2 \times 1m \times 2 \times 1m}$$

AC analysis

Step 2:-

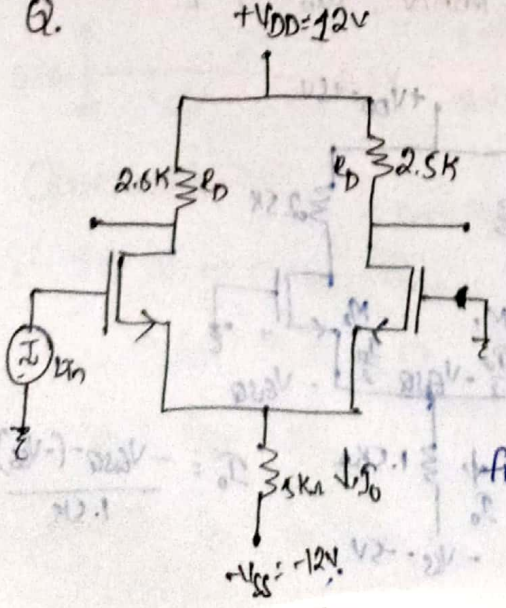
Now,

$g_m = 2mA/V.$

$$\frac{v_o}{v_{in}} = -g_m R_D = -2mA/V\,(2.5K\Omega) = 5\ V/V$$

$$\Rightarrow \boxed{\frac{v_o}{v_{in}} = 5\ V/V}$$

Q.



DC Analysis:

Apply KVL,

$$I_D = \frac{12V - V_{GSQ}}{5K} \rightarrow (1)$$

Assume it is in sat:

$$\frac{I_D}{2} = \frac{1m \times 2}{2}[V_{GSQ} - 1]^2 \rightarrow (2)$$

from (1) & (2)

$$10V_{GSQ}^2 - 19V_{GSQ} - 2 = 0$$

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$V_{GSQ} = 2V \quad \Rightarrow \quad I_D = 2mA.$

M_1 & M_2

$I_{DQ1} = I_{DQ2} = \frac{I_D}{2} = 1mA$

$V_{DQ1} = V_{DD} - \frac{I_D}{2} R_D = V_{DQ2} = 9.5V$

$V_{BQ1} = V_{GQ2} = 0V$

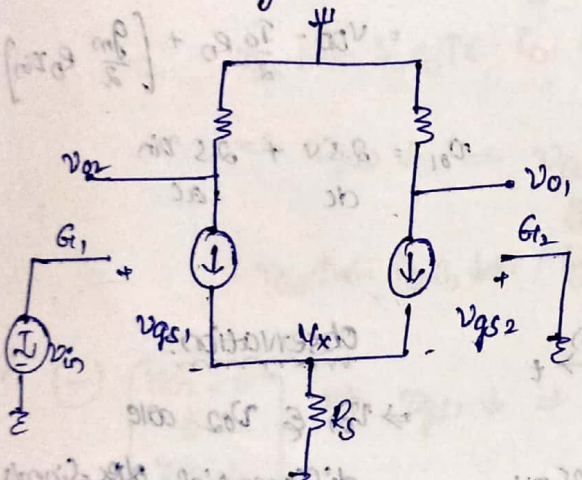
$\Rightarrow V_D > V_G \Rightarrow$ Indeed Sat.

In Sat:

$g_m = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right) I_{DQ}}$ $\qquad g_{m1} = g_{m2} = g_m$

$\boxed{g_m = 2mA/V}$

Now, AC Analysis:



Applij. Nodal at V_x

$-g_m v_{gs1} + \frac{V_x}{R_S} - g_m v_{gs2} = 0$

$\frac{V_x}{R_S} = g_m [v_{gs1} + v_{gs2}]$

$-v_{gs2}\left(g_m + \frac{1}{R_S}\right)$

$-v_{gs2}\left[g_m + \frac{1}{R_S}\right] = g_m v_{gs1}$

$-g_m v_{gs2} - \frac{v_{gs2}}{R_S} = g_m [v_{gs1}]$

$\frac{1}{R_S} \Rightarrow \infty \quad \because g_m >> \frac{1}{R_S} \quad \Rightarrow \boxed{v_{gs2} = -v_{gs1}} \rightarrow (2)$

$\Rightarrow v_{gs1} = \frac{v_{in}}{2}, \quad v_{gs2} = -\frac{v_{in}}{2}$

$v_o = v_{o1} - v_{o2}$

$v_o = -g_m R_D \cdot v_{in}$

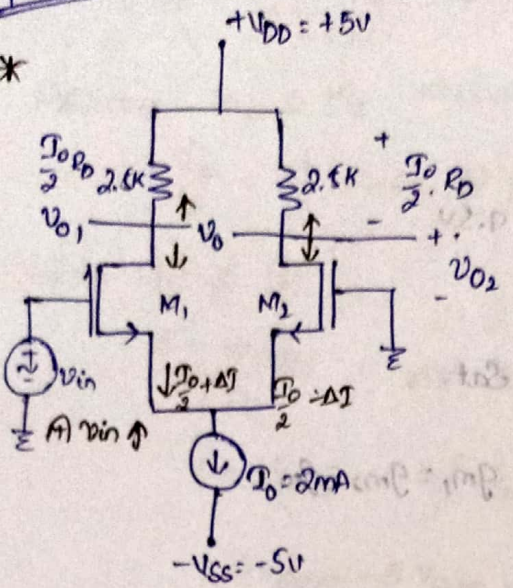
$\frac{v_o}{v_{in}} = -g_m R_D = 5 V/V$

$v_{o1} = -g_m v_{gs1} R_D$

$v_{o2} = -g_m v_{gs2} R_D$

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8/3/22



$\mu_n C_{ox} = 1 mA/V^2$

$V_{tn} = 1V \quad \frac{W}{L} = 2 \quad \lambda = 0$

By observation:

$I_{DQ1} = I_{DQ2} = \frac{I_D}{2} = 1mA$

$V_{DQ1} = V_{DQ2} = V_{DD} - \frac{I_D}{2} \cdot R_D = 2.5V$

M_1 & M_2 are identical Sat.

$\Rightarrow g_{m1} = g_{m2} = g_m = 2mA/V.$

$v_{o1} = DC + AC$

$= V_{DD} - \frac{I_D}{2} R_D + \left[-\frac{g_m}{2} R_D v_{in} \right]$

$v_{o1} = 2.5V + [-2.5 v_{in}]$

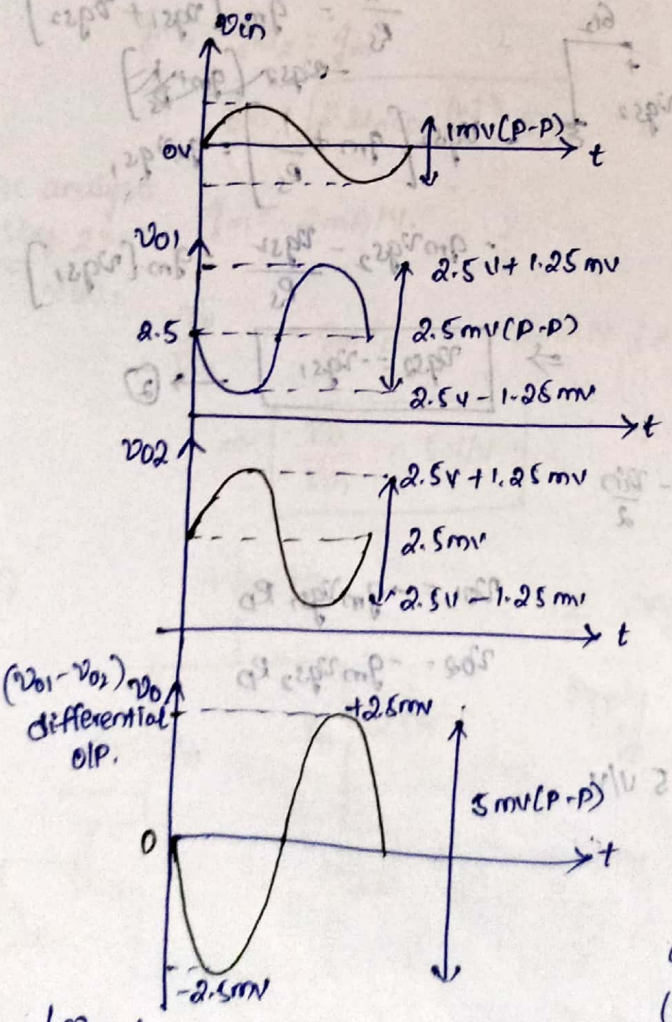
dc ac

$v_{o2} = DC + AC$

$= V_{DD} - \frac{I_D}{2} R_D + \left[\frac{g_m}{2} R_D v_{in} \right]$

$v_{o1} = 2.5V + 2.5 v_{in}$

dc ac



Observation:

$\Rightarrow v_{o1}$ & v_{o2} are differential & Signals.

$\Rightarrow v_o = v_{o1} - v_{o2}$

↓

differential o/p.

$\Rightarrow v_{o1}, v_{o2} \Rightarrow$ Single ended o

2.

* Advantage.

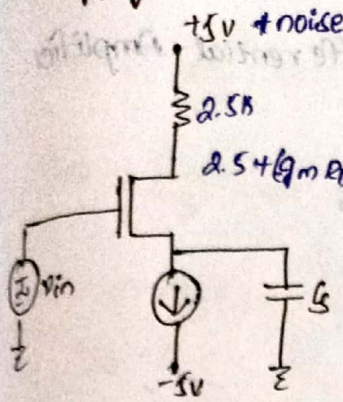
In taking differential o/p, $v_o = v_{o1} - v_{o2}$, voltage swings will be doubled compared to single ended (v_{o1} & v_{o2}) voltage swings. & CS amplifier.

$\frac{|v_{op-p}|}{|v_{in\,p-p}|} = \frac{g_m}{1m} = 5 mA/V$

$* |A_{vl}| = \frac{v_o}{v_{in}} = -g_m R_D = |-2 \times 2.5k| = 5 V/V$

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Supply Noise.



3. Advantage.

⇒ By taking differential o/p $v_o = v_{o1} - v_{o2}$ supply noises are completly removed. compared to CS

Note :- Single ended o/p's will have supply noises.

*

1. (+) $\begin{bmatrix} v_{in} > 0 \\ \text{or} \\ v_{in} \uparrow \end{bmatrix}$ $\Rightarrow v_{gs1} \uparrow$ $v_{gs2} \downarrow$ $\Rightarrow v_{GS1} \uparrow$ $(V_{GS@} + v_{gs1})$

$v_{gs1} = \frac{v_{in}}{2}$, $v_{gs2} = -\frac{v_{in}}{2}$

$i_d = g_m v_{gs}$

$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{GS} - V_{tn})^2$

$\Downarrow$

$v_{o1} \downarrow \Leftarrow i_{D1} R_D \uparrow \Leftarrow i_{D1} \uparrow$

$\Rightarrow v_{gs2} \downarrow \Rightarrow v_{GS2} \downarrow (V_{GS@} + v_{gs2})$

$\Downarrow$

$v_{o2} \uparrow \Leftarrow i_{D2} R_D \downarrow \Leftarrow i_{D2} \downarrow$

2. (−) $\begin{bmatrix} v_{in} < 0 \\ \text{or} \\ v_{in} \downarrow \end{bmatrix}$ $\Rightarrow v_{gs1} \downarrow \Rightarrow v_{GS1} \downarrow$

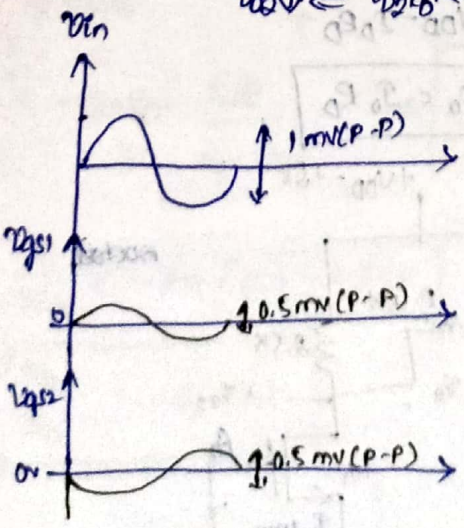
$\Downarrow$

$v_{o1} \uparrow \Leftarrow i_{D1} R_D \downarrow \Leftarrow i_{D1} \downarrow$

$\Rightarrow v_{gs2} \uparrow \Rightarrow v_{GS2} \uparrow$

$\Downarrow$

$v_{o2} \downarrow \Leftarrow i_{D2} R_D \uparrow \Leftarrow i_{D2} \uparrow$

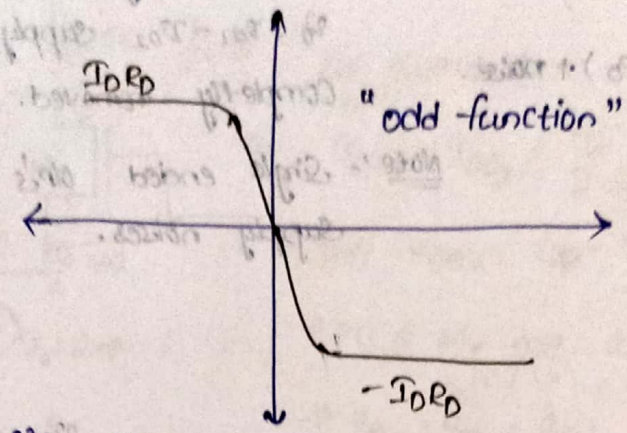


v_{gs1} & v_{gs2} are differential i/ps.

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Large Signal Operation :-

Transfer characteristics of Mosfet Differential Amplifier



$v_{in} 0 \Rightarrow v_{GS1} = v_{GS2} \Rightarrow I_D R_D$

$i_{D1} = i_{D2} \Rightarrow \boxed{v_{O1} = v_{O2}}$

$v_{in} > 0 \Rightarrow v_{GS1} > v_{GS2} \Rightarrow i_{D1} > i_{D2}$

$\Rightarrow i_{D1} R_D > i_{D2} R_D \Rightarrow \boxed{v_{O1} < v_{O2}}$

@ one value of v_{in}

$i_{D1} = I_0$ & $i_{D2} = 0$

$\Rightarrow v_{O1} = V_{DD} - I_0 R_D$ & $v_{O2} = V_{DD}$

$v_0 = v_{O1} - v_{O2} = -I_D R_D$

$v_{in} < 0 \Rightarrow v_{GS1} < v_{GS2} \Rightarrow i_{D1} < i_{D2}$

$\Downarrow$

$i_{D1} R_D < i_{D2} R_D \Rightarrow \boxed{v_{O1} > v_{O2}}$

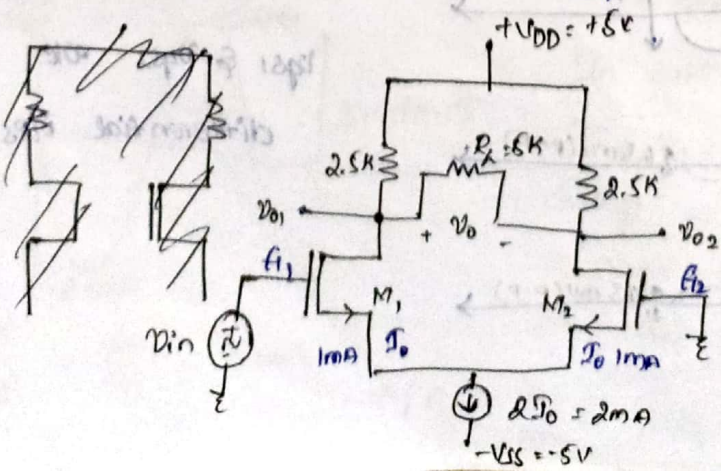
@ one value of v_{in}

$i_{D1} = 0$ & $i_{D2} = I_D$

$\Rightarrow v_{O1} = V_{DD}$ & $v_{O2} = V_{DD} - I_D R_D$

$\Rightarrow \boxed{v_0 = I_0 R_D}$

9/3/22



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$\frac{v_o}{v_{in}} = -g_m R_D$

$v_{o1} = -\frac{g_m R_D}{2} v_{in} \Rightarrow \frac{v_{o1}}{v_{in}} = -\frac{g_m R_D}{2}$

$v_{o2} = \frac{g_m R_D}{2} v_{in} \Rightarrow \frac{v_{o2}}{v_{in}} = \frac{g_m R_D}{2}$

* DC Analysis:

$v_{in} = 0$

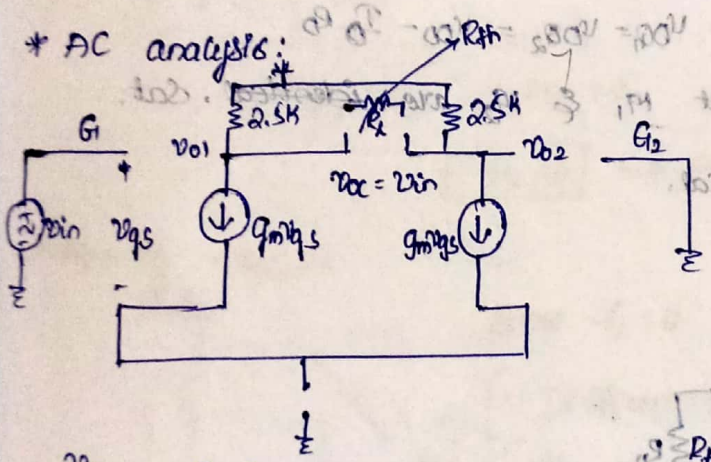
$V_{GSQ_2} = V_{GSQ_1} = V_{GSQ}$ [M_1 & M_2 are identical]

$I_{DQ_1} = I_{DQ_2} = I_D$

$V_{DQ_1} = V_{DQ_2} = 2.5V$, $V_{GSQ} = 0$

$g_{m_1} = g_{m_2} = g_m = 2\,mA/V.$

* AC analysis:



$v_{oc} = -g_m R_D \cdot v_{in}$

$R_{th} = 2R_D$

$v_o = \frac{R_L}{R_L + R_{th}} v_{in}$

$\frac{v_o}{v_{in}} = -g_m R_D \cdot \frac{R_L/2}{R_L + R_D}$

$\Rightarrow \boxed{\frac{v_o}{v_{in}} = -g_m [R_D // \frac{R_L}{2}]}$

$\Rightarrow \frac{v_o}{v_{in}} = -2m [2.5K // 2.5K]$

$\boxed{\frac{v_o}{v_{in}} = -2.5\ V/V}$

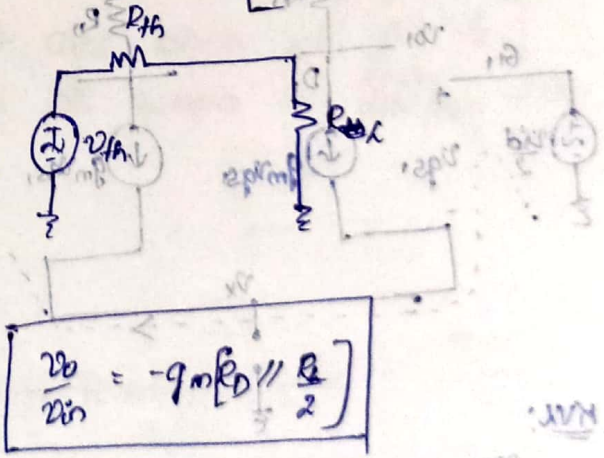
Nodal @ v_{o1} & v_{o2}

①: $\frac{v_{DQ_1} - 5}{2.5K} + \frac{v_{DQ_1} - v_{DQ_2}}{5K} + Im = 0$

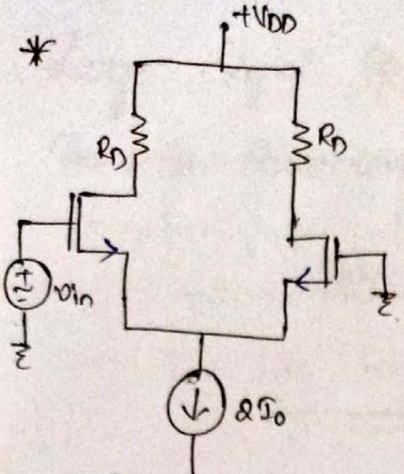
②: $\frac{v_{DQ_2} - 5}{2.5K} + \frac{v_{DQ_2} - v_{DQ_1}}{5K} + Im = 0$

solving ① & ②

$v_{DQ_1} = 2.5V$, $v_{DQ_2} = 2.5V$

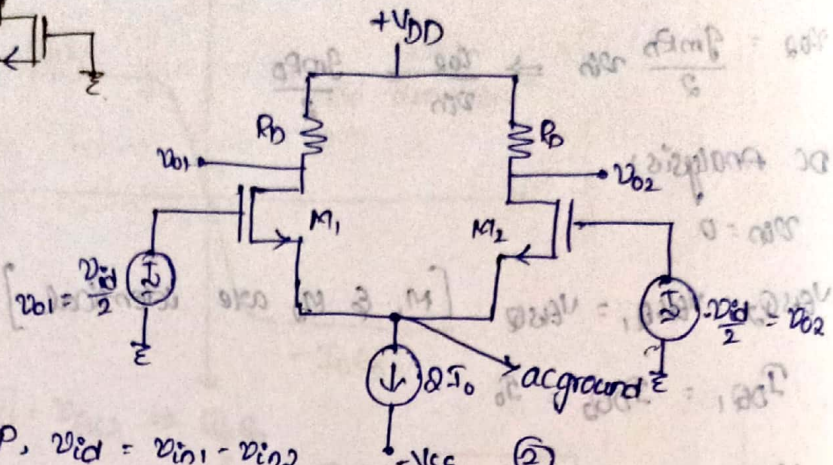


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$v_{gs1} = \frac{v_{in}}{2}$ & $v_{gs2} = -\frac{v_{in}}{2}$

Differential signals



Differential i/p, $v_{id} = v_{in1} - v_{in2}$

DC Analysis,

$v_{id} = 0$

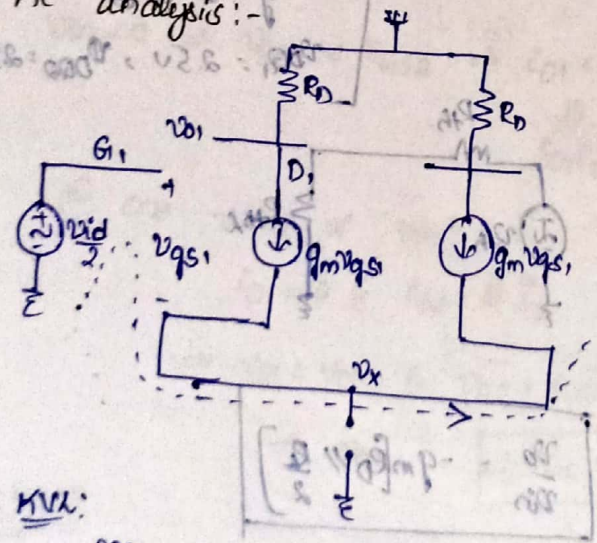
$I_{DQ1} = I_{DQ2} = I_0$ & $V_{DQ1} = V_{DQ2} = V_{DD} - I_D R_D$

R_D is taken such that M_1 & M_2 are ~~identical~~, sat.

M_1 & M_2 $\Rightarrow$ identical.

$g_{m1} = g_{m2} = g_m$.

AC analysis :-



KVL:

$-\frac{v_{id}}{2} + v_{gs1} - v_{gs2} - \frac{v_{id}}{2} = 0$

$v_{id} = v_{gs1} - v_{gs2}$ $\rightarrow$ (1)

Nodal @ v_x

$g_m v_{gs1} = -g_m v_{gs2}$

$v_{gs1} + v_{gs2} = 0$ $\rightarrow$ (2)

from (1) & (2)

$v_{gs1} = \frac{v_{id}}{2}$ & $v_{gs2} = -\frac{v_{id}}{2}$ $\rightarrow$ differential signals.

$v_{o1} = -g_m v_{gs1} R_D$

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$v_{o1} = -\frac{g_m R_D}{2} \cdot v_{id}$

Single ended diff. gain, $\frac{v_{o1}}{v_{id}} = -\frac{g_m R_D}{2}$

$v_{o2} = -g_m v_{gs2} R_D$

$= -g_m\left(-\frac{v_{id}}{2}\right) R_D$

Single ended diff. gain, $\frac{v_{o2}}{v_{id}} = \frac{g_m R_D}{2}$

$v_o = v_{o1} - v_{o2}$

$= -\frac{g_m R_D}{2} - \frac{g_m R_D}{2}$

$= -g_m R_D$

Now, $A_d = \frac{v_o}{v_{id}} = -g_m R_D$ → Differential gain.

⇒ finding v_x.

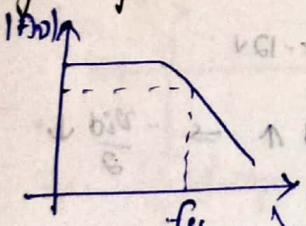
$-\frac{v_{id}}{2} + v_{gs1} + v_x = 0$

$-\left(-\frac{v_{id}}{2}\right) + v_{gs2} + v_x = 0$

$(v_{gs1} + v_{gs2}) + 2v_x = 0$ ($i \to 0$)

$\boxed{v_x = 0}$ → AC ground.

Frequency response.



Here $f_{z1} = 0$ (CS amplifier)

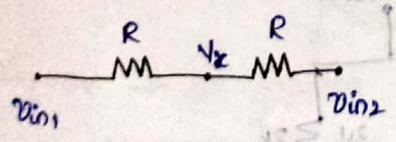
[∵ Differential Amplifier]

[No caps which will give f_z.]

→ This will behave as low pass filter.

10/3/22

⇒



$v_{in1} = 2.5V + \sin\omega t$ mv

$v_{in2} = 2.5V - \sin\omega t$ mv } differential inputs.

Nodal @ v_x

$\frac{v_x - v_{in1}}{R} + \frac{v_x - v_{in2}}{R} = 0$

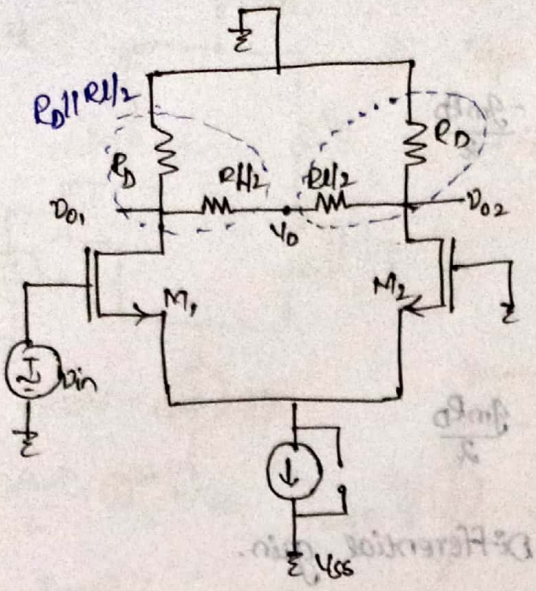
$2v_x - \underbrace{(v_{in1} + v_{in2})}_{5V} = 0$

$2v_x = 5V$

$\boxed{v_x = 2.5V}$ → DC

⇒ v_x is a ac ground.

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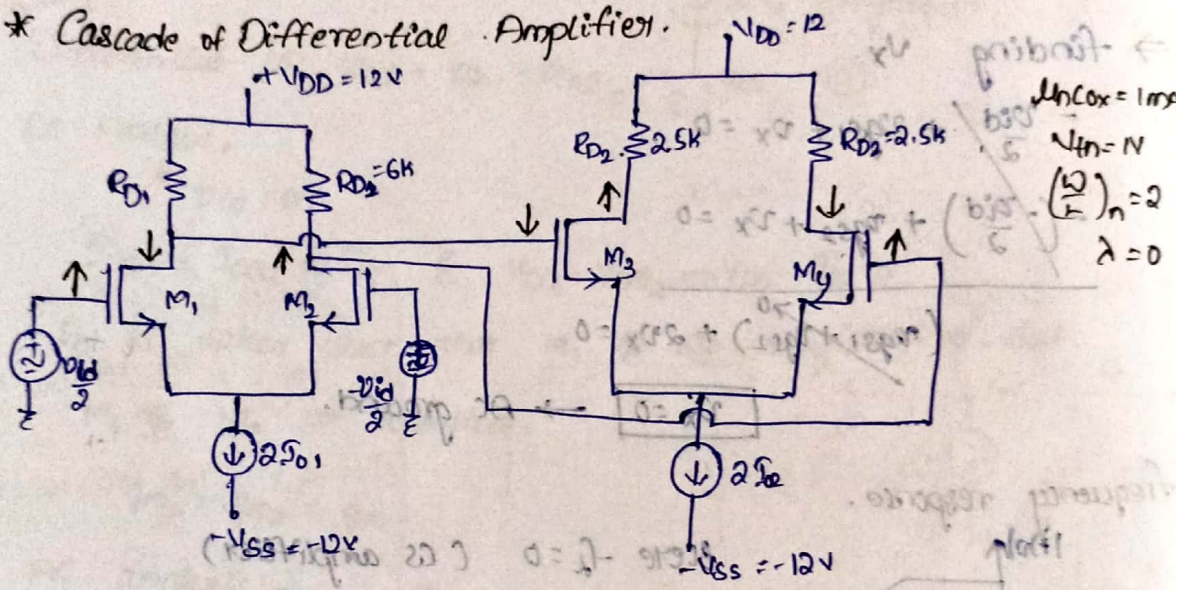
$v_o = v_{o1} - v_{o2}$

v_{o1} & v_{o2} are differential signals.

Now,

$$\frac{v_{out}}{v_{in}} = -g_m(R_D \| R_{L/2})$$

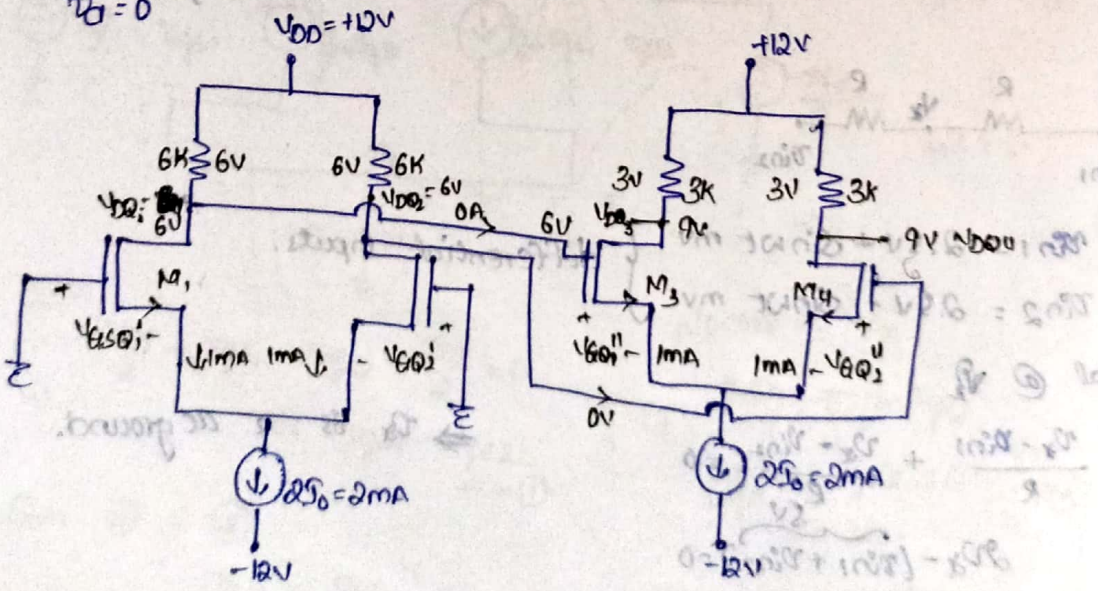
* Cascade of Differential Amplifier.



* $v_{id} = 0V$ (initially) as $v_{id} \uparrow \Rightarrow \frac{v_{id}}{2} \uparrow \Rightarrow -\frac{v_{id}}{2} \downarrow$

DC Analysis :-

$v_{id} = 0$



First stage : $M_1, M_2 \Rightarrow$ identical

Assume M_1 & $M_2 \Rightarrow$ Sat.

Second stage.

Assume $M_3, M_4 \Rightarrow$ Sat.

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$V_{GSQ1} = V_{GSQ2} = V_{GSQ}$

$= \sqrt{\frac{2I_{DQ}}{\mu_n C_{ox} \frac{W}{L}}} + V_{th}$

$= 2V$

$V_{GSQ3} = V_{GSQ4} = V_{GSQ}$

$= \sqrt{\frac{2I_{DQ}}{\mu_n C_{ox} \frac{W}{L}}} + V_{th}$

$= 2V$

$I_{DQ1} = I_{DQ2} = 1mA$

$V_{DQ1} = V_{DQ2} = V_{DD} - I_{DQ1} R_D = 6V$

$V_{GQ1} = V_{GQ2} = 0V$

$V_{DQ} > V_{GQ}$

$\Rightarrow$ Indeed saturation. (M_1, M_2)

$g_{m1} = g_{m2} = g_m'$

$= \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right) I_{DQ}}$

$g_m' = 2mA/V.$

$I_{DQ3} = I_{DQ4} = 1mA$

$V_{DQ3} = V_{DQ4} = V_{DD} - I_{D2} R_{D_2} = 9V$

$V_{GQ3} = V_{GQ4} = 6V$

$V_{DQ} > V_{GQ}$

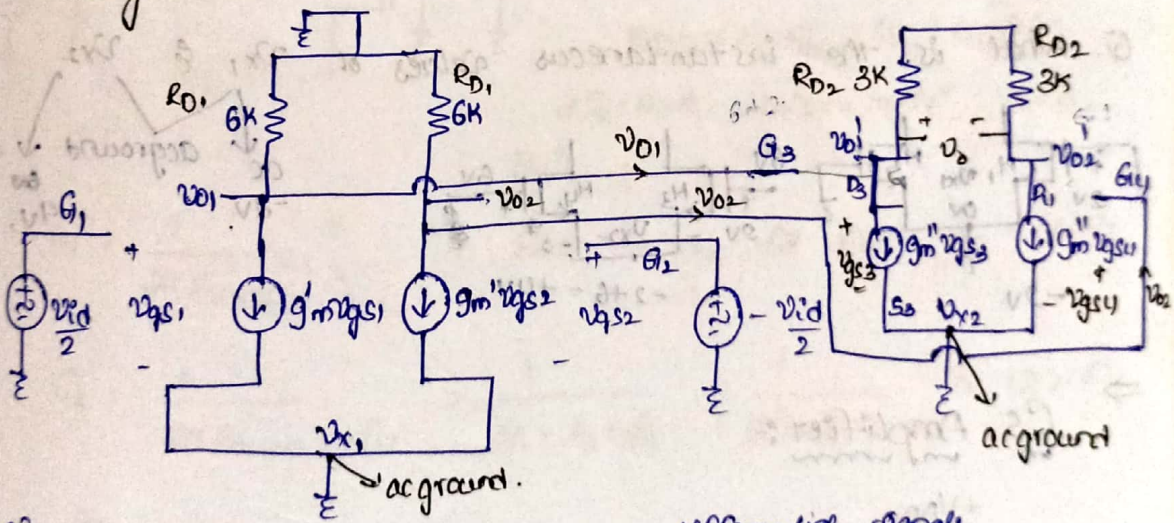
$\Rightarrow$ Indeed saturation. (M_3, M_4)

$g_{m3} = g_{m4} = g_m'$

$= \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right) I_{DQ}}$

$g_m'' = 2mA/V.$

AC Analysis:-



$v_{x1} = 0V \rightarrow$ ac ground $\therefore \frac{v_{id}}{2}, -\frac{v_{id}}{2} \Rightarrow$ differential signals.

$v_{gs1} = \frac{v_{id}}{2}, \quad v_{gs2} = -\frac{v_{id}}{2}$

$v_{o1} = -g_m' v_{gs1} R_D, \quad v_{o2} = -g_m' v_{gs2} R_D$

$v_{o1} = -\frac{g_m' R_D}{2} v_{id}$

$v_{o2} = +\frac{g_m' R_D}{2} v_{id}$

} differential signals.

Similarly v_{x2} = ac ground = 0V.

v_{o1}' & v_{o2}' are differential signals.

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$\Rightarrow \boxed{v_{gs3} = v_{o1} \text{ & } v_{gs4} = v_{o2}}$

$v_{o1}' = -g_m'' v_{gs3} R_{D2}$

$= -g_m'' R_{D2} \cdot v_{o1}$

$v_{o1}' = -g_m'' R_{D2} \cdot \frac{-g_m' R_{D1} v_{id}}{2}$

$v_{o1}' = \frac{g_m' g_m'' R_{D1} R_{D2} v_{id}}{2}$

$v_{o2}' = -g_m'' v_{gs4} R_{D2}$

$= -g_m'' R_{D2} \cdot v_{o2}$

$= -g_m'' R_{D2} \cdot \frac{+g_m R_{D1}}{2} v_{id}$

$= \frac{-g_m' g_m'' R_{D1} R_{D2} \cdot v_{id}}{2}$

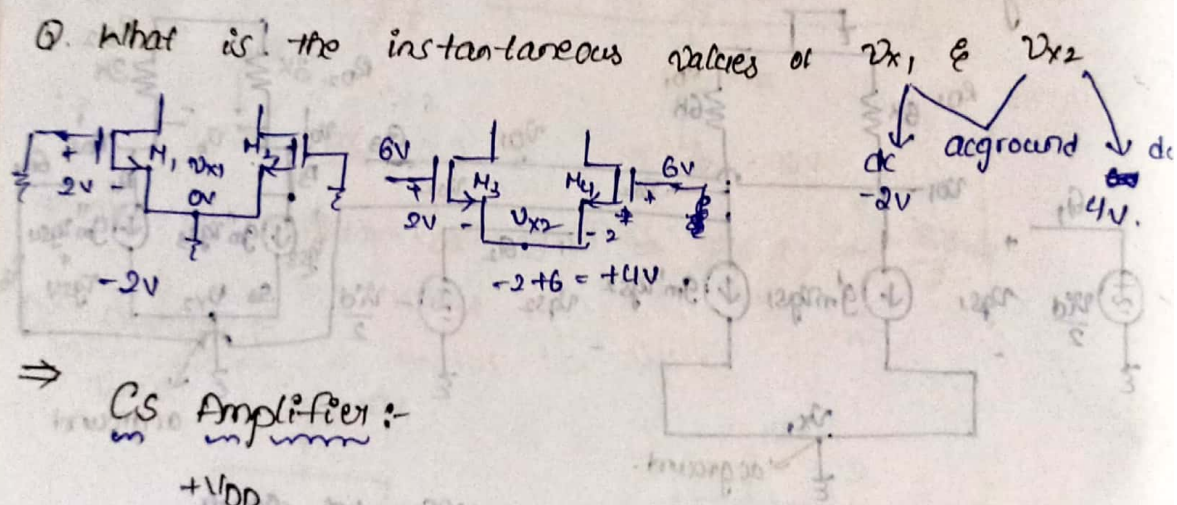
$v_o = v_{o1}' - v_{o2}' = g_m' g_m'' R_{D1} R_{D2} v_{id}$

$\frac{v_o}{v_{id}} = g_m' g_m'' R_{D1} R_{D2}$

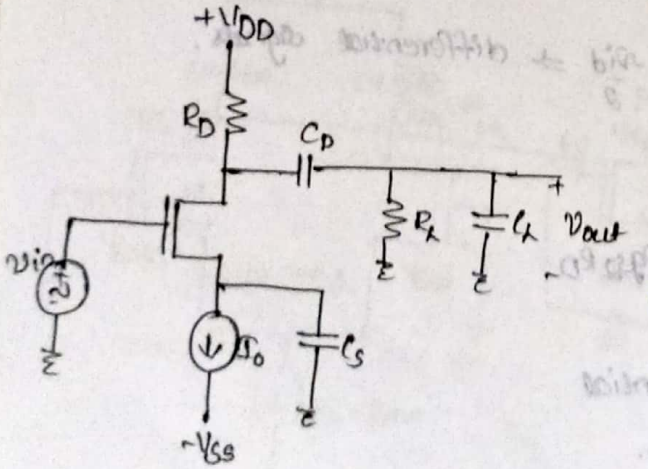
$= [g_m' R_{D1}] [g_m'' R_{D2}]$

$A_d = \frac{v_o}{v_{id}} = [2m \times 6k] [2m \times 3k] \Rightarrow \boxed{A_v = 72 V/V}$

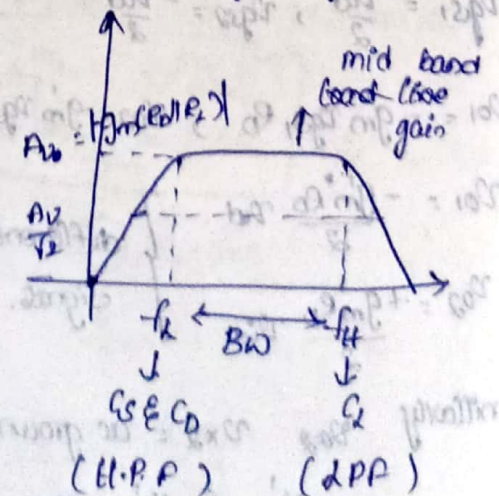
Q. What is the instantaneous values of v_{x1} & v_{x2}



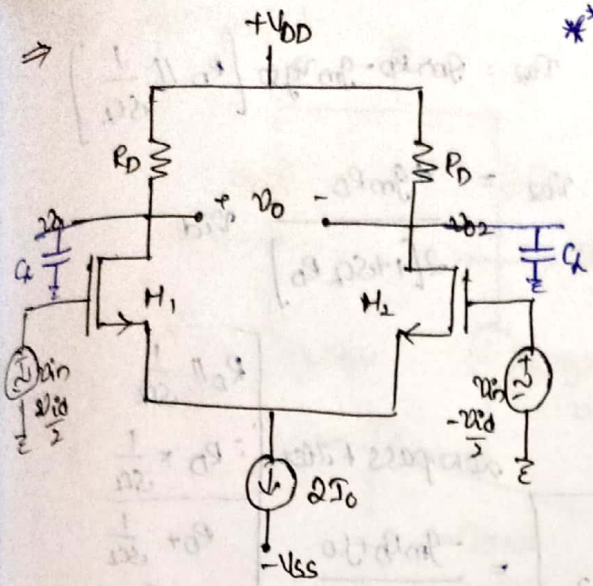
$\Rightarrow$ CS Amplifier :-



-frequency response

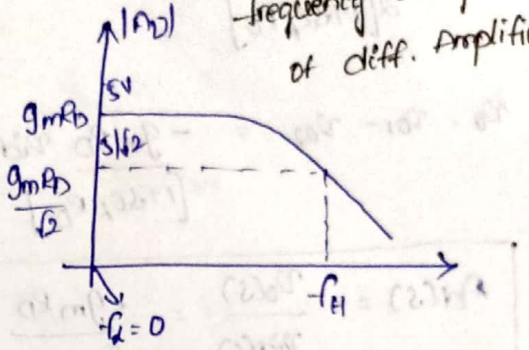


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** ∵ In diff. Amplifier, there is no Bypass, coupling caps.

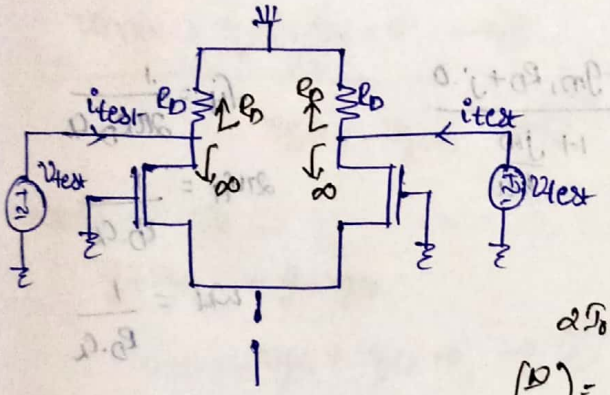
$\Rightarrow f_L = 0$



frequency response of diff. Amplifier.

f_H is bcz of C_L. $\Rightarrow f_H = \frac{1}{2\pi R_{across} C_L \cdot C_L}$

R_{across, C_L} :-



$R_{across, C_L} = R_D // \infty$

$\Rightarrow R_{across, C_L} = R_D$

$V_{DD} = +5V$, $V_{SS} = -5V$, $R_D = 2.5k$.

$2I_0 = 2mA$, $\mu_n C_{ox} = 1mA/V^2$, $V_{tn} = 2$,

$\left(\frac{W}{L}\right) = 2$ $\lambda = 0$

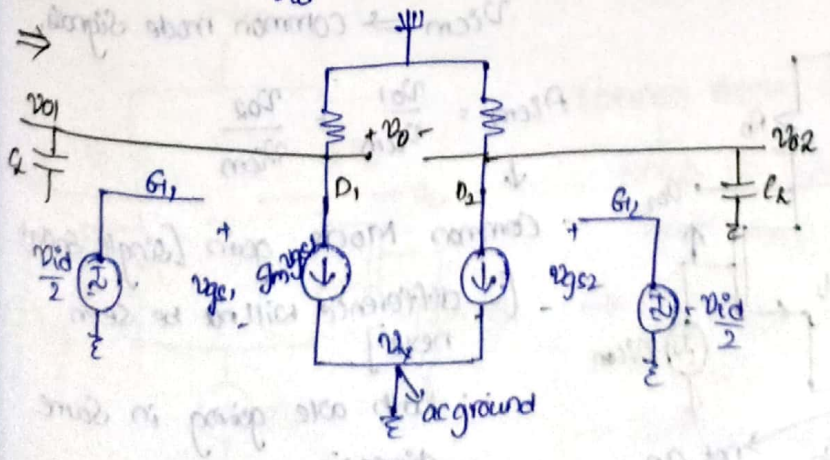
What is C_L for which $f_H = 50kHz$

$f_H = \frac{1}{2\pi R_{across, C_L} \cdot C_L}$

$C_L = \frac{1}{2\pi R_{across, C_L} \cdot f_H} = \frac{1}{2\pi \times R_D \times f_H} = \frac{1}{2\pi \times 2.5 \times 50kHz} = 127nF.$

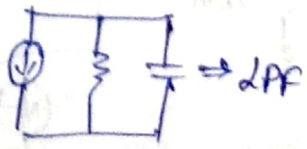
$g_{m1} = g_{m2} = g_m = 2mA/V.$

$A_{vd} = \frac{v_o}{v_{id}} = -g_m R_D = -5V/V.$



$v_{gs1} = \frac{v_{id}}{2}$

$v_{gs2} = -\frac{v_{id}}{2}$



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$v_{o1} = -g_m v_{gs1}\left[R_D \,//\, \frac{1}{sC_L}\right]$ $\quad v_{o2} = g_m R_D - g_m v_{gs2}\left[R_D \,//\, \frac{1}{sC_L}\right]$

$v_{o1} = \frac{-g_m R_D}{2[1+sC_L R_D]} v_{id}$ $\quad v_{o2} = \frac{+g_m R_D}{2[1+sC_L R_D]} v_{id}$

$v_o = v_{o1} - v_{o2} = \frac{-g_m R_D}{[1+sC_L R_D]} v_{id}$

$$A_d(s) = \frac{v_o(s)}{v_{id}(s)} = \frac{-g_m R_D}{[1+sC_L R_D]}$$

↓ differential gain as a function of frequency.

$= \frac{-g_m R_D + j.0}{1 + j\omega C_L R_D}$

low pass filter.

$R_D \,//\, \frac{1}{sC_L} = R_D \times \frac{\frac{1}{sC_L}}{R_D + \frac{1}{sC_L}} = \frac{R_D}{1+sC_L R_D}$

$|A_d(s)| = \frac{-g_m R_D}{1+sC_L R_D} = \frac{-g_{m1} R_D + j.0}{1 + \frac{j\omega}{\omega_H}}$

$|A_d(s)| = \frac{g_m R_D}{\sqrt{1+\left(\frac{\omega}{\omega_H}\right)^2}}$

$f_H = \frac{1}{2\pi R_D C_L}$

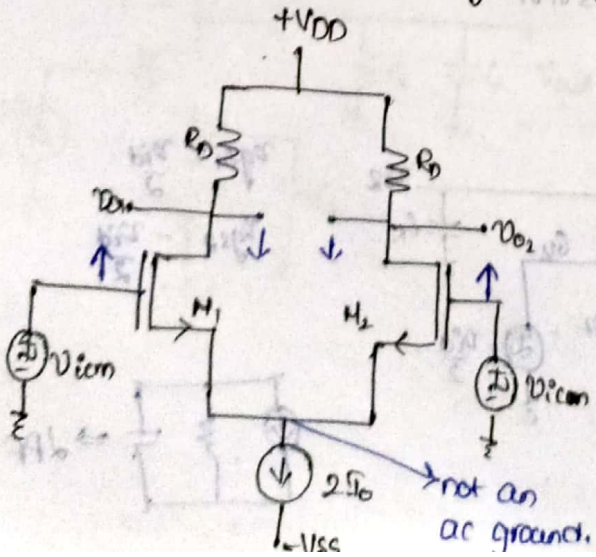
$2\pi f_H = \frac{1}{R_D C_L}$

$\omega_H = \frac{1}{R_D C_L}$

@ $\omega = 0$ (dc) gain $\Rightarrow |A_d(s)|_{@\omega=0} = g_m R_D$ ** → DC gain.

@ $\omega = \omega_H \Rightarrow |A_d(s)|_{@\omega=\omega_H} = \frac{g_m R_D}{\sqrt{1+\left(\frac{\omega_H}{\omega_H}\right)^2}} = \frac{g_m R_D}{\sqrt{2}}$

* If common mode (Noise) signals gave, what will be the gain.



V_{icm} ⇒ common mode signals.

$A_{icm} = \frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}}$

↓

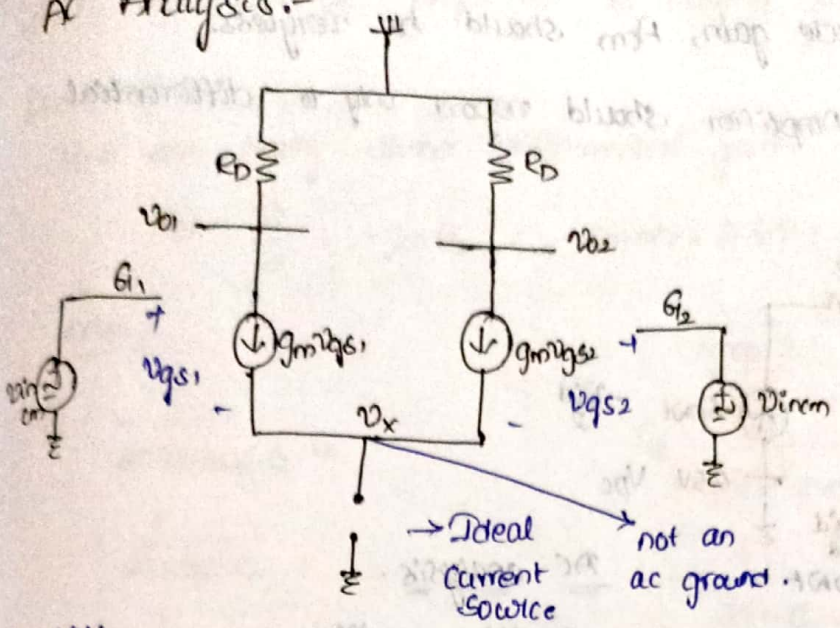
Common Mode gain [single ended]

[∵ difference will not be seen here].

both are going in same direction.

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AC Analysis:-



KVL

$-v_{icm} + v_{gs1} + v_x = 0 \rightarrow (1)$

$-v_{icm} + v_{gs2} + v_x = 0 \rightarrow (2)$

(+) (−) (−)

$v_{gs1} = v_{gs2} \rightarrow (I)$ [not differential signal].

Nodal @ v_x

$g_m v_{gs1} = -g_m v_{gs2}$

$v_{gs1} + v_{gs2} = 0 \rightarrow (II)$

from I & II

$$\boxed{v_{gs1} = v_{gs2} = 0}$$

$v_{o1} = -g_m v_{gs1} R_D = 0$

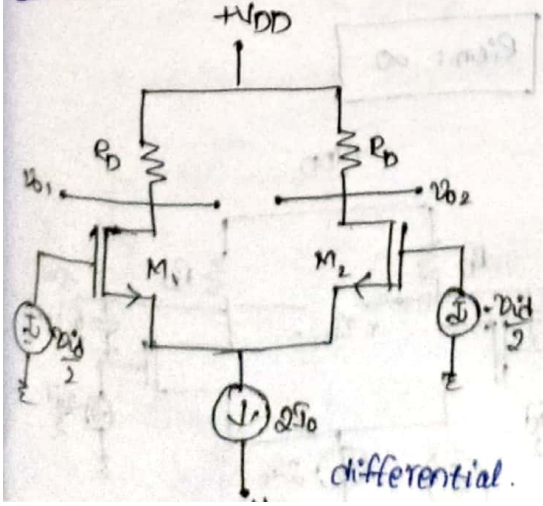
$v_{o2} = -g_m v_{gs2} R_D = 0$

$\Rightarrow \frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} = 0 = A_{cm}$ (common mode gain)

↓

for the ideal tail-current source.

13/2/22



differential.

Common mode signal ⇒ undesired.

↓

which is common to both the input v_{in1} & v_{in2}

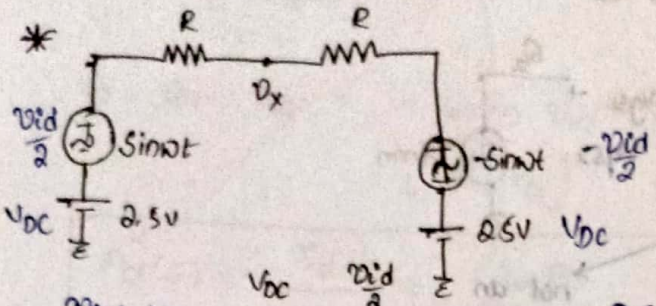
→ We treat common mode signal as noise.

→ Differential Amplifier shouldn't respond to common mode signal.

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i.e., Common mode gain, A_{cm} should be very less.

→ Differential Amplifier should respond only to differential i/p signal.

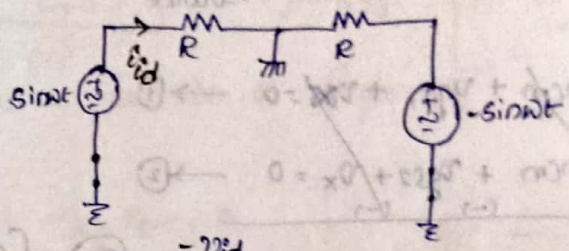


V_{DC} $\frac{v_{id}}{2}$

$v_{in1} = 2.5V + \sin\omega t$

$v_{in2} = 2.5V - \sin\omega t$

AC analysis.

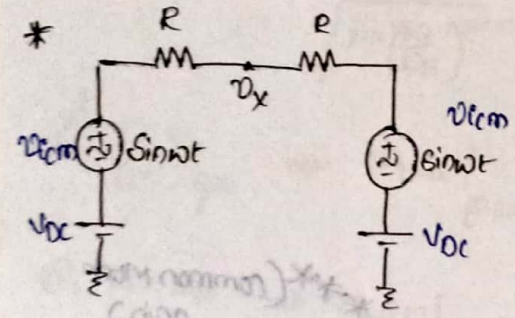


Instantaneous value

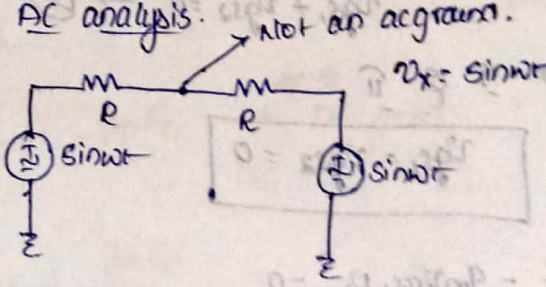
$v_x = 2.5V + 0(\sin\omega t)$

$-\frac{v_{id}}{2} + i_{id}R = 0$

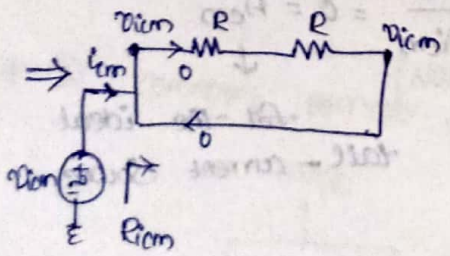
differential input resistance ← $R_{id} = \frac{v_{id}}{i_{id}} = 2R$



AC analysis.



Instantaneous value of $v_x = 2.5V + \sin(\omega t)$ mV.



$R_{icm} = \frac{v_{icm}}{i_{cm}} = \frac{v_{icm}}{0} = \infty$

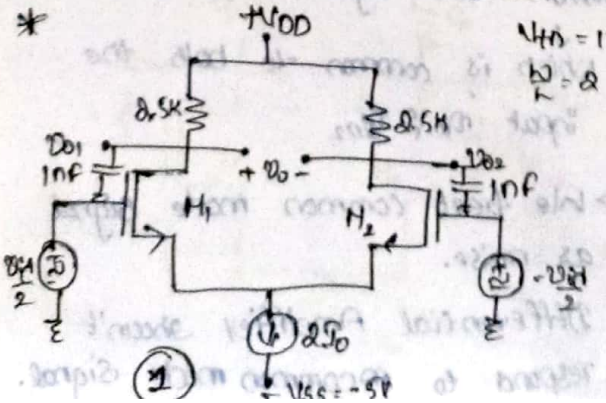
$[\because i_{icm} = 0]$

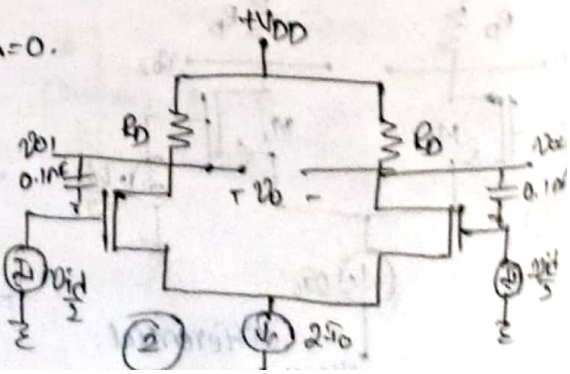
$\Rightarrow R_{icm} = \infty$

$\mu_n C_{ox} = 1mA/V^2$

$V_{tn} = 1V$

$\frac{W}{L} = 2, \lambda = 0.$





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which differential Amplifier is having more speed.

Observation:

Both are having same differential gain

$$A_d = \frac{v_i}{v_o} = -g_m R_D = -2mA/V \times 2.5k = -5 V/V.$$

Amp 1

$$f_H = \frac{1}{2\pi R_{across,C_L} \cdot C_L}$$

$$= \frac{1}{2\pi \times R_D \cdot C_L}$$

$$= \frac{1}{2\pi \times 2.5k \times 1nF}$$

$f_H = 63.6\ kHz$

$f_L = 0$

$BW = f_H - f_L = 636\ kHz.$

Amp 2

$$f_H = \frac{1}{2\pi \cdot R_{across,C_L} \cdot C_L}$$

$$= \frac{1}{2\pi \times R_D \times C_L}$$

$$= \frac{1}{2\pi \times 2.5k \times 0.1nF}$$

$f_H = 636\ kHz$; $f_L = 0$

$(B.W) = f_H - f_L = 636\ kHz.$

$$f_H = \frac{1}{2\pi RC} = \frac{1}{2\pi\tau}$$ → time constant.

** low τ ⇒ high speed ⇒ Bandwidth high.

What is the τ of this Amplifier. ⇒ $R_D \cdot C_L$.

⇒ Amp. 2 has high speed.

* τ is more for 1, less for 2.

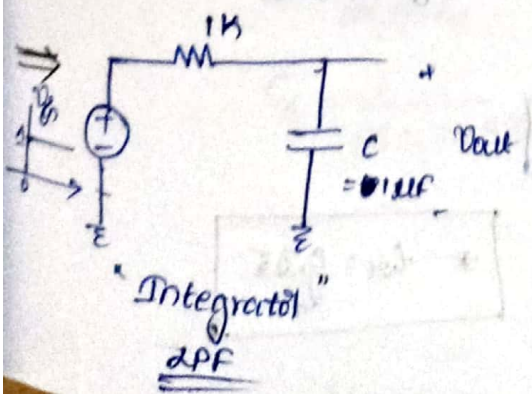
Speed is less for 1, less high for 2.

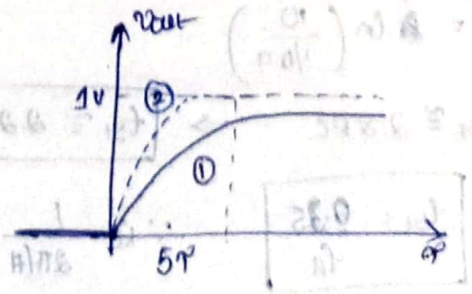
* ⇒ Speed is directly proportional to Bandwidth.

[speed ∝ BW]

⇒ $(B.W)_2 = 10.(B.W)_1$.

⇒ differential Amplifier ② having more speed.





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$R = 1K, C = 1\mu F$

1) $\tau_1 = RC$

$\tau_1 = 1K \times 1\mu F = 1ms \Rightarrow f_H = \frac{1}{2\pi \times 1K \times 1\mu F} = 159.15Hz.$

2) $\tau_2 = 0$

$\Rightarrow f_H = \frac{1}{2\pi \times 1K \times 0.1\mu F} = 1.59KHz.$ more f_H. $\Rightarrow$ more. BW

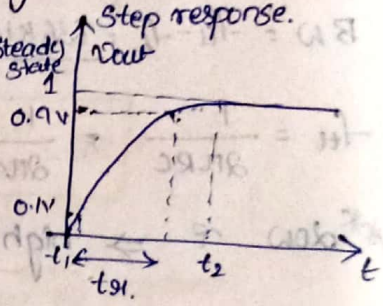
$\Rightarrow$ more speed $\Rightarrow$ low τ.

$$V_{out}(t) = V_{out\,final} + \left[V_{out\,initial} - V_{out\,final}\right] e^{-t/RC}$$

$$= 1V + (0-1)e^{-t/\tau}$$

$$\boxed{V_{out}(t) = 1 - e^{-t/\tau}}$$

Rise time 't_{r1}' :- The time taken to charge the cap. from 10% to 90%.



$V_{out}(t) = 1 - e^{-t/\tau}$

@ $t = t_1 \Rightarrow V_{out}(t = t_1) = 0.1V.$

$0.1V = 1 - e^{-t/\tau}$

$e^{-t/\tau} = 0.9V$

$\Rightarrow e^{t_1/\tau} = \frac{1}{0.9V}$

$$t_1 = \tau \ln\left(\frac{1}{0.9}\right)$$

@ $t = t_2 \Rightarrow V_{out}(t = t_2) = 0.9V$

$0.9V = 1 - e^{-t/\tau}$

$e^{-t/\tau} = 0.1$

$\frac{1}{0.1V} = e^{t_2/\tau}$

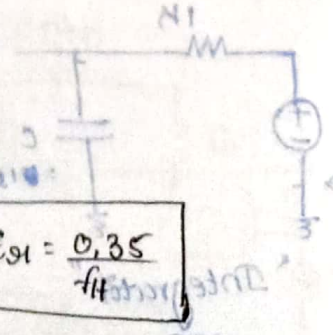
$t_2 = \tau \ln\left(\frac{1}{0.1}\right) = t_2 = \tau \ln 10.$

$t_2 - t_1 = \tau \ln\left(\frac{10}{1/0.9}\right)$

$t_{r1} \cong 2.2RC \Rightarrow \boxed{t_{r1} \cong 2.2\tau}$

$\boxed{t_{r1} = \frac{0.35}{f_H}}$ $\because RC = \frac{1}{2\pi f_H}$

$\star\ \boxed{t_{r1} = \frac{0.35}{f_H}}$

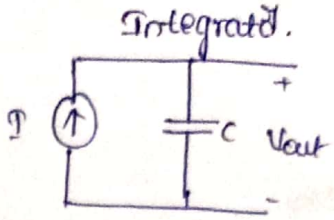


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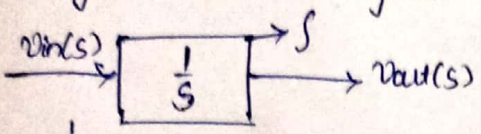
* We can realize an integrator with an capacitor. (Bucket)

Integral, Differentials ⇒ Linear.

⇒ Caps, & Inductors are Linear.



* Integrator is lowpass filter.

* 

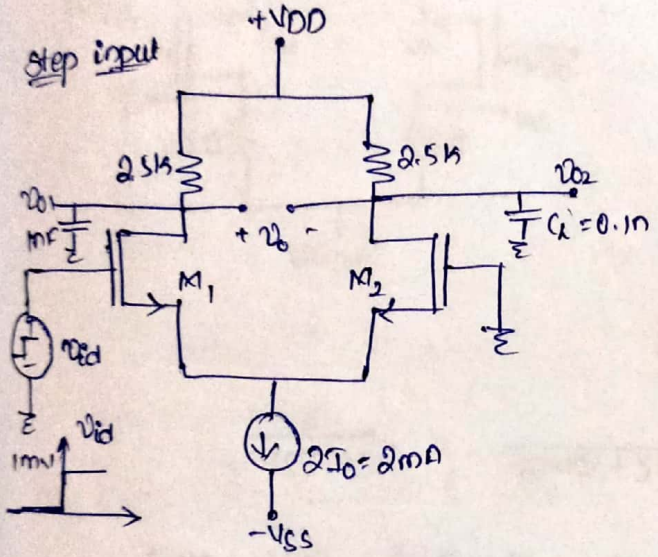
$\frac{1}{S} = \frac{1}{j\omega}$

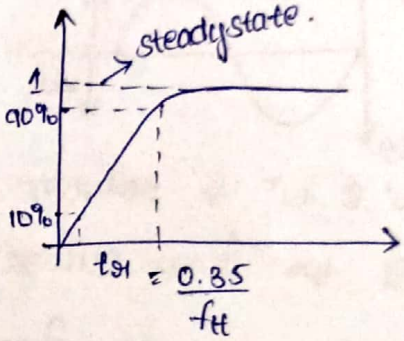
at $\omega = 0 \Rightarrow$ value ∞

$\omega = \infty \Rightarrow 0$

⇒ lowpass filter.

Step Response of Differential Amplifier.





Design a differential amplifier for having a rise time 1 μs for a step input.

$t_{sl} = \frac{0.35}{f_H} \Rightarrow f_H = \frac{0.35}{1\mu s} \Rightarrow f_H = 350\ kHz$

$f_H = \frac{1}{2\pi R_{acros,} C_L C_L} = 350kHz$

Assuming MOS is in sat let $R_D = 3k\Omega$

$\Rightarrow C_L = \frac{1}{2\pi R_D f_H}$

$C_L = \frac{1}{2\pi \times 3K \times 350K} \Rightarrow C_L = 1.51 \times 10^{-10} F.$

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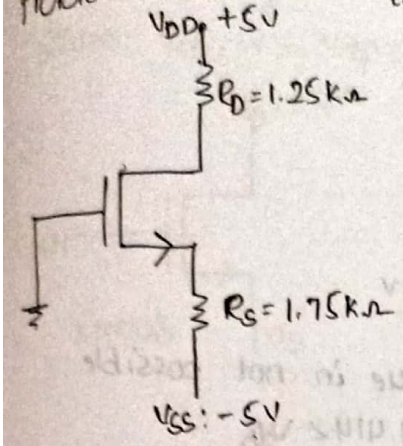
Assignment - 2

N180119
M. Suryakumari

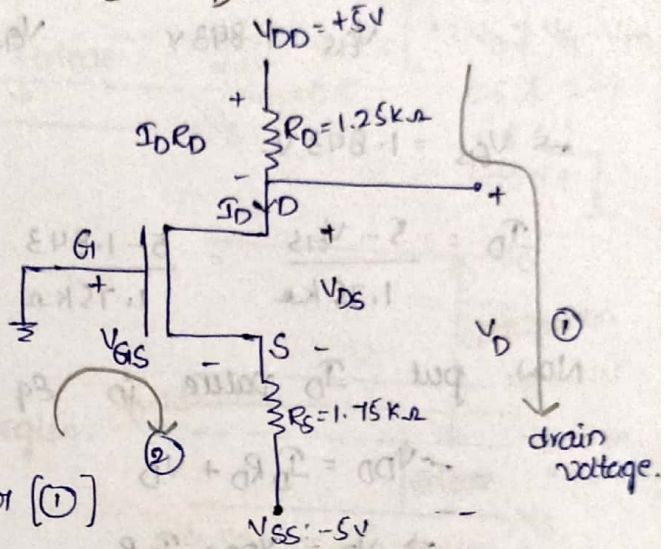
Problem :- Given :- $V_{tn} = 0.5V$

$\mu_n C_{ox} = 1mA/V^2$

$\left(\frac{W}{L}\right)_n = 2$



Find V_D & I_D



Sol:- i, It is NMOS.

ii, Mark the terminals.

$V_D = V_D - 0V$

By Applying KVL in outter [1]

$$V_{DD} = I_D R_D + V_D \longrightarrow (1)$$

$$I_D = -\frac{1}{R_D} V_D + \frac{V_{DD}}{R_D} \longrightarrow (2)$$

Assume NMOS is in saturation region

$$V_{DS} \geq V_{GS} - V_t$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n [V_{GS} - V_t]^2$$

$$I_D = \frac{1}{2} \times 1m \times 2 [V_{GS} - 0.5]^2 \longrightarrow (2)$$

Apply KVL in loop (2)

$$V_{GS} + I_D R_S - 5 = 0$$

$$I_D = \frac{5 - V_{GS}}{1.75k\Omega} \longrightarrow (3)$$

Solving (2) & (3)

$$\frac{5 - V_{GS}}{1.75k\Omega} = \frac{1}{2} \times 1m \times 2 [V_{GS} - V_t]^2$$

$$5 - V_{GS} = 1.75 [V_{GS} - 0.5]^2$$

$$5 - V_{GS} = \frac{7}{4} [V_{GS}^2 + 0.25 - V_{GS}]$$

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$$20 - 4V_{GS} = 7V_{GS}^2 + \frac{7}{4} - 7V_{GSn}$$

$$7V_{GS}^2 + \frac{7}{4} - 7V_{GSn} - 20 + 4V_{GSn} = 0$$

$$7V_{GS}^2 - 3V_{GSn} - \frac{73}{4} = 0$$

$$1.75V_{GS}^2 - 0.75V_{GS} - 4.5625 = 0$$

$V_{GS} = 1.843\,V$ $\qquad$ $V_{GS} = -1.414\,V$

$\Rightarrow V_{GS} = 1.843\,V.$ $\qquad$ this value in not possible $\because -1.414 < V_{th}$

$$I_D = \frac{5 - V_{GS}}{1.75\,k\Omega} = \frac{5 - 1.843}{1.75\,k\Omega} = 1.804\,mA.$$

Now put I_D value in Eq ①

$$V_{DD} = I_D R_D + V_D$$

$$\Rightarrow V_D = V_{DD} - I_D R_D$$

$$= 5 - (1.804m \times 1.25K)$$

$$V_D = 2.745\,V.$$

Now justify our assumption

In Saturation, $V_{DS} \geq V_{GS} - V_{th}$

$$V_D - V_S \geq V_G - V_S - V_{th}$$

$$2.745 > 0 - 0.5$$

$$2.745 > -0.5$$

$\therefore$ MOSFET is in saturation region.

$I_D = 1.804mA$, $V_D = 2.745\,V$

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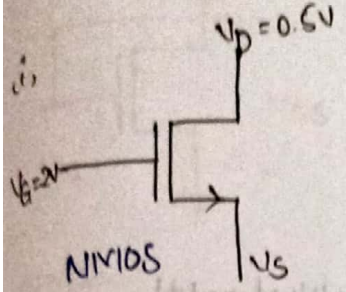
Assignment-3

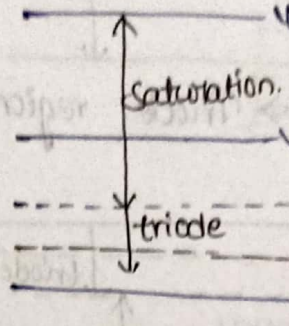
N180119
M. Suryakumari.

Find the region of operation for the following

Given $V_{tn} = 1V$, $V_{tp} = -1V$, $V_{GSn} > V_{tn}$; $V_{SGp} > |V_{tp}|$

(i)





$\Rightarrow$ triode region.

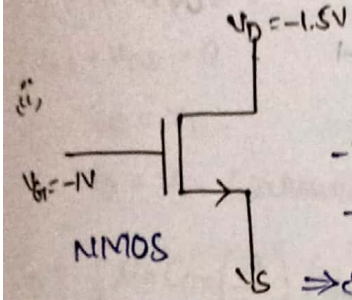
[$\because V_D \not\geq V_G - V_{tn}$

$0.5 \not\geq 2 - 1$

$0.5 \leq 1$

triode]

(ii)

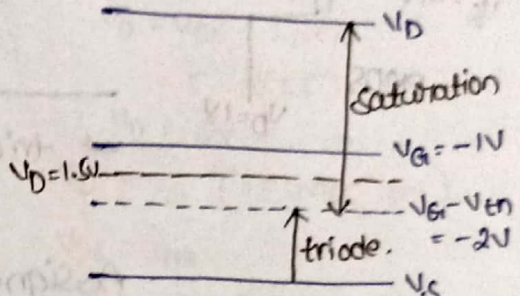


$V_D \geq V_G - V_{tn}$

$-1.5 \geq -1 - 1$

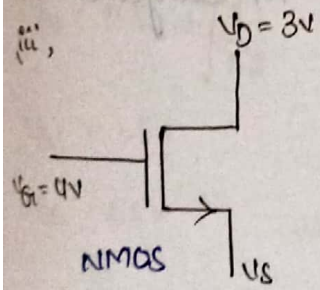
$-1.5 \geq -2V$

$\Rightarrow$ Saturation region.



$\Rightarrow$ saturation region.

(iii)

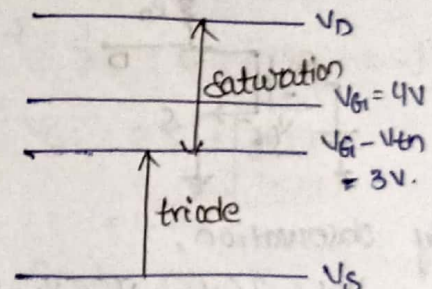


$V_D \geq V_G - V_{tn}$

$3 \geq 4 - 1$

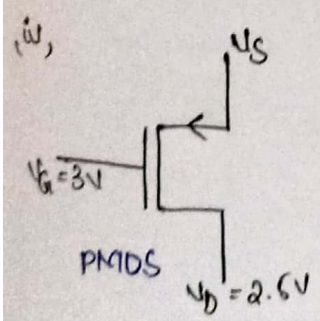
$3 = 3$

$\Rightarrow$ Saturation region. (Edge).



$\Rightarrow$ Edge of saturation.

(iv)

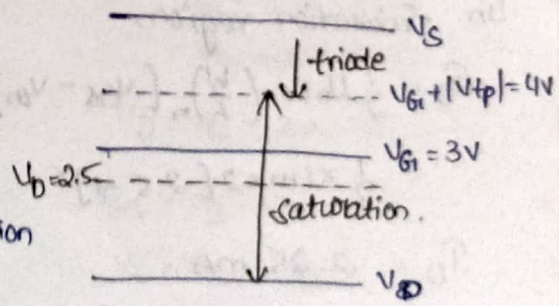


$V_D \leq V_G + |V_{tp}|$

$2.5 \leq 3 + 1$

$2.5 \leq 4$

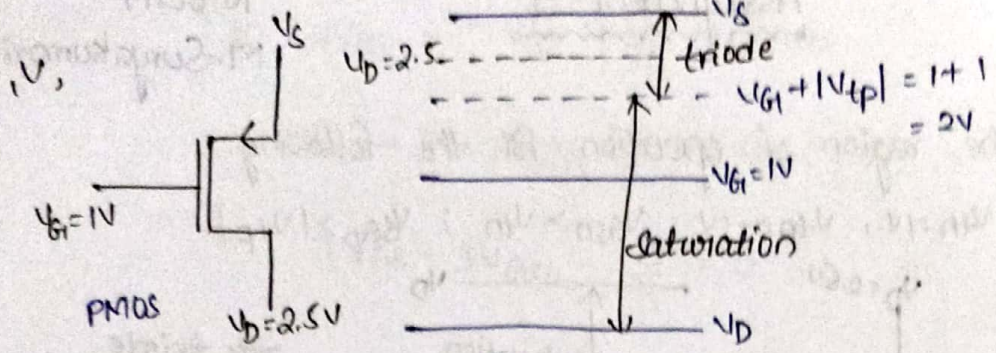
$\Rightarrow$ saturation region



$\Rightarrow$ Saturation region.

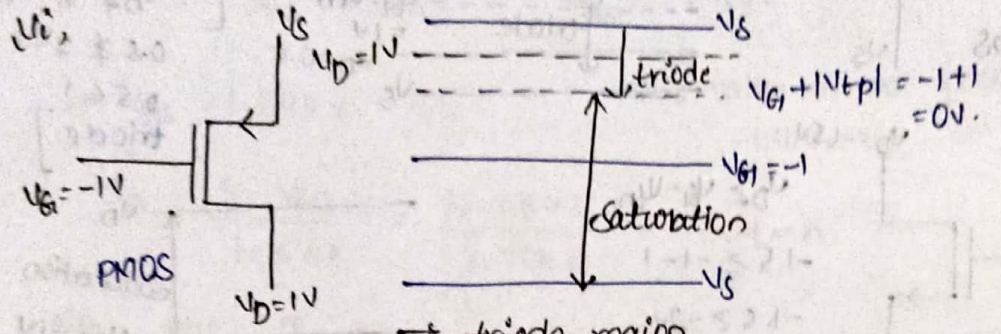
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(v)



⇒ Triode region.

(vi)

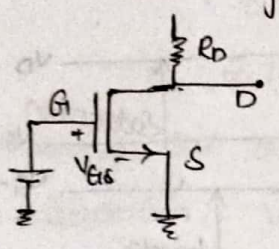


⇒ triode region.

Assignment-4

N180119
M. Suryakumari

Repeat the above problem



Given $V_{tn} = 1V$

$\left(\frac{W}{L}\right)_n = 2$

$\mu_n C_{ox} = 1 mA/V^2$

By observation,

$V_{GS} = 2.5V$, $V_D = V_G - V_{tn} = 2.5 - 1 = 1.5V$

$V_D = V_{DD} - I_D R_D$

In saturation region,

$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n [V_{GS} - V_{tn}]^2$

$= \frac{1}{2} \times 1m \times 2 [2.5-1]^2$

$I_D = 2.25 mA.$

$V_D = V_{DD} - I_D R_{Dmax}$

$1.5 = 5 - 2.25 (R_D max)$

$R_{Dmax} = \frac{5-1.5}{2.25} = 1.5 k\Omega$

$\boxed{R_{Dmax} = 1.5 k\Omega}$

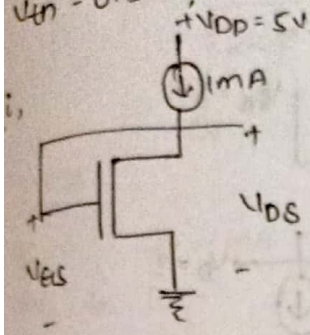
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Assignment

N180119
M. Surya kumari.

$V_{tn} = 0.5V$, $\mu_n C_{ox} = 1mA/V^2$, $\left(\frac{W}{L}\right)_n = 2$

i,



NMOS.

$I_D = 1mA$

$-V_{GS} + V_{DS} = 0$

$V_{GS} = V_{DS}$

$V_D = V_G$ (Saturation)

$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS} - V_{tn})^2$

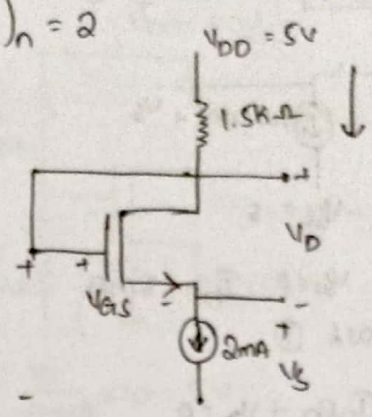
$1 = \frac{1}{2} \times 1 \times 2 [V_{GS} - 0.5]^2$

$V_{GS} = 0.5 + \sqrt{\frac{2.1}{1.2}}$

$V_{GS} = 1.5V$

$V_{DS} = 1.5V$

ii,



$V_{SS} = 5V$

NMOS.

$I_D = 2mA$

$V_D = V_{DD} - I_D R_D$

$= 5 - 2(1.5)$

$V_D = 2V$

$V_D > V_G$ (N MOS ON)

$V_{GS} = V_{DS}$

$V_G = V_D$ (Saturation)

$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS} - V_{tn}]^2$

$2 = \frac{1}{2} \times 1 \times (2) [V_{GS} - 0.5]^2$

$V_{GS} = 0.5 + \sqrt{\frac{2(2)}{1 \times 2}}$

$= 1.914$

Apply KVL,

$-5 + 1.5(I_D) + V_D = 0$

$V_D = 5 - 1.5k(2)$

$V_D = 2V$

$V_D = V_G = 2V$.

$V_{GS} = V_G - V_S$

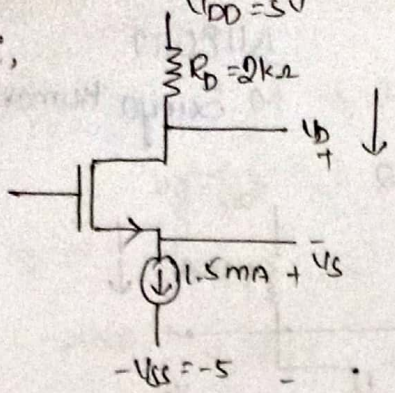
$V_S = V_{GS} - V_G$

$= -1.914 + 2$

$V_S = 0.086$

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(iii)



NMOS. $V_G=0$ $I_D=1.5mA$

Apply KVL ①

$-V_{DD}+I_DR_D+V_D=0$

$V_D=5-1.5(2)$

$V_D=2V$

Assume saturation

$I_D=\frac{1}{2}\mu_nC_{ox}\left(\frac{W}{L}\right)_n(V_{GS}-V_{tn})^2$

$V_{GS}=0.5+\sqrt{\frac{2(1.5)}{1(2)}}$

$=0.5+1.225$

$V_{GS}=1.725$

KVL in inner loop

$-V_{GS}-V_S=0$

$V_S=-V_{GS}=-1.725$

$V_{DS}=V_D-V_S$

$=2+1.725$

$V_{DS}=3.725$

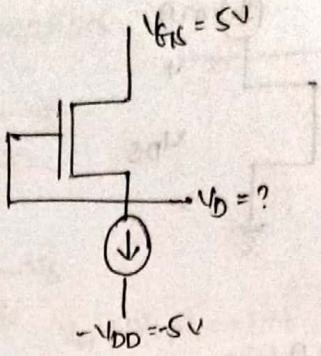
$V_D=2V > V_G$

$\Rightarrow$ Saturation

(iv) $V_{tp}=-0.5V$

$\mu_nC_{ox}=0.5mA/V^2$

$\left(\frac{W}{L}\right)_p=2$



PMOS.

$V_{DS}=V_{GS}$

$V_D=V_G$

Diode is connected

$\Rightarrow$ saturation region.

$V_{SG}=|V_{tp}|+\sqrt{\frac{2(2)}{(0.5)^2}}$

$=0.5+2$

$=2.5V$

$V_{SG}=V_S-V_G$

$=5-V_G$

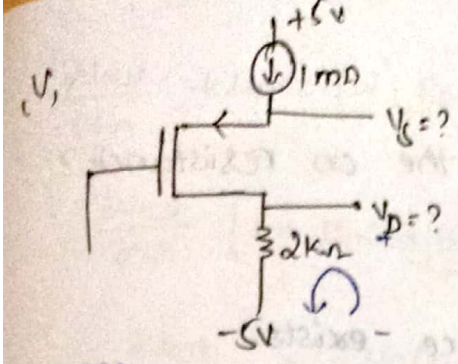
$V_G=5-2.5$

$V_G=2.5V$

$V_D=V_G$

$V_D=2.5V.$

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PMOS.

$V_G = 0$, $I_D = 1mA$

KVL in loop

$-V_D + 2(I_D) - 5 = 0$

$V_D = -5 + 2(1)$

$V_D = -3V$

Assume it is in saturation region.

$$V_{SG} = |V_{tp}| + \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_p}}$$

$$= 0.5 + \sqrt{\frac{2(1)}{0.5(2)}}$$

$$= 0.5 + 1.414$$

$V_{SG} = 1.914V$

$V_{SG} = V_S - V_G$

$V_{SG} = V_S - 0$

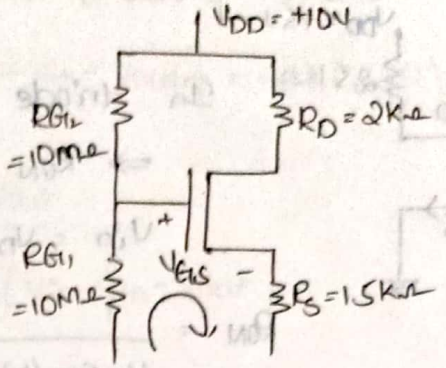
$V_{SG} = V_S = 1.914$

$V_S > V_G$

$\Rightarrow$ Saturation region.

Q. $\mu_n C_{ox} = 1mA/V^2$, $\left(\frac{W}{L}\right)_n = 2$

Find V_{GS}, I_D, V_D, V_S & V_{DS}



$$V_G = \frac{10}{10+10} \times 10 = 5V$$

Apply KVL

$-V_G + V_{GS} + 1.5K(I_D) = 0$

$$I_D = \frac{V_G - V_{GS}}{1.5} = \frac{5 - V_{GS}}{1.5} \rightarrow (1)$$

Assume it is in saturation

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS} - V_{th}]^2$$

$$= \frac{1}{2} \times 1 \times 2 [V_{GS} - 1]^2 \rightarrow (2)$$

from (1) & (2)

$$\frac{5 - V_{GS}}{1.5} = V_{GS}^2 - 2V_{GS} + 1$$

$5 - V_{GS} = 1.5V_{GS}^2 - 3V_{GS} + 1.5$

$V_{GS} = 2.33, -1$

$\boxed{V_{GS} = 2.33}$

$$I_D = \frac{5 - 2.33}{1.5} \Rightarrow I_D = 1.78$$

$V_S = I_D R_S = 1.78 \times 1.5 = 2.67V$

$V_{DS} = V_D - V_S = 6.414 - 2.67$

$V_{DS} = 3.77V$

$V_D = 10 - 2K(I_D)$

$= 10 - 2(1.78)$

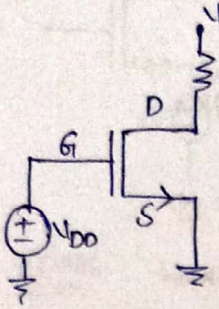
$V_D = 6.414$

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30/12/21

Assignment

* For the above problem, what is the on resistance?



In triode region,

$\Rightarrow R_{ON}$ resistance exists.

$V_{in} = V_{DD} = 5V = V_{GS}$

$$R_{ON} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_n [V_{GS} - V_{th}]}$$

$$= \frac{1}{1 \times 2(5-1)} = \frac{1}{g_m} = 125\,k\Omega$$

$$\boxed{R_{ON} = 125\,k\Omega}$$

* Find slope $\frac{\partial V_{out}}{\partial V_{in}}$ in triode region at $V_{in} = 3V$.

In triode region,

$V_{in} = 3V$

We know that

$$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[(V_{in} - V_{th}) V_{out} - \frac{1}{2} V_{DS}^2\right]$$

$$V_{DS} = V_{out} = V_{DD} - I_D R_D$$

$$\text{Gain} = \frac{\partial V_{out}}{\partial V_{in}}$$

$$V_{out} = V_{DD} - \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[(V_{GS} - V_{th}) V_{out} - \frac{1}{2} V_{DS}^2\right] R_D$$

Here $V_{GS} = V_{in}$; $V_{DS} = V_{out}$

$$V_{out} = V_{DD} - \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[(V_{in} - V_{th}) V_{out} - \frac{1}{2} V_{out}^2\right] R_D$$

Now,

$$\frac{\partial V_{out}}{\partial V_{in}} = 0 - \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[(1) V_{out} + \frac{\partial V_{out}}{\partial V_{in}} (V_{in} - V_{th}) - \frac{2}{2} V_{out} \cdot \frac{\partial V_{out}}{\partial V_{in}}\right]$$

$$\frac{\partial V_{out}}{\partial V_{in}} = \left[-\mu_n C_{ox} \left(\frac{W}{L}\right)_n R_D V_{out} - \mu_n C_{ox} \left(\frac{W}{L}\right)_n R_D \frac{\partial V_{out}}{\partial V_{in}} [V_{in} - V_{th} - V_{out}]\right]$$

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$$\frac{\partial V_{out}}{\partial V_{in}} + \mu_n C_{ox}\left(\frac{W}{L}\right)_n R_D \frac{\partial V_{out}}{\partial V_{in}}\left[V_{in} - V_{tn} - V_{out}\right] = -\mu_n C_{ox}\left(\frac{W}{L}\right)_n R_D V_{out}$$

$$\frac{\partial V_{out}}{\partial V_{in}}\left[1 + \mu_n C_{ox}\left(\frac{W}{L}\right)_n R_D\left[V_{in} - V_{tn} - V_{out}\right]\right] = -\mu_n C_{ox}\left(\frac{W}{L}\right)_n R_D V_{out}$$

$$\frac{\partial V_{out}}{\partial V_{in}} = \frac{-\mu_n C_{ox}\left(\frac{W}{L}\right)_n R_D V_{out}}{1 + \mu_n C_{ox}\left(\frac{W}{L}\right)_n R_D\left[V_{in} - V_{tn} - V_{out}\right]}$$

at $V_{in} = 3 \Rightarrow$ ~~$V_{out} = 0.514$~~

$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)_n \left[(V_{in} - V_{tn})V_{out} - \frac{1}{2}V_{out}^2\right]$$

$$V_{out} = 5 - I_D R_D \quad (I_D = 0)$$

$$= 5 - (1m)(2)\left[(3-1)V_{out} - \frac{1}{2}V_{out}^2\right]$$

$$V_{out} = 5 - 5\left[2V_{out} - \frac{1}{2}V_{out}^2\right]$$

$$2V_{out} = 10 - 10\left[2V_{out} - V_{out}^2\right]$$

$$2V_{out} = 10 - 20V_{out} + 10V_{out}^2$$

$$10V_{out}^2 - 22V_{out} + 10 = 0$$

$$5V_{out}^2 - 11V_{out} + 5 = 0$$

$$V_{out} = 0.51477, \quad 3.8853 \times \quad (\because V_{DS} < V_{GS} - V_{tn})$$

$$\Rightarrow V_{out} = 0.514$$

Now,

$$\frac{\partial V_{out}}{\partial V_{in}} = \frac{-\mu_n C_{ox}\left(\frac{W}{L}\right)_n R_D V_{out}}{1 + \mu_n C_{ox}\left(\frac{W}{L}\right)_n R_D\left[V_{in} - V_{tn} - V_{out}\right]}$$

$$= \frac{-(1m)(2) \times 2.5K \times 0.51477}{1 + 1m \times 2.5K \times 2\,(3 - 1 - 0.51477)}$$

$$= -0.30546$$

$$\left|\frac{\partial V_{out}}{\partial V_{in}}\right| = 0.30546$$

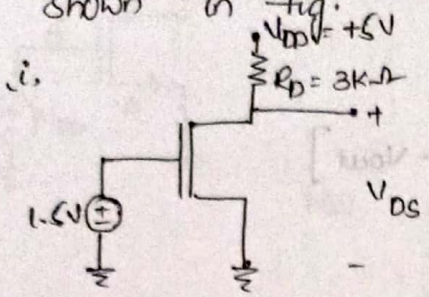
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Assignment

N180119
M. Surya Kumari.

1. Draw the load lines for the following MOSFET circuits shown in fig.

i.



$V_{tn} = 0.5V$

$\left(\frac{W}{L}\right)_n = 2$

$\mu_n C_{ox} = 1mA/V^2$

Apply KVL,

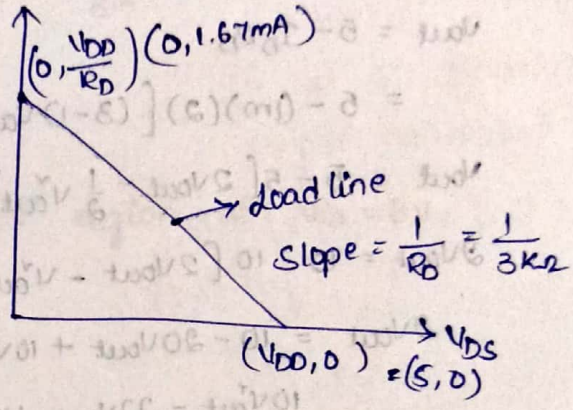
$V_{DD} = I_D R_D + V_{DS}$

$I_D = -\frac{1}{R_D} V_{DS} + \frac{V_{DD}}{R_D}$

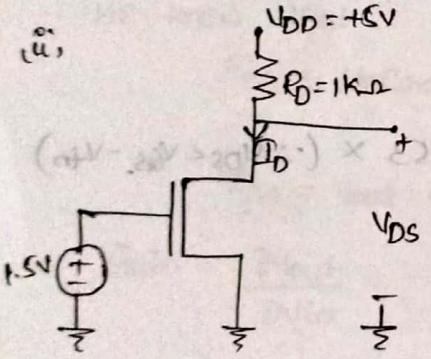
$y = mx + c$

$\therefore m = -\frac{1}{R_D} = -\frac{1}{3}$

$c = \frac{V_{DD}}{R_D} = \frac{5}{3K\Omega}$



ii.



$V_{tn} = 0.5V$

$\left(\frac{W}{L}\right)_n = 3$

$\mu_n C_{ox} = 1mA/V^2$

Apply KVL

$V_{DD} = I_D R_D + V_{DS}$

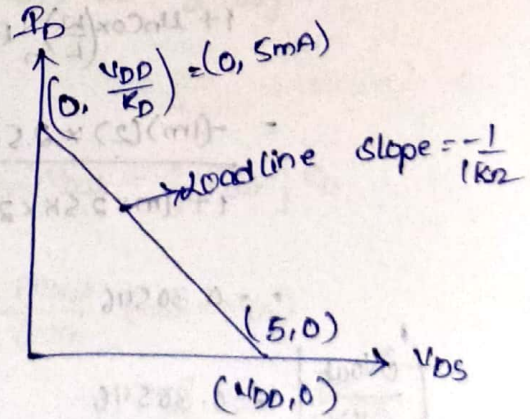
$I_D = -\frac{1}{R_D} V_{DS} + \frac{V_{DD}}{R_D}$

(load line Eqn)

x - intercept, $V_{DD} = 5V$

y - intercept, $c = \frac{V_{DD}}{R_D} = \frac{5}{1K\Omega} = 5mA$

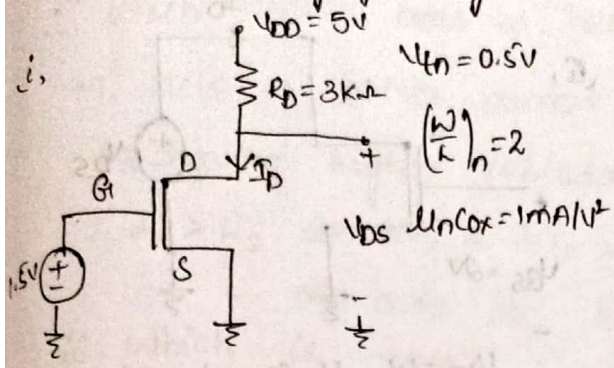
slope = $m = -\frac{1}{R_D} = -\frac{1}{1K\Omega}$



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2. For the above circuits find Q i.e, operating point & show this graphically.

i,



$V_S = 0 \Rightarrow V_{GS} = 1.5V$

Assume MOSFET in sat. region.

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS} - V_{tn}]^2$$

$$= \frac{1}{2} \times 1 \times 2 [1.5 - 0.5]^2$$

$I_D = 1mA$

Apply KVL in outer loop

$V_{DS} = V_{DD} - I_D R_D = 5 - 1(3) = 2V$

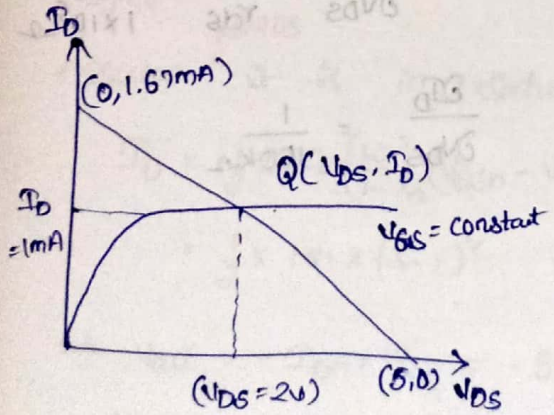
Check:

$V_{DS} > V_{GS} - V_{tn}$

$2 > 1.5 - 0.5$

$2 > 1$ (True)

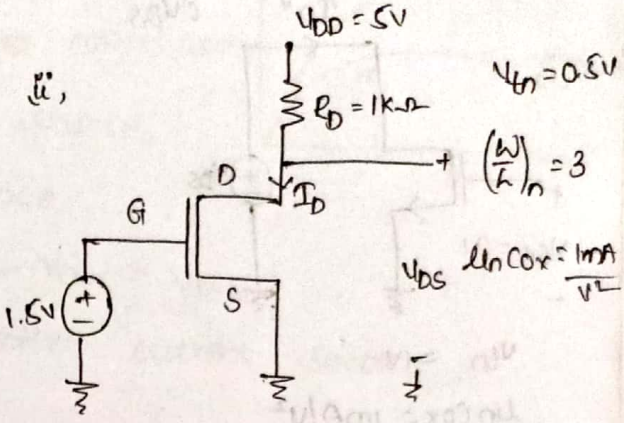
(MOSFET in saturation)



$Q(V_{DS}, I_D) = (2, 1mA)$

N180119

ii,



$V_S = 0 \Rightarrow V_{GS} = 1.5V$

Assume MOSFET in in sat.

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS} - V_{tn}]^2$$

$$= \frac{1}{2}(1)(3)[1.5 - 0.5]^2$$

$I_D = 1.5mA$

Apply KVL in outer loop

$V_{DS} = V_{DD} - I_D R_D$

$= 5 - 1.5(3)$

$= 3.5V$

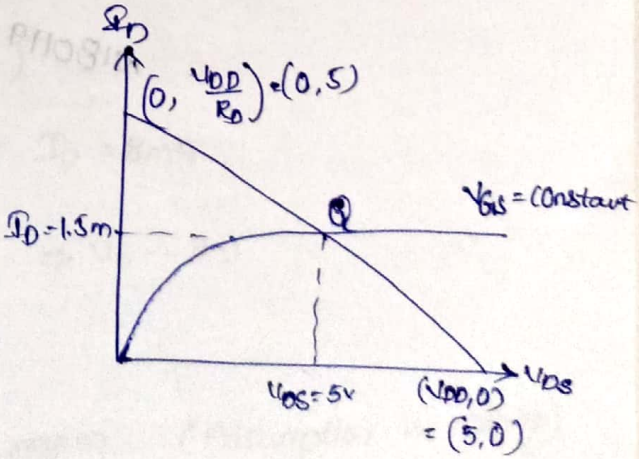
Check:

$V_{DS} > V_{GS} - V_{tn}$

$3.5 > 1.5 - 0.5$

$3.5 > 1$ (True)

$\Rightarrow$ MOSFET is in sat.

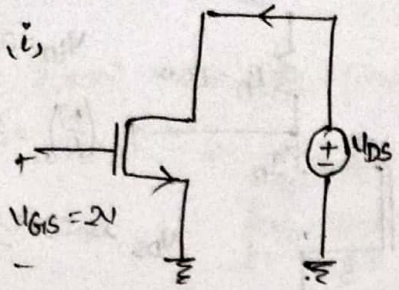


$Q(V_{DS}, I_D) = (3.5, 1.5mA)$

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3. Find the slope $\frac{\partial I_D}{\partial V_{DS}}$ in saturation region for MOSFET.

(i)



$V_{th} = 1V$

$\mu_n C_{ox} = 1mA/V^2$

$\left(\frac{W}{L}\right)_n = 2$, $V_A = 100V$

Given,

MOSFET in sat. region.

$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS} - V_{th}]^2$

$= \frac{1}{2}(1)(2)[2-1]$

$I_D = 1mA$

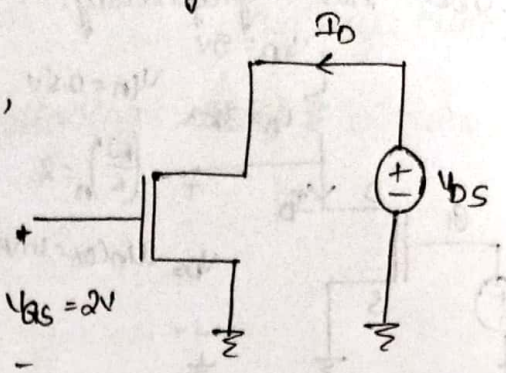
$\lambda = \frac{1}{V_A} = \frac{1}{100} = 0.01V^{-1}$

$r_{DS} = \frac{1}{\lambda_n I_D} = \frac{1}{0.01 \times 1mA} = 1 \times 10^5 \Omega$

Slope $= \frac{\partial I_D}{\partial V_{DS}} = \frac{1}{r_{ds}} = \frac{1}{1 \times 10^5}$

$\frac{\partial I_D}{\partial V_{DS}} = \frac{1}{100k\Omega}$

(ii)



$V_{th} = 1V$, $\mu_n C_{ox} = 1 mA/V^2$

$\left(\frac{W}{L}\right)_n = 2$, $\lambda_n = 0.01V^{-1}$

Given,

MOSFET is in Sat. region

$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{GS} - V_{th}]^2$

$= \frac{1}{2} \times 1mA \times 2 \times [2-1]^2$

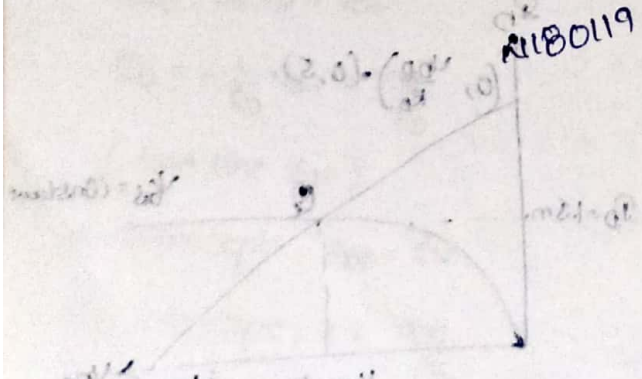
$I_D = 1mA$

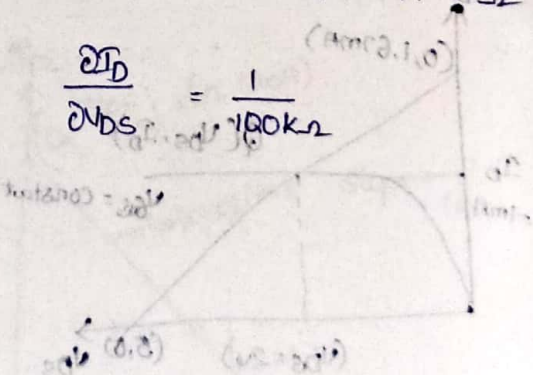
$\lambda = \frac{1}{V_A} = 0.01V^{-1}$

$r_{ds} = \frac{1}{\lambda_n I_D} = \frac{1}{0.01 \times 1mA} = 1 \times 10^5 \Omega$

Slope $= \frac{\partial I_D}{\partial V_{DS}} = \frac{1}{r_{ds}} = \frac{1}{1 \times 10^5 \Omega}$

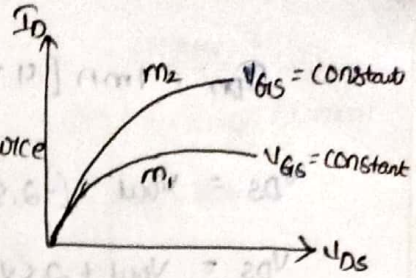
$\frac{\partial I_D}{\partial V_{DS}} = \frac{1}{100k\Omega}$





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* Which MOSFET has longer channel?



i, Which MOSFET acts as better current source

M_1 acts as better current source,

M_1 having higher resistance

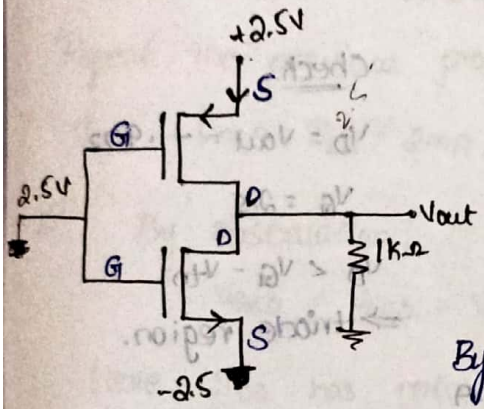
$L_1 > L_2 \Rightarrow \lambda_{n1} < \lambda_{n2} \Rightarrow r_{ds1} > r_{ds2}$

$\therefore$ M_1 acts as better current source.

ii, Which is true?

(A) $r_{ds1} > r_{ds2}$ B) $r_{ds1} < r_{ds2}$ C) $r_{ds1} = r_{ds2}$

Since $\lambda_{n1} < \lambda_{n2} \Rightarrow r_{ds1} > r_{ds2}$ N180119



$\mu_n C_{ox}\left(\frac{W}{L}\right)_n = 1mA/V^2$; $\mu_p C_{ox}\left(\frac{W}{L}\right)_p = 1mA/V^2$

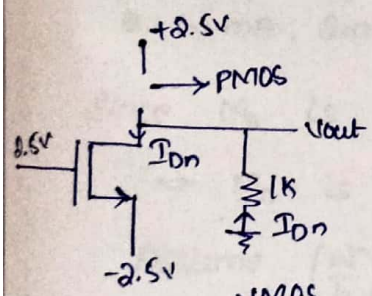
$V_{tn} = |V_{tp}| = 1V$

I_{DP} ? , I_{DN} = ?

By observation:

PMOS: $V_{SGP} = 0V < |V_{tp}|$

$\Rightarrow$ PMOS OFF $\Rightarrow I_{DP} = 0$



NMOS: $V_{GSn} = 5V > V_{tn}$

$\Rightarrow$ NMOS ON

We don't region of operation.

Assume it is in Saturation:

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSn} - V_{tn})^2$$

$$= \frac{1}{2} \times 1m \times (5-1)^2 \Rightarrow I_D = 8mA$$

$\Rightarrow V_{out} = -I_{Dn} \times 1K = -8V \Rightarrow V_D = -8V$

$V_{G1} = 2.5V$

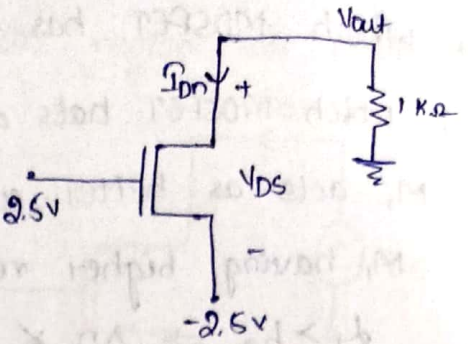
$V_D < V_{G1} - V_{tn}$

$\Rightarrow$ ~~Saturation~~ Triode region (Assumption is wrong)

$$\Rightarrow I_{Dn} = \mu_n C_{ox}\left(\frac{W}{L}\right)_n \left[(V_{GSn} - V_{tn})V_{DSn} - \frac{1}{2}V_{DSn}^2\right]$$

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$$I_{Dn} = 1mA\left[4V_{DSn} - \frac{1}{2}V_{DS}^2\right]$$



$$V_{DS} = V_{out} - (-2.5V)$$

$$V_{DS} = V_{out} + 2.5V$$

Now

$$I_{Dn} = 1mA\left[4(V_{out}+2.5V) + \frac{1}{2}(V_{out}+2.5V)^2\right]$$

$$\frac{-V_{out}}{1K\Omega} = 1mA\left[4(V_{out}+2.5V) + \frac{1}{2}(V_{out}+2.5V)^2\right]$$

$$-V_{out} = 4V_{out} + 10 + \frac{1}{2}V_{out}^2 + \frac{5}{2}V_{out} + 6.25$$

$\Rightarrow V_{out} = 6.972V, -1.972V$

↓ not possible since we assumed in triode region

↓ Crt answer.

Check.

$V_D = V_{out} = -1.972$

$V_G = 2.5$

$V_D < V_G - V_{tn}$

$\Rightarrow$ triode region.

$$\Rightarrow I_{Dn} = \frac{(-1.972V)}{1K\Omega} = -1.972\,mA$$

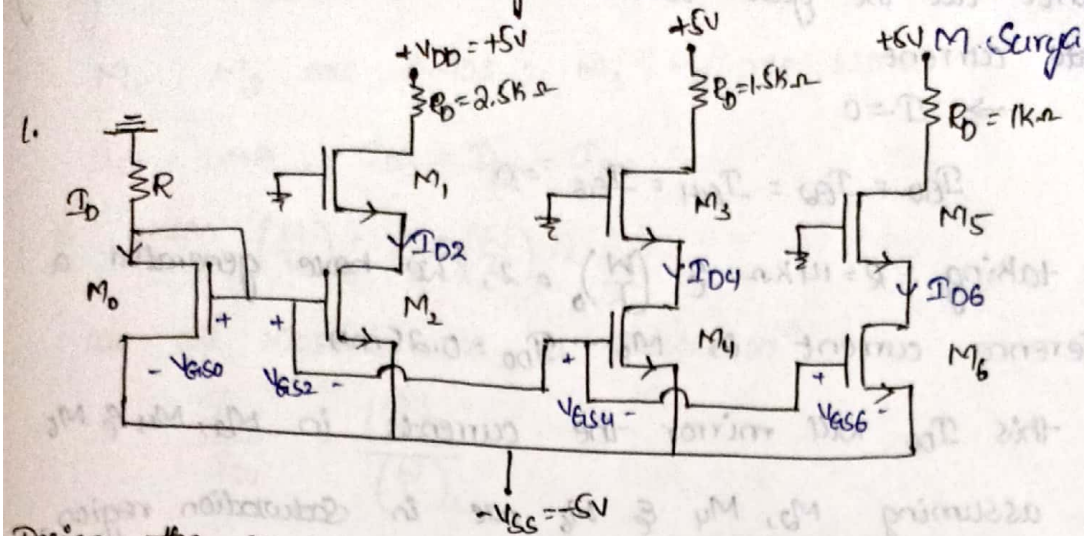
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Assignment

N180119

M. Surya kumari

1.



Design the current mirror ckt & find $\left(\frac{W}{L}\right)_2, \left(\frac{W}{L}\right)_4, \left(\frac{W}{L}\right)_6$ given $\mu_n C_{ox} = 1 mA/V^2$ is constant for all Mosfets, $V_t = 1V$ for all Mosfets.

Repeat the previous problem for $I_{D0} = 0.25 mA$, $I_{D2} = 0.75 mA$, $I_{D4} = 1.5 mA$, $I_{D6} = 2 mA$.

Sol:- By observation,

$$V_{GS0} = V_{GS2} = V_{GS4} = V_{GS6} \; ; \; V_{t0} = V_{t1} \cdots V_{t6} = 1V$$

Here I_{D0} has mirrored into M_2, M_4, M_6 as $0.75 mA$, & $1.5 mA$, $2 mA$.

Since M_0 is carrying $I_{D0} = 0.25 mA$ & $V_D = V_G$

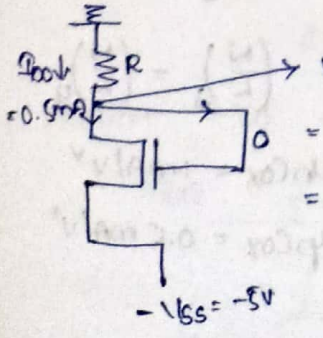
$\Rightarrow M_0$ is in saturation region.

Assume $\left(\frac{W}{L}\right)_0 = 2$

Now, $I_{D0} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_0 (V_{GS0} - V_{t0})^2$

$$V_{GS0} = \sqrt{\frac{2 I_{D0}}{\mu_n C_{ox} \left(\frac{W}{L}\right)_0}} + V_{t0} = \sqrt{\frac{2 \times 0.25m}{1m \times 2}} + 1V = 1.5V$$

$\therefore V_{GS0} = V_{GS2} = V_{GS4} = V_{GS6} = 1.5V$



Now, $I_{D0} = \frac{0V - (-3.5)}{R}$

$$R = \frac{3.5}{0.25m} = 14 K\Omega$$

$\boxed{R = 14 K\Omega}$

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⇒ Since all the gate terminals of Mosfets don't draw any gate current

⇒ $I_G = 0$

$$I_{G0} = I_{G2} = I_{G4} = I_{G6} = 0$$

⇒ By taking $R = 14k\Omega$ & $\left(\frac{W}{L}\right)_0 = 2$, we have generated a reference current in M_0 $I_{D0} = 0.25mA$

Now this I_{D0} will mirror the currents in M_2, M_4 & M_6

Now assuming M_2, M_4 & M_6 are in saturation region.

$$I_{D0} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_0 (V_{GS0} - V_{t0})^2$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{t2})^2$$

$$I_{D4} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_4 (V_{GS4} - V_{t4})^2$$

$$I_{D6} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_6 (V_{GS6} - V_{t6})^2$$

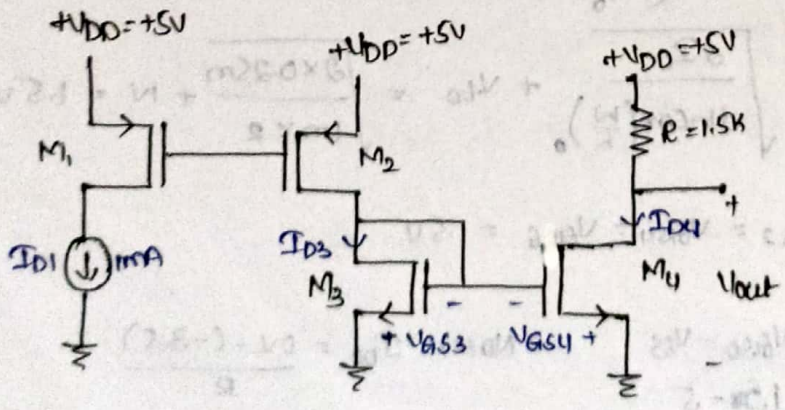
as V_{GS}, V_t is same for M_2, M_4, M_6 & M_0 these terms will be cancelled.

Now, $\frac{I_{D2}}{I_{D0}} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_0} \Rightarrow \frac{0.75m}{0.25m} = \frac{(W/L)_2}{2} \Rightarrow \left(\frac{W}{L}\right)_2 = 6$

$\frac{I_{D4}}{I_{D0}} = \frac{\left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_0} \Rightarrow \frac{1.5m}{0.25m} = \frac{(W/L)_4}{2} \Rightarrow \left(\frac{W}{L}\right)_4 = 12$

$\frac{I_{D6}}{I_{D0}} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_0} \Rightarrow \frac{2m}{0.25m} = \frac{(W/L)_6}{2} \Rightarrow \left(\frac{W}{L}\right)_6 = 16$

2.



All mosfets are in saturation region.

$\lambda = 0$

Given

$V_{tn} = 1V$, $V_{tp} = -1V$

$\left(\frac{W}{L}\right)_2 = 2 \times \left(\frac{W}{L}\right)_1$

$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4$

$\mu_n C_{ox} = 1mA/V^2$

$\mu_p C_{ox} = 0.5mA/V^2$

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By observation

M_1, M_2 are PMOS ; M_3, M_4 are NMOS.

$I_{D1} = 1mA$, $I_{D3} = I_{D2} = I_{D4}$

& given $\left(\frac{W}{L}\right)_2 = 2\left(\frac{W}{L}\right)_1$

& all Mos-fets are in saturation

$$\frac{I_{D2}}{I_{D1}} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}$$

$$I_{D2} = 2 \times 1mA \Rightarrow \boxed{I_{D2} = 2mA}$$

Here M_3 will mirror I_{D3} in M_4 as I_{D4}

$V_{GS3} = V_{GS4}$, $V_{th} = 1V$

$$\frac{I_{D4}}{I_{D3}} = \frac{\left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_3}$$

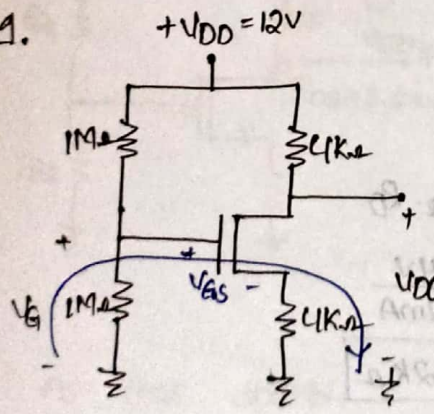
$\Rightarrow I_{D4} = I_{D3} = I_{D2} = 2mA$. & $I_{D1} = 1mA$.

27/1/22

Assignment

NIB0119
M. Surya kumari

1.



Find I_D for given $\mu_n C_{ox} = 1mA/V^2$

$\left(\frac{W}{L}\right)_n = 2V$, $V_{th} = 1V$.

$$V_G = \frac{R_{eq2}}{R_{eq2} + R_{eq2}} \times V_{DD} = \frac{1M}{1+1} \times 12 = 6V.$$

Now Apply KVL

$$-V_G + V_{GS} + I_{DQ} \cdot R_S = 0$$

$$6 + V_{GS} + I_{DQ} \cdot 4 = 0 \Rightarrow I_{DQ} = \frac{6 - V_{GS}}{4K\Omega} \rightarrow (1)$$

Assume MOS is in sat:

$$I_{DQ} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{GS} - V_{th})^2$$

$$= \frac{1}{2}(1m)(2)(V_{GS} - V_{th})^2 \Rightarrow I_{DQ} = (V_{GS} - V_{th})^2 1m \rightarrow (2)$$

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① = ②

$$\frac{6 - V_{GS}}{4K\Omega} = (1m)(V_{GS} - V_{tn})^2$$

$$6 - V_{GS} = 4(V_{GS}^2 + 1 - 2V_{GS})$$

$$4V_{GS}^2 - 8V_{GS} + 4 - 6 + V_{GS} = 0$$

$$4V_{GS}^2 - 7V_{GS} - 2 = 0$$

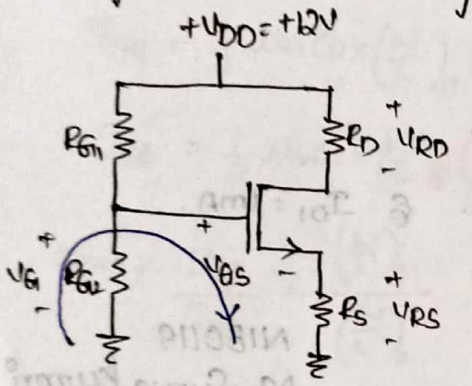
$$V_{GS} = 2V \quad , -\frac{1}{4} \text{ (not possible)}$$

$$\therefore V_{GS} = 2V$$

$$\Rightarrow I_{DQ} = \frac{6 - V_{GS}}{4K} = \frac{6-2}{4K} = 1mA$$

$$\Rightarrow \boxed{I_{DQ} = 1mA}$$

2. Repeat the above problem for having $I_{DQ} = 2mA$.



given $\mu_n C_{ox} = 1mA/V^2$

$V_{tn} = 1V$

$\left(\frac{W}{L}\right)_n = 2, \quad V_{DD} = 12V$

$I_{DQ} = 2mA$

As rule of thumb

$$V_{RS} = V_{RD} = \frac{V_{DD}}{3} = 4V$$

$$\Rightarrow V_{RS} = I_{DQ} \cdot R_S \qquad \Rightarrow V_{RD} = I_{DQ} \cdot R_D$$

$$\Rightarrow R_S = \frac{4V}{2mA} \qquad \Rightarrow R_D = \frac{4V}{2mA}$$

$$\boxed{R_S = 2K\Omega} \qquad \Rightarrow \boxed{R_D = 2K\Omega}$$

Apply KVL:

$$-V_G + V_{GSQ} + I_{DQ} R_S = 0$$

$$V_G = V_{GSQ} + 4V \rightarrow ①$$

$$V_G = \frac{R_{G2}}{R_{G1} + R_{G2}} V_{DD} \rightarrow ②$$

In sat :-

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS} - V_t)^2 \Rightarrow V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n}} + V_{tn}$$

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$$V_{GS} = \sqrt{\frac{2(2mA)}{1m \times 2}} + 1 = 2.414V \Rightarrow \boxed{V_{GS} = 2.414V}$$

$$\Rightarrow V_G = V_{GS} + 4 \Rightarrow V_G = 2.414V + 4 \Rightarrow \boxed{V_G = 6.414V}$$

Now, from (2)

$$V_G = \frac{R_{G2}}{R_{G1} + R_{G2}} \times 12$$

$$\frac{6.414}{12} = \frac{R_{G2}}{R_{G1} + R_{G2}}$$

$$R_{G1} + R_{G2} = \frac{R_{G2}}{0.5345}$$

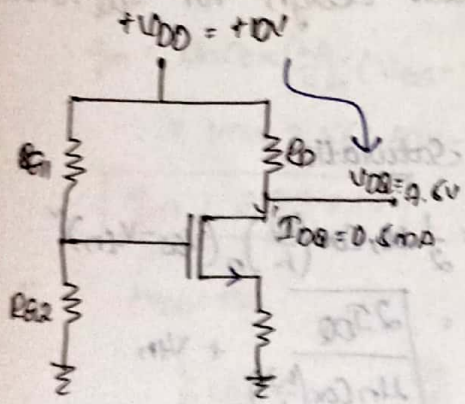
$$\Rightarrow 0.5345 R_{G1} + (0.5345 - 1) R_{G2} = 0$$

$$0.5345 R_{G1} = 0.4655 R_{G2}$$

$$R_{G1} = 0.8709 R_{G2}$$

Let $R_{G2} = 1M\Omega \Rightarrow R_{G1} = 0.8709M\Omega$

3. Design the voltage divider biasing ckt in order to establish $I_{DQ} = 0.5mA$ & $V_{DQ} = 7.5V$ given $\mu_n C_{ox} = 1mA/V^2$



$V_{tn} = 1V$, $\left(\frac{W}{L}\right)_n = 2$, $\lambda = 0$

Apply KVL,

$$-V_{DD} + I_{DQ} R_D + V_{DQ} = 0$$

$$R_D = \frac{V_{DD} - V_{DQ}}{I_{DQ}}$$

$$R_D = \frac{10 - 7.5}{0.5m} = 5K\Omega$$

$$\boxed{R_D = 5K\Omega}$$

As mos should be in sat :-

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{GS} - V_{tn})^2$$

$$V_{GS} = \sqrt{\frac{2 I_D}{\mu_n C_{ox} \left(\frac{W}{L}\right)_n}} + V_{tn} = \sqrt{\frac{2 \times 0.5m}{1m \times 2}} + 1 = 1.707V$$

let us assume $V_{DS} = 3V$ (∵ MOS is in saturation region)

$V_{DS} > V_{GS} - V_{tn}$

$$V_{DQ} = V_{DS} + V_{RS}$$

$$V_{DQ} = 3 + I_{DQ} \cdot R_S$$

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$$R_S = \frac{V_{DQ} - 3}{I_{DQ}} = \frac{7.5 - 3}{0.5m} = 9k\Omega$$

$$\boxed{R_S = 9k\Omega}$$

NOW, $V_G = \frac{R_{G2}}{R_{G1} + R_{G2}} V_{DD}$; Apply KVL,

$$-V_G + V_{GS} + I_{DQ} R_S = 0$$

$$V_G = V_{GS} + (0.5m)(9k)$$

$$V_G = 1.707 + 4.5 = 6.207$$

$$\frac{6.207}{10} = \frac{R_{G2}}{R_{G1} + R_{G2}}$$

$$0.6207 = \frac{R_{G2}}{R_{G1} + R_{G2}}$$

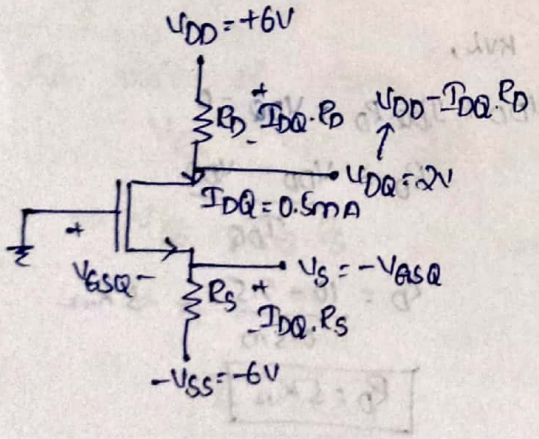
$$0.6207 R_{G1} + (0.6207 - 1) R_{G2} = 0$$

$$R_{G1} = \frac{0.3793}{0.6207} R_{G2}$$

$$\therefore R_{G1} = 0.61108 R_{G2}$$

$\Rightarrow$ if $R_{G2} = 1M\Omega \Rightarrow R_{G1} = 0.61108 M\Omega$

4. Repeat dual supply biasing circuit design for $I_{DQ} = 0.5mA$ & $V_{DQ} = 2V$



In Saturation:

$$I_{DQ} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{GS} - V_{tn})^2$$

$$V_{GSQ} = \sqrt{\frac{2 I_{DQ}}{\mu_n C_{ox} \left(\frac{W}{L}\right)_n}} + V_{tn}$$

$$= \sqrt{\frac{2 \times 0.5m}{1m \times 2}} + 1V$$

$$V_{GSQ} = 0.707 + 1 = 1.707V$$

Now apply KVL

$$+V_{GSQ} + I_{DQ} \cdot R_S - V_{SS} = 0$$

$$R_S = \frac{V_{SS} - V_{GS}}{I_D} = \frac{6 - 1.707}{0.5} = 8.586k\Omega$$

$$\boxed{R_S = 8.586k\Omega}$$

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apply KVL,

$$V_{DQ} = V_{DD} - I_{DQ} R_D$$

$$R_D = \frac{V_{DD} - V_{DQ}}{I_{DQ}} = \frac{6-2}{0.5m} = 8K\Omega$$

$\therefore R_S = 8.586\ K\Omega$, $R_D = 8\ K\Omega$

NIB0119

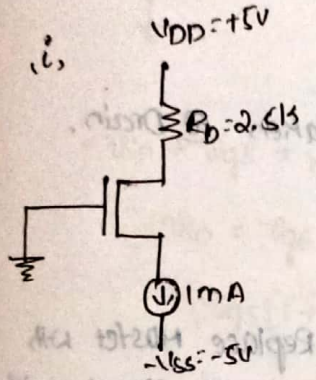
31/1/22

Assignment

NIB0119
M. Surya kumari

Q. Find transconductance g_m. Given, $\mu_n C_{ox} = 1mA/V^2$

i,



By observation,

$I_D = 1mA$

Mosfet is in saturation

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS} - V_{tn})^2$$

$$\Rightarrow V_{GS} = V_{tn} + \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n}} = 1V + 0.894 = 1.894V$$

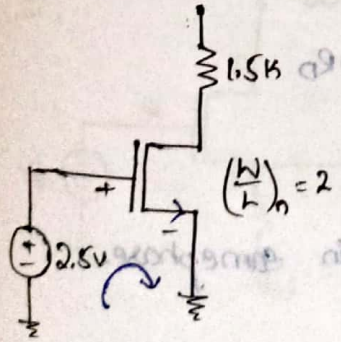
$V_{GS} = 1.894\ V$

$$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS} - V_{tn})$$

$$= 1m \times 2.5(1.894 - 1) = 2.23\ A/V$$

$$\boxed{g_m = 2.23\ A/V}$$

ii,



By Applying KVL,

$$-2.5 + V_{GSQ} = 0$$

$$V_{GSQ} = 2.5V$$

$$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS} - V_{tn})$$

$$= 1m \times 2\ (2.5 - 1)$$

$$g_m = 3\ mA/V$$

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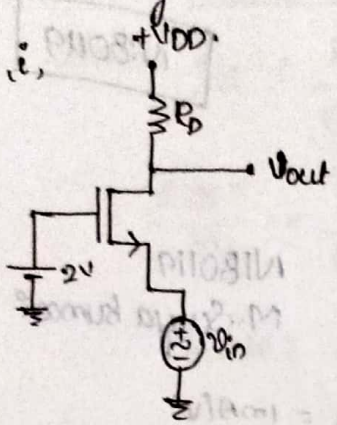
4/2/22

Assignment

N180119
M. Surya Kumari.

Find the small signal voltage gain, capacitance for the following ckts shown below using small signal model ($\lambda = 0$)

i)



For i) find small signal voltage gain,

apply signal model

1. Short circuit DC sources.
2. Replace Mosfet with its small signal model
3. Do the analysis.

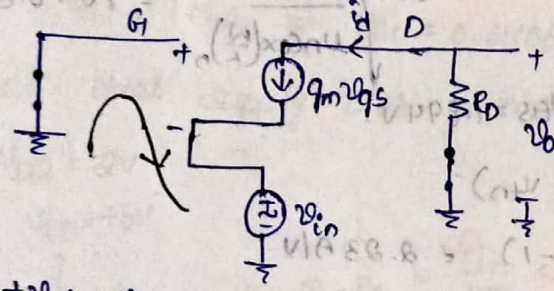
By observation:

i/p v_{in} applied @ source ; o/p v_{out} taken @ Drain.

Apply AC analysis, & small signal model

1. 2V (dc) & V_{DD}(dc) are short circuited.

2) Replace Mosfet with small signal model.



$+v_{gs} + v_{in} = 0$

$$\boxed{v_{gs} = -v_{in}}$$

$v_{out} = -i_d R_D$ [$i_d = g_m v_{gs}$

$= -g_m v_{gs} R_D$

$v_{out} = -g_m(-v_{in}) R_D$

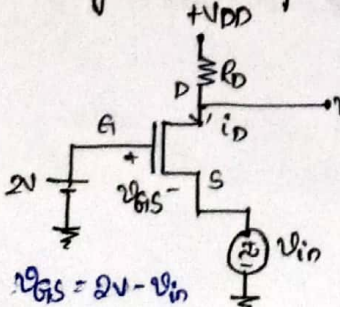
$$\boxed{A_v = \frac{v_{out}}{v_{in}} = +g_m R_D}$$

'+' refers here both i/p & o/p are in samephase.

'0°' phase.

Why same phase here?

Qualitative Analysis



(inst)

$v_{OUT} = V_{DD} - i_D R_D$

$v_{GS} = 2V - v_{in}$

$v_{in} \uparrow \Rightarrow v_{GS} \downarrow \Rightarrow i_D \downarrow$

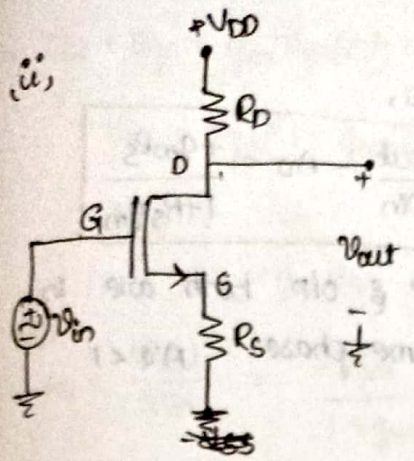
$\Downarrow$

$v_{out} \uparrow \Leftarrow i_D R_D \downarrow$

$\Rightarrow v_{in} \uparrow \Rightarrow v_{out} \uparrow \Rightarrow$ Samephase.

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(ii)



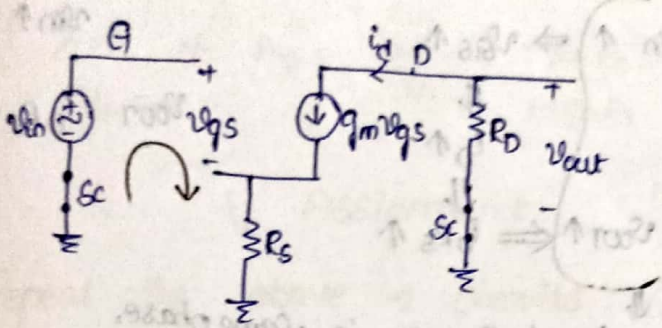
By observation:

i/p : v_{in} ⇒ Gate ; o/p : v_{out} ⇒ Drain

Apply Small Signal Model of AC analysis

1) V_{GSQ} & V_{DD} ⇒ S.C (D.C)

2) Replace Mosfet with Small Signal model



3) Do the Analysis.

$A_v = \frac{v_{out}}{v_{in}}$

$v_{out} = -i_d R_D$

$v_{out} = -g_m v_{gs} R_D$

$-v_{in} + v_{gs} + i_d R_S = 0$

$v_{in} = v_{gs} + g_m v_{gs} R_S$

$v_{gs}[1 + g_m R_S] = v_{in}$

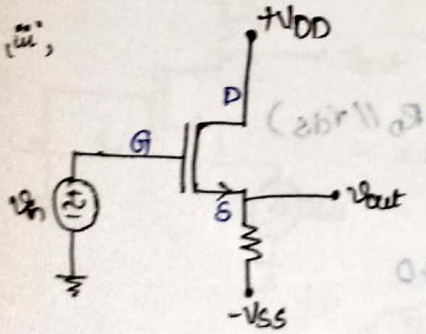
$v_{gs} = \frac{v_{in}}{1 + g_m R_S}$

Now, $v_{out} = -g_m \frac{v_{in}}{1+g_m R_S} R_D$

$$\frac{v_{out}}{v_{in}} = A_v = \frac{-g_m R_D}{1 + g_m R_S}$$

* Here Small Signal voltage gain decreases because of the presence of negative feedback provided by R_S. and -ve sign tells us i/p & o/p are 180° out of phase.

(iii)



Here $-V_{SS}$ gives Q. point.

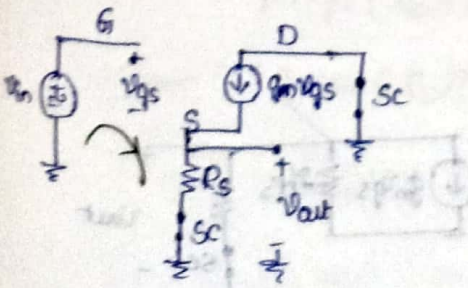
By observation:

i/p : v_{in} ⇒ G ; o/p : v_{out} ⇒ S

Apply AC analysis:

1. SC the $-V_{SS}$ & V_{DD}
2. Replace Mosfet with its small signal model
3. Do the Analysis.

$A_v = \frac{v_{out}}{v_{in}}$



$v_{out} = i_d R_S$

$v_{out} = g_m v_{gs} R_S$

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$$-v_{in} + v_{gs} + i_d R_s = 0$$

$$-v_{in} + v_{gs} + g_m v_{gs} R_s = 0$$

$$v_{gs}[1 + g_m R_s] = v_{in}$$

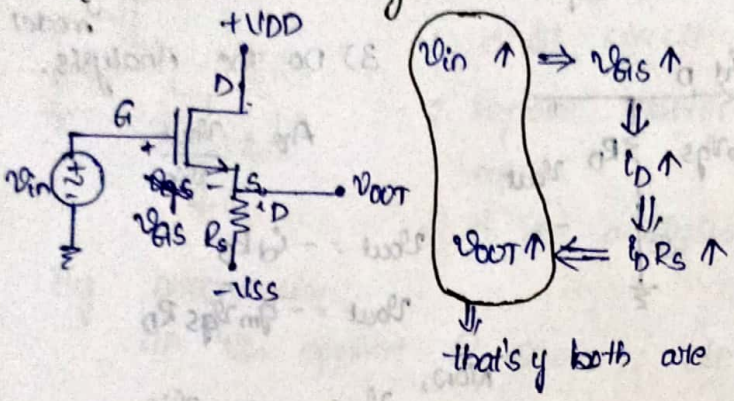
$$v_{gs} = \frac{v_{in}}{1 + g_m R_s}$$

Now,

$$\boxed{\frac{v_{out}}{v_{in}} = A_v = \frac{+g_m R_s}{1 + R_s g_m}}$$

i/p & o/p both are in same phase. $A_v < 1$

Qualitative Analysis



$v_{in} \uparrow \Rightarrow v_{GS} \uparrow \Downarrow i_D \uparrow \Downarrow i_D R_s \uparrow \Rightarrow v_{out} \uparrow$

that's y both are in same phase.

$v_{in} \uparrow \Rightarrow v_{gs} \uparrow$

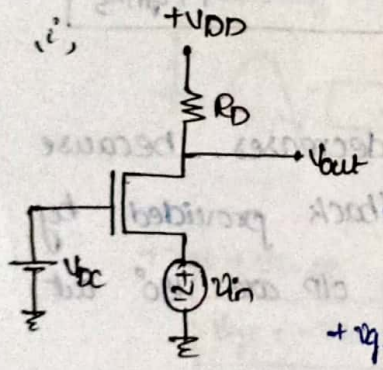
$v_{OUT} = i_D R_s - V_{SS}$

Assignment

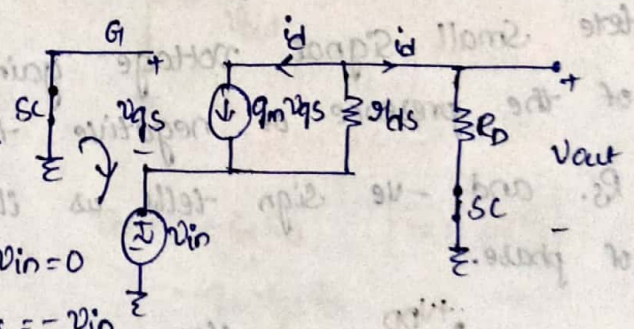
N180119
M. Surya kumari.

1. Find A_v for $\lambda \neq 0$

(i)



i/p @ source ; o/p @ drain



$+v_{gs} + v_{in} = 0$

$v_{gs} = -v_{in}$

Now,

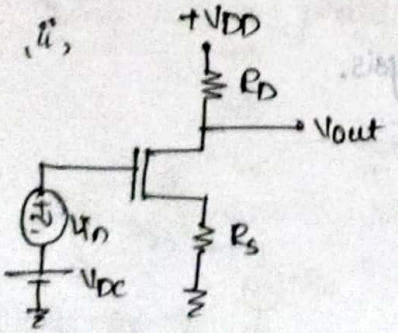
$$v_{out} = -i_d (R_D // r_{ds}) = -g_m v_{gs} (R_D // r_{ds})$$

$$v_{out} = g_m v_{in} (R_D // r_{ds})$$

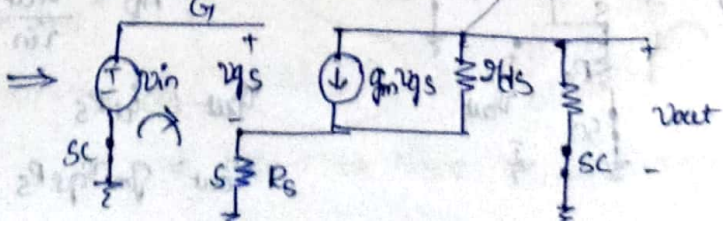
$$A_v = \frac{v_{out}}{v_{in}} = g_m (R_D // r_{ds}) \quad \lambda \neq 0$$

if $\lambda = 0 \Rightarrow r_{ds} = \infty \Rightarrow A_v = g_m R_D$

(ii)



i/p @ gate
o/p @ drain



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$-v_{in} + v_{gs} + g_m v_{gs}(R_S) = 0$

$v_{in} = v_{gs}(1 + g_m R_S)$

$v_{gs} = \frac{v_{in}}{1+g_m R_S}$

$v_{out} = -i_d (R_D // r_{ds})$

$= -g_m v_{gs} (R_D // r_{ds})$

$v_{out} = -g_m \cdot \frac{v_{in}}{1+g_m R_S} (R_D // r_{ds})$

NOW,

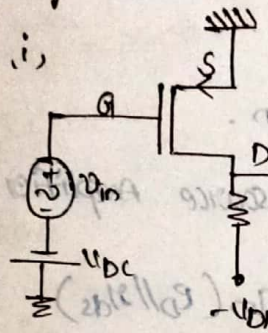
$A_V = \frac{v_{out}}{v_{in}} = \frac{-g_m}{1+g_m R_S} (R_D // r_{ds}) \quad \lambda \neq 0$

if $\lambda = 0 \Rightarrow r_{ds} = \infty$ $\quad A_V = \frac{v_{out}}{v_{in}} = \frac{-g_m R_D}{1+g_m R_S}$

Assignment N180119

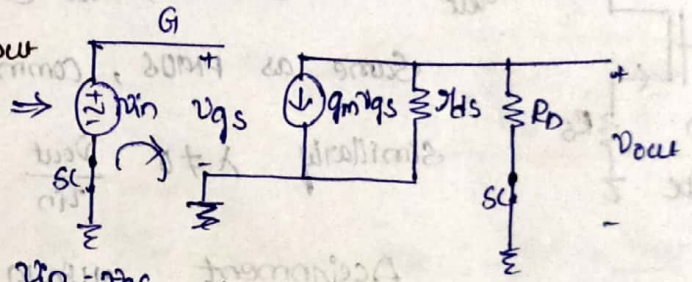
1. Repeat the above 4 circuits for finding A_V ($\lambda \neq 0$)

(i)



v_{in} @ gate ; v_{out} @ drain

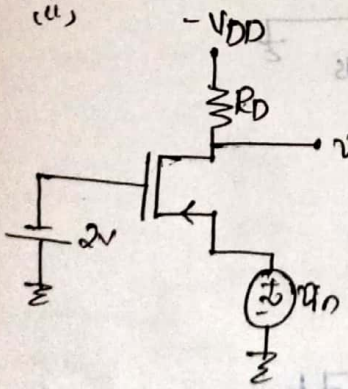
$\Rightarrow$ Common source, PMOS



$v_{in} = v_{gs}$; $v_{out} = -g_m v_{gs}(R_D // r_{ds})$

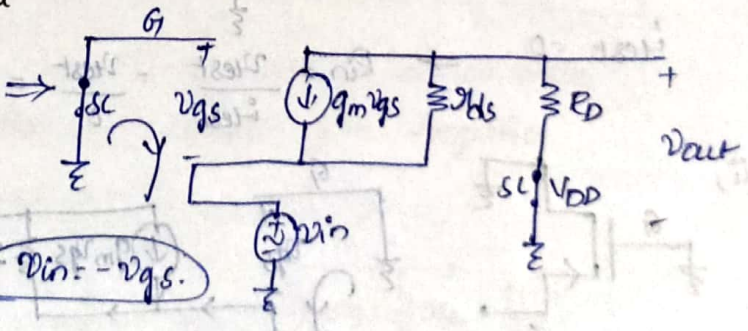
$A_V = \frac{v_{out}}{v_{in}} = -g_m (R_D // r_{ds})$

(ii)



NO (-ve) feedback

v_{in} @ source, v_{out} @ drain



$v_{in} = -v_{gs}$.

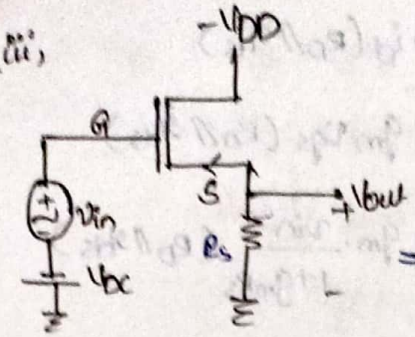
$v_{out} = -g_m v_{gs} (R_D // r_{ds})$

$v_{out} = +g_m v_{in} (R_D // r_{ds})$

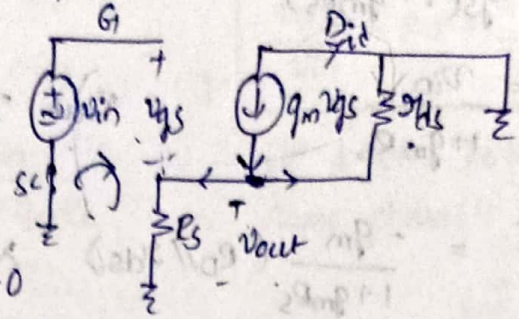
$\Rightarrow A_V = \frac{v_{out}}{v_{in}} = g_m (R_D // r_{ds})$

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(iii)



-ve feedback given by Rs.
Vin @ Gate ; Vout @ Source.



$-V_{in} + V_{gs} + R_s(g_m V_{gs}) = 0$

$V_{in} = V_{gs}(1 + g_m R_s)$

$V_{gs} = \frac{V_{in}}{1 + g_m R_s}$

$V_{out} = g_m V_{gs}(R_s + r_{ds})$

$V_{out} = g_m \cdot \frac{V_{in}}{1 + g_m R_s}(r_{ds} + R_s)$

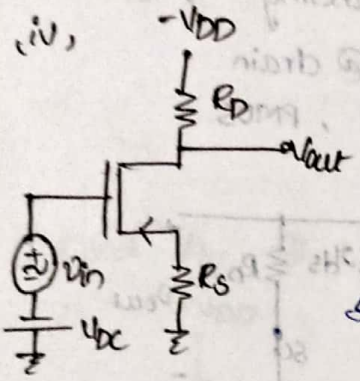
$A_V = \frac{V_{out}}{V_{in}} = \frac{g_m(r_{ds} + R_s)}{1 + g_m R_s}$

$-V_{out} - g_m V_{gs} r_{ds} = 0$

$-g_m V_{gs} r_{ds} + V_{out} = 0$

$V_{out} = g_m \cdot \frac{V_{in}}{1 + g_m R_s} r_{ds}$

(iv)



-ve feedback given by Rs
Vin @ Gate, Vout @ drain.

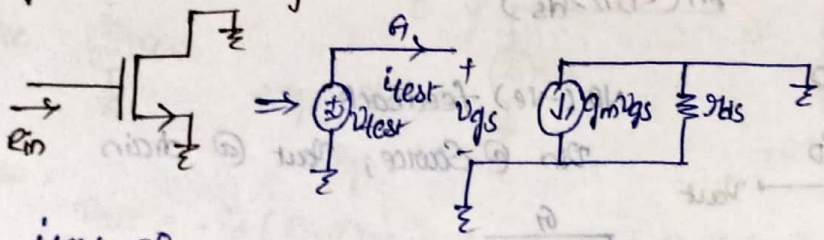
Same as PMOS, common source Amplifier

Similarly $\lambda \neq 0$ $\frac{V_{out}}{V_{in}} = -g_m(R_D // r_{ds}) + \frac{g_m r_{ds}}{1 + g_m R_s}$

Assignment N180119

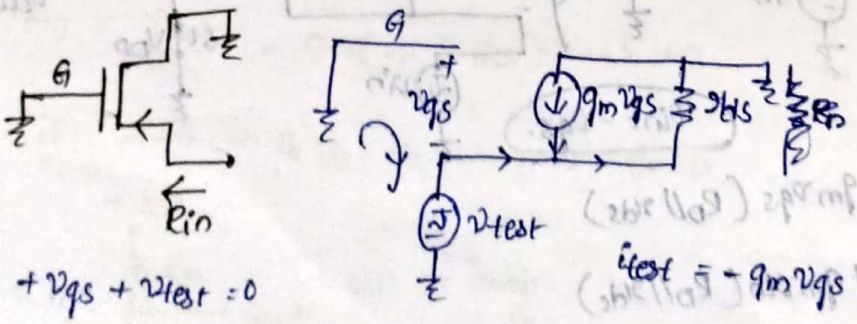
Q. Repeat above problems for $\lambda \neq 0$ find Rin & Rout.

(i)



$i_{test} = 0 \Rightarrow R_{in} = \frac{V_{test}}{i_{test}} = \frac{V_{test}}{0} = \infty$

(ii)



$+V_{gs} + V_{test} = 0$

$V_{test} = -V_{gs}$

$\Rightarrow R_{in} = \frac{V_{test}}{i_{test}} = g_m + \frac{1}{r_{ds}}$

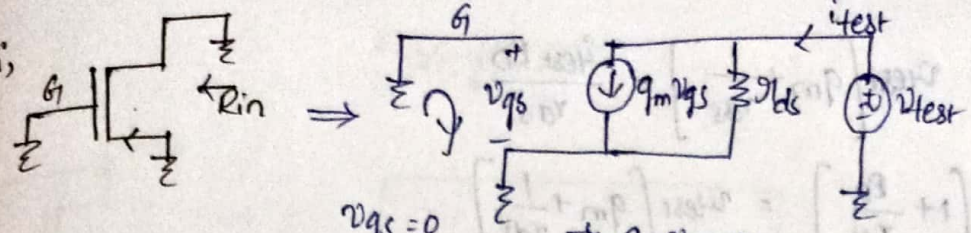
$i_{test} = -g_m V_{gs} + \frac{V_{test} - 0}{r_{ds}}$

$i_{test} = g_m V_{test} + \frac{V_{test}}{r_{ds}}$

$i_{test} = V_{test}\left[g_m + \frac{1}{r_{ds}}\right]$

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(ii)



$v_{gs} = 0 \Rightarrow g_m v_{gs} = 0$

$\Rightarrow \frac{v_{test}}{i_{test}} = R_{in} = r_{ds}$

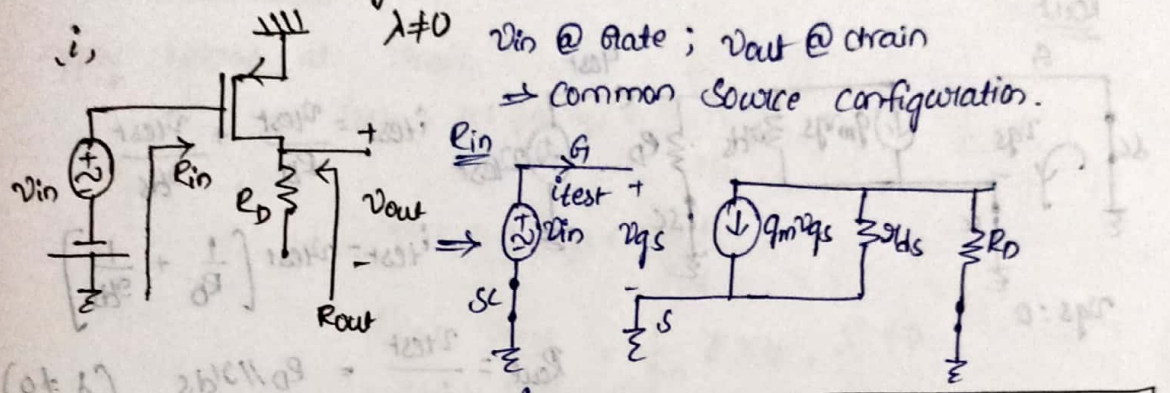
N180119

Assignment on 4-2-21

Q. Find Small Signal i/p & o/p resistances R_{in} & R_{out}.

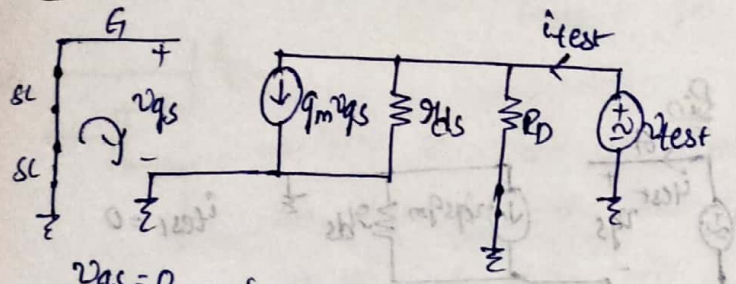
(i) $\lambda \neq 0$ v_{in} @ Gate ; v_{out} @ drain

$\Rightarrow$ common source configuration.



$i_{test} = 0 \Rightarrow R_{in} = \frac{v_{test}}{i_{test}} = \frac{v_{test}}{0} = \infty$

Rout



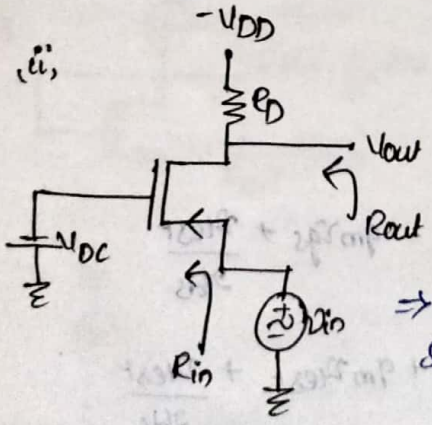
$v_{gs} = 0 \Rightarrow g_m v_{gs} = 0$

$i_{test} = \frac{v_{test}}{R_D} + \frac{v_{test}}{r_{ds}}$

$i_{test} = v_{test}\left[\frac{1}{R_D} + \frac{1}{r_{ds}}\right]$

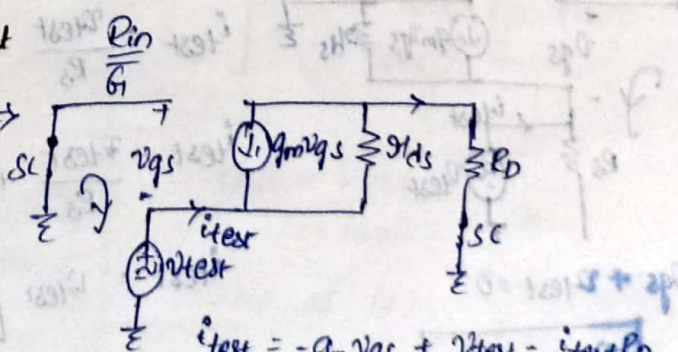
$$R_{out} = \frac{v_{test}}{i_{test}} = \frac{R_D r_{ds}}{R_D + r_{ds}}$$

(ii)



v_{in} @ Source , v_{out} @ drain

$\Rightarrow$ Common gate Amplifier



$+v_{gs} + v_{test} = 0$

$v_{gs} = -v_{test}$

$$i_{test} = -g_m v_{gs} + \frac{v_{test} - i_{test} R_D}{r_{ds}}$$

$$i_{test} = g_m v_{test} + \frac{v_{test} - i_{test} R_D}{r_{ds}}$$

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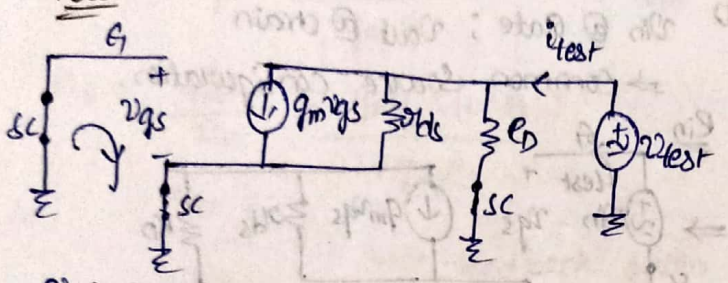
$$i_{test} = v_{test}\left[g_m + \frac{1}{r_{ds}}\right] - \frac{i_{test} R_D}{r_{ds}}$$

$$i_{test}\left[1 + \frac{R_D}{r_{ds}}\right] = v_{test}\left[g_m + \frac{1}{r_{ds}}\right]$$

$$\frac{v_{test}}{i_{test}} = R_{in} = \frac{1 + \frac{R_D}{r_{ds}}}{g_m + \frac{1}{r_{ds}}} = \frac{r_{ds} + R_D}{g_m r_{ds} + 1} \Rightarrow (\lambda \neq 0)$$

$$\lambda = 0 \Rightarrow r_{ds} = \infty \Rightarrow R_{in} = \frac{1}{g_m}$$

R_{out}



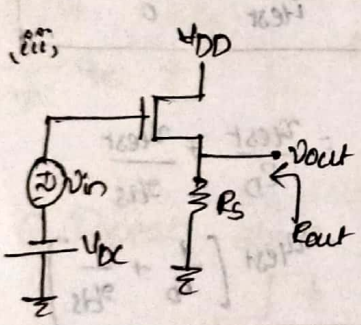
$$i_{test} = \frac{v_{test}}{R_D} + \frac{v_{test}}{r_{ds}}$$

$$i_{test} = v_{test}\left[\frac{1}{R_D} + \frac{1}{r_{ds}}\right]$$

$$R_{out} = \frac{v_{test}}{i_{test}} = R_D // r_{ds} \quad (\lambda \neq 0)$$

if $\lambda = 0 \Rightarrow R_{out} = R_D$

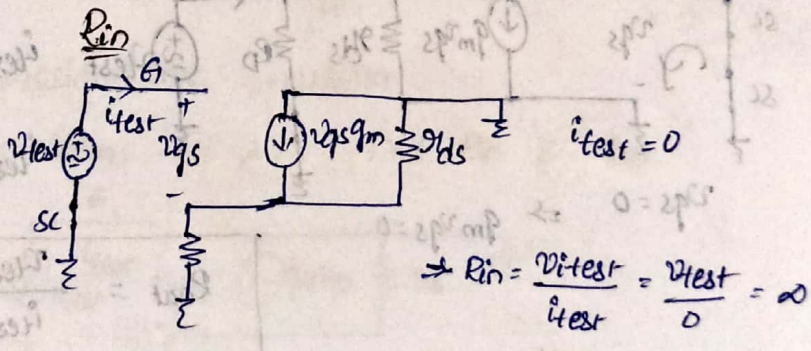
(iii)



v_{in} @ gate;
v_{out} @ source

$\Rightarrow$ Common Drain Amplifier.

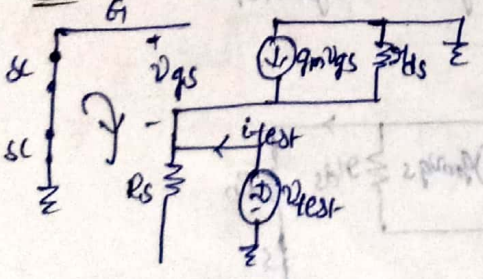
R_{in}



$$\Rightarrow R_{in} = \frac{v_{itest}}{i_{test}} = \frac{v_{test}}{0} = \infty$$

$$\boxed{R_{in} = \infty}$$

R_{out}



$$i_{test} = \frac{v_{test}}{R_S} - g_m v_{gs} + \frac{v_{test}}{r_{ds}}$$

$$i_{test} = \frac{v_{test}}{R_S} + g_m v_{test} + \frac{v_{test}}{r_{ds}}$$

$$i_{test} = v_{test}\left[\frac{1}{R_S} + g_m + \frac{1}{r_{ds}}\right]$$

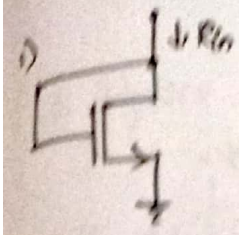
$$+ v_{gs} + v_{test} = 0$$

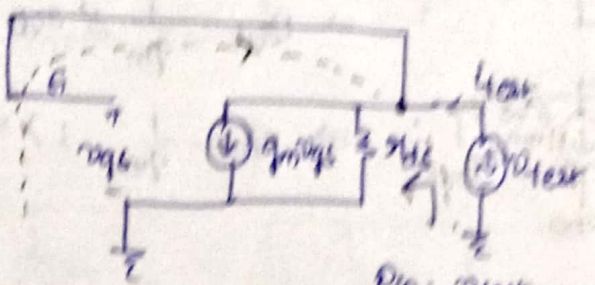
$$\boxed{v_{test} = -v_{gs}}$$

$$R_{out} = \frac{v_{test}}{i_{test}} = R_S // 1/g_m // r_{ds}$$

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Assignment

1) 



By observation:

$-v_{gs} + v_{test} = 0$

$\boxed{v_{gs} = v_{test}}$

$R_{in} = \frac{v_{test}}{i_{test}}$

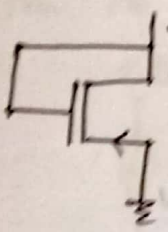
Apply Nodal at drain

$$i_{test} = 0 + g_m v_{gs} + \frac{v_{test} - 0}{r_{ds}}$$

$$i_{test} = g_m v_{gs} + \frac{v_{test}}{r_{ds}}$$

$$R_{in} = \frac{v_{test}}{i_{test}} = \frac{1}{g_m} \,//\, r_{ds}, \quad \lambda \neq 0$$

$$R_{in} = \frac{v_{test}}{i_{test}} = \frac{1}{g_m}, \quad \lambda = 0.$$ (R_{in} is less bcz diode corrected load

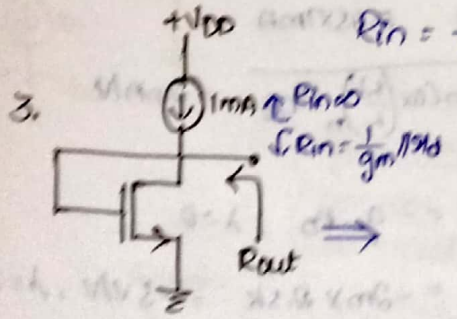
2. 

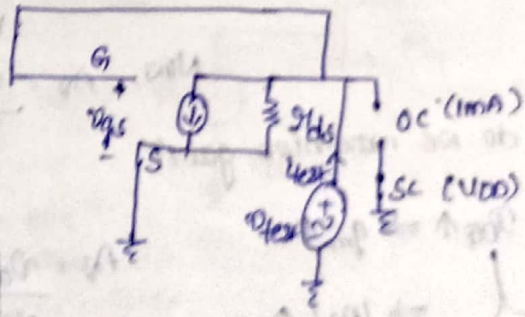
⇒ This is same as above

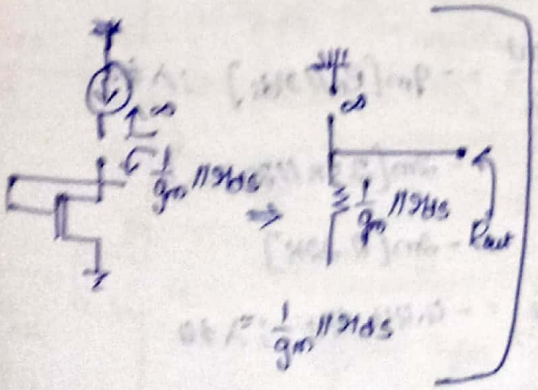
⇒ diode connected load using PMOS

⇒ $R_{in} = \frac{1}{g_m} \,//\, r_{ds}$ for $\lambda \neq 0$

$R_{in} = \frac{1}{g_m}$ for $\lambda = 0$

3. 





$R_{out} = \frac{v_{test}}{i_{test}}$

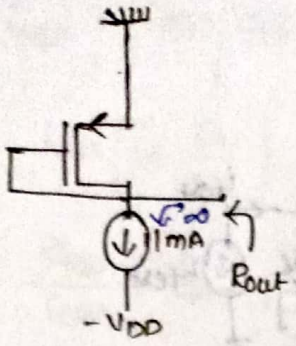
Same as (1)

⇒ $R_{out} = \frac{1}{g_m} \,//\, r_{ds}$; $\lambda \neq 0$

$R_{out} = \frac{1}{g_m}$; $\lambda = 0$

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(4)

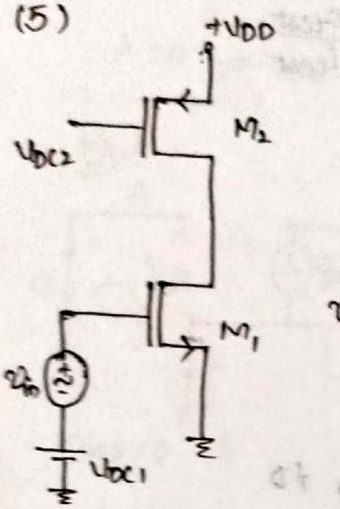


⇒ Same as (3) this using PMOS.

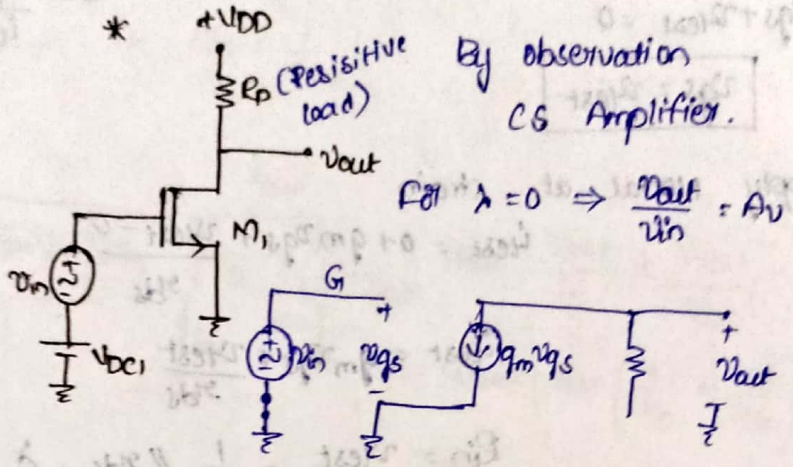
⇒ $R_{out} = \frac{1}{g_m} // r_{ds}$; $\lambda \neq 0$

⇒ $R_{out} = \frac{1}{g_m}$; $\lambda = 0$

(5)



*



By observation CG Amplifier.

For $\lambda = 0 \Rightarrow \frac{v_{out}}{v_{in}} = A_v$

$\Rightarrow A_v = -g_m R_D$; $\lambda = 0$

$A_v = -g_m[R_D // r_{ds}]$; $\lambda \neq 0$

* V_{DD} : 5V

R_D : 2.5 kΩ

$\mu_n C_{ox}$: 1mA/V²

V_{tn} = 1V

V_{DC1} = 2V, $\left(\frac{W}{L}\right)_n = 2$

$\lambda = 0.5 V^{-1}$

DC Analysis ⇒ Q. Point

from Earlier analysis,

I_{DQ} = 1mA & V_{DQ} = 2.5V

$r_{ds} = \frac{1}{\lambda I_{DQ}} = \frac{1}{0.05 \times 1mA} = 20 k\Omega$

$g_m = \sqrt{2 \mu_n C_{ox} \left(\frac{W}{L}\right)_n I_{DQ}} = 2mA/V$

Now, $A_v = \frac{v_{out}}{v_{in}} = -g_m R_D$; $\lambda = 0$

$A_v = -2m \times 2.5K = -5 V/V$, $\lambda = 0$

$A_v = \frac{v_{out}}{v_{in}} = -g_m[R_D // r_{ds}]$; $\lambda \neq 0$

$= -2m[2.5K // 20 K\Omega]$

$= -2m[2.22K]$

$A_v = -4.44 V/V$; $\lambda \neq 0$

*How do we maximize gain?

Sol: If $I_{DQ} \uparrow \Rightarrow g_m \uparrow$

$\Rightarrow |A_v| \uparrow$

power dissipation ↑ $= V_{DD} \cdot I_{DQ}$

$I_{DQ} \cdot R_D \uparrow$

$\Rightarrow V_{DQ} \downarrow$

$\Rightarrow$ voltage swing ↓

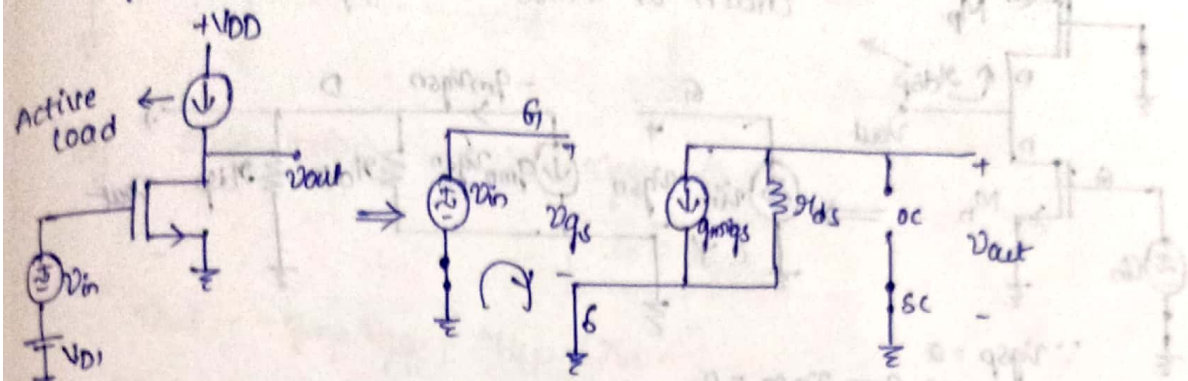
Drawbacks

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2. If $R_D \uparrow \Rightarrow I_{DQ} R_D \uparrow \rightarrow V_{DQ} \downarrow$ $(V_{DD} - I_{DQ} R_D)$

$\Rightarrow$ voltage swings $\downarrow$ (drawback)

3. Replace R_D with current source.



$-V_{in} + V_{gs} = 0$

$V_{in} = V_{gs}$

$V_{out} = -g_m V_{gs} r_{ds}$

$\frac{V_{out}}{V_{in}} = A_V = -g_m r_{ds}$

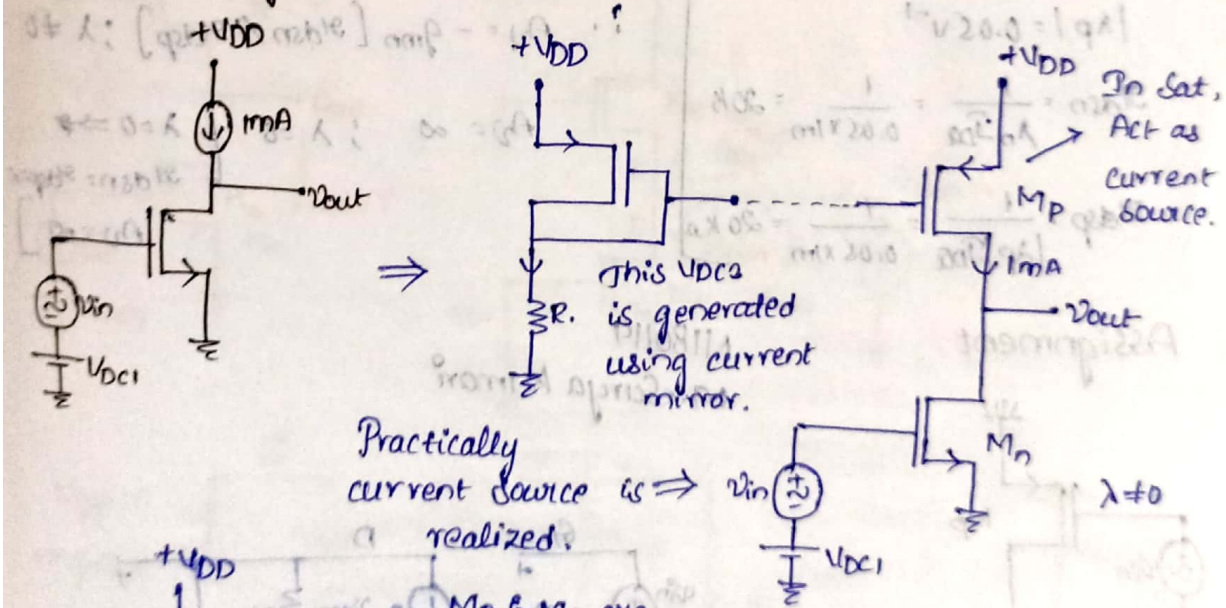
$= -2m \times 20K$

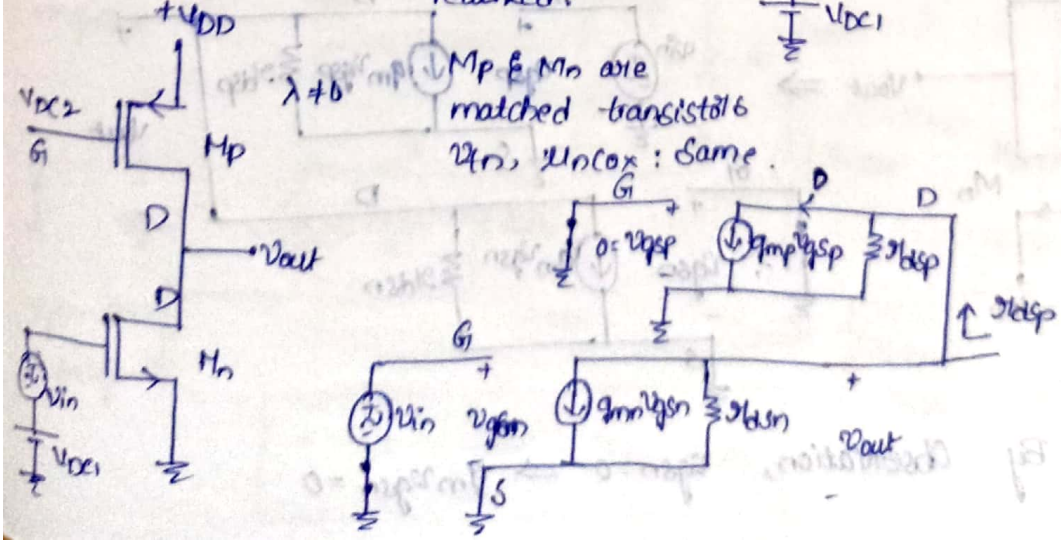
$A_V = -40 V/V$

Maximum achievable Gain "Intrinsic Gain."

$\Rightarrow$ Intrinsic gain is achieved by using Active Load.

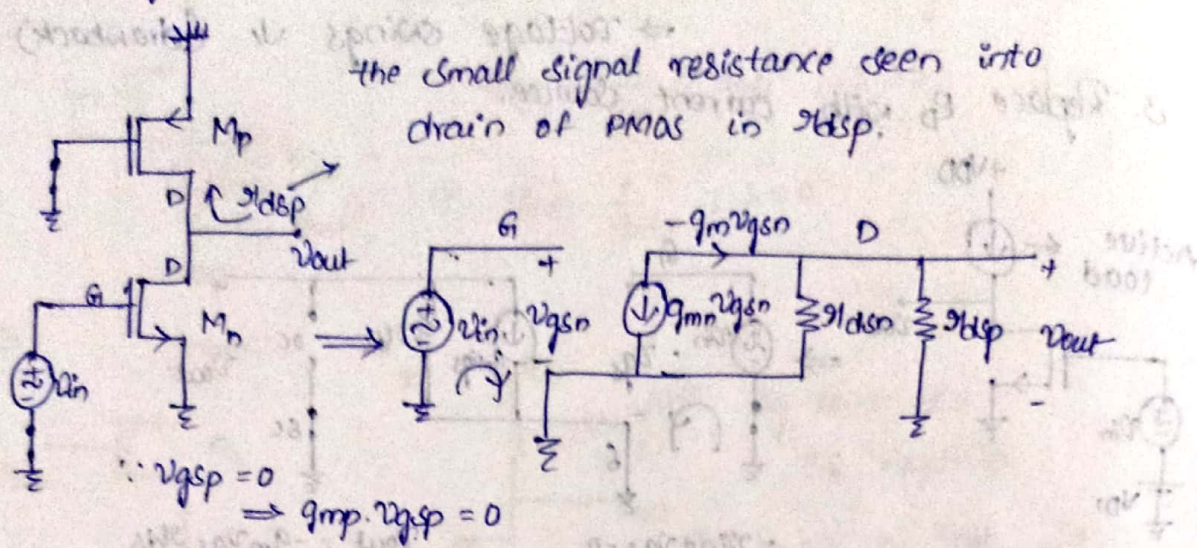
* How do you realize current source?





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finding A_v Apply AC analysis.



the small signal resistance seen into drain of PMOS is r_{dsp}.

$\because v_{gsp} = 0$

$\Rightarrow g_{mp} \cdot v_{gsp} = 0$

$v_{in} = v_{gsn}$

$v_{out} = -g_{mn} v_{gsn} [r_{dsn} // r_{dsp}]$

$\frac{v_{out}}{v_{in}} = A_v = -g_{mn} [r_{dsn} // r_{dsp}]$

$= -2m [20k // 20k] = -2m (10k)$

$\boxed{A_v = -20 \text{ V/V}}$

$\lambda_n = 0.05 V^{-1}$

$|\lambda_p| = 0.05 V^{-1}$

$r_{dsn} = \frac{1}{\lambda_n I_{DQ}} = \frac{1}{0.05 \times 1m} = 20k$

$r_{dsp} = \frac{1}{|\lambda_p| I_{DQ}} = \frac{1}{0.05 \times 1m} = 20k\Omega$

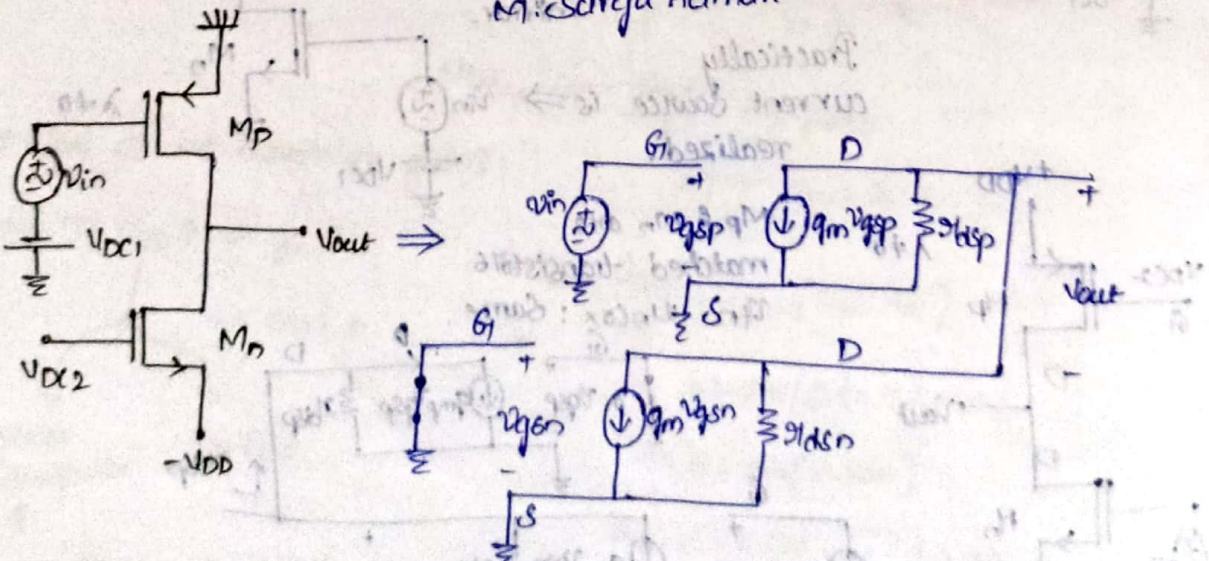
$\therefore A_v = -g_{mn} [r_{dsn} // r_{dsp}] ; \lambda \neq 0$

$\therefore A_v = \infty ; \lambda = 0$ [$\lambda = 0 \Rightarrow r_{dsn} = r_{dsp} = \infty$, $A_v = \infty$]

Assignment

N180119

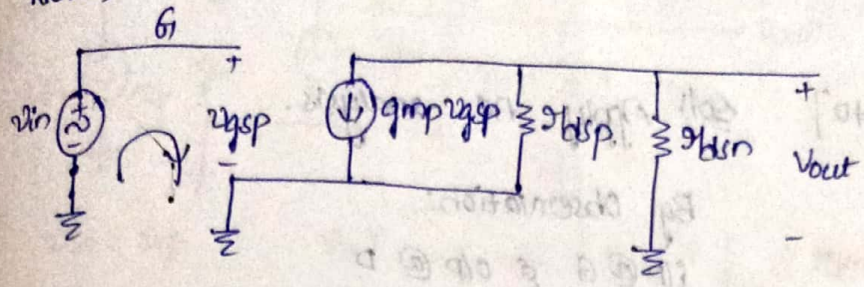
M. Surya Kumari



By Observation, $v_{gsn} = 0 \Rightarrow g_m v_{gsn} = 0$

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Now,



By observation, $-v_{in} + v_{gsp} = 0$

$$\boxed{v_{in} = v_{gsp}}$$

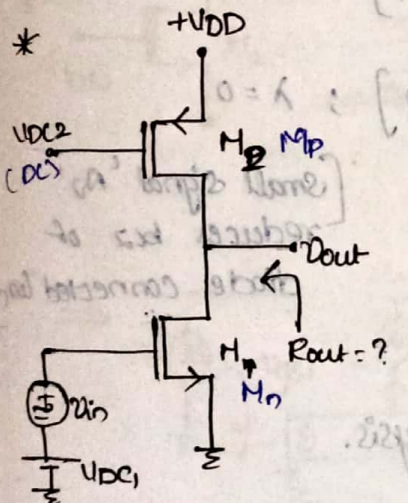
$$v_{out} = -g_{mp} v_{gsp} [r_{dsp} // r_{dsn}]$$

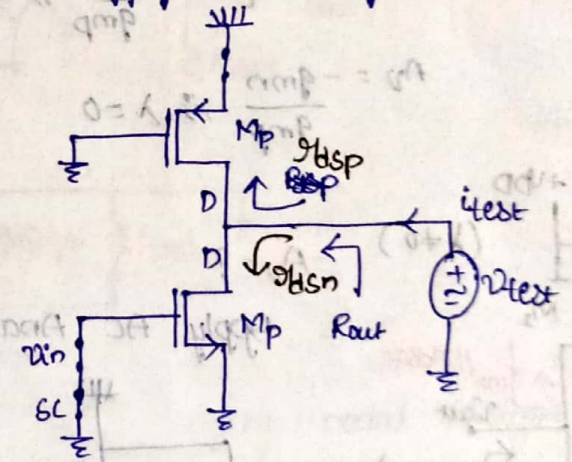
$$= -g_{mp} v_{in} [r_{dsp} // r_{dsn}]$$

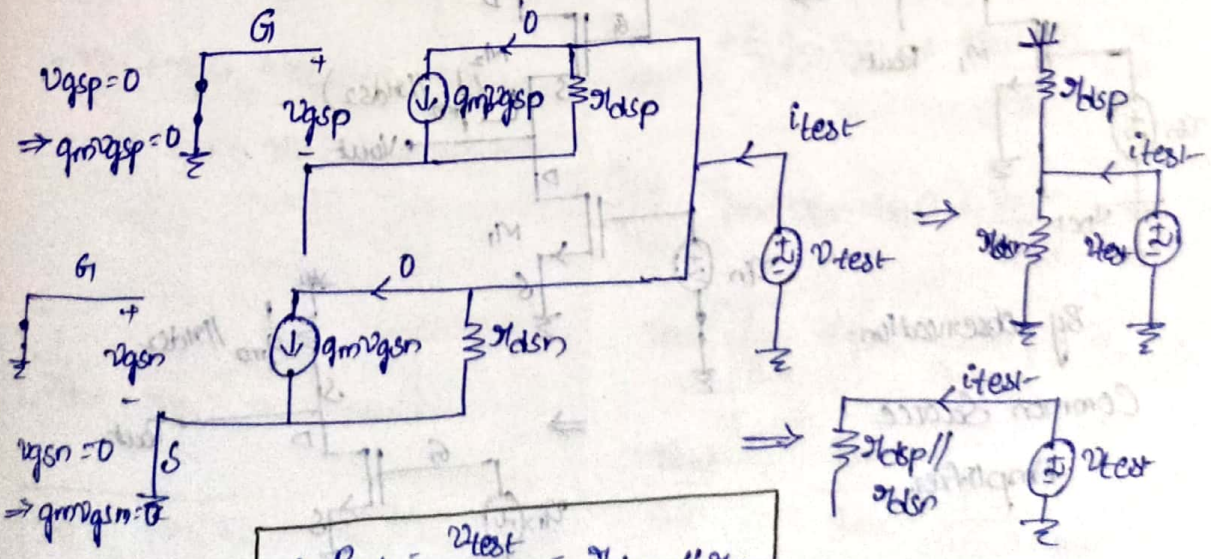
$$\boxed{A_v = \frac{v_{out}}{v_{in}} = -g_{mp} [r_{dsp} // r_{dsn}]} \quad \lambda \neq 0$$

$A_v = \infty$ $[\because r_{dsn} = r_{dsp} = \infty]$ for $\lambda = 0$.

* Sol:- Apply AC Analysis.



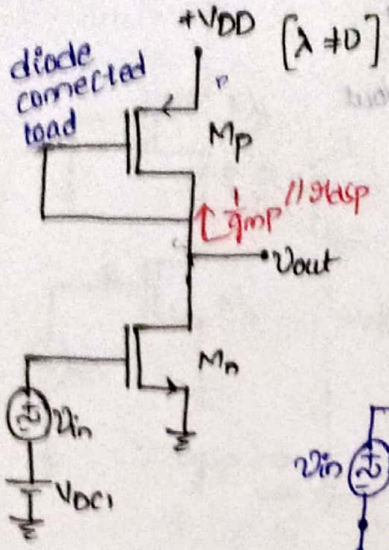




$$\Rightarrow R_{out} = \frac{v_{test}}{i_{test}} = r_{dsn} // r_{dsp}$$

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(2) Find

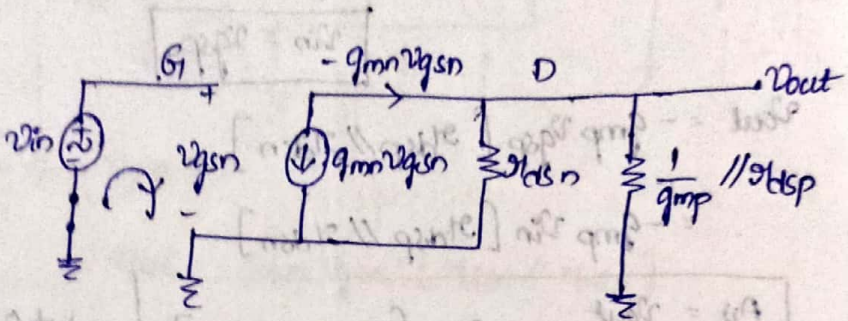


Sol:- Apply AC analysis.

By Observation:

i/p @ G & o/p @ D

common Source Amplifier.



$v_{in} = v_{gsn}$

$v_{out} = -g_{mn} v_{gsn} \left[r_{dsn} \,//\, \frac{1}{g_{mp}} \,//\, r_{dsp} \right]$

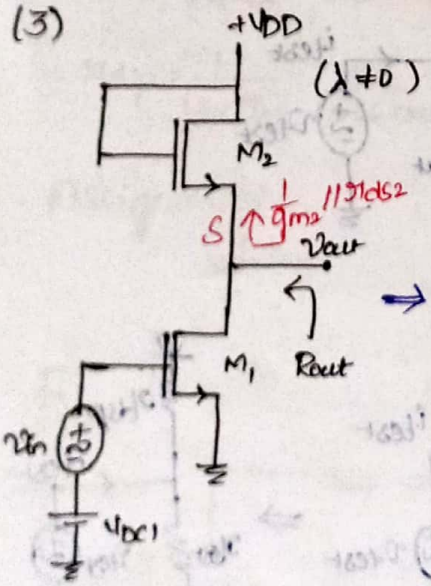
NOW, $\frac{v_{out}}{v_{in}} = A_v = -g_{mn} \left[r_{dsn} \,//\, \frac{1}{g_{mp}} \,//\, r_{dsp} \right] ; \lambda \neq 0$

$A_v = -g_{mn} \left[\infty \,//\, \frac{1}{g_{mp}} \,//\, \infty \right] ; \lambda = 0$

$A_v = -\frac{g_{mn}}{g_{mp}} ; \lambda = 0$

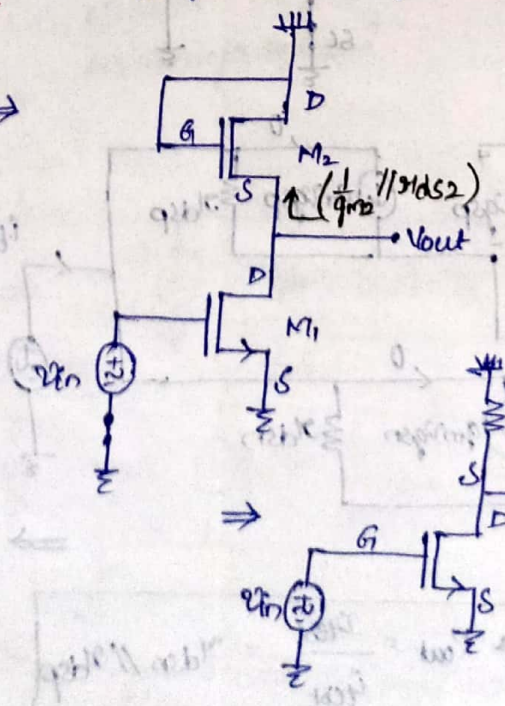
[Small signal 'Av' reduces bcz of diode connected load]

(3)



$A_v = ?$

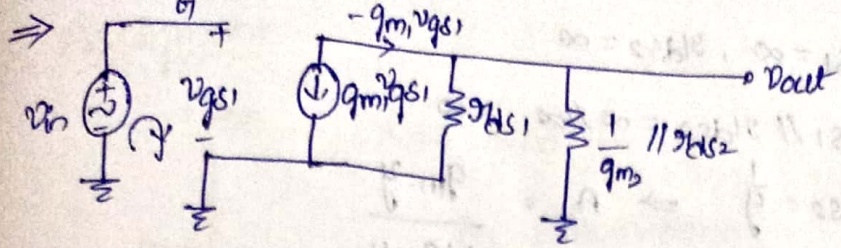
Apply AC Analysis.



By observation:

Common Source Amplifier.

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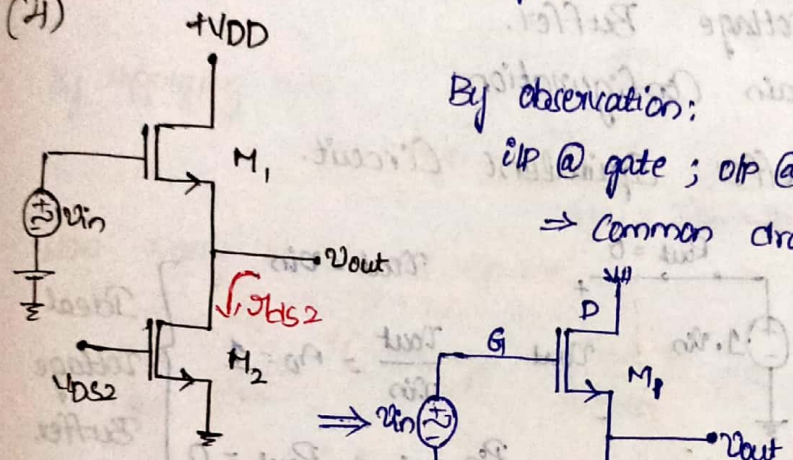


$v_{in} = v_{gs1}$ $\quad v_{out} = -g_{m1}v_{gs1}\left[r_{ds1} // \frac{1}{g_{m2}} // r_{ds2}\right]$

$$A_v = \frac{v_{out}}{v_{in}} = -g_{m1}\left[r_{ds1} // \frac{1}{g_{m2}} // r_{ds2}\right] \quad ; \lambda \neq 0$$

$$A_v = \frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2}} \quad ; \lambda = 0$$

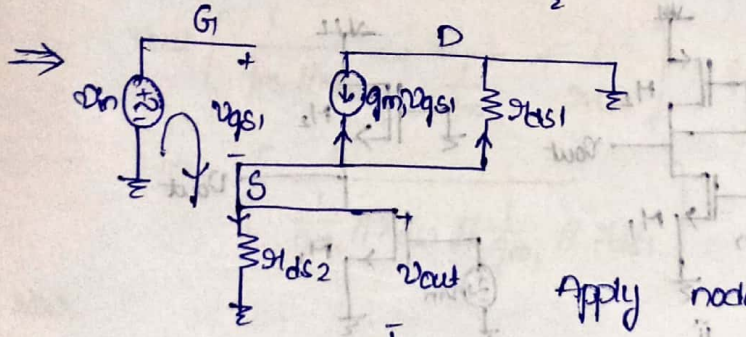
(H)



By observation:

i/p @ gate ; o/p @ source.

⇒ Common drain Amplifier.



Apply nodal Analysis @ the Source

$$-v_{in} + v_{gs1} + v_{out} = 0$$

$$v_{gs1} = v_{in} - v_{out}$$

$$\frac{v_{out} - 0}{r_{ds2}} + (-g_{m1}v_{gs1}) + \frac{v_{out} - 0}{r_{ds1}} = 0$$

$$\Rightarrow \frac{v_{out}}{r_{ds2}} - g_{m1}(v_{in} - v_{out}) + \frac{v_{out}}{r_{ds1}} = 0$$

$$v_{out}\left[\frac{1}{r_{ds2}} + g_{m1} + \frac{1}{r_{ds1}}\right] = g_{m1} \cdot v_{in}$$

$$\left[\frac{1}{r_{ds1}} + \frac{1}{r_{ds2}} = \frac{1}{r_{ds1} // r_{ds2}}\right]$$

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + \frac{1}{r_{ds1} // r_{ds2}}}$$

$$A_v = \frac{g_{m1}\left[r_{ds1} // r_{ds2}\right]}{1 + g_{m1}\left[r_{ds1} // r_{ds2}\right]} \quad ; \lambda \neq 0$$

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If $\lambda = 0 \Rightarrow r_{ds1} = \infty$, $r_{ds2} = \infty$

$\Rightarrow r_{ds1} // r_{ds2} = \infty // \infty = \infty$

put $r_{ds1} // r_{ds2} = \frac{1}{y} \Rightarrow A_v = \frac{g_m \cdot y}{1 + g_m y}$

as $\frac{1}{y} \Rightarrow \infty$

$\Rightarrow y \Rightarrow 0$

$A_v = \lim_{y \to 0} \frac{g_m}{y + g_m}$

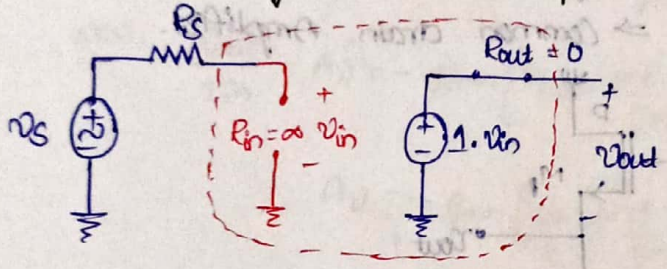
$A_v = \frac{g_m}{0 + g_m} = 1 \Rightarrow A_v = 1$

$\therefore A_v = 1$ for $\lambda = 0$.

$\Rightarrow$ This is voltage Buffer.

Common Drain Configuration.

Ideal voltage Buffer Equivalent Circuit.



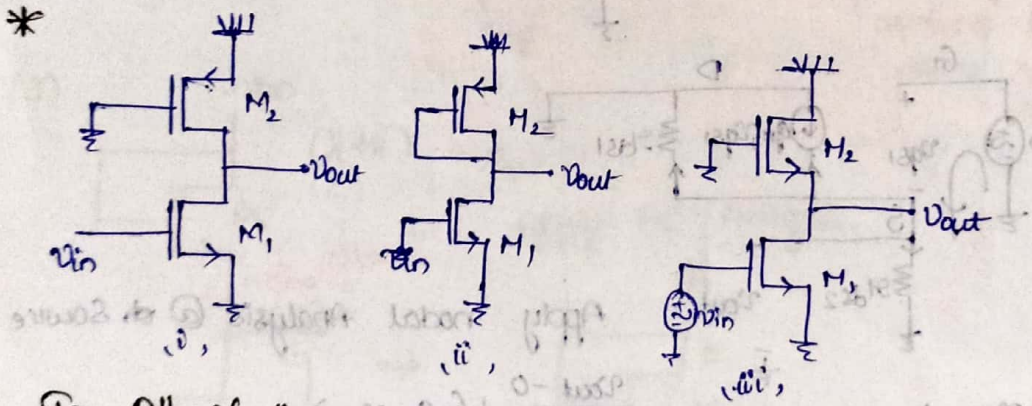
$V_{out} = V_{in}$

$\frac{V_{out}}{V_{in}} = A_v = 1$

$R_{in} = \infty$; $R_{out} = 0$

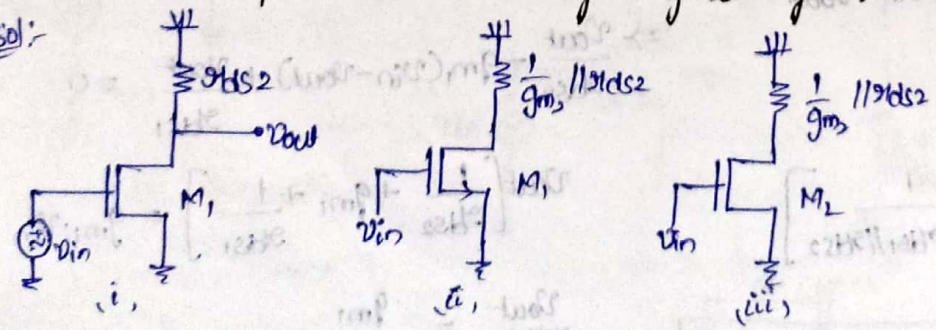
} Ideal voltage Buffer.

*



In All of the above three circuits I_{DQ} in M_1 is same which Amplifier is having highest gain?

Sol:-



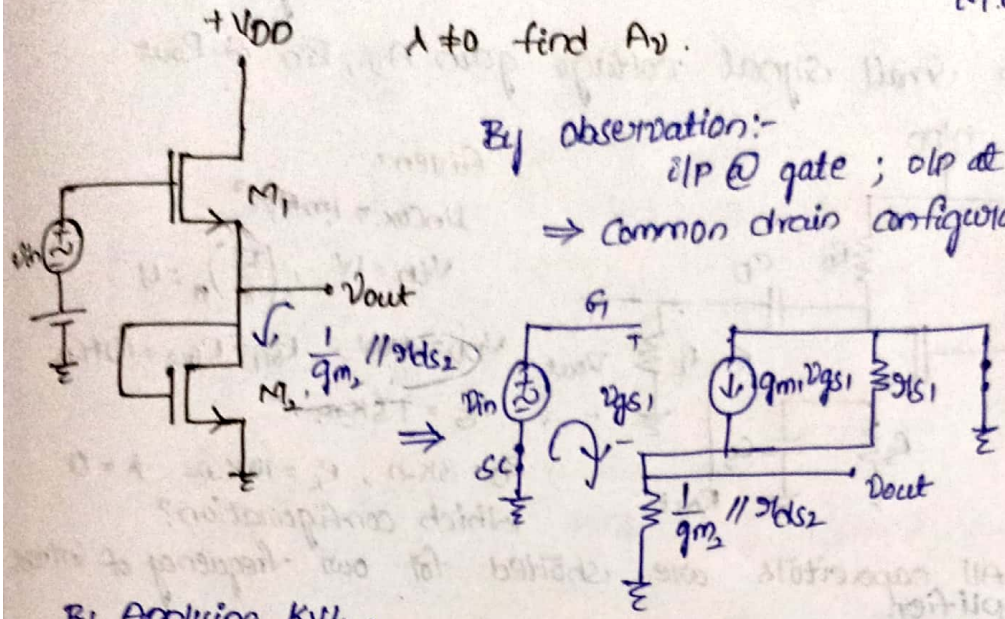
Ampl. i, is having high small signal voltage gain than ii, & iii,

$\because$ the small signal resistance seen into the drain of M_2 in Amplifier i, is 'r_{ds2}' which is higher.

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Assignment

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M. Suryakumari



$\lambda \neq 0$ find A_v.

By observation:-
i/p @ gate ; o/p at source
$\Rightarrow$ common drain configuration.

By Applying KVL,

$$-V_{in} + V_{gs1} + V_{out} = 0$$

$$V_{gs1} = V_{in} - V_{out}$$

NOW Apply Nodal at source.

$$\frac{V_{out} - 0}{\frac{1}{g_{m2}} // r_{ds2}} + (-g_{m1} V_{gs1}) + \frac{V_{out} - 0}{r_{ds1}} = 0$$

$V_{gs1} = V_{in} - V_{out}$

$$V_{out}\left[\frac{1}{\frac{1}{g_{m2}} // r_{ds2}} + g_{m1} + \frac{1}{r_{ds1}}\right] = g_{m1} V_{in}$$

$$V_{out}\left[\frac{1}{\frac{1}{g_{m2}} // r_{ds2}} + \frac{1}{\frac{1}{g_{m1}}} + \frac{1}{r_{ds1}}\right] = g_{m1} V_{in}$$

$$V_{out}\left[\frac{1}{\frac{1}{g_{m2}} // r_{ds2} // \frac{1}{g_{m1}} // r_{ds1}}\right] = g_{m1} V_{in}$$

NOW,

$$A_v = \frac{V_{out}}{V_{in}} = g_{m1}\left[\frac{1}{g_{m2}} // r_{ds2} // \frac{1}{g_{m1}} // r_{ds1}\right] \quad \text{for } \lambda \neq 0$$

$$A_v = \frac{V_{out}}{V_{in}} = g_{m1}\left[\frac{1}{g_{m2}} // \frac{1}{g_{m1}}\right]$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{m2} + g_{m1}} \quad \text{for } \lambda = 0$$

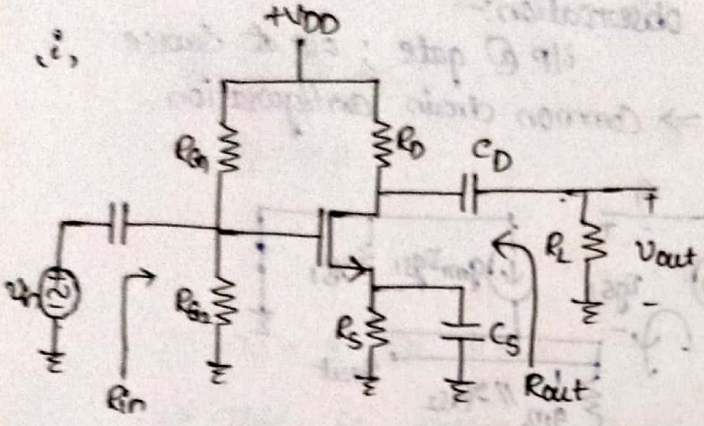
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Assignment

N180119
M. Surya kumari

Q. Find the Small signal voltage gain A_v, R_{in} & R_{out}

i)



Given:

$\mu_n C_{ox} = 1mA/V^2$

$V_{th} = 1V$, $\left(\frac{W}{L}\right)_n = 4$

$V_{DD} = +10V$, $R_{G1} = R_{G2} = 10M\Omega$

$R_S = 1.5K\Omega$

$R_D = 3K\Omega$, $R_L = 10K\Omega$ $\lambda = 0$

Which configuration?

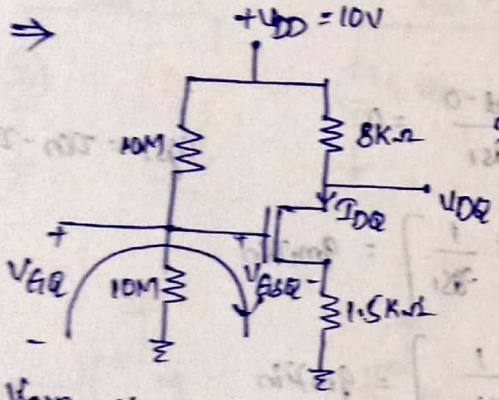
Assume All capacitors are shorted for our frequency of intrest.

CS Amplifier.

Sol:- Step 1: DC Analysis. for find Q. point.

for DC: $\omega = 0 \Rightarrow |Z_C| = \frac{1}{0.C} = \infty \Rightarrow$ O.C

$\Rightarrow$



Assume MOSfet is in Sat.

$I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSQ} - V_{th})^2$

$= \frac{1}{2} \times 1mA \times 4 \times (V_{GSQ} - 1)^2$

$= 2(V_{GSQ} - 1)^2$

$I_{DQ} = \frac{1}{2}[1m][4][V_{GSQ} - 1]^2 \rightarrow (1)$

$V_{GSQ} = V_{GQ} = \frac{R_{G2}}{R_{G1}+R_{G2}} \times V_{DD}$

$= \frac{10M}{10M+10M} \times 10$

$\Rightarrow V_{GSQ} = V_{GQ} = 5V$

Apply KVL in loop

$-V_{GQ} + V_{GSQ} + I_{DQ} \cdot R_S = 0$

$-5 + V_{GSQ} + I_{DQ}[1.5K] = 0$

$I_{DQ} = \frac{5 - V_{GSQ}}{1.5K} \rightarrow (2)$

from (1) & (2)

$2[V_{GSQ} - 1]^2 = \frac{5 - V_{GSQ}}{1.5K}$

$5 - V_{GSQ} = (1.5K)\,2\,[V_{GSQ}^2 + 1 - 2V_{GSQ}]$

$5 - V_{GSQ} = 3V_{GSQ}^2 + 3 - 6V_{GSQ}$

$3V_{GSQ}^2 - 5V_{GSQ} - 2 = 0 \Rightarrow V_{GSQ} = 2V, \frac{-1}{3}$ (X)

(V)

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$\Rightarrow I_D = \frac{5 - V_{GSQ}}{1.5K} \Rightarrow I_D = \frac{5-2}{1.5K} \Rightarrow I_D = 2mA$

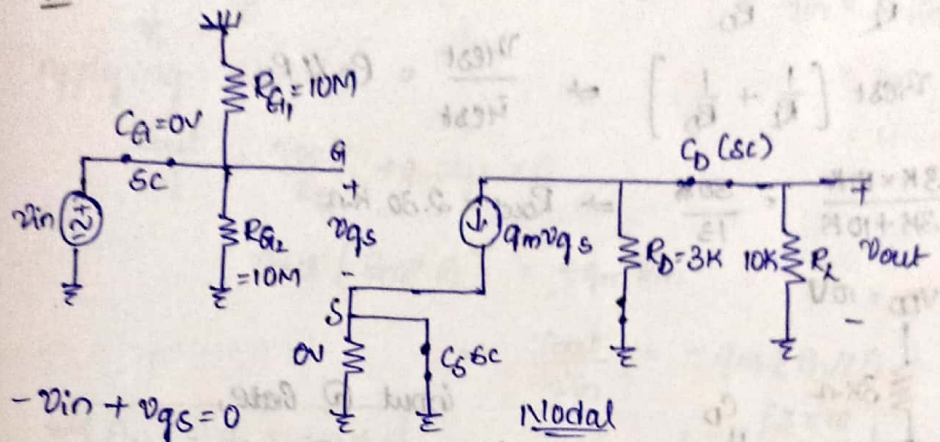
$V_{DQ} = V_{DD} - I_D R_D$

$= 10 - 2m(3K) \Rightarrow V_{DQ} = 4V$

$\Rightarrow$ operating point $(V_{DQ}, I_{DQ}) = (4V, 2mA)$

Step2: Small Signal Analysis.

A_V



$-v_{in} + v_{gs} = 0$

$v_{gs} = v_{in}$

Nodal

$\frac{v_{out}}{R_L} + \frac{v_{out}}{R_D} + g_m v_{gs} = 0$

$\frac{v_{out}}{R_L} + \frac{v_{out}}{R_D} + g_m v_{in} = 0$

$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{GSQ} - V_{th})$

$= 1mA \times 4 [2-1]$

$g_m = 4\ mA/V$

$v_{out}[R_D // R_L] + g_m v_{in} = 0$

$\frac{v_{out}}{v_{in}} = -g_m [R_D // R_L]$

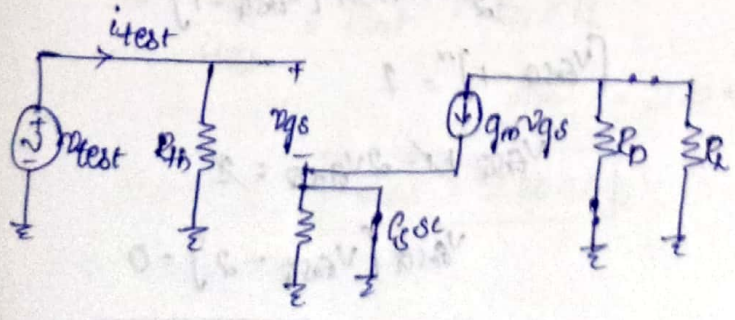
$A_V = \frac{v_{out}}{v_{in}} = -g_m \left(\frac{R_D R_L}{R_D + R_L}\right)$

$\Rightarrow A_V = -4\left[\frac{3 \times 10}{3+10}\right] = -4\left[\frac{30}{13}\right]$

$\Rightarrow A_V = -9.2307\ V/V$

(v_{in} & v_{in} are 180° out of phase)

R_{in}



$R_{in} = R_{th} = \frac{v_{test}}{i_{test}}$

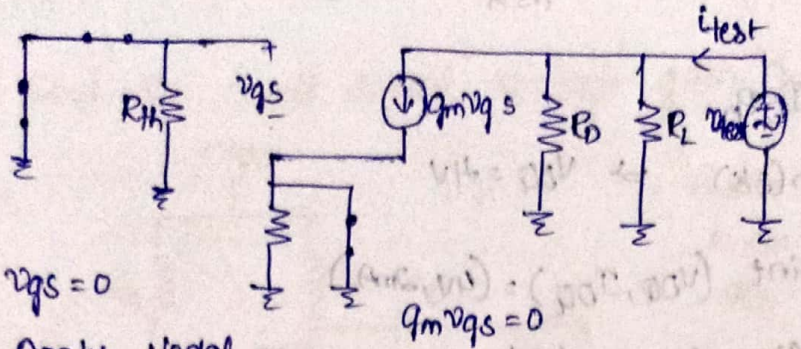
$R_{th} = R_{G_1} // R_{G_2}$

$= \frac{10M \times 10M}{(10+10)}$

$R_{th} = 5M\Omega$

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Rout



$v_{gs} = 0$

$g_m v_{gs} = 0$

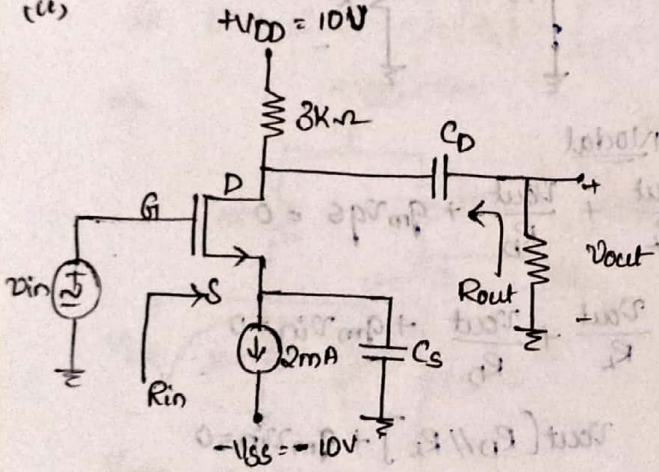
Apply Nodal

$$i_{test} = \frac{v_{test}}{R_L} + \frac{v_{test}}{R_D} + 0$$

$$i_{test} = v_{test}\left[\frac{1}{R_L} + \frac{1}{R_D}\right] \Rightarrow \frac{v_{test}}{i_{test}} = R_D // R_L$$

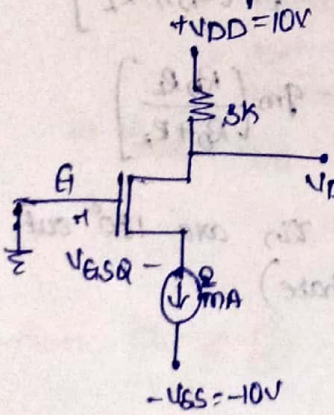
$$R_{out} = \frac{3K \times 10K}{3K + 10K} = \frac{30}{13} \Rightarrow R_{out} = 2.30\ K\Omega$$

(ii)



input @ Gate,
output @ drain
⇒ Common Source Amplifier.

Step1 : Finding Q. Points. DC Analysis.



$V_{DQ} = V_{DD} - I_D R_D$
$= 10 - 2(3)$
$= 4V$

By observation:

$I_{DQ} = 2mA$, $V_G = 0V$.

Assume it is in Sat :-

$$I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSQ} - V_{tn})^2$$

$$2mA = \frac{1}{2} \times 1m \times 4\left[V_{GSQ} - 1\right]^2$$

$$\left[V_{GSQ} - 1\right]^2 = 1$$

$$V_{GSQ}^2 + 1 - 2V_{GSQ} = 1$$

$$V_{GSQ}\left[V_{GSQ} - 2\right] = 0$$

$$\Rightarrow \boxed{V_{GSQ} = 2V}$$

Justification

$V_{GSQ} - V_{tn} > V_{DQ}$

$2 - 1 > 4$

$1 > 4$

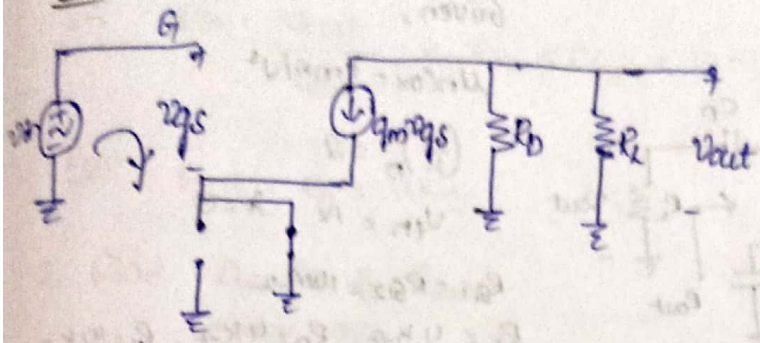
⇒ Saturation.

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$\Rightarrow$ Q.point $(V_{DQ}, I_{DQ}) = (4V, 2mA)$

Step2:- Small Signal Analysis.

A_v



$-v_{in} + v_{gs} = 0$

$\boxed{v_{gs} = v_{in}}$

$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{GSQ} - V_{th})$

$= 1m \times 4 [2-1]$

$= 4$

Applying Nodal:

$$\frac{v_{out}}{R_L} + \frac{v_{out}}{R_D} + g_m v_{gs} = 0$$

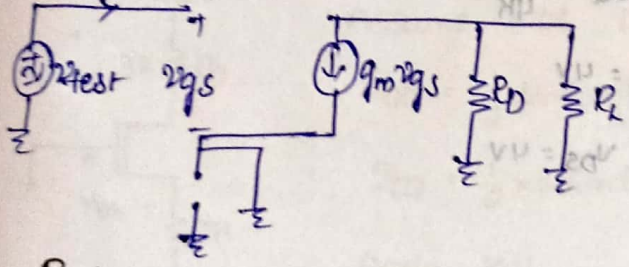
$$v_{out}[R_D // R_L] = -g_m v_{in}$$

$$\Rightarrow \frac{v_{out}}{v_{in}} = -g_m [R_D // R_L]$$

$$= -4\left[\frac{3 \times 10}{3+10}\right] = -9.2307 V/V$$

$\Rightarrow \boxed{A_v = -9.2307 V/V}$

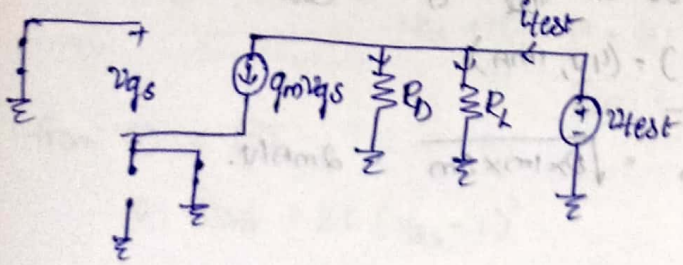
R_{in}



$$R_{in} = \frac{v_{test}}{i_{test}} = \frac{v_{test}}{0} = \infty$$

$\Rightarrow \boxed{R_{in} = \infty}$

R_{out}:-



$v_{gs} = 0$

$\Rightarrow g_m v_{gs} = 0$

$$\Rightarrow \frac{v_{test}}{i_{test}} = R_{out} = R_D // R_L$$

$$= \frac{30}{13} = 2.30 K\Omega$$

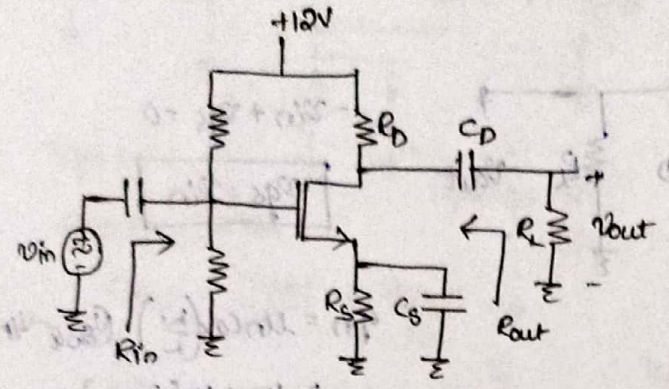
$\boxed{R_{out} = 2.30 K\Omega}$

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Assignment

N180119
M. Surya kumari.

1. Find A_V, R_{in} & R_{out}?



Given,

$\mu_n C_{ox} = 1\,mA/V^2$

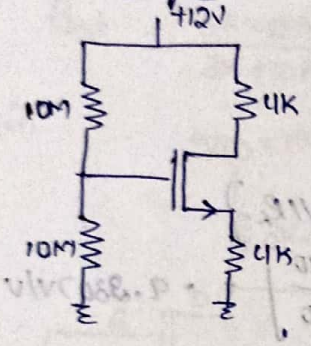
$\left(\frac{W}{L}\right)_n = 2$

$V_{th} = 1V$, $\lambda = 0$

$R_{G1} = R_{G2} = 10M\Omega$

$R_S = 4k\Omega$, $R_D = 4k\Omega$, $R_L = 10k\Omega$

DC Analysis:



$V_G = \frac{R_{G_2} \times V_{DD}}{R_{G_1} + R_{G_2}} = \frac{10M \times 12}{10M + 10M}$

V across $R_D = \frac{12V}{3} = 4V$ [Here V_{DD} is equally distributed]

$\Rightarrow I_D \cdot R_D = 4V$

$\Rightarrow I_{DQ} = \frac{4V}{4K} = 1mA$

$\therefore V_{DQ} = 12V - 4V = 8V$; $V_S = 4V$

$V_{GQ} = \frac{10}{10+10} \times 12 = 6V \Rightarrow V_{DS} = 4V$.

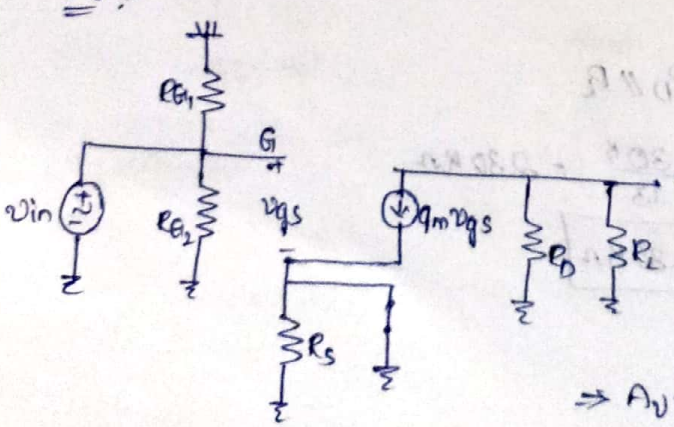
Justification:-

Since $V_G = 6V$ & $V_{DQ} = 8V \Rightarrow V_{DQ} > V_G \Rightarrow$ Sat

$\therefore$ Q. Point $(V_{DQ}, I_{DQ}) = (4V, 1mA)$

$g_m = \sqrt{2 I_{DQ} \mu_n C_{ox} \left(\frac{W}{L}\right)_n} = \sqrt{2 \times 1m \times 2m} = 2mA/V.$

Ans:-



By observation:

$v_{in} = v_{gs} \rightarrow (1)$

$v_{out} = -g_m v_{gs} (R_D // R_L)$

$\Rightarrow A_V = \frac{v_{out}}{v_{in}} = -g_m (R_D // R_L)$

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$\Rightarrow A_v = -2m\,(4K\Omega \,//\, 10K\Omega)$

$$\boxed{A_v = -5.714 \text{ V/V}}$$

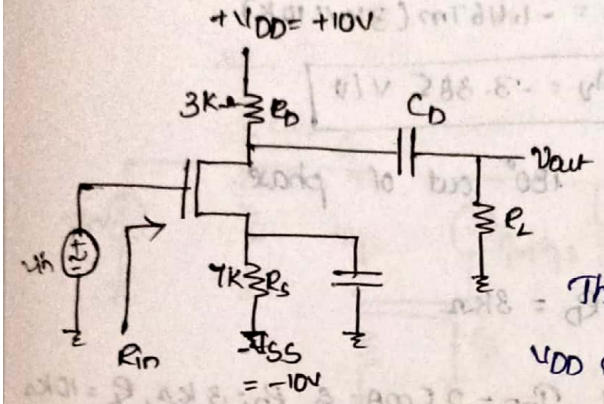
Rin

$$R_{in} = \frac{v_{test}}{i_{test}} = R_{G_1} // R_{G_2} = 10M // 10M = 5M\Omega$$

Rout

$$R_{out} = R_D = 4K\Omega$$

2. Find A_v, Rin & Rout



$\mu_n C_{ox} = 0.5 mA/V^2$ $\left(\frac{W}{L}\right)_n = 2$

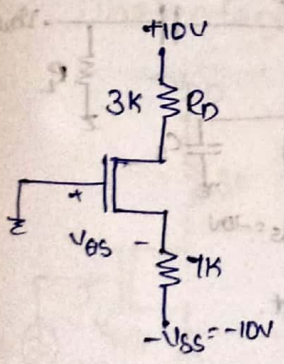
$V_{th} = 1V$ $\lambda = 0$

$R_D = 3K\Omega$, $R_S = 7K\Omega$

This is dual supply circuit then V_{DD} & V_{SS} in CS configuration.

DC Analysis:

C_D & C_S are shorted, $V_{in} \Rightarrow$ S.C



Assume MOS is in Sat:

$$I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS} - V_{th})^2$$

$$I_{DQ} = \frac{1}{2} \times 0.5m(2)(V_{GS}-1)^2 \Rightarrow I_{DQ} = 0.5m(V_{GS}-1)^2 \rightarrow (1)$$

Apply KVL,

$$V_{GS} + I_{DQ} \cdot 7K - 10 = 0$$

$$I_{DQ} = \frac{10 - V_{GSQ}}{7K\Omega} \rightarrow (2)$$

from (1) & (2)

$$10 - V_{GSQ} = 3.5(V_{GS}-1)^2$$

$$10 - V_{GSQ} = 3.5V_{GSQ}^2 + 3.5 - 7V_{GSQ}$$

$$3.5V_{GSQ}^2 - 6V_{GSQ} - 6.5 = 0 \rightarrow$$

$$V_{GSQ} = 2.467, \; -0.752 (\times)$$

$$\Rightarrow I_{DQ} = \frac{10 - 2.467}{7K} = 1.08\,mA \; ; \; V_{DQ} = 10 - 3(1.08m) = 6.771V$$

$V_{DQ} > V_{GSQ}$

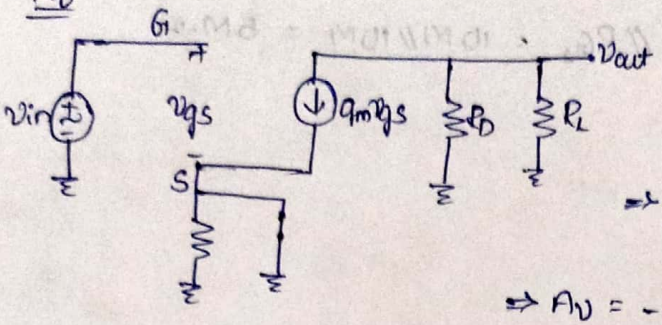
$\Rightarrow$ Saturation

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$g_m = \sqrt{2 I_{DQ} \mu_n C_{ox} \left(\frac{W}{L}\right)_n} = 0.5m \times 2 \times (2.467 - 1V)$

$g_m = 1.467 mA/V.$

A_V



$V_{in} = V_{gs}$

$V_{out} = -g_m V_{gs} (R_D // R_L)$

$\Rightarrow \frac{V_{out}}{V_{in}} = A_V = -g_m (R_D // R_L)$

$\Rightarrow A_V = -1.467m (3K // 10K)$

$\boxed{A_V = -3.385 \text{ V/V}}$

'-' indicates i/p & o/p are 180° out of phase.

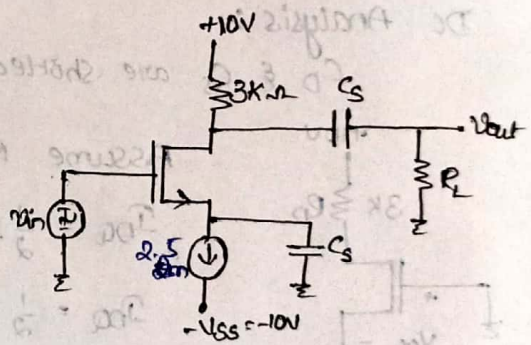
R_{in}

$R_{in} = \infty$

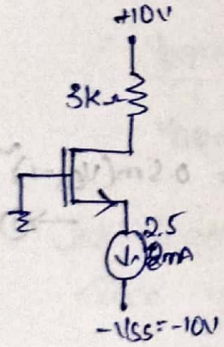
R_{out}

$R_{out} = R_D = 3K\Omega$

3. Repeat the above problem for $I_{DQ} = 2.5mA$ & $R_D = 3 K\Omega$, $R_L = 10K\Omega$ for $\lambda = 0$. find A_V, R_{in} & R_{out}.



DC Analysis.



$I_{DQ} = 2.5mA$

$V_{DQ} = 10 - (3K \times 2.5m)$

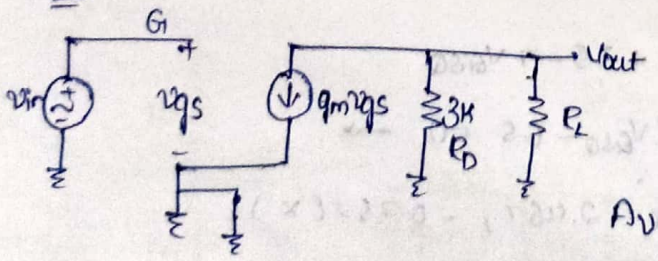
$V_{DQ} = 2.5V$

$V_G = 0$, $V_{DQ} = 2.5V \Rightarrow$ Indeed Sat.

$g_m = \sqrt{2 I_{DQ} \mu_n C_{ox} \left(\frac{W}{L}\right)_n} = \sqrt{2 \times 2.5m \times 1m \times 2} = \sqrt{10} mA/V$

$\boxed{g_m = 3.162 mA/V}$

A_V



$V_{in} = V_{gs}$

$V_{out} = -g_m V_{gs} (R_D // R_L)$

$A_V = \frac{V_{out}}{V_{in}} = -g_m (R_D // R_L)$

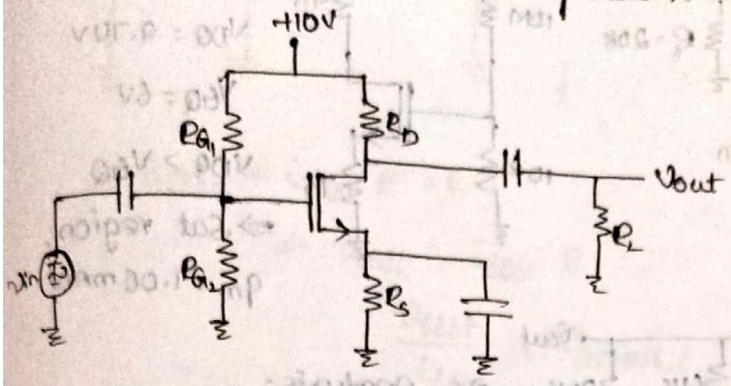
$= -3.612m (3K // 10K)$

$\boxed{A_V = -7.2977 \text{ V/V}}$

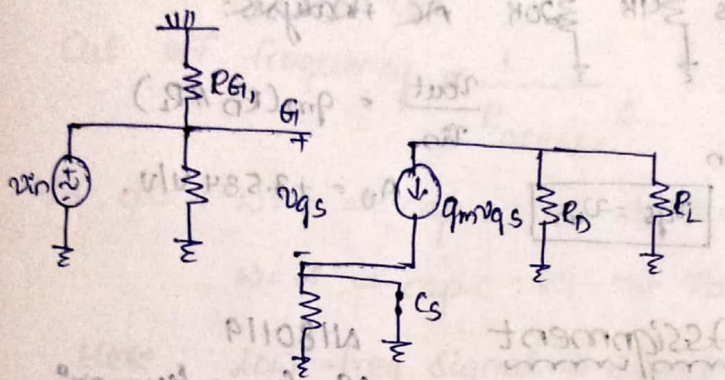
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Rin $R_{in} = \infty$ Rout $R_{out} = R_D = 3K\Omega$

4. Which nodes are 'AC' ground?



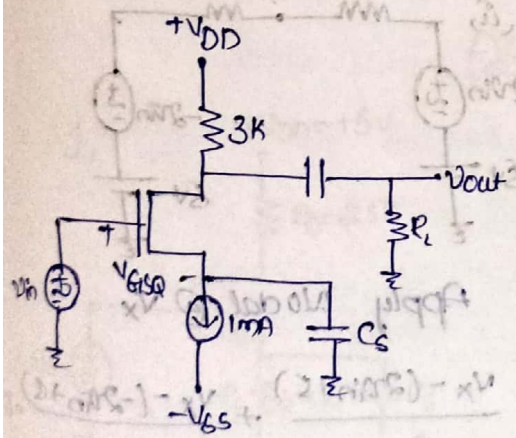
to find AC grounds, Apply AC analysis.

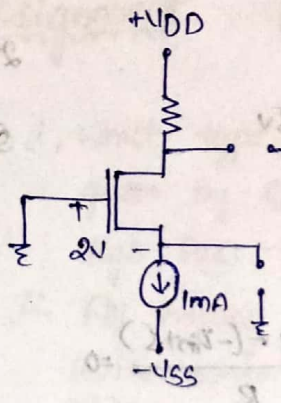


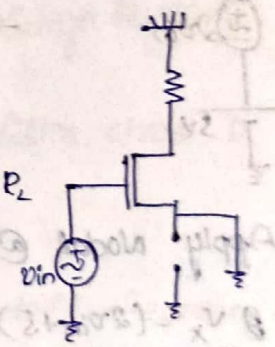
C_S & V_{DD} are AC grounds.

5. Find instantaneous source voltage V_S?

Instantaneous Source voltage $v_S = V_S + v_s$







DC voltage: $V_{GS} = 2V$

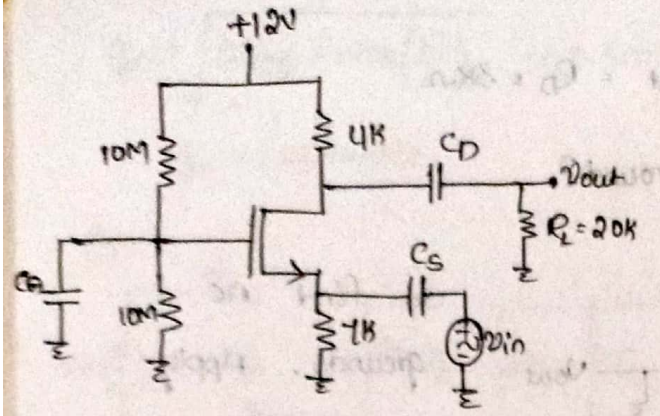
$\Rightarrow \because V_G = 0V \Rightarrow V_S = -2V$

ac voltage $v_S = 0V$

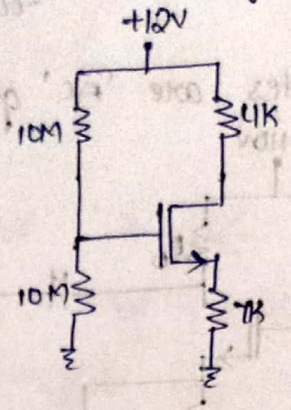
$\Rightarrow$ Instantaneous Source voltage

$$\boxed{V_S = 2V}$$

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DC Analysis.



$I_{DQ} = 0.56\ mA$

$V_{DQ} = 9.74\ V$

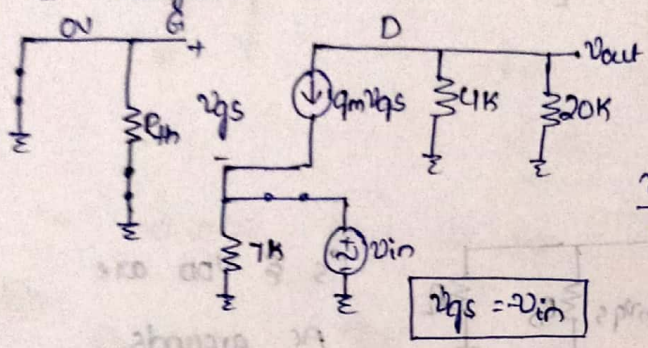
$V_{tQ} = 6\ V$

$V_{DQ} > V_{tQ}$

$\Rightarrow$ Sat region.

$g_m = 1.06\ mA/V$

AC Analysis.



$V_{gs} = -V_{in}$

AC Analysis:

$\frac{V_{out}}{V_{in}} = g_m(R_D \parallel R_L)$

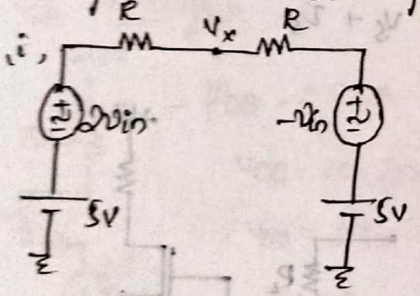
$A_V = +3.584\ V/V.$

Assignment

N180119

M. Surya Kumari.

1. Repeat the above problem.



Apply Nodal @ V_x

$$\frac{V_x - (2v_{in}+5)}{R} + \frac{V_x - (-v_{in}+5)}{R} = 0$$

$$\frac{2V_x}{R} - \frac{2v_{in}}{R} - \frac{5}{R} + \frac{v_{in}}{R} - \frac{5}{R} = 0$$

$$\frac{2V_x}{R} - \frac{v_{in}}{R} - \frac{10}{R} = 0$$

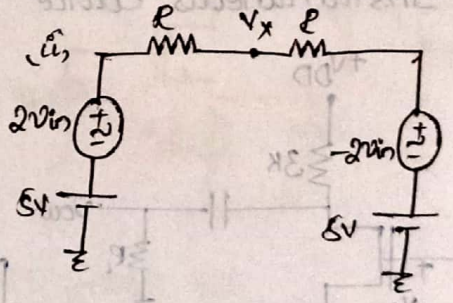
$$2V_x = v_{in} + 10$$

$$V_x = \frac{v_{in}+10}{2}$$

Here V_x is not fixed

$\Rightarrow$ It is varying

$\Rightarrow$ V_x is not ac ground.



Apply Nodal @ V_x

$$\frac{V_x - (2v_{in}+5)}{R} + \frac{V_x - (-2v_{in}+5)}{R} = 0$$

$$\frac{2V_x}{R} - \frac{2v_{in}}{R} - \frac{5}{R} + \frac{2v_{in}}{R} - \frac{5}{R} = 0$$

$$\frac{2V_x}{R} - \frac{10}{R} = 0$$

$$V_x = \frac{10}{2} = 5V$$

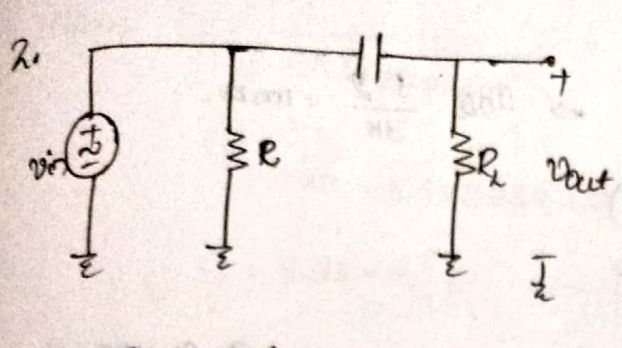
Here V_x is fixed

$\Rightarrow$ Not varying.

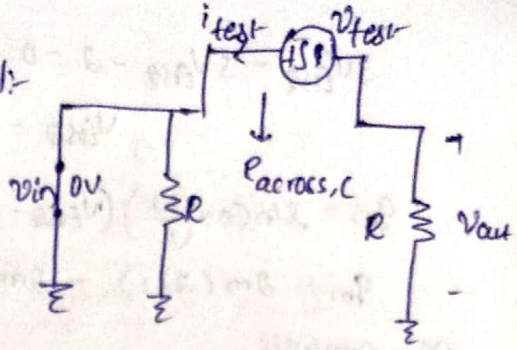
$\Rightarrow$ V_x is an ac ground.

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2.



Sol:-



$-v_{test} + i_{test} \cdot R = 0$

$\Rightarrow v_{test} = i_{test} \cdot R$

$\frac{v_{test}}{i_{test}} = R_{across,C} = R.$

Cut off frequency $= \frac{1}{R_{across,C} \, C} = \frac{1}{RC}$

for dc : $\omega = 0 \Rightarrow$ cap.c : oc $\Rightarrow v_{out} = 0$

$\omega = \infty \Rightarrow$ cap c : sc $\Rightarrow v_{out} = v_{in}$

Here Low freq. signal $\Rightarrow$ Stopping or Attenuating

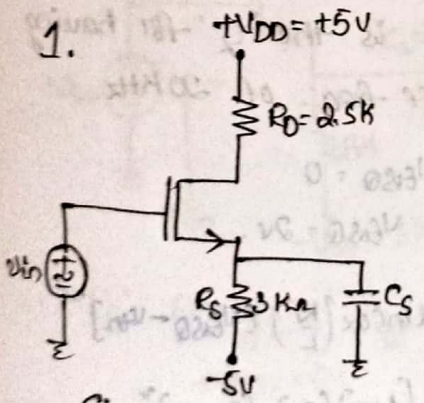
High freq. signals $\Rightarrow$ Passing.

$\Rightarrow$ High Pass Filter.

Assignment

N180119
M. Surya kumari.

1.



i, Which type of filter chars is given by C_S?

High Pass filter.

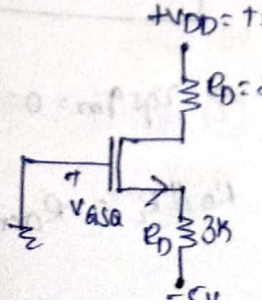
ii, For having a cutoff frequency of 100 Hz. what should be the value of 'C_S'.

Given: $\mu_n C_{ox} = 1 mA/V^2$

$V_{tn} = 1V$

$\left(\frac{W}{L}\right)_n = 2$, $\lambda = 0$

Do DC analysis for g_m.



$V_{GSQ} + 3k(I_{DQ}) - 5 = 0$

$I_{DQ} = \frac{5 - V_{GSQ}}{3k} \rightarrow (1)$

In sat:

$I_{DQ} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n [V_{GSQ} - V_{tn}]^2$

$= \frac{1}{2} \times 1m \times (2) [V_{GSQ} - 1]^2 \rightarrow (2)$

(1) = (2)

$\frac{5 - V_{GSQ}}{3K} = [V_{GSQ} - 1]^2$

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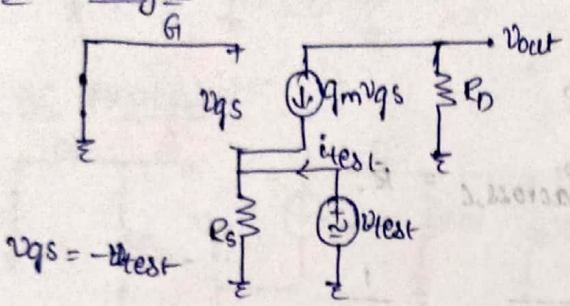
$3V_{GSQ}^2 - 5V_{GSQ} - 2 = 0$

$V_{GSQ} = 2 \Rightarrow I_{DQ} = \frac{5-2}{3K} = 1mA.$

$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GSQ} - V_{tn})$

$g_m = 2m(2-1) = 2mA/V.$

AC Analysis.



Apply Nodal, @ source

$i_{test} = \frac{v_{test}}{R_S} - g_m v_{gs}$

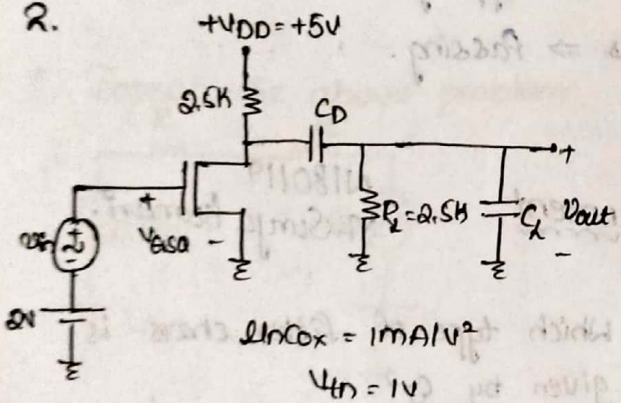
$i_{test} = \frac{v_{test}}{R_S} + g_m v_{test}$

$\frac{v_{test}}{i_{test}} = R_{across,C_S} = \frac{1}{g_m} // R_S$

$\Rightarrow C_S = \frac{1}{2\pi f_L R_{across,C_S}} = \frac{1}{2\pi(100)\left(\frac{1}{g_m} // C_S\right)} = \frac{1}{2\pi(100)\left(\frac{1}{2m} // 3K\right)}$

$C_S = \frac{1}{2\pi(100)(0.4885K)} = 3.714\mu F$ $\boxed{C_S = 3.714\mu F}$

2.



$\mu_n C_{ox} = 1mA/V^2$

$V_{tn} = 1V$

$\left(\frac{W}{L}\right)_n = 2$

i, Which type of the fitter chars. does C_L gives?

low pass filter.

ii, What is the 'C_L' for having cut-off freq. of 20 KHz.

$-V_{G1} + V_{GSQ} = 0$

$V_{GSQ} = 2V.$

$I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)[V_{GSQ} - V_{tn}]^2$

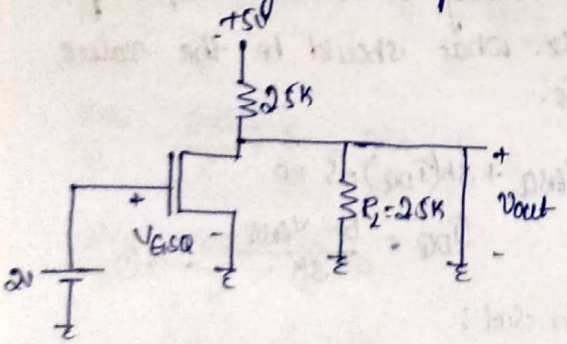
$= \frac{1}{2}.[1m][2][2-1]^2$

$I_{DQ} = 1mA$

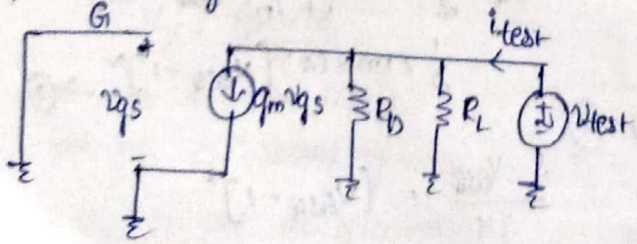
$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)[2-1]$

$g_m = 1m(2)(1) \Rightarrow \boxed{g_m = 2mA/V}$

i, DC Analysis for g_m.



ii, AC Analysis



$v_{gs} = 0 \Rightarrow v_{gs} g_m = 0$

$\frac{v_{test}}{i_{test}} = R_D // R_L = R_{across,C_L}$

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Now, $C_L = \frac{1}{2\pi R_{Dacross,C_L} \cdot f_L}$

$C_L = \frac{1}{2\pi \times (2.5K \| 2.5K)(20Hz)} = \frac{1}{157.07 \times 10^6}$

$C_L = 6.36 \times 10^{-9} F \Rightarrow \boxed{C_L = 6.36 nF}$

Assignment

~~Cut-off~~ voltage gain in dB.

i, $A_v = 100 V/V$

$|A_v|_{dB} = 20 \log_{10} A_v$

$= 20 \log_{10} 100$

$= 20 \times 2$

$|A_v|_{dB} = 40 dB$

ii, $A_v = 0.1 V/V$

$|A_v|_{dB} = 20 \log 0.1$

$= 20 \log_{10} 10^{-1}$

$= -20$

$|A_v|_{dB} = -20 dB$

iii, $A_v = 1000 V/V$

$|A_v|_{dB} = 20 \log_{10} A_v$

$= 20 \log_{10} 1000$

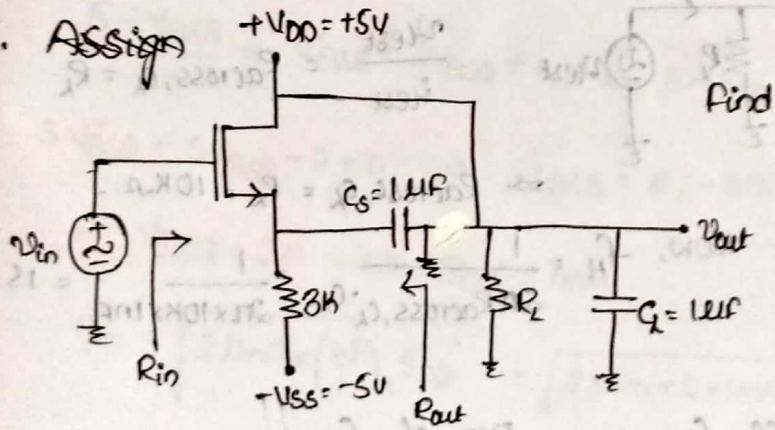
$= 20 \times 3$

$|A_v|_{dB} = 60 dB$

Assignment

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1. Assign



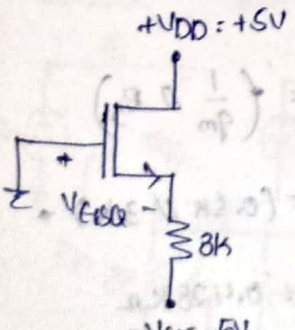
Find f_L, f_H & Midband gain. Given:

$\mu_n C_{ox} = 1 mA/V^2$

$V_{tn} = 1V$

$\left(\frac{W}{L}\right)_n = 2$

i, DC Analysis to find Q.point & then g_m.



$V_{GSQ} + 3K(I_{DQ}) - 5 = 0$

$I_{DQ} = \frac{5 - V_{GSQ}}{3K} \rightarrow (1)$

Assume MOS in sat:

$I_{DQ} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{GSQ} - V_{tn})^2$

$I_{DQ} = \frac{1}{2} \times 1 \times 2 (V_{GSQ} - 1)^2 = (V_{GSQ} - 1)^2 \rightarrow (2)$

from (1) & (2)

$\frac{5 - V_{GSQ}}{3K} = V_{GSQ}^2 + 1 - 2V_{GSQ}$

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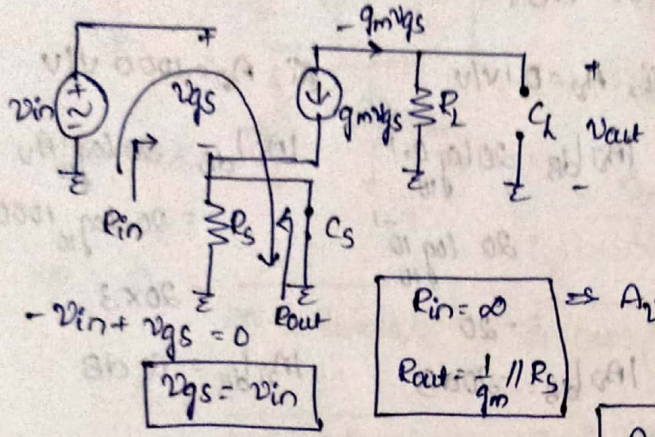
$5 - V_{GSQ} = 3V_{GSQ}^2 - 6V_{GSQ} + 3$

$3V_{GSQ}^2 - 5V_{GSQ} - 2 = 0 \Rightarrow V_{GSQ} = 2, -0.33\,(X)$

$\Rightarrow V_{GSQ} = 2V, \quad I_{DQ} = 1mA.$

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_n I_{DQ}} = \sqrt{2(1m)(2)(1mA)} = 2\,mA/V$$

ii, Midband gain ⇒ Small signal voltage gain:



$v_{out} = -g_m v_{gs}(R_L)$

$\frac{v_{out}}{v_{in}} = -g_m R_L$

$-v_{in} + v_{gs} = 0$

$v_{gs} = v_{in}$

$R_{in} = \infty$

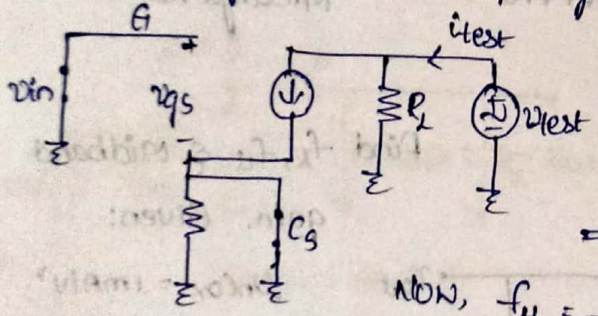
$R_{out} = \frac{1}{g_m} // R_S$

$\Rightarrow A_v = -g_m R_L$

$= -2mA/V \times 10K\Omega$

$A_v = -20\,V/V$

iii, f_H : higher cutoff frequency. BCZ of C_L.



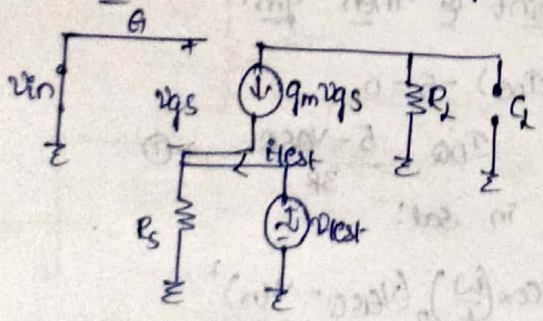
$\frac{v_{test}}{i_{test}} = R_{across, C_L} = R_L$

$\Rightarrow R_{across, C_L} = R_L = 10K\Omega.$

NOW, $f_H = \frac{1}{2\pi R_{across, C_L} \cdot C_L} = \frac{1}{2\pi \times 10K \times 1nF} = 15\,Hz.$

$\Rightarrow \boxed{f_H = 15\,Hz}$

iv, f_L : lower cutoff frequency. BCZ of C_S.



$\Rightarrow \frac{v_{test}}{i_{test}} = \left(\frac{1}{g_m} // R_S\right)$

$R_{across, C_S} = (0.5K // 3K)$

$R_{across, C_S} = 0.428K\Omega$

$v_{gs} = -v_{test}$

Nodal @ source.

$i_{test} = \frac{v_{test}}{R_S} - g_m v_{gs}$

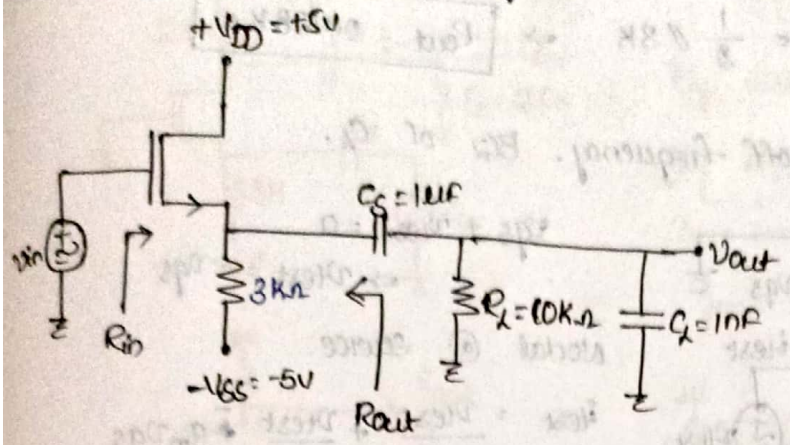
Now, $f_L = \frac{1}{2\pi R_{across, C_S} \cdot C_S} = \frac{1}{2\pi \times 0.428K \times 1\mu F}$

$\boxed{f_L = 37\,Hz}$

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Assignment

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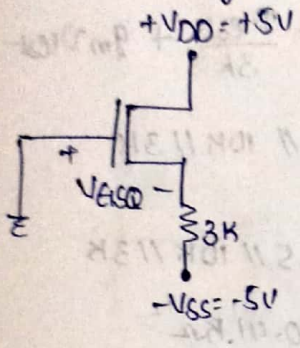
Find f_L, f_H & midband gain, given

$\mu_n C_{ox} = 1mA/V^2$

$V_{tn} = 1V$,

$\left(\frac{W}{L}\right)_n = 2$, $\lambda = 0$.

(1) DC Analysis.



$V_{GSQ} + I_{DQ}(3K) - 5 = 0$

$V_{GSQ} = 5 - I_{DQ} = \frac{5 - V_{GSQ}}{3K}$ → ①

as $V_{DQ} > V_{GQ}$ ⇒ sat.

$\Rightarrow I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSQ} - V_{tn})^2$

$= \frac{1}{2} \times 1m \times 2 (V_{GSQ} - 1)^2$

from ① & ②

$I_{DQ} = (V_{GSQ} - 1)^2$ → ②

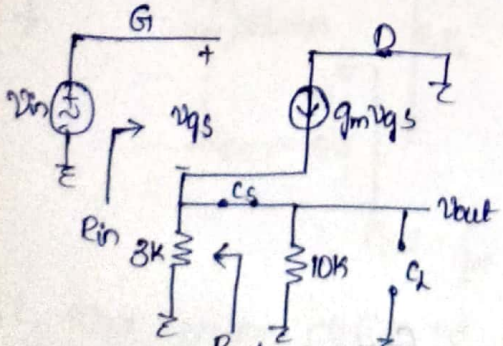
$\frac{5 - V_{GSQ}}{3K} = V_{GSQ}^2 - 2V_{GSQ} + 1 \Rightarrow 5 - V_{GSQ} = 3V_{GSQ}^2 - 6V_{GSQ} + 3$

$3V_{GSQ}^2 - 5V_{GSQ} - 2 = 0 \Rightarrow V_{GSQ} = 2, -0.33(X)$

$\Rightarrow V_{GSQ} = 2V \Leftrightarrow I_{DQ} = 1mA$

$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_n I_{DQ}} = \sqrt{2 \times 1m \times 2 \times 1mA} = 2mA/V.$

(2) Midband gain (small signal voltage gain)



input KVL, $-v_{in} + v_{gs} + v_{out} = 0$

$v_{out} = -g_m v_{gs}(10K // 13K)$

$\Rightarrow v_{out} = g_m(v_{in} - v_{out})(3K // 10K)$

$v_{out} = g_m(v_{in} - v_{out})(2.3K)$

$v_{out}(1 + 2.3K g_m) = v_{in} g_m 2.3K$

$\frac{v_{out}}{v_{in}} = \frac{g_m 2.3K}{1 + g_m 2.3K} = \frac{2(2.3)}{1 + 2(2.3)}$

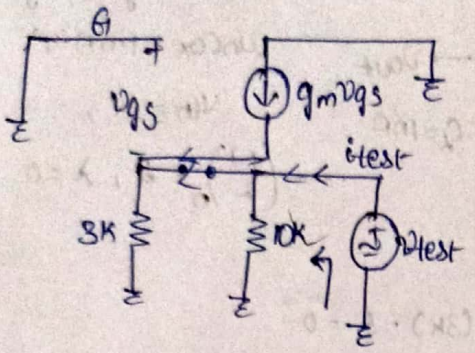
$\boxed{A_v = 0.82 V/V}$ Buffer.

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$R_{in} = \infty$

$R_{out} = \frac{1}{g_m} // R_S = \frac{1}{2} // 3K \Rightarrow$ **$R_{out} = 0.428\,K\Omega$**

(3) f_H : Higher cutoff frequency. Bcz of C_L.



$v_{gs} + v_{test} = 0$

$\Rightarrow v_{test} = -v_{gs}$

Nodal @ source.

$i_{test} = \frac{v_{test}}{10K} + \frac{v_{test}}{3K} - g_m v_{gs}$

$i_{test} = \frac{v_{test}}{10K} + \frac{v_{test}}{3K} + g_m v_{test}$

$\frac{v_{test}}{i_{test}} = \frac{1}{g_m} // 10K // 3K$

$R_{across, C_L} = 0.5 // 10K // 3K$

$R_{across, C_L} = 0.41\,K\Omega$

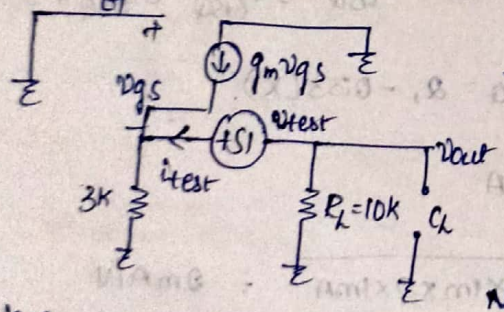
Now,

$f_H = \frac{1}{2\pi R_{across, C_L} \cdot C_L}$

$= \frac{1}{2\pi \times 0.41K \times 10F}$

$f_H = 388.18$ KHz

(4) f_L : Lower cutoff frequency. Bcz of C_S.



$\frac{v_{test}}{i_{test}} = R_{across, C_S} = \left(\frac{1}{g_m} // R_S\right) + R_L$

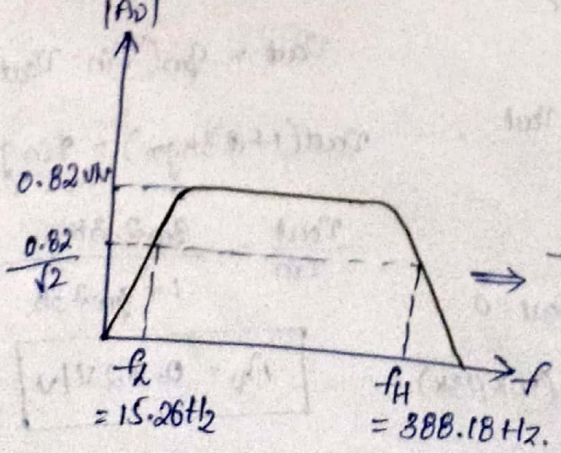
$= (3K // 0.5K) + 10K$

$R_{across, C_S} = 10.428K$

Now,

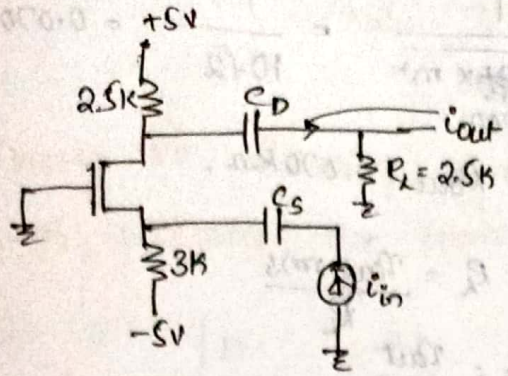
$f_L = \frac{1}{2\pi \cdot R_{across, C_S} \cdot C_S} = \frac{1}{2\pi \times 10.428K \times 1\mu F} = 15.26$ Hz.

$\Rightarrow$ **$f_L = 15.26$ Hz**



$\Rightarrow$ frequency response of CD Amplifier.

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1. 

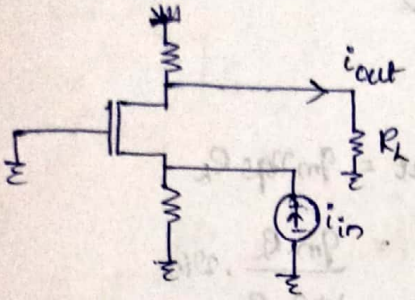
find $\frac{i_{out}}{i_{in}} = ?$

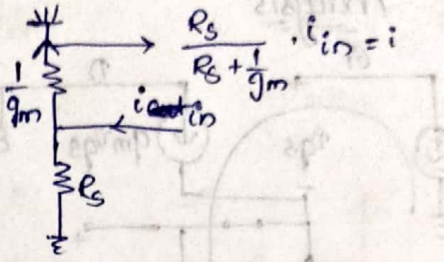
By observation,

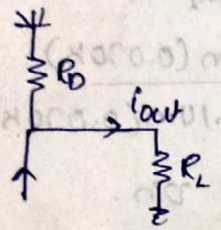
By doing DC Analysis

$I_D = 1mA$ (sat)

$g_m = 2 mA/V$







$i_{out} = i \cdot \frac{R_D}{R_D + R_L}$

$$\frac{i_{out}}{i_{in}} = \frac{R_S}{R_S + \frac{1}{g_m}} \cdot \frac{R_D}{R_D + R_L}$$

$$\Rightarrow A_I = \frac{3K}{3K+0.5A} \cdot \frac{1}{2} \Rightarrow \boxed{A_I = \frac{3}{4} A/A}$$

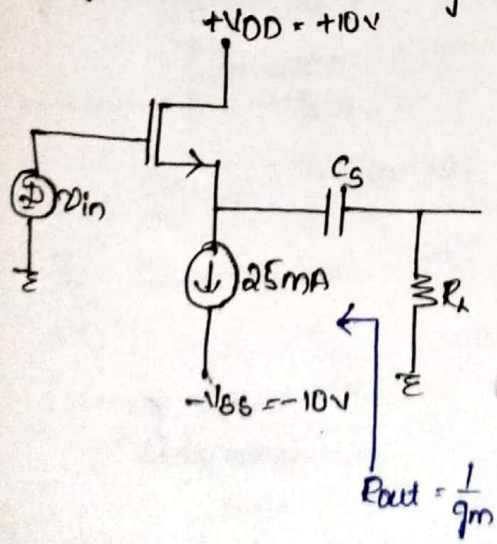
Assignment

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* Repeat the above problem for $I = 25 mA$

$\mu_n C_{ox} = 1mA/V^2$, $V_{tn} = 1V$, $\frac{W}{L} = 4$, $\lambda = 0$

$v_{in} = 0.5 \sin \omega t$ volts.



By observation:

$I_{DQ} = 25 mA$

$V_{DQ} = 10V$, $V_{GQ} = 0V$

$V_{DQ} > V_{GQ}$

$\Rightarrow$ Saturation.

i, Max. power delivered to R_L when $R_L = R_{out}$

$$R_L = R_{out} = \frac{1}{g_m} = \frac{1}{\sqrt{2 \times \mu_n C_{ox} \frac{W}{L} I_{DQ}}}$$

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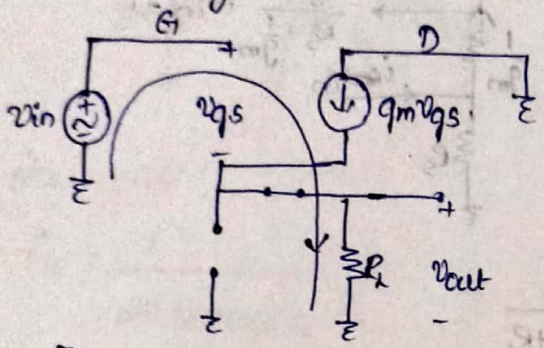
$$R_L = \frac{1}{\sqrt{2 \times 1m \times 4 \times 25m}} = \frac{1}{\sqrt{200 \times m^2}} = \frac{1}{10\sqrt{2}} = 0.070\,k\Omega$$

$\Rightarrow$ Max. power when $R_L = R_{out} = 0.070\,k\Omega$.

(ii) Max power delivered in $R_L = \frac{v_{out\,rms}^2}{R_L}$

We have to find $v_{out\,rms} = \frac{v_{out}}{\sqrt{2}}$

AC analysis



$$-v_{in} + v_{gs} + g_m v_{gs} R_L = 0$$

$$v_{gs} = \frac{v_{in}}{1 + g_m R_L}$$

$$v_{out} = g_m v_{gs} R_L$$

$$v_{out} = \frac{g_m \cdot R_L}{1 + g_m R_L} \cdot v_{in}$$

$$v_{out} = \frac{14.14m\,(0.070K)}{1 + 14.14m\,(0.070K)} \cdot v_{in}$$

$$v_{out} = 0.419\, v_{in}.$$

$$v_{out}(t) = 0.49\, v_{in}(t)$$

$$v_{out} = 0.419 \times 0.5 \sin\omega t$$

$$v_m = 0.248$$

$$v_{out\,rms} = \frac{v_m}{\sqrt{2}} = \frac{0.248}{\sqrt{2}}$$

$\Rightarrow v_{out\,rms} = 0.175$

Now,

Max power $= \frac{v_{out\,rms}^2}{R_L}$

$= \frac{(0.175)^2}{0.070K}$

$= 0.414\,mW$

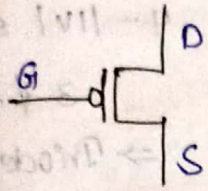
$\Rightarrow$ Max. Power $= 0.414\,mW$

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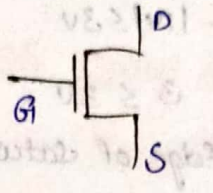
Assignment

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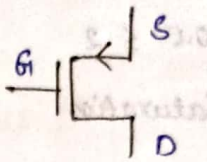
1. Among the following symbols which are nMOS and pMOS. Indicates the terminals also.

a) 

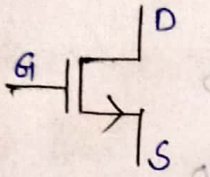
PMOS

b) 

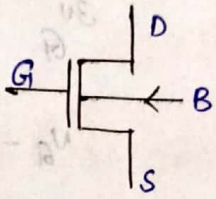
NMOS

c) 

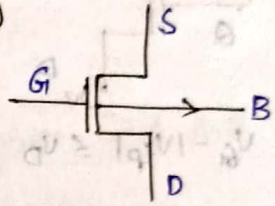
PMOS

d) 

NMOS

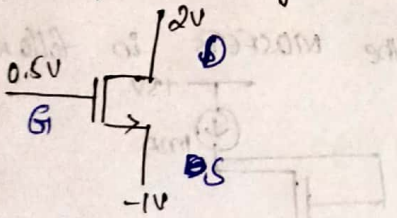
e) 

NMOS

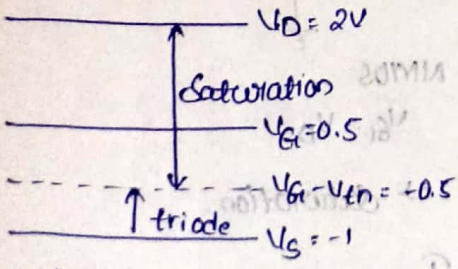
f) 

PMOS

2. For the following MOSFETS mark the terminals and find region of operation. Given $V_{tn} = 1V$ and $V_{tp} = 1V$.

i) 

NMOS

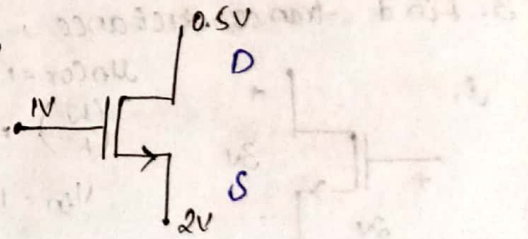


$V_G - V_{tn} \leq V_D$

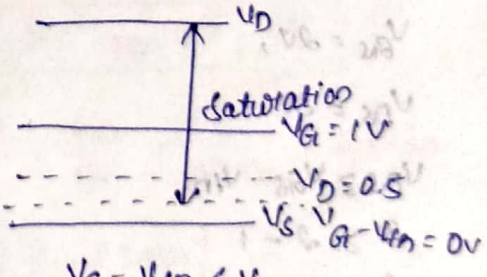
$0.5 - 1 \leq 2$

$-0.5 \leq 2$

$\Rightarrow$ Saturation.

ii) 

NMOS

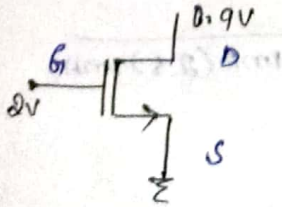


$V_G - V_{tn} \leq V_D$

$1 - 1 \leq 0.5$

$0 \leq 0.5$

$\Rightarrow$ saturation.

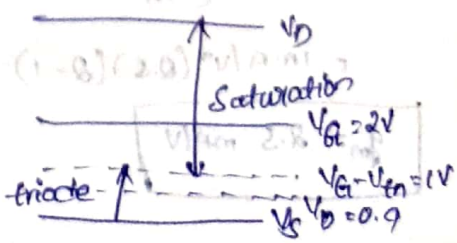
iii) 

$V_G - V_{tn} \geq V_D$

$2 - 1 \geq 0.9$

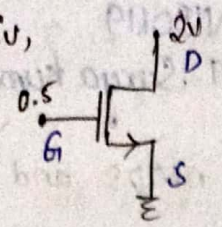
$1 \geq 0.9$

$\Rightarrow$ triode.



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(iv)



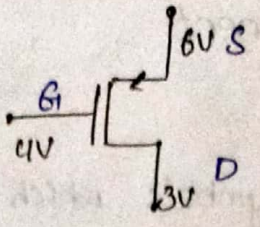
$V_G - V_{tn} \le V_D$

$0.5 - 1 \le 2$

$-0.5 \le 2$

⇒ Saturation

(v)



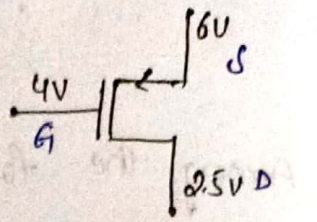
$V_G - |V_{tp}| \le V_D$

$4V - |1V| \le 3V$

$3 \le 3V$

⇒ Edge of saturation.

(vi)



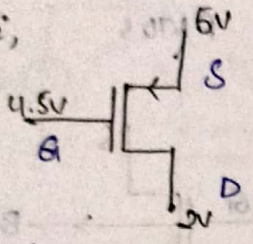
$V_G - |V_{tp}| \le V_D$

$4 - |1V| \le 2.5$

$3 \nleq 2.5$

⇒ Triode.

(vii)



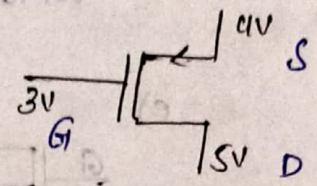
$V_G - |V_{tp}| \le V_D$

$4.5 - |-1| \le 2V$

$3.5 \nleq 2V$

⇒ triode

(viii)



$V_G - |V_{tp}| \le V_D$

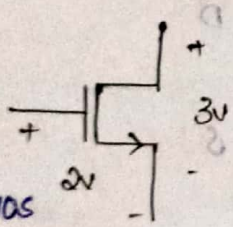
$3 - |-1| \le 5V$

$2 \le 5V$

⇒ Saturation.

3. Find transconductance, g_m of the MOSFETs in following

(i)



NMOS

$\mu_n C_{ox} = 1\ mA/V^2$

$\left(\frac{W}{L}\right) = 2.5$

$V_{tn} = 1V$

$V_{GS} = 2V,$

$V_{DS} = 3V$

$V_{DS} \ge V_{GS} - V_{tn}.$

$3 \ge 2 - 1$

$3 \ge 1$

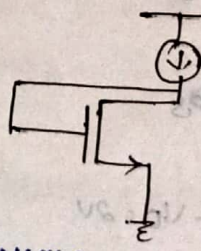
⇒ Saturation.

Now,

$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{GSQ} - V_{tn})$

$= 1mA/V^2 (2.5)(2-1)$

$\boxed{g_m = 2.5\ mA/V}$



NMOS

$V_G = V_D$

⇒ Saturation.

$I_{DQ} = 1mA$

Now,

$g_m = \sqrt{2 \mu_n C_{ox} \left(\frac{W}{L}\right)_n I_{DQ}}$

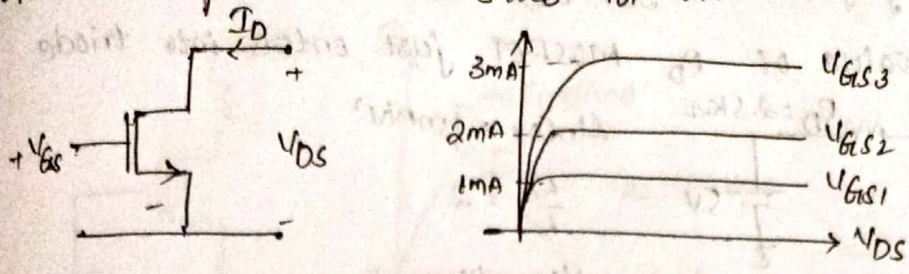
$= \sqrt{2 \times 1mA (2.5) 1mA}$

$g_m = 5$

$\boxed{g_m = 2.23}$

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4. The output characteristics for the MOSFET is shown



which is correct?

A) $V_{GS1} > V_{GS2} > V_{GS3}$

B) $V_{GS1} < V_{GS2} < V_{GS3}$

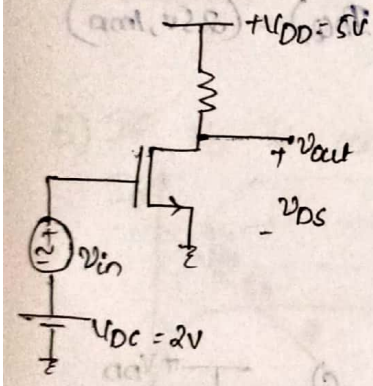
C) $V_{GS1} > V_{GS2} < V_{GS3}$

D) $V_{GS1} < V_{GS2} > V_{GS3}$

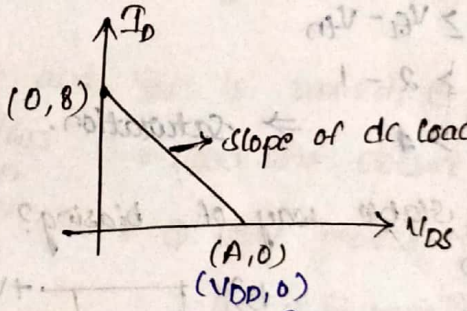
Sol:- Option B

$V_{GS1} < V_{GS2} < V_{GS3}$

5) The load line chart's for below circuit is given. Find A, B and slope of dc load line.



$\mu_n C_{ox} = 1mA/V^2$, $\lambda = 0$, $\frac{W}{L} = 2$, $V_{th} = 1V$



$V_{DD} = 5V$

$V_{DS} = V_{DD} - I_D R_D$

$I_D = -\frac{1}{R_D} V_{DS} + \frac{V_{DD}}{R_D}$

$y = mx + c$

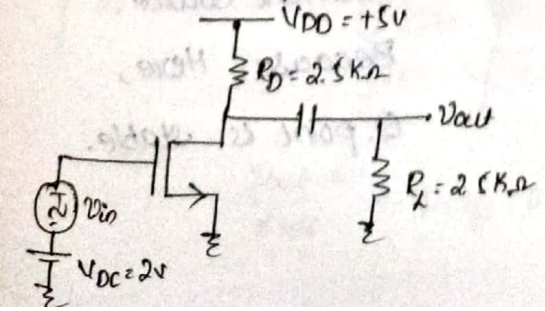
$\Rightarrow$ **$A = V_{DD} = 5V$**

$B = \frac{V_{DD}}{R_D} = \frac{5}{2.5k} = 2.5mA$

Slope $= -\frac{1}{R_D} = -\frac{1}{2.5k} = 0.4mA$

$B = 2.5mA$

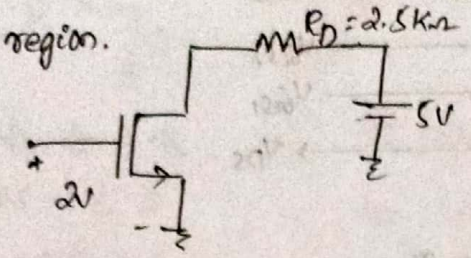
6. Draw loadline for the circuit below. Find slope of ac load line and slope of dc loadline.



I_D

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7. Find operating point, $Q(V_{DQ}, I_{DQ})$ for the MOSFET shown below.
At which value of R_D MOSFET just enters into triode region.



$\mu_n C_{ox} = 1 mA/V^2$

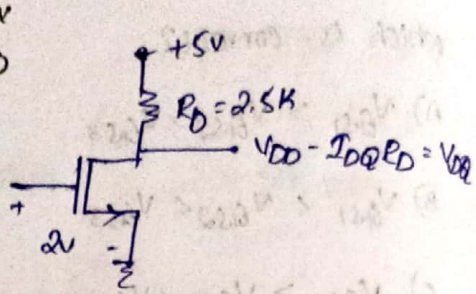
$\frac{W}{L} = 2$

$V_{tn} = 1V$

$\lambda = 0$

NMOS:

By observation, $V_{GS} = 2V$



Assume it is saturation.

$\Rightarrow I_{DQ} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS} - V_{tn})^2$

$= \frac{1}{2} \times 1m \times 2\,(2-1)^2$

$\boxed{I_{DQ} = 1mA}$

$\Rightarrow V_{DQ} = 5 - 1m(2.5k)$

$= 5 - 2.5$

$\boxed{V_{DQ} = 2.5V}$

$\therefore$ Q. Point : $(V_{DQ}, I_{DQ}) = (2.5V, 1mA)$

check:-

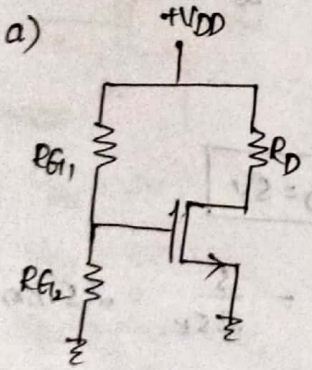
$V_D \geq V_G - V_{tn}$

$2.5 \geq 2 - 1$

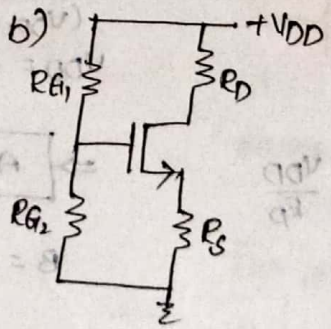
$2.5 > 1$ $\Rightarrow$ saturation.

8. Which is stable way of biasing?

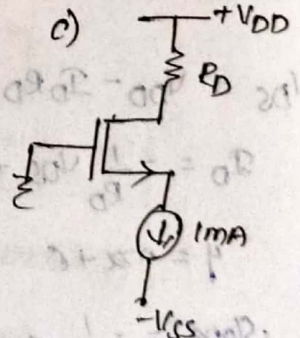
a)



b)



c)



If $I_{DQ} \uparrow$, -ve feedback is present.

If $I_{DQ} \downarrow$, No -ve feedback.

Bad way of biasing

c) is the Best way.

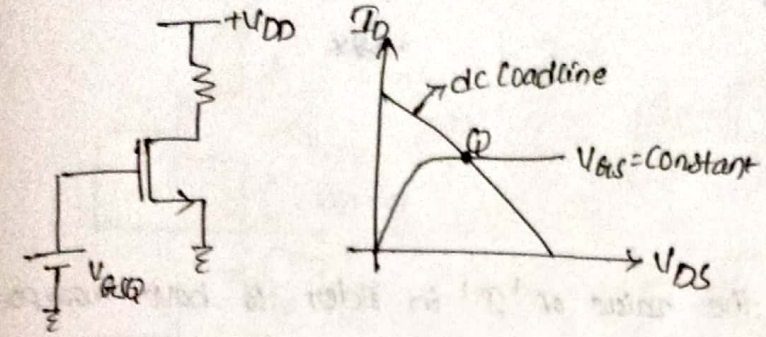
Biasing Using constant current source.

Because Here,

Q. point is stable.

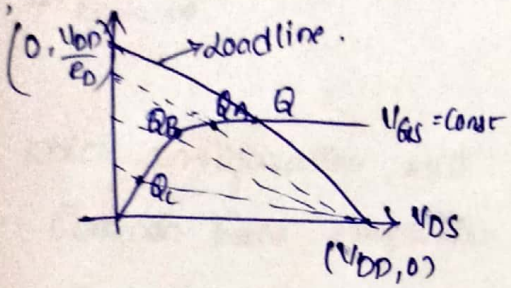
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9. Consider the circuit below



A) If R_D is varied and V_{GS} = constant. Q. Point will move on.

i,



Q. Point will move from

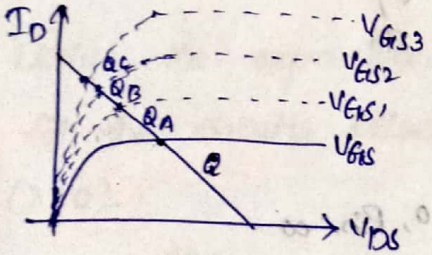
$Q \longrightarrow Q_A \longrightarrow Q_B \longrightarrow Q_C$

↓

(Edge of saturation)

ii, load line Eqn. $I_D = -\frac{1}{R_D} V_{DS} + \frac{V_{DD}}{R_D}$ * load line changes.

B) If R_D is constant and V_{GS} is varied, Q point will move



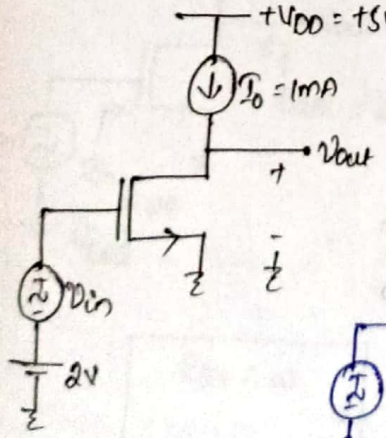
* load line doesn't change

* Q. Point moves from

$Q \longrightarrow Q_A \longrightarrow Q_B \longrightarrow Q_C$

Saturation Triode

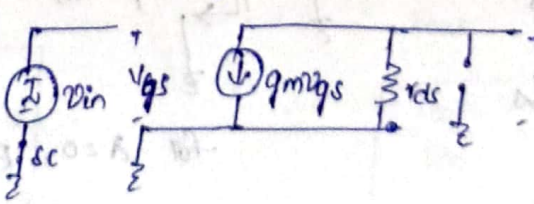
10. The intrinsic gain for amplifier below is -5 v/v. Calculate r_{ds}.



Intrinsic gain: max. possible voltage gain.

$A_v = -5$ v/v

Small signal Model



KVL: $v_{in} = v_{gs}$

KCL: $\frac{v_{out}}{r_{ds}} + g_m v_{gs} = 0 \Rightarrow \frac{v_{out}}{r_{ds}} = -g_m v_{gs}$

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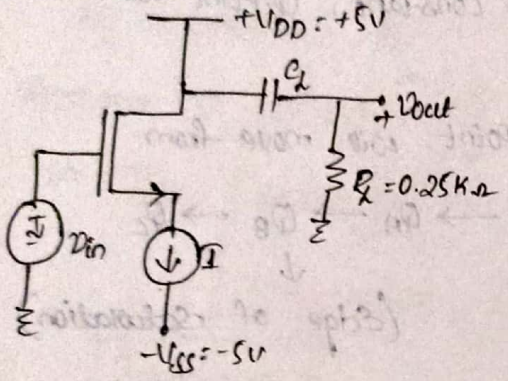
$$\frac{v_{out}}{v_{in}} = -g_m r_{ds}$$

$$5 = -g_m r_{ds}$$

$$r_{ds} = \frac{-5}{g_m}$$

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) I_{DQ}}$$

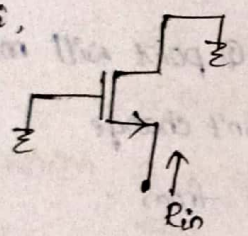
11. What should be the value of 'I' in order to have max. power dissipation in load R_L.



$\mu_n C_{ox} = 1\,mA/V^2$, $V_{tn} = 1V$, $\frac{W}{L} = 8$, $\lambda = 0$

12. Find small signal resistance for circuits below. for both $\lambda = 0$, $\lambda \neq 0$.

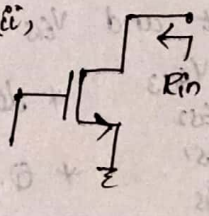
i,



for $\lambda = 0$, $R_{in} = \frac{1}{g_m}$

$\lambda \neq 0$, $R_{in} = \frac{1}{g_m} // r_{ds}$

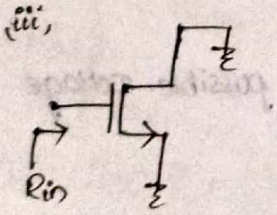
ii,



for $\lambda = 0$, $R_{in} = \infty$

$\lambda \neq 0$, $R_{in} = r_{ds}$

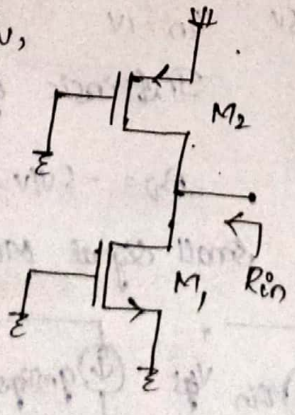
iii,



for $\lambda = 0$, $R_{in} = \infty$

$\lambda \neq 0$, $R_{in} = \infty$

iv,



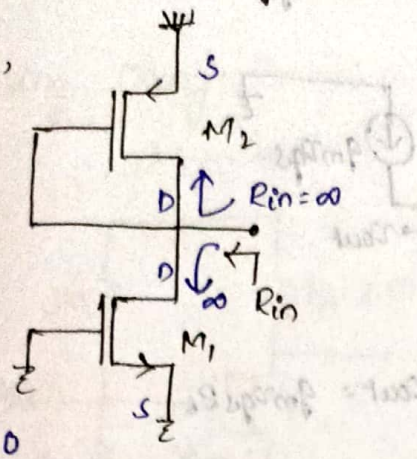
for $\lambda = 0$, $R_{in} = \infty$

$\lambda \neq 0$, $R_{in} = r_{ds}$

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13. Find small signal Resistance for circuits below. $\lambda = 0$

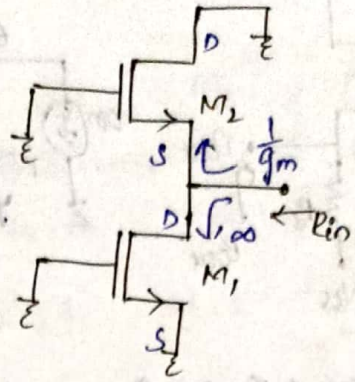
i,



$\lambda = 0$

$\Rightarrow R_{in} = \infty$

ii,



$\Rightarrow R_{in} = \frac{1}{g_m} \parallel \infty$

$\Rightarrow R_{in} = \frac{1}{g_m}$

14. Which configuration will give least small signal i/p resistance?

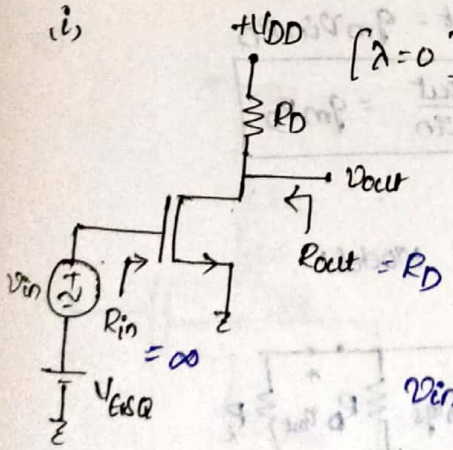
A. Common Gate Amplifier will give least i/p res. at Source terminal.

15. Which configuration will give least small signal O/P resista?

A. Common Drain Amplifier. (at Source terminal)

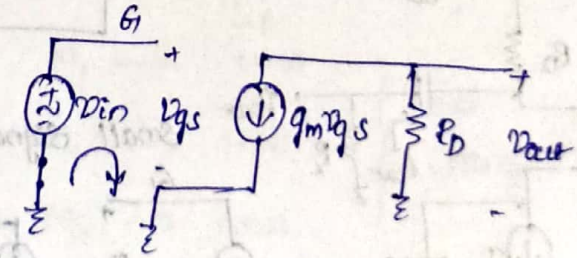
16. Derive the expression for small voltage gain, ($A_V = \frac{v_{out}}{v_{in}}$) for the circuits below. Name the type of Configaration. ($\lambda = 0$).

i,



$[\lambda = 0]$

Small signal voltage gain:



$v_{in} = v_{gs}$

$v_{out} = -g_m v_{gs} R_D$

$v_{out} = -g_m v_{in} R_D$

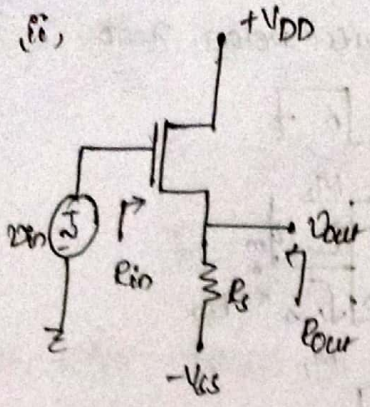
$R_{in} = \infty$

$R_{out} = R_D$

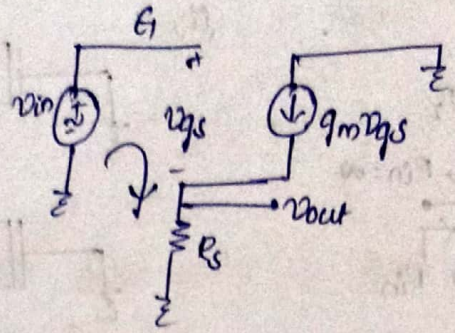
$\frac{v_{out}}{v_{in}} = -g_m R_D$

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(ii)



$R_{in} = \infty$, $R_{out} = \frac{1}{g_m} \,//\, R_S$



$-V_{in} + V_{gs} + V_{out} = 0$

$V_{gs} = V_{out} + V_{in}$

$-V_{in} + V_{gs} + g_m V_{gs} R_S = 0$

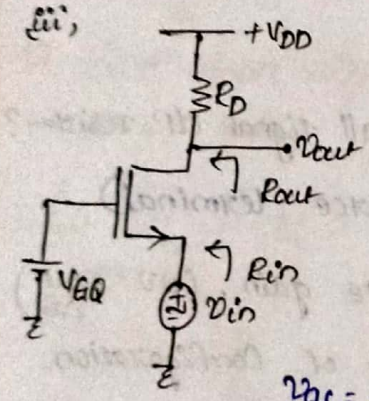
$V_{gs} = \frac{V_{in}}{1 + g_m R_S}$

$V_{out} = g_m V_{gs} R_S$

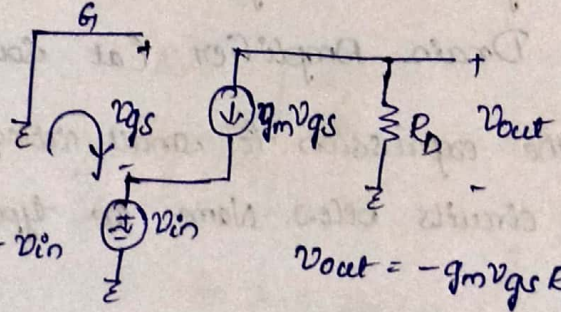
$V_{out} = g_m \cdot \frac{V_{in}}{1+g_m R_S} R_S$

$$A_V = \frac{V_{out}}{V_{in}} = \frac{g_m R_S}{1 + g_m R_S}$$

(iii)



$R_{in} = \frac{1}{g_m}$, $R_{out} = R_D$



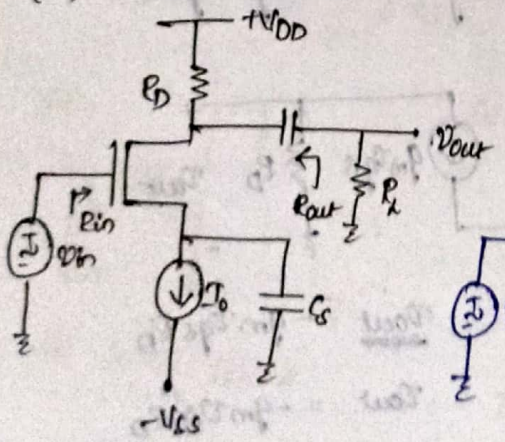
$V_{gs} = -V_{in}$

$V_{out} = -g_m V_{gs} R_D$

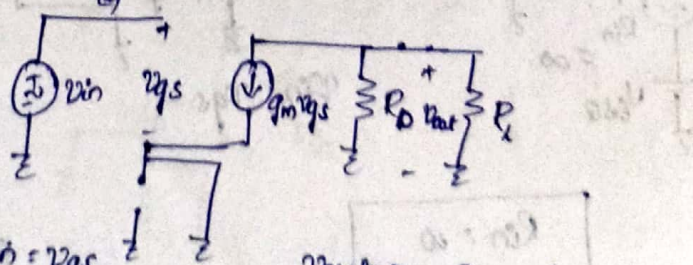
$V_{out} = g_m V_{in} R_D$

$$\Rightarrow \frac{V_{out}}{V_{in}} = g_m R_D$$

(iv)



Small signal Model:



$R_{in} = \infty$

$R_{out} = R_D$

$V_{in} = V_{gs}$

$V_{out} = -g_m V_{gs} (R_D \,//\, R_L)$

$V_{out} = -g_m V_{in} (R_D \,//\, R_L)$

$$A_V = \frac{V_{out}}{V_{in}} = -g_m (R_D \,//\, R_L)$$

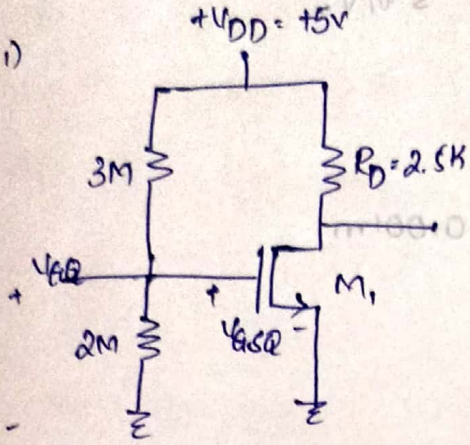
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Lab. - 1

Biasing Using Constant V_{GS}

1)



	M_1	M_2	M_3
Kp	$\mu_n C_{ox}$ = 1mA/V²	1.5	1mA/V²
Vto	V_{tn} = 1V	1V	1.1V
	$\frac{W}{L} = 2$	$\frac{W}{L} = 2$	$\frac{W}{L} = 2$

I_{DQ}

$M_1 \longrightarrow I_d = 0.001$ 1 mA

$I_G = -0.001$

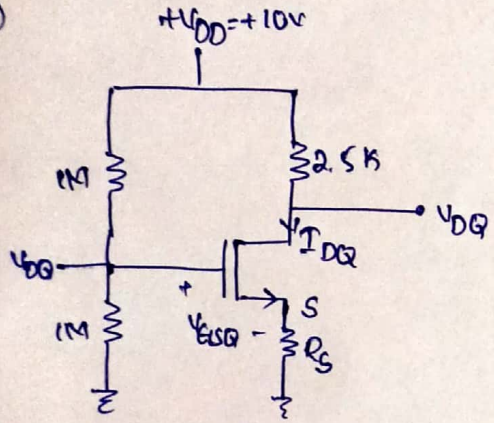
$M_2 \longrightarrow$ 1.5 mA

$M_3 \longrightarrow$ 0.8 mA

$V_{GSQ} = 2V = V_{GG}$

* $\mu_n C_{ox} \uparrow \Rightarrow I_{DQ} \uparrow$
* $V_{tn} \uparrow \Rightarrow I_{DQ} \downarrow$

2)



$V_{GSQ} = 5V = \frac{R_{G2}}{R_{G1}+R_{G2}} \cdot V_{DD}$

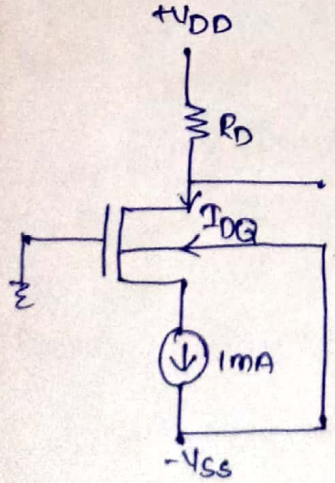
I_{DQ}

$M_1 \longrightarrow$ 1 mA.

$M_2 \longrightarrow$ 1.05 mA.

$M_3 \longrightarrow$ 0.97 mA.

3)



I_D

$M_1 \longrightarrow$ 1mA

$M_2 \longrightarrow$ 1mA

$M_3 \longrightarrow$ 1mA.

} No Change.

Here body should be connected to -Vss.

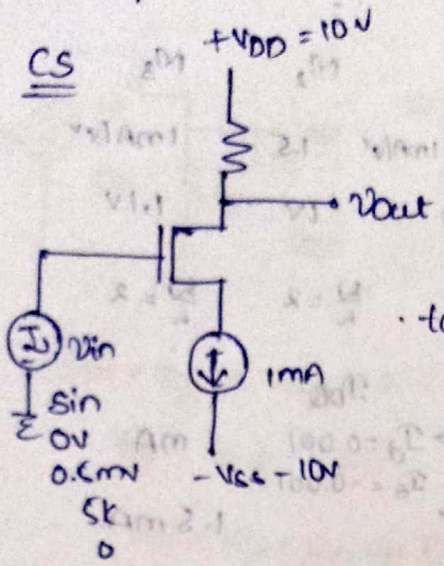
* Here $\Rightarrow$ Best Biasing.

* Voltage → branch
  Current → Node.
* NMOS body → least supply, PMOS body → highest supply. (∵ It should be in reverse bias not to flow i)

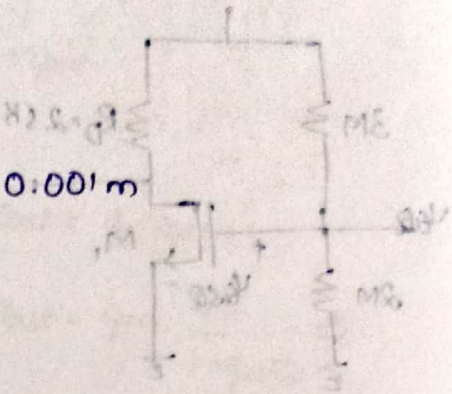
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Floating source.

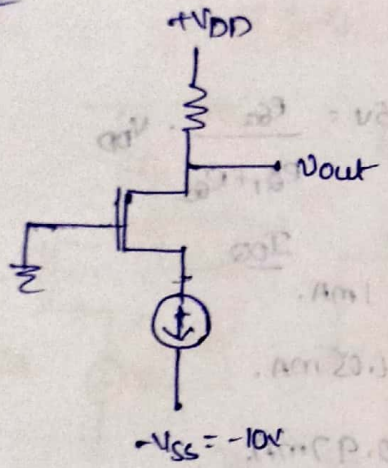
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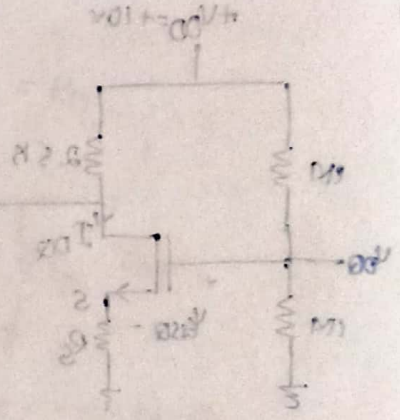


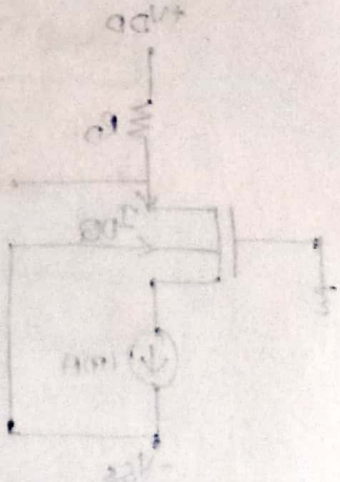
$\frac{V_{out}}{V_{in}} = 5\ V/V.$



CG





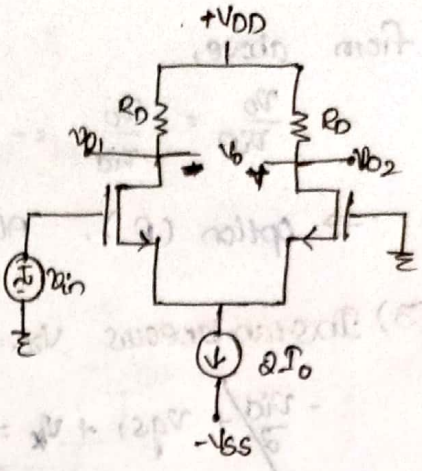


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Assignment

1. For the given circuit, if M_1 & M_2 are in saturation region. If small signal voltage gain $\frac{v_o}{v_{in}} = +10\,V/V$ then $\frac{v_{o1}}{v_{in}}$, $\frac{v_{o2}}{v_{in}}$ are ____, ____



~~$\frac{v_o}{v_{in}} = \frac{v_{o1}}{v_{in}}$~~

$v_{o1} = V_{DD} - I_D R_{D1}$ $\quad v_{o2} = V_{DD} - I_D R_{D2}$

$= -(V_{DD} - I_D R_D)$ $\quad = V_{DD} - I_D R_D$

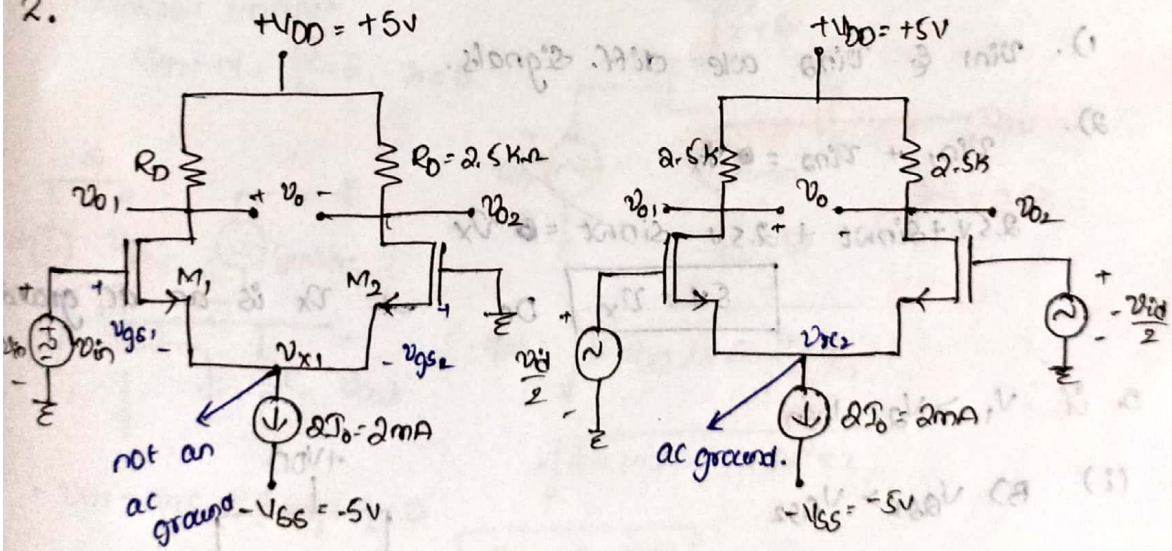
$= -x$ $\quad = x$

$v_o = v_{o2} - (v_{o1}) = x - (-x) = 2x$

$10 = 2x \Rightarrow x = 5 \Rightarrow \frac{v_{o1}}{v_{in}} = -5\,V/V, \quad \frac{v_{o2}}{v_{in}} = 5\,V/V.$

A) option (B)

2.



$\Downarrow$

$-v_{in} + v_{gs1} - v_{gs2} = 0$

$v_{gs1} - v_{gs2} = v_{in}$ $\quad$ **$v_{gs1} = -v_{gs2}$**

in above fig,

$v_{id} = v_{in}$

In as we know, $v_{gs1} = \frac{v_{id}}{2}$, $v_{gs2} = -\frac{v_{id}}{2}$

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$$\frac{v_{o1}}{v_{in}} = \frac{v_{o1}}{v_{id}} = \frac{-g_m R_D}{2} \quad ; \quad \frac{v_{o2}}{v_{in}} = \frac{v_{o2}}{v_{id}} = \frac{g_m R_D}{2}$$

from above,

$$\frac{v_o}{v_{in}} = \frac{v_o}{v_{id}} = -g_m R_D$$

⇒ option (f). All the above.

(3) Instantaneous v_x.

$$-\frac{v_{id}}{2} + v_{gs1} + v_x = 0$$

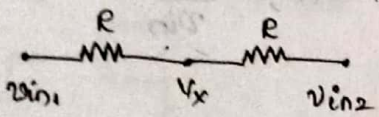
$$-\left(\frac{v_{id}}{2}\right) + v_{gs2} + v_x = 0$$

$$(v_{gs1} + v_{gs2}) + v_x = 0$$

($v_{gs1} + v_{gs2} \to 0$)

$$\boxed{v_x = 0}$$

⇒ option A. (0V)

4. 

$v_{in1} = 2.5V + \sin\omega t$

$v_{in2} = 2.5V - \sin\omega t$

1). v_{in1} & v_{in2} are diff. signals.

2).

$v_{in1} + v_{in2} = v_x$

$2.5V + \sin\omega t + 2.5V - \sin\omega t = v_x$

$\boxed{5V = v_x}$ DC ⇒ v_x is an ac ground.

5. if $V_1 > V_2$ then

(i) B) $V_{GS1} > V_{GS2}$

ii, A) $i_{D1} > i_{D2}$

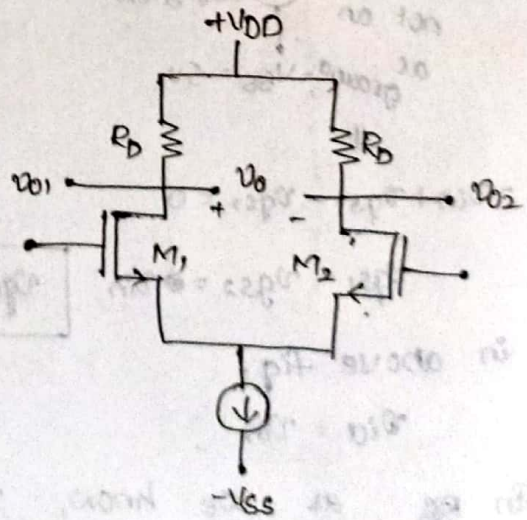
iii, B) $v_{o1} < v_{o2}$

iv, as $v_{o1} < v_{o2}$

$v_o = v_{o1} - v_{o2}$

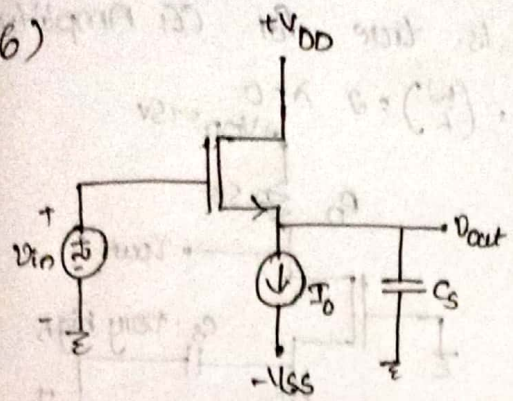
⇒ $v_o < 0$

A) $v_o < 0$



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(6)

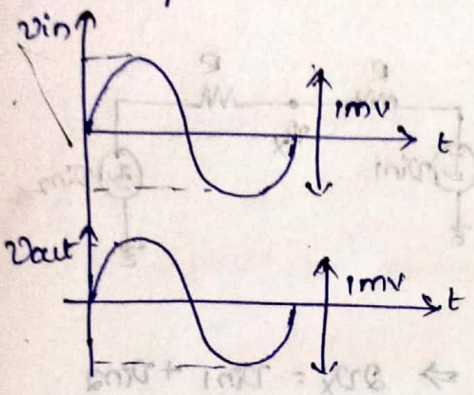


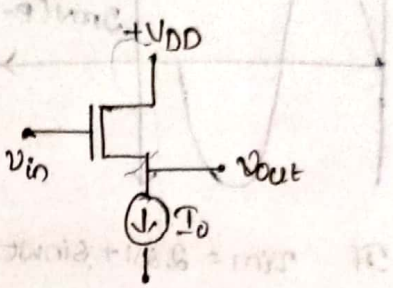
$\frac{V_{out}}{V_{in}} = 1$

(Voltage Buffer).

(7) for CD Amplifier:-

CD Amplifier is same phase

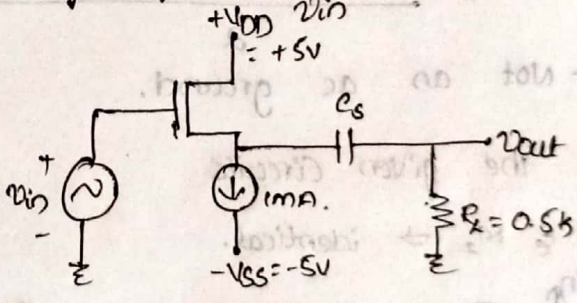


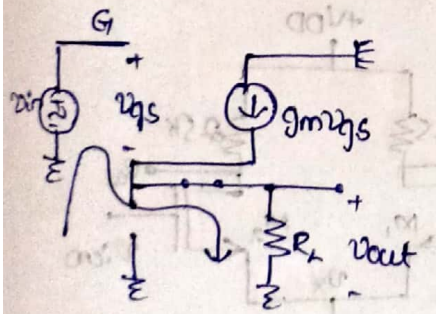


(8) Find small signal voltage gain $\frac{V_{out}}{V_{in}} = ?$

$\mu_n C_{ox} = 1mA/V^2$

$V_{th} = 1V$, $\frac{W}{L} = 2$, $\lambda = 0$





$-V_{in} + V_{gs} + g_m V_{gs} R_L = 0$

$V_{in} = V_{gs}(1 + g_m R_L)$

$$V_{gs} = \frac{V_{in}}{1 + g_m R_L}$$

$$g_m = \sqrt{2 I_{DQ} \mu_n C_{ox} \left(\frac{W}{L}\right)_n}$$

$$= \sqrt{2 \times 1mA \times 1mA/V^2 \times 2}$$

$$g_m = 2mA/V$$

$-V_{out} + g_m V_{gs} R_L = 0$

$$V_{out} = g_m \cdot \frac{V_{in}}{1 + g_m R_L} \cdot R_L$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = \frac{g_m R_L}{1 + g_m R_L} = \frac{2 \times 1/2}{1 + 2 \times \frac{1}{2}} = \frac{1}{2} V/V.$$

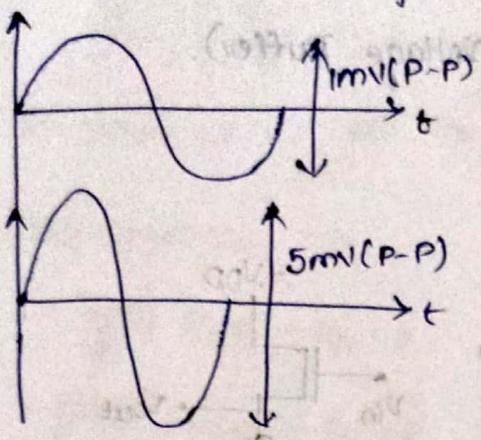
$\Rightarrow$ gain becomes half.

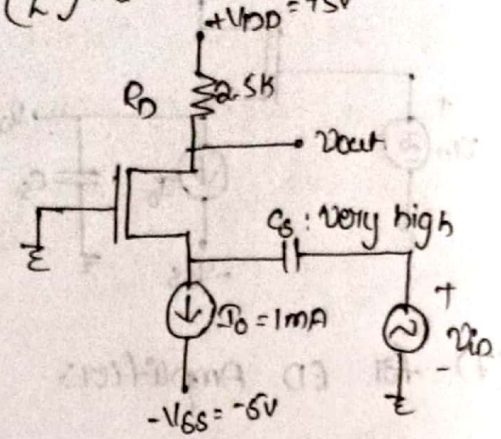
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(9) Which of the following graph is true for CG Amplifier.

given $\mu_n C_{ox} = 1\,mA/V^2$, $V_{tn} = 1V$, $\left(\frac{W}{L}\right) = 2$ $\lambda = 0$

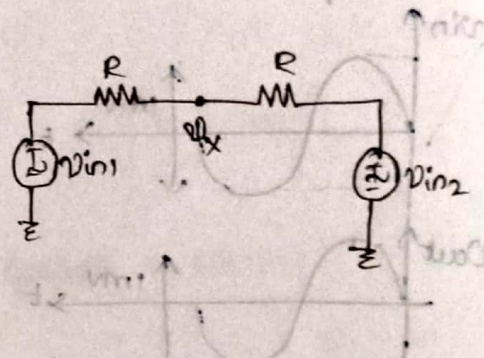
CG Amplifier $\Rightarrow$ 0° phase.





(10) If $v_{in1} = 2.5V + \sin\omega t\ (mV)$

$v_{in2} = 2.5V + \sin\omega t\ (mV)$



Nodal @ v_x

$$\frac{v_x - v_{in1}}{R} + \frac{v_x - v_{in2}}{R} = 0 \Rightarrow 2v_x = v_{in1} + v_{in2}$$

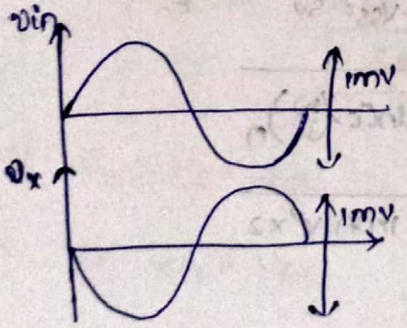
$$v_x = \frac{2.5 + \sin\omega t + 2.5 + \sin\omega t}{2} = \frac{5 + \sin\omega t}{2}$$

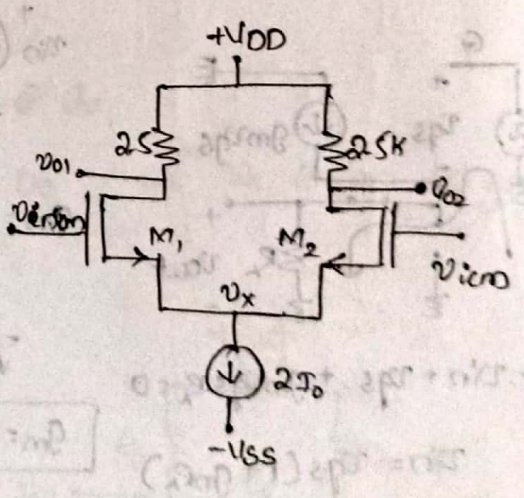
$\Rightarrow$ Not an ac ground.

(11) For the given circuits

M_1 & M_2 $\Rightarrow$ identical.

i,





ii, $\frac{v_{o1}}{v_{icm}} = \frac{v_{o1}}{v_{icm}} = 0$

(12)

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