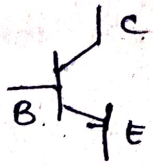
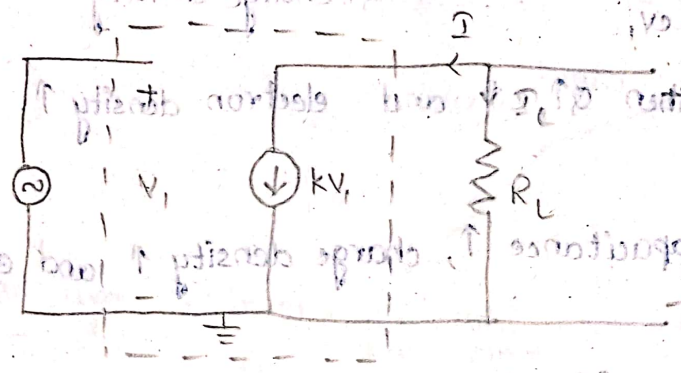
MOSFET

Ac equivalent circuit → Small signal model
→ large signal model



* If applied voltage is in mv, then it is called as small signal model.
* If applied voltage is in terms of volts (2V, 3V), then it is called as large signal model.

Let us build an amplifier



Equivalent circuit of transistor

from the circuit,

$I + I_L = 0$

$kV_i + \frac{V_o}{R_L} = 0$

$\frac{V_o}{R_L} = -kV_i$

$V_o = -kV_i R_L$

$V_{in} = V_i$

$V_o = -kV_{in} R_L$

-ve sign represents out of phase

K: constant (or) amplification factor

* MOSFET is a voltage dependent current source.

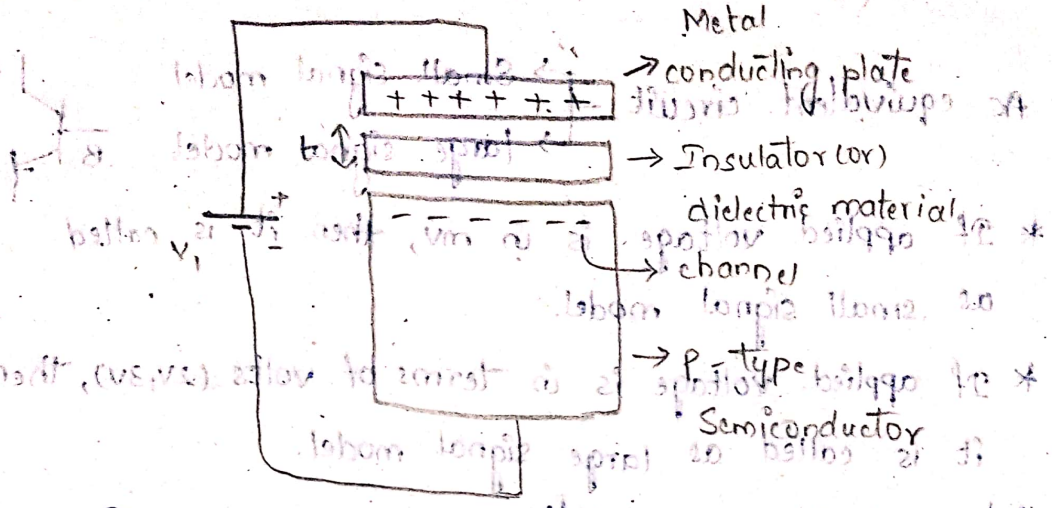
High input impedance device

Resistance = $10^{12} - 10^{15}\ \Omega$

infinity (ideally)

Zero current in MOSFET

MOSFET as a capacitor application:



case ①: If $V_1 \uparrow$

$Q = CV_1$ Q: charge density

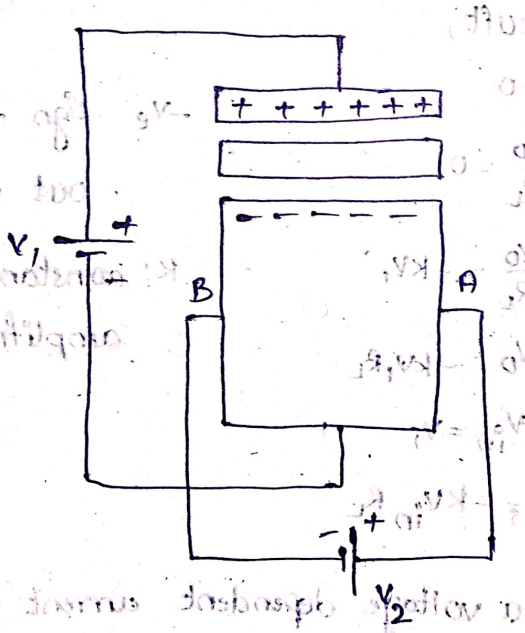
If $V_1 \uparrow$ then $Q \uparrow$, $C \uparrow$ and electron density $\uparrow$.

case ②:

If $t \downarrow$, capacitance $\uparrow$, charge density $\uparrow$ and electron density $\uparrow$.

$$C = \frac{\varepsilon A}{d}$$ here $d = t$ (thickness)

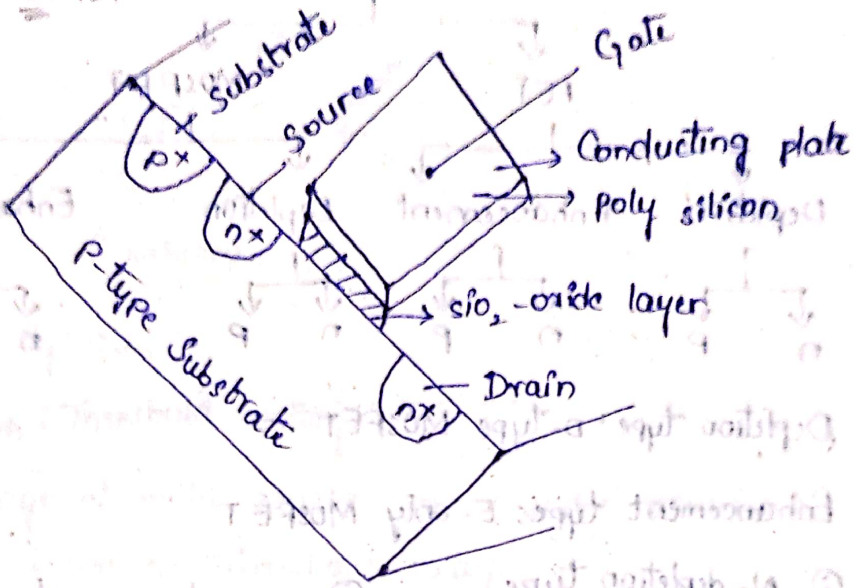
case ③:



If $V_1 \uparrow$ then charge density increases in metal and also electron density increases in P-type semiconductor. Then the current between A and B $\uparrow$ and resistance $\downarrow$.

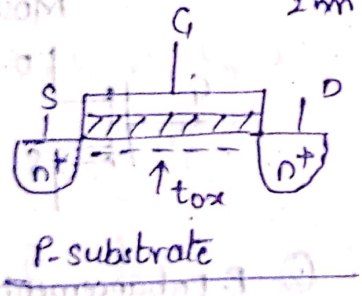
e^- moves from B to A and current from A to B. Because of applied voltage V_i, current is controlled. Therefore it is voltage dependent current control device.

MOS structure:



* Oxide layer thickness - 15A° - 18A°
  2nm - 50nm

$C = \frac{\varepsilon A}{t_{ox}}$

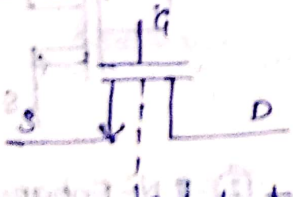


Oxide capacitance - capacitance per unit area

$C_{ox} = \frac{C}{A} = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}}$

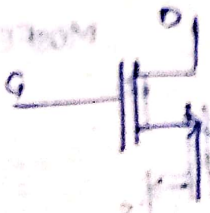
* MOSFET is a four terminal (Gate, drain, source, substrate), symmetrical device.

*

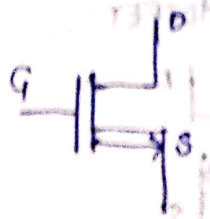


⇒ Symbol of MOSFET

≃

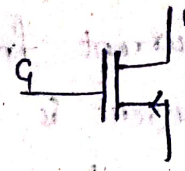


≃



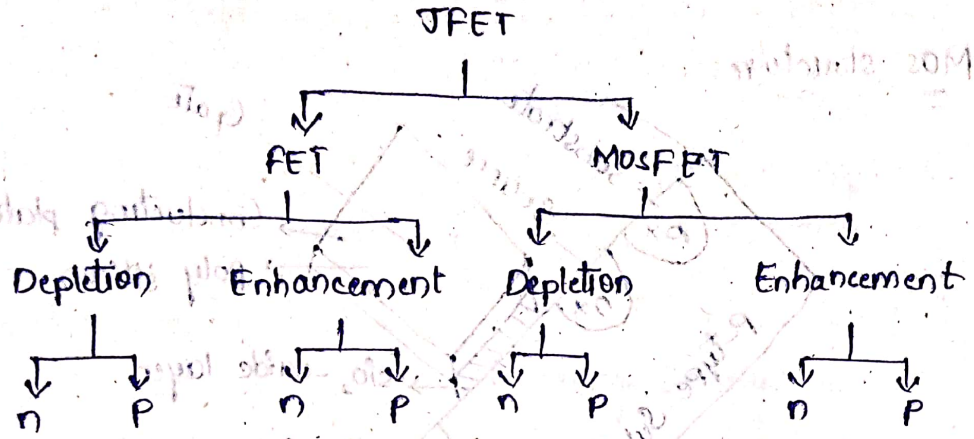
N channel enhancement type MOSFET

*



P-channel enhancement type MOSFET.

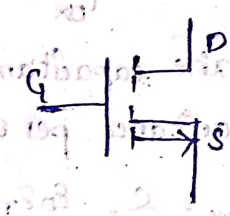
classification:



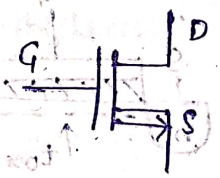
Depletion type: D-type MOSFET

Enhancement type: E-only MOSFET

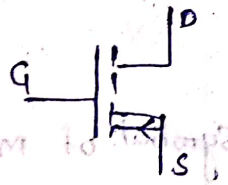
① N-depletion type MOSFET



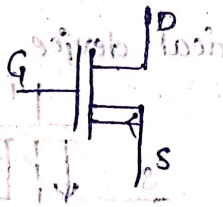
② N-Enhancement type MOSFET



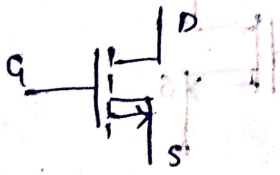
① P-depletion type MOSFET



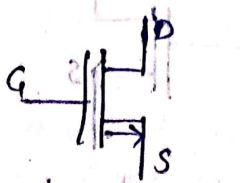
② P-Enhancement type MOSFET



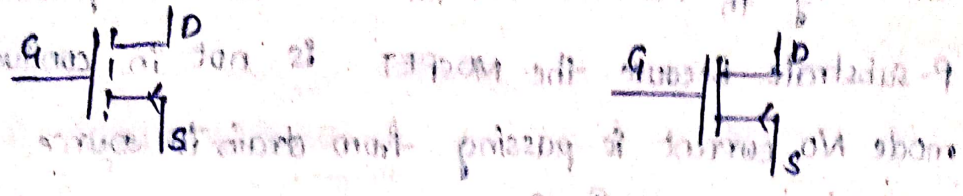
① N-depletion type MOSFET



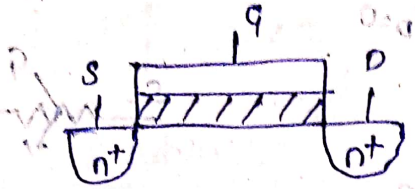
② N-Enhancement type MOSFET



① P-depletion type MOSFET ② P-Enhancement type MOSFET



MOS operation:



P-substrate

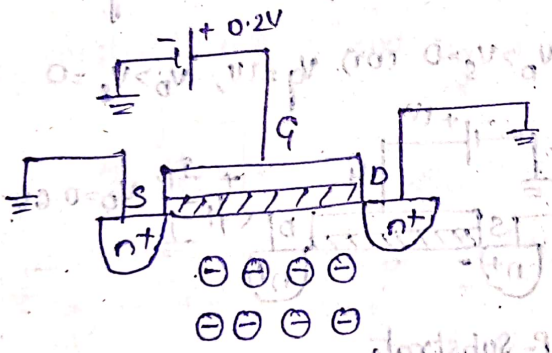
Case ①: $V_g = 0.2V$

V_{Th} : Threshold voltage

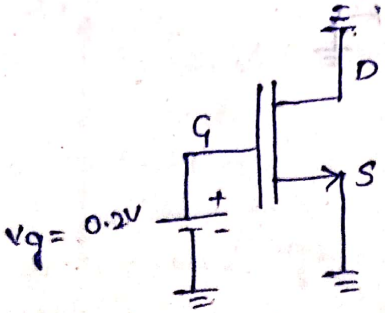
The voltage at which MOSFET comes under conduction mode is called as Threshold voltage.

$V_{th} = 1V$

$V_g = 0.2V$, $V_S = 0V$, $V_D = 0$



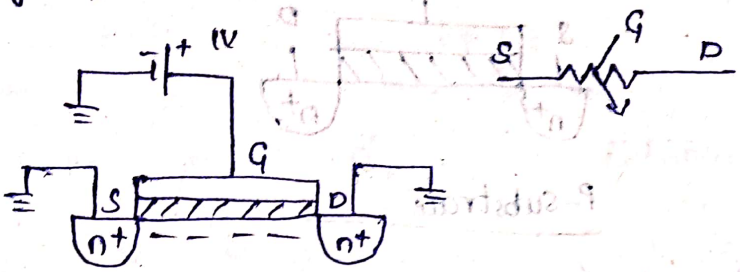
P-substrate

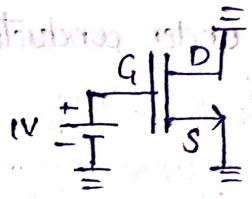


channel is not created between source and drain. since $V_g < V_{th}$. More no. of immobile ions are present in P-substrate because the MOSFET is not in conduction mode. No current is passing from drain to source.

$I_D = 0$

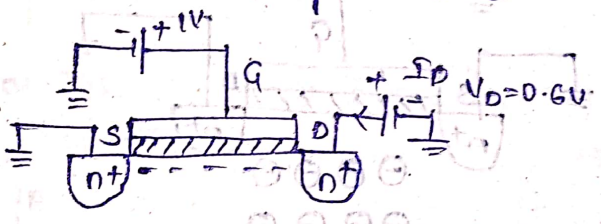
Case (2): $V_g = V_{th}$, $V_S = 0$, $V_D = 0$

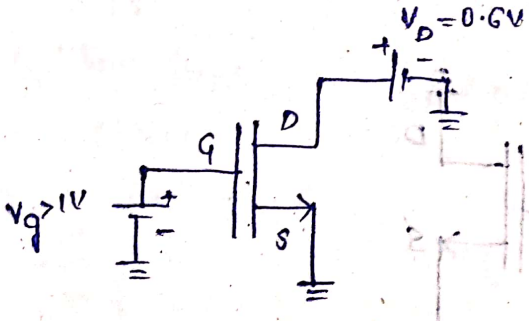




channel is created from source to drain. MOSFET comes under conduction mode. current is zero ($I_D = 0$). since drain is grounded.

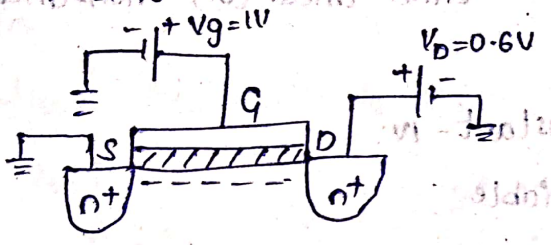
Case (2): $V_g > V_{th}$, $V_D > V_S = 0$ (or) $V_g = 1V$, $V_D > V_S = 0$

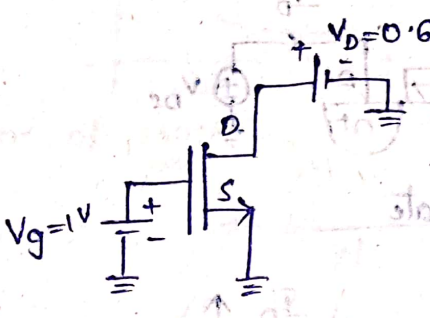




MOSFET is in conduction mode. channel is created from source to drain and current flows from drain to source.

Case (4): $V_g = 1V$, $V_D > V_S = 0$

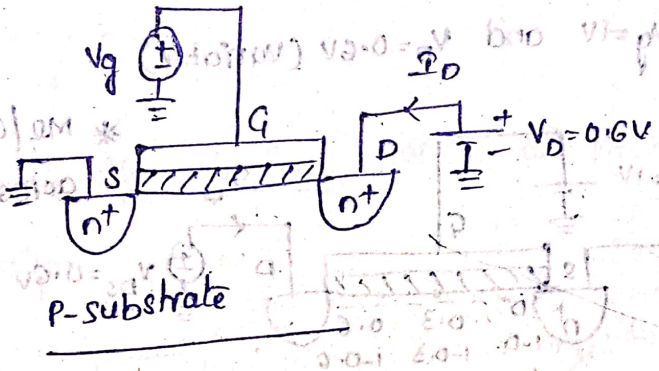


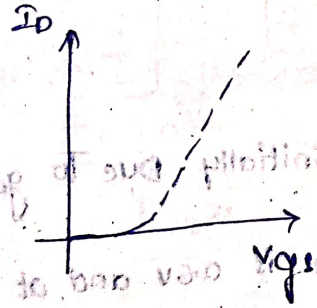


MOSFET is in conduction mode. channel is created from source to drain. Current flows from drain to source

Case (5): $V_g > V_{th}$, $V_D > V_S = 0$

case (1): V_D - constant = 0.6V and V_g - variable





may be linear / non-linear variations,

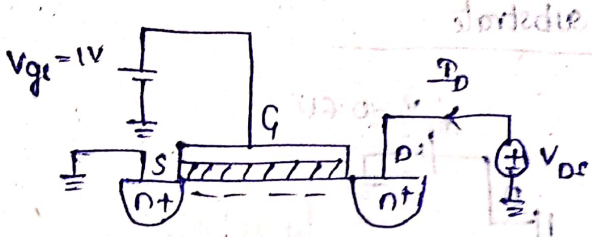
① If $V_g = 0$ and it is not in conduction mode until it reaches to V_{th}.

② If we increase gate voltage to more than V_{th} then we can observe either linear (or) non-linear variations.

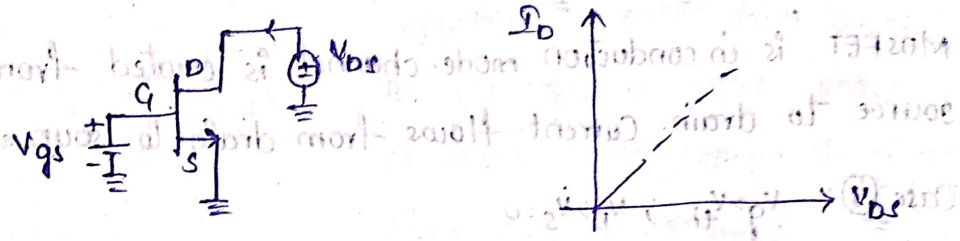
Case II:

V_g - constant - 1V

V_D - Variable



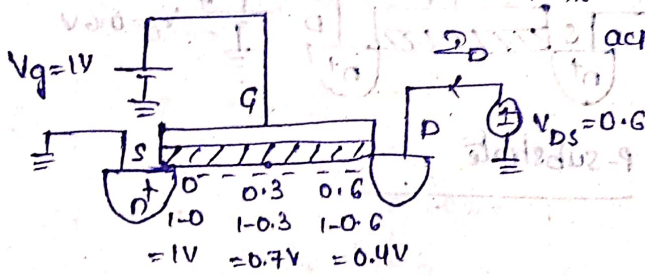
P-type Substrate



may be linear (or) non-linear increment

Case ⑥: V_g = 1V and V_D = 0.6V (variable)

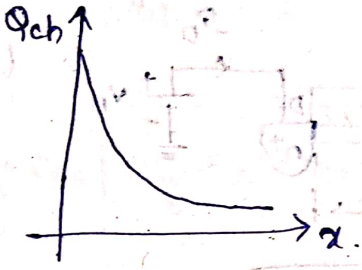
* MΩ/GΩ resistance across gate
∴ Current = 0



P- substrate

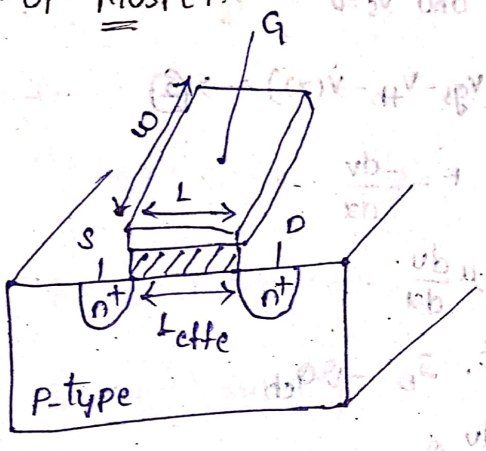
* Voltage at source is zero initially. Due to gate voltage it becomes 1V.
* At drain the initial voltage is 0.6V and at the middle it is less than 0.6V and greater than 0V.

* Let us consider 0.3V.
* Due to gate voltages, drain voltage becomes 0.4V.
* Therefore voltage increases from source to drain and electron density is more at source and minimum at drain.
* Current flows from drain to source



If V_{DS} ↑ then channel length decreases (channel length modulation)

Dimensions of MOSFET:

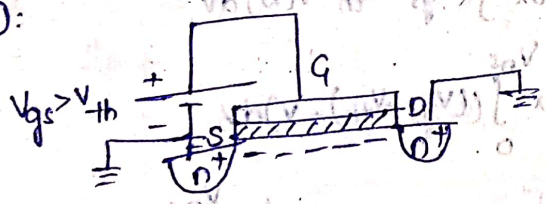


Gate area = L × W

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}}$$

Drain characteristics of the MOSFET (or) Drain current equation analysis:

Case ①:



$V_{gs} - V_{th}$ → overdrive voltage

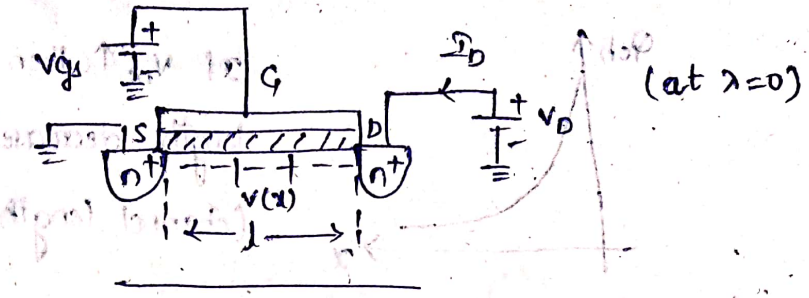
$V_{gs} > V_{th}$

$V_s, V_D = 0$

Q_{ch} Total = Gatearea $\times C_{ox}(V_{gs} - V_{th})$

Q_{ch} total $= WL\, C_{ox}(V_{gs} - V_{th})$

Case (2) :



$V_{gs} > V_{th}$, $V_D > 0$ and $V_s = 0$

$$Q_{ch} = W C_{ox}(V_{gs} - V_{th} - V(x)) \longrightarrow (2)$$

$$v = \mu E \qquad E = -\frac{dv}{dx}$$

$$v = -\mu \frac{dv}{dx}$$

Total drain current, $I_D = -v Q_{ch}$

$$I_D = \mu \frac{dv}{dx} Q_{ch}$$

$$I_D = \mu \frac{dv}{dx} W C_{ox}(V_{gs} - V_{th} - V(x))$$

$$I_D\, dx = \mu W C_{ox}(V_{gs} - V_{th} - V(x))\, dv$$

Integrating on both sides

$$\int I_D\, dx = \mu W C_{ox} \int (V_{gs} - V_{th} - V(x))\, dv$$

$$\int_0^L I_D\, dx = \mu W C_{ox} \int_0^{V_{DS}} ((V_{gs} - V_{th}) - V)\, dv$$

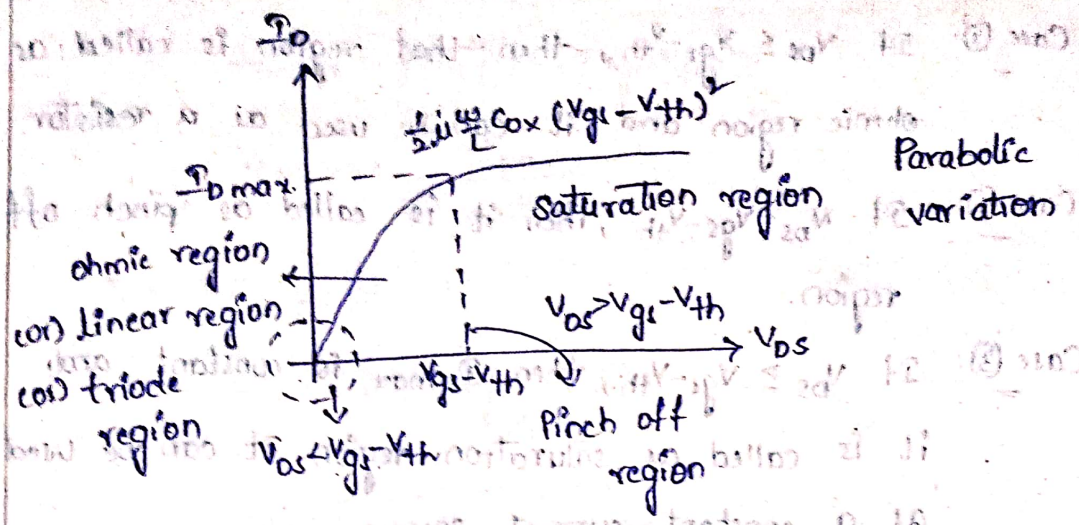
$$I_D L = \mu W C_{ox} \left[(V_{gs} - V_{th})V - \frac{V^2}{2}\right]_0^{V_{DS}}$$

$$I_D L = \mu W C_{ox} \left[(V_{gs} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$I_D = \mu \frac{W}{L} C_{ox} \left[(V_{gs} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right] \longrightarrow (1)$$

($\frac{W}{L}$: aspect ratio)

Scanned with OKEN Scanner



$$\frac{\partial I_D}{\partial V_{DS}} = \mu\frac{W}{L}C_{ox}\left[(V_{gs}-V_{th}) - V_{DS}\right]$$

$$\frac{\partial I_D}{\partial V_{DS}} = 0 \Rightarrow V_{DS} = V_{gs}-V_{th}$$

Substitute in I_D,

$$I_{D\,max} = \mu\frac{W}{L}C_{ox}\left[(V_{gs}-V_{th})^2 - \frac{(V_{gs}-V_{th})^2}{2}\right]$$

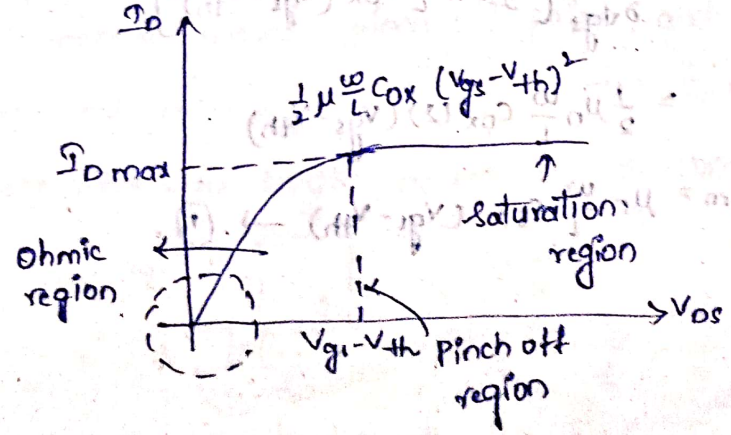
$$I_{D\,max} = \frac{1}{2}\mu\frac{W}{L}C_{ox}(V_{gs}-V_{th})^2$$

$$I_{D\,max} = \frac{1}{2}\mu_n\left(\frac{W}{L}\right)_n C_{ox}(V_{gs}-V_{th})^2 = k(V_{gs}-V_{th})^2$$

$$\left[\because k = \frac{1}{2}\mu_n\left(\frac{W}{L}\right)_n C_{ox}\right]$$

* In ohmic region, MOSFET can be used as resistor.
* In saturation region, it can be used as constant current source.

Region of operations of MOSFET:



Scanned with OKEN Scanner

Case ①: If $V_{DS} \leq V_{gs}-V_{th}$, then that region is called as ohmic region and it can be used as a resistor.

Case ②: If $V_{DS}=V_{gs}-V_{th}$, then it is called as pinch off region.

Case ③: If $V_{DS} \geq V_{gs}-V_{th}$, then I_{Dmax} is constant and it is called as saturation region. It can be used as a constant current source.

Drain resistance:

$$R_{DON} = R_D = \frac{V_{DS}}{I_D}$$

To use it as a resistor,

condition: $2(V_{gs}-V_{in})V_{DS} >> V_{DS}^2$

$$\Rightarrow I_D = \mu_n C_{ox} \frac{w}{L}\left[(V_{gs}-V_{in})V_{DS}\right]$$

$$R_{DON} = \frac{V_{DS}}{\mu_n C_{ox} \frac{w}{L}(V_{gs}-V_{in})V_{DS}}$$

$$R_{DON} = \frac{1}{\mu_n C_{ox} \frac{w}{L}(V_{gs}-V_{in})}$$

Transconductance (g_m):

Case ①:

$$g_m = \frac{\partial I_{Dmax}}{\partial V_{gs}}$$

$$= \frac{\partial}{\partial V_{gs}}\left[\frac{1}{2}\mu_n \frac{w}{L} C_{ox}(V_{gs}-V_{th})^2\right]$$

$$= \frac{1}{2}\mu_n \frac{w}{L} C_{ox}(2)(V_{gs}-V_{th})$$

$$g_m = \mu_n \frac{w}{L} C_{ox}(V_{gs}-V_{th}) \rightarrow (1).$$

Case (2): $I_{Dmax} = \frac{1}{2}\mu_n \frac{W}{L} C_{ox} (V_{gs}-V_{th})^2$

$$V_{gs}-V_{th} = \sqrt{\frac{2I_{Dmax}}{\mu_n \frac{W}{L} C_{ox}}}$$

Substitute in (1),

$$g_m = \mu_n \frac{W}{L} C_{ox} \sqrt{\frac{2I_{Dmax}}{\mu_n \frac{W}{L} C_{ox}}}$$

$$g_m = \sqrt{2\mu_n \frac{W}{L} C_{ox} I_{Dmax}}$$

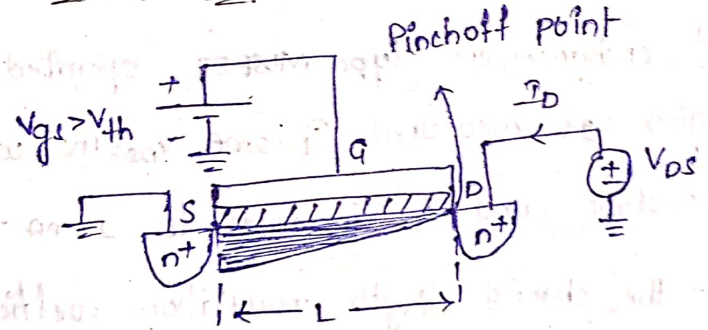
Case (3):

$$\frac{g_m}{I_{Dmax}} = \frac{\mu_n \frac{W}{L} C_{ox} (V_{gs}-V_{th})}{\frac{1}{2}\mu_n \frac{W}{L} C_{ox} (V_{gs}-V_{th})^2}$$

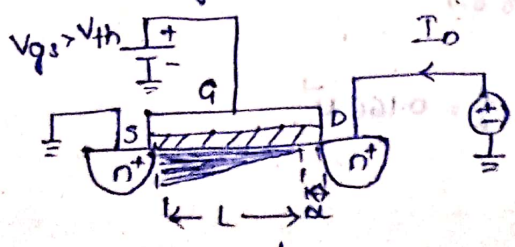
$$\frac{g_m}{I_{Dmax}} = \frac{2}{(V_{gs}-V_{th})}$$

$$g_m = \frac{2I_{Dmax}}{V_{gs}-V_{th}}$$

Channel length Modulation:



If channel reaches pinch off point and V_{DS} increases more and more, the channel moves from drain to source and the length decreased is considered as ΔL.



$$I_{Dmax} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2(1+\lambda V_{DS})$$

↓ channel length modulation coefficient

units for λ: V^{-1} (Volt^{-1})

$$I_{Dmax} = \frac{1}{2}\mu_n C_{ox}\frac{W}{(L-\Delta L)}(V_{gs}-V_{th})^2$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L\left(1-\frac{\Delta L}{L}\right)}(V_{gs}-V_{th})^2$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2\left(1-\frac{\Delta L}{L}\right)^{-1}$$

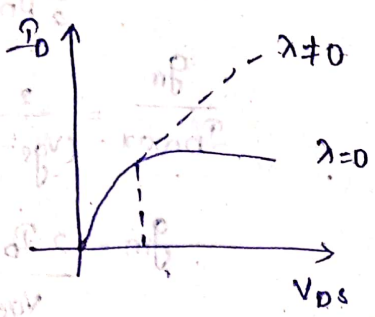
$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2\left(1+\frac{\Delta L}{L}\right)$$

we know that $\Delta L \propto V_{DS}$

$$\Delta L = \lambda' V_{DS}$$

$$\frac{\Delta L}{L} = \frac{\lambda'}{L}V_{DS}$$

$$\frac{\Delta L}{L} = \lambda V_{DS}$$



$$I_{Dmax} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2(1+\lambda V_{DS})$$

Pb: In n-channel enchancement type MOSFET operated in saturation region. It measured, $I_D = 2mA$, $V_{DS} = 4V$ while keeping V_{gs} constant and I_D increases to 2.2mA then $V_{DS} = 5V$. Find the channel length modulation coefficient.

$$\frac{2\times10^{-3}}{2.2\times10^{-3}} = \frac{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2(1+4\lambda)}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2(1+5\lambda)}$$

$$\frac{2}{2.2} = \frac{1+4\lambda}{1+5\lambda}$$

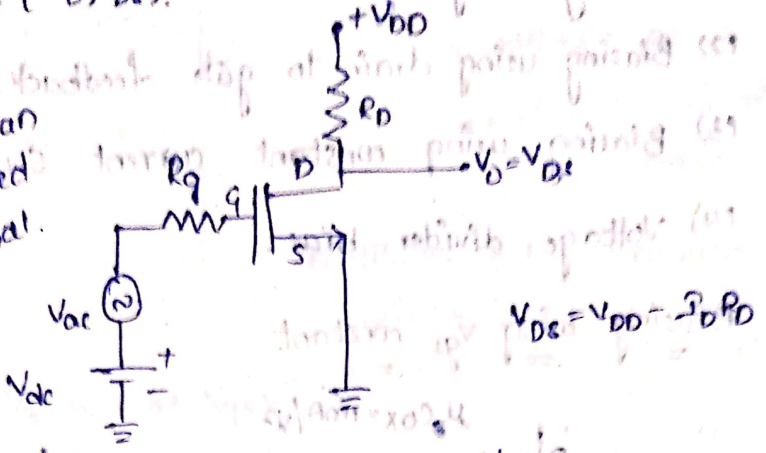
$$\therefore 2+10\lambda = 2.2+8.8\lambda$$

$$\lambda = \frac{0.2}{1.2} = \frac{1}{6} = 0.166\ V^{-1}$$

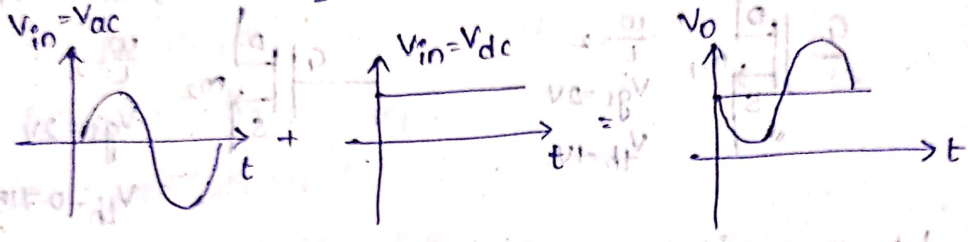
Scanned with OKEN Scanner

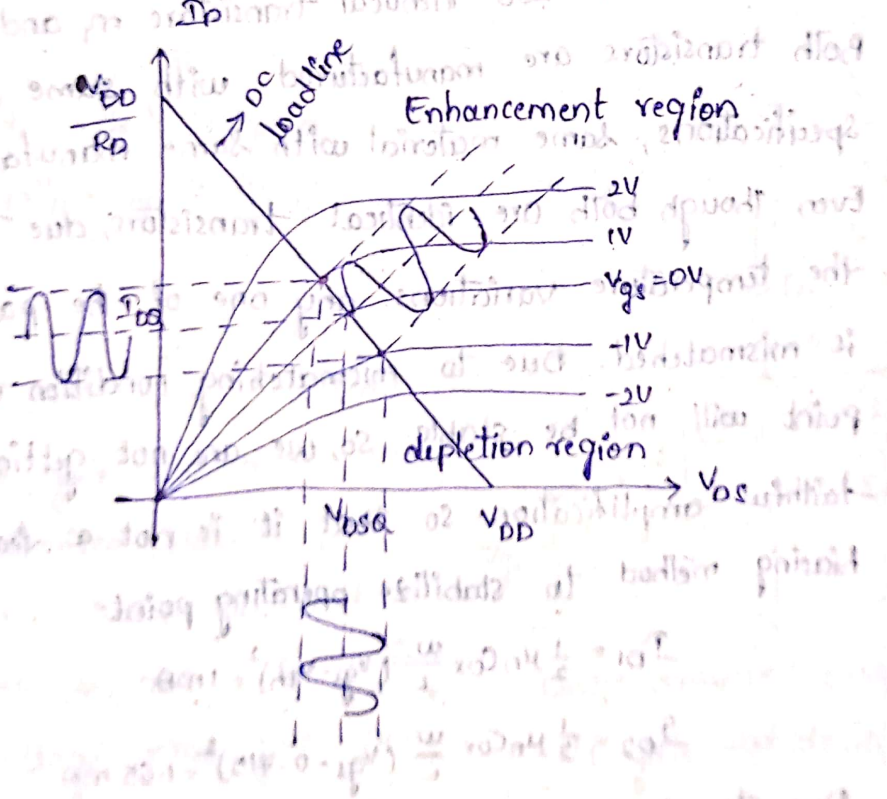
MOSFET biasing:

Using proper biasing, we can able to stabilize the operating point (I_D, V_{DS}).



microphone can be used for ac signal.





Biasing Techniques:

There are 4 types of biasing techniques.

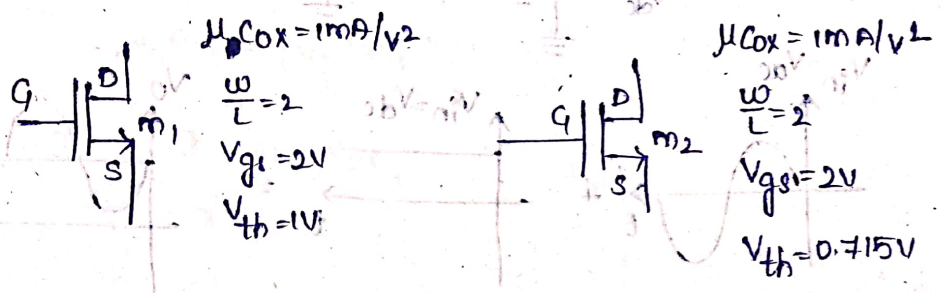
(1) Biasing using V_{gs} constant.

(2) Biasing using drain to gate feedback resistor

(3) Biasing using constant current source

(4) Voltage divider bias.

(1) Biasing using V_{gs} constant:



Let us consider two identical transistors m_1 and m_2. Both transistors are manufactured with same specifications, same material with same manufacturer. Even though both are identical transistors, due to the temperature variations any one of the parameter is mismatched. Due to mismatching condition operating point will not be stable. So, we are not getting faithful amplification so that it is not a feasable biasing method to stabilize operating point.

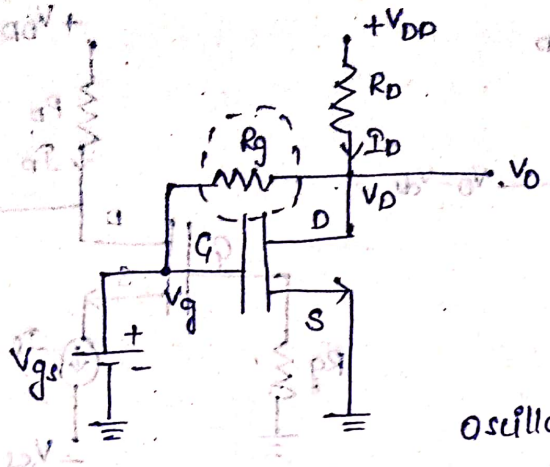
$$I_{D1} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 = 1mA$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{gs} - 0.715)^2 = 1.65\ mA$$

Due to threshold voltage mismatch, operating point will not be stable.

Scanned with OKEN Scanner

(2) Biasing using drain to gate feedback resistor:



Rg: feedback resistor

⇒ -ve feedback ckt

⇒ MOSFET as a amplifier in saturation region

Oscillator ⇒ +ve feedback

from circuit,

$V_{gd} = 0 \Rightarrow V_g - V_d = 0 \Rightarrow V_g = V_d$

from the circuit,

Apply KVL for o/p loop

$-V_{DD} + I_D R_D + V_D = 0$

$V_D = V_{DD} - I_D R_D$

$V_{gs} = V_{ds}$

$V_g - V_s = V_d - V_s \Rightarrow V_g = V_d$

$V_g = V_D = V_{DD} - I_D R_D$

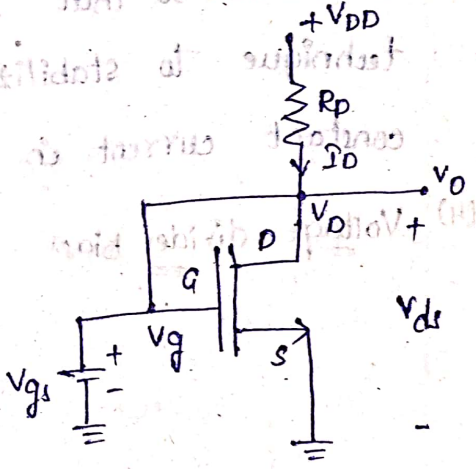
Case (5):

from the above circuit,

$R_{gd} \simeq 0$ (short circuited)

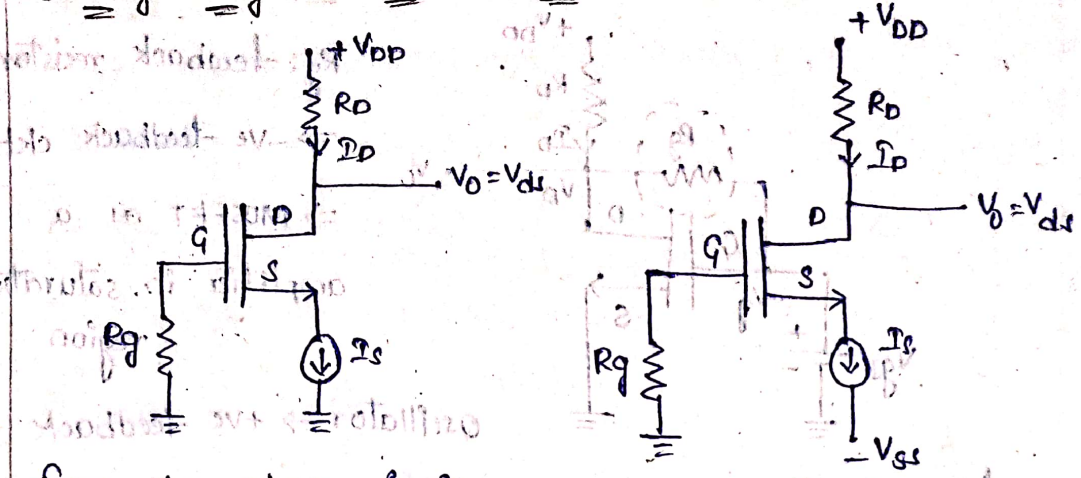
So that gate and drain are short circuited. feedback path connected between i/p and o/p nodes. So that it is having same voltage across gate and drain. $I_g = 0$ (high resistance)

$V_g = V_D = V_{DD} - I_D R_D$



Diode connected device - if gate and drain are s.c.

(3) Biasing using constant current source:



from the above circuit,

Voltage across R_D is $I_D R_D$.

The drain current flowing through R_D and through MOSFET device and reaches to source terminal. Drain current cannot flowing through the gate terminal because it can be offered by high resistance.

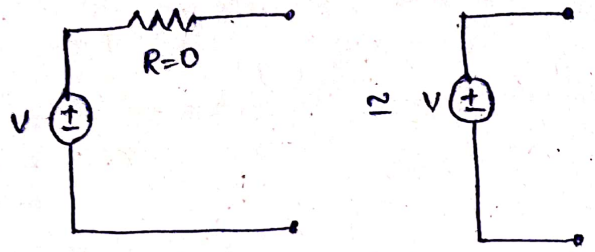
So that, $I_g = 0$.

According to circuit, same current flowing to the drain to source. So that $I_d = I_s$. So it is a best biasing technique to stabilize the operating point due to constant current in between drain to source.

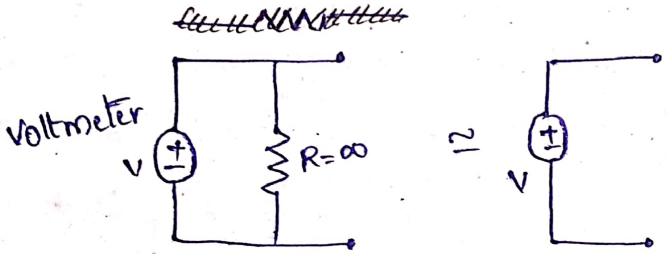
(4) Voltage divider bias:

Basics:

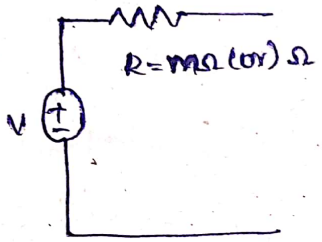
Ideal voltage Source:



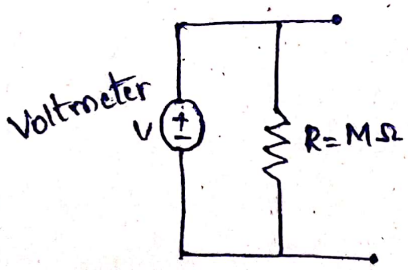
Zero resistance acts as a short circuit Ideal Voltage source is having zero internal resistance. Like that, ideal voltmeter is in parallel ~~with Voltage Source~~ with infinite internal resistance.



Practical voltage Source:

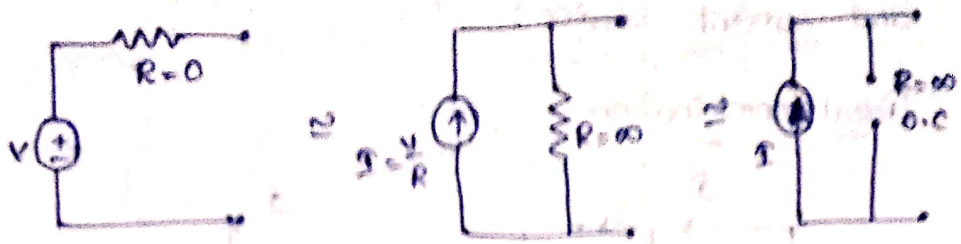


Practical voltage source is having mΩ (or) Ω. Practical voltmeter is having MΩ (or) GΩ of resistance in Parallel.

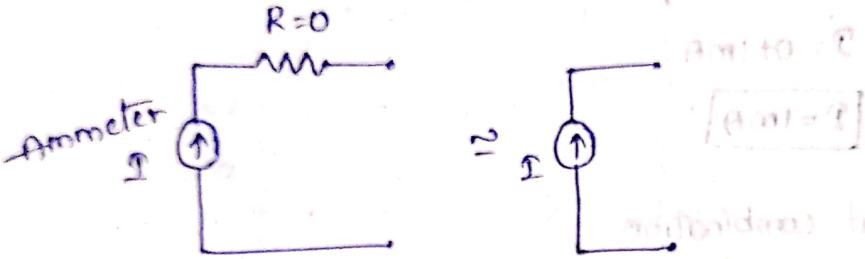


Scanned with OKEN Scanner

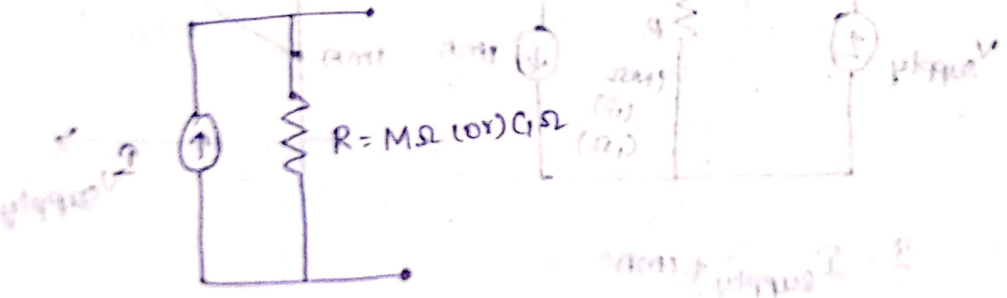
Ideal current Source:



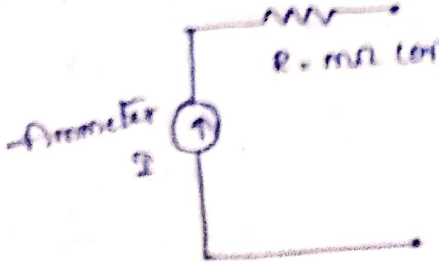
Ideal current source is in parallel with resistor having infinite resistance. Ideal ammeter is in ~~Parallel~~ Series with resistor having zero resistance.



Practical current Source:

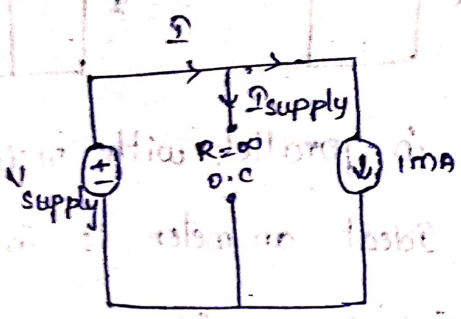


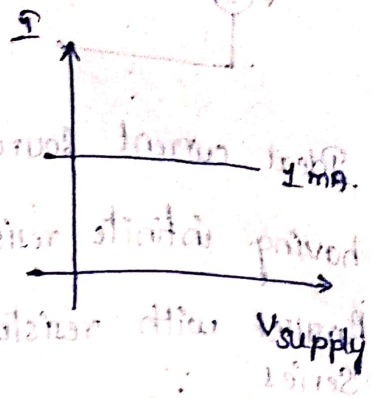
Practical current source is in Parallel with resistor having MΩ (or) GΩ resistance. Practical ammeter is in Series with resistor having mΩ (or) Ω.



Drawing of IV characteristics for voltage source and current source:

Ideal combination:

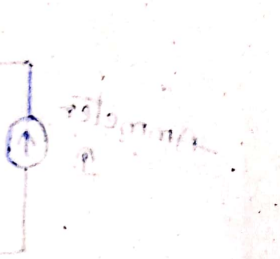




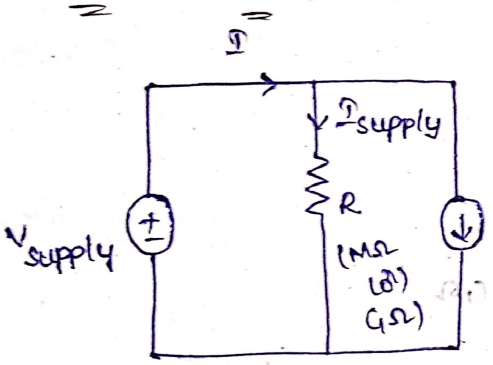
$I = I_{supply} + 1mA$

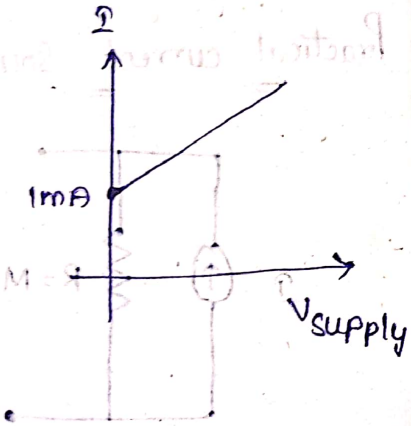
$I = 0 + 1mA$

$\boxed{I = 1mA}$



Practical combination:

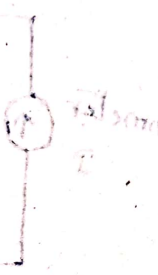




$I = I_{supply} + 1mA$

$I = \frac{V_{supply}}{R} + 1mA \quad (\because y = mx + c)$

pb: Let us consider two voltage source circuits (or) Voltmeter circuits. Justify the which circuit is better among those two circuits,



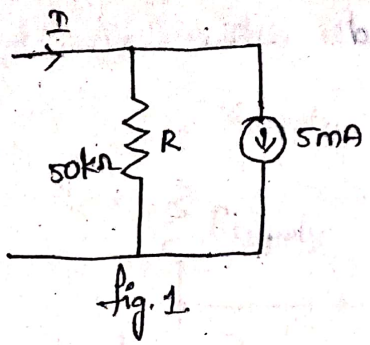


fig. 1

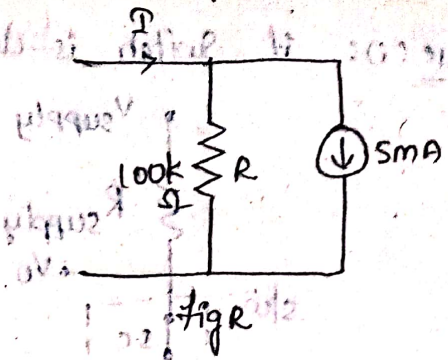


fig 2

$I = \frac{1}{50\times10^3} \times V_s + 5mA$

$I = \frac{1}{100\times10^3} \times V_s + 5mA$

Slope : $\frac{1}{50\times10^3}$

Slope : $\frac{1}{100\times10^3}$

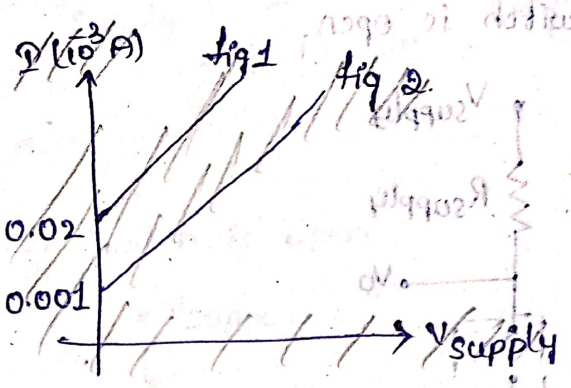
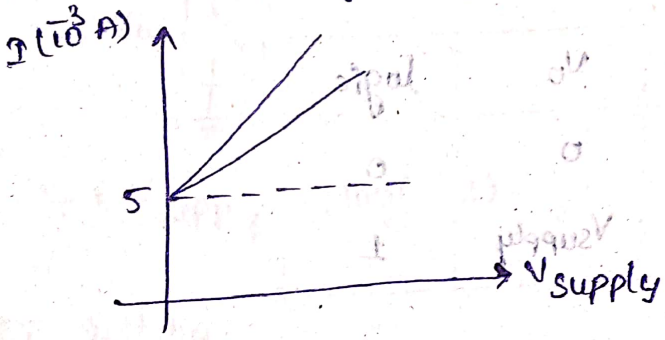
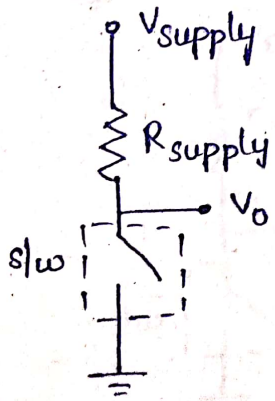
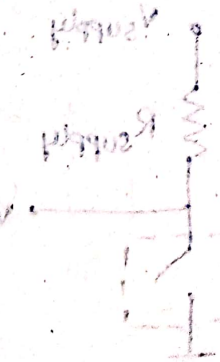


fig 2 is better circuit because it is having lesser slope compared to figure 1

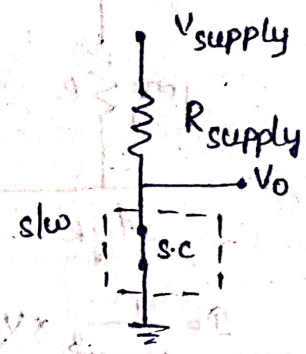


Ideal Switches:



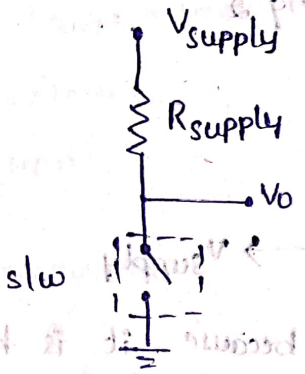


Case (i): if Switch is closed



Here $V_o = 0$ (logic "0")

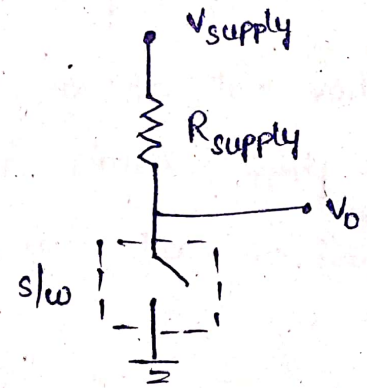
case (ii): if switch is open.



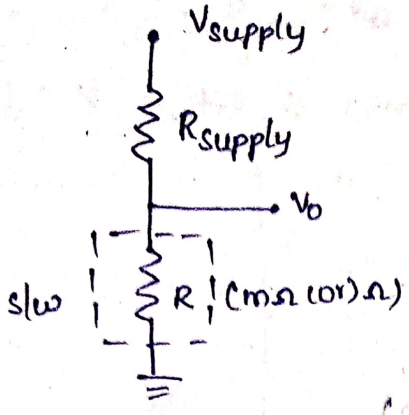
$V_o = V_{supply}$ (logic - 1)

Switch	V_o	logic
closed	0	0
open	V_{supply}	1

Practical Switch:



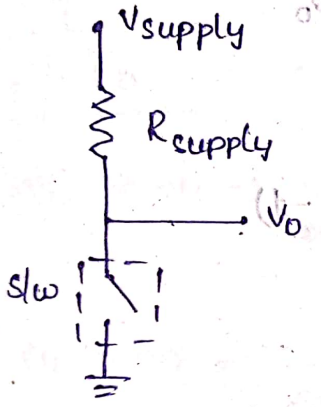
Case 1: If switch is closed.



$$V_o = V_{supply} \times \frac{R}{R + R_{supply}} \quad (\text{logic-0})$$

$$= mV \simeq 0$$

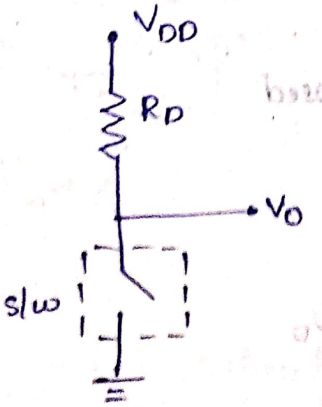
Case 2: If switch is open



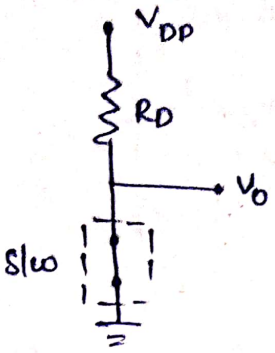
$$V_o = V_{supply} \quad (\text{logic} - 1)$$

MOSFET Switches:

Ideal Switch:

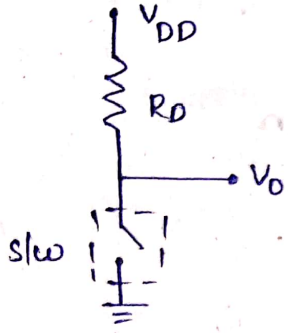


Case (i): if switch is closed



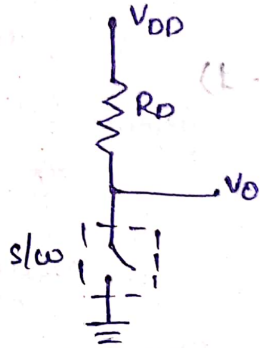
$V_O = 0$ (logic-0)

Case (ii): if switch is open

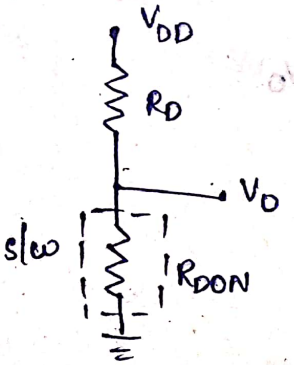


$V_O = V_{DD}$ (logic -1).

Practical Switch:

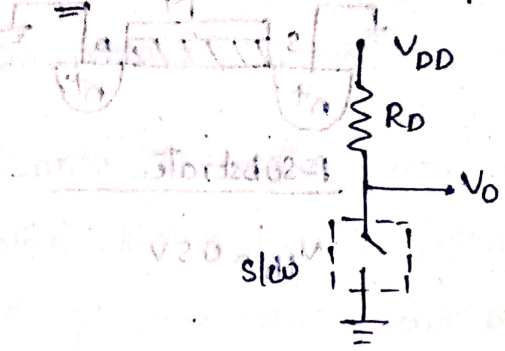


Case (i): if switch is closed



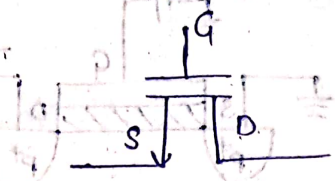
$$V_o = V_{DD} \times \frac{R_{DON}}{R_{DON} + R_D} \quad \text{(logic-0)}$$

Case(ii): if Switch is open



$V_o = V_{DD}$ (logic-1)

MOSFET switches:

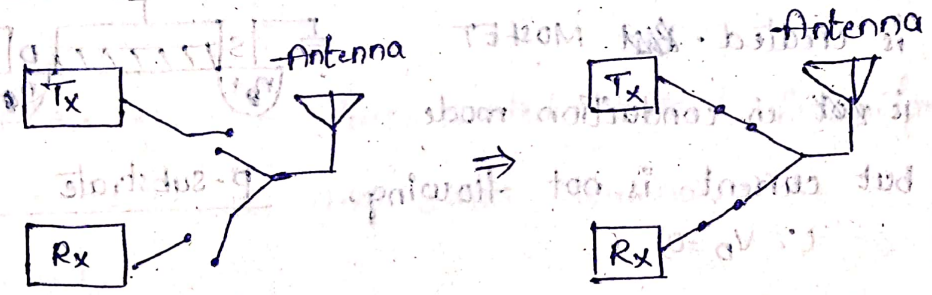


(i) if $V_{gs} > V_{th} \Rightarrow$ ON $\Rightarrow$ short circuit $\Rightarrow$ ON switch

(ii) if $V_{gs} < V_{th} \Rightarrow$ OFF $\Rightarrow$ open circuit $\Rightarrow$ OFF switch

Application for MOSFET switch:

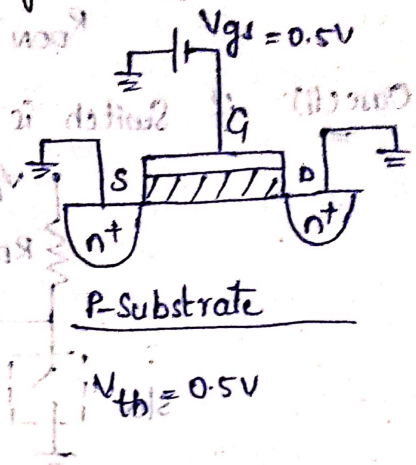
Bluetooth devices:



Switches are closed.

Therefore data transferred from transmitter to receiver via antenna.

Q) If V_{gs} is negative, is there any channel created for a given MOSFET (or) not.



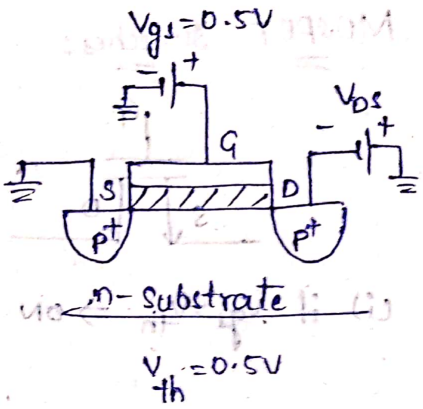
As V_{gs} is negative,

$V_{gs} < V_{th}$

$-0.5 < 0.5$

Therefore no channel is created.

Q) If V_{gs} is +ve, is there any channel is created or not for a given MOSFET.



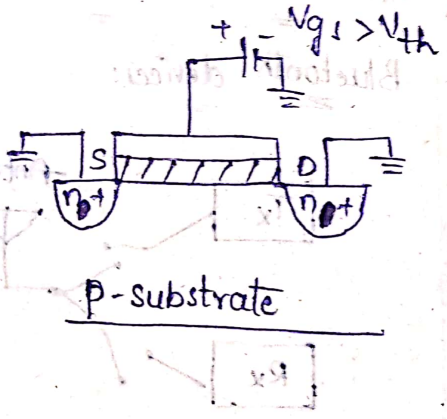
P-type MOSFET becomes ON for -ve Voltages.

Given V_{gs} is +ve.

Therefore MOSFET doesn't come under conduction mode.

channel is also not created.

Q) If V_{gs} is +ve, how much drain current available for the given circuit



As $V_{gs} > V_{th}$, channel is created. But MOSFET is not in conduction mode but current is not flowing.

($\because V_D = 0$)

if $V_D \neq 0$, then drain current is available for the given circuit.

Q) What is the polarity of threshold voltage in NMOS and PMOS?

In NMOS, $V_{th} \geq 0$

In PMOS, $V_{th} \leq 0$

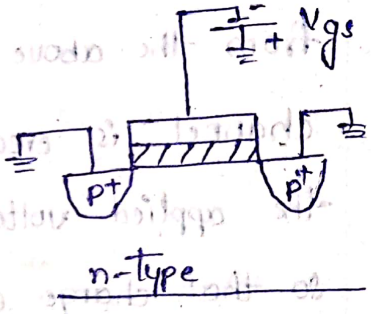
Q) In order to create a channel in NMOS and PMOS, what should be the polarity of gate to source voltage and what should be the ON condition of PMOS and NMOS?

In NMOS, $V_{gs} \geq 0$, $V_{th} > 0$ and $V_{gs} \geq V_{th}$

In PMOS, $V_{gs} \leq 0$, $V_{th} < 0$ and $V_{gs} \leq V_{th}$

PMOSFET

From the above structure, channel will be existing in b/w source to drain. so that charge carriers also moves from source to drain. Drain current is zero due to the grounding of drain terminal.



$\therefore I_D = 0$

From the above structure, created channel is uniform because of source and drain terminals are grounded.

channel existing condition for PMOSFET:

In NMOSFET:

$V_{gsn} \geq V_{thn}$

In PMOSFET:

$V_{gsp} \leq V_{thp}$

$V_{gp} - V_{sp} \leq V_{thp}$

$-(V_{gp} - V_{sp}) \leq -V_{thp}$

$V_{sp} - V_{gp} \geq V_{thp}$

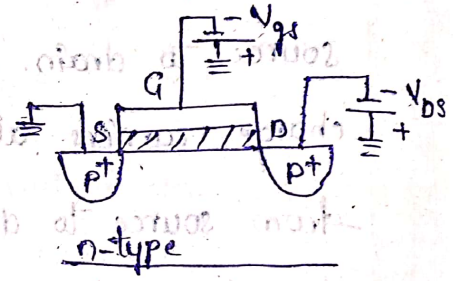
$V_{sgp} \geq V_{thp}$

$\therefore \boxed{V_{sgp} \geq V_{thp}}$

↓

channel existing condition for PMOSFET.

from the above structure, non-uniform channel is created due to the applied voltage of V_{gs}. so that charge carriers are travelling from one terminal to other terminal. Due to that current also travelling from source to drain.



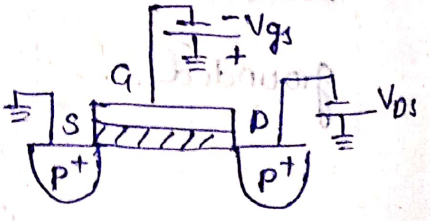
Drain current equation for PMOSFET:

Case 1:

$V_{gs} < V_{th}$, $V_{DS} = 0$

Q_{ch} total = Gate area $\times C_{ox}(V_{sg} - V_{th})$

Q_{ch} total = $WLC_{ox}(V_{sg} - V_{th})$



Case ②:

$V_{gs} < V_{th}$, $V_D > 0$ and $V_B = 0$

$$Q_{ch} = WC_{ox}(V_{sg} - V_{th} - V(x))$$

$$v = \mu E \qquad E = -\frac{dv}{dx}$$

$$v = -\mu \frac{dv}{dx}$$

Total drain current, $I_D = -vQ_{ch}$

$$I_D = \mu \frac{dv}{dx} WC_{ox}(V_{sg} - V_{th} - V)$$

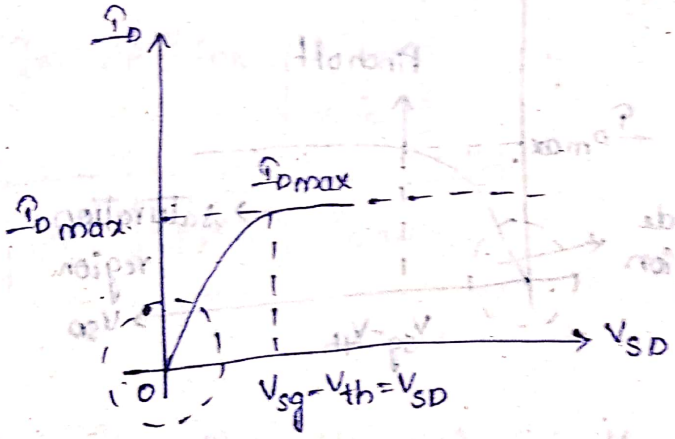
$$I_D\, dx = \mu WC_{ox}(V_{sg} - V_{th} - V)\, dv$$

Integrating on both sides,

$$\int_0^L I_D\, dx = \mu WC_{ox} \int_0^{V_{SD}} (V_{sg} - V_{th} - V)\, dV$$

$$I_D L = \mu WC_{ox}\left[(V_{sg} - V_{th})V_{SD} - \frac{V_{SD}^2}{2}\right]$$

$$I_D L = \mu WC_{ox}\left[(V_{sg} - |V_{th}|)V_{SD} - \frac{V_{SD}^2}{2}\right] \longrightarrow (1)$$



Condition for using as a voltage variable resistor.

$$(V_{sg} - |V_{th}|)V_{SD} = \frac{V_{SD}^2}{2}$$

$$2[V_{sg} - |V_{th}|] = V_{SD}$$

Scanned with OKEN Scanner

To find maximum drain current, differentiating I_D wrt V_{SD} and making it zero.

$$\frac{\partial I_D}{\partial V_{SD}} = 0$$

$$(V_{sg} - |V_{thp}|) - V_{SD} = 0$$

$$V_{SD} = V_{sg} - |V_{thp}|$$

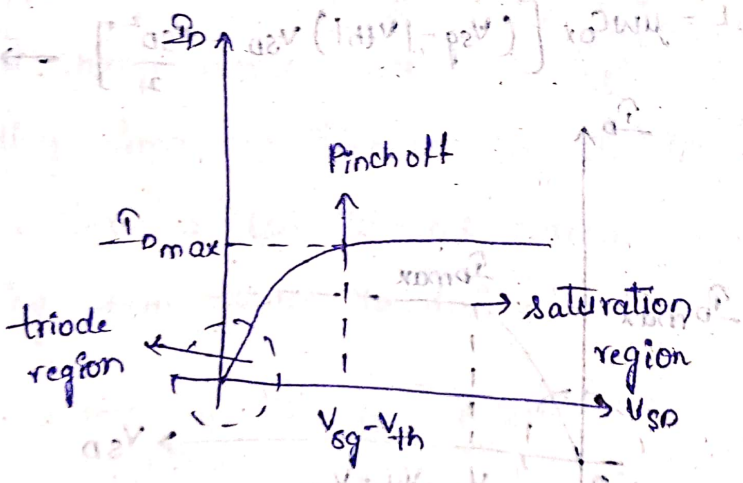
Substitute in ①,

$$\boxed{I_{Dmax} = \frac{1}{2}\mu_p C_{ox} \frac{w}{L} \left(V_{sg_p} - V_{thp}\right)^2}$$

① If $V_{SD} < V_{sg} - V_{th}$, PMOSFET acts as a voltage variable resistor. It is in triode region.

② If $V_{SD} = V_{sg} - V_{th}$, PMOSFET results maximum current. It is in pinchoff region.

③ If $V_{SD} > V_{sg} - V_{th}$, It is in saturation region acts as a constant current source, amplifier.



$$R_{DON} = \frac{V_{SD}}{I_D}$$

$$= \frac{V_{SD}}{\mu_p C_{ox} \frac{w}{L} (V_{sg} - V_{th}) V_{SD}}$$

$$R_{DON} = \frac{1}{\mu_p C_{ox} \frac{W}{L} (V_{sgp} - V_{thp})}$$

If $V_{sg} = V_{th}$, R_{DON} goes to infinity.

Transconductance (g_m):

Case ①: $g_m = \frac{\partial I_{Dmax}}{\partial V_{sg}}$

$$= \frac{\partial}{\partial V_{sg}} \left[\frac{1}{2} \mu_p \frac{W}{L} C_{ox} (V_{sg} - V_{th})^2 \right]$$

$$= \frac{1}{2} \mu_p \frac{W}{L} C_{ox} (2) (V_{sg} - V_{th})$$

$$\boxed{g_m = \mu_p \frac{W}{L} C_{ox} (V_{sg} - V_{th})}$$

Case ②:

$$I_{Dmax} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{sg} - V_{th})^2$$

$$V_{sg} - V_{th} = \sqrt{\frac{2 I_{Dmax}}{\mu_p C_{ox} \frac{W}{L}}}$$

WL : Gate area

$\frac{W}{L}$: aspect ratio

unit for $\mu_p C_{ox}$: $\frac{Amp}{V^2}$

Substitute in case ①,

$$g_m = \mu_p \frac{W}{L} C_{ox} \sqrt{\frac{2 I_{Dmax}}{\mu_p C_{ox} \frac{W}{L}}}$$

$$\boxed{g_m = \sqrt{2 \mu_p C_{ox} \frac{W}{L} I_{Dmax}}}$$

Case ③:

$$\frac{g_m}{I_{Dmax}} = \frac{\mu_p \frac{W}{L} C_{ox} (V_{sg} - V_{th})}{\frac{1}{2} \mu_p \frac{W}{L} C_{ox} (V_{sg} - V_{th})^2}$$

$$\boxed{g_m = \frac{2 I_{Dmax}}{V_{sg} - V_{th}}}$$

Scanned with OKEN Scanner

Q Given NMOS $\mu_n C_{ox} = 2\,mA/V^2$, $\left(\frac{W}{L}\right)_n = 2$, $V_{gs_n} = 2V$, $V_{th_n} = 1V$, $V_{DS} = 1V$. find the drain current and transconductance

$$I_{Dmax} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})$$

$$= \frac{1}{2}(2\times10^{-3})(2)(2-1)$$

$$= 2mA$$

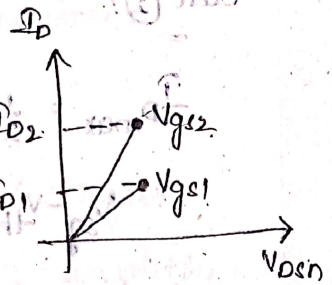
$$g_m = \frac{2I_{Dmax}}{V_{gs} - V_{th}} = 4m\Omega^{-1}$$

Q Let us consider a graphical curve and justify which of the following curve is true. Take it as condition.

$V_{DSn} << 2V_{OV}$. V_{OV} : overdrive voltage

I_{D2} is more than I_{D1}.

(i) $V_{gs1} > V_{gs2}$ (ii) $V_{gs1} < V_{gs2}$



(iii) We have

$$R_{DON} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})}$$

consider $V_{gs1} < V_{gs2}$

as $V_{gs1} \downarrow \Rightarrow R_{DON} \uparrow \Rightarrow I_{D1} \downarrow$

Hence condition (ii) satisfies.

Q In NMOS $\mu_n C_{ox} = 5\,\mu A/V^2$, $V_{th} = 2V$, $\frac{W}{L} = 10$, $V_{DS} = 2V$.

Case ①: $V_{gs1} = 2V$

Case ②: $V_{gs_n} = 4V$

find the drain current, transconductance, R_{DON}.

Case (1):

$I_{Dmax} = \frac{1}{2}(5\times10^{-6})(10)(2-2)^2$

$= 0$

$g_m = \frac{2I_{Dmax}}{V_{gs}-V_{th}} = 0$

$I_D = (5\times10^{-6})(10)\left(\frac{-4}{2}\right)$

$= -100\,\mu A$

$R_{DON} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})} = \infty$

Case (2):

$I_{Dmax} = \frac{1}{2}(5\times10^{-6})(10)(4-2)^2$

$= 100\times10^{-6}\,A$

$= 10^{-4}\,A = \frac{1}{10}\,mA$

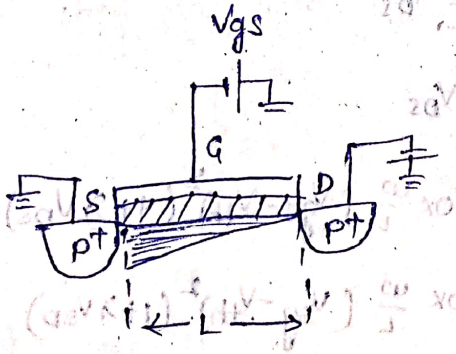
$g_m = \frac{2\times100\times10^{-6}}{(4-2)} = 100\times10^{-6}\,\frac{A}{V}$

$R_{DON} = \frac{1}{(5\times10^{-6})(10)(4-2)} = \frac{1}{100\times10^{-6}} = 10^4\,\Omega$

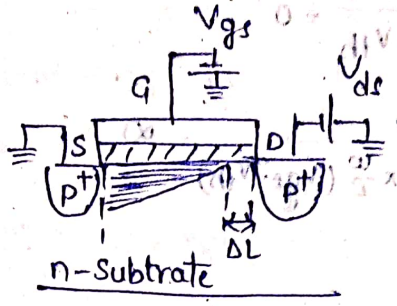
$I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{gs}-V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$

$= (5\times10^{-6})(10)\left[(2)(2) - \frac{(2)^2}{2}\right] = 100\times10^{-6}\,A$

Channel length modulation in P-MOSFET:



If channel reaches pinchoff point and V_{DS} increases more and more, the channel moves from drain to source and length decreased is considered as ΔL.



$$I_{Dmax} = \frac{1}{2}\mu_p C_{ox}\frac{w}{L}(V_{gs}-V_{th})^2(1+\lambda V_{DS})$$

λ : channel length modulation coefficient

units for $\lambda : V^{-1}$ (Volt^{-1}).

$$I_{Dmax} = \frac{1}{2}\mu_p C_{ox}\frac{w}{(L-\Delta L)}(V_{gs}-V_{th})^2$$

$$= \frac{1}{2}\mu_p C_{ox}\frac{w}{L\left(1-\frac{\Delta L}{L}\right)}(V_{gs}-V_{th})^2$$

$$= \frac{1}{2}\mu_p C_{ox}\frac{w}{L}(V_{gs}-V_{th})^2\left(1-\frac{\Delta L}{L}\right)^{-1}$$

$$= \frac{1}{2}\mu_p C_{ox}\frac{w}{L}(V_{gs}-V_{th})^2\left(1+\frac{\Delta L}{L}\right)$$

We know that, $\Delta L \propto V_{DS}$

$$\Delta L = \lambda' V_{DS}$$

$$\frac{\Delta L}{L} = \frac{\lambda'}{L}V_{DS}$$

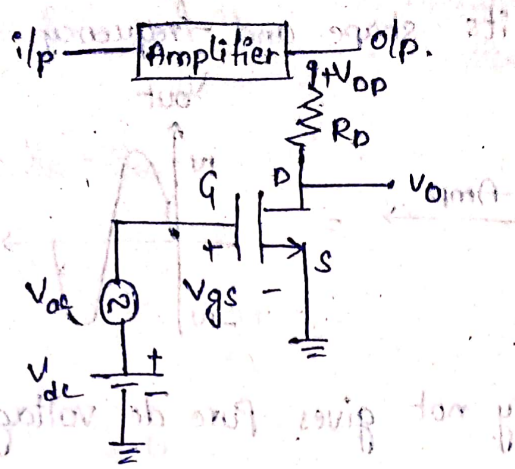
$$\frac{\Delta L}{L} = \lambda V_{DS}$$

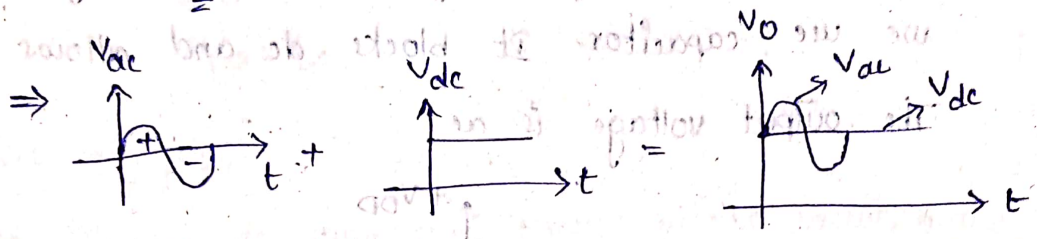
$$I_{Dmax} = \frac{1}{2}\mu_p C_{ox}\frac{w}{L}(V_{gs}-V_{th})^2(1+\lambda V_{DS})$$

$$I_{Dmax} = \frac{1}{2}\mu_p C_{ox}\frac{w}{L}(V_{sg}-V_{th})^2(1+\lambda V_{SD})$$

Scanned with OKEN Scanner

MOSFET small signal analysis: Biasing





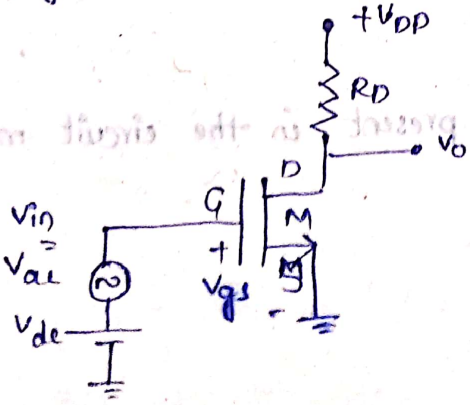
To establish operating point stable, irrespective changes of temperature, pressure, humidity or any other circuit Parameters.

Biasing can be done only by using dc supplies only.

Main funda of amplifier application for the given MOSFET is don't apply ac input directly without biasing.

first we can apply dc input, second we can apply ac input.

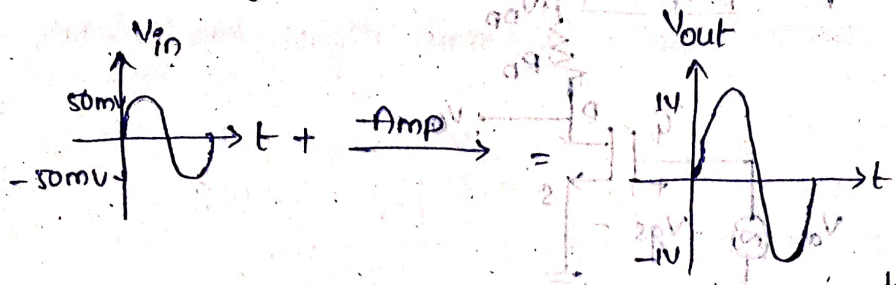
If applied voltage input is in mv, then it is small signal. They are used as amplifier.



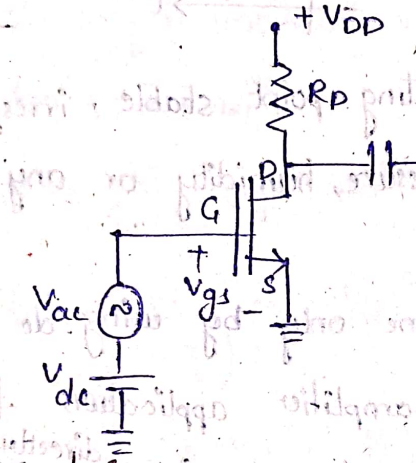
* If applied voltage i/p is in volts, it is large signal or power signal.

Scanned with OKEN Scanner

* Amplifier converts weak signal to strong signal without changing its shape and frequency.



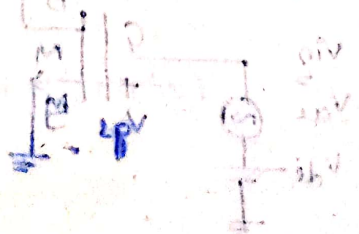
* Output voltage may not gives pure dc voltage due to V_{DD}. Therefore we use capacitor. It blocks dc and allows ac. The output voltage is ac.



Small signal analysis:

Dc analysis:

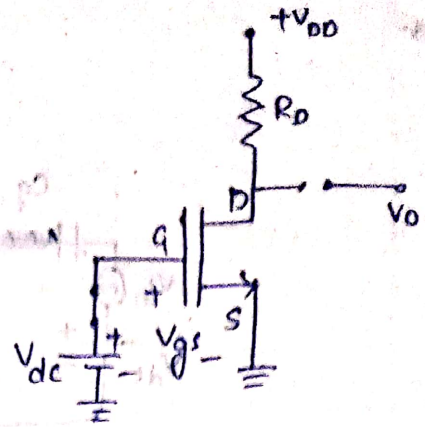
* Make all ac components to zero.
* All the dependent or independent ac voltage sources are short circuited.
* All the dependent or independent ac current sources are open circuited.
* All the capacitors present in the circuit make it as open circuited.



$V_{DS} = V_D = V_{DD} - I_D R_D$ } Operating Point

$I_D = \frac{V_{DD} - V_{DS}}{R_D}$

$V_{gs} = V_{dc}$



Case ①: $V_{DS} = 0$

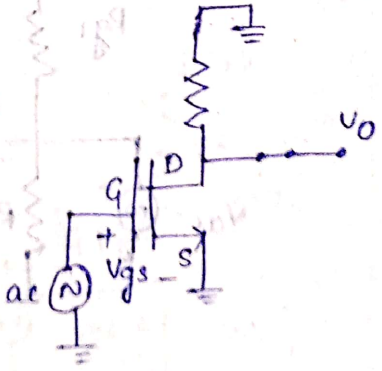
$\Rightarrow I_D = \frac{V_{DD}}{R_D}$

Case ②: $I_D = 0$

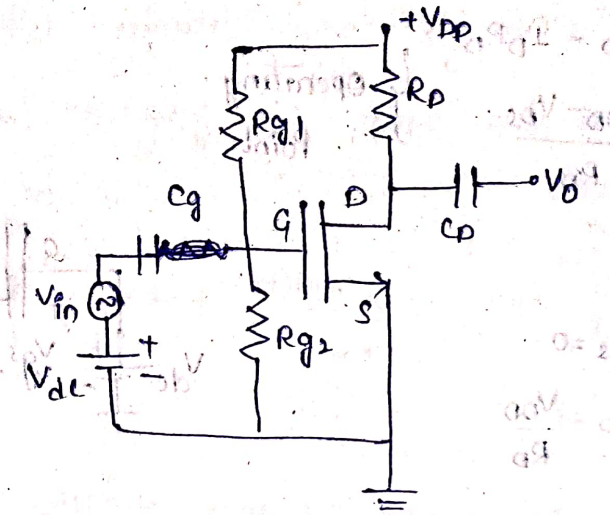
$V_{DD} = V_{DS}$

Ac analysis:

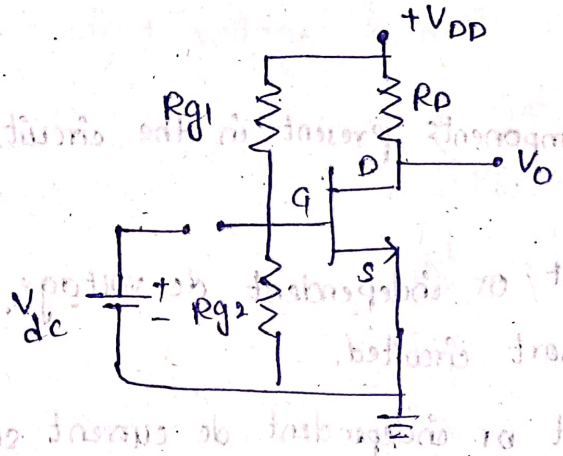
* All the dc components present in the circuit, make it as zero.
* All the dependent or independent dc voltage sources are short circuited.
* All the dependent or independent dc current sources are open circuited.
* All the capacitors present in the circuit make it as short circuited.



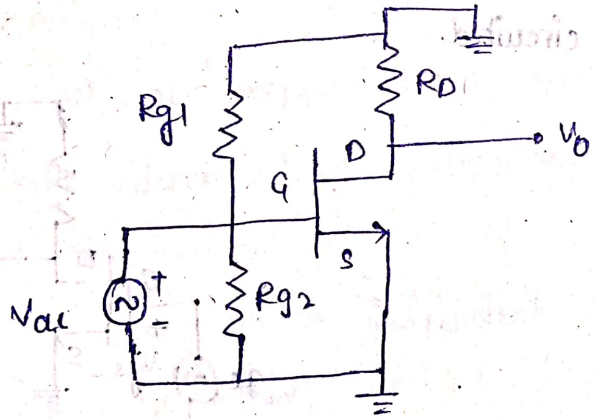
Scanned with OKEN Scanner



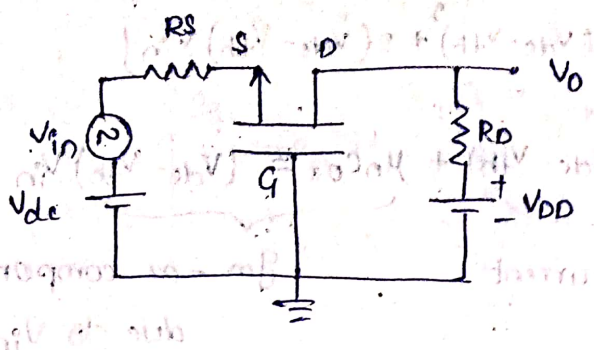
dc equivalent circuit:



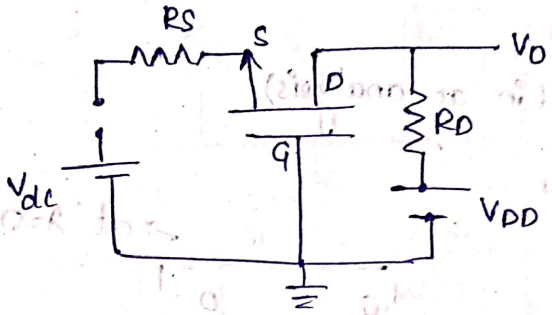
ac equivalent circuit:



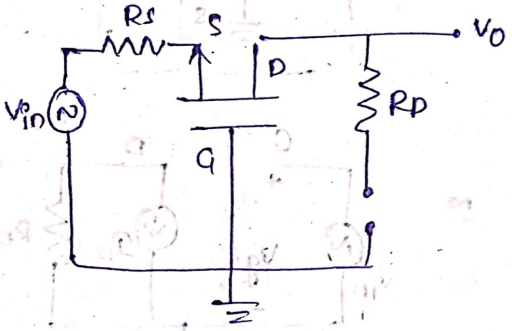
*



dc equivalent circuit:



ac equivalent circuit:

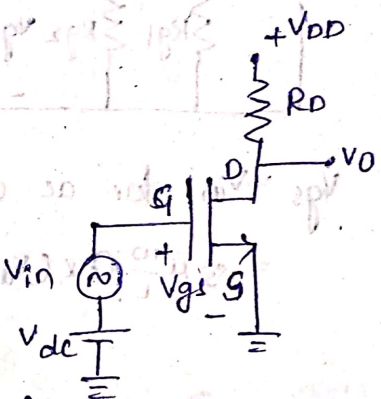


Small signal analysis:

ac analysis:

In saturation region,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2$$



from the circuit,

$$V_{gs} = V_{in} + V_{dc}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} + (V_{dc}-V_{th}))^2$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[V_{in}^2 + (V_{dc}-V_{th})^2 + 2V_{in}(V_{dc}-V_{th})\right]$$

$V_{in}^2 <<< 2(V_{dc}-V_{th})$

Scanned with OKEN Scanner

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[(V_{dc}-V_{th})^2 + 2(V_{dc}-V_{th})V_{in}\right]$$

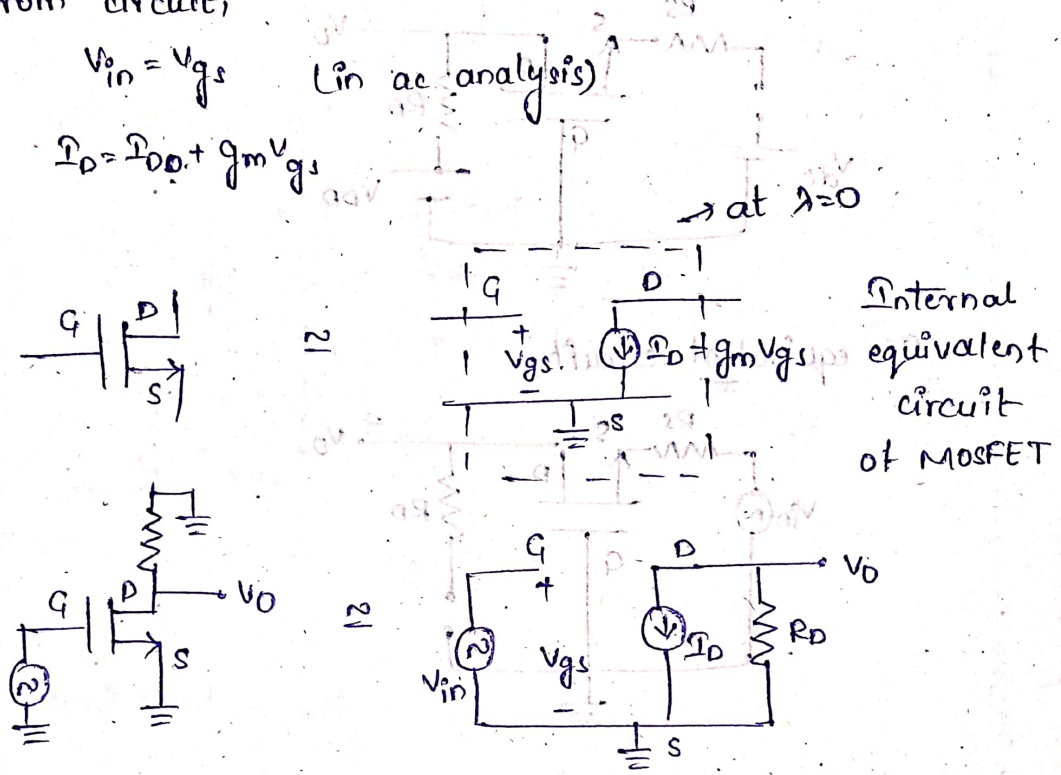
$$I_D = \underbrace{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{dc}-V_{th})^2}_{I_{DO}\text{ – dc current}} + \underbrace{\mu_n C_{ox}\frac{W}{L}(V_{dc}-V_{th})V_{in}}_{g_m\text{ – ac component due to }V_{in}}$$

$$I_D = I_{DO} + g_m V_{in}$$

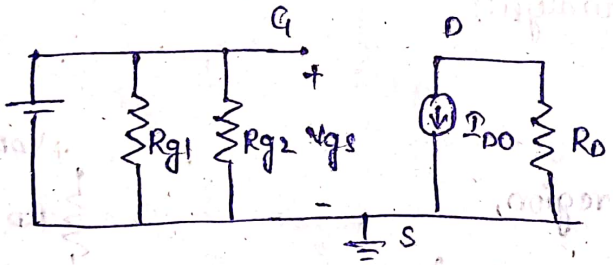
from circuit,

$V_{in} = V_{gs}$ (in ac analysis)

$I_D = I_{DO} + g_m V_{gs}$



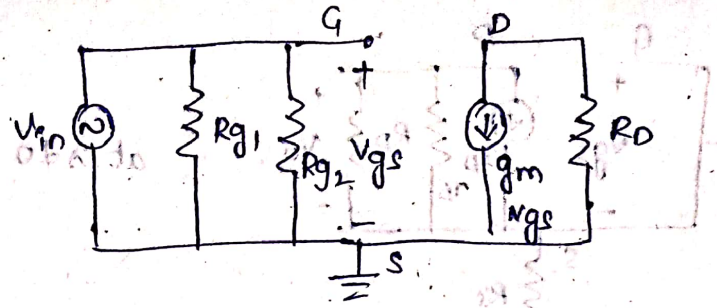
(1)



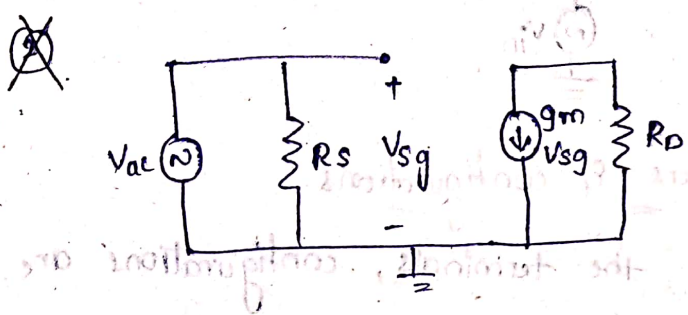
$V_{gs} = V_{in}$; for ac analysis

$$= \frac{1}{2}\mu\frac{W}{L}C_{ox}(V_{dc}-V_{th})^2 + \underbrace{\mu\frac{W}{L}C_{ox}(V_{dc}-V_{th})}_{g_m}\underbrace{V_{in}}_{V_{gs}}$$

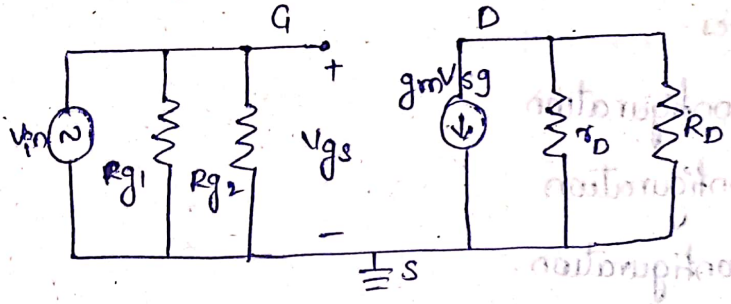
$$= I_{DO} + g_m V_{gs}$$



at $\lambda = 0$

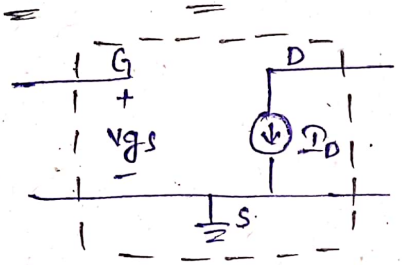


(1)

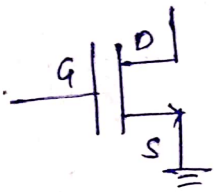


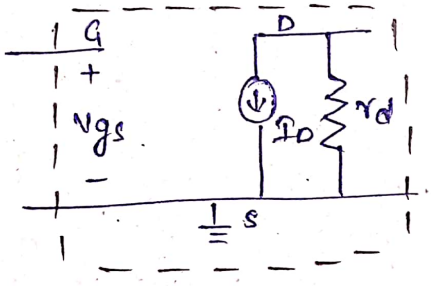
at $\lambda \neq 0$

MOSFET internal circuit:



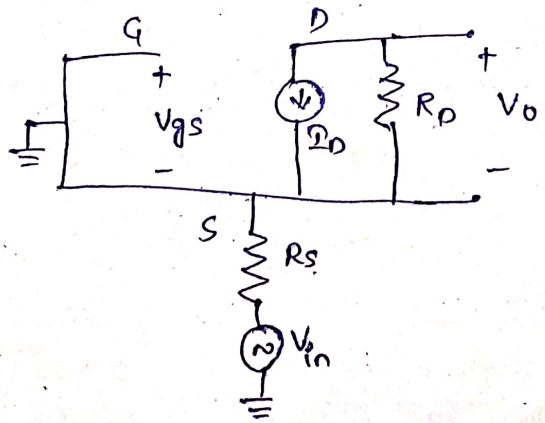
$\Rightarrow$ at $\lambda = 0$





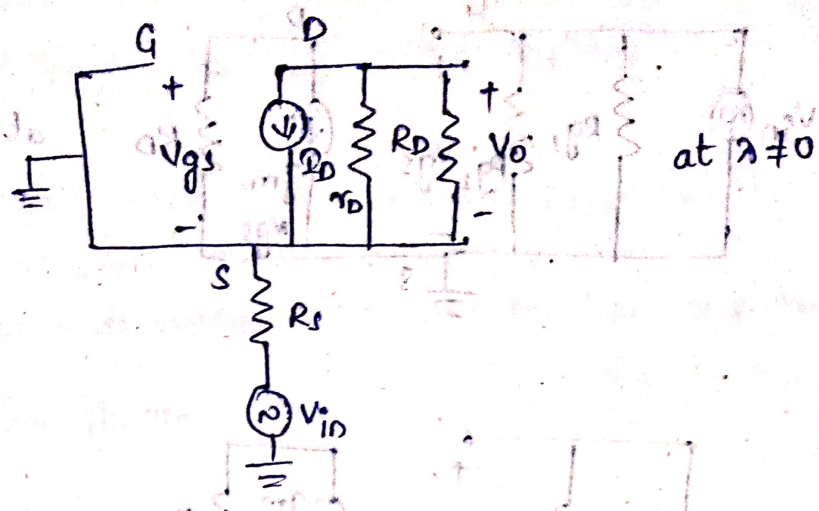
at $\lambda \neq 0$

(2)



at $\lambda = 0$

Scanned with OKEN Scanner



MOSFET Amlifiers & configurations:

Depending upon the terminals, configurations are of 3 types.

(1) CS configuration

(2) CG configuration

(3) CD configuration.

Depending upon terminals, amplifiers are of 3 types.

(1) common source amplifier

(2) common Gate amplifier

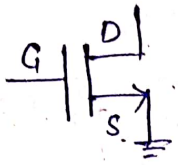
(3) common drain amplifier

(1) Common Source amplifier:

i/p terminal - Gate

o/p terminal - Drain

common terminal - Source

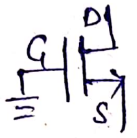


(2) Common Gate amplifier:

i/p terminal - Source

o/p terminal - Drain

common - Gate

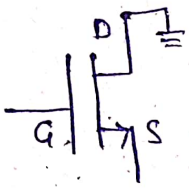


(3) Common Drain amplifier:

i/p - Gate

o/p - Source

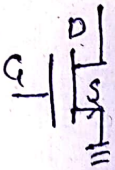
common - Drain



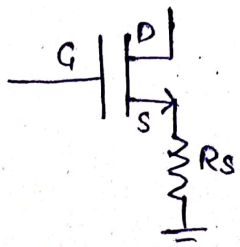
(1) Common Source amplifier:

(i) common source amplifier without R_S.

R_S: source resistance

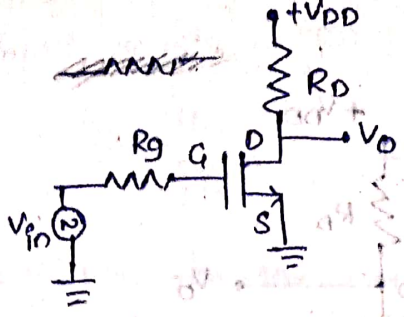


(ii) Common Source amplifier with R_S.

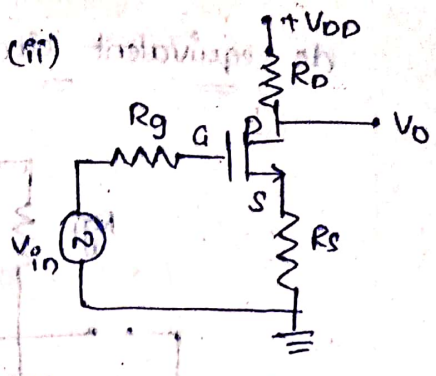


Scanned with OKEN Scanner

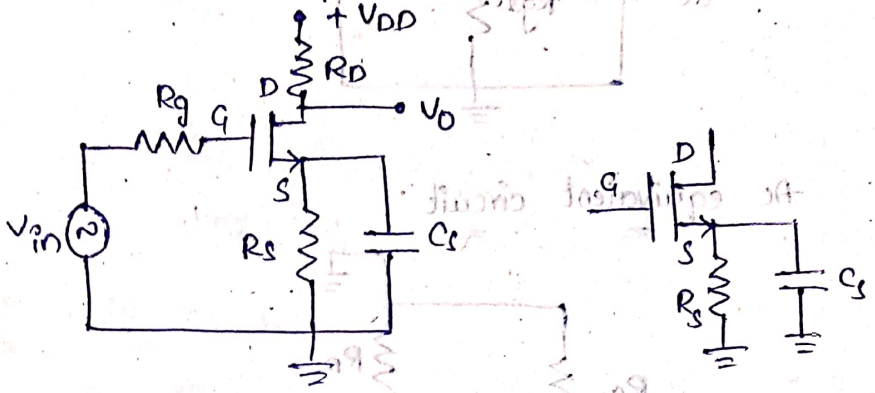
(i)



(ii)



(iii) common Source amplifier with R_S & C_S.



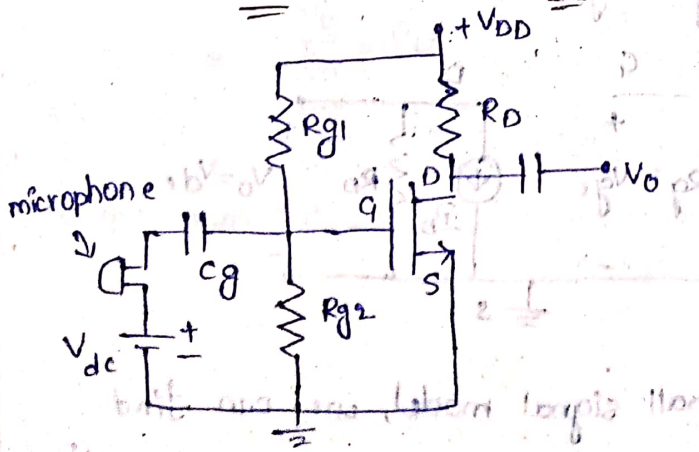
R_S reduces the voltage gain and increase stability.

$$\text{Stability} \propto \frac{1}{\text{voltage gain}} \quad \text{stability} \propto \frac{1}{\text{gain}}$$

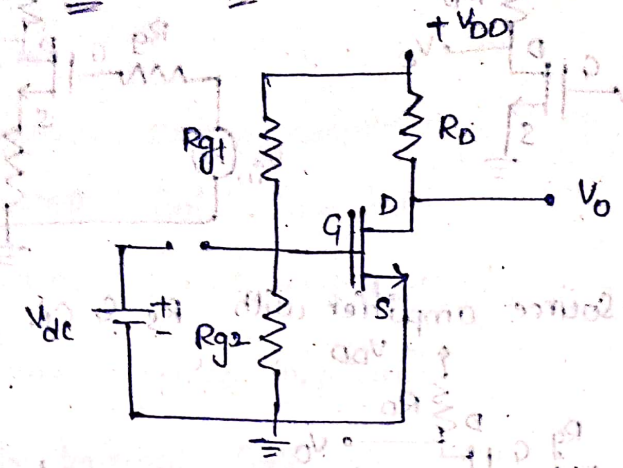
By placing C_S in parallel to R_S, the reduction in voltage gain doesn't takes place. In ac, capacitor becomes short circuit and voltage, current passes through it without any reduction.

Therefore (i) and (iii) conditions are same.

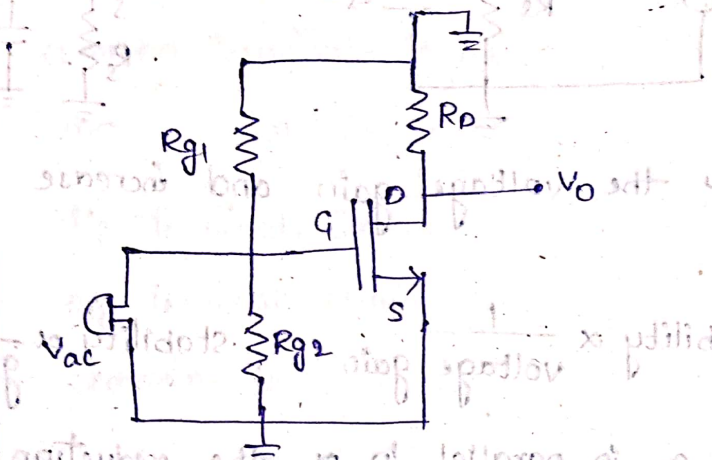
(i) common Source without R_S.



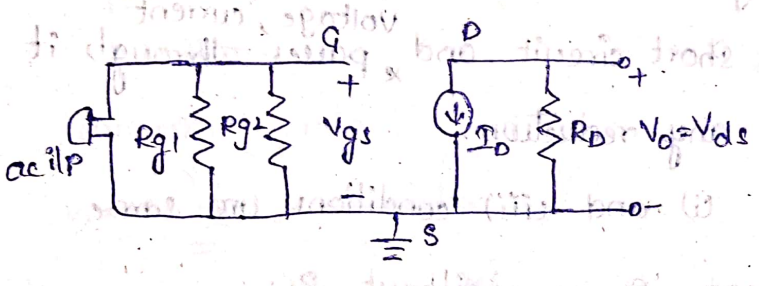
dc equivalent circuit:



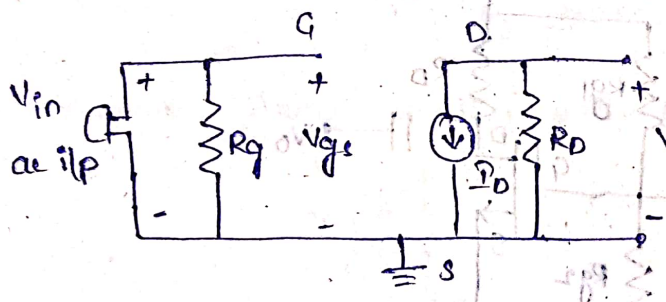
ac equivalent circuit:



Small signal model:



$R_g = R_{g1} \parallel R_{g2}$



By using small signal model, we can find input resistance, output resistance and voltage gain.

Input resistance (R_i) :

$$R_i = \frac{V_{in}}{I_{in}}$$

Apply KVL for the input loop

$$-V_{in} + I_{in} R_g = 0$$

$$V_{in} = I_{in} R_g$$

$$\frac{V_{in}}{I_{in}} = R_g$$

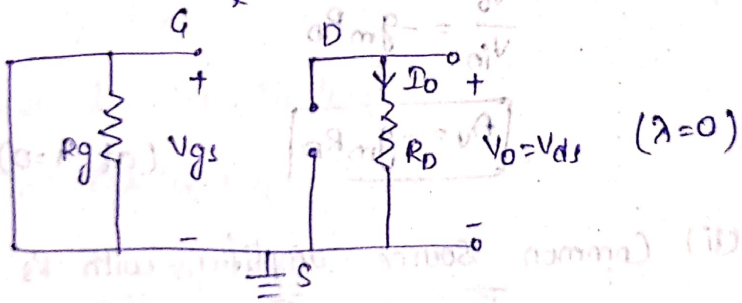
$$\boxed{R_i = R_g}$$

Output resistance (R_o) :

$$R_o = \frac{V_o}{I_o}$$

* short circuit the externally applied input voltage source.

* Open circuit the internal current source.



from the circuit,

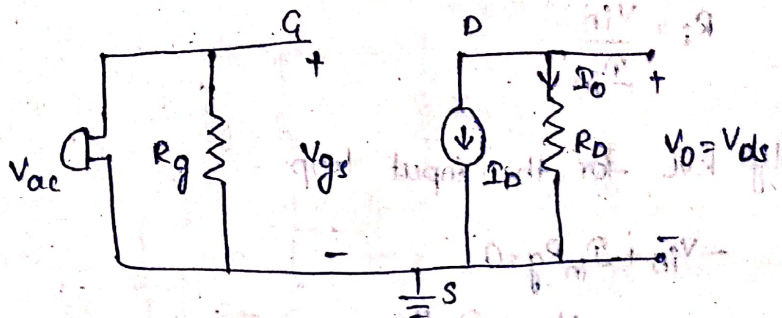
$$V_o = I_o R_D$$

$$\frac{V_o}{I_o} = R_D$$

$$\boxed{R_o = R_D}$$

* If $\lambda \neq 0$, $R_o = R_D \| r_o$

Voltage gain (A_V):



$$A_V = \frac{V_o}{V_{in}} \longrightarrow (1)$$

from the circuit, $V_o = I_o R_D \longrightarrow (2)$

$$I_o + I_D = 0$$

$$I_o = -I_D$$

$$I_o = -g_m V_{gs}$$

$$I_o = -g_m V_{in} \longrightarrow (3)$$

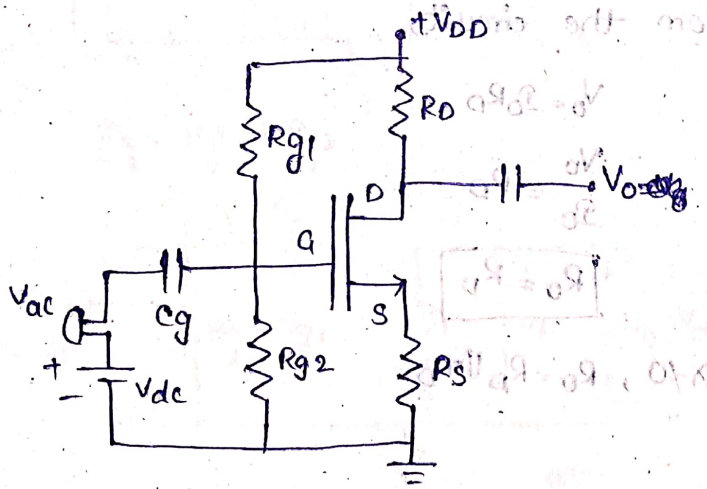
Substitute (3) in (2),

$$V_o = -g_m V_{in} R_D$$

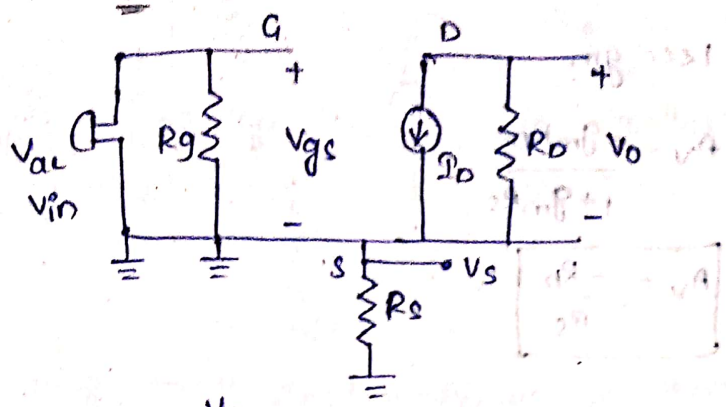
$$\frac{V_o}{V_{in}} = -g_m R_D$$

$$\boxed{A_V = -g_m R_D} \quad (\text{at } \lambda = 0)$$

(ii) Common Source amplifier with R_S:



Voltage gain (A_V):



$$A_V = \frac{V_o}{V_{in}} \rightarrow (1)$$

From the circuit, $V_o = I_o R_D \rightarrow (2)$

$$I_o + I_D = 0$$

$$I_o = -I_D$$

[-ve sign indicates out of phase]

$$I_o = -g_m V_{gs}$$

$$I_o = -g_m V_{in}$$

$$V_o = -g_m V_{gs} R_D \rightarrow (3)$$

from the circuit,

$$V_s = I_D R_s$$

Apply KVL for the i/p loop

$$-V_{in} + V_{gs} + V_s = 0$$

$$V_{in} = V_{gs} + V_s$$

$$V_{in} = V_{gs} + I_D R_s$$

$$V_{in} = V_{gs} + g_m V_{gs} R_s$$

$$V_{in} = V_{gs}(1 + g_m R_s) \rightarrow (4)$$

Substitute (3) and (4) in (1),

$$A_V = \frac{-g_m V_{gs} R_D}{V_{gs}(1 + g_m R_s)}$$

$$\boxed{A_V = \frac{-g_m R_D}{1 + g_m R_s}}$$

Scanned with OKEN Scanner

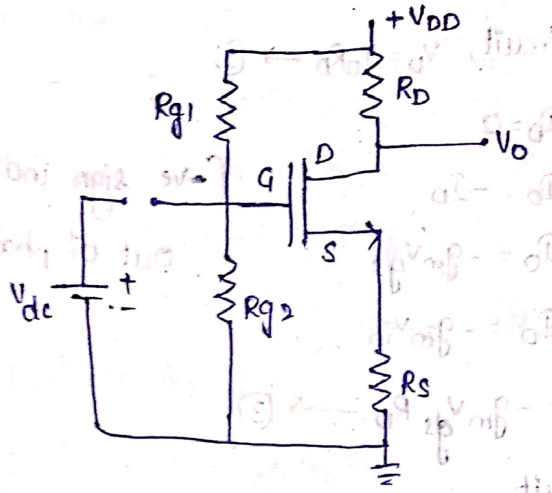
If $R_S \uparrow$, gain $\downarrow \Rightarrow$ stability $\uparrow$.

If $1 \ll g_m$

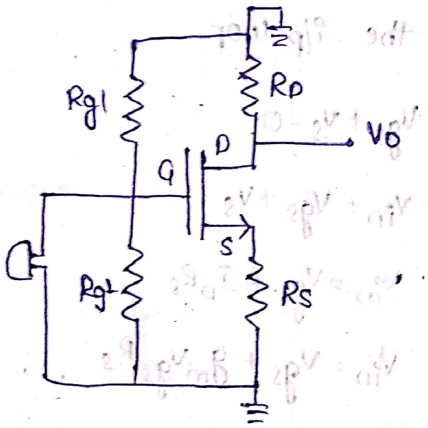
$$A_V = \frac{-g_m R_D}{1 + g_m R_S}$$

$$\boxed{A_V = \frac{-R_D}{R_S}}$$

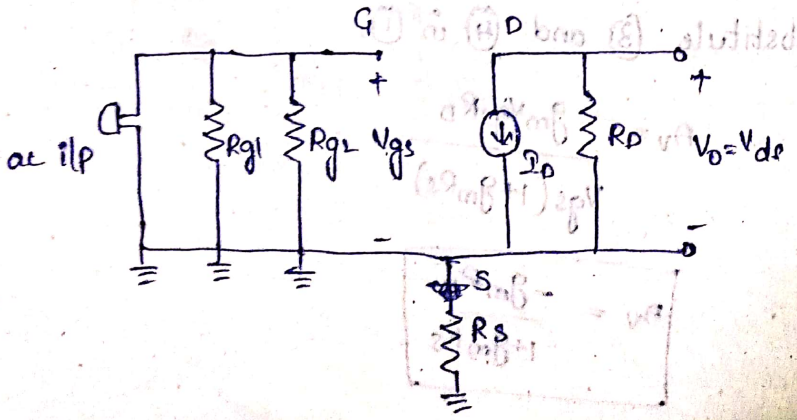
DC equivalent circuit:



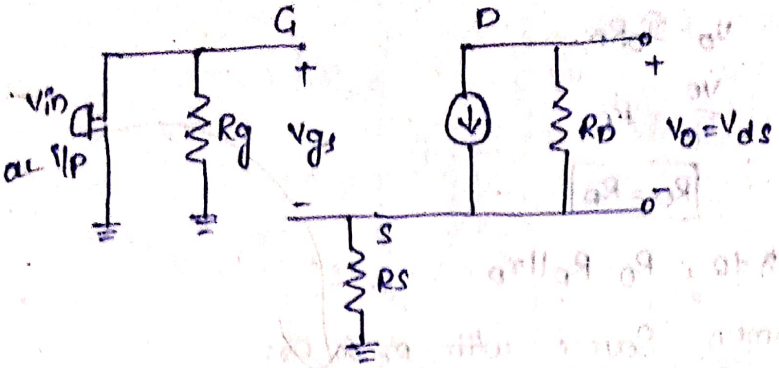
Ac equivalent circuit:



Small signal model:



$R_g = R_{g1} \parallel R_{g2}$



By using small signal model, we can find input resistance, output resistance and voltage gain.

Input resistance (R_i):

$$R_i = \frac{V_{in}}{I_{in}}$$

Apply KVL for the input loop

$$-V_{in} + I_{in} R_g = 0$$

$$V_{in} = I_{in} R_g$$

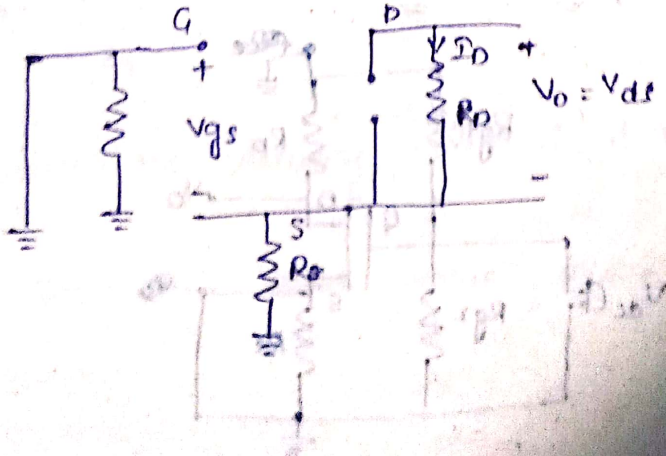
$$\frac{V_{in}}{I_{in}} = R_g$$

$$\boxed{R_i = R_g}$$

Output resistance (R_o):

$$R_o = \frac{V_o}{I_o}$$

* short circuit the externally applied input voltage source.
* open circuit the internal current source.



from the circuit,

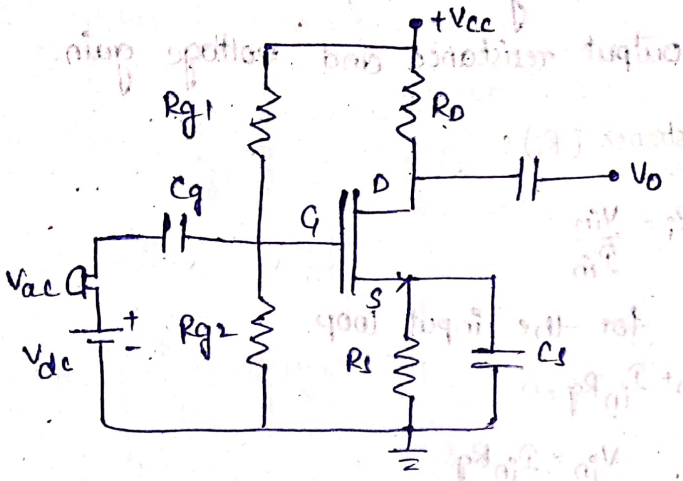
$$V_o = I_o R_D$$

$$\frac{V_o}{I_o} = R_o$$

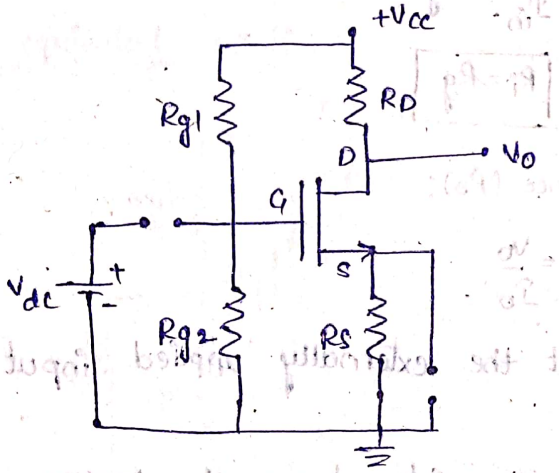
$$\boxed{R_o = R_D}$$

* If $\lambda \neq 0$, $R_o = R_D \| r_D$.

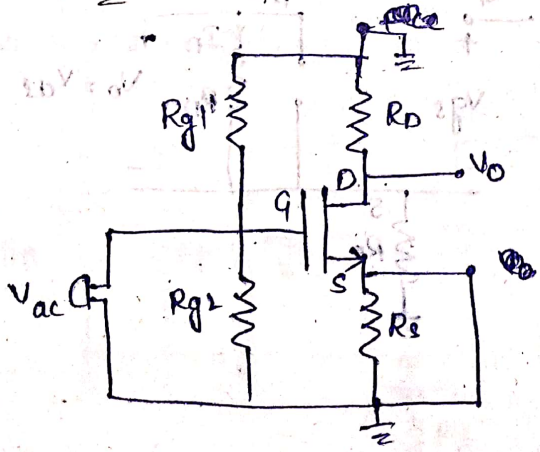
(iii) Common Source with R_S & C_S:

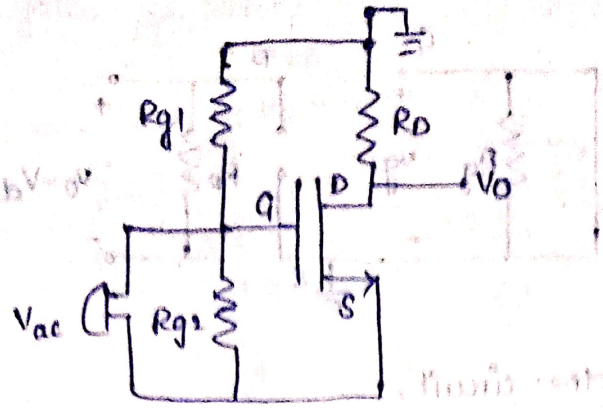


DC equivalent circuit:

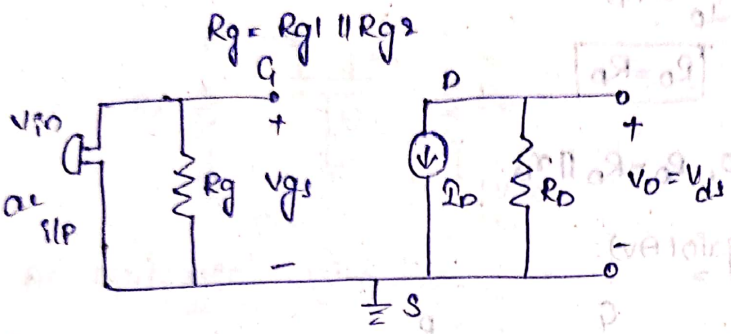


Ac equivalent circuit:





Small Signal model:



Input resistance (R_i):

$$R_i = \frac{V_{in}}{I_{in}}$$

Apply KVL for the input loop

$$-V_{in} + I_{in} R_g = 0$$

$$V_{in} = I_{in} R_g$$

$$\frac{V_{in}}{I_{in}} = R_g$$

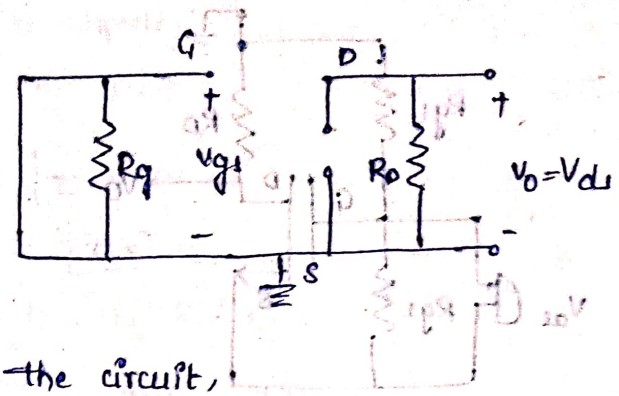
$$\boxed{R_i = R_g}$$

Output resistance (R_o):

$$R_o = \frac{V_o}{I_o}$$

* short circuit the externally applied input voltage source.
* Open circuit the internal current source.

Scanned with OKEN Scanner



from the circuit,

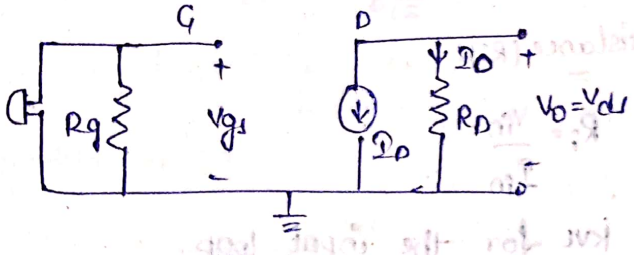
$$V_o = I_o R_D$$

$$\frac{V_o}{I_o} = R_D$$

$$\boxed{R_o = R_D}$$

* If $\lambda \neq 0$, $R_o = R_D \| r_o$.

Voltage gain (A_v):



$$A_v = \frac{V_o}{V_{in}} \rightarrow (1)$$

from the circuit, $V_o = I_o R_D \rightarrow (2)$

$$I_o + I_D = 0$$

$$I_o = -I_D$$

$$I_o = -g_m V_{gs}$$

$$I_o = -g_m V_{in} \rightarrow (3)$$

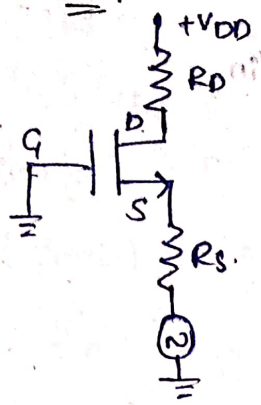
Substitute (3) in (2),

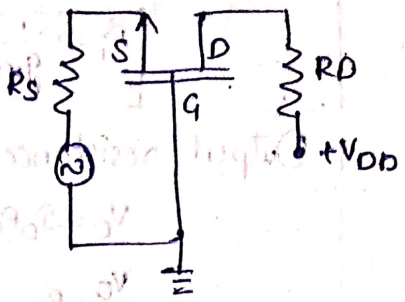
$$V_o = -g_m V_{in} R_D$$

$$\frac{V_o}{V_{in}} = -g_m R_D$$

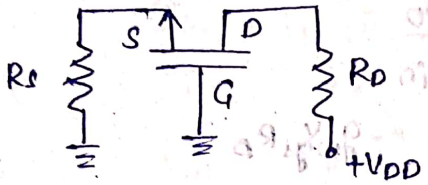
$$\boxed{A_v = -g_m R_D} \quad (\text{at } \lambda = 0).$$

(2) Common gate amplifier:

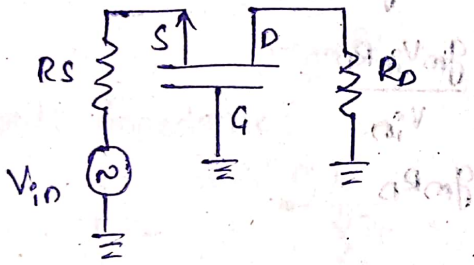




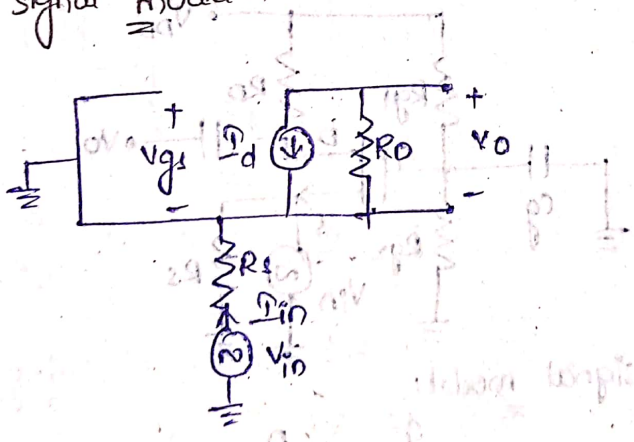
DC equivalent circuit:



AC equivalent circuit:



Small signal model:



Input resistance:

$$I_{in} = -I_d$$

$$I_{in} = -g_m V_{gs}$$

$$V_{sg} = V_{in}$$

$$I_{in} = g_m V_{in}$$

Scanned with OKEN Scanner

$$R_i = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{g_m V_{in}}$$

$$\boxed{R_i = \frac{1}{g_m}}$$

Output resistance:

$$V_o = I_o R_D$$

$$\frac{V_o}{I_o} = R_D$$

$$R_D = R_o$$

Voltage gain: $A_V = \frac{V_o}{V_{in}}$

$$V_o = I_o R_D = -g_m V_{gs} R_D$$

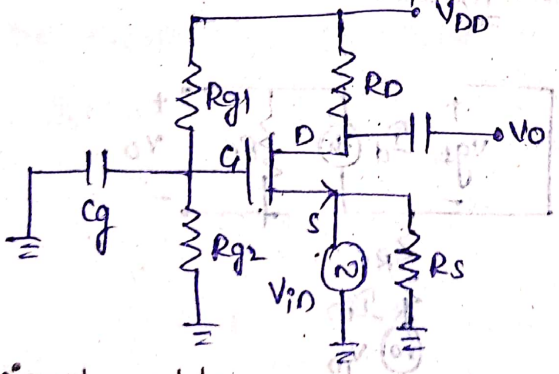
$$= g_m V_{sg} R_D$$

$$V_o = g_m V_{in} R_D$$

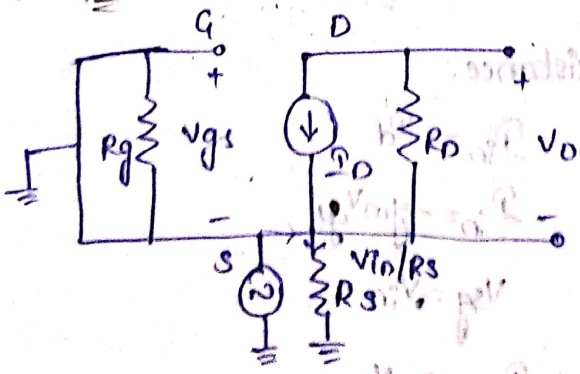
$$A_V = \frac{g_m V_{in} R_D}{V_{in}}$$

$$A_V = g_m R_D$$

$\Rightarrow$



Small signal model:



$$I_{RS} = \frac{V_{in}}{R_S}$$

$$I_{in} + I_D = I_{RS} \qquad V_{gs} = -V_{in}$$

$$I_{in} + g_m V_{gs} = V_{in}/R_S$$

$$I_{in} + (-g_m V_{in}) = (V_{in}/R_S)$$

$$I_{in} = g_m V_{in} + \frac{V_{in}}{R_S}$$

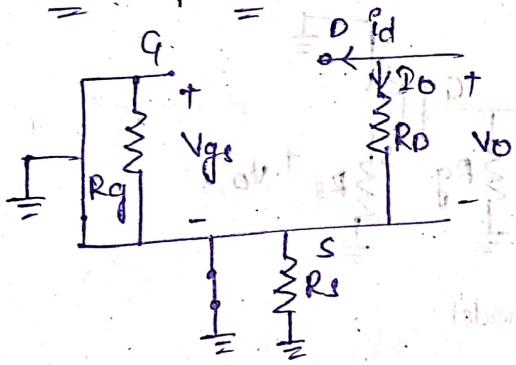
$$I_{in} = V_{in}\left(\frac{1}{R_S} + g_m\right)$$

$$\frac{I_{in}}{V_{in}} = \frac{1+g_m R_S}{R_S}$$

$$\frac{V_{in}}{I_{in}} = \frac{R_S}{1+g_m R_S}$$

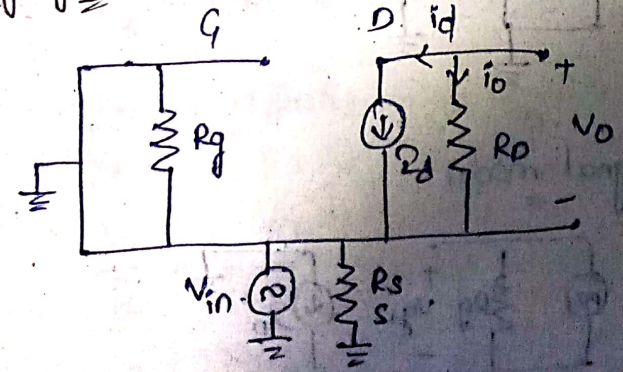
$$R_i = \frac{R_S}{1+g_m R_S}$$

Output impedance:



$$\frac{V_o}{I_D} = R_D \Rightarrow R_o = \frac{V_o}{I_D}$$

Voltage gain:



$$A_V = \frac{V_o}{V_{in}}$$

$$V_o = i_o R_D = g_m V_{in} R_D$$

$$A_V = \frac{V_o}{V_{in}} = \frac{g_m V_{in} R_D}{V_{in}}$$

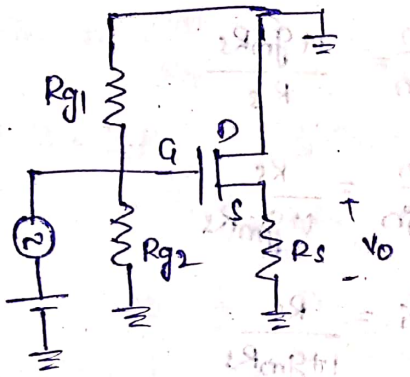
$$A_V = g_m R_D$$

$i_o = -i_d$

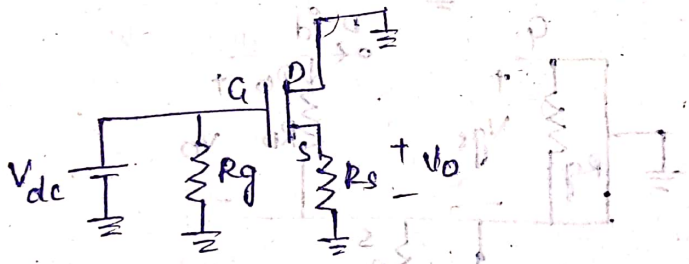
$= -g_m V_{gs}$

$= g_m V_{in}$

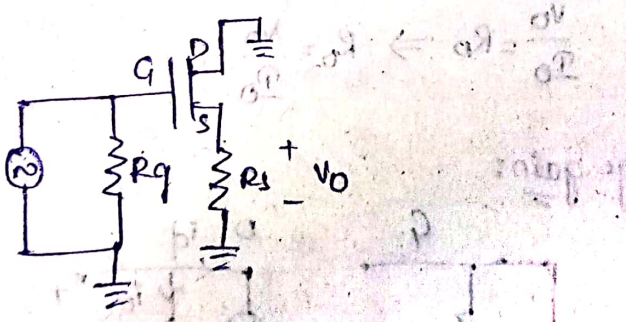
(3) Common drain amplifier (Source follower)



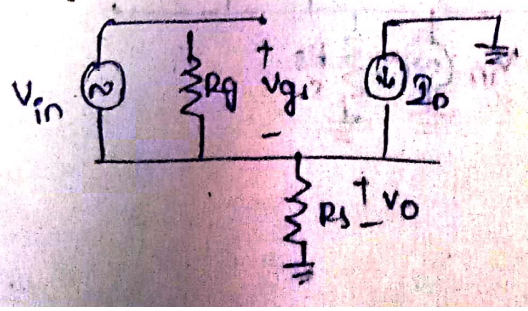
dc equivalent model:



ac equivalent model:



Small signal model:



Scanned with OKEN Scanner

Input resistance:

$$\frac{V_{in}}{I_{in}} = R_i$$

Apply KVL to input loop

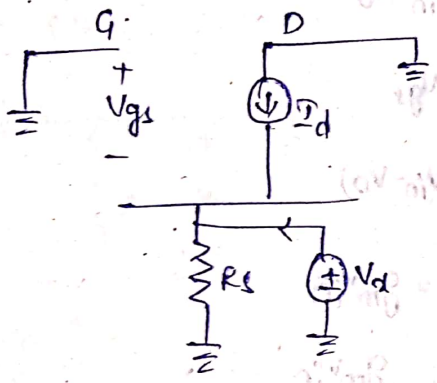
$$-V_{in} + I_{in} R_g = 0$$

$$I_{in} R_g = V_{in}$$

$$R_g = \frac{V_{in}}{I_{in}}$$

$$R_i = R_g$$

Output resistance:



$$V_{gs} = -V_x$$

$$i_d + i_x = V_x / R_s$$

$$g_m V_{gs} + i_x = V_x / R_s$$

$$i_x = V_x / R_s - g_m V_{gs}$$

$$i_x = \frac{V_x}{R_s} + g_m V_x$$

$$\frac{i_x}{V_x} = \left(\frac{1}{R_s} + g_m\right)$$

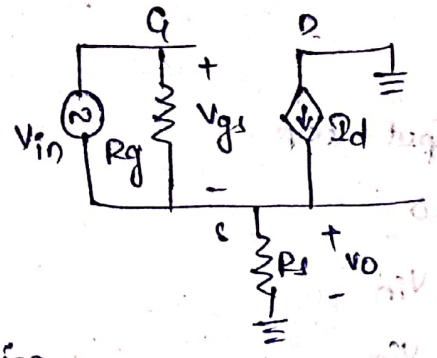
$$\frac{i_x}{V_x} = \frac{1 + g_m R_s}{R_s}$$

$$\frac{V_x}{i_x} = \frac{R_s}{1 + g_m R_s}$$

$$R_o = \frac{R_s}{1 + g_m R_s}$$

Scanned with OKEN Scanner

Voltage gain:



Applying KVL,

$$-V_{in}+V_{gs}+V_o=0$$

$$V_{in}=V_{gs}+V_o$$

$$V_{gs}=V_{in}-V_o$$

$$\frac{V_o}{R_s}=g_m V_{gs}$$

$$\frac{V_o}{R_s}=g_m(V_{in}-V_o)$$

$$\frac{V_o}{R_s}+g_m V_o=g_m V_{in}$$

$$\frac{1}{R_s}+g_m=\frac{g_m V_{in}}{V_o}$$

$$\frac{1+g_m R_s}{R_s}=\frac{g_m V_{in}}{V_o}$$

$$\frac{1+g_m R_s}{R_s g_m}=\frac{V_{in}}{V_o}$$

$$\frac{V_o}{V_{in}}=\frac{g_m R_s}{1+g_m R_s}$$

Filters:

* It is a frequency selective network
* It can select certain band of frequency.
* Audio frequency range = 20Hz to 20kHz
* Radio frequency range => 20kHz
* Voice frequency range = 300Hz to 3.4kHz

Scanned with OKEN Scanner

Male = 75Hz

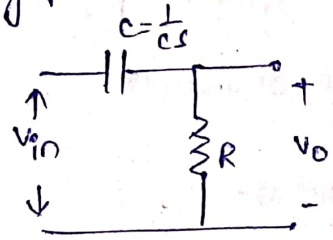
female = 175Hz

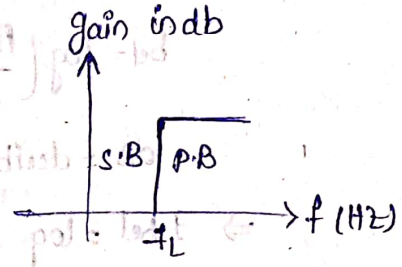
They are divided into two

* pass band – It pass all kind of frequencies
* stop band

Pass band
- LPF – allows only low frequencies
- HPF – allows only high frequencies
- BPF – allows only certain band of frequencies
- BRF – allows frequencies other than the certain band.

Highpass filter

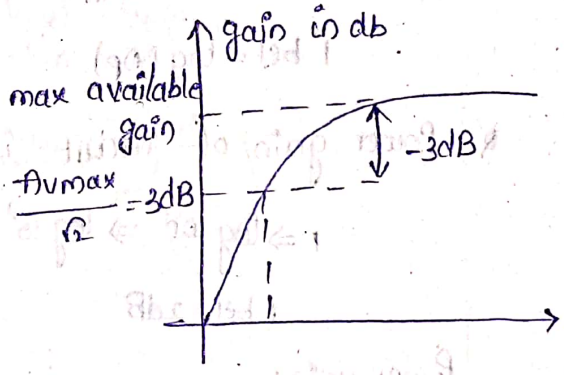




$$V_o = \frac{V_{in} \times R}{\frac{1}{cs} + R}$$

Voltage gain

$$\Rightarrow \frac{V_o}{V_{in}} = \frac{RCs}{1+RCs}$$



$s = j\omega$

$s = j2\pi f$

$$\frac{V_o}{V_{in}} = \frac{RCj\omega}{1+RCj\omega} = \frac{RCj2\pi f}{1+RCj2\pi f} = \frac{j\left(\frac{f}{f_L}\right)}{1+j\left(\frac{f}{f_L}\right)}$$

$f_L = \frac{1}{2\pi RC}$ — f: applied frequency

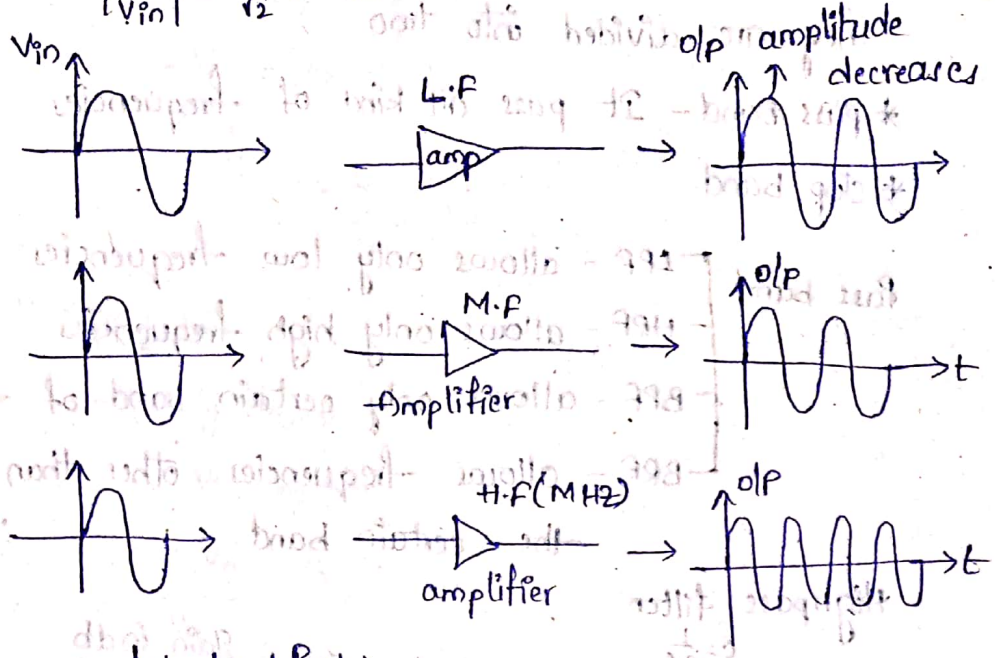
f_L: cutoff frequency

$$Av_{max} \left|\frac{V_o}{V_{in}}\right| = \frac{|f/f_L|}{\sqrt{1+\left(\frac{f}{f_L}\right)^2}}$$

Scanned with OKEN Scanner

at $f = f_L$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{1}{\sqrt{2}} = -3dB$$



$$bel = \log\left(\frac{P_{out}}{P_{in}}\right)$$

dB = decibel

$$\Rightarrow 1\,bel = \log\left(\frac{P_{out}}{P_{in}}\right)$$

$$1\,bel = \log(A_P)$$

Q. Power gain of circuit is 100. Find it in decibels.

$$1 \Rightarrow \log 100 \Rightarrow \log 10^2 \Rightarrow 2$$

1 bel = 2dB

Power gain:

Power gain can be defined as the ratio of output Power to input power

$$A_{pdb} = 10 \log\left(\frac{P_{out}}{P_{in}}\right)$$

$$A_{pdb} = 10 \log(A_P)$$

↳ factor

Q. Represent power gain in terms of decibels with 1000.

$$A_{pdb} = 10\log(1000) = 10\log 10^3 = 10 \times 3$$

$$= 30db$$

Properties of power gain:

(1) Each time the ordinary power gain increases or decreases by a factor of 2, the decibel power gain is increases or decreases by 3db.

factor	decibel
2	3.01 db
0.5	-3.01db
1	0db
10	10db

Voltage gain in db: It can be defined as ratio of output voltage to input voltage.

$$A_v db = 10 \log\left(\frac{P_{out}}{P_{in}}\right)$$

$$= 10 \log\left(\frac{V_{out}}{V_{in}} \cdot \frac{I_{out}}{I_{in}}\right)$$

$$= 10 \log\left(\frac{V_{out}}{V_{in}} \cdot \frac{I_{out}}{I_{in}}\right)$$

$$= 10 \log\left(\frac{V_{out}}{V_{in}} \times \frac{\frac{V_{out}}{R_L}}{\frac{V_{in}}{R_{in}}}\right)$$

If $R_L = R_{in}$

$$\Rightarrow 10 \log\left(\frac{V_o}{V_{in}}\right)^2$$

$$= 20 \log\left(\frac{V_o}{V_{in}}\right)$$

$$A_v (\text{in db}) = 20 \log (A_v)$$

Properties of voltage gain:

Each time the ordinary voltage gain increases or decreases by a factor of 2 other the decibel voltage gain increases or decreases by 6db.

Scanned with OKEN Scanner

factor	decibel
2	6db
0.5	-6db
1	0db
10	20db
20	26db

Current gain in db:

It can be defined as the ratio of output current to input current.

$$A_I \text{ in db} = 10 \log \left(\frac{P_{out}}{P_{in}} \right)$$

$$= 10 \log \left(\frac{V_{out}}{V_{in}} \cdot \frac{I_{out}}{I_{in}} \right)$$

$$= 10 \log \left(\frac{I_{out} R_L}{I_{in} R_{in}} \cdot \frac{I_{out}}{I_{in}} \right)$$

$$= 10 \log \left(\frac{I_{out}^2}{I_{in}^2} \times \frac{R_L}{R_{in}} \right)$$

If $R_L = R_{in}$

$$\Rightarrow 10 \log \left(\frac{I_{out}^2}{I_{in}^2} \right)$$

$$= 20 \log \left(\frac{I_{out}}{I_{in}} \right)$$

$$= 20 \log (A_I)$$

Properties of current gain:

Each time the ordinary current gain increases or decreases by a factor of 2, then the decibel current gain increases or decreases by 6db.

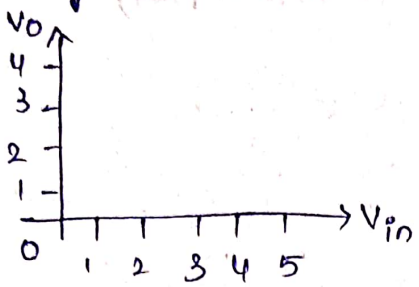
factor	decibel
2	6
0.5	-6
1	0
10	20
20	26

Scanned with OKEN Scanner

Linear Scale and logarithemic Scale:

Linear Scale starts from 0 onwards.

* It is nothing but a ordinary scale. The distance between any two numerical values is equal.



Logarithemic Scale:

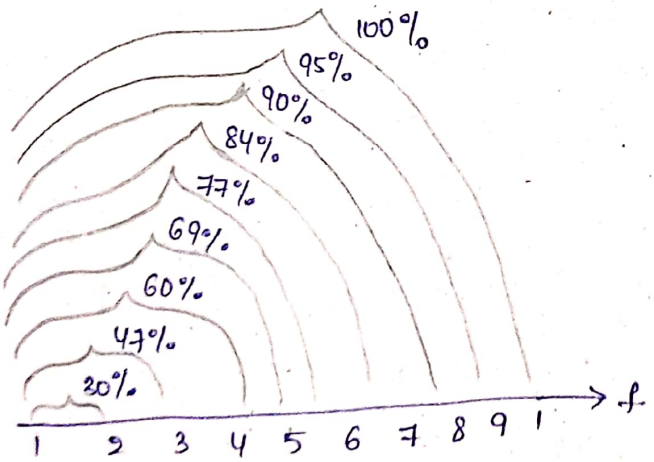
There are two types of logarithemic Scale.

(1) Semi-log scale (one scale is ordinary & other scale is log scale).

(2) Double-log scale (both sides are log scales).

(1) Semi-log Scale:

It must starts from 1 onwards.



$\log_{10} 2 = 0.301 = 30\% \rightarrow (1-2)$

$\log_{10} 3 = 0.477 = 47\% \rightarrow (1-3)$

$\log_{10} 4 = 0.601 = 60\% \rightarrow (1-4)$

$\log_{10} 5 = 0.69 = 69\% \rightarrow (1-5)$

Scanned with OKEN Scanner

$\log_{10}^{6} = 0.77 = 77\% \rightarrow (1-6)$

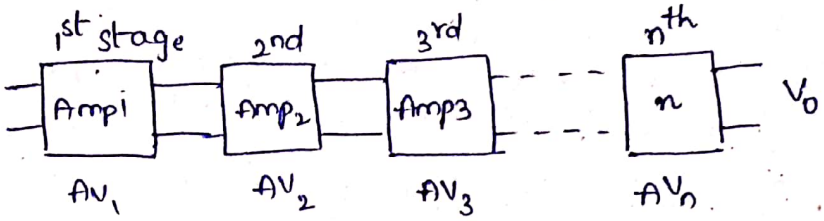
$\log_{10}^{7} = 0.84 = 84\% \rightarrow (1-7)$

$\log_{10}^{8} = 0.903 = 90\% \rightarrow (1-8)$

$\log_{10}^{9} = 0.95 = 95\% \rightarrow (1-9)$

Multistage amplifier: (cascade amplifiers)

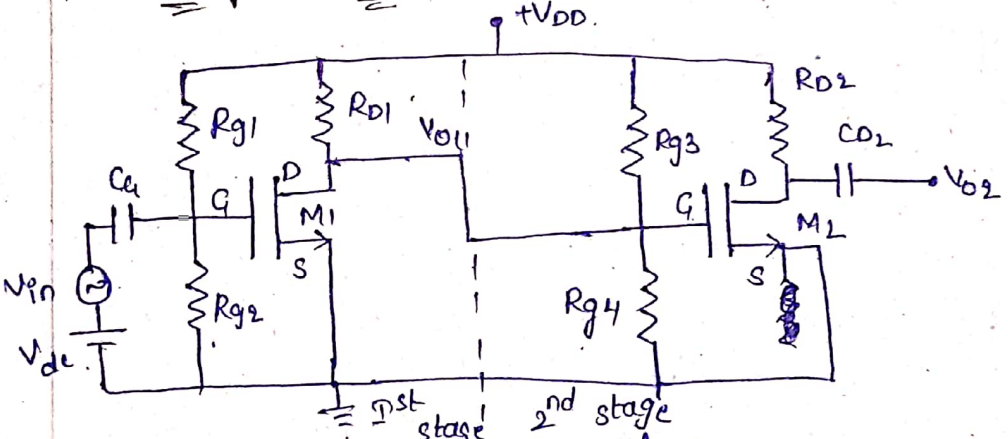
Single stage amplifiers → Gain ≈ 10 to 8



Overall voltage gain $A_V = A_{V_1} \times A_{V_2} \times A_{V_3} \times \dots \times A_{V_n}$.

* Maximum no. of amplifiers that can be used is 7.
* Same type of amplifiers are used in cascade amplifiers.
* If we use different type of amplifiers (CS-CG) then they are called as cascoding amplifiers.
* Small signal voltage gain (mid frequency gain).

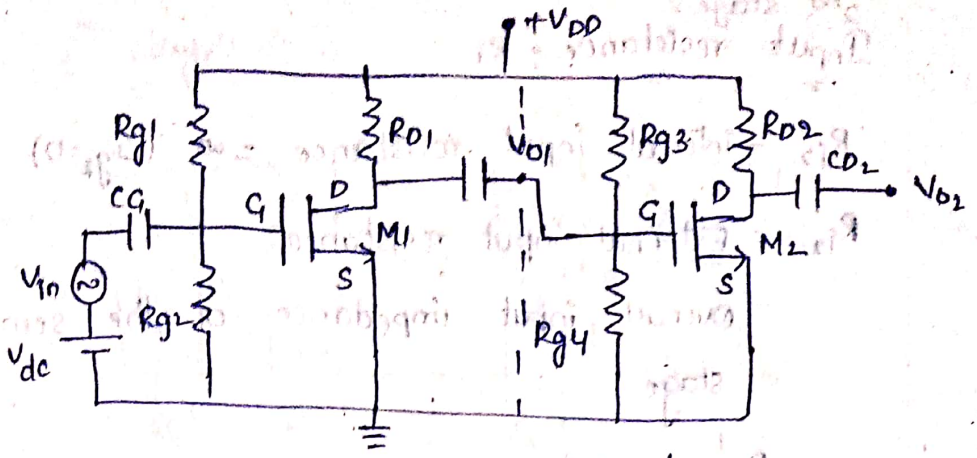
Multistage CS amplifier:



Direct coupled amplifier

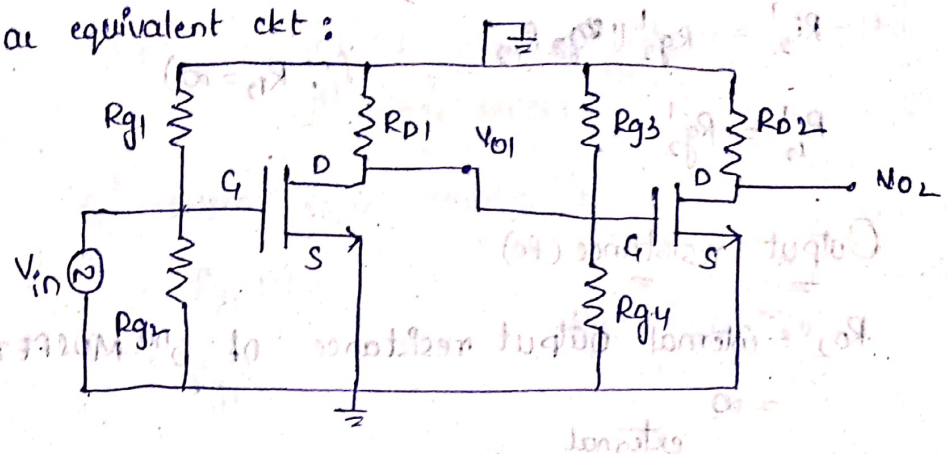
* Disadvantage: Output distorted due to lack of capacitor in the output V_{O1}.
* coupling elements: RC
* RC coupled amplifiers can be used for the above disadvantage.

Scanned with OKEN Scanner

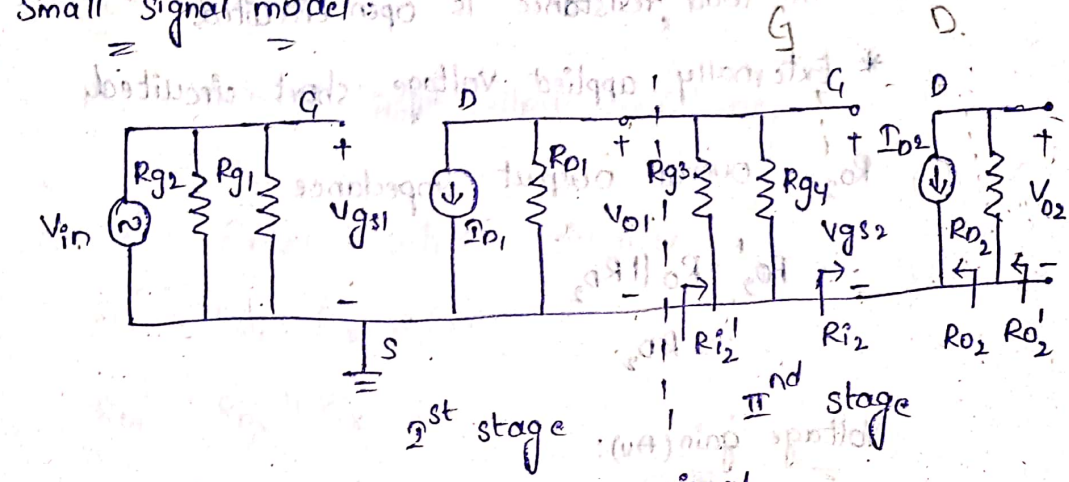


I^st stage II^nd stage

ac equivalent ckt:



Small signal model:



1^st stage II^nd stage

* When we start the small signal analysis of multistage amplifier, we can start analysis from the last stage onwards.

* R_{i_2}' acts as load for 1^st stage

2nd stage:

Input resistance: R_i

R_{i_2} = internal input resistance $= \infty$ $(I_{g_2} = 0)$

R_{i_2}' = External input resistance

overall input impedance of the second stage

$R_{g_2}' = R_{g_3} \parallel R_{g_4}$

$R_{i_2}' = R_{g_2}' \parallel R_{i_2}$ $(\because R_{i_2} = \infty)$

$R_{i_2}' = R_{g_2}'$

Output resistance (R_o):

R_{o_2} = internal output resistance of 2nd MOSFET

$= \infty$

external

* All load resistance is open circuited.

* Externally applied voltage short circuited

R_{o_2}' = overall output impedance

$R_{o_2}' = R_o \parallel R_{D_2}$

$= R_{D_2}$

Voltage gain (A_v):

$A_{v_2} = \frac{V_{o_2}}{V_{o_1}}$

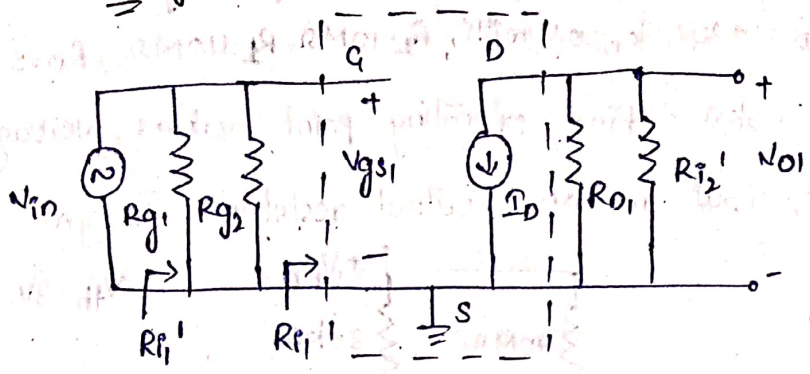
$A_{v_2} = \frac{V_{o_2}}{V_{gs_2}} \times \frac{V_{gs_2}}{V_{o_1}}$ (if no resistance exist in series between V_{o_1}, V_{gs_2} then $V_{o_1} = V_{gs_2}$).

$A_{v_2} = -g_m R_{D_2}$

$A_{v_2} = -g_m R_{o_2}'$ $(\because R_{o_2}' = R_{o_2})$

Scanned with OKEN Scanner

1st stage:



Input impedance:

$R_{i_1} = \infty$ internal input resistance of the 1st stage MOSFET.

R_{i_1}' = overall input resistance.

$= R_{g_1}' \,||\, R_{i_1}$

$R_{g_1}' = R_{g_1} \,||\, R_{g_2}$

$R_{i_1}' = R_{g_1}'$

Output impedance:

R_{o_1} = internal output resistance

$= \infty$

R_{o_1}' = External output resistance.

$R_{o_1}' = R_{D_1} \,||\, R_{i_2}' \,||\, R_{o_1}$

$R_{o_1}' = R_{D_1} \,||\, R_{i_2}'$

Voltage gain (A_V):

$A_{V_1} = -g_m R_{o_1}'$

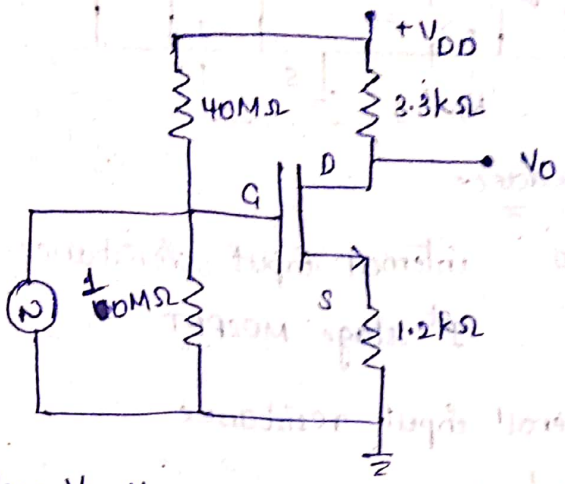
Overall voltage gain, $A_V = \frac{V_{o_2}}{V_{in}}$

$A_V = \frac{V_{o_2}}{V_{o_1}} \times \frac{V_{o_1}}{V_{in}}$

$A_V = -g_{m_2} R_{o_2}' \times -g_{m_1} R_{o_1}'$

$A_V = g_{m_1} g_{m_2} R_{o_1}' R_{o_2}'$

Q. Consider a common source single stage amplifier. $V_{DD} = +30V$, $k_n = 0.4$ mills, $R_1 = 10M\Omega$, $R_2 = 40M\Omega$, $R_D = 2.3k\Omega$, $RS = 1.2k\Omega$. find operating point values, voltage gain, input resistance, output resistance, I_D, g_m.



$V_{th} = 3V$.

$V_{gs} = V_g - V_s$

$= V_{DD} \times \frac{R_2}{R_1+R_2} - I_D R_s$

$= 30 \times \frac{10}{40+10} - I_D R_s$

$= 6 - I_D R_s$

$I_D = k_n (V_{gs} - V_{th})^2$

$I_D = 0.4 \times 10^{-3} (V_{gs} - 3)^2$

$V_{gs} = 6 - 0.4 \times 10^{-3} (V_{gs} - 3)^2 \times 1.2 \times 10^3$

$= 6 - 0.48 (V_{gs}^2 + 9 - 6V_{gs})$

$= -0.48 V_{gs}^2 - 4.32 + 2.88 V_{gs} + 6$

$0 = -0.48 V_{gs}^2 + 2.88 V_{gs} + 1.68 - V_{gs}$

$-0.48 V_{gs}^2 + 1.88 V_{gs} + 1.68 = 0.$

$V_{gs} = 4.667 V,$

$-0.75 V.$ V_{gs} shouldn't be -ve.

$I_D = 0.4 \times 10^{-3} (4.667 - 3)^2 = 1.111 mA$

$I_D = 0.4 \times 10^{-3} (-0.75 - 3)^2 = 5.625 mA$

* $g_m = \frac{2 I_D}{V_{gs} - V_{th}} = \frac{2 \times 1.111 mA}{4.667 - 3}$

$= 1.33 \times 10^{-3} \Omega^{-1}$

Scanned with OKEN Scanner

* Input resistance = $R_1 \| R_2$

$$= \frac{40 \times 10 \times 10^{12}}{(40+10)\,10^6}$$

$$= 8 \times 10^6 \Omega = 8M\Omega$$

* Output resistance = $R_S \| R_D$

$$= \frac{3.96 \times 10^{12}}{4.5 \times 10^6}$$

$$= R_D = 3.3k\Omega$$

* Voltage gain = $\frac{-g_m R_D}{1+g_m R_1}$

$$= \frac{-1.33 \times 10^{-3} \times 3.3 \times 10^3}{1 + 1.33 \times 10^{-3} \times 1.2 \times 10^3}$$

$$= 1.693$$

Relation between internal drain resistance (r_d (or) r_o) and channel length modulation (λ):

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{w}{L} (V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$$

$$\frac{\partial I_D}{\partial V_{DS}} = \frac{1}{2}\mu_n C_{ox} \frac{w}{L} (V_{gs} - V_{th})^2 \frac{d}{\partial V_{DS}} (1 + \lambda V_{DS})$$

$$\frac{\partial I_D}{\partial V_{DS}} = \frac{1}{2}\mu_n C_{ox} \frac{w}{L} (V_{gs} - V_{th})^2 \lambda$$

$$\frac{1}{r_o} = I_D \lambda$$

$$\boxed{r_o = \frac{1}{\lambda I_D}}$$

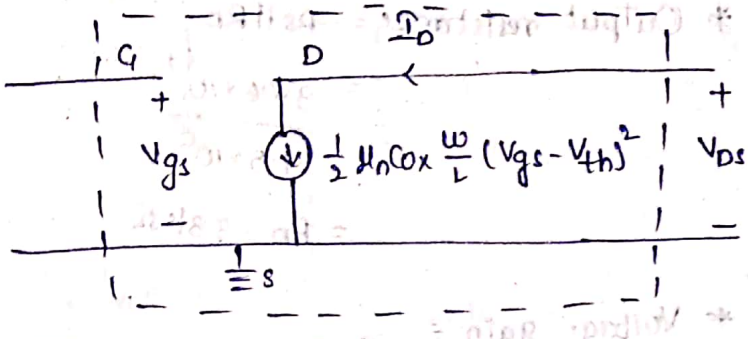
If $\lambda = 0$, $r_o = \infty$ (open circuited)

Scanned with OKEN Scanner

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2 + \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2 \lambda V_{DS}.$$

$$I_D = I_{DO} + \frac{V_{DS}}{r_O} \qquad (\because r_O = \frac{1}{\lambda I_D})$$

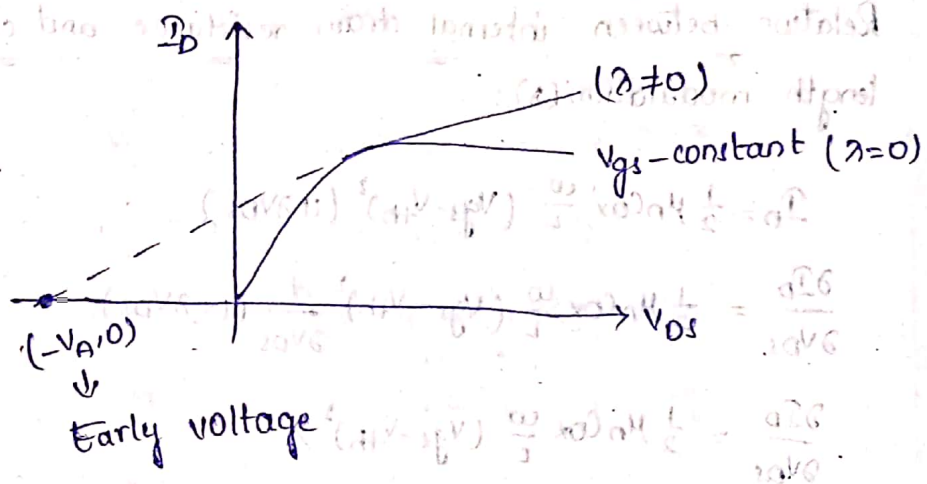
Large signal model:



NMOS FET characteristics:

We know that, Drain current equation due to the channel length modulation is given by

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2(1+\lambda V_{DS}) \longrightarrow (1)$$



Early voltage

from the graphical phenomena, Eq (1) = 0, at Point $(-V_A, 0)$

Replace V_{DS} with $-V_A$.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2(1-\lambda V_A)$$

$$0 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2(1-\lambda V_A)$$

$$V_A = \frac{1}{\lambda} \Rightarrow \lambda = \frac{1}{V_A}$$

Scanned with OKEN Scanner

Substitute $\lambda = \frac{1}{V_A}$ in ①,

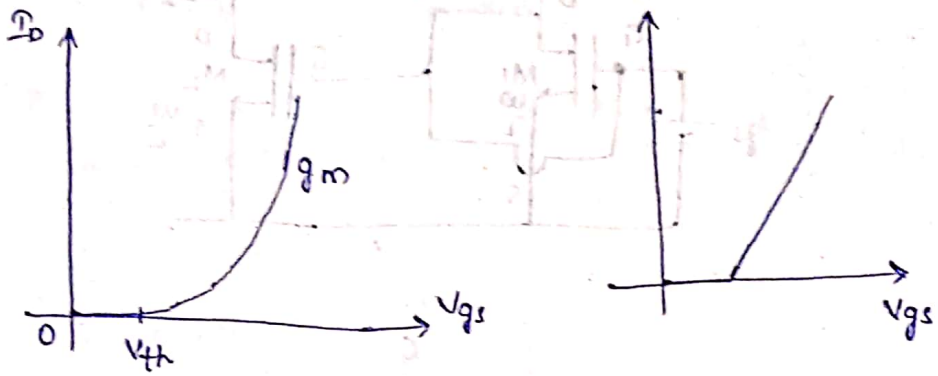
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2\left(1+\frac{V_{DS}}{V_A}\right) \rightarrow \text{Early effect equation}$$

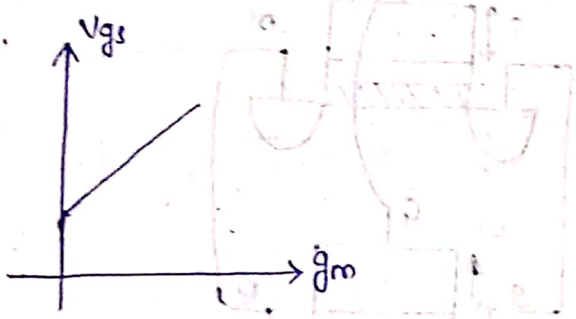
Concept of Transconductance: and more on g_m:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2$$

$$\frac{\partial I_D}{\partial V_{gs}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(2)(V_{gs}-V_{th})$$

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})$$





$$g_m = \frac{2I_{Dmax}}{V_{gs}-V_{th}}$$

$$g_m = \sqrt{2I_{Dmax}\mu_n C_{ox}\frac{W}{L}}$$

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th}).$$

Scanned with OKEN Scanner

Case①: when $V_{gs} - V_{th} \rightarrow$ constant

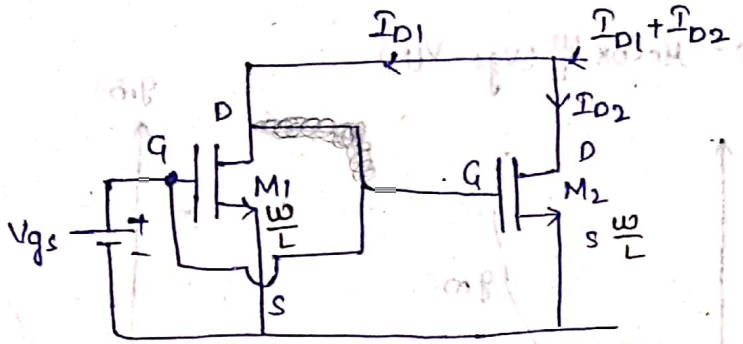
$$g_m \propto \frac{w}{L}$$

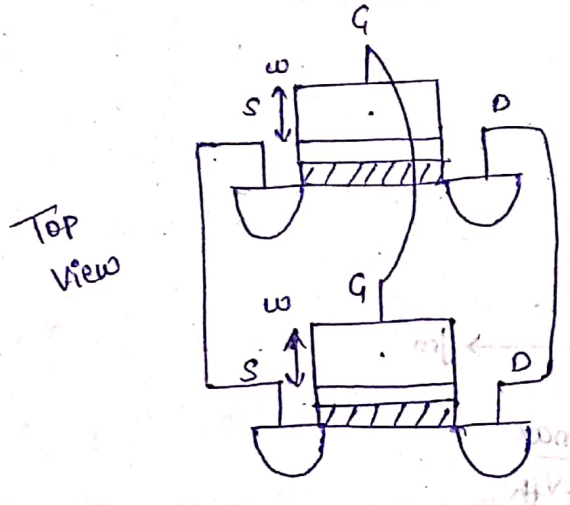
$$g_m \propto (V_{gs} - V_{th}) \rightarrow \frac{w}{L} \text{ constant}$$

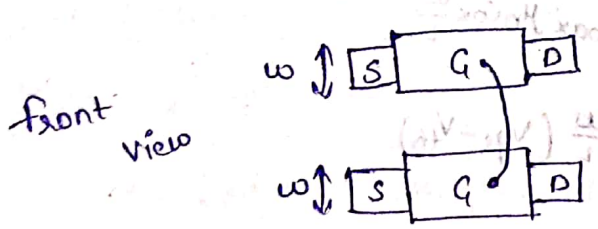
Case②: $I_{Dmax} \rightarrow$ constant

$$g_m \propto \frac{1}{V_{gs} - V_{th}}$$

$$g_m \propto I_{Dmax} \quad [V_{gs} - V_{th} \rightarrow \text{constant}]$$







from the above structure, those two plates are very close to each other. Therefore width doubles.

$$I_{D1} = I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{w}{L}(V_{gs}-V_{th})^2$$

$$I_{D1}+I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{2w}{L}(V_{gs}-V_{th})^2$$

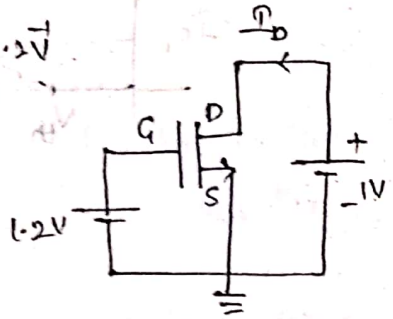
$$g_m = \frac{2I_{D1}}{(V_{gs}-V_{th})}$$

(new) $$g_m = 2\left[\frac{2I_{D1}}{(V_{gs}-V_{th})}\right]$$

Q. Let us consider a NMOS bias circuit

$\mu_n C_{ox} = 100\ \mu A/V^2$, $\frac{w}{L}=10$, $V_{th}=0.5V$, $\lambda=0.2V^{-1}$

Find I_D, g_m, r_o



$V_{gs} = 1.2V$

$$I_D = \frac{1}{2}100\times10^{-6}\times10(1.2-0.5)^2$$

$$= \frac{1}{6}\times10^{-3}\times0.7^2$$

$$= 0.245\ mA$$

$$g_m = \frac{2I_D}{V_{gs}-V_{th}} = 0.7$$

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.2\times0.245\times10^{-3}} = \frac{1}{4.9\times10^{-5}} = 20408.16$$

$$= 20.4\ k\Omega$$

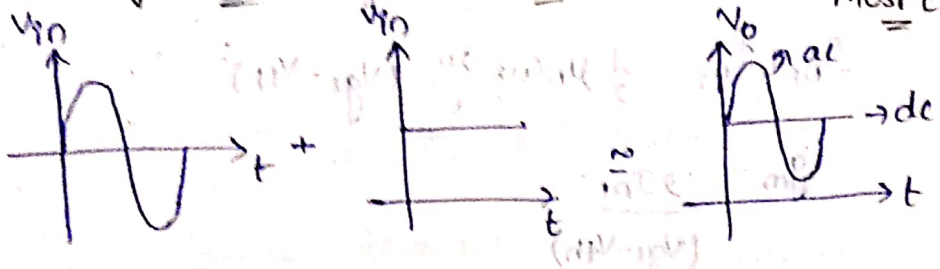
$$I_D = \frac{1}{2}\times100\times10^{-6}\times10(1.2-0.5)^2(1+(0.2)(1))$$

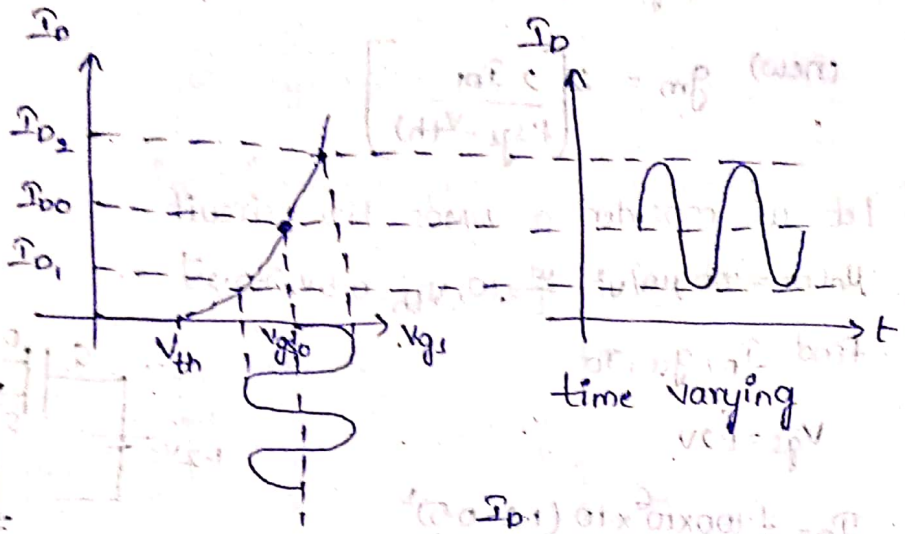
$$= 2.94\times10^{-4}\ A = 0.294\ mA$$

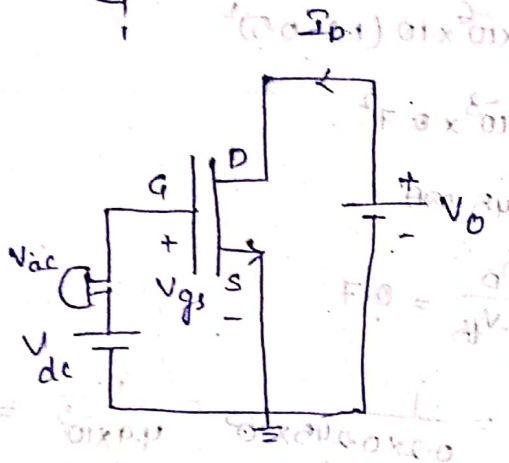
$$r_o = \frac{1}{I_D} = 3.4\ k\Omega$$

Scanned with OKEN Scanner

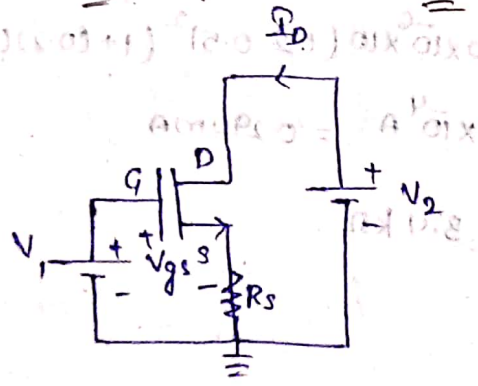
Combining of time response & I/V characteristics of MOSFET:







Large and Small signal operation of MOSFET:



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2$$

$$V_{gs} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}} + V_{th}$$

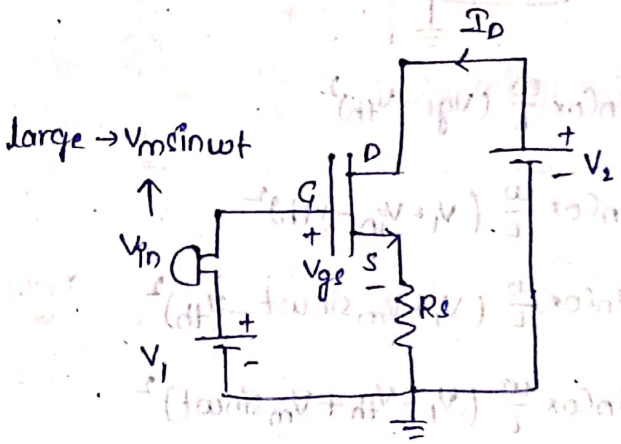
Scanned with OKEN Scanner

Apply KVL for i/p loop.

$$-V_1 + V_{gs} + I_D R_s = 0$$

$$V_1 = V_{gs} + I_D R_s$$

$$\boxed{V_1 = \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{w}{L}}} + V_{th} + I_D R_s}$$

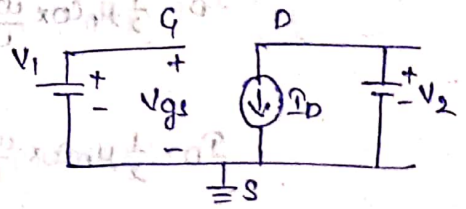


R_s: stabilization resistor

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{w}{L} (V_{gs} - V_{th})^2$$

$$V_{gs} = \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{w}{L}}} + V_{th}$$

large signal Equivalent ckt for



$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{w}{L} (V_{gs} - V_{th})^2$$

Apply KVL for i/p loop

$$-V_{in} - V_1 + V_{gs} + I_D R_s = 0$$

$$V_{in} + V_1 = V_{gs} + I_D R_s$$

$$V_{in} + V_1 = \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{w}{L}}} + V_{th} + I_D R_s$$

$$\boxed{V_1 + V_m \sin\omega t = \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{w}{L}}} + V_{th} + I_D R_s}$$

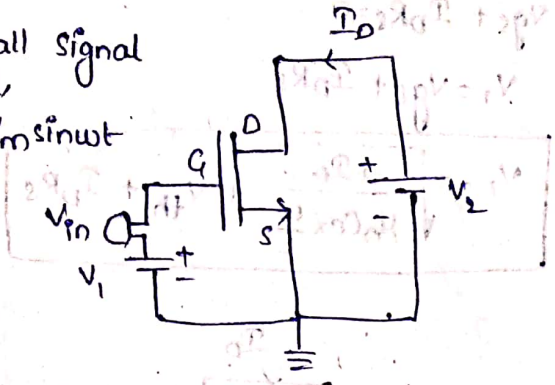
From the above equation, we can concluded that I_D calculations are more massive or complicated. so that it is not a feasable circuit. Due to calculation complications, we can move on to small signal operation.

Scanned with OKEN Scanner

Small signal operation of MOSFET:

Small signal

$V_{in} = V_m \sin\omega t$



KVL for i/p loop

$V_{gs} = V_{in} + V_1$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_1+V_{in}-V_{th})^2$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_1+V_m\sin\omega t-V_{th})^2$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_1-V_{th}+V_m\sin\omega t)^2$$

$V_m \sin\omega t << V_1 - V_{th}$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_1-V_{th})^2\left(1+\frac{V_m\sin\omega t}{V_1-V_{th}}\right)^2$$

$(a+b)^2 = a^2+b^2+2ab$

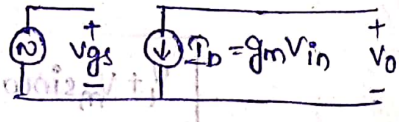
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_1-V_{th})^2\left(1+\frac{2V_m\sin\omega t}{V_1-V_{th}}\right)$$

$(1+x)^2 = 1+2x+x^2$ ↓ ignore

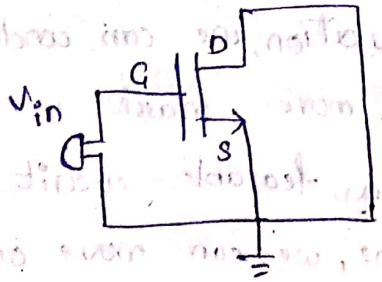
$$I_D = I_{DO}\left(1+\frac{2V_m\sin\omega t}{V_1-V_{th}}\right)$$

$$I_D = I_{DO} + \frac{2I_{DO}}{V_1-V_{th}}\sin\omega t \cdot V_m$$

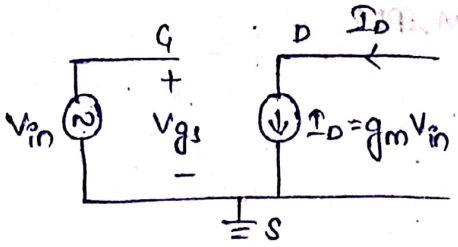
$$\boxed{I_D = I_{DO} + g_m v_{in}} \Rightarrow$$



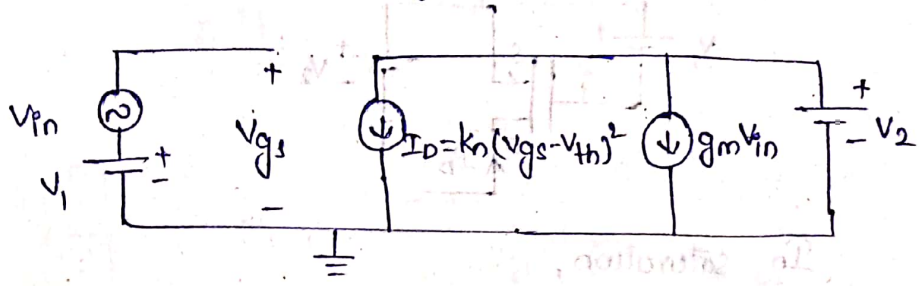
ac equivalent:



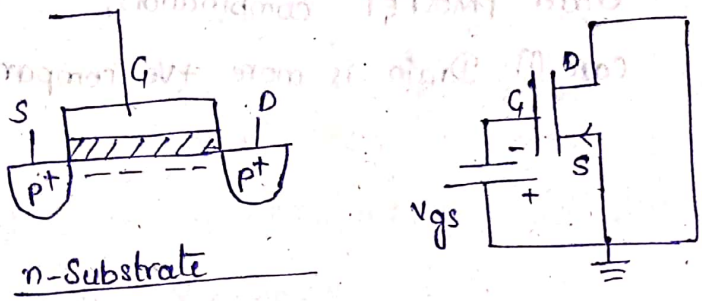
Scanned with OKEN Scanner



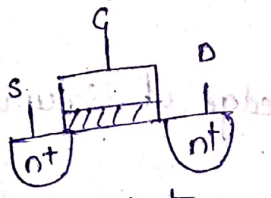
Small signal model for given ckt.



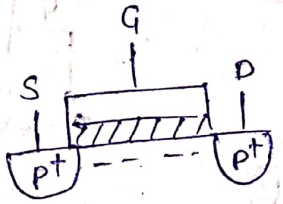
PMOSFET:

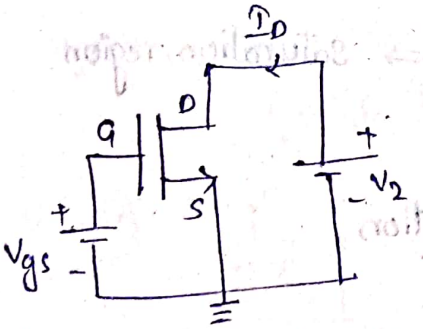


NMOSFET



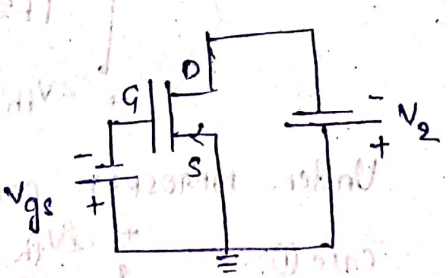
PMOSFET





V_{th} = +ve

gate is more +ve than source



V_{th} = −ve

source is more +ve than V_{gs}.

channel created by default.

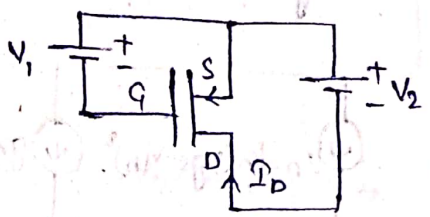
Scanned with OKEN Scanner

conditions for PMOSFET

(i) $V_g < V_s$

(ii) $V_{thp} < 0$

(iii) $V_D < V_s$.

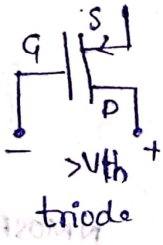


In saturation,

$$I_D = \frac{-1}{2} \mu_p C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 (1 - \lambda V_{DS})$$

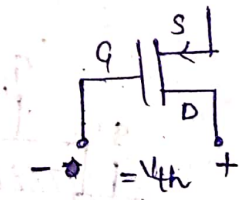
Under PMOSFET combination,

Case (1): Drain is more +ve compared to gate



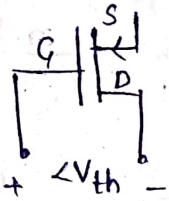
triode

Case (2):



⇒ edge of Saturation

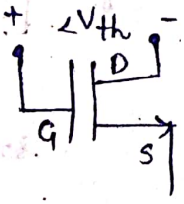
Case (3):



⇒ Saturation region.

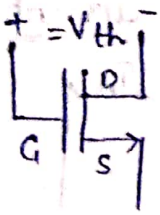
Under NMOSFET combination,

Case (1):

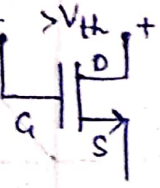


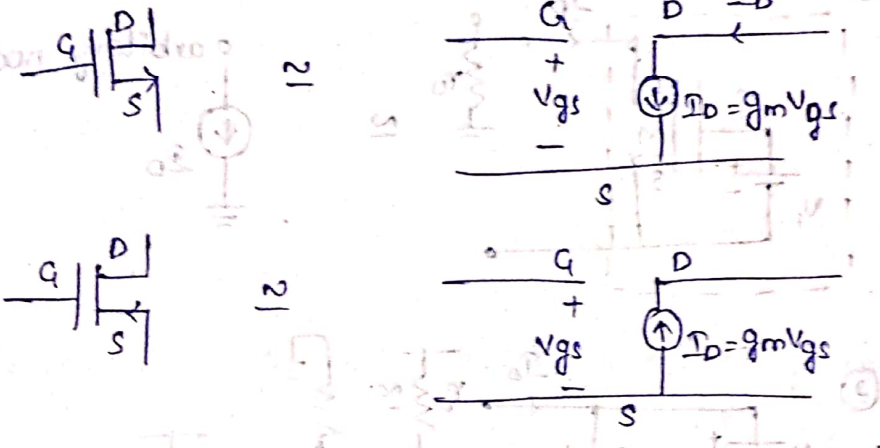
⇒ triode region

Case ②: $+ = V_{th} -$ ⇒ edge of saturation

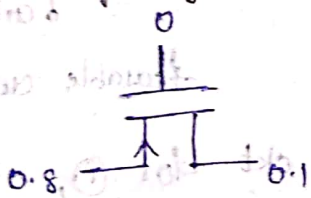


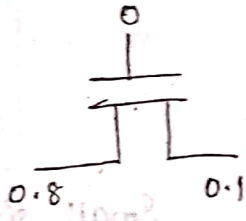
Case ③: $- > V_{th} +$ ⇒ Saturation.





Q Identify the type of MOSFET and also indicate the operating region. $V_{th} = -0.6V$





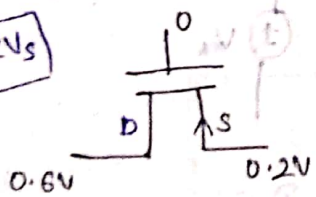
$V_{gs} = V_g - V_S = 0 - 0.8 = -0.8V$

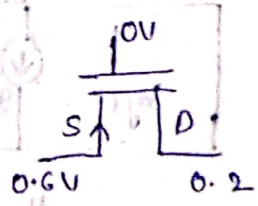
$V_{ds} = V_d - V_S = 0.1 - 0.8 = -0.7V$

$V_{gs} - V_{th} = -0.8 + 0.6 = -0.2 > -0.7$

$V_{gs} - V_{th} > V_{ds}$ (Saturation)

$V_D < V_S$





$V_{gs} = 0 - 0.6 = -0.6V$

$V_{ds} = 0.2 - 0.6 = -0.4V$

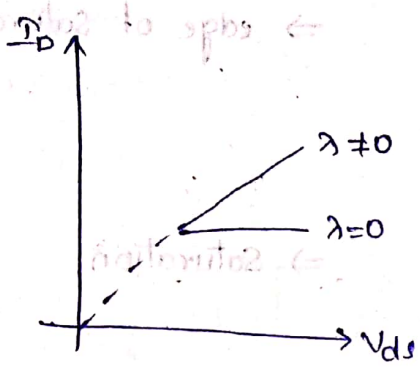
$V_{gs} - V_{th} = -0.6 + 0.6 = 0 > -0.4V$

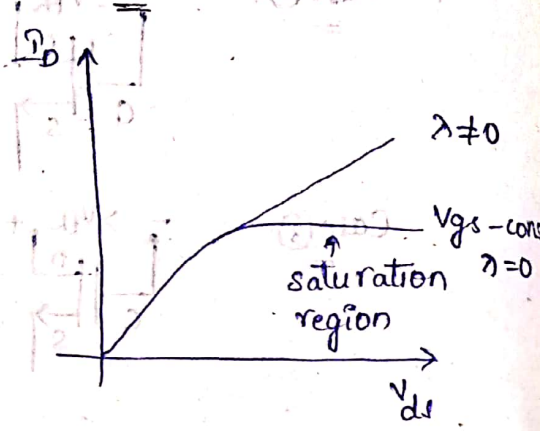
$V_{ds} < V_{gs} - V_{th}$

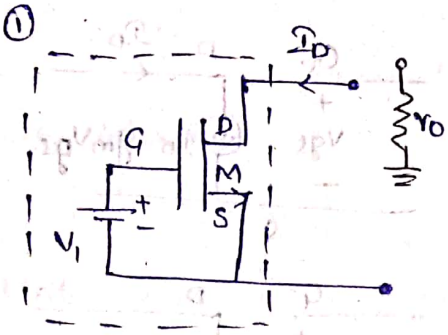
(Saturation)

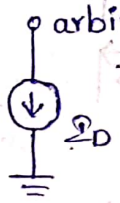
Scanned with OKEN Scanner

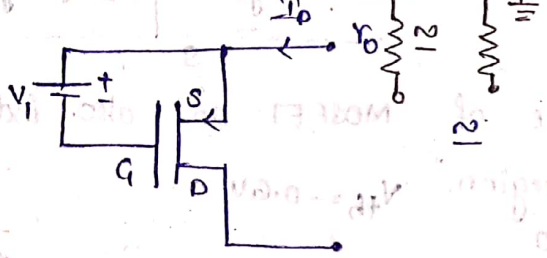
MOSFET as a constant current source:

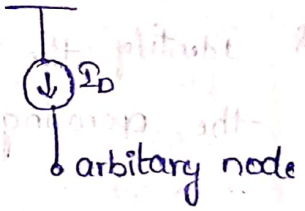




① 

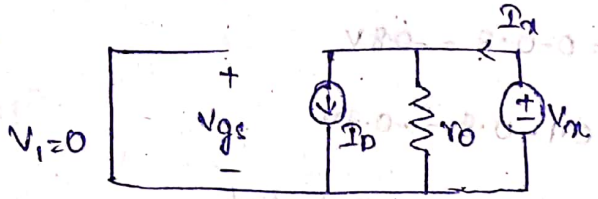
$\cong$ 

② 

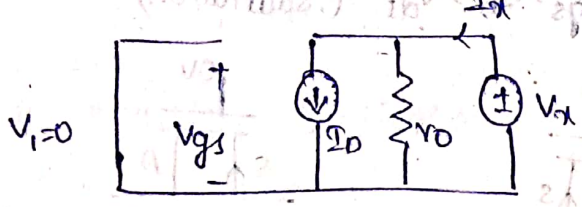
$\cong$ $\cong$ 

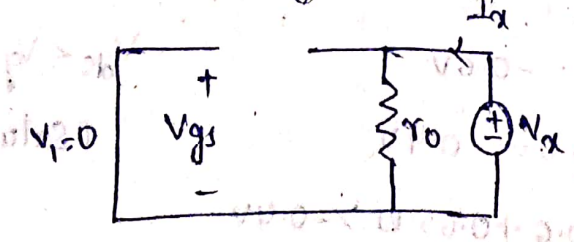
feasable current source

Small signal equivalent ckt for ①,



V_x: Test Voltage



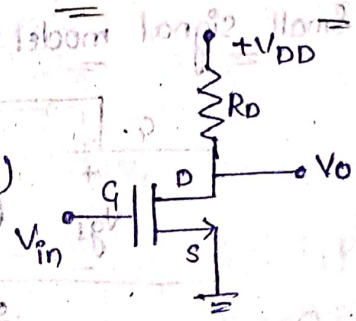


$\frac{V_x}{I_x} = r_o$

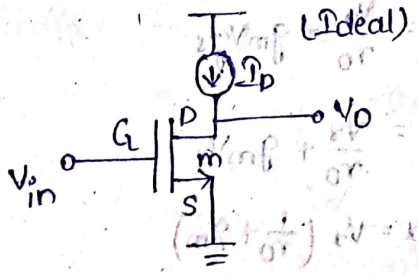
Common Source with constant current source load:

$A_V = -g_m R_D \quad (\lambda = 0)$

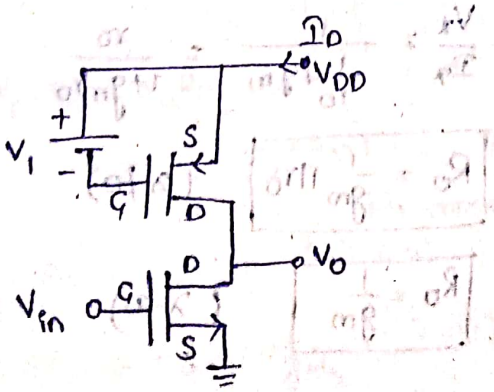
$= -g_m (R_D \| r_O) \quad (\lambda \neq 0)$



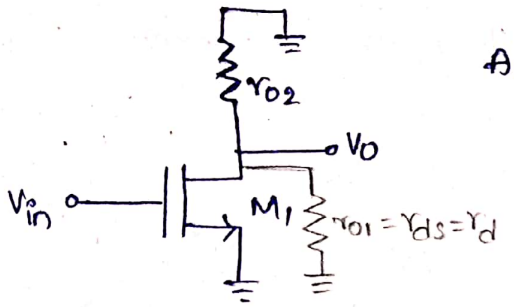
To increase gain, Passive loads are replaced with active loads.



≃



≃

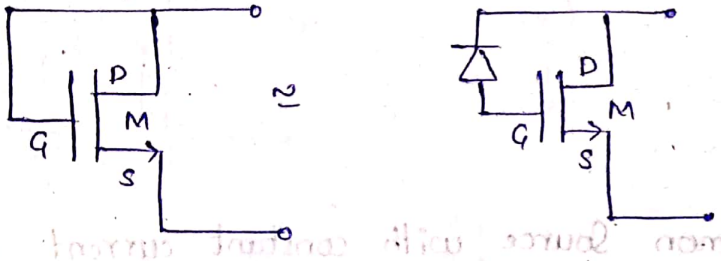


$A_V = -g_m r_{O2}$ $(\lambda = 0)$

$= -g_m (r_{O2} \| r_{O1})$ $(\lambda \neq 0)$

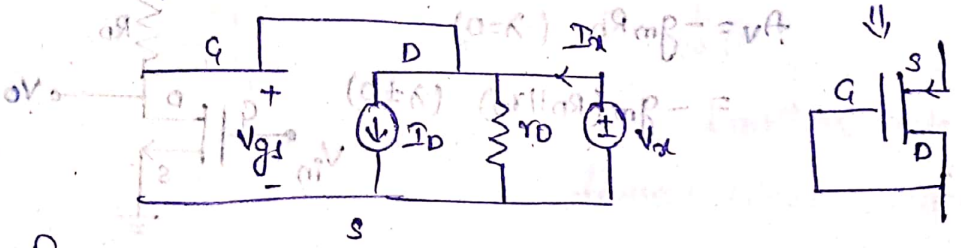
This gain is very high compared to gain in Passive loads.

Diode connected ≃ device can be used as (active load)



Small signal model:

PMOSFET ⇓



from the circuit,

$V_x = V_{gs}$

$I_x = \frac{V_x}{r_O} + g_m V_{gs}$

$I_x = \frac{V_x}{r_O} + g_m V_x$

$I_x = V_x \left(\frac{1}{r_O} + g_m\right)$

$\frac{V_x}{I_x} = \frac{1}{\frac{1}{r_O} + g_m} = \frac{r_O}{1 + g_m r_O}$

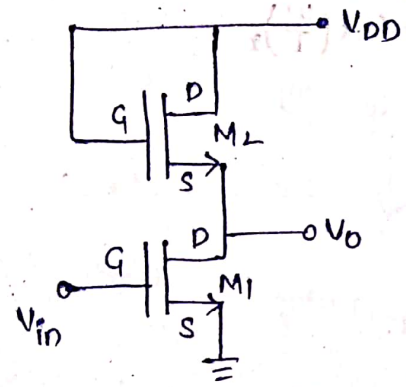
$\frac{1}{g_m} \| r_O = \frac{\frac{1}{g_m} r_O}{\frac{1}{g_m} + r_O} = \frac{r_O}{1 + g_m r_O}$

$\boxed{R_O = \frac{1}{g_m} \| r_O}$ $(\lambda \neq 0)$

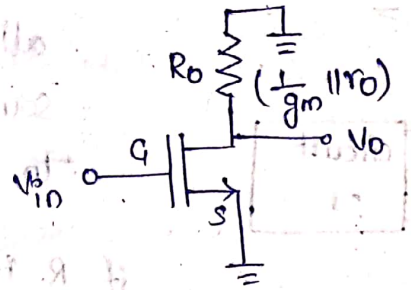
$\boxed{R_O = \frac{1}{g_m}}$ $(\lambda = 0)$

Scanned with OKEN Scanner

MOSFET diode connected device as load:

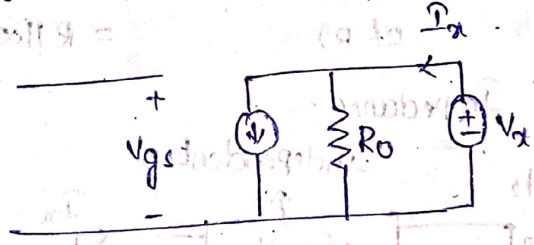


$\approx$



(for $\lambda \neq 0$)

Small signal model:



$A_v = -g_m R_o$

$V_{in} = V_{gs}$

$I_x = \frac{V_x}{R_o} + g_m V_{in}$

$I_x = V_x \left(\frac{1}{R_o} + g_m\right)$

$V_x = \frac{I_x}{\left(\frac{1}{R_o} + g_m\right)}$

$V_o = I_x R_o$

$V_o = -I_D R_o$

$= -g_m V_{gs} \left(\frac{1}{g_m} \| r_o\right)$

$\frac{V_o}{V_{in}} = -g_m R_o$

$V_o = V_x = I_x R_o$

$= V_x \left(\frac{1}{R_o} + g_m\right)$

for M1

for mosfet 2 and $\lambda = 0$

$\left(R_D = \frac{1}{g_m} \| r_o\right)$

$\Rightarrow \frac{V_o}{V_{in}} = A_V = -g_{m_1} R_D \quad (\lambda \neq 0)$

$= -g_{m_1} \cdot \frac{1}{g_{m_2}} \quad (\lambda = 0)$

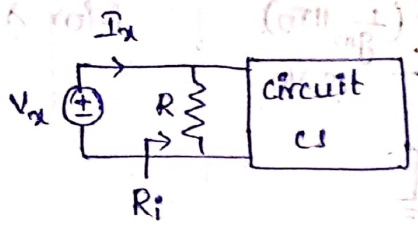
Scanned with OKEN Scanner

$$A_V = \sqrt{\frac{2I_D\mu_n C_{ox}\left(\frac{W}{L}\right)_1}{2I_D\mu_n C_{ox}\left(\frac{W}{L}\right)_2}}$$

$$A_V = \sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

Port Impedances:

Input port Impedance:



all independent sources are equal to zero

$$R_i = \frac{V_x}{I_x} = \infty \text{ (absence of R)}$$

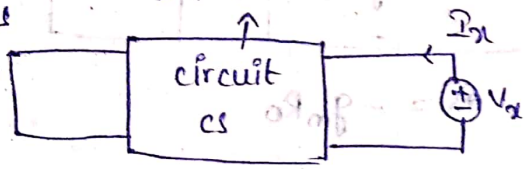
if R is present

$$R_i' = (R \parallel R_i) = R \parallel \infty = R$$

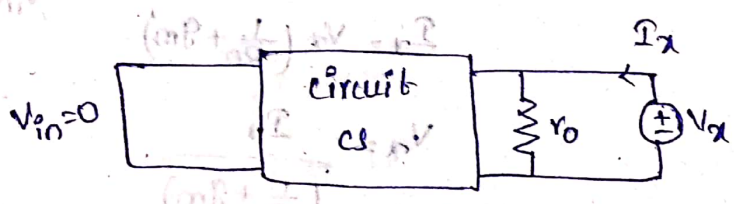
Output port Impedance:

Independent = 0

Input terminals must be short circuited $V_{in}=0$



$$R_O = \frac{V_x}{I_x} = \infty$$



$$R_O = \infty \parallel r_o$$

$$R_O \approx r_o$$

Scanned with OKEN Scanner

Diode connected device as load:

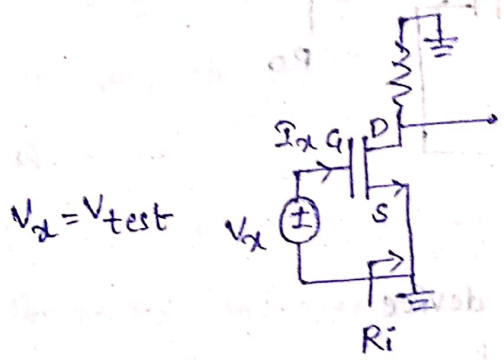
M_1	M_2	A_v
$\lambda=0$	$\lambda=0$	$-g_{m_1}\frac{1}{g_{m_2}}$
$\lambda=0$	$\lambda\neq0$	$-g_{m_1}\left(\frac{1}{g_{m_2}}\|\|r_{o_2}\right)=-g_{m_1}(R_o)$
$\lambda\neq0$	$\lambda=0$	$-g_{m_1}\left(\frac{1}{g_{m_2}}\|\|r_{o_1}\right)$
$\lambda\neq0$	$\lambda\neq0$	$-g_{m_1}\left(\frac{1}{g_{m_2}}\|\|r_{o_1}\|\|r_{o_2}\right)$

Port Impedances:

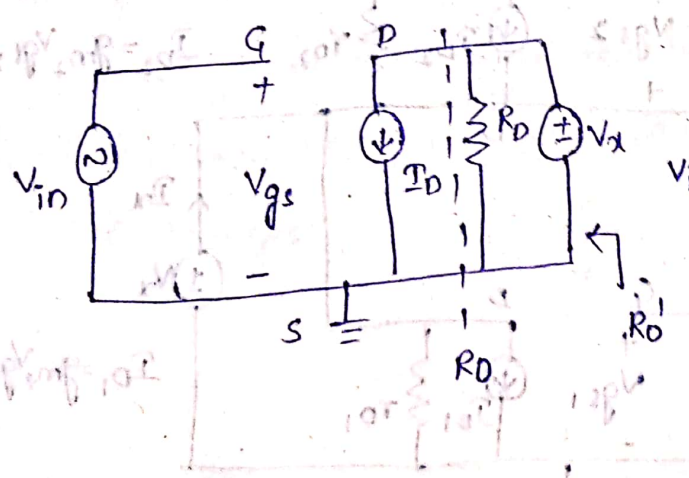
I/o impedances:

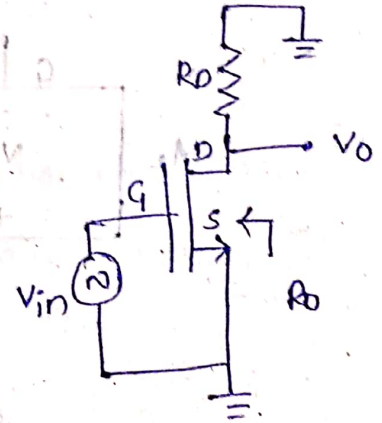
* Small signal
* Replace i/p voltage with test voltage

$$R_i=\frac{V_x}{I_x}=\infty \text{ (open circuited)}$$



* for o/p impedance



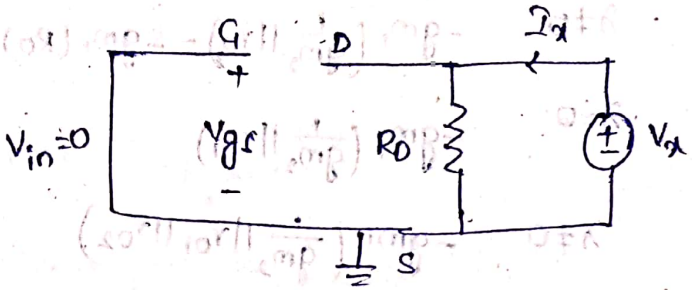


$R_o' = R_o \| R_D \quad (R_o = \infty)$

$R_o' = \infty \| R_D$

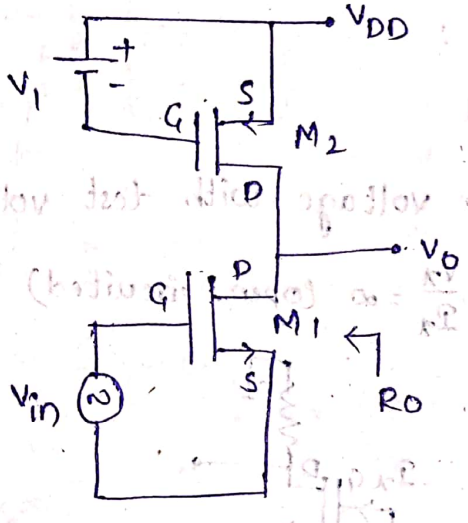
$R_o' = R_D$

$R_o' = \frac{V_x}{I_x}$



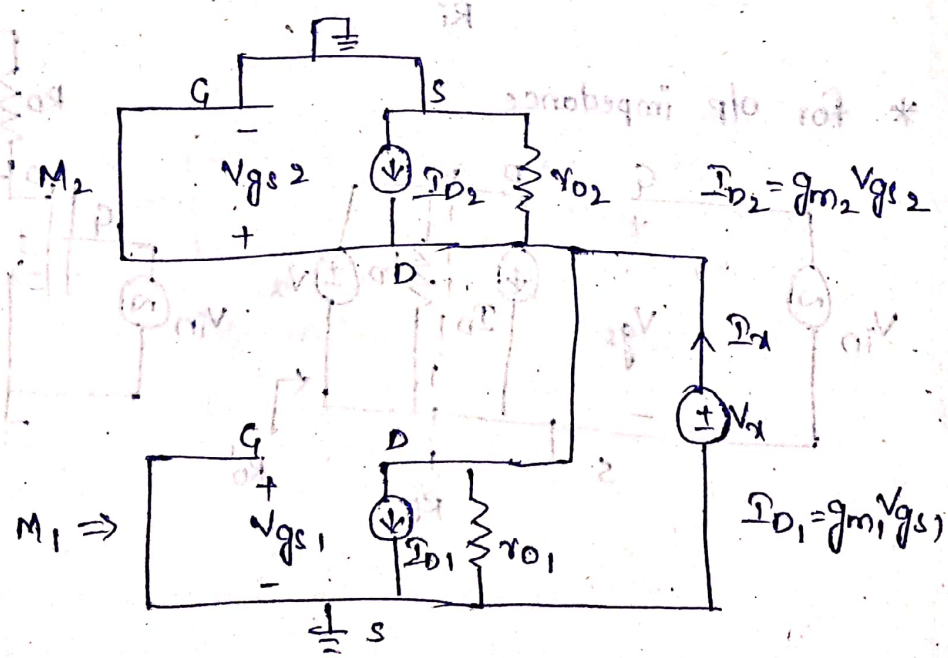
with various loads

①

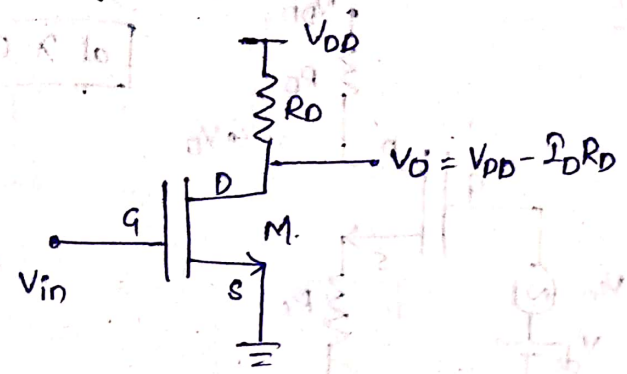


② Current Source

③ diode connected device



Problems of gain voltages:



$$A_V = -g_m R_D$$

$$g_m = \sqrt{2 I_D \mu_n C_{ox} \frac{W}{L}}$$

factors affecting the gate variations.

(1) If temperature varies, mobility varies, so that Voltage gain and transconductance also varies.

(2) Supply voltage

If Supply voltage (V_{DD}) changes, I_D, g_m and A_V also changes.

(3) Processing

During the process voltage gain will be changes.

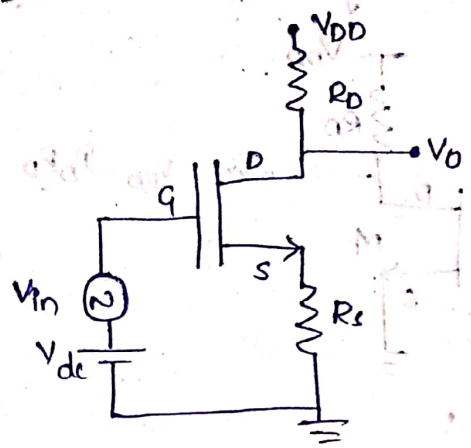
Processors: microprocessers, microcontrollers, DSP Processor.

(4) Signal level

Depending upon the signal variation (or) signal level [small signal (or) large signal], voltage gain changes.

Scanned with OKEN Scanner

Degeneration of common Source stage :



at $\lambda = 0$

Step 1: Biasing conditions (ac input = 0)

Apply KVL for input loop

$$-V_{dc} + V_{gs} + I_D R_s = 0$$

$$V_{dc} = V_{gs} + I_D R_s \longrightarrow (1)$$

Assume device is under saturation region.

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{th})^2$$

$$V_{gs} = \sqrt{\frac{I_D}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}}} + V_{th}$$

$$V_{gs} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}} + V_{th}$$

$$V_{dc} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}} + V_{th} + I_D R_s \quad (\text{from } (1))$$

Voltage across drain terminal

$$V_D = V_{DD} - I_D R_D$$

$$V_D \geq V_{dc} - V_{th}$$

$$\boxed{V_{DD} - I_D R_D \geq V_{dc} - V_{th}}$$

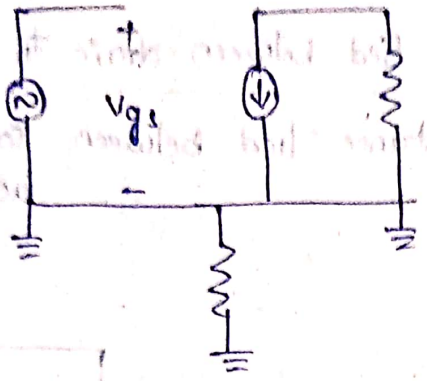
$$V_S = I_D R_s$$

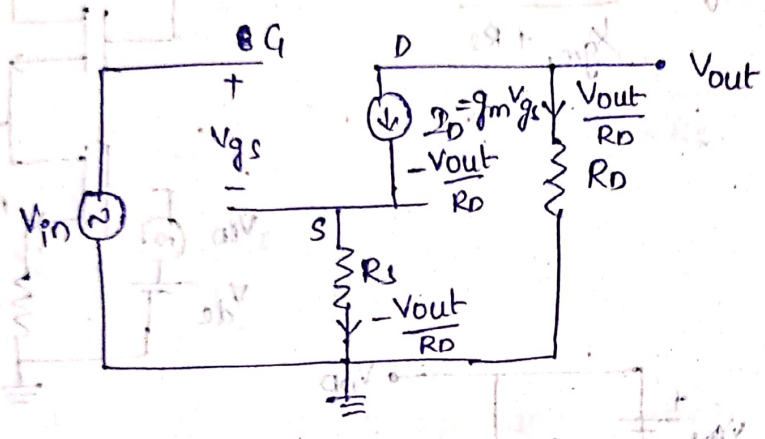
$$V_{DS} = V_D - V_S = V_{DD} - I_D(R_s + R_D)$$

Scanned with OKEN Scanner

step 2: Small signal parameter calculations

(Av, Ro, Ri)





$$g_m V_{gs} = -\frac{V_{out}}{R_D}$$

$$V_{gs} = -\frac{V_{out}}{R_D g_m} \longrightarrow (1)$$

Apply KVL for input loop:

$$-V_{in} + V_{gs} - \frac{V_{out}}{R_D} R_S = 0$$

$$-V_{in} - \frac{V_{out}}{R_D g_m} - \frac{V_{out}}{R_D} R_S = 0$$

$$-V_{in} = V_{out}\left[\frac{1}{R_D g_m} + \frac{R_S}{R_D}\right]$$

$$-V_{in} = V_{out}\left[\frac{1 + g_m R_S}{g_m R_D}\right]$$

$$\frac{V_{out}}{V_{in}} = \frac{-g_m R_D}{1 + g_m R_S}$$

$$\boxed{A_V = \frac{-g_m R_D}{1 + g_m R_S}}$$

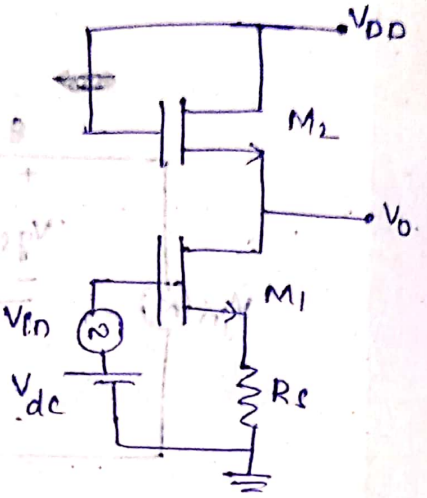
Scanned with OKEN Scanner

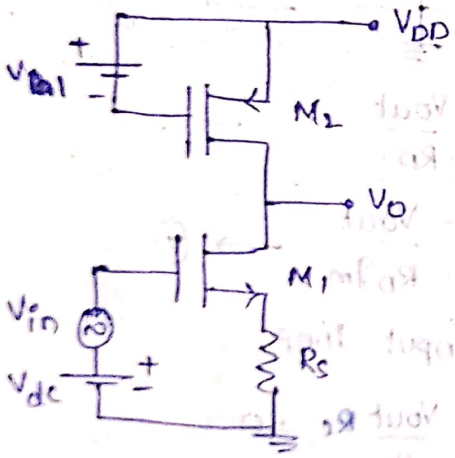
$$A_V = \frac{-R_D}{\frac{1}{g_m} + R_S}$$

$\frac{1}{g_m} << R_S$

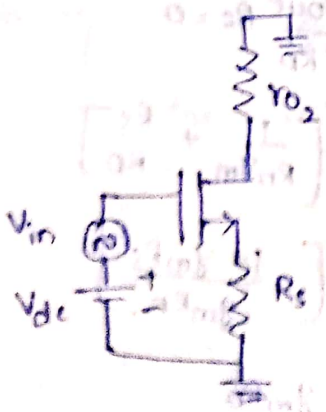
A_V = Resistance tied between drain to ac ground / $\frac{1}{g_m}$ + Resistance tied between source to ac ground

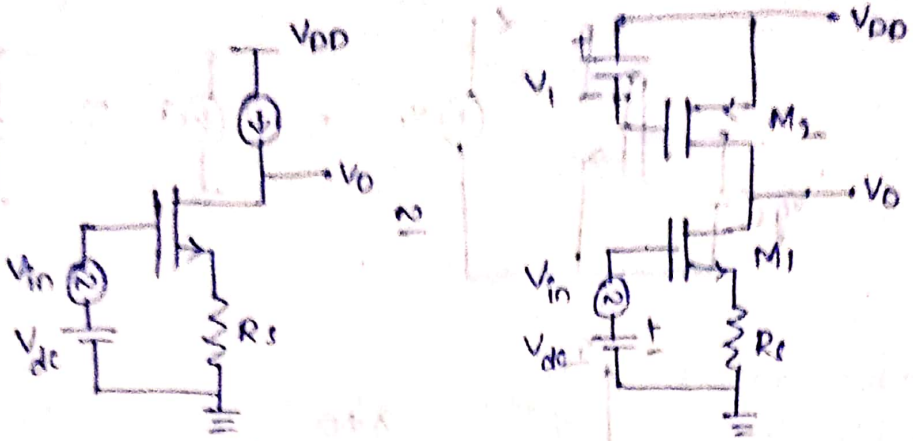
$$A_V = \frac{-g_{m_2}}{g_{m_1} + R_S}$$

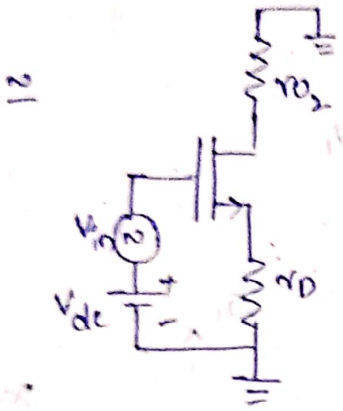




$$A_V = \frac{-r_{o_2}}{g_m + R_S}$$

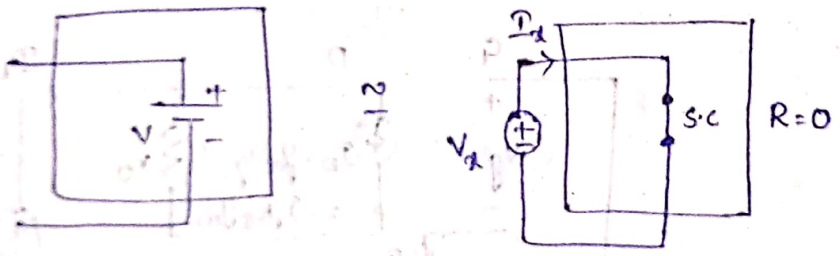


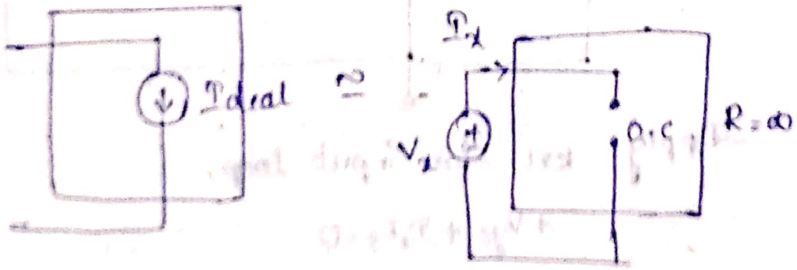


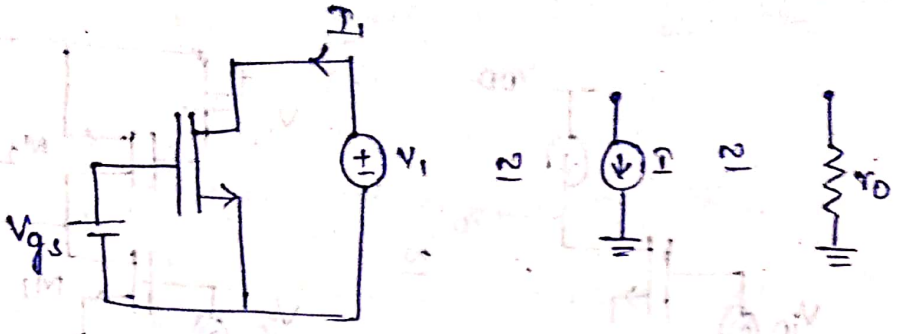


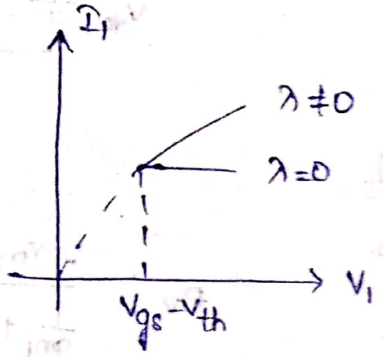
$$A_V = \frac{-r_{O2}}{\frac{1}{g_{m1}} + R_S}$$

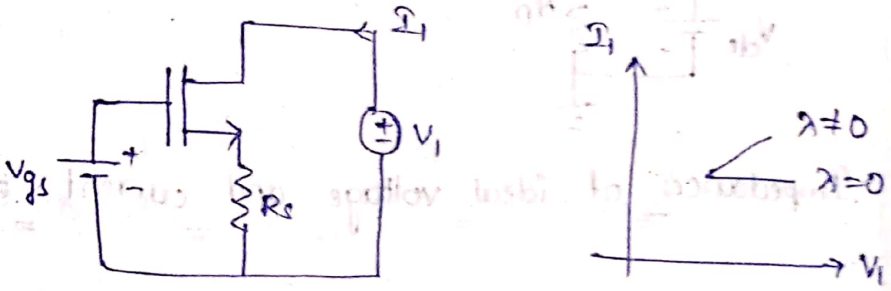
Impedance of ideal voltage and current sources :

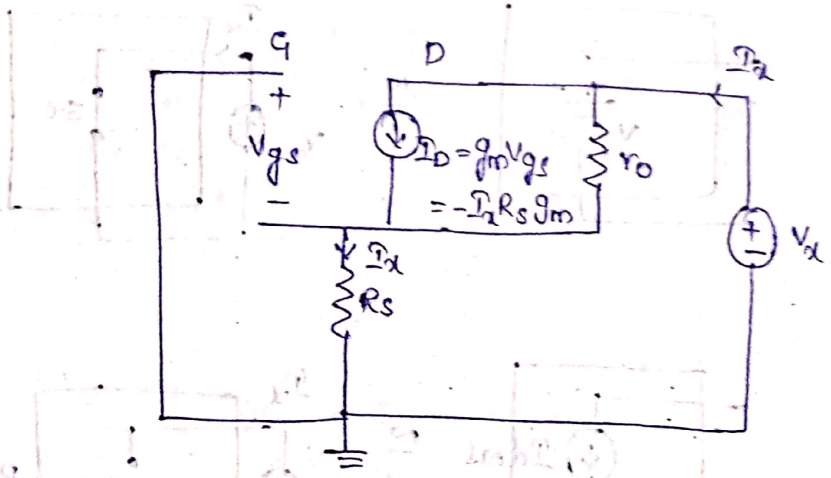












Apply kvl for input loop,

$$+V_{gs} + I_x R_s = 0$$

$$V_{gs} = -I_x R_s \rightarrow (1)$$

Current flowing through r_o is $I_x - (-I_x g_m R_s)$

$$= I_x + I_x g_m R_s$$

Scanned with OKEN Scanner

Apply KVL for o/p loop,

$$-V_x + r_o I_x (1 + g_m R_s) + I_x R_s = 0$$

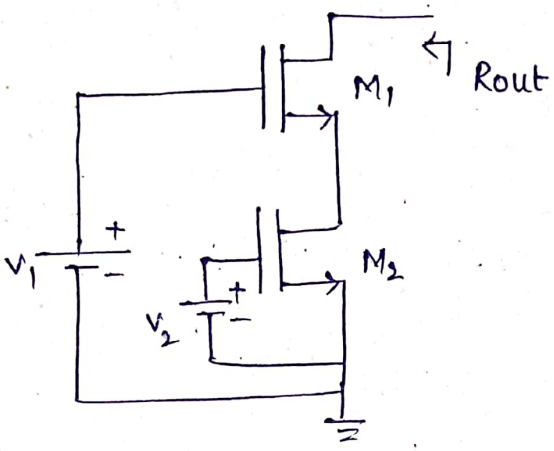
$$-V_x = -I_x \left[r_o (1 + g_m R_s) + R_s \right]$$

$$\frac{V_x}{I_x} = r_o (1 + g_m R_s) + R_s$$

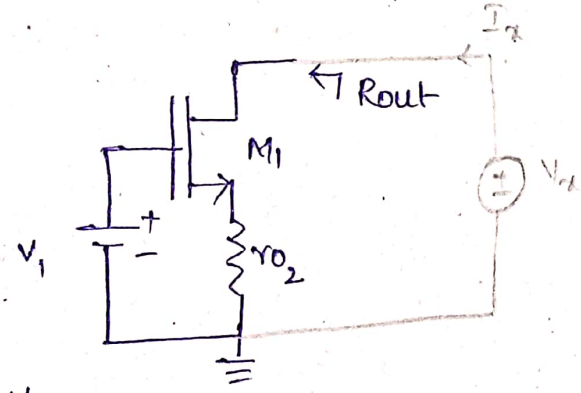
$$R_{out} = \frac{V_x}{I_x} = R_s (1 + g_m r_o) + r_o$$

R_s : degeneration resistance

$g_m r_o$: intrinsic gain



≈



$$R_{out} = \frac{V_x}{I_x} = r_{o_2} (1 + g_{m_1} r_{o_1}) + r_{o_1}$$

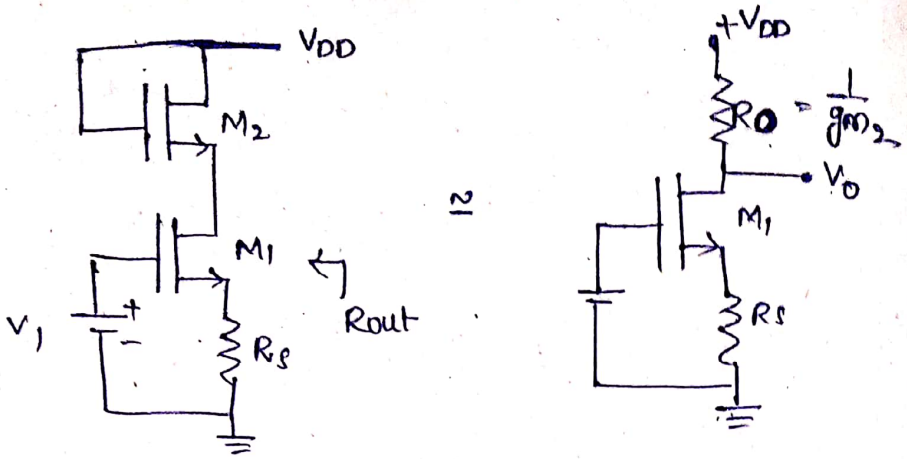
$1 \ll\ll g_{m_1} r_{o_1}$

$r_{o_2} \gg\gg r_{o_1}$

$$R_{out} = g_{m_1} r_{o_1} r_{o_2}$$

$g_{m_1} r_{o_1}$: intrinsic gain

Scanned with OKEN Scanner



$$R_{out} = R_s(1+g_{m_1}R_O) + R_O$$

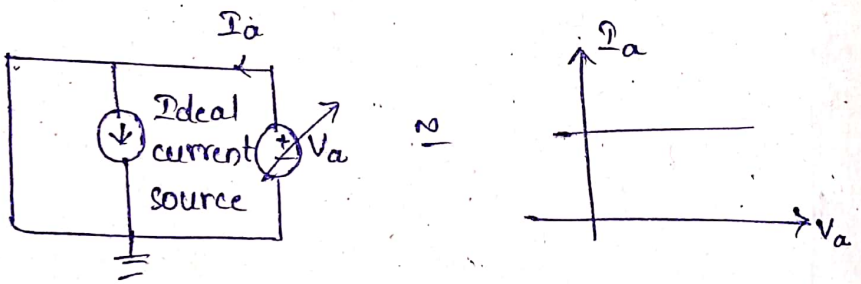
$$= R_s\left(1+g_{m_1}\frac{1}{g_{m_2}}\right) + \frac{1}{g_{m_2}} \quad (\lambda = 0)$$

$$R_{out} = R_O \,||\, \left[R_s\left(1+g_{m_1}\frac{1}{g_{m_2}}\right) + \frac{1}{g_{m_2}}\right] \quad (\lambda \neq 0)$$

$$= R_O \,||\, \left[R_s(1+g_{m_1}r_O) + r_O\right] \quad (\lambda \neq 0)$$

$$= \frac{1}{g_{m_2}} \,||\, \left[R_s(1+g_{m_1}r_O) + r_O\right]$$

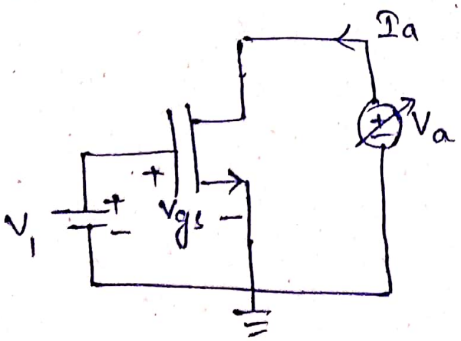
Cascode current Sources:



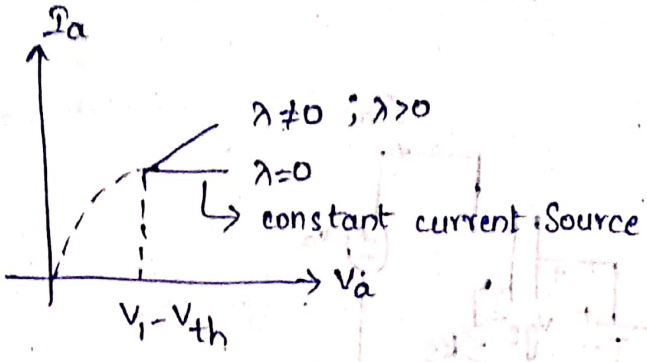
As the current is constant, slope is zero.

Observation – 1:

Let us build a current source



Scanned with OKEN Scanner

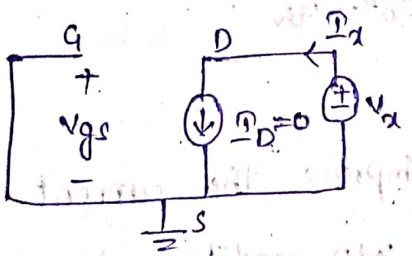


If $V_a > V_1 - V_{th}$, it can be used as a constant current source at $\lambda = 0$.

We can't able to use mosfet as a constant current source for entire life.

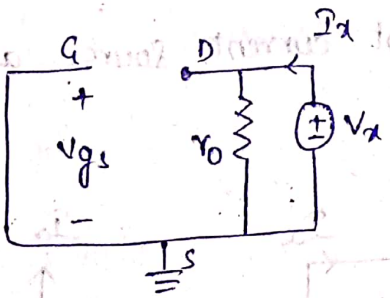
Mosfet can act as a constant current source in saturation region at $\lambda = 0$.

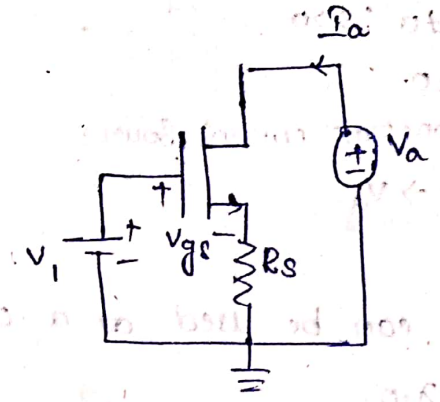
If $\lambda \neq 0$, It can't be used as a constant current source. So, We will place R_s to use it as constant current source.



$R_{out} = \infty \quad (\lambda = 0)$

$R_{out} = r_o \quad (\lambda \neq 0)$

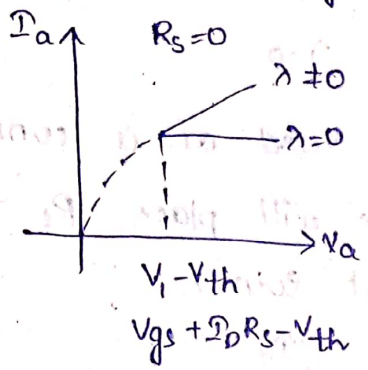




-Apply KVL for the input loop

$$-V_1 + V_{gs} + I_D R_s = 0$$

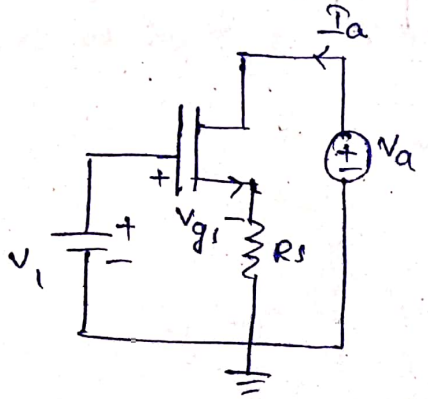
$$V_1 = V_{gs} + I_D R_s$$

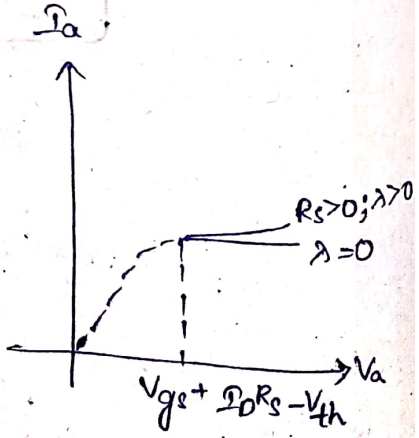


Observation-2:

-How do we improve the current source

-As $R_s \neq 0$, at $\lambda \neq 0$ condition also MOSFET acts as a constant current source as the slope decreases.

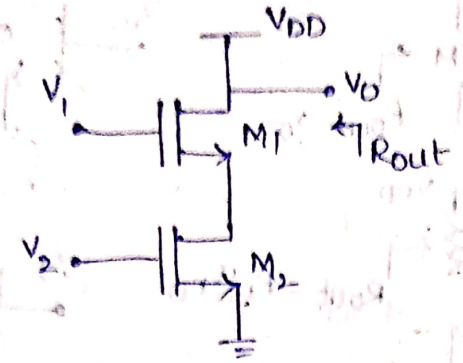




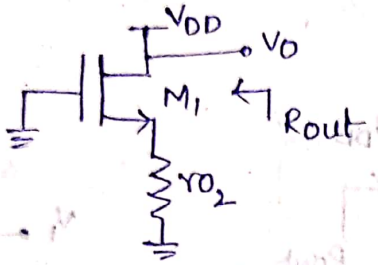
Scanned with OKEN Scanner

Observation - 3:

Cascode current Source



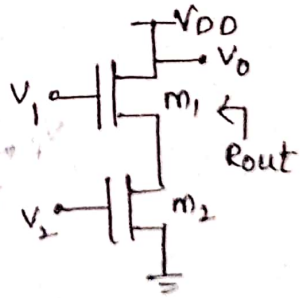
≈



$$R_{out} = (1 + g_{m1} r_{o1}) r_{o2} + r_{o1}$$

$$R_{out} = g_{m1} r_{o1} r_{o2}$$

Q. If w is doubled and I_D constant. What happened to R_{out} and A_V



$$g_{m1} = \sqrt{2 I_{D max} \frac{w}{L} \mu_n C_{ox}}$$

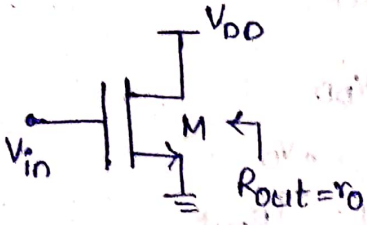
$$g_{m2} = \sqrt{2 I_{D max} \left(\frac{2w}{L}\right) \mu_n C_{ox}}$$

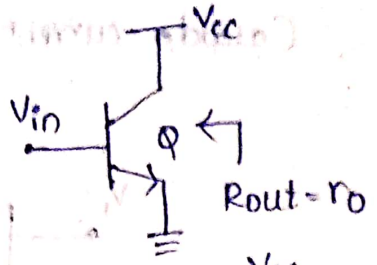
$$R_{out} = g_{m1} r_{o1} r_{o2}$$

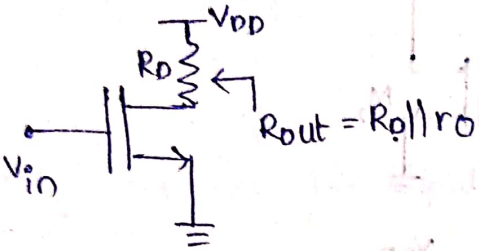
$$R_{out}' = G \, R_{out}$$

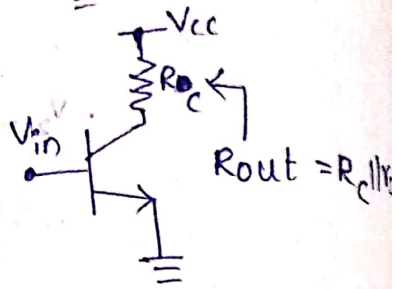
$$A_{V_2} = G \, A_{V_1}$$

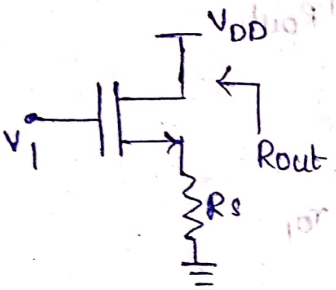
Bipolar cascode current source:

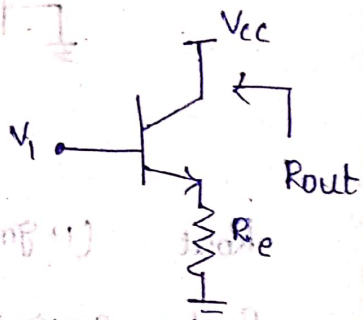








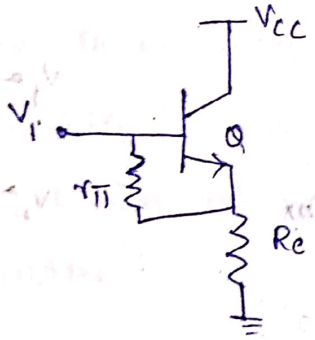




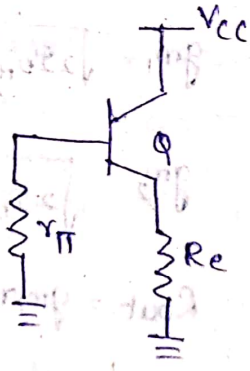
$R_{out} = (1+g_{m_1} r_{o_1}) R_S + r_{o_1}$

$R_{out} = (1+g_{m_1} r_{o_1}) R_e + r_{o_1}$

*

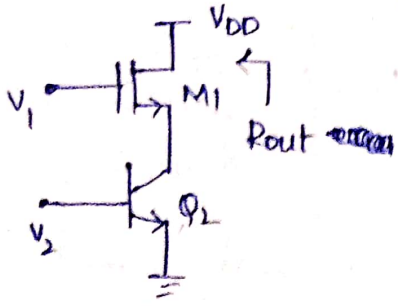


≃

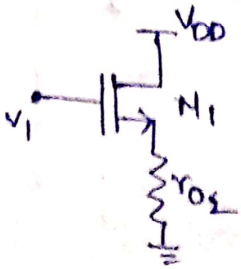


$R_{out} = (1+g_{m_1} r_{o_1})(R_e \| r_\pi) + r_{o_1}$

*

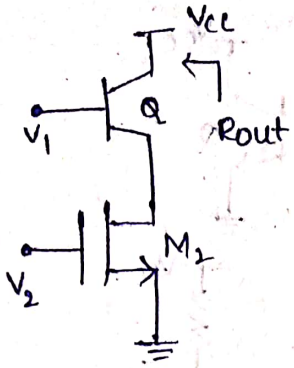


≃

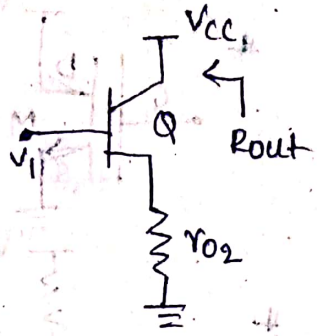


$R_{out} = (1+g_{m_1} r_{o_1}) r_{o_2} + r_{o_1}$

*



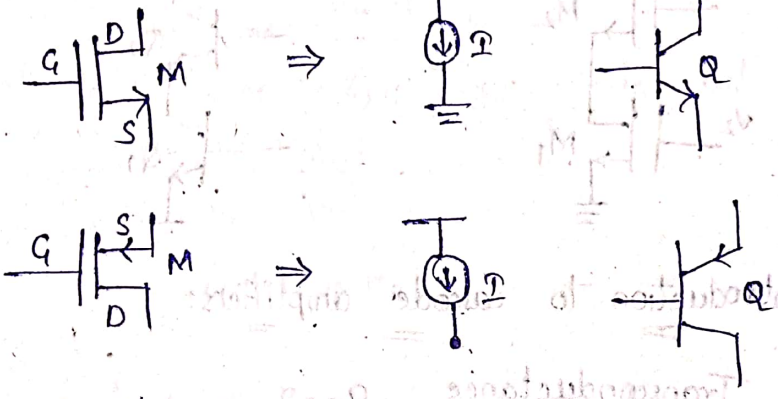
≈



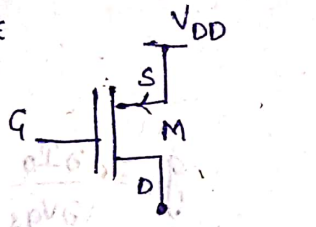
$R_{out} = (1+g_{m_1} r_{o_1}) r_{o_2} + r_{o_1}$

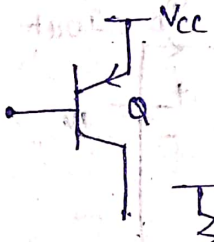
$R_{out} = (1+g_{m_1} r_{o_1})(r_\pi \| r_{o_2}) + r_{o_1}$

P-Type Current Sources :

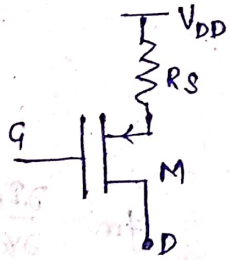


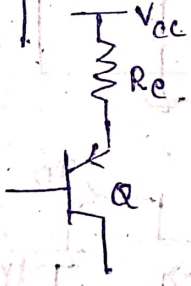
*



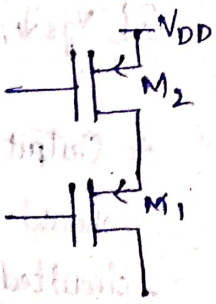


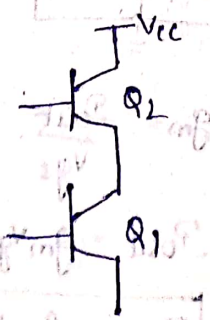
*



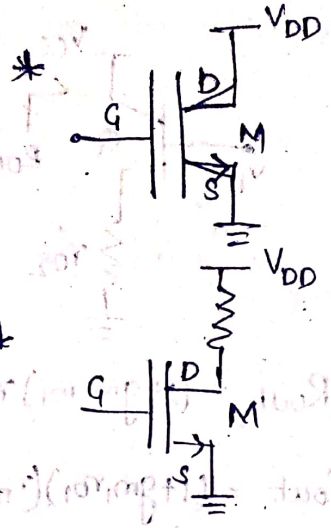


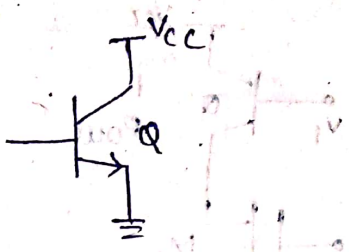
*

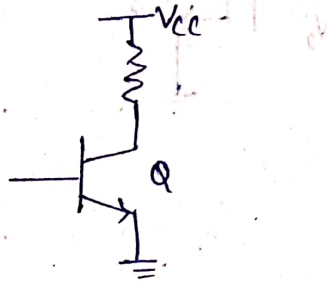


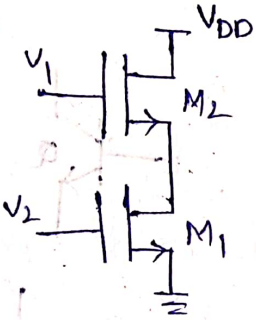


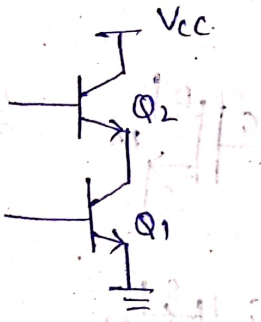
Scanned with OKEN Scanner





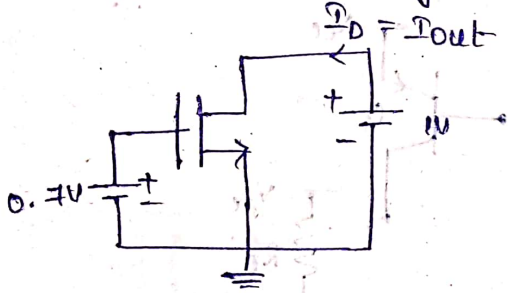




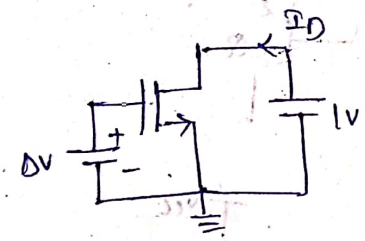


Introduction to cascode amplifiers:

(1) Transconductance $g_m = ?$



$$g_m = \frac{\partial I_D}{\partial V_{gs}}$$



$$g_m = \frac{\partial I_D}{\partial V_{gs}}$$

If $V_{gs} \downarrow$, $g_m \uparrow$, $I_D \uparrow$

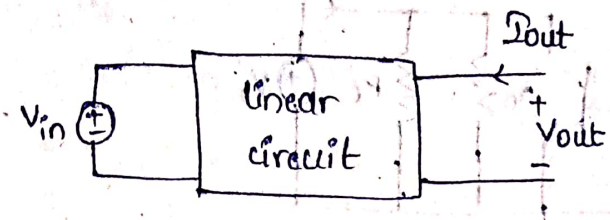
$$g_m = \frac{I_{out}}{V_{gs}}$$

$$I_{out} = g_m V_{gs}$$

$$\boxed{I_{out} = g_m V_{in}}$$

* Output voltage should be short circuited, to find g_m.

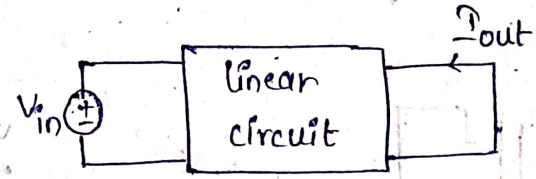
General linear circuit:



$$A_V = \frac{V_{out}}{V_{in}} = -G_m R_{out}$$

$G_m \rightarrow g_m$, $R_{out} \rightarrow R_D$

step 1: Transconductance

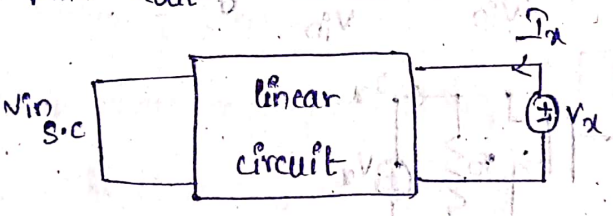


Short circuit the output voltage terminal

$$G_m = \frac{I_{out}}{V_{in}}$$

$$\boxed{I_{out} = G_m V_{in}}$$

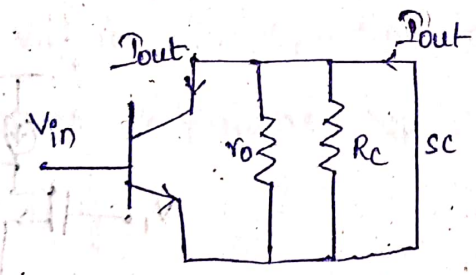
step 2: find R_{out}

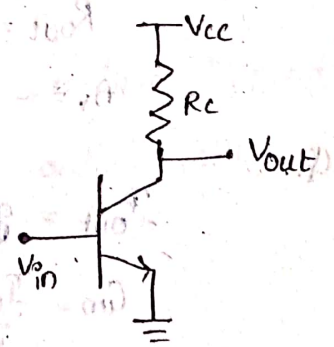


$$R_{out} = \frac{V_x}{I_x}$$

$$\boxed{G_m = -g_m}$$

Q.



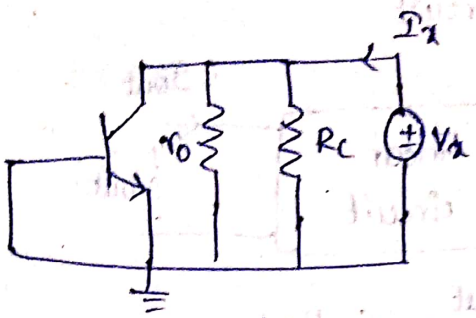


$$I_{out} = g_m V_{in}$$

$$G_m = \frac{I_{out}}{V_{in}} = \frac{g_m V_{in}}{V_{in}} = g_m$$

$$G_m = g_m$$

$$R_{out} = r_o \| R_c$$

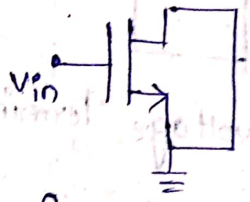


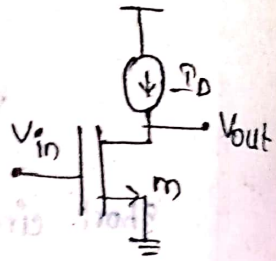
$R_{out} = r_o \| R_C$

$A_v = -G_m R_{out}$

$= -g_m (R_C \| r_o)$

Q.

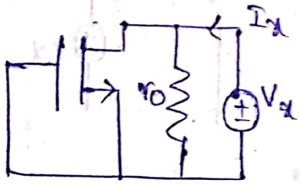




$G_m = \frac{I_{out}}{V_{in}}$

$I_{out} = G_m V_{in}$

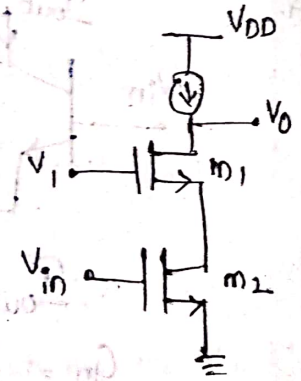
$G_m = \frac{I_{out}}{V_{in}} = \frac{g_m V_{in}}{V_{in}} = g_m$



$R_{out} = r_o$

$A_v = -g_m r_o$

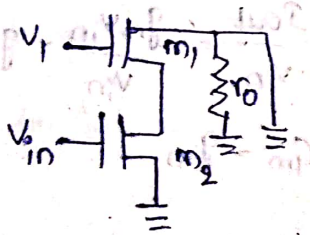
Q.



$I_{out} = g_{m_2} V_{in}$

$G_m = \frac{I_{out}}{V_{in}}$

$G_m = g_{m_2}$

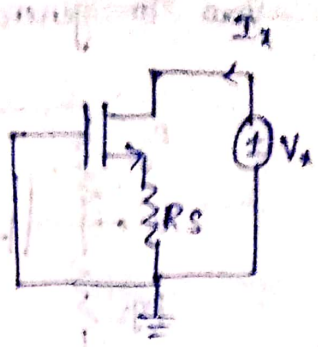


Scanned with OKEN Scanner

$R_{out} = ?$

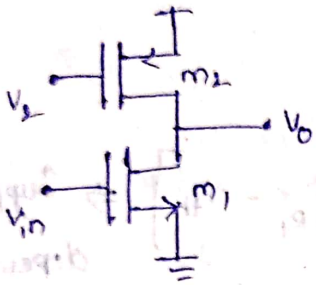
$R_s(1+g_m r_{o1}) + r_{o1}$

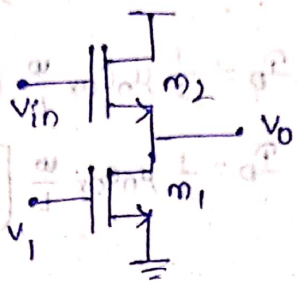
$= r_{o2}(1+g_m r_{o1}) + r_{o1}$



Current mirrors:

Constant current sources are everywhere.

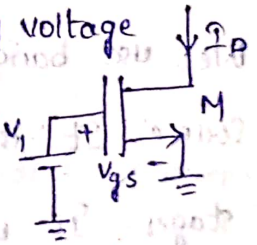




Problems of biasing current source:

M is turned on

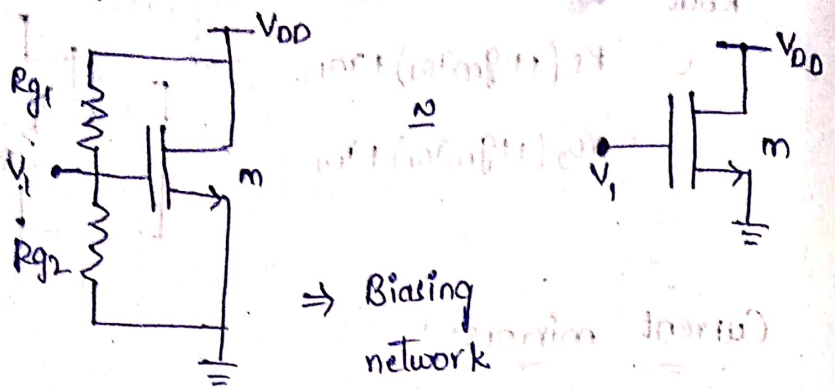
$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_1 - V_{th})^2$ ⇒ Independent of Supply voltage



If temperature changes, mobility changes. Therefore I_D is changing (not constant) (unstable).

* V_{th} is also dependent on temperature. Depending upon temperature, V_{th} changes and I_D also changes.

How to generate V_1 voltage across gate terminal



$\Rightarrow$ Biasing network

$$V_1 = V_{DD} \times \frac{R_2}{R_2 + R_1}$$

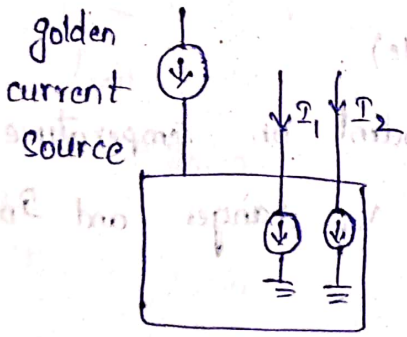
$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_1 - V_{th})$$

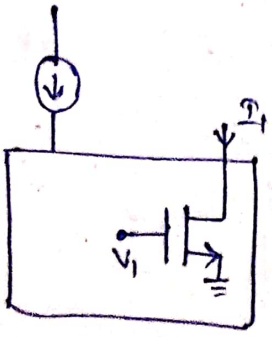
$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left[V_{DD} \times \frac{R_2}{R_2 + R_1} - V_{th} \right]$$ $\Rightarrow$ Supply dependent (V_{DD})

If Supply voltage changes, I_D changes.

Basic concepts in current mirror:

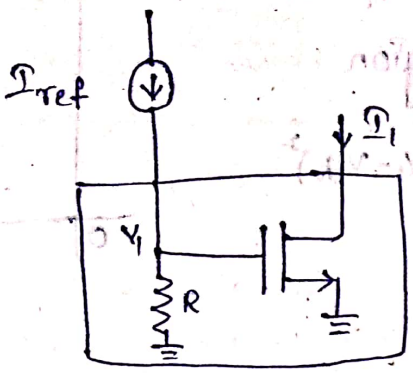
We use bandgap circuit to build golden current source. It is cloning & copy of further stages. It will drive other stages.





Scanned with OKEN Scanner

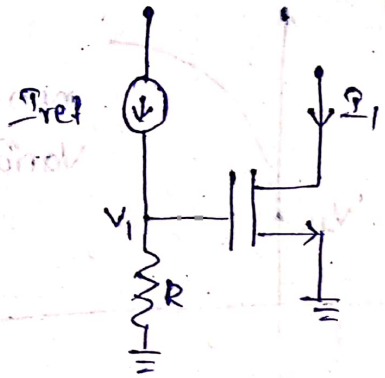
To apply V_1 voltage (for conduction)



$V_1 = I_{ref} \cdot R$

this voltage drives the MOSFET.

* MOSFET is under saturation.



$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_1 - V_{th})^2$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (I_{ref} \cdot R - V_{th})^2$$

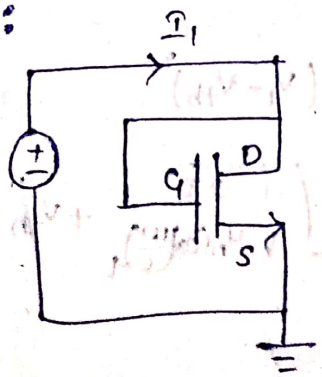
R is also a temperature dependent parameter.

μ_n, R, V_{th} – temperature dependent.

First build one golden current source using bandgap circuit.

Next we copy (or) clone this current source to build many other sources.

Case (i) :

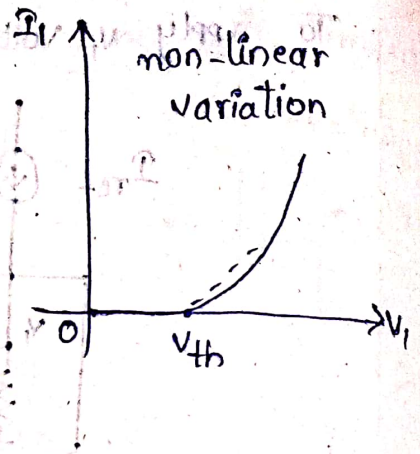


diode connected device

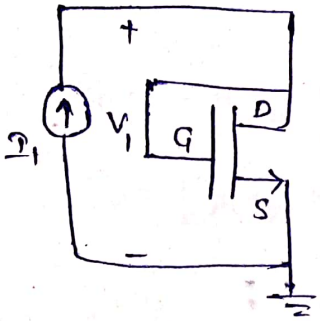
$V_1 \geq V_{th}$

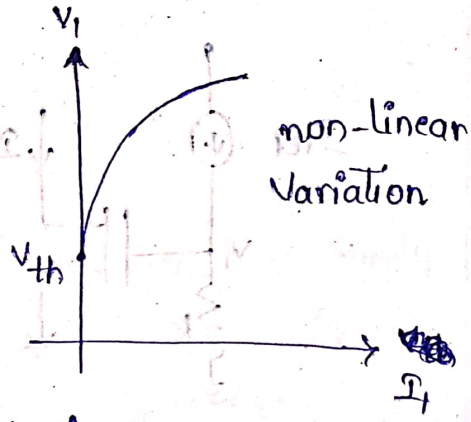
M is turn on & in saturation region

$$I_1 = \frac{1}{2}\mu_n C_{ox}\frac{w}{L}(V_1 - V_{th})^2$$



case (ii):

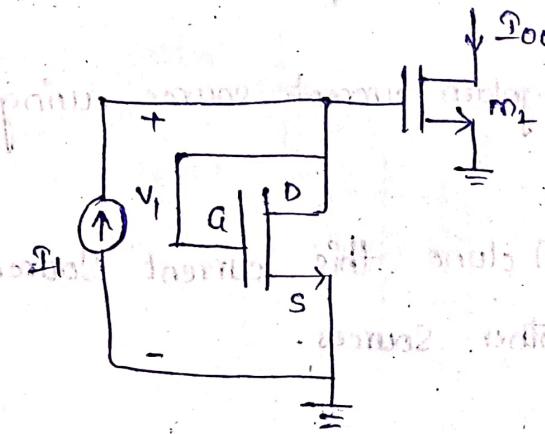




$$I_1 = \frac{1}{2}\mu_n C_{ox}\frac{w}{L}(V_1 - V_{th})^2$$

$$V_1 = \sqrt{\frac{2I_1}{\mu_n C_{ox}\frac{w}{L}}} + V_{th}$$

Case (iii):



I_{out} V_1 drives m_2.

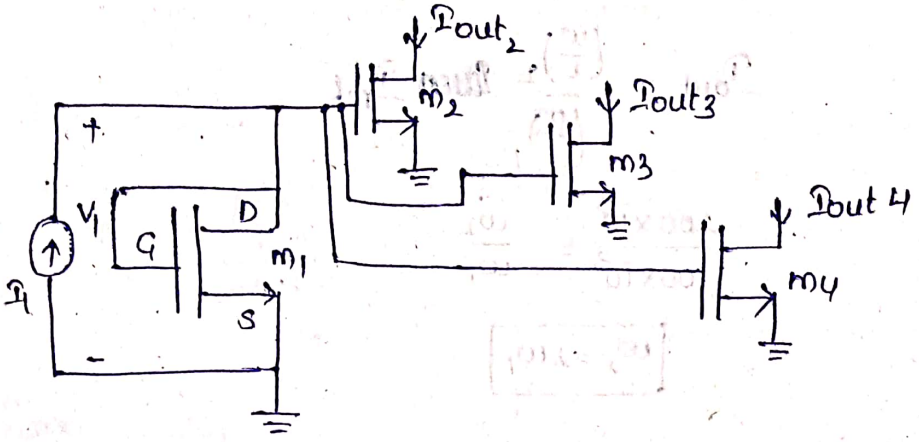
$$I_{out} = \frac{1}{2}\mu_n C_{ox}\frac{w}{L}(V_1 - V_{th})^2$$

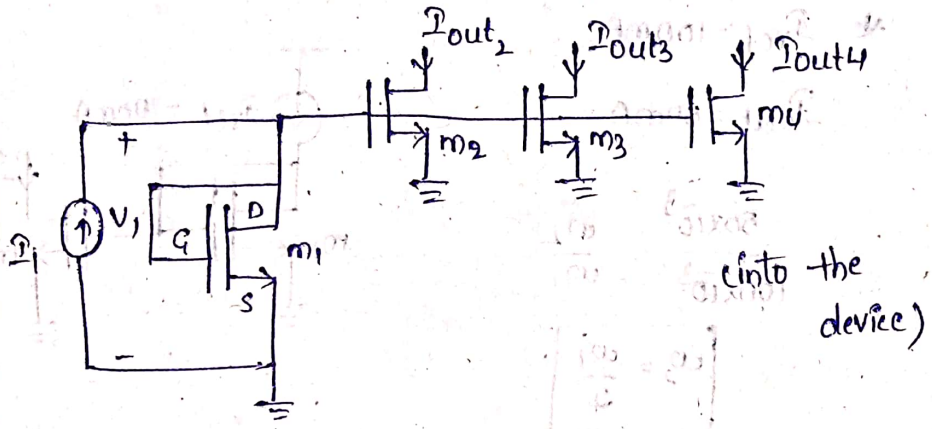
$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{w}{L}\right)_2\left(\sqrt{\frac{2I_1}{\mu_n C_{ox}\left(\frac{w}{L}\right)_1}} + V_{th} - V_{th}\right)^2$$

Scanned with OKEN Scanner

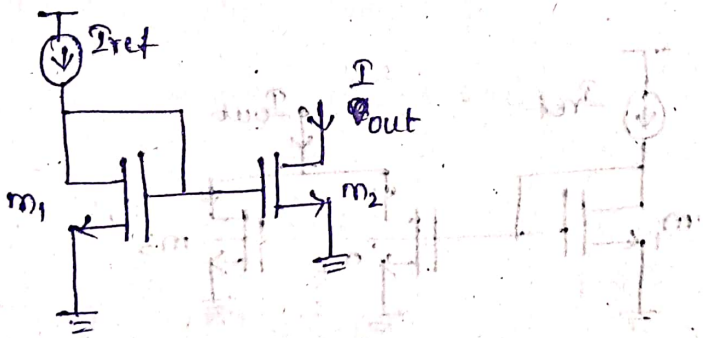
$$I_{out} = \frac{\left(\frac{w}{L}\right)_2}{\left(\frac{w}{L}\right)_1} I_1$$

All the problems are rectified by using current mirrors.





(into the device)



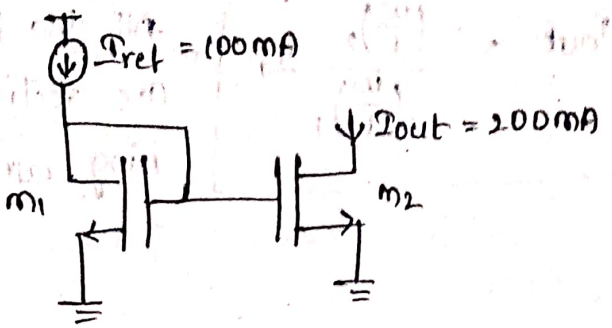
$$I_{out} = \frac{\left(\frac{w}{L}\right)_2}{\left(\frac{w}{L}\right)_1} I_{ref}$$

(i) $L_1 = L_2$

(ii) w_1 & w_2 selecting accordingly.

Scanned with OKEN Scanner

Q.



$$I_{out} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} I_{ref}$$

$$\frac{200 \times 10^{-3}}{100 \times 10^{-3}} = \frac{W_2}{W_1}$$

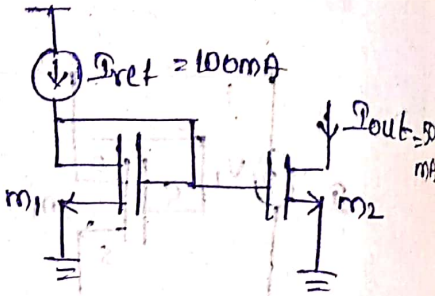
$$\boxed{W_2 = 2W_1}$$

* I_{ref} = 100mA

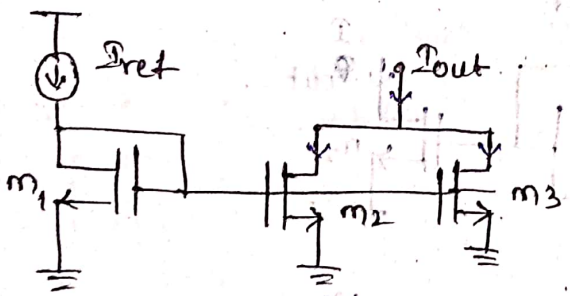
I_{out} = 50mA

$$\frac{50 \times 10^{-3}}{100 \times 10^{-3}} = \frac{W_2}{W_1}$$

$$\boxed{W_2 = \frac{W_1}{2}}$$



Q.



$$I_{out} = \frac{W_2}{W_1} I_{ref}$$

$$I_{out} = \frac{W_3}{W_1} I_{ref}$$

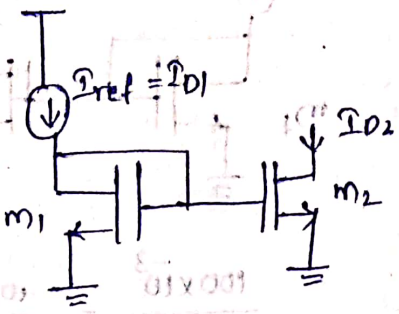
will be
wildar

$$I_{out} = \frac{W_2}{W_1} I_{ref} + \frac{W_3}{W_1} I_{ref}$$

Alternate approach:

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_1 - V_{th})^2$$

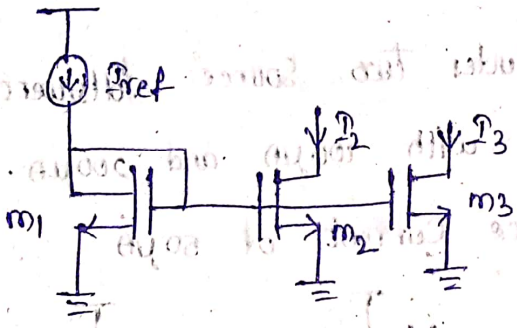
$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_1 - V_{th})^2$$



$$\frac{I_{D2}}{I_{D1}} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}$$

$$I_{D2} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} I_{D1}$$

Proper Scaling:



(1) Always select same 'L'.

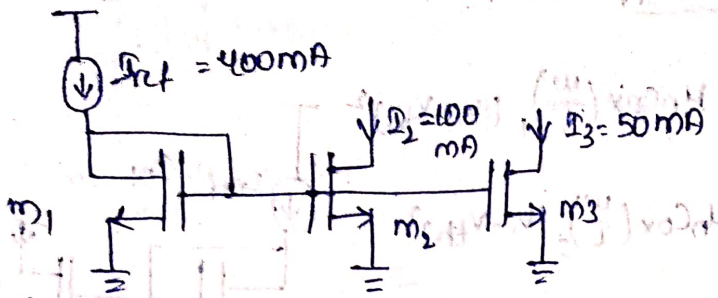
(2) Scale properly widths (W).

$$I_2 = \left(\frac{W_2}{W_1}\right) I_{ref}$$

$$I_3 = \left(\frac{W_3}{W_1}\right) I_{ref}$$

Scanned with OKEN Scanner

Q.



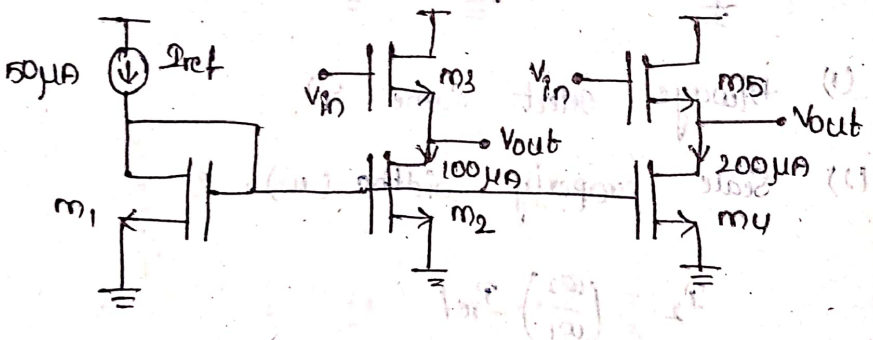
$$\frac{100\times10^{-3}}{400\times10^{-3}} = \frac{w_2}{w_1}$$

$$\boxed{w_2 = \frac{1}{4} w_1}$$

$$\frac{50\times10^{-3}}{400\times10^{-3}} = \frac{w_3}{w_1}$$

$$\boxed{w_3 = \frac{1}{8} w_1}$$

Q. A circuit includes two source followers biased at saturation with 100μA and 200μA. We have a reference current of 50μA



$$\frac{100\mu A}{50\mu A} = \frac{w_2}{w_1}$$

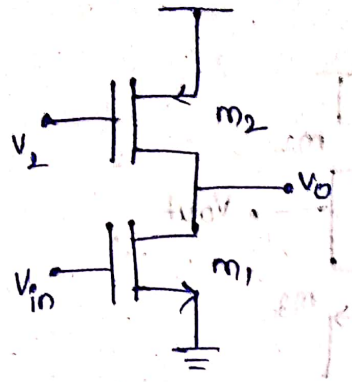
$$\boxed{w_2 = 2w_1}$$

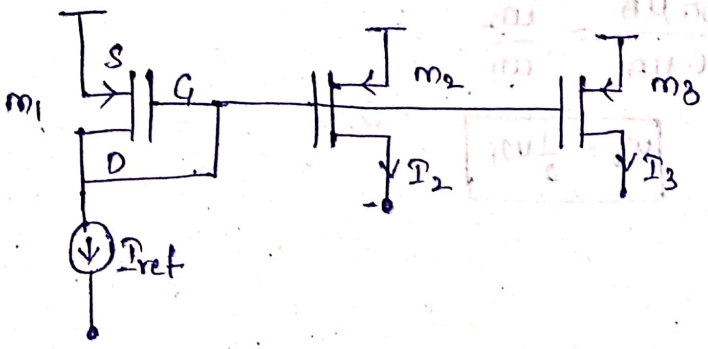
$$\frac{200\mu A}{50\mu A} = \frac{w_3}{w_1}$$

$$\boxed{w_3 = 4w_1}$$

Scanned with OKEN Scanner

P MOSFET current mirror:

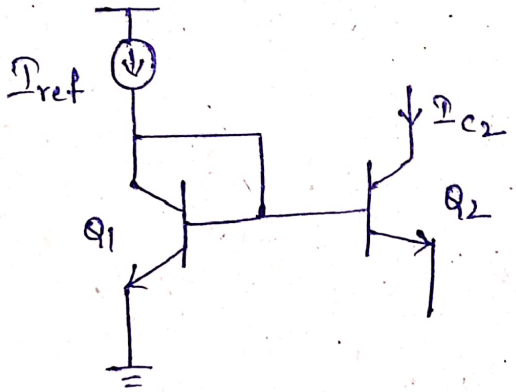




$$I_2 = \left(\frac{w_2}{w_1}\right) I_{ref}$$

$$I_3 = \left(\frac{w_3}{w_1}\right) I_{ref}$$

BJT current mirror:

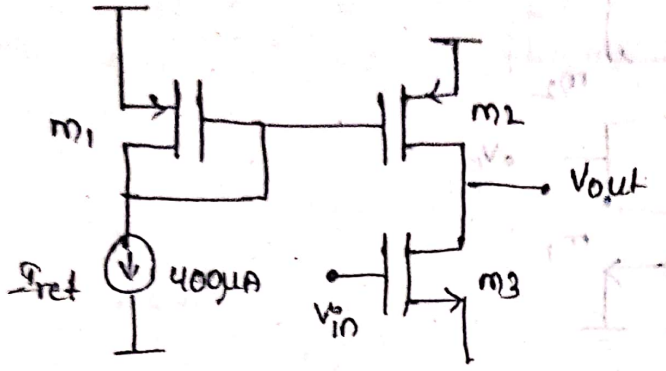


$$I_{c_1} = I_{s_1} \frac{e^{V_{BE}}}{V_T}$$

$$I_{c_2} = I_{s_2} \frac{e^{V_{BE}}}{V_T}$$

$$\frac{I_{c_2}}{I_{c_1}} = \frac{I_{s_2}}{I_{s_1}}$$

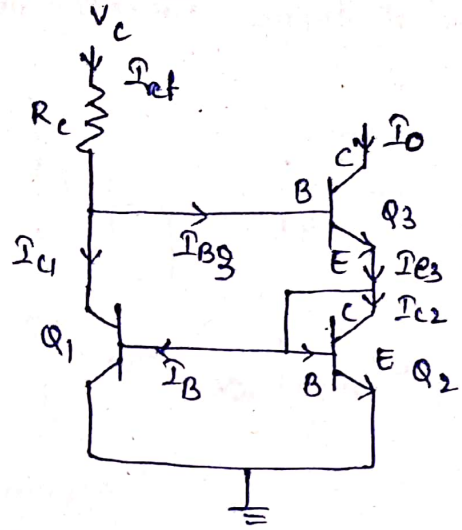
Q. An N-MOSFET common source stage requires a load current equal to 200μA. $I_{ref} = 400\mu A$

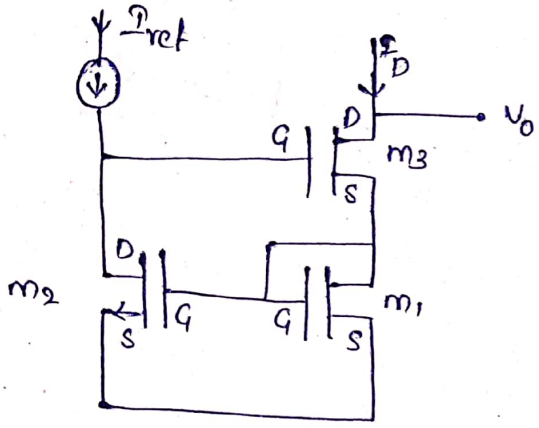


$$\frac{200\,\mu A}{400\,\mu A} = \frac{\omega_2}{\omega_1}$$

$$\boxed{\omega_2 = \frac{1}{2}\omega_1}$$

Wilson current mirror (or) current source:





$$I_{ref} = I_{C1} + I_{B3} \quad \text{—(1)}$$

$$I_{E3} = I_{C2} + 2I_B$$

$$I_{E3} = I_{C2} + \frac{2I_{C2}}{\beta} = I_{C2}\left(1 + \frac{2}{\beta}\right)$$

$$I_{C2} = \frac{\beta}{\beta+2} I_{E3}$$

$I_{C2} = I_{C1}$, also $I_{E3} \approx I_o$

$$I_{C1} = \frac{\beta}{\beta+2} I_{E3}$$

Putting in eq (1),

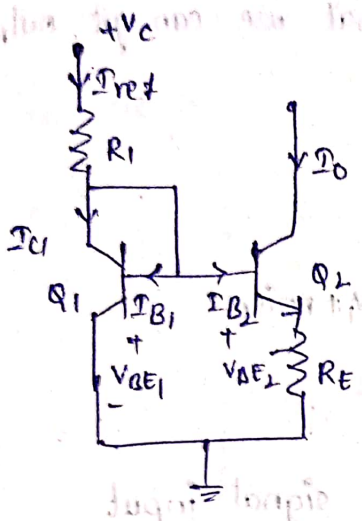
$$I_{ref} = \frac{\beta}{\beta+2} I_o + \frac{I_o}{\beta}$$

$$I_{ref} = \frac{\beta^2 + \beta + 2}{\beta(\beta+2)} I_o$$

Scanned with OKEN Scanner

$$I_O = \frac{\beta^2+2\beta}{\beta^2+\beta+2} I_{ref}$$

WILDAR current mirror:



$(I_O < I_{ref})$

Here $I_{C_2} = I_O$

KVL

$$-V_{BE_1} + V_{BE_2} + I_{E_2} R_E = 0$$

$$R_E = \frac{V_{BE_1} - V_{BE_2}}{I_{E_2}}$$

$$I_C = I_S e^{V_{BE}/V_T}$$

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$$

$$V_{BE_1} = V_T \ln\left(\frac{I_{C_1}}{I_S}\right)$$

$$V_{BE_2} = V_T \ln\left(\frac{I_{C_2}}{I_S}\right)$$

$$V_{BE_1} - V_{BE_2} = V_T \ln\left(\frac{I_{C_1}}{I_O}\right)$$

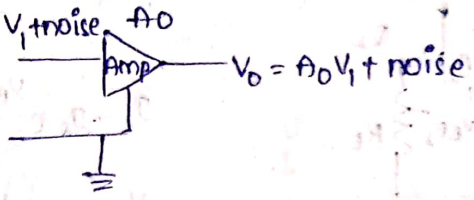
$$R_E = \frac{V_T \ln\left(I_{C_1}/I_O\right)}{(\beta+1) I_O}$$

Differential amplifiers:

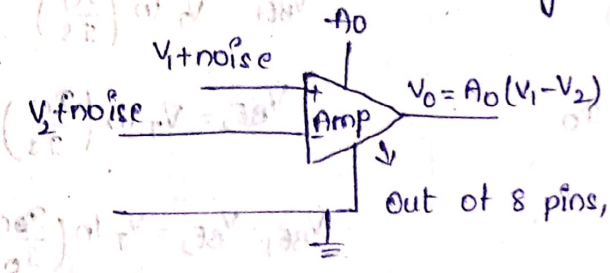
Noise coupling:

To eliminate the noise for further stages, we use differential amplifiers. Here we use two input signals simultaneously. So that we can get output as difference of two inputs.

Eg: ECG



Here noise is carried due to signal input.



Out of 8 pins, 5 pins are used

+ : non-inverting input

− : inverting input

$V_0 = A_0 (V_1 + noise - (V_2 + noise))$

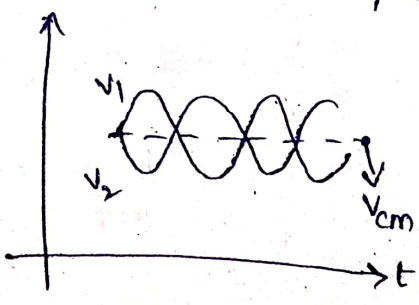
$V_0 = A_0 (V_1 - V_2)$

Here we have eliminated the noise in the o/p.

Differential signals:

The signals that which we are considering must be equal and opposite in amplitude

Eg:



Scanned with OKEN Scanner

These two signals are having same average (or) dc values.

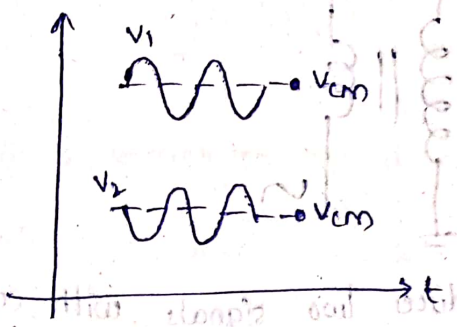
$V_1 = V_m \sin\omega t$

$V_2 = -V_m \sin\omega t$ } equal and opposite in amplitude

V_{cm} : common mode voltage levels.

V_{cm} should be same for both the signals (V_1 & V_2)

*

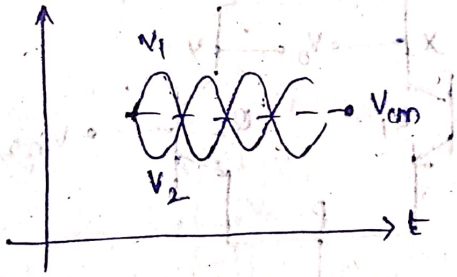


Both are having different V_{cm}'s. Therefore both are not differential signals.

Properties:

(1) The signals are having equal and opposite amplitude.

(2) They have same common mode voltage (or) average value (V_{cm}).



$V_1 = V_m \sin\omega t + V_{cmin}$

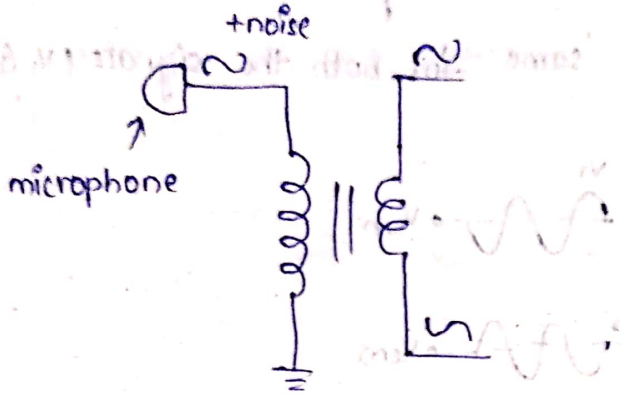
$V_2 = -V_m \sin\omega t + V_{cmin}$

$V_o = V_1 - V_2$

V_{cmin} : common mode input voltage

amplitude	V_1	V_2	$V_1 - V_2$
Peak amplitude	V_m	$-V_m$	$2V_m$
P-P amplitude	$2V_m$	$2V_m$	$4V_m$

How to generate the differential signals?

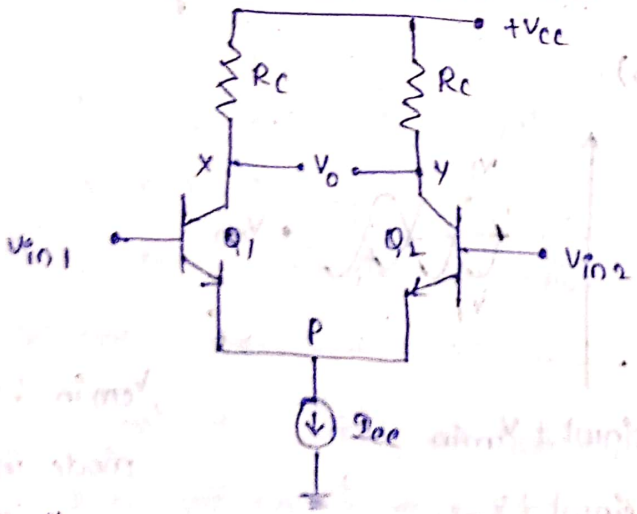


Transformer produces two signals with equal and opposite amplitudes (differential signals).

Differential amplifier Pairs:

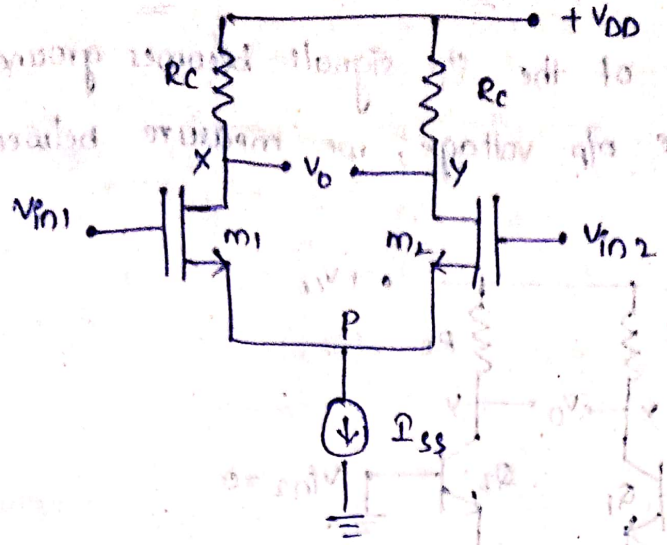
There are 4 types of differential amplifiers

(1) Dual i/p & balanced o/p differential amplifiers.



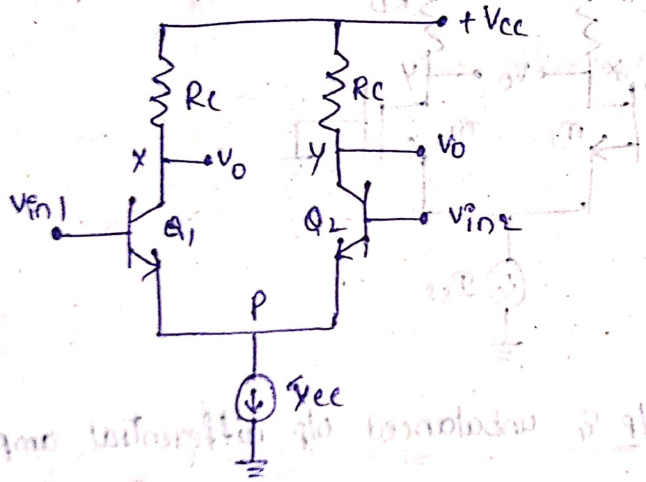
Both are identical and symmetric transistors.

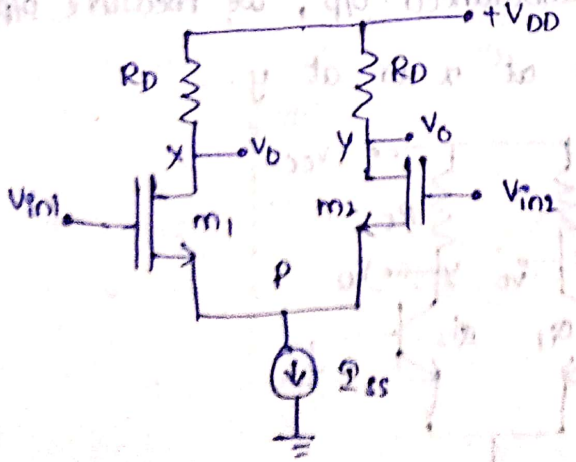
To obtain balanced output, we measure o/p voltage in between x and y.



(2) Dual i/p & unbalanced o/p differential amplifiers:

To obtain unbalanced o/p, we measure o/p either at x or at y.

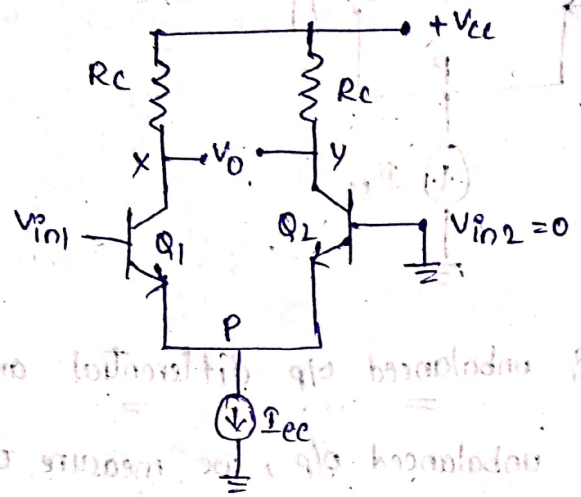


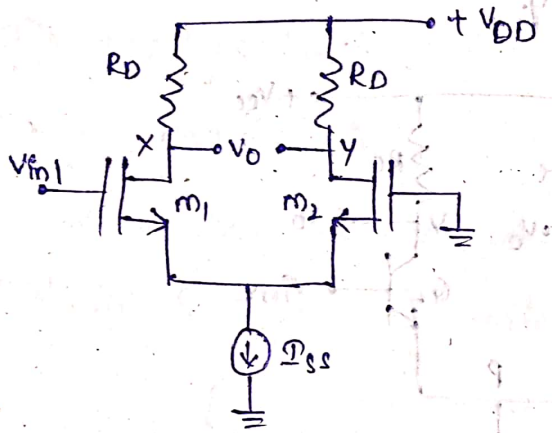


Scanned with OKEN Scanner

(3) Single i/p & balanced o/p differential amplifiers:

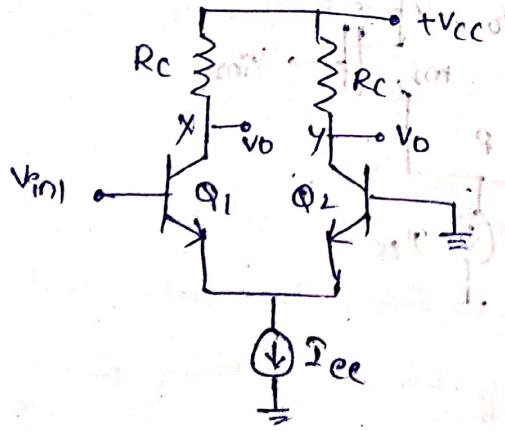
Either one of the i/p signals becomes ground. To measure o/p voltage, we measure between x and y.

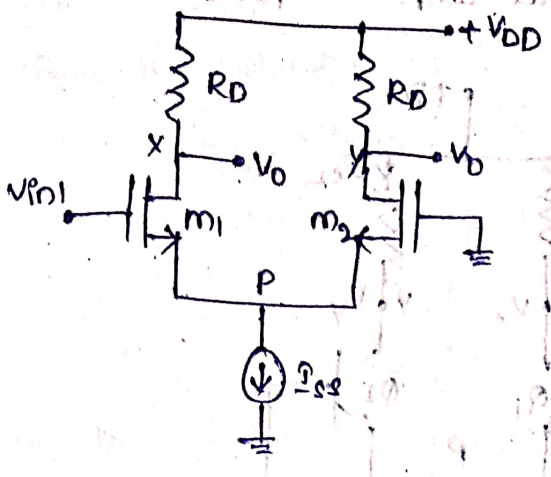




(4) Single i/p & unbalanced o/p differential amplifiers:

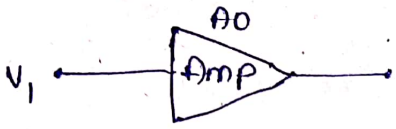
To measure unbalanced o/p, we measure o/p Voltage either at x or at y.



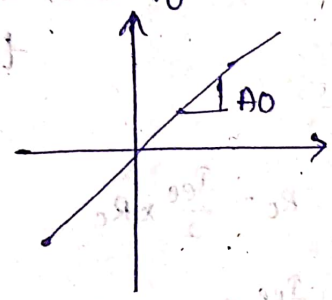


Example:

Case ①:

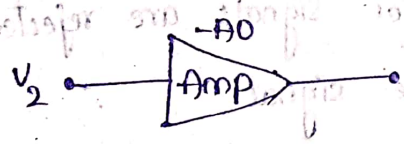


$\frac{V_0}{V_1} = A_0 = \text{gain}$

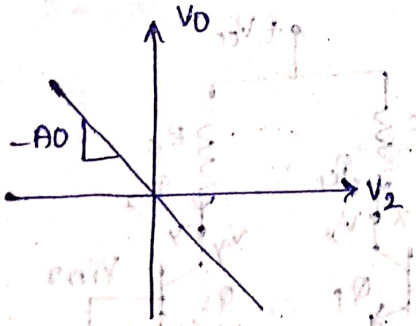


Here slope = A0 (Gain)

Case ②:



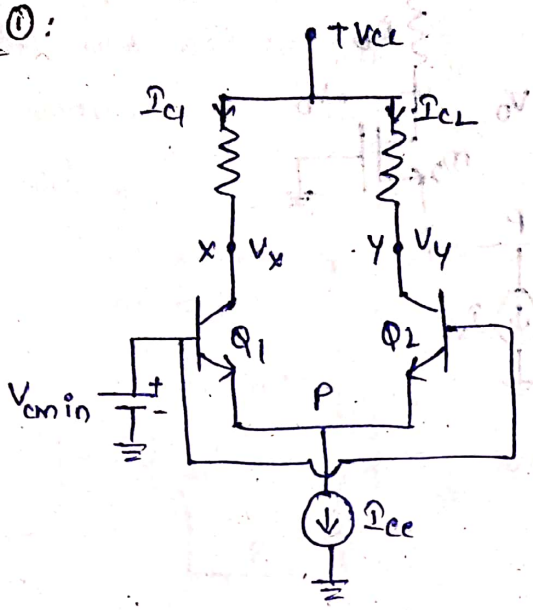
$\frac{V_0}{V_2} = -A_0 = \text{Gain}$



Here slope = -A0

Bipolar differential amplifier pairs:

Case ①:



Apply KCL at P,

$$I_{C1} + I_{C2} = I_{ee}$$

$$I_{C1} = I_{C2} = I_C \quad \text{(since both are identical transistors)}$$

$$I_{C1} = I_{C2} = \frac{I_{ee}}{2}.$$

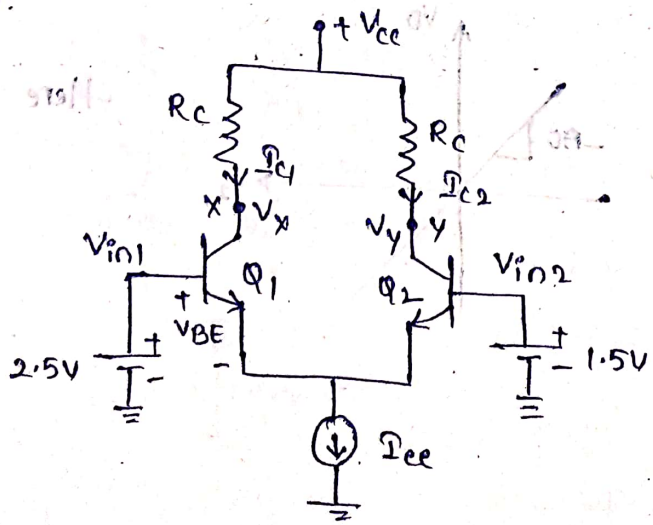
Voltage drop across $R_C = \frac{I_{ee}}{2} \times R_C$

$$V_y = V_x = V_{cc} - \frac{I_{ee}}{2} R_C$$

Differential amplifier signals are rejected by the common mode signal.

if $V_{in1} - V_{in2} = 0$; $V_x - V_y = 0$

Case ②:



Scanned with OKEN Scanner

consider Q_1 is ON,

from the circuit,

$$-V_{in1} + V_{BE} + V_p = 0$$

$$V_p = 2.5 - V_{BE} = 2.5 - 0.8V$$

$$= 1.7V$$

Q_2 is in OFF condition, since base voltage less than the emitter voltage (1.5V < 1.7V)

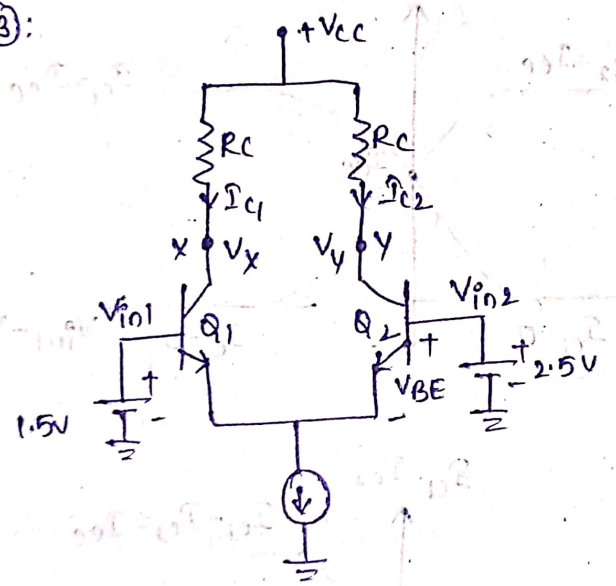
$$\therefore I_{C_2} = 0$$

$$V_y = V_{cc}$$

$$I_{C_1} = I_{ee}$$

$$V_x = V_{cc} - I_{ee} R_c$$

case (3):



consider Q_2 is ON,

from the circuit,

$$-V_{in2} + V_{BE} + V_p = 0$$

$$V_p = 2.5 - 0.8$$

$$= 1.7V$$

Q_1 is in OFF condition since base voltage is less than the emitter voltage (1.5 < 1.7V)

Scanned with OKEN Scanner

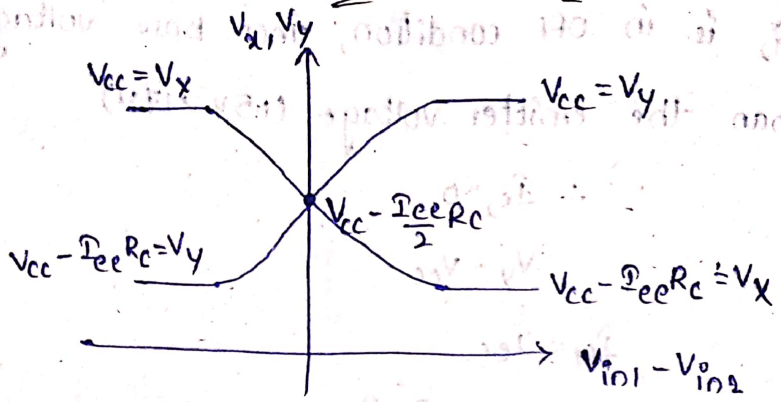
$\therefore I_{C1} = 0$

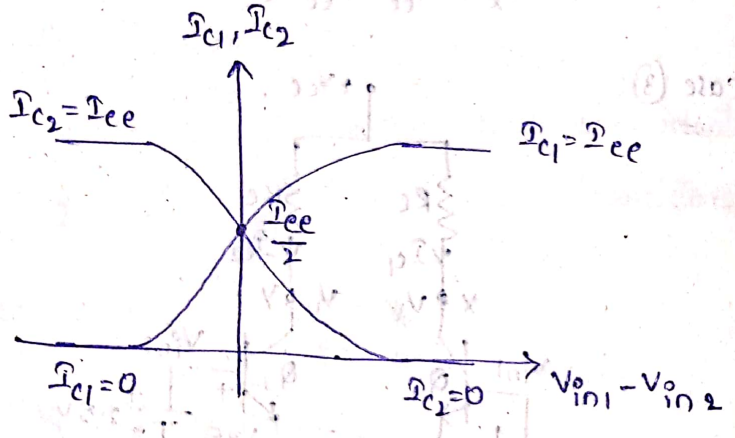
$V_x = V_{CC}$

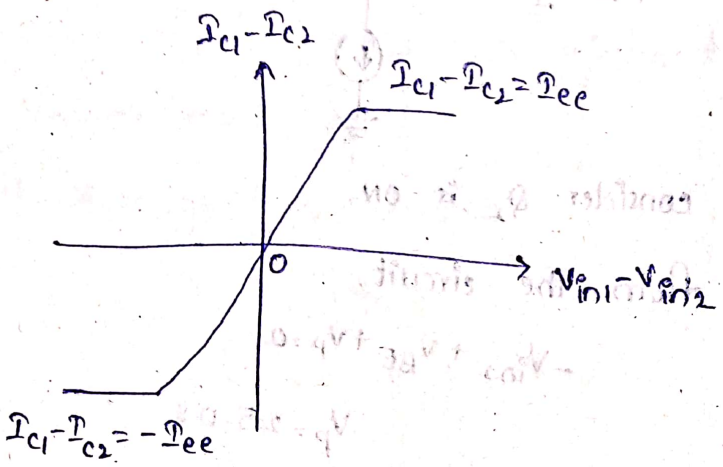
$I_{C2} = I_{EE}$

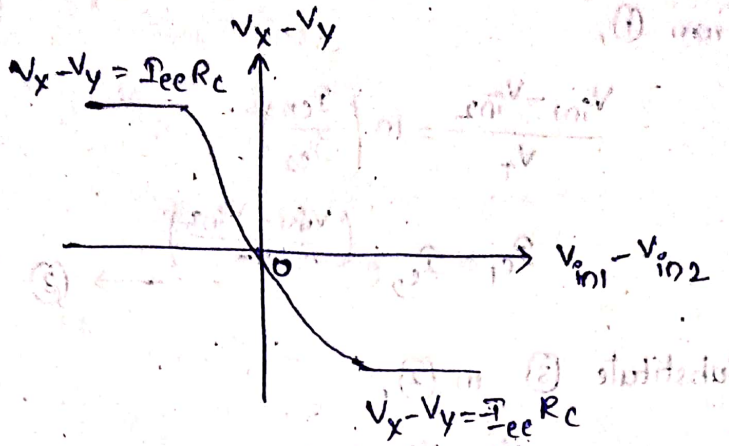
$V_y = V_{CC} - I_{EE} R_C$

I/o characteristics of differential amplifiers :









Objective:

Derive equations for I_{C1}, I_{C2}, V_x, V_y and $V_x - V_y$ as a function of $V_{in1} - V_{in2}$.

$$I_{C1} = I_S e^{\frac{V_{BE1}}{V_T}}$$

$$V_{BE1} = V_T \ln\left(\frac{I_{C1}}{I_S}\right)$$

$$I_{C2} = I_S e^{\frac{V_{BE2}}{V_T}}$$

$$V_{BE2} = V_T \ln\left(\frac{I_{C2}}{I_S}\right)$$

$$V_p = V_{in1} - V_{BE1}$$

$$V_p = V_{in2} - V_{BE2}$$

$$\Rightarrow V_{in1} - V_{BE1} = V_{in2} - V_{BE2}$$

$$V_{in1} - V_{in2} = V_{BE1} - V_{BE2}$$

$$V_{in1} - V_{in2} = V_T \ln\left(\frac{I_{C1}}{I_S}\right) - V_T \ln\left(\frac{I_{C2}}{I_S}\right)$$

$$V_{in1} - V_{in2} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right) \rightarrow (1)$$

from the circuit,

$$I_{C1} + I_{C2} = I_{ee} \rightarrow (2)$$

Scanned with OKEN Scanner

from ①,

$$\frac{V_{in1}-V_{in2}}{V_T} = \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

$$I_{C1} = I_{C2}\, e^{\left(\frac{V_{in1}-V_{in2}}{V_T}\right)} \longrightarrow ③$$

Substitute ③ in ②,

$$I_{C2}\, e^{\left(\frac{V_{in1}-V_{in2}}{V_T}\right)} + I_{C2} = I_{ee}$$

$$\boxed{I_{C2} = \frac{I_{ee}}{1+e^{\left(\frac{V_{in1}-V_{in2}}{V_T}\right)}}}$$

from ①,

$$I_{C2} = \frac{I_{C1}}{e^{\left(\frac{V_{in1}-V_{in2}}{V_T}\right)}}$$

Substitute in ②,

$$I_{C1} + \frac{I_{C1}}{e^{\left(\frac{V_{in1}-V_{in2}}{V_T}\right)}} = I_{ee}$$

$$I_{C1}\left[1 + \frac{1}{e^{\left(\frac{V_{in1}-V_{in2}}{V_T}\right)}}\right] = I_{ee}$$

$$I_{C1}\left[1 + e^{\left(\frac{V_{in2}-V_{in1}}{V_T}\right)}\right] = I_{ee}$$

$$\boxed{I_{C1} = \frac{I_{ee}}{1+e^{\left(\frac{V_{in2}-V_{in1}}{V_T}\right)}}}$$

Scanned with OKEN Scanner

Case ①: If $V_{in1} = V_{in2}$

$$I_{C1} = \frac{I_{ee}}{2}$$

$$I_{C2} = \frac{I_{ee}}{2}$$

Case ②: If $V_{in1} > V_{in2}$

$$I_{C1} = \frac{I_{ee}}{1+e^{\frac{-V_{in1}}{V_T}}} \qquad I_{C2} = \frac{I_{ee}}{1+e^{\frac{V_{in1}}{V_T}}}$$

Case ③: If $V_{in2} > V_{in1}$

$$I_{C1} = \frac{I_{ee}}{1+e^{\frac{V_{in2}}{V_T}}} \qquad I_{C2} = \frac{I_{ee}}{1+e^{\frac{-V_{in2}}{V_T}}}$$

Consider $V_x = V_{cc} - I_{ee}R_c = V_{cc} - I_{C1}R_c$

$$V_y = V_{cc} - I_{C2}R_c$$

$$V_x = V_{cc} - \frac{I_{ee}}{1+e^{\left(\frac{V_{in2}-V_{in1}}{V_T}\right)}} R_c$$

$$V_y = V_{cc} - \frac{I_{ee}}{1+e^{\left(\frac{V_{in1}-V_{in2}}{V_T}\right)}} R_c$$

$$V_x - V_y = V_{cc} - \frac{I_{ee}}{1+e^{\left(\frac{V_{in2}-V_{in1}}{V_T}\right)}} R_c - V_{cc} + \frac{I_{ee}}{1+e^{\left(\frac{V_{in1}-V_{in2}}{V_T}\right)}} R_c$$

$$V_x - V_y = -I_{ee}R_c \left[\frac{I_{ee}}{1+e^{\left(\frac{V_{in2}-V_{in1}}{V_T}\right)}} - \frac{I_{ee}}{1+e^{\left(\frac{V_{in1}-V_{in2}}{V_T}\right)}} \right]$$

Scanned with OKEN Scanner

$$V_x - V_y = -I_{ee}R_c\left[\frac{1}{1+e^{\frac{V_2-V_1}{V_T}}} - \frac{1}{1+e^{\frac{V_1-V_2}{V_T}}}\right]$$

$$= -I_{ee}R_c\left[\frac{1+e^{\frac{V_1-V_2}{V_T}} - 1 - e^{\frac{V_2-V_1}{V_T}}}{\left(1+e^{\frac{V_2-V_1}{V_T}}\right)\left(1+e^{\frac{V_1-V_2}{V_T}}\right)}\right]$$

let $\frac{V_1-V_2}{V_T} = x$ then $-\frac{(V_1-V_2)}{V_T} = -x$

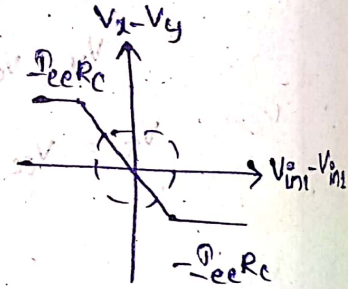
$$= -I_{ee}R_c\left[\frac{e^x - e^{-x}}{(1+e^{-x})(1+e^x)}\right]$$

$$= -I_{ee}R_c \tanh x$$

$$= -I_{ee}R_c \tanh\left(\frac{V_1-V_2}{2V_T}\right)$$

We need to eliminate the tan hyperbolic here to avoid the non-linear variation.

$$V_x - V_y = -I_{ee}R_c \tanh\left(\frac{V_{in1}-V_{in2}}{2V_T}\right)$$



(a) find the slope of the characteristic curve if $V_{in1} - V_{in2} = 0$.

$$\frac{V_{in1}-V_{in2}}{2V_T} << 1$$

then $\tanh\left(\frac{V_{in1}-V_{in2}}{2V_T}\right) << 1$

$$\Rightarrow \tanh\left(\frac{V_{in1}-V_{in2}}{2V_T}\right) = \frac{V_{in1}-V_{in2}}{2V_T}$$

Scanned with OKEN Scanner

Now,

$$V_x - V_y = -R_c I_{ee}\left(\frac{V_{in1} - V_{in2}}{2V_T}\right)$$

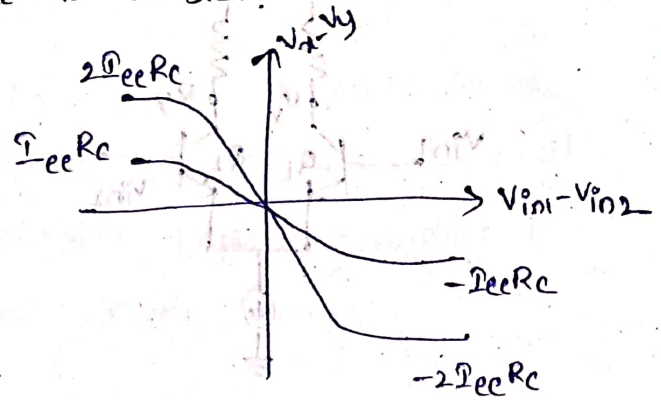
$$A_d = \frac{V_x - V_y}{V_{in1} - V_{in2}} = \frac{-R_c I_{ee}}{2V_T} \simeq \text{slope}$$

$\downarrow$ differential gain

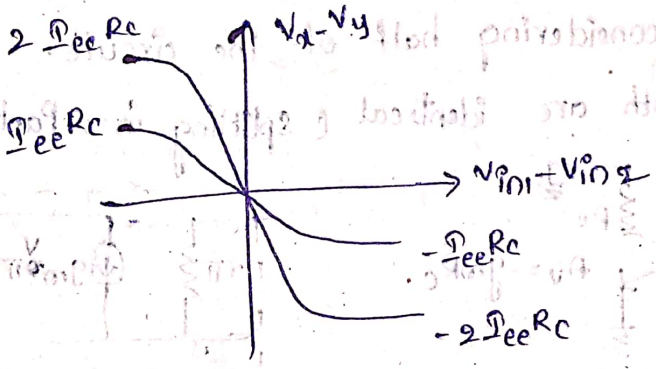
= gain

what happens if I_{ee} is doubled?

→ slope increases hence gain increases.



what happens if R_c is doubled?



what happens if ambient temperature drops to accordingly or considerably.

$$V_T \propto \frac{1}{\text{slope}}$$

if $V_T \downarrow$ then slope $\uparrow$

* CMRR = common mode rejection ratio

A_C = common mode gain

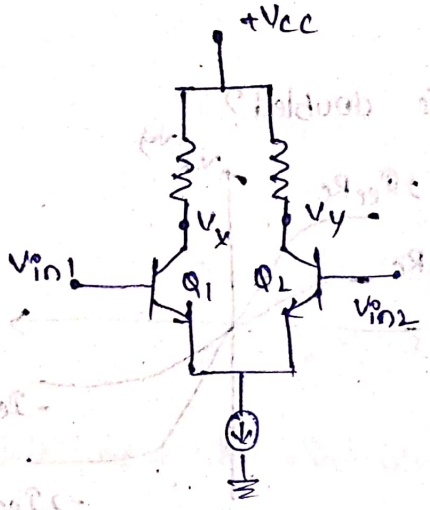
Scanned with OKEN Scanner

A_d = differential gain

$A_c = \frac{V_{in1} + V_{in2}}{2}$ $\qquad A_d = V_{in1} - V_{in2}$

$CMRR = \frac{A_d}{A_c}$

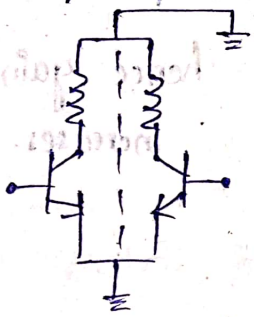
Small signal model of BJT:



Both Q_1 & Q_2 are identical

$g_{m1} = g_{m2} = g_m$

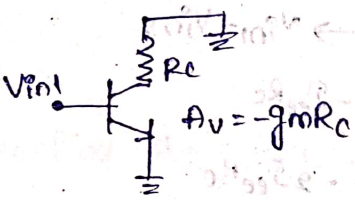
$\Rightarrow$ Ac equivalent

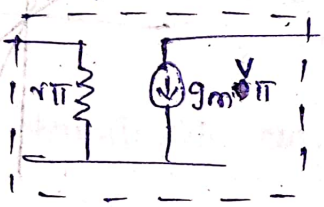


(Ac Model)

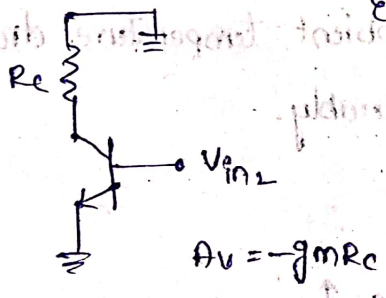
Case (i):

Only considering half of the circuit as both are identical (splitting in 2 Parts)





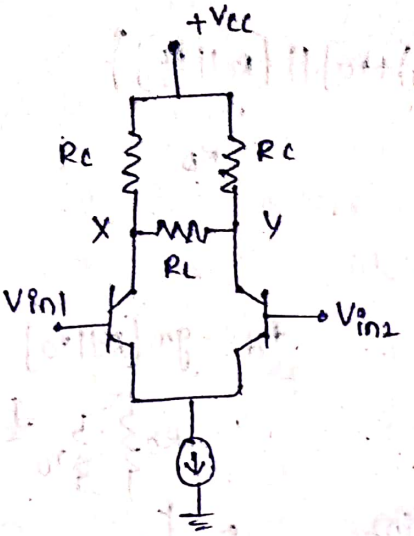
Equivalent small circuit in BJT:



if $V_A \neq 0$ (Early voltage)

then $A_v = -g_m (R_c \| r_o)$

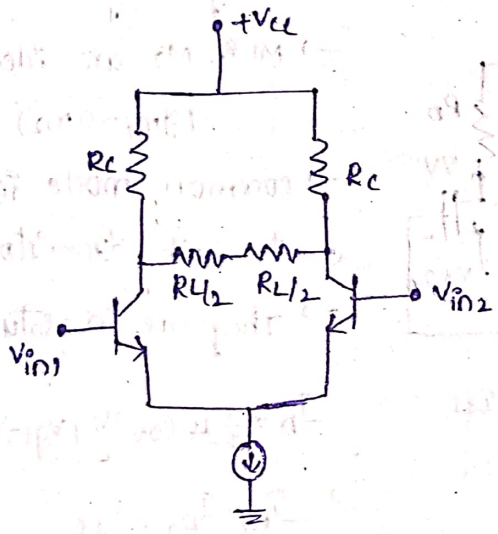
Case (2):



As the R_L is placed in between the x and y then R_L is divided into two halfs equally to both transistors

$$Z_o = \frac{R}{1-\frac{1}{A_V}} \simeq R$$ → if a resistor is placed in b/w i/p and o/p then the division of resistance happens according to the Millen's theorem

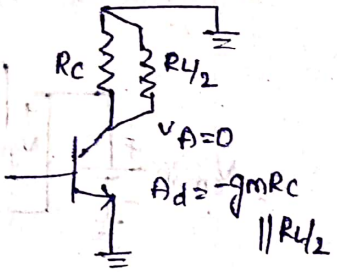
$$Z_i = \frac{R}{1-A_V}$$



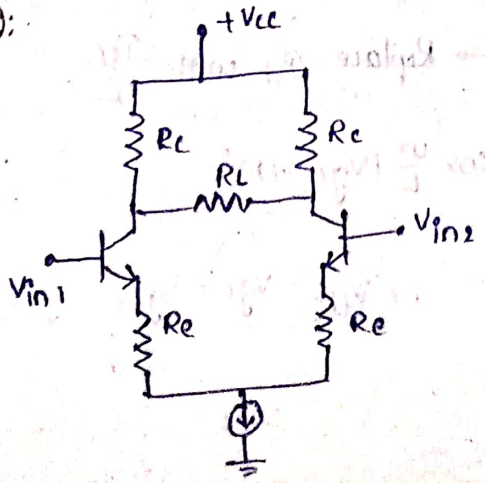
$V_A \neq 0$

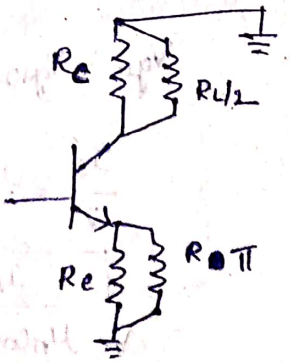
$$A_d = -g_m R_c \,||\, \frac{R_L}{2} \,||\, r_o$$

$A_d = -g_m R_c \,||\, R_L/2$



Case (3):





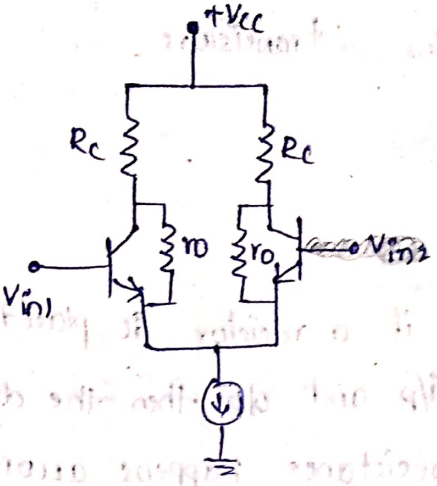
Scanned with OKEN Scanner

$A_d = -g_m R_{out}$

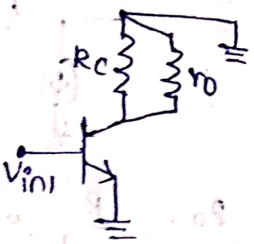
$R_{out} = \left(\left[(1+g_m r_o)(r_e \| r_\pi) + r_o \right] \| \left[R_c \| \frac{R_L}{2} \right] \right)$

R_s ↑ ; R_D ↑

Case (4):-



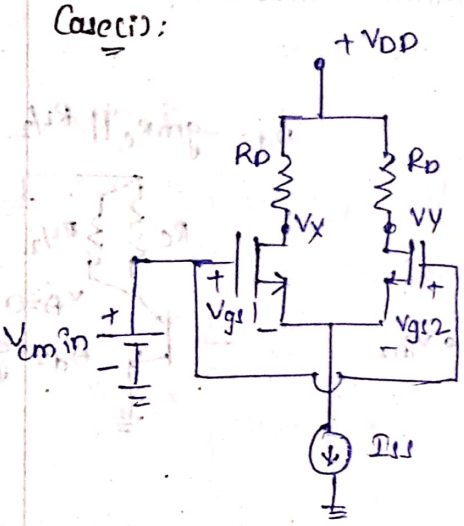
$A_d = -g_m [R_c \| r_o]$



half symmetrical circuit

MOSFET differential amplifier:

Case (i):



Large signal analysis

→ M1 & M2 are identical ($g_{m1} = g_{m2}$)

→ common mode input is to both transistors

→ They are in saturation

$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2$

$I_{D1} + I_{D2} = I_{SS}$

→ as they are symmetric

$I_{D1} = I_{D2} = \frac{I_{SS}}{2}$

$V_{gs1} = V_{gs2}$ → Replace I_d with $\frac{I_{SS}}{2}$

$\frac{I_{SS}}{2} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs1} - V_{th})^2$

$\sqrt{\frac{I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} + V_{th} = V_{gs} = V_{gs1} = V_{gs2}$

$$V_{gs} - V_{th} = \sqrt{\frac{I_{ss}}{\mu_n C_{ox} \frac{W}{L}}}$$ differential overdrive voltage

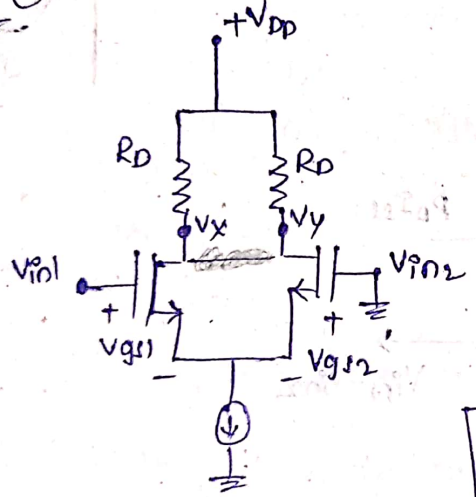
→ if $V_{in1} = V_{in2}$ the differential pair is in equilibrium so that equilibrium overdrive voltage of the differential amplifier is given by

$$V_{gs} - V_{th} = \sqrt{\frac{I_{ss}}{\mu_n C_{ox} W/L}}$$

→ Even if we suddenly change the input voltage, the MOSFET o/p doesn't get changed. here,

$V_x = V_{DD} - \frac{I_{ss}}{2} R_D$, $V_y = V_{dd} - \frac{I_{ss}}{2} R_D$.

Case (2):



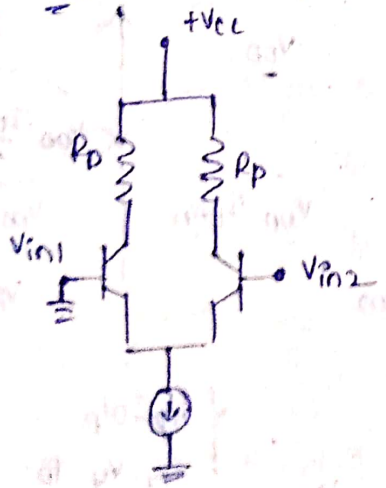
if $V_{in2} = 0V$ then the mosfet will not be in saturation.

$I_{D2} = 0$

$I_{D1} = I_{DD} = I_D$

$$V_x = V_{DD} - I_D R_D$$
$$V_y = V_{DD}$$

Case (3):



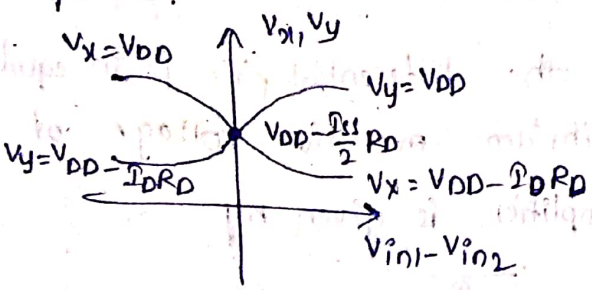
M1 is off and M2 is ON and in saturation.

$I_{D1} = 0$

$$V_x = V_{DD}$$
$$V_y = V_{DD} - I_D R_D$$

Scanned with OKEN Scanner

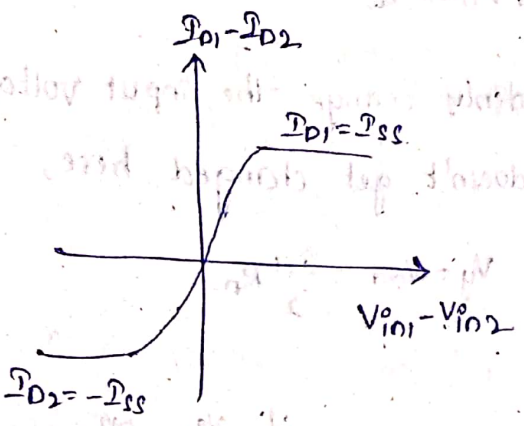
Input-Output characteristics of the MOSFET differential amplifiers:

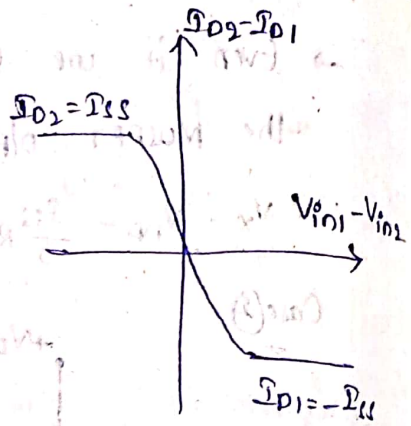


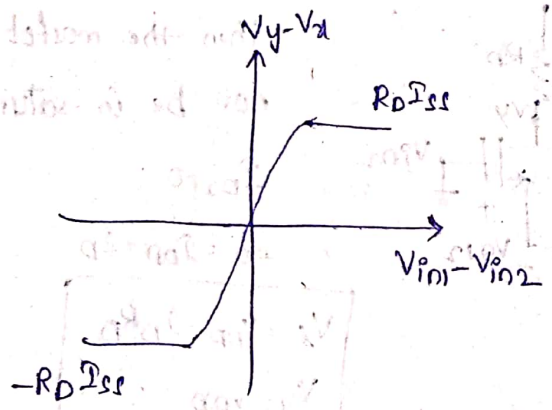
Case ①: $V_{DD} - \frac{I_{SS}}{2} R_D$

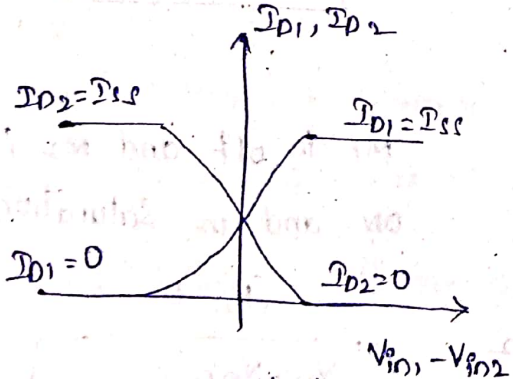
Case ②: $V_x = V_{DD} - I_D R_D$
$V_y = V_{DD}$

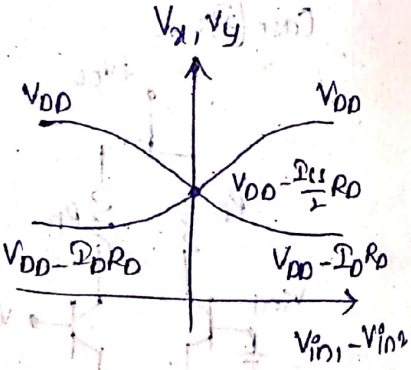
Case ③: $V_x = V_{DD}$
$V_y = V_{DD} - I_D R_D$

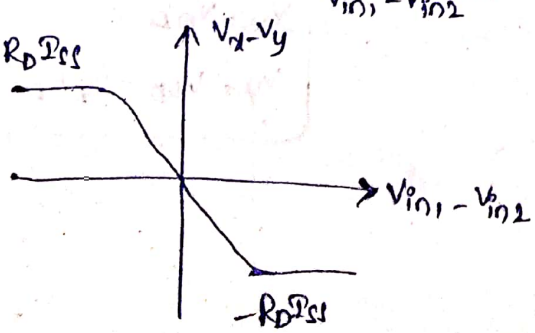










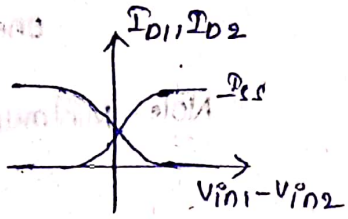


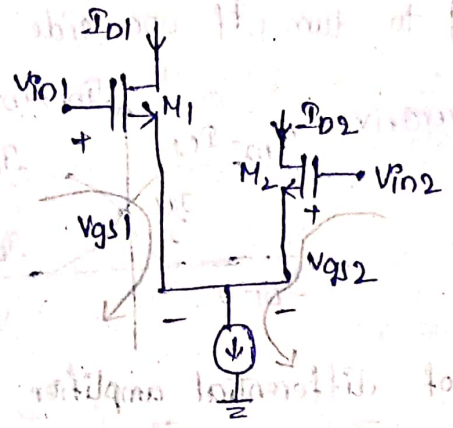
{ i/p - o/p
$V_x - V_y$ to
$V_{in1} - V_{in2}$ }

* Min voltage required to turn off the one transistor $(V_{in1} - V_{in2})$

M_2 off & M_1 is in saturation.

(a) What is the minimum value of $V_{in1} - V_{in2}$ at which one transistor is turned off.





→ M_1 is in higher potential than M_2

→ M_1 is ON.

$I_{D1} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{gs1} - V_{th})^2$

$I_{D1} = I_D$

$$\boxed{V_{gs1} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} + V_{th}}$$

Case (2): M_2 is off

$I_{D2} = 0$

$I_{D2} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{gs2} - V_{th})^2$

$\frac{1}{2}\mu_n C_{ox} \frac{W}{L} = 0 \Rightarrow V_{gs2} - V_{th} = 0$

$$\boxed{V_{gs2} = V_{th}}$$

applying KVL in the input loop

$-V_{in1} + V_{gs1} + V_p = 0$

$V_p = V_{in1} - V_{gs1}$

$V_p = V_{in2} - V_{gs2}$

$V_{in1} - V_{gs1} = V_{in2} - V_{gs2}$

$V_{in1} - \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} - V_{th} = V_{in2} - V_{th}$

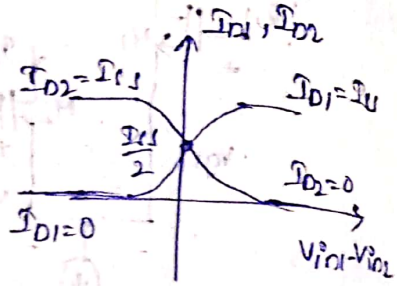
Scanned with OKEN Scanner

$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}} = \sqrt{2}\, V_{OV}$$

↓

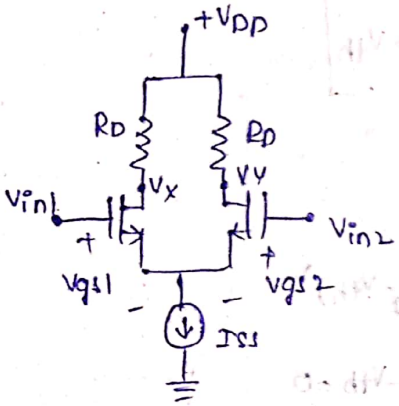
voltage required to turn off one transistor ($\sqrt{2}V_{OV}$)

Note: Minimum $|V_{in1} - V_{in2}|$ to turn off one side $= \sqrt{2}\, V_{overdrive}$



Large Signal analysis of differential amplifier

MOSFET:



applying the KVL for the input loop,

$$-V_{in1} + V_{gs1} + V_P = 0$$

$$V_P = V_{in1} - V_{gs1}$$

$$V_P = V_{in2} - V_{gs2}$$

$$V_{gs1} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} + V_{th}$$

$$V_{gs2} = \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}} + V_{th}$$

$$\Rightarrow V_{in1} - V_{in2} = V_{gs1} - V_{gs2}$$

$$\Rightarrow V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}}$$

$$V_X = V_{DD} - I_{D1}R_D$$

$$V_Y = V_{DD} - I_{D2}R_D$$

$$V_X - V_Y = -R_D(I_{D1} - I_{D2})$$

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs1} - V_{th})^2$$

Scanned with OKEN Scanner

$$\sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} = V_{gs1} - V_{th}$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs2} - V_{th})^2$$

$$\sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}} = V_{gs2} - V_{th}$$

$$V_{gs1} - V_{th} - V_{gs2} + V_{th} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}}$$

$$V_{gs1} - V_{gs2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}}$$

$$(V_{gs1} - V_{gs2})^2 = \frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}} + \frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}} - \sqrt{\frac{4I_{D1}I_{D2}}{(\mu_n C_{ox}\frac{W}{L})^2}}$$

$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$

Case (1): $I_{D1} - I_{D2} = 0$ if $V_{in1} - V_{in2} = 0$

Case (2): It is valid only if $V_{in1} - V_{in2} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$

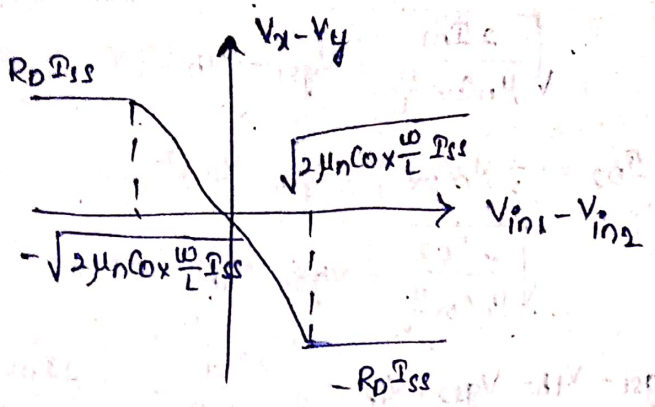
the above equation is valid only if M1 & M2 are on (or) near tearing off if $V_{in1} - V_{in2} = 0$

then $I_{D1} = I_{D2}$

Differential current equation can be valid only if $|V_{in1} - V_{in2}| \leq \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$

$$V_x - V_y = -\frac{R_D}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$

Scanned with OKEN Scanner



Case (i):

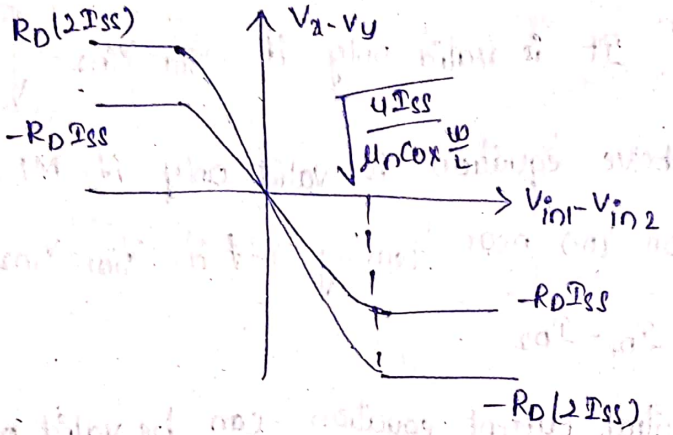
$$\text{if } (V_{in1} - V_{in2})^2 << \frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}}$$

$$V_x - V_y = -\frac{R_D}{2} \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2}) 2 \sqrt{\frac{I_{SS}}{\mu_n C_{ox} \frac{W}{L}}}$$

$$= -R_D \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}} \quad (V_{in1} - V_{in2})$$

$$\text{Slope} = A_d = \frac{V_x - V_y}{V_{in1} - V_{in2}} = -R_D \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}}$$

Case (ii): What happens if I_{SS} is doubled



~~Among~~ Among those two curves which is more linear

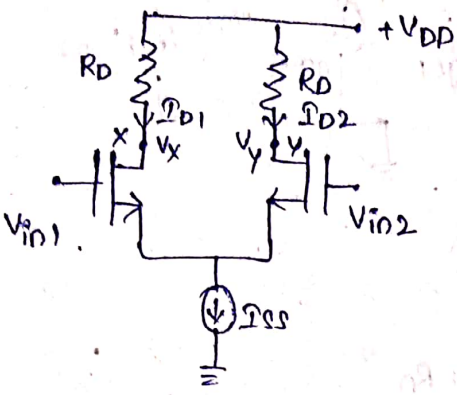
⇒ Second one is more linear.

* If $\frac{W}{L}$ is doubled ⇒ linearity decreases

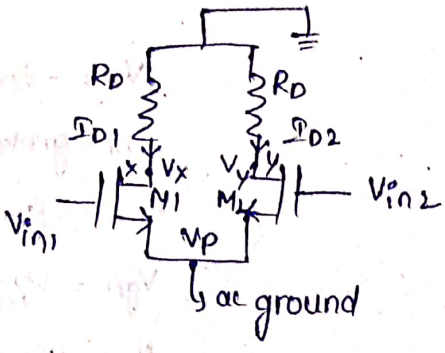
⇒ The circuit becomes less linear because it can take only a smaller input difference before it dies.

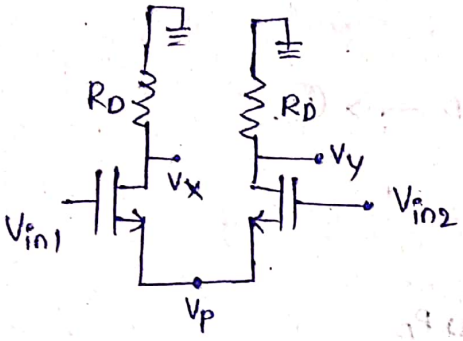
Scanned with OKEN Scanner

Small signal analysis of the MOSFET differential amplifier.

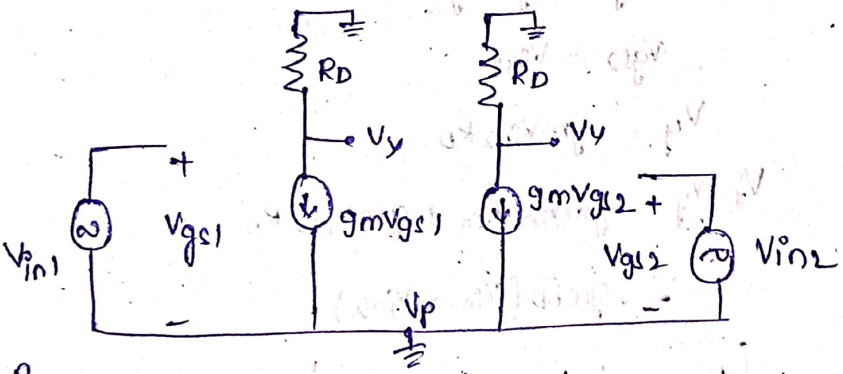


all dc components are short and open circuited.





$g_{m1} = g_{m2} = g_m$



Because of identical property, from input loop

$$-V_{in1} + V_{gs1} + V_p = 0$$

$$V_p = V_{in1} - V_{gs1}$$

2nd i/p loop, $-V_{in2} + V_{gs2} + V_p = 0$

$$V_p = V_{in2} - V_{gs2}$$

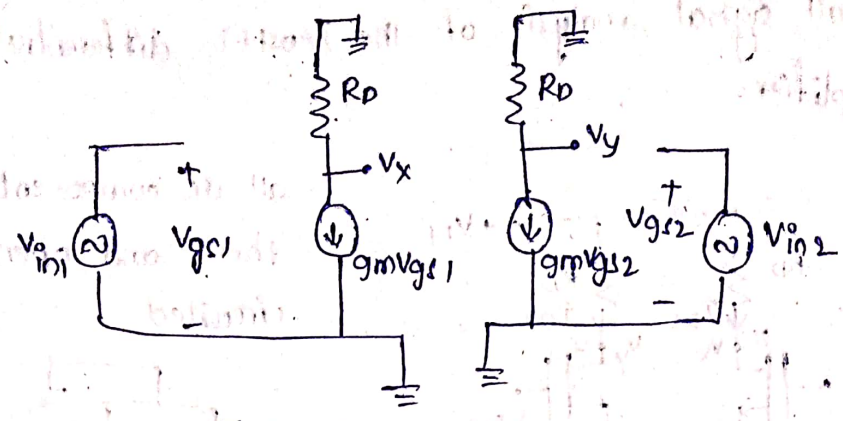
$$V_{in1} - V_{in2} = V_{gs1} - V_{gs2}$$

from the circuit,

$$I_{D1} + I_{D2} = 0$$

$$g_m V_{gs1} + g_m V_{gs2} = 0 \Rightarrow V_{gs1} = -V_{gs2}$$

Scanned with OKEN Scanner



$$V_x = -I_{D1} R_D$$

$$I_{D1} = g_m V_{gs1}$$

$$V_x = -g_m V_{gs1} R_D$$

$$V_{gs1} = V_{in1}$$

$$V_x = -g_m V_{in1} R_D \longrightarrow (1)$$

$$V_y = -I_{D2} R_D$$

$$I_{D2} = g_m V_{gs2}$$

$$V_y = -g_m V_{gs2} R_D$$

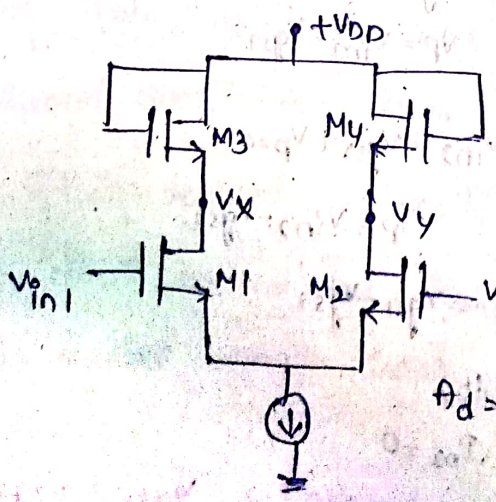
$$V_{gs2} = V_{in2}$$

$$V_y = -g_m V_{in2} R_D$$

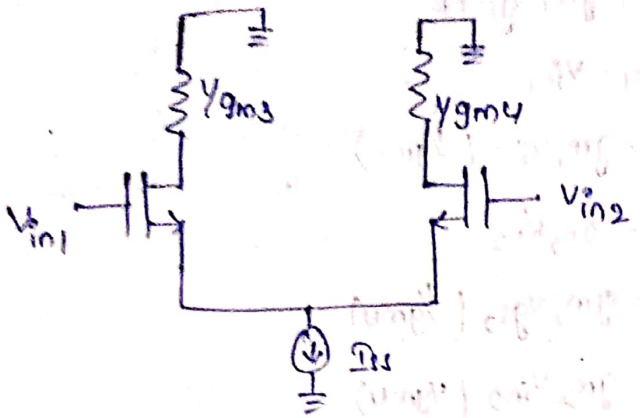
$$V_x - V_y = -g_m V_{in1} R_D + g_m V_{in2} R_D$$

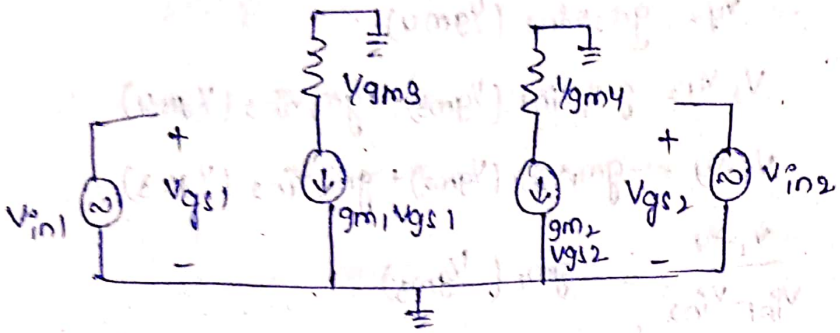
$$= -g_m R_D (V_{in1} - V_{in2})$$

$$\boxed{A_d = \frac{V_x - V_y}{V_{in1} - V_{in2}} = -g_m R_D}$$



$$A_d = -g_{m1}\left(\frac{1}{g_{m3}} \| r_o\right)$$





$$-V_{in1} + V_{gs1} + V_p = 0$$

$$V_p = V_{in1} - V_{gs1}$$

$$-V_{in2} + V_{gs2} + V_p = 0$$

$$V_p = V_{in2} - V_{gs2}$$

$$V_{in1} - V_{in2} = V_{gs1} - V_{gs2}$$

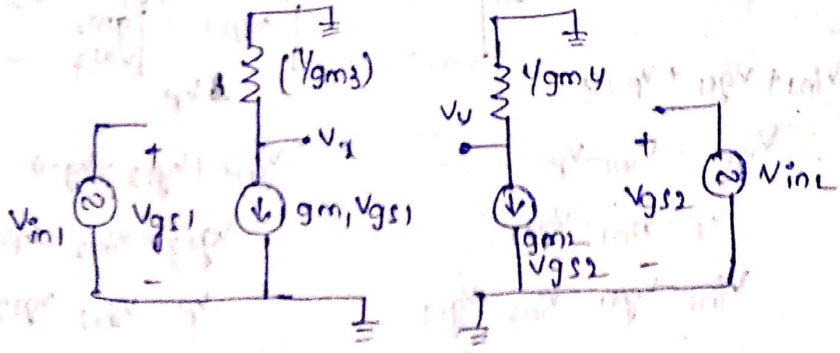
from the circuit,

$$I_{D1} + I_{D2} = 0$$

$$g_{m1} V_{gs1} + g_{m2} V_{gs2} = 0$$

$$g_{m1} V_{gs1} = -g_{m2} V_{gs2}$$

$$V_{gs2} = \frac{-g_{m1} V_{gs1}}{g_{m2}}$$



$$V_x = -I_{D1} R_D$$

$I_{D1} = g_{m1} V_{gs1}$

$V_{gs1} = V_{in1}$

$V_x = -g_{m1} V_{in1} (1/g_{m3})$

$V_y = -I_{D2} R_{D2}$

$I_{D2} = g_{m2} V_{gs2} (1/g_{m4})$

$I_{D2} = g_{m2} V_{in2} (1/g_{m4})$

$V_y = -g_{m2} V_{in2} (1/g_{m4})$

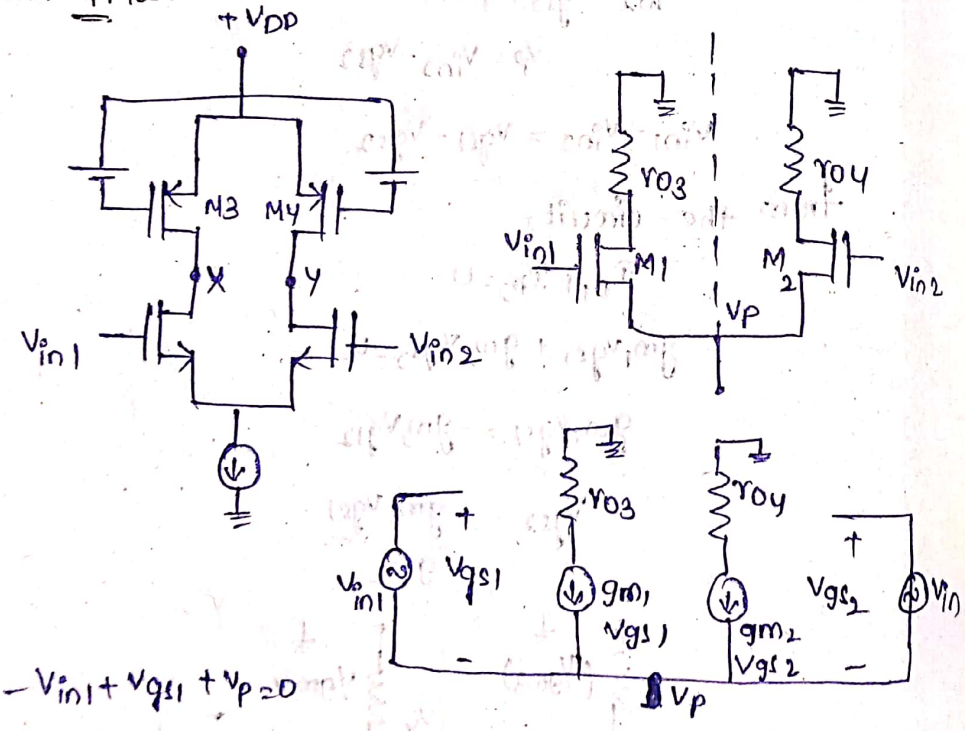
$V_x - V_y = -g_{m1} V_{in1} (1/g_{m3}) + g_{m2} V_{in2} (1/g_{m4})$

$V_x - V_y = -g_{m1} V_{in1} (1/g_{m3}) + g_{m1} V_{in2} (1/g_{m3})$

$$\frac{V_x - V_y}{V_{in1} - V_{in2}} = -g_{m1} (1/g_{m3})$$

$\lambda \neq 0$ $$\frac{V_x - V_y}{V_{in1} - V_{in2}} = -g_{m1} \left(\frac{1}{g_{m3}} \| r_o\right)$$

With PMOS:



$-V_{in1} + V_{gs1} + V_P = 0$

$V_{gs1} = V_{in1} - V_P$

$V_P = V_{in1} - V_{gs1}$

$V_{in1} - V_{gs1} = V_{in2} - V_{gs2}$

$V_{in1} - V_{in2} = V_{gs1} - V_{gs2}$

$-V_{in2} + V_{gs2} + V_g = 0$

$V_{gs2} = V_{in2} - V_P$

$V_P = V_{in2} - V_{gs2}$

Scanned with OKEN Scanner

$I_{D1} + I_{D2} = 0$

$g_{m1} V_{gs1} + g_{m2} V_{gs2} = 0$

$g_{m1} V_{gs1} = -g_{m2} V_{gs2}$

both are identical

$V_{gs1} = -V_{gs2}$

$V_x = -I_{D1} R_{D1}$ $\qquad$ $V_y = -I_{D2} R_{D2}$

$I_{D1} = g_{m1} V_{gs1}$ $\qquad$ $I_{D2} = g_{m2} V_{gs2}$

$V_x = -g_{m1} V_{gs1} r_{O3}$ $\qquad$ $V_y = -g_{m2} V_{gs2} r_{O4}$

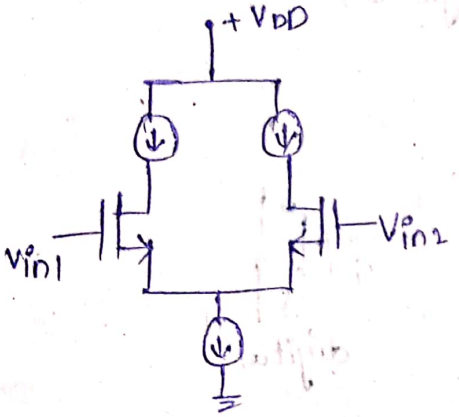
$V_x - V_y = -g_{m1} V_{in1} r_{O3} + g_{m2} V_{in2} r_{O3}$

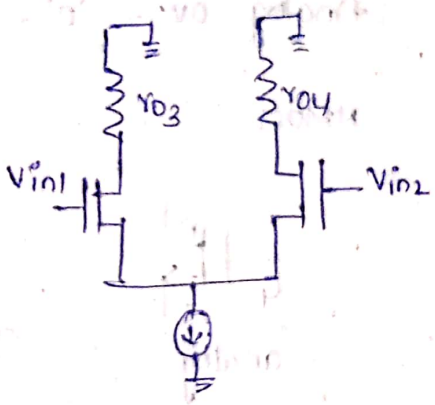
$= -g_{m1} V_{in1} r_{O3} + g_{m1} V_{in2} r_{O3}$

$$\frac{V_x - V_y}{V_{in1} - V_{in2}} = -g_{m1} r_{O3}$$

$\lambda \neq 0 \quad -g_{m1} (r_{O3} \| r_{O1})$

with current source

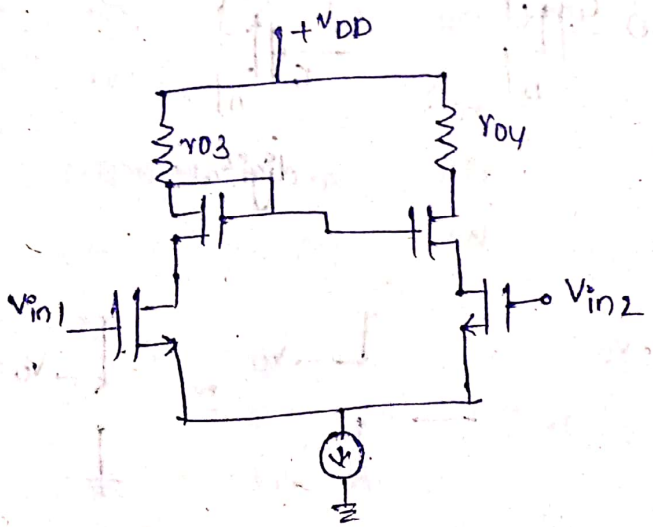




$A_d = -g_{m1} r_{O3} \quad \lambda = 0$

$-g_{m1} (r_{O3} \| r_{O1}) \quad \lambda \neq 0$

with current mirror



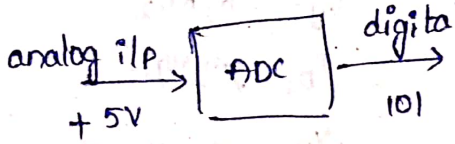
$$\frac{I_{ref}}{I_{out}} = \frac{W_1/L_1}{W_2/L_2}$$

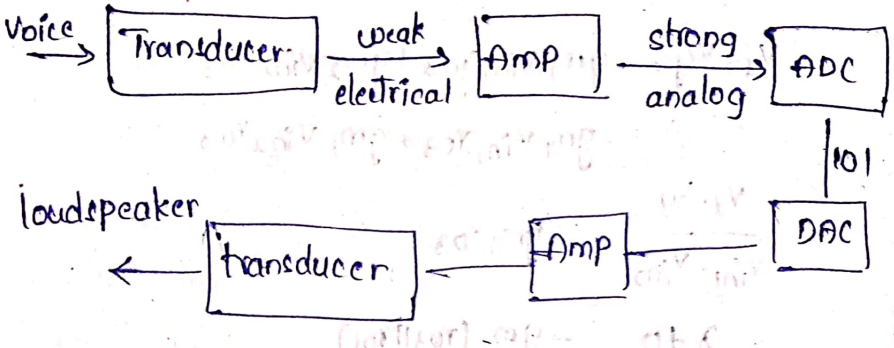
$$I_{out} = I_{ref} \frac{(W/L)_2}{(W/L)_1}$$

CMOS: complementary metal oxide semiconductor

⇓

maximum i/p voltage +5V.

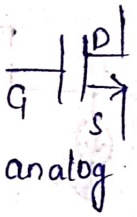




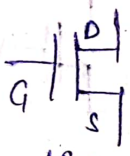
Analog +5V – 1 – logic1, high

Analog 0V – '0' – logic-0, low

NMOS:

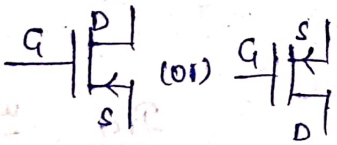


analog

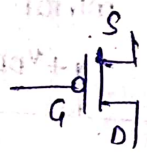


digital

PMOS:

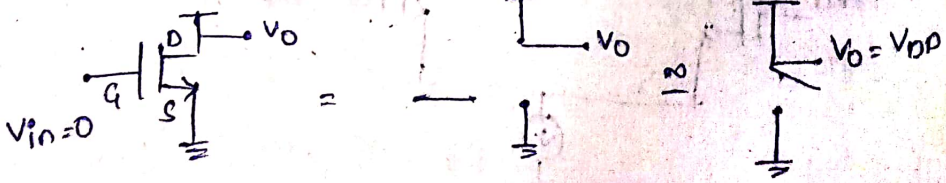


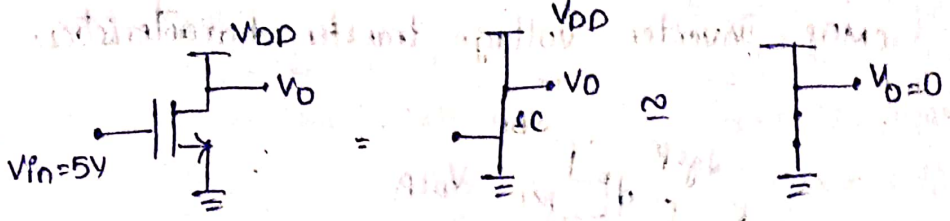
analog



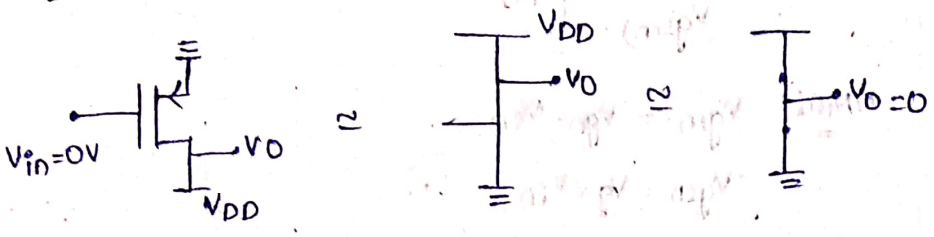
digital

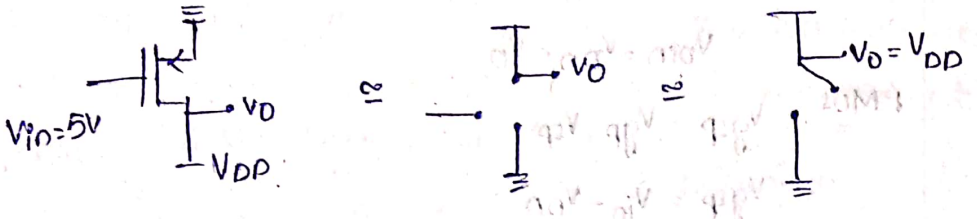
NMOS:



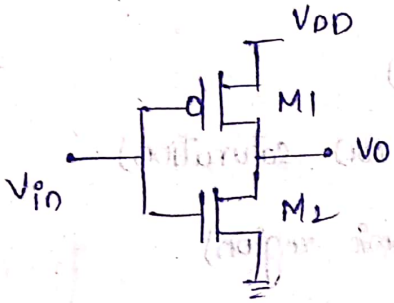


PMOS:





CMOS Inverter:



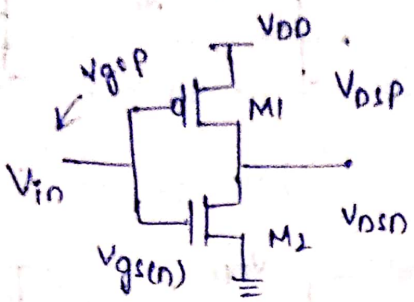
CMOS inverter can be establish by cascading of PMOS & NMOS body of NMOS should be connected to lower power supply (or) ground. & the body of PMOS should be connected to high power supply. (or) V_{DD}.

	+5V	0V
(M2) NMOS	ON	OFF
(M1) PMOS	OFF	ON

Vin	M1	M2	VO
0	ON	OFF	VDD
1	OFF	ON	0

Scanned with OKEN Scanner

CMOS Inverter voltage transfer characteristics:



NMOS: $V_{gsn} = V_{gn} - V_{sn}$

$V_{gsn} = V_g = V_{in}$

$V_{DSn} = V_{Dn} - V_{sn}$

$V_{DSn} = V_{Dn} = V_O$

PMOS: $V_{gsp} = V_{gp} - V_{sp}$

$V_{gsp} = V_{in} - V_{DD}$

$V_{DSp} = V_{Dsp} - V_{sp}$

$V_{DSp} = V_D - V_{DD}$

NMOS: $V_{gsn} < V_{th}$ (cutoff)

$V_{gsn} > V_{th}$ (linear (or) saturation)

$V_{gsn} - V_{th} > V_{DSn}$ (ohmic region)

$V_{gsn} - V_{th} < V_{DSn}$ (saturation region)

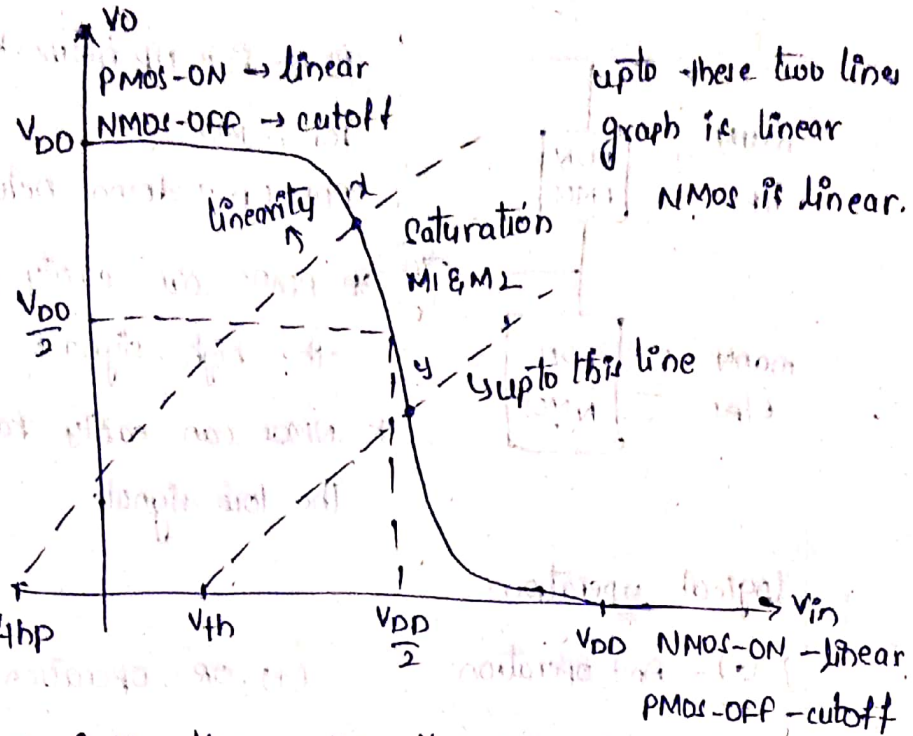
PMOS: $V_{gsp} < V_{th}$ (saturation (or) linear)

$V_{gsp} > V_{th}$ (cutoff)

$V_{gsp} - V_{th} > V_{DSp}$ (saturation)

$V_{gsp} - V_{th} < V_{DSp}$ (ohmic (or) linear)

Scanned with OKEN Scanner



upto these two lines graph is linear

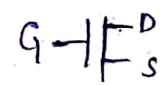
NMOS is linear.

b/w x & y, $V_{gsn} - V_{th} < V_{DSn}$ } saturation

$V_{gsp} - V_{th} > V_{DSp}$ }

CMOS logic circuit rules:

CMOS
- NMOS
- PMOS



$V_{in}=0$

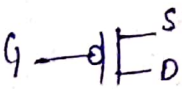
N-MOS can pass low signals

if $V_{in}=0$, NMOS-OFF (D to S is o.c)

$V_o = V_{dd}$

if $V_{in}=1$, NMOS-ON (D to S is s.c)

$V_o = 0$

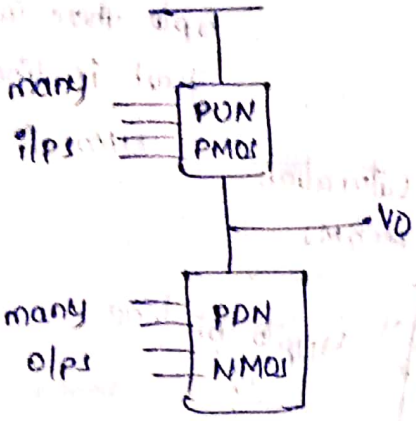


$V_o=0$ if $V_{in}=0$, PMOS-ON (S to D is short circuited)

$V_o=V_{dd}$ if $V_{in}=1$, PMOS-OFF (S to D is Open circuited)

PMOS can easily pass high signals.

Scanned with OKEN Scanner



PUN- Pull up network (PMOS)
-for N-MOS
PDN (Pull down network)

* PMOS can easily passes the high signals.
* NMOS can easily passes the low signals.

Logical operation:

(·)- And operation

PMOS- parallel
NMOS- series

$\overline{A \cdot B} = \overline{AB}$

(+) OR operation

PMOS - Series
NMOS - Parallel

We apply inverter to the output it already it is as NOT then we don't apply inverter.

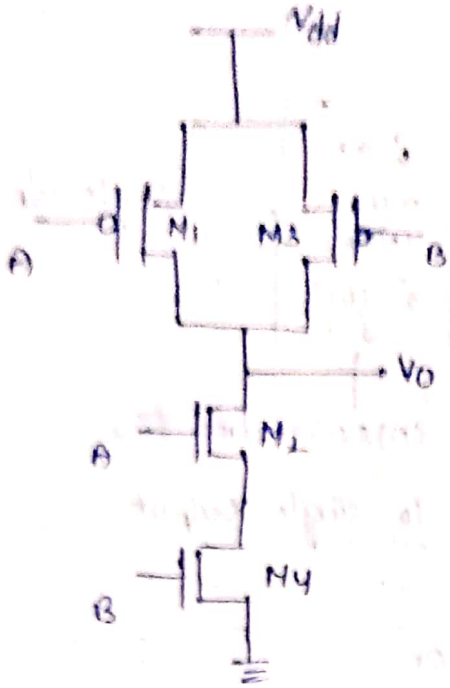
NAND Gate:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

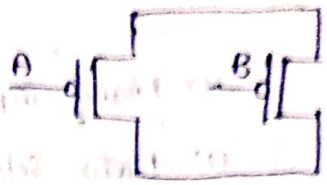


$Y = \overline{AB}$

Scanned with OKEN Scanner



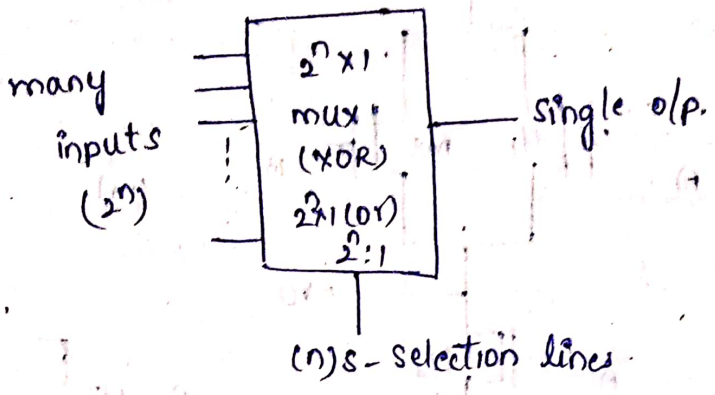
(or)



A	B	M_1	M_3	M_2	M_4	V_O
0	0	1	1	0	0	1
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	1	0	0	1	1	0

Scanned with OKEN Scanner

Multiplexer:



(1) Many inputs to single Output

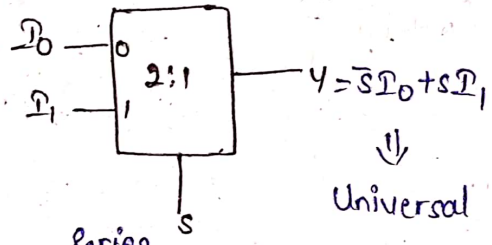
(2) Data Selector

(3) Data combinor

(4) Parallel to serial converter

(5) Universal equation circuit.

2×1 mux:



S	Y
0	D_0
1	D_1

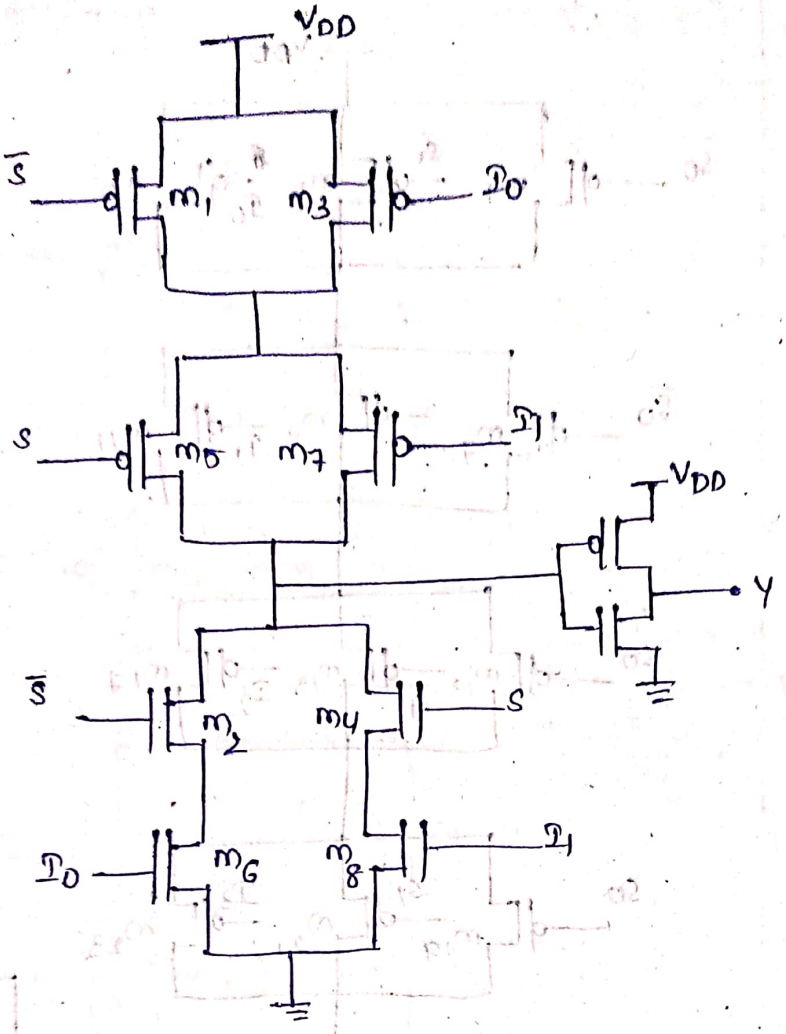
Universal equation of MUX

Series

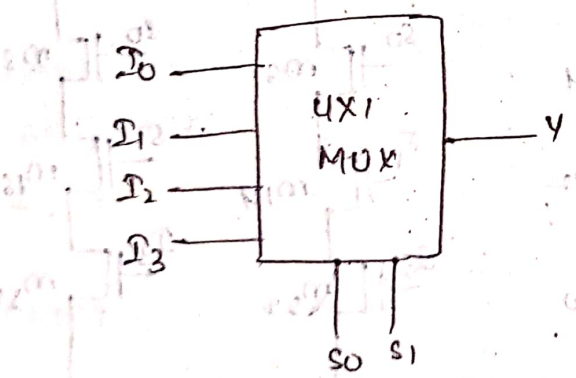
$Y = \bar{s}D_0 + sD_1$

PMOS → Parallel

Parallel



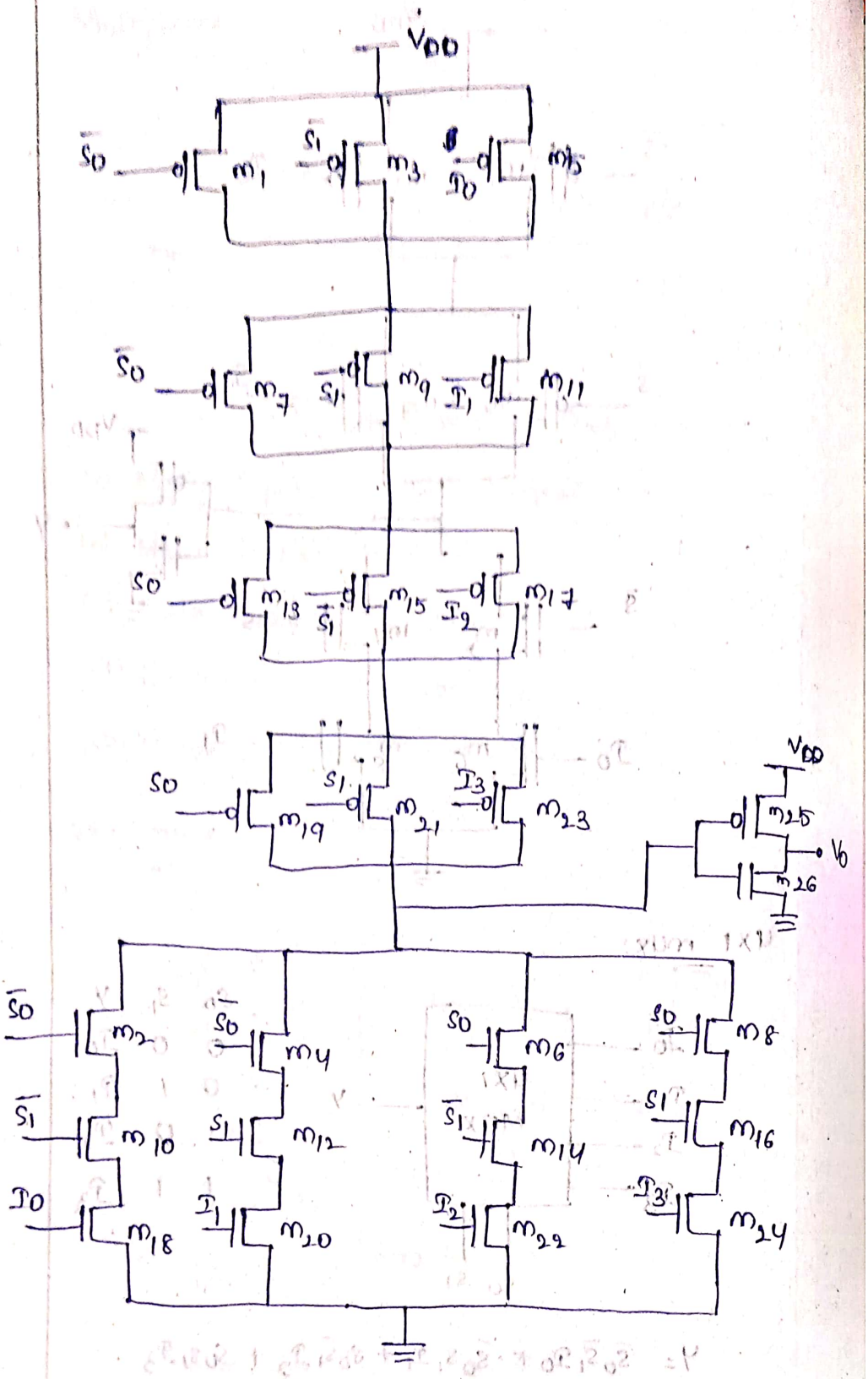
4X1 mux:



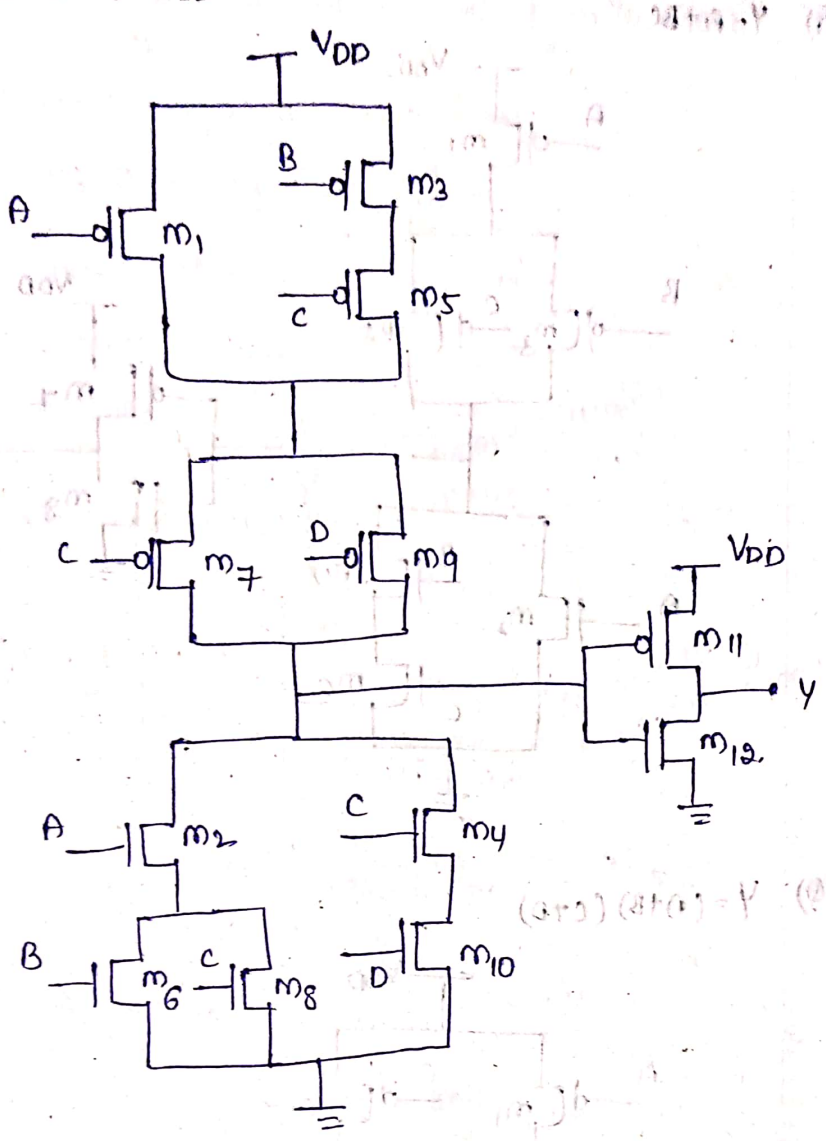
S_0	S_1	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

$$Y = \bar{S}_0 \bar{S}_1 D_0 + \bar{S}_0 S_1 D_1 + S_0 \bar{S}_1 D_2 + S_0 S_1 D_3$$

Scanned with OKEN Scanner


VDD
S0
S1
I0
I1
I2
I3
m1
m2
m3
m4
m5
m6
m7
m8
m9
m10
m11
m12
m13
m14
m15
m16
m17
m18
m19
m20
m21
m22
m23
m24
m25
m26
Vo

$F = A \cdot (B+C) + CD$



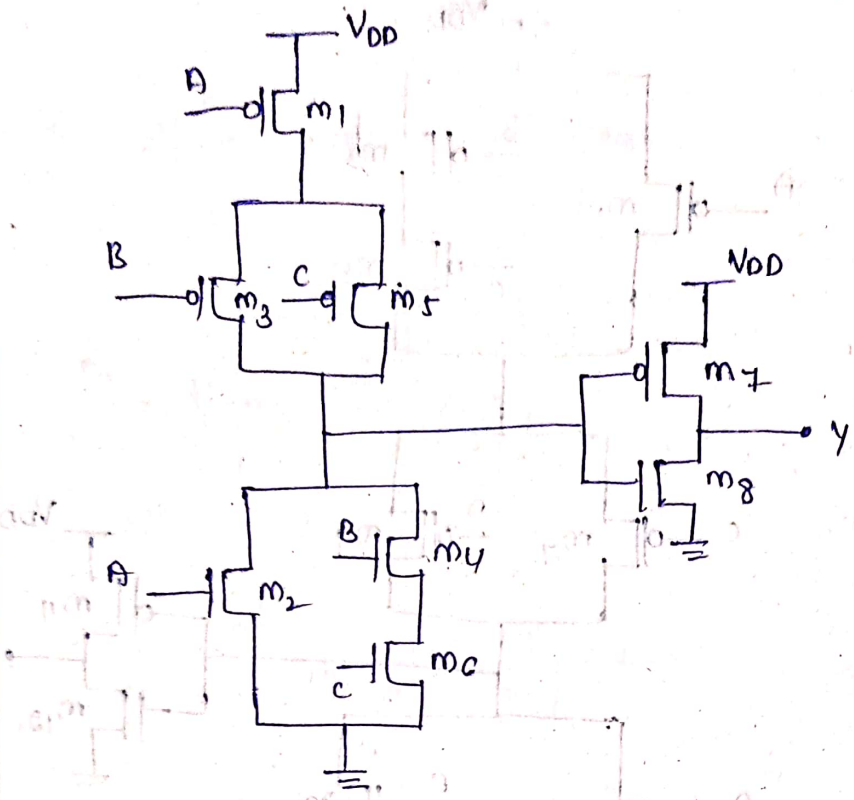
Q) $A+BC$

Q) $(A+B)(C+D)$

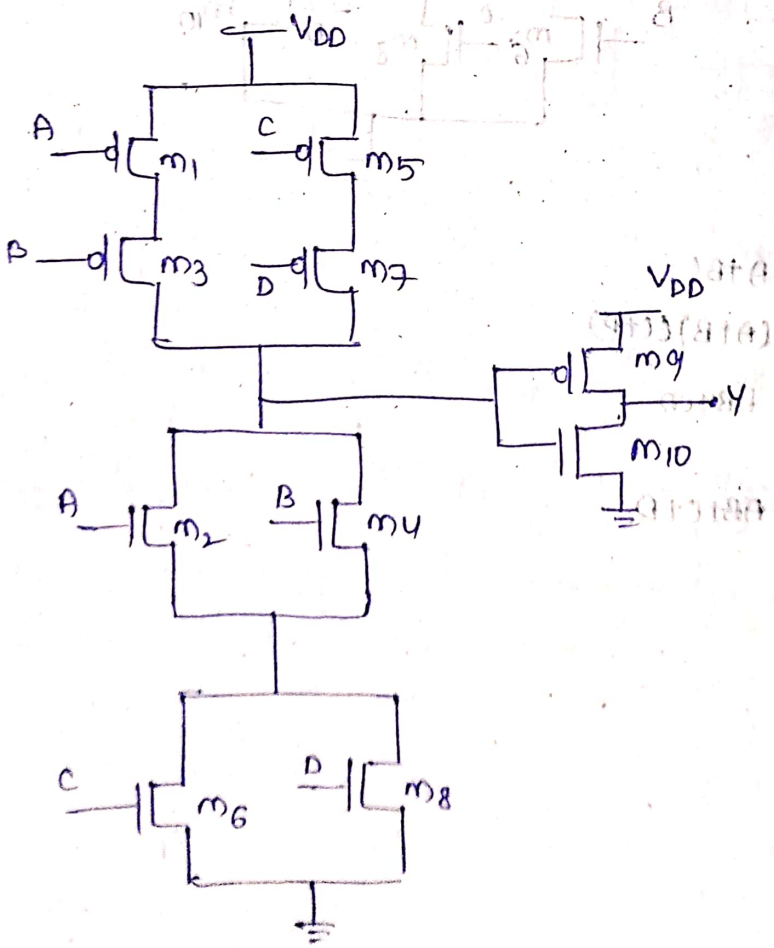
Q) $AB+CD$

Q) $AB+C+D$

Q) $Y = A + BC$



Q) $Y = (\bar{A}+B)(C+D)$



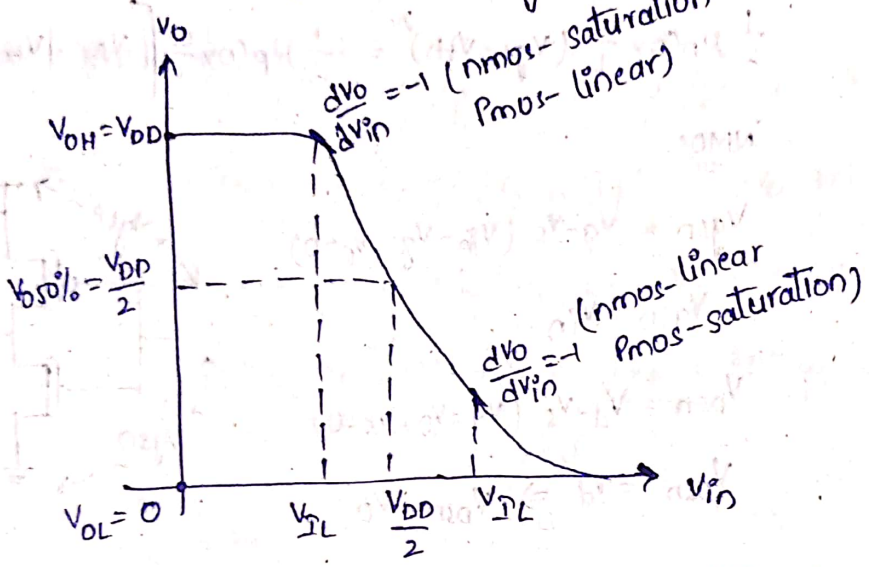
CMOS Inverter Parameters : V_{IL}, V_{IH}, V_{OL}, V_{OH}

V_{IL} : input voltage at low logic

V_{IH} : input voltage at high logic

V_{OH} : output voltage at high logic

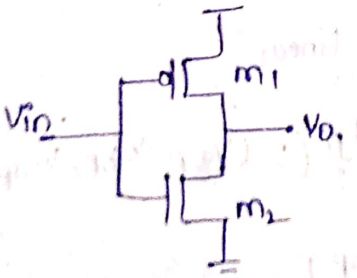
V_{OL} : output voltage at low logic



Noise margin at low level $= V_{IL} - V_{OL}$

Noise margin at high level, $NMH = V_{DD} - V_{IH}$

How much noise can be tolerated by the logic circuit - Noise margin.



Both are asymmetrical mosfets

V_{IL} Calculations:

Case (i):

$\frac{dV_o}{dV_{in}} = -1$ — nmos - saturation, Pmos - linear

V_{IL} calculations: Case (1)

I_{Dn} sat = I_{Dp} linear

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs}-V_{th})^2 = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[(V_{sg}-|V_{th}|)2V_{SD}-V_{SD}^2\right]$$

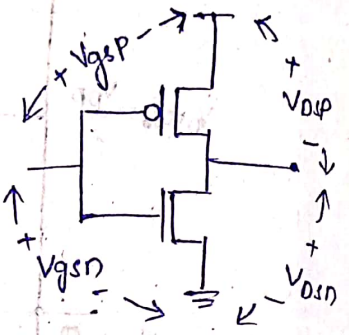
NMOS:

$V_{gsn} = V_g - V_s$ $(V_{in}=V_g, V_s=0)$

$V_{gsn} = V_{in}$

$V_{DSn} = V_d - V_s$ $(V_d=V_o, V_s=0)$

$V_{DSn} = V_d \Rightarrow V_{DSn} = V_o$



PMOS:

$V_{gsp} = V_g - V_s = V_g - V_{dd} = V_{in} - V_{dd}$ $(V_{in}=V_g, V_s=V_{dd})$

$V_{dsp} = V_d - V_s$

$= V_d - V_{dd}$

$= V_o - V_{dd}$

$\Rightarrow$ I_{Dn} sat = I_{Dp} linear

$$\frac{k_n}{2}(V_{gs}-V_{thn})^2 = \frac{k_p}{2}\left(2(V_{gsp}-V_{thp})V_{DSp}-V_{DSp}^2\right)$$

$$\frac{k_n}{2}(V_{in}-V_{thn})^2 = \frac{k_p}{2}\left(2(V_{in}-V_{DD}-V_{thp})(V_o-V_{DD})-(V_o-V_{DD})^2\right)$$

Differentiating w.r.t V_{in}.

Scanned with OKEN Scanner

$$\frac{k_n}{2}\left[2(V_{in}-V_{thn})\right] = \frac{k_p}{2}\left[2\left[(V_{in}-V_{DD}-V_{thp})\left(\frac{dV_o}{dV_{in}}\right)\right.\right.$$

$$\left.\left.+ (V_o-V_{DD})(1)\right] - 2(V_o-V_{DD})\frac{dV_o}{dV_{in}}\right]$$

$$k_n(V_{in}-V_{thn}) = k_p\left[(V_{in}-V_{DD}-V_{thp})(-1) + V_o - V_{DD} + (V_o-V_{DD})\right]$$

$$k_n(V_{in}-V_{thn}) = k_p\left[-V_{in}+V_{DD}+V_{thp}+V_o-V_{DD}+V_o-V_{DD}\right]$$

$$k_nV_{in} - k_nV_{thn} = -k_pV_{in} + k_pV_{thp} + k_pV_o + k_pV_o - k_pV_{DD}$$

$$k_nV_{in} + k_pV_{in} = k_pV_{thp} + k_nV_{thn} + 2k_pV_o - k_pV_{DD}$$

$$V_{in} = \frac{k_pV_{thp} + k_nV_{thn} + 2k_pV_o - k_pV_{DD}}{k_n + k_p}$$

$$\frac{k_n}{k_p} = k_r$$

$$V_{in} = \frac{2V_o + k_rV_{thn} - V_{DD} + V_{thp}}{1+k_r}$$

V_{IH} calculation:

$-\frac{dV_o}{dV_{in}} = -1$, nmos-linear, Pmos-saturation.

I_{Dn} linear = I_{Dp} saturation

$$\frac{k_n}{2}\left[2(V_{gsn}-V_{thn})V_{dsn} - V_{dsn}^2\right] = \frac{k_p}{2}(V_{gs_p}-V_{thp})^2$$

$$\frac{k_n}{2}\left(2(V_{in}-V_{thn})(V_o-V_{DD}) - (V_o-V_{DD})^2\right) = \frac{k_p}{2}(V_{in}-V_{thp})^2$$

Scanned with OKEN Scanner

$$\frac{k_n}{2}\left[2(V_{in}-V_{DD}-V_{thn})(V_o-V_{DD})-(V_o-V_{DD})^2\right]=\frac{k_p}{2}(V_{in}-V_{thp})^2$$

$$\frac{k_n}{2}\left[2\left[(V_{in}-V_{DD}-V_{th})\frac{dV_o}{dV_{in}}+(V_o-V_{DD})-2(V_o-V_{DD})(-1)\right]\right]$$

$$=\frac{k_p}{2}\left[2(V_{in}-V_{thp})\right]$$

$$k_n\left[V_{in}+V_{DD}+V_{th}+V_o-V_{DD}+V_o-V_{DD}\right]=k_p(V_{in}-V_{thp})$$

$$k_pV_{in}+k_nV_{in}=+k_pV_{thp}+k_nV_{th_n}+2k_nV_o-k_nV_{DD}$$

$$V_{in}=\frac{k_pV_{DD}+k_pV_{thp}+2k_nV_o+k_nV_{thn}}{k_n+k_r}$$

for symmetrical CMOS Inverter

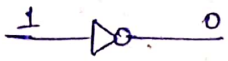
$$V_{thn}=|V_{thp}|$$

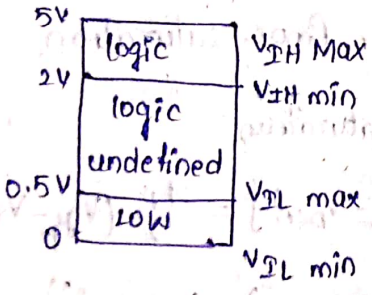
$$k_r=\frac{k_n}{k_p}=1$$

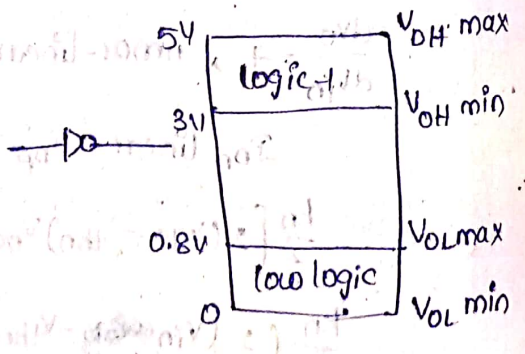
$$V_{IL}=\frac{1}{8}(3V_{DD}+2V_{th})$$

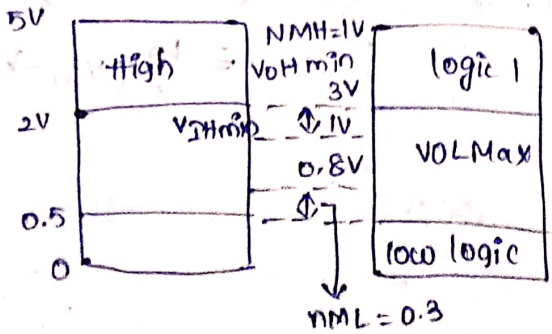
$$V_{IH}=\frac{1}{8}(5V_{DD}-3V_{th})$$

Logic gates voltage levels:









$$NMH=V_{OH}\,min-V_{IH}\,min$$

$$NML=V_{OL}\,max-V_{IL}\,min$$

Scanned with OKEN Scanner

CMOS Inverter static & dynamic power dissipation:

total power
- static power — leakage power
- Dynamic power
  - switching Power
  - Internal power

static power: in the form of leakage so called as leakage power.

Static power is the power dissipated by a transistor when it is not switching i.e., when it is static.

input is not transitioning from 0-1 or 1-0 at gate

Types:

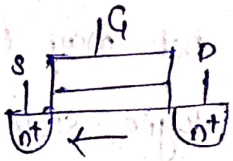
(1) Subthreshold leakage

(2) Gate leakage

(3) Junction leakage

Subthreshold leakage:

Sub-threshold leakage current is the current which flows between drain and source when $V_{gs} < V_{th}$ (for nmos), $V_{sg} < |V_{thl}|$ (Pmos).

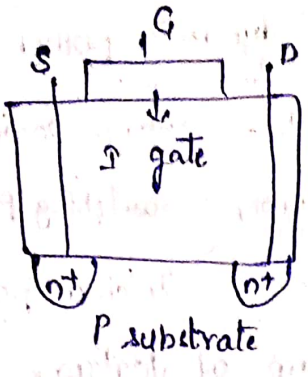


even $V_{gs} < V_{th}$, there is a small amount of current flows from drain to source, that current is called subthreshold leakage current.

Gate leakage:

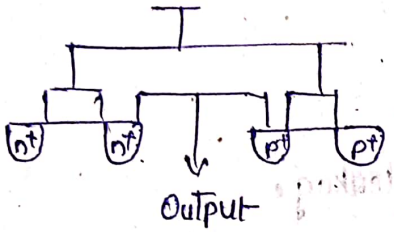
Leakage through gate is observed when gate oxide is very thin and it allows current to pass through it.

Scanned with OKEN Scanner



Junction leakage:

P-N junctions in a transistor from diodes, these diodes are reverse-biased, however reversed biased diodes still conduct a small amount of current, which causes junction leakage current



Dynamic power:

Dynamic power is the power which is dissipated when the circuit is active, and a circuit is active anytime voltage on input net changes due to some stimulus applied.

Note:

change in the voltage in input net may (or) may not lead to change in the logic state of output. But in both the cases dynamic power will be dissipated.

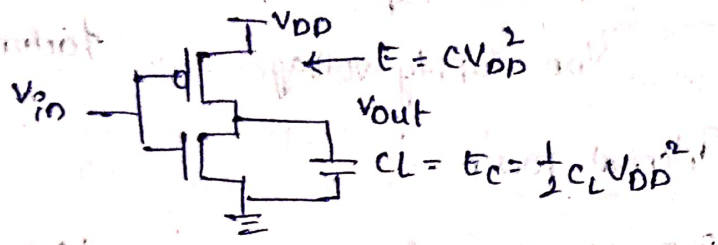
Switching power:

(change in input - change in output)

Switching power is the power dissipated while

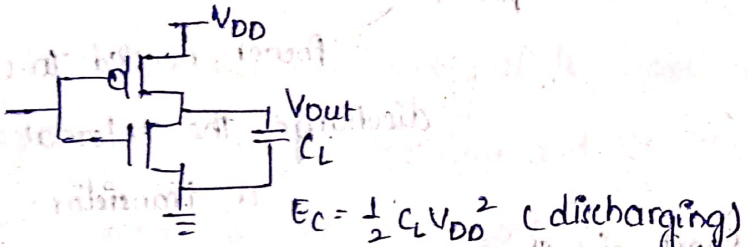
charging and discharging the load capacitor at the output of the cell.

when input switches from 1 to 0:



half of the energy is loose in the form of heat by P-mos transistors.

when input switches from 0 back to 1



Switching power equation:

* When the input switches from 1 to 0, the PMOS transistor turns ON & charges the load to V_{DD}. at that time; the energy delivered by the power supply is $E = CV_{DD}^2$

Now, the energy stored in the capacitor i.e., the energy used to change the capacitor

$$E_C = \frac{1}{2} C_L V_{DD}^2$$

Only half is dissipated as heat in the PMOS transistor.

Now, when the input switches from 0 back 1, the PMOS transistor turns off & nmos transistor turns ON, discharging the capacitor.

Scanned with OKEN Scanner

$P_{switching} = \frac{1}{2} \alpha C_L V_{DD}^2 f$. input switches 'α' times in a cycle

f = frequency

C_L = load capacitance

V_{DD} = supply voltage

Switching activity factor.

Internal power:

Internal power is any power which is dissipated within the boundary of a cell.

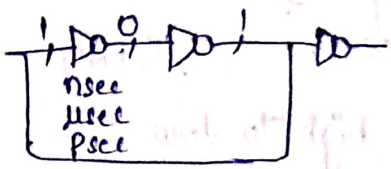
Internal power
- Short circuit power
- Power needed to charge or discharge the internal nodes of a transistor.

Short circuit power:

Short circuit power is the power dissipated when both PMOS & NMOS are on simultaneously during input transition.

Propagation delay in CMOS Inverter:

* Propagation delay is in Nanoseconds for CMOS circuits.



N: no. of not gates

t_{pd}: Propagation time delay

$$f_{max} = \frac{1}{2Nt_{pd}}$$

* free running oscillator (or) ring oscillator

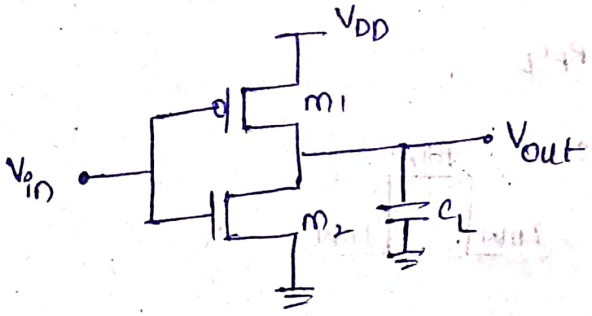
* Propagation delay:

The time it takes for a signal to travel (or) Propagating through a medium and it be received after it has been sent.

(or)

The time taken by a gate (or) logic circuit Propagating an input signal to the output of the gate is called propagation delay.

*



C_L: load Capacitor

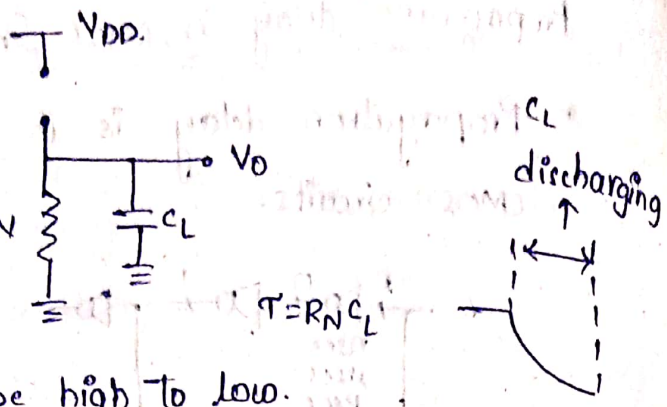
Case ①:

Input signal is 1 (low to high)



M_1 – off

M_2 – ON.



Output will be high to low.

Capacitor is discharging via NMOSFET.

Case (2):

* i/p signal is from high to low.

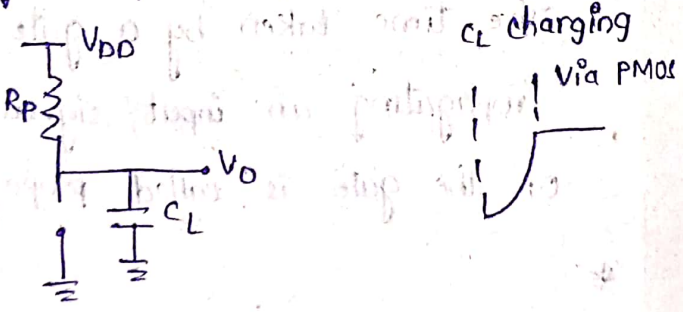
$V_{in} = 0$

O/p will be low to high

Here M_1 – ON

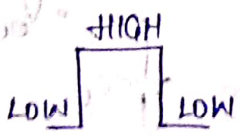
M_2 – OFF

* C_L charging via pmos upto V_{DD}

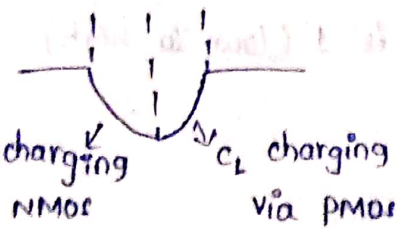


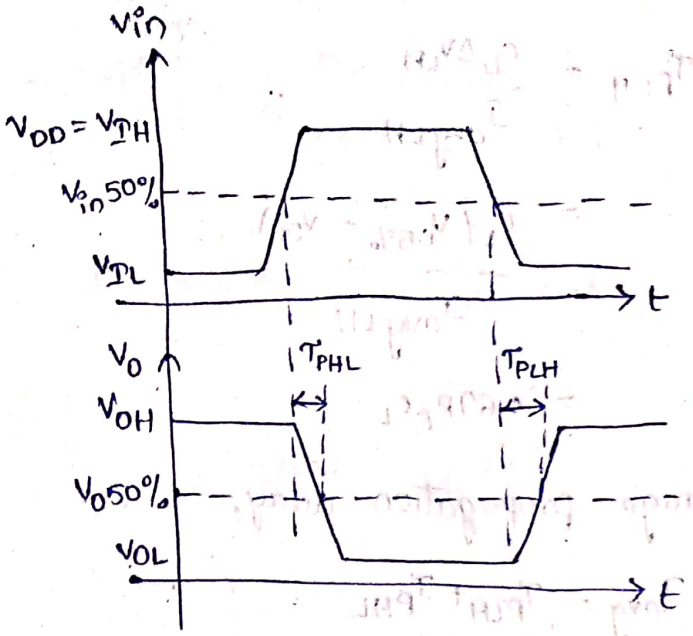
$\tau = R_P C_L$

Input signal:



o/p signal:





$$\tau_{avg} = \frac{\tau_{PLH} + \tau_{PHL}}{2}$$

How to minimise the propagation delay

(1) By decreasing the load capacitance, so that minimizing the size of the integrated circuit.

(2) By increasing width of MOS transistor. It is known as gate sizing.

(3) full voltage swing, V_{OL} is ground, V_{OH} is V_{DD}.

Note:

* Propagation delay from high to low,

$$\tau_{PHL} = \frac{C_L \Delta V_{HL}}{I_{avg\,HL}}$$

$$= \frac{C_L (V_{OH} - V_{050\%})}{I_{avg\,HL}}$$

$$= 0.69 R_N C_L$$

$$R_N = \frac{12.5}{\left(\frac{W}{L}\right)_N}$$

$$R_P = \frac{30}{\left(\frac{W}{L}\right)_P}$$

Scanned with OKEN Scanner

* $\tau_{PLH} = \frac{C_L \Delta V_{LH}}{I_{avg\,LH}}$

$= \frac{C_L (V_{05\%} - V_{OL})}{I_{avg\,LH}}$

$= 0.69 R_p C_L$

* Average propagation delay,

$\tau_{avg} = \frac{\tau_{PLH} + \tau_{PHL}}{2}$

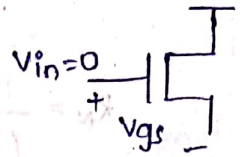
$f_{max} = \frac{1}{2 \tau_{avg\,pd}}$

Pass transistors: logic:

It helps in reducing no.of transistors.

* In CMOS inverters, Nand gate can be realised using 4 transistors but using pass transistor logic, it can be realised using only 2 transistors.

*

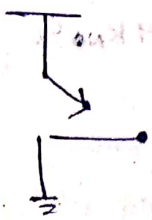


$\simeq$ $V_{gs} < V_{th}$

then NMOS - off (0.c)

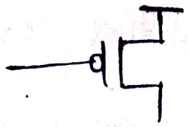
$V_0 = V_{DD}$.

NMOS strongly passes low signals.



if $V_{in} = 1 \Rightarrow V_0 = 0V$

Scanned with OKEN Scanner

* 

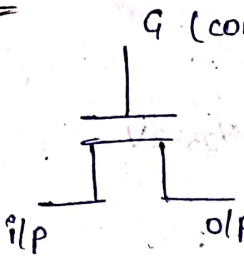
$V_{gs} > V_{th}$ ..

PMOS - OFF (O.C)

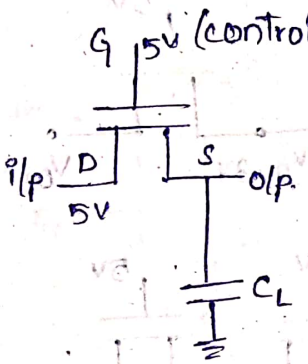
$V_O = 5V$

if $V_{gs} < V_{th} \Rightarrow$ PMOS (S.C) $V_O = 0V$

* Case ①:



Apply voltages.



$V_{th} = 1V$

o/p voltage $= V_g - V_{th}$

$= 5 - 1$

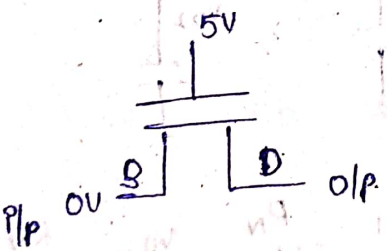
$= 4V$

NMOS also passes weak logic "1".

So here C_L charges.

Because here V_{in} is logic 1 and o/p is 4V.

Case ②:



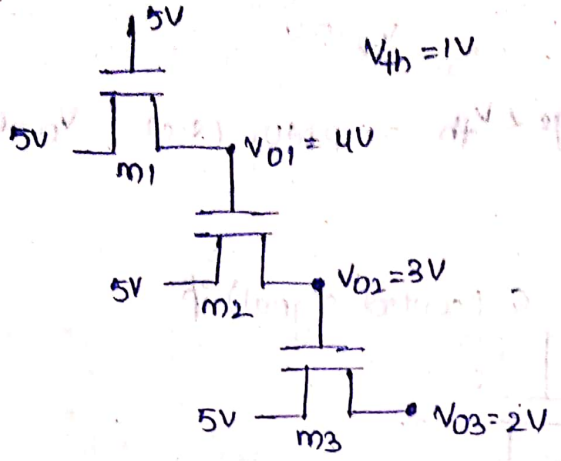
NMOS can strongly pass logic "0".

∴ o/p = logic "HIGH".

$= V_g - V_{th} = 4V$

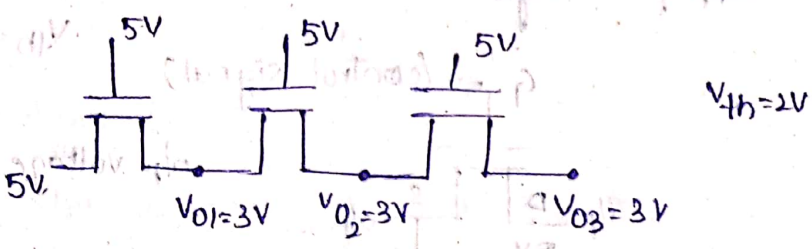
$V_0 = \min(V_D, V_{gs} - V_{th})$

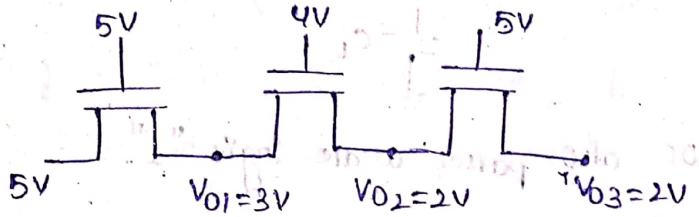
Q)



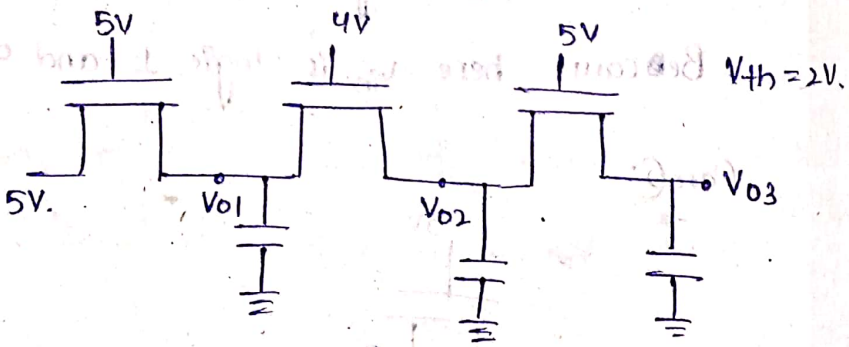
Parallel Pass transistor

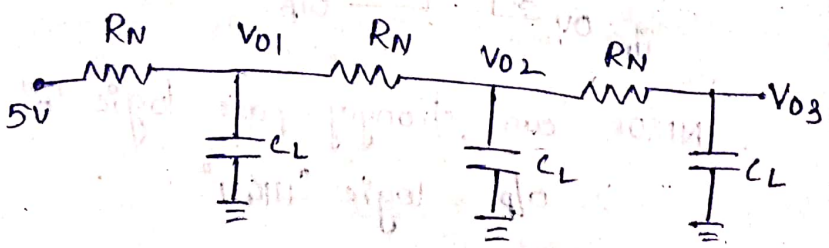
Q) Series Pass transistor





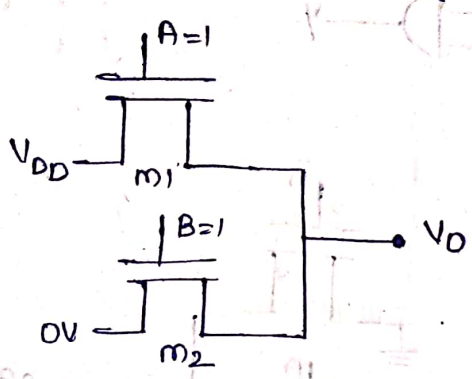
*



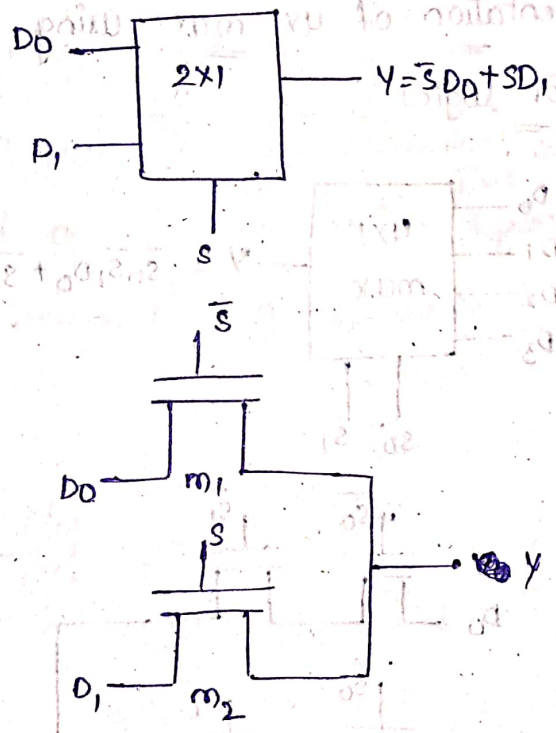


Sneak path: (Drawback of Pass transistor logic)

If Both the NMOS are ON, then entire i/p goes to ground ⇒ Sneak path.



Implementation of 2x1 mux using pass transistor logic:



if $S=0 \Rightarrow V_O = D_0$ [M1-ON ; M2-OFF]

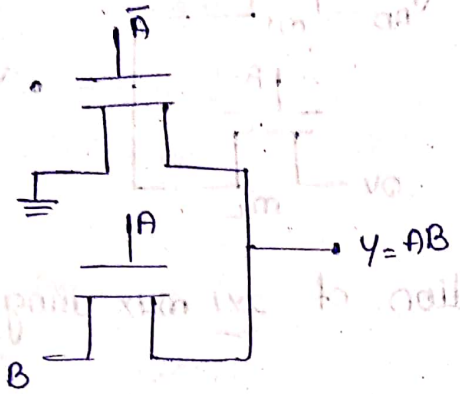
if $S=1 \Rightarrow V_O = D_1$ [M1-OFF ; M_2-ON]

Scanned with OKEN Scanner

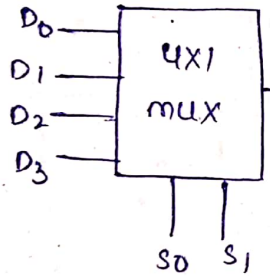
Implementation of AND gate using pass transistor logic:

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

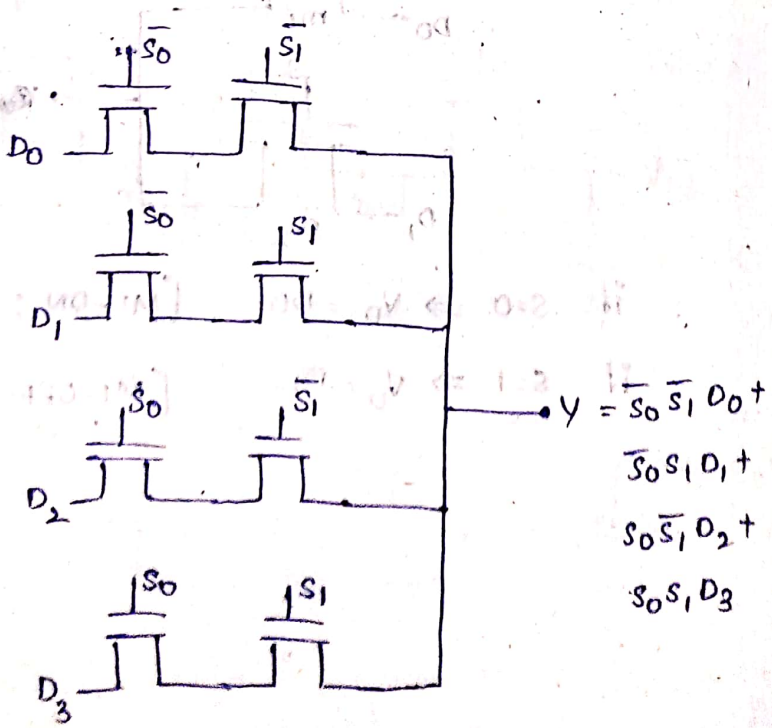


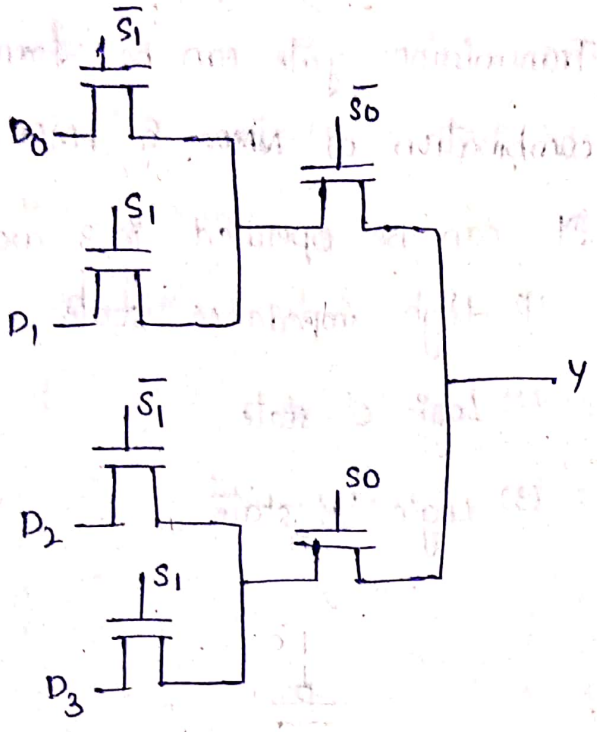


Implementation of 4x1 mux using pass transistor logic:



$$Y = \bar{S_0}\bar{S_1}D_0 + \bar{S_0}S_1D_1 + S_0\bar{S_1}D_2 + S_0S_1D_3$$



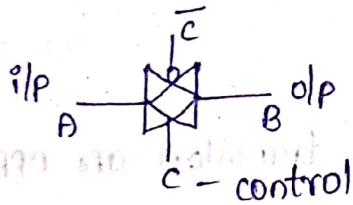


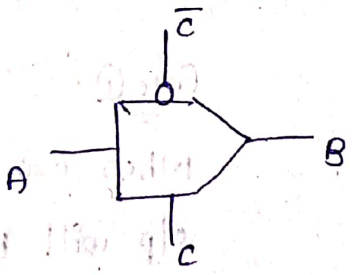
Transmission gates:

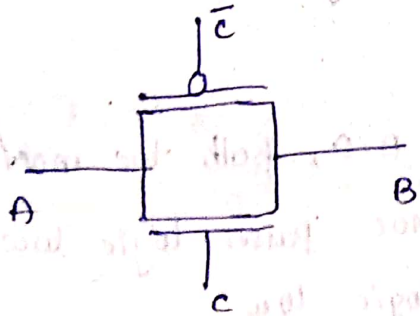
Reduce the no.of gates.

Transmission gates is non-mechanical delay. It consists of one i/p two control i/ps, one o/p.

By using transmission gates, we can reduce no.of gates.





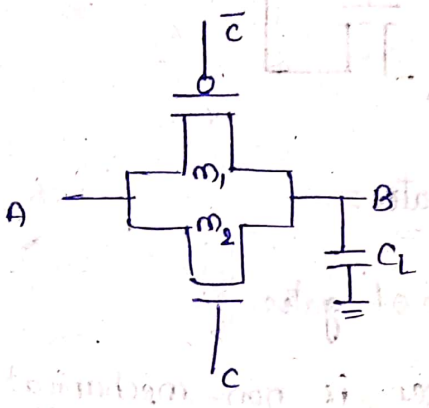


Scanned with OKEN Scanner

* Transmission gate can be formed parallel combination of NMOS & PMOS.

* It can be operated in 3 modes/states
  (1) High impedance state
  (2) Logic '0' state
  (3) Logic '1' state

*



C	A	B	
0	0		High impedance state
0	1		High impedance state
1	0		logic-0
1	1		logic-1

Case (1):

When C=0, both the transistors are off (O.C). O/p will be in high impedance state.

Case (2):

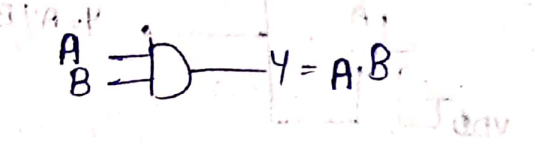
when C=1 and A=0, Both the mosfets are ON. As NMOS passes logic low, O/p will be logic low.

Case (3):

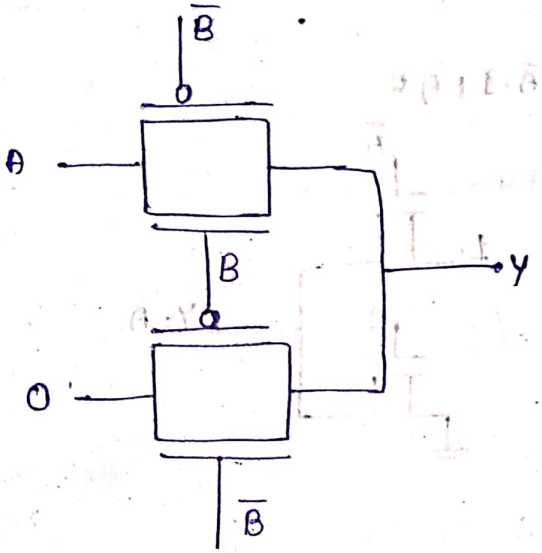
When C=1 and A=1, Both the transistors are ON. PMOS strongly passes logic 1. Therefore o/p will be logic "HIGH".

Realization of AND Gate using transmission gates:

No. of transmission gates required = no. of i/ps



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



Case (1): If B=0,

transmission gate 1 is off, 2 is ON.

Therefore o/p will be zero (based on above ckt)

Case (2): If B=1

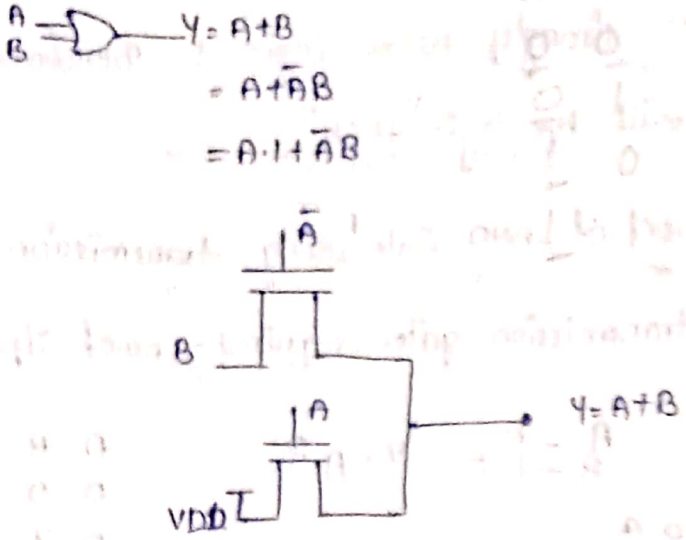
transmission gate 1 is ON

o/p = A.

Scanned with OKEN Scanner

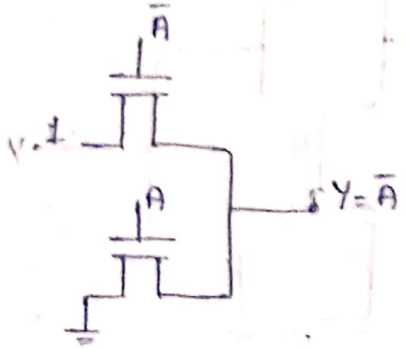
Using Pass transistor logic:

OR Gate:



NOT Gate:

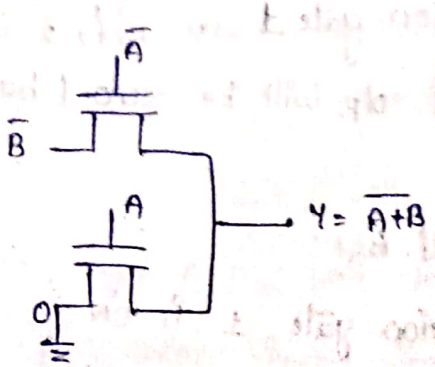
$Y = \bar{A} \cdot 1 + A \cdot 0$



NOR Gate:

$Y = \overline{A+B}$

$= \bar{A} \cdot \bar{B} + A \cdot 0$

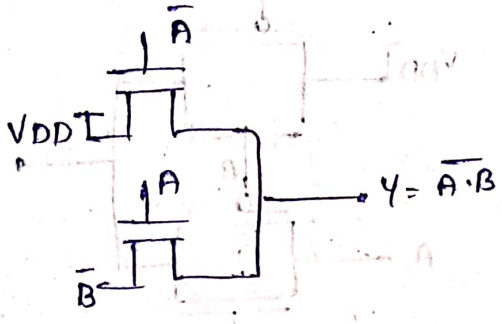


Scanned with OKEN Scanner

NAND Gate:

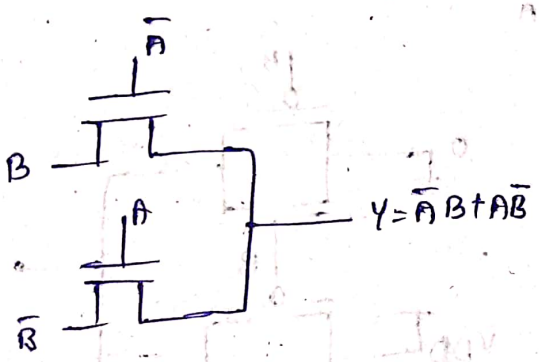
$Y = \overline{A \cdot B} = \bar{A} + \bar{B}$

$= \bar{A} + A\bar{B} = \bar{A} \cdot 1 + A\bar{B}$



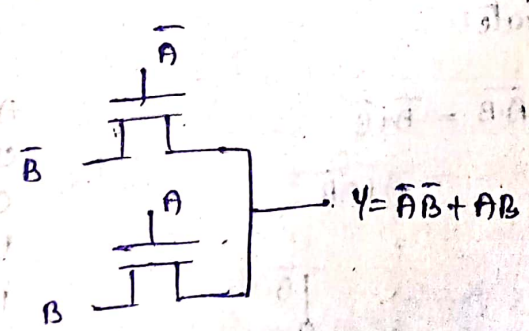
XOR Gate:

$Y = \bar{A}B + A\bar{B}$



XNOR Gate:

$Y = \bar{A}\bar{B} + AB$



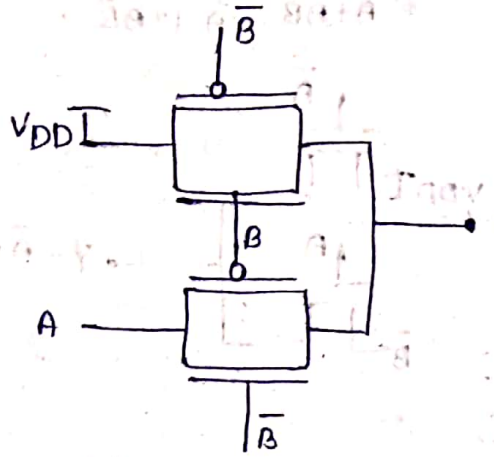
Scanned with OKEN Scanner

Using transmission gates:

OR Gate:

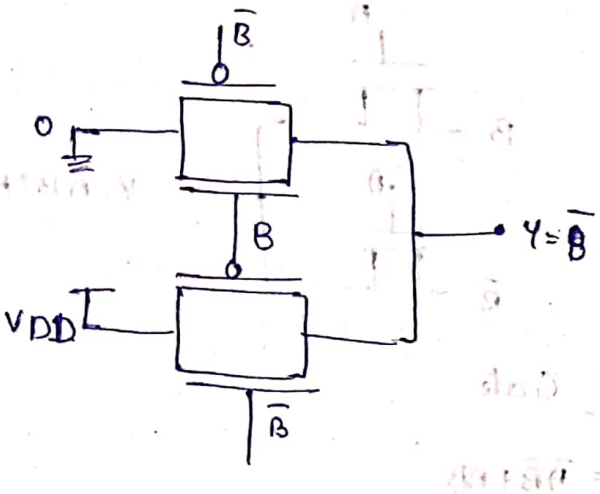
$Y = A + B$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



NOT Gate:

$Y = \bar{A}$

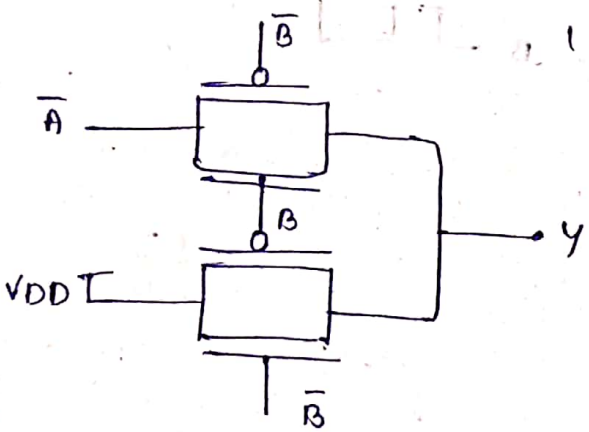


NAND Gate:

$Y = \overline{A \cdot B} = \bar{A} + \bar{B}$

$= \bar{A} + A\bar{B}$

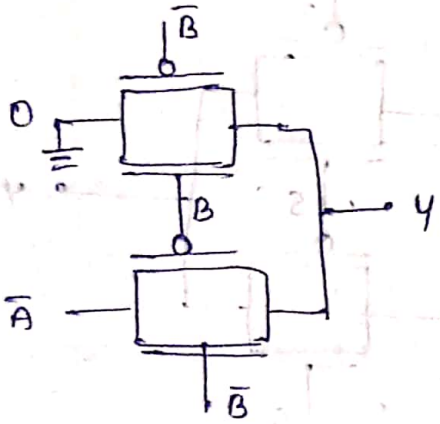
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



Scanned with OKEN Scanner

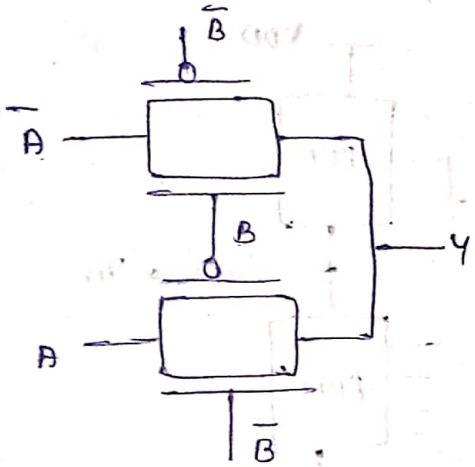
NOR Gate:

$Y = \overline{A+B}$



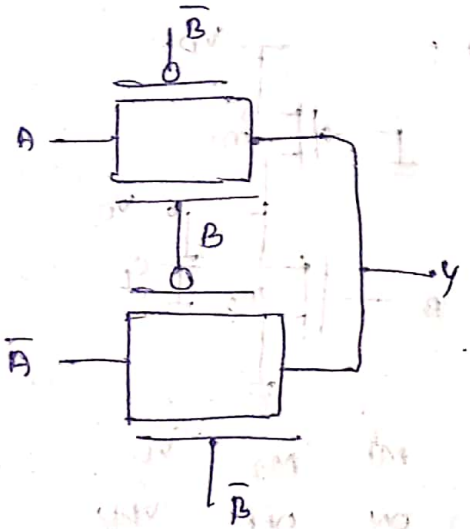
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

XOR Gate:



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

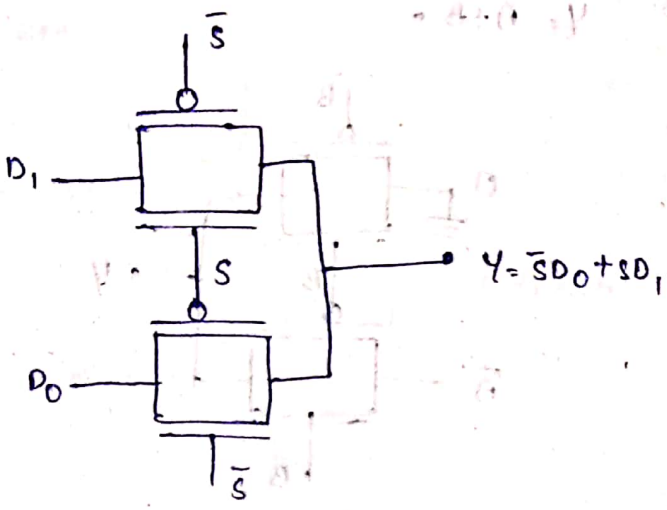
XNOR Gate:



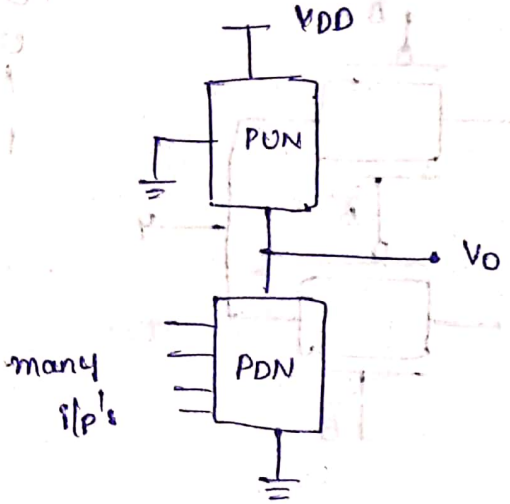
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Scanned with OKEN Scanner

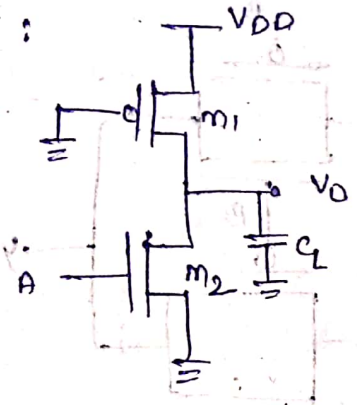
2x1 mux:



Pseudo NMOS:



Inverter:



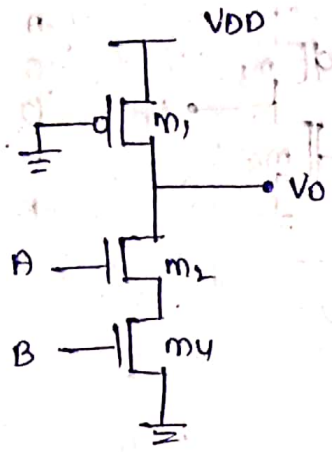
A	M1	M2	V_O
0	ON	OFF	VDD
1	ON	ON	$V_D = V_{DD} \times \frac{R_N}{R_N + R_P}$

↓

Bad logic

Scanned with OKEN Scanner

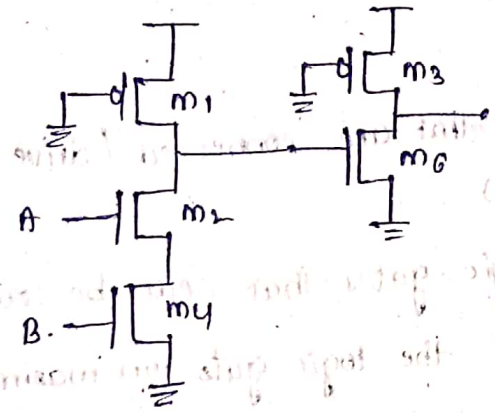
NAND Gate:



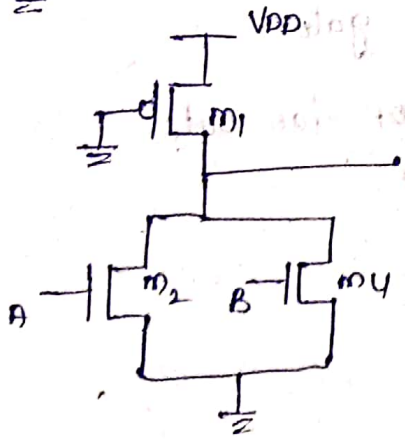
A	B	Vo
0	0	1
0	1	1
1	0	1
1	1	0

A	B	m_1	m_2	m_4	Vo
0	0	ON	OFF	OFF	VDD = 1
0	1	ON	OFF	ON	VDD = 1
1	0	ON	ON	OFF	VDD = 1
1	1	ON	ON	ON	0

AND Gate:



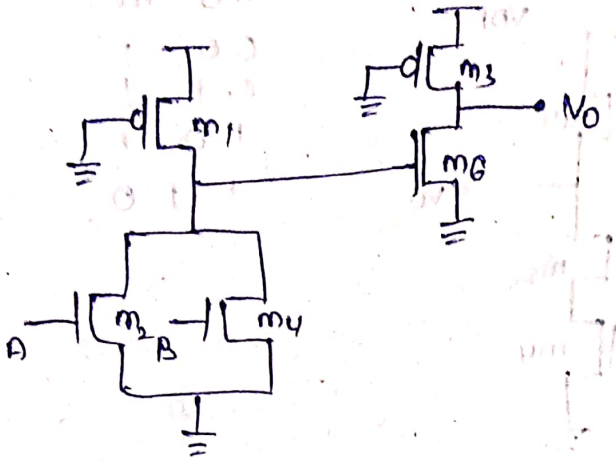
NOR Gate:



A	B	Vo
0	0	VDD
0	1	0
1	0	0
1	1	0

Scanned with OKEN Scanner

OR Gate:

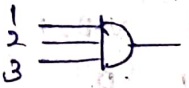


A	B	V_O
0	0	0
0	1	V_{DD}
1	0	V_{DD}
1	1	V_{DD}

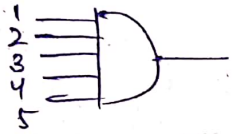
Fan in & fan out:

Fan in:

no. of inputs driven by the logic gate.



fan in = 3



fan in = 5

fan out:

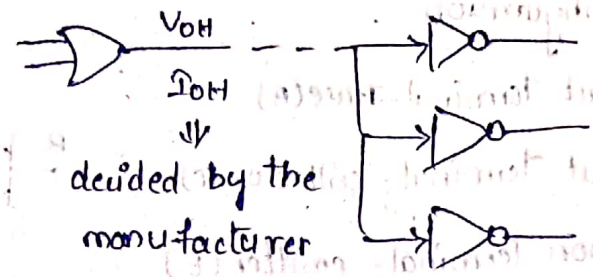
no. of outputs that are connected / drive by the logic circuit (or)

no. of logic gates that can be connected at the output of the logic gate (or) maximum no. of logic gate inputs that can be connected to the output of the logic gate.

There are 2 types of fan outs:

① high state fanout

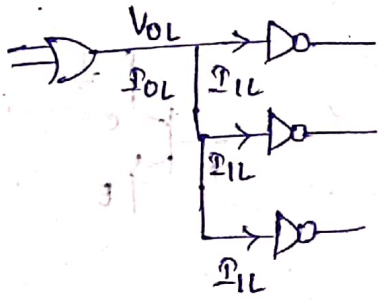
② Low state fanout



High state fanout = $\frac{(I_{OH})_{max}}{I_{IH}}$

Low state fanout:

$$\frac{(I_{OL})_{max}}{I_{IL}}$$



Q. Let us consider a $(I_{OH})_{max} = 1mA$ & $I_{IH} = 0.1mA$. Find high state fanout?

High state fanout = $\frac{1mA}{0.1mA} = 10$

Q. $(I_{OL})_{max} = 4mA$ & $I_{IL} = 0.2mA$ low state fanout

Low state fanout = $\frac{4mA}{0.2mA} = \frac{4 \times 10}{2} = 20$

fan out = min (fanout (high), fanout (low))

Scanned with OKEN Scanner

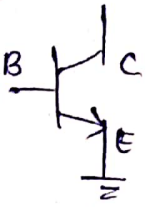
Bipolar junction transistor

CE configuration:

input terminal - Base(B)

Output terminal - collector (C)

common terminal - emitter (E)

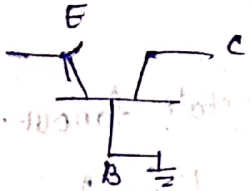


CB configuration:

i/p - emitter

o/p - collector

common - Base

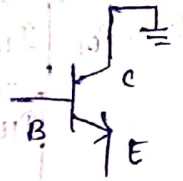


CC configuration

i/p - Base

o/p - emitter

common - collector

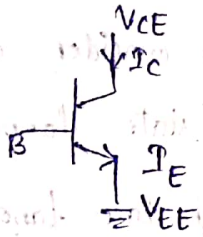


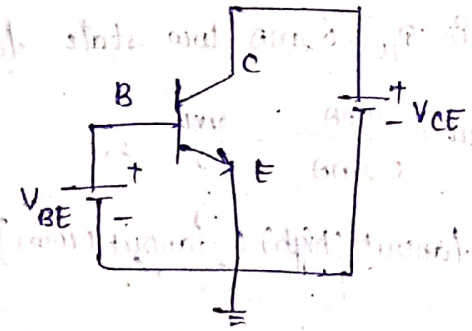
CE configuration:

i/p Parameters - V_{BE}, I_b

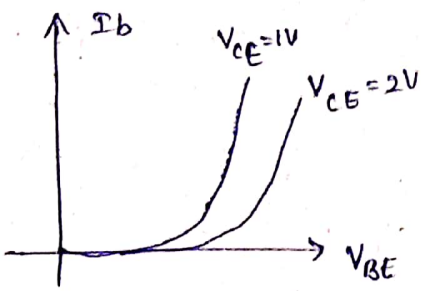
o/p Parameters - V_{CE}, I_c

$$I_e = I_c + I_b$$

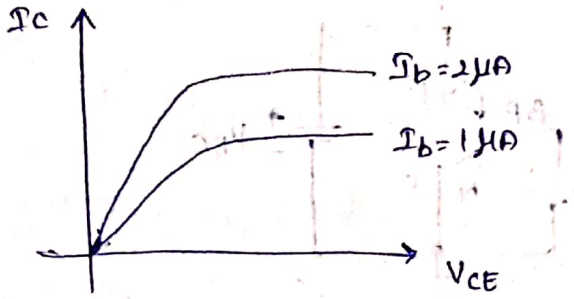




I/p characteristics



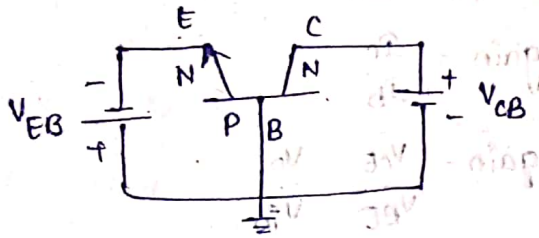
o/p characteristics :



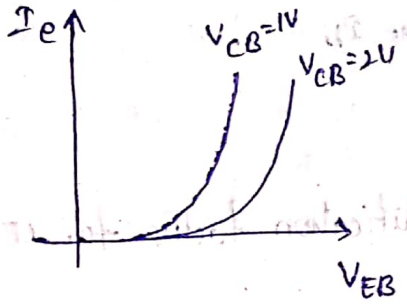
CB configuration :

i/p Parameters - V_{BE}, I_e

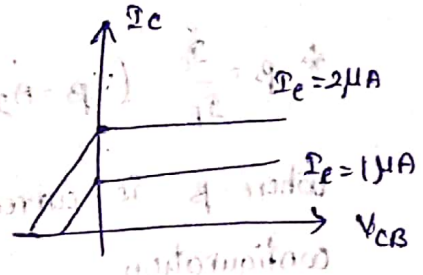
o/p Parameters - V_{CB}, I_C



i/p characteristics :



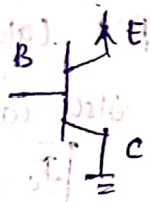
o/p characteristics :



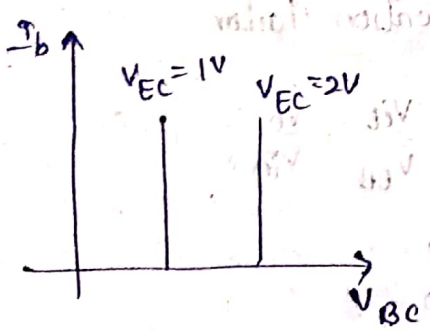
common collector configuration :

i/p parameters - V_{BC}, I_b

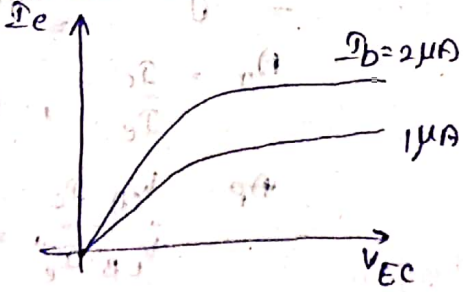
o/p parameters - V_{EC}, I_e



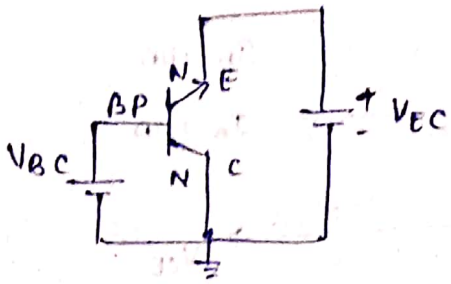
i/p characteristics



o/p characteristics



Scanned with OKEN Scanner



CE configuration amplification factor:

$$I_e = I_c + I_b$$

A = Gain = $\frac{\text{Output Parameter}}{\text{Input Parameter}}$

A_I = current gain = $\frac{I_c}{I_b}$

A_V = voltage gain = $\frac{V_{CE}}{V_{BE}} = \frac{V_o}{V_{in}}$

A_P = Power gain = $\frac{P_o}{P_{in}} = \frac{V_{CE} \cdot I_c}{V_{BE} \cdot I_b}$

* $\beta = \frac{I_c}{I_b}$ $\left(\because \beta = A_I = \frac{I_c}{I_b}\right)$

where β is current amplification factor for CE configuration.

Range of β: 50-200

* $\beta > 1$ (always)

* β also called as hfe.

$$\boxed{I_c = \beta I_b}$$

CB configuration amplification factor:

$$A_I = \frac{I_c}{I_e}, \quad A_V = \frac{V_{CE}}{V_{EB}} = \frac{V_o}{V_{in}}$$

$$A_P = \frac{V_{CB} \cdot I_c}{V_{EB} \cdot I_e} = \frac{P_o}{P_{in}}$$

$$\alpha = \frac{I_c}{I_e} \Rightarrow \boxed{I_c = \alpha I_e}$$

Scanned with OKEN Scanner

where α is current amplification factor of CB configuration.

$\alpha < 1$ (always)

CC configuration = amplification factor:

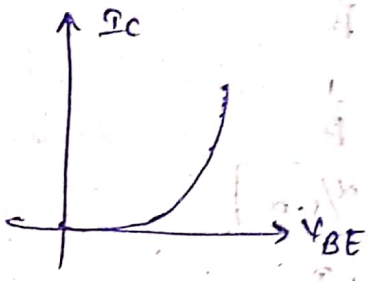
$$A_I = \frac{I_e}{I_b}$$

$$A_V = \frac{V_{EC}}{V_{BC}} = \frac{V_o}{V_{in}}, \quad A_P = \frac{V_{EC} \cdot I_e}{V_{BC} \cdot I_b} = \frac{P_o}{P_{in}}$$

$$\gamma = \frac{I_e}{I_b} \Rightarrow \boxed{I_e = \gamma I_b} \quad \gamma = 1$$

where γ is current amplification factor of CC configuration.

* If V_{BE} ↑ then I_C also increases.
* V_{BE} must be greater than 0.7V to get into the conduction mode.



$$I_c = I_s \left(e^{\frac{V_{BE}}{V_T}} - 1 \right)$$

we have $I_c = \beta I_b$

from ① & ②,

$$I_b = \frac{I_s}{\beta} \left(e^{\frac{V_{BE}}{V_T}} - 1 \right)$$

Scanned with OKEN Scanner

Relation between α, β, γ:

CE configuration $\Rightarrow \beta = \frac{I_C}{I_B}$, $I_C = \beta I_B$

↓

DC gain

CB configuration $\Rightarrow \alpha = \frac{I_C}{I_E} \Rightarrow I_C = \alpha I_E$

CC configuration $\Rightarrow \gamma = \frac{I_E}{I_b} \Rightarrow I_E = \gamma I_b$

WKT $I_E = I_C + I_b$

$$\frac{I_E}{I_C} = 1 + \frac{I_b}{I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\frac{1}{\alpha} = \frac{\beta+1}{\beta}$$

$$\boxed{\alpha = \frac{\beta}{1+\beta}}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\frac{1}{\alpha} - 1 = \frac{1}{\beta}$$

$$\frac{1-\alpha}{\alpha} = \frac{1}{\beta}$$

$$\boxed{\beta = \alpha/1-\alpha}$$

$$I_E = I_C + I_b$$

$$\frac{I_E}{I_b} = \frac{I_C}{I_b} + 1$$

$$\gamma = \beta + 1$$

$$\beta = \gamma - 1$$

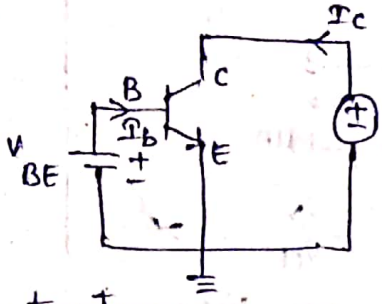
$$\gamma = \beta + 1$$

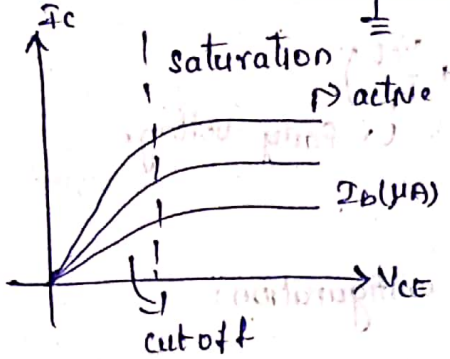
$$= 1 + \frac{\alpha}{1-\alpha}$$

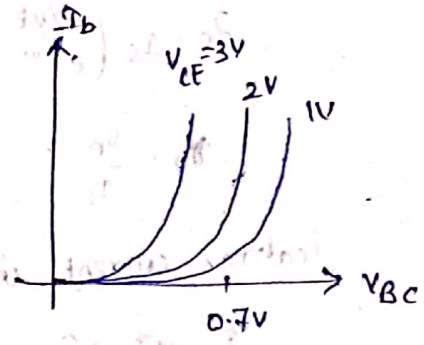
$$\gamma = \frac{1}{1-\alpha} = 1+\beta$$

Scanned with OKEN Scanner

Early effect (or) Base width modulation:

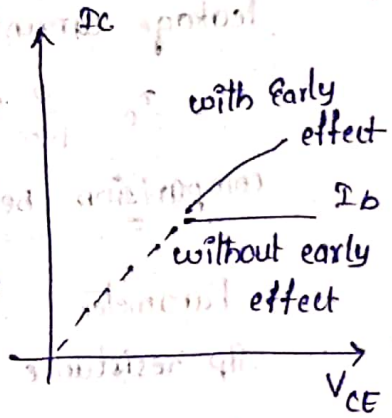


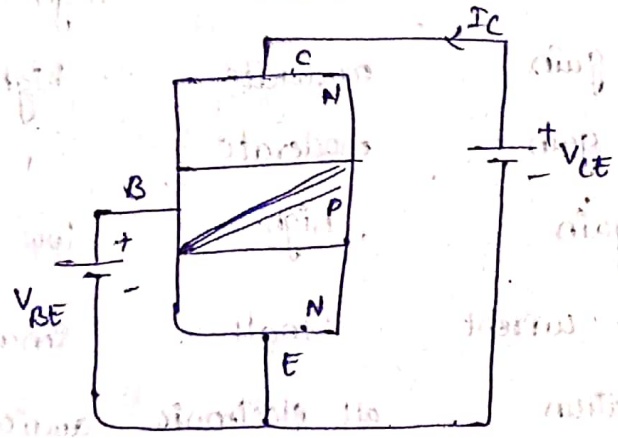




As we increase the V_{CE} the transistor comes to the on state before than its maximum cut in voltage (0.7V).

* In reverse bias, we get constant graph that means it is without early effect.
* By increasing reverse voltage, the graph changes & that is with early effect.

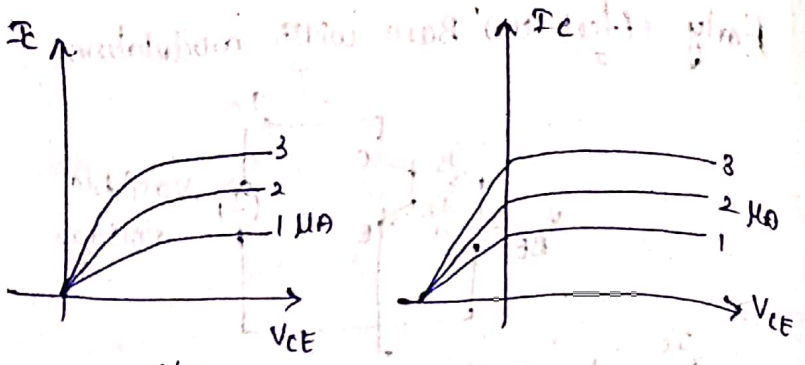




$$I_C = I_S \left(e^{\frac{V_{BE}}{V_T}} - 1 \right)$$

$$I_S = \frac{A q n_i^2 D_n}{N_B W_0}$$

↳ effective base width



$$I_C = I_S \left(e^{\frac{V_{BE}}{V_T}} - 1\right)\left(1 + \frac{V_{CE}}{V_A}\right)$$

↳ Early voltage

$$r_o = \frac{V_A}{I_C}$$

Leakage current in CB configuration:

$$I_C = \alpha I_E + I_{CBO}$$

↳ collector to base current when emitter is open circuited.

Leakage current in CE configuration:

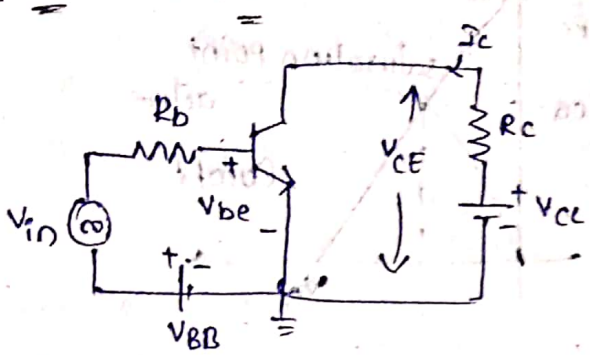
$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

Comparision between CE, CB & CC:

Parameter	CE	CB	CC
i/p resistance	1kΩ - 100kΩ	low - 100Ω	High - 1MΩ
o/p resistance	≃ 10kΩ	High - 1MΩ	low - 100Ω
Voltage gain	moderate	high	1
Current gain	moderate	1	high
Power gain	high	low	medium
leakage current	Small	Small	high
application	all electronic devices	audio frequency	impedance matching
phase shift	180° out of phase	0°	0°

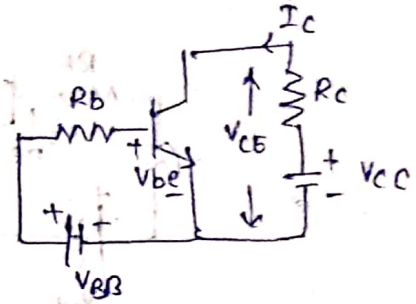
Biasing of BJT:

concept of DC load line:



DC analysis:

all ac components are zero



apply KVL for i/p loop;

$$-V_{BB} + R_b I_b + V_{be} = 0$$

$$I_b = \frac{V_{BB} - V_{be}}{R_b}$$

$$I_b = \left(\frac{-1}{R_b}\right) V_{be} + \left(\frac{1}{R_b}\right) V_{bb} \quad -(1)$$

$$y = mx + c$$

apply KVL for o/p loop,

$$-V_{cc} + I_c R_c + V_{ce} = 0$$

$$I_c = \frac{V_{cc} - V_{ce}}{R_c}$$

$$I_c = \left(\frac{-1}{R_c}\right) V_{ce} + \frac{1}{R_c} V_{cc} \quad -(2)$$

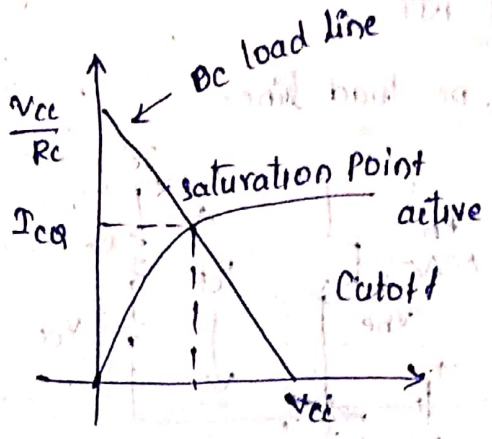
Case (1): $I_c = 0$

$V_{cc} = V_{ce}$

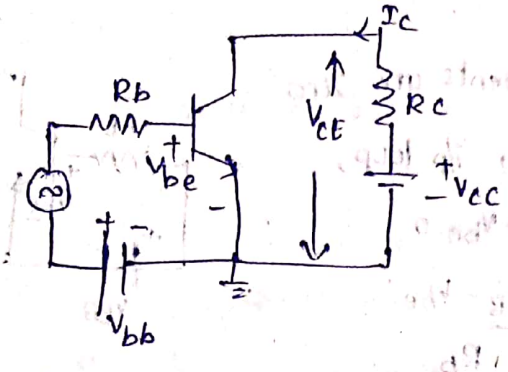
Case (2): $V_{ce} = 0$

$$I_c = \frac{V_{cc}}{R_c}$$

Scanned with OKEN Scanner

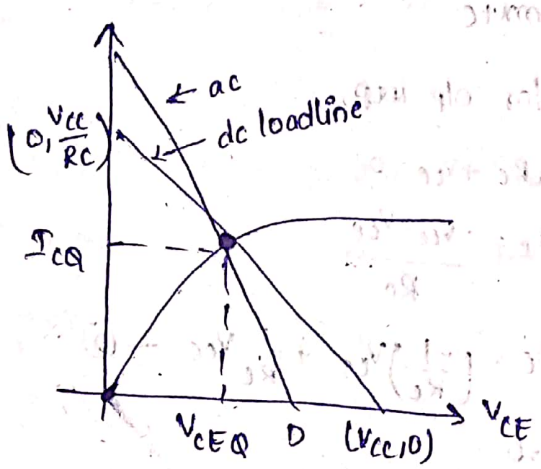


Dc input:



Ac loadline:

all dc components are zero.



$$V_{CE} = V_{CEQ} + I_c R_c$$

$$V_{CE} = V_{CEQ} + I_c R_c$$

$$I_c = I_{CQ} + \frac{V_{CE}}{R_c}$$

$$S = \frac{1+\beta}{1-\beta \frac{\partial I_b}{\partial I_c}}$$

Scanned with OKEN Scanner

Small Signal analysis of BJT:

Current Equation:

$$I_C = I_S\left(e^{\frac{V_{BE}}{V_T}} - 1\right) \approx I_S e^{\frac{V_{BE}}{V_T}}$$

$\Rightarrow I_S$ is very less

I_S: Saturation (or) minority charge carrier (or) reverse saturation current.

* $\beta = \frac{I_C}{I_b}$ $\quad \beta > 1$

  $\alpha = \frac{I_C}{I_e}$ $\quad \alpha < 1$

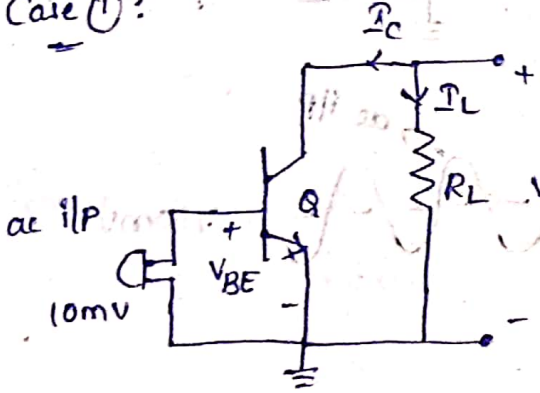
  $\gamma = \frac{I_e}{I_b}$ $\quad \gamma$

* Other names for cc is Emitter follower, Voltage follower, buffer, high input impedance to low input impedance, unity voltage gain

* $I_C = I_S e^{\frac{V_{BE}}{V_T}}$

  $V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$

* Case (1):



$I_C + I_L = 0$

$I_C = -I_L$

$I_C = -\frac{V_o}{R_L}$

$V_o = 100mV$

$V_o = -I_C R_L$

$I_S = 5 \times 10^{-6}$ A

we know that

$$I_C = I_S\left(e^{\frac{V_{BE}}{V_T}} - 1\right)$$

Scanned with OKEN Scanner

$V_O = -I_C R_L$

$100mV = -I_C R_L$

$I_C = I_S \left(e^{\frac{V_{BE}}{V_T}} - 1 \right)$

$= 5 \times 10^{-16} \left(e^{\frac{100mV}{26mV}} - 1 \right)$

$I_C = 2.35 \times 10^{-16}\ A$

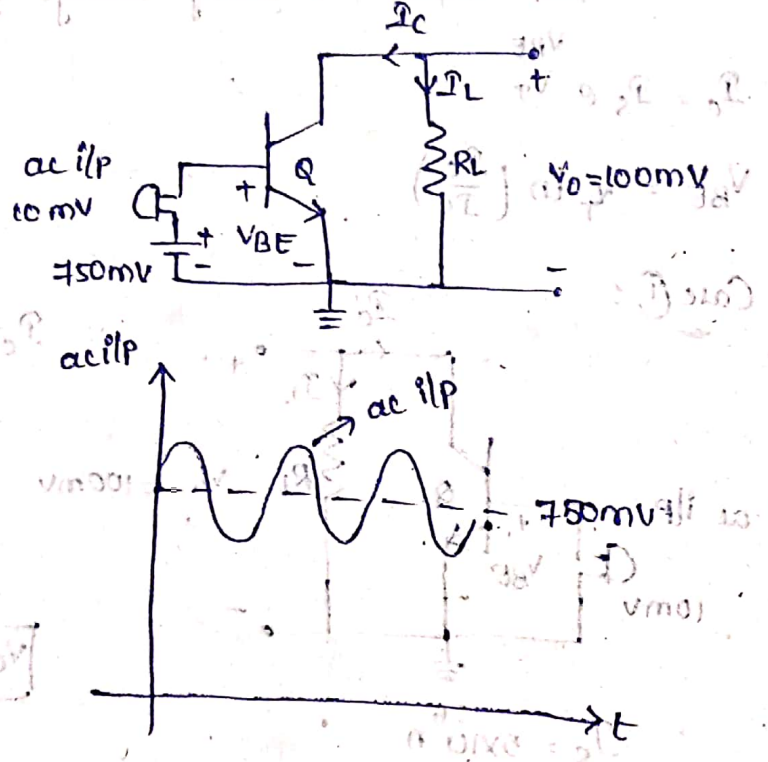
$R_L = \frac{-V_O}{I_C}$

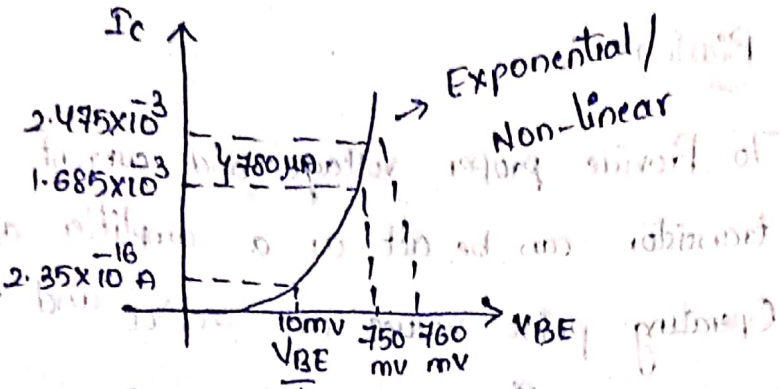
$= \frac{-100mV}{2.35 \times 10^{-16}}$

$R_L = 4.25 \times 10^{14}\ \Omega$

Only using ac voltage, didn't amplify input accurately due to high load resistance.

Case ②:





$$I_C = I_S\, e^{\frac{V_{BE}}{V_T}}$$

Consider ac i/p = 0

$\therefore V_{BE} = 750\,mV$

$$I_C = I_S\left(e^{\frac{V_{BE}}{V_T}} - 1\right)$$

$I_C = 1.685\,mA$

$V_O = -I_C R_L$

$R_L = 59.34\,\Omega$

Now consider both ac and dc inputs:

$\therefore V_{BE} = 760\,mV$:

$I_C = 2.475\,mA$

$R_L = 40.4\,\Omega$

with difference $\Rightarrow R_L = \frac{V_O}{I_C}$

$= \frac{100\,mV}{780\,\mu A} \approx 129\,\Omega$

To increase collector current, every circuit must have biasing voltage otherwise amplification doesn't occur.

Scanned with OKEN Scanner

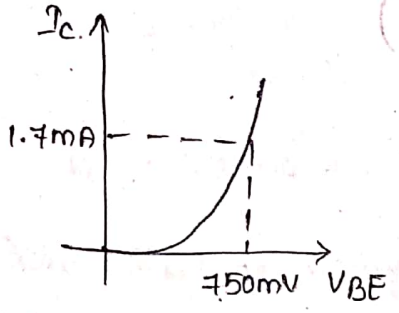
Biasing

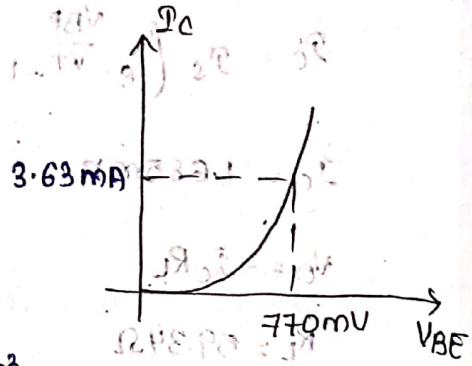
To Provide proper voltage and current so that transistor can be act as a amplifier application.

Operating point values are I_C, V_{CE} and V_{BE}

Q ②

which operating point curve is better among those two curves.





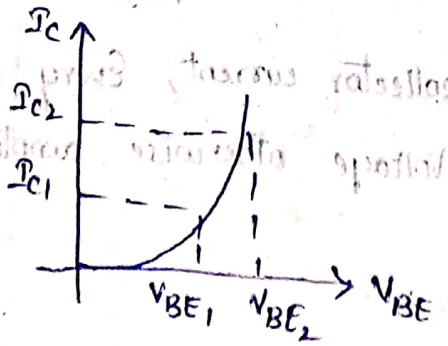
$$I_C = 5\times10^{-16}\left(e^{\frac{770\times10^{-3}}{26\times10^{-3}}}-1\right)$$

$$= 3.63 \text{ mA}$$

slope for second graph is more compared to first curve. Second graph is better.

Concept of transconductance (g_m):

slope is nothing but g_m



$$g_m = \frac{\Delta I_C}{\Delta V_{BE}} = \frac{I_C}{V_{BE}} = \frac{\partial I_C}{\partial V_{BE}}$$

$$I_c = I_S e^{\frac{V_{BE}}{V_T}}$$

$$\frac{\partial I_c}{\partial V_{BE}} = I_S e^{\frac{V_{BE}}{V_T}} \cdot \frac{1}{V_T}$$

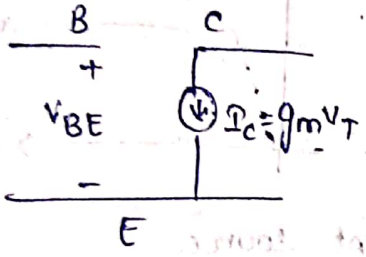
$$\frac{\partial I_c}{\partial V_{BE}} = \frac{I_c}{V_T}$$

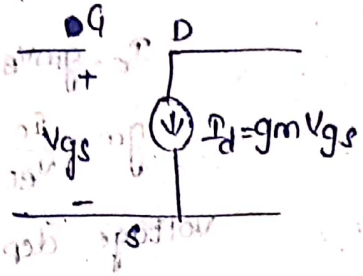
$$g_m = \frac{I_c}{V_T} \Rightarrow I_c = g_m V_T$$

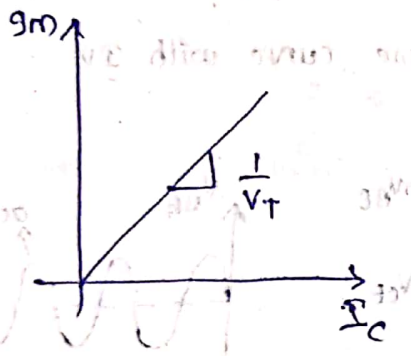
In MOSFET,

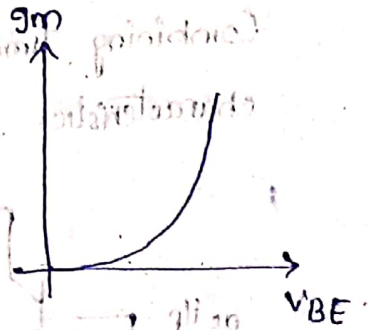
$$g_m = \frac{I_d}{V_{gs}}$$

$$I_d = g_m V_{gs}$$





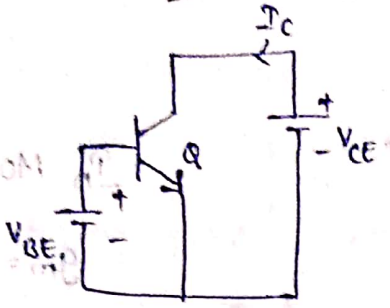


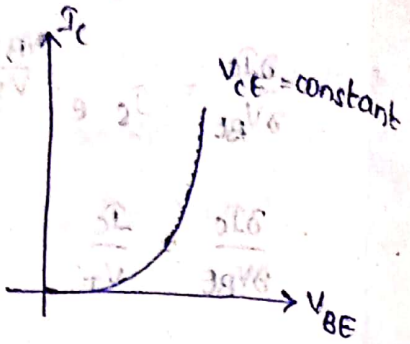


$$g_m = \frac{I_c}{V_T}$$

$$\frac{g_m}{I_c} = \frac{1}{V_T}$$

I/V characteristics of BJT :-



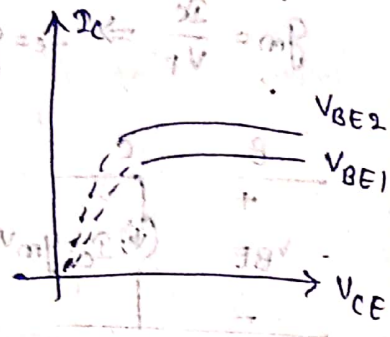


$$I_C = I_S e^{\frac{V_{BE}}{V_T}}$$

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$$

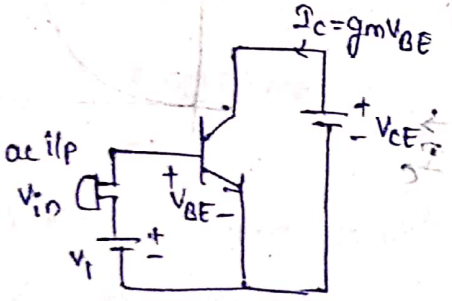
$$I_C = g_m V_{BE}$$

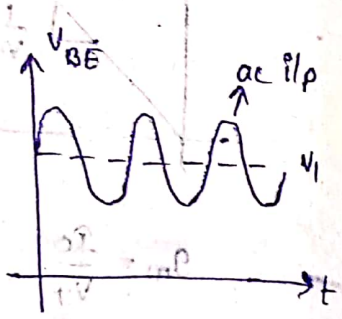
$$g_m = \frac{I_C}{V_{BE}}$$

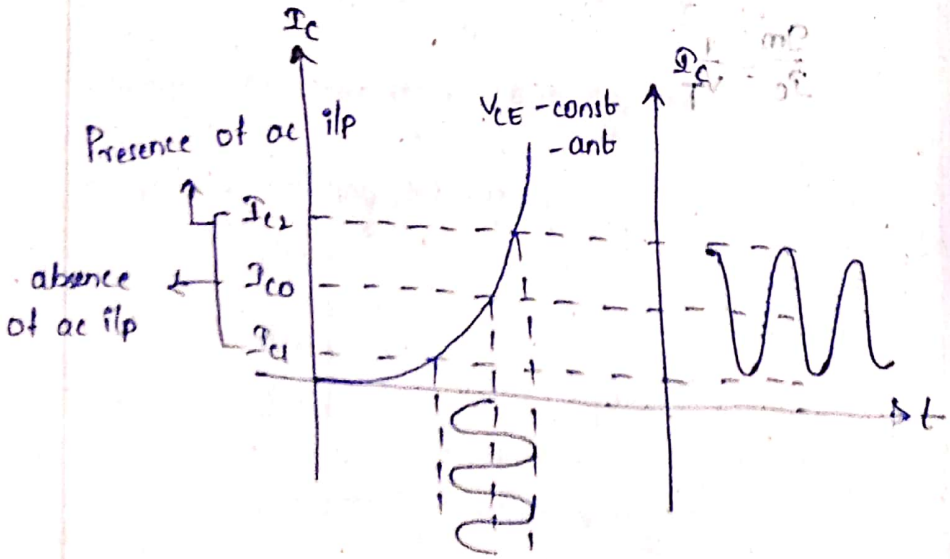


Voltage dependent current source.

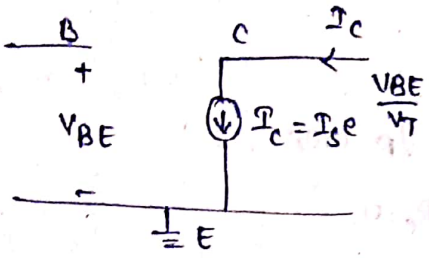
Combining time response curve with I/V characteristics.







Simple bipolar transistor model:



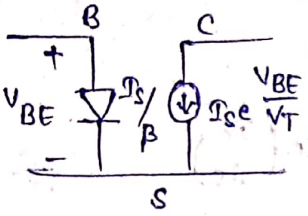
$I_c = \beta I_b$

$I_b = I_c/\beta$

$= \frac{I_S e^{V_{BE}/V_T}}{\beta}$

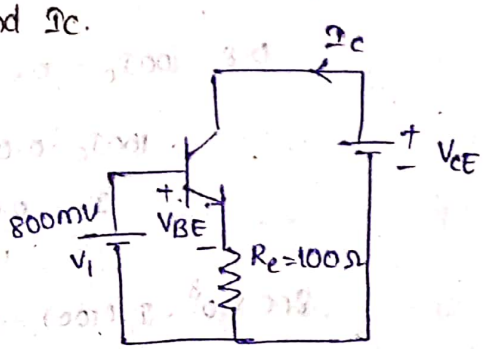
$$I_b = \frac{I_S}{\beta} e^{\frac{V_{BE}}{V_T}}$$

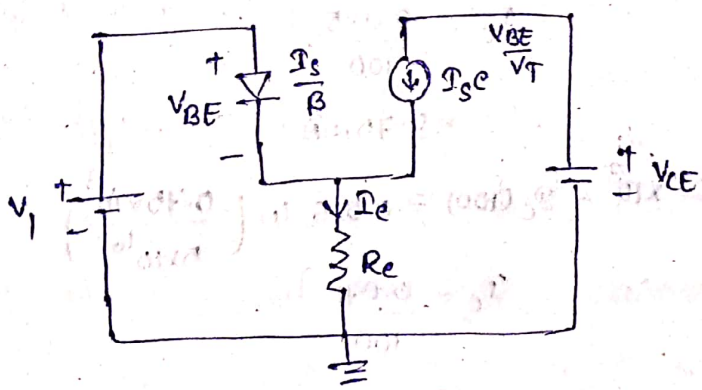
we have to add a diode in place of open circuit due to the availability of Base current.



large signal model

Let us consider a BJT biasing circuit with $R_c = 100\,\Omega$, $I_S = 5\times10^{-16}$ A. find I_C.





$$I_e = I_c + I_b$$

$$I_b = \frac{I_c}{\beta}$$

$$I_e \approx I_c$$

apply KVL for i/p loop

$$-V_1 + V_{BE} + I_e R_e = 0$$

$$V_1 = V_{BE} + I_e R_e$$

$$I_c = \frac{V_1 - V_{BE}}{R_e}$$

$$I_c = I_s e^{\frac{V_{BE}}{V_T}}$$

$$V_{BE} = V_T \ln\left(\frac{I_c}{I_s}\right)$$

$$V_1 - I_c R_e = V_T \ln\left(\frac{I_c}{I_s}\right)$$

Let $I_c = 1mA$

$$800 \times 10^{-3} - I_c(100) = 0.026 \ln\left(\frac{10^{-3}}{5 \times 10^{-16}}\right)$$

$$0.8 - 100 I_c = 0.026 \ln(0.2 \times 10^{13})$$

$$100 I_c = 0.063$$

$$I_c = \frac{0.063}{100} = 0.63mA$$

$$800 \times 10^{-3} - I_c(100) = 0.026 \ln\left(\frac{0.63 \times 10^{-3}}{5 \times 10^{-16}}\right)$$

$$I_c = \frac{0.075}{100}$$

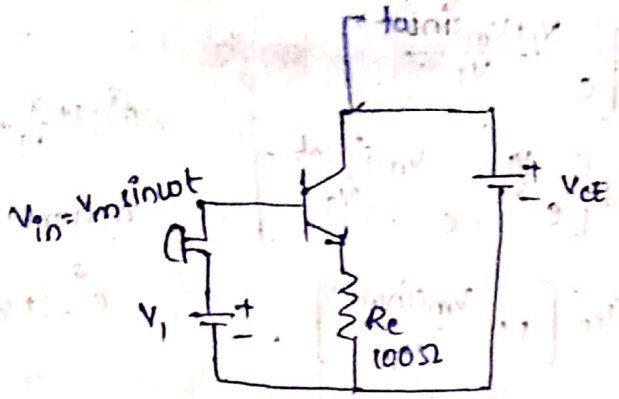
$$= 0.75mA$$

$$800 \times 10^{-3} - I_c(100) = 0.026 \ln\left(\frac{0.75 \times 10^{-3}}{5 \times 10^{-16}}\right)$$

$$I_c = \frac{0.071}{100}$$

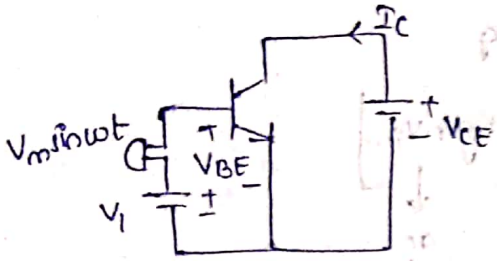
$$= 0.71 mA$$

Scanned with OKEN Scanner



$$V_1 + V_m \sin\omega t - I_C R_e = V_T \ln\left(\frac{I_C}{I_S}\right)$$

*



$$V_{BE} = V_1 + V_m \sin\omega t$$

$$I_C = I_S\, e^{\frac{V_{BE}}{V_T}}$$

$$I_C = I_S\, e^{\frac{V_1 + V_m \sin\omega t}{V_T}}$$

Large signal operation:

The signal is arbitarily large in the order of volts, from the circuit given input is sinusoidal output signal may be (or) may not be sinusoidal.

Small signal operation:

In small signal operation signal variation is in the order of mv (or) the signal peturbes (variations) the bias operating point by using a small signal operation.

Scanned with OKEN Scanner

$$I_c = I_s \left[e^{\frac{V_1 + V_m \sin\omega t}{V_T}} \right]$$

$$= I_s \left[e^{\frac{V_1}{V_T}} \cdot e^{\frac{V_m \sin\omega t}{V_T}} \right]$$

$$= I_{co} \left[1 + \frac{V_m \sin\omega t}{V_T} \right]$$

$$= I_{co} + \frac{I_{co}}{V_T} V_m \sin\omega t$$

↑ biasing

$$e^x = 1 + \frac{x}{1!} + \frac{x^2}{2!} + \dots$$

assume $V_{in} << V_T$

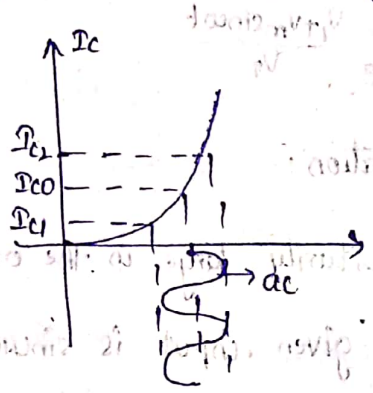
$e^{\varepsilon} = 1 + \varepsilon$

$$\boxed{I_c = I_{co} + g_m V_{in}}$$

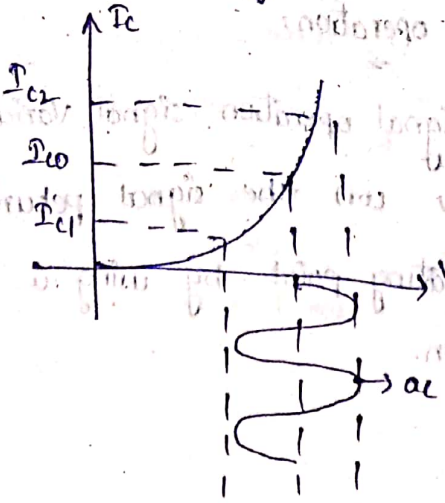
dc ac

if $V_m < V_T$ then it is small signal.

if $V_m > V_T$ then it is large signal.



Small signal variation.



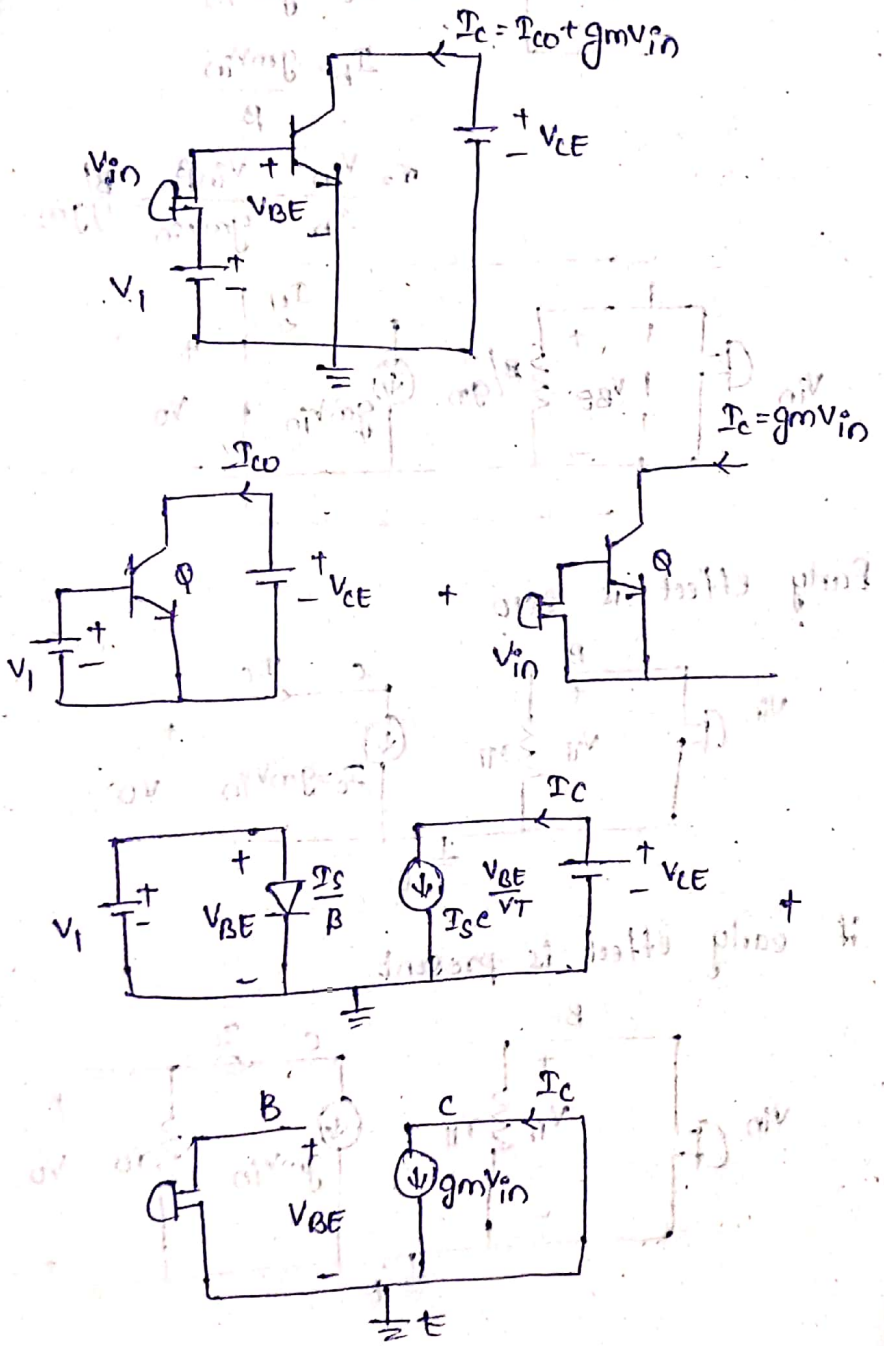
large signal variations

In small signal operation collector current varies sinusoidally.

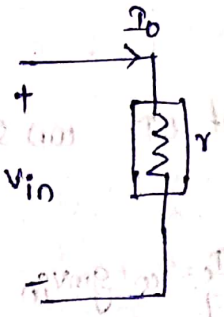
In small signal model,

$$I_c = I_{co} + g_m v_{in}$$

Small signal analysis of BJT (or) Small signal model of BJT



Here in small signal model β in the place of open circuit we have to keep a component due to the availability of Base current



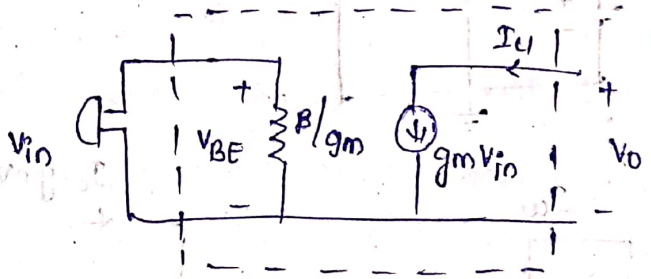
$I_c = \beta I_b$

$I_b = \frac{I_c}{\beta}$

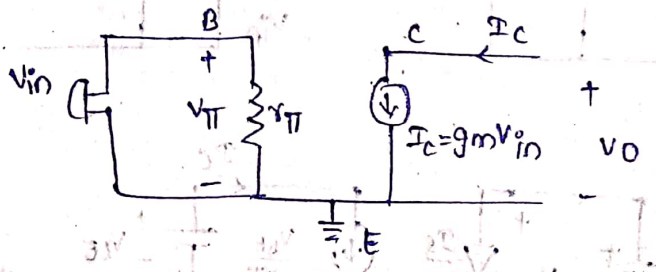
$I_c = g_m V_{in}$

$I_b = \frac{g_m V_{in}}{\beta}$

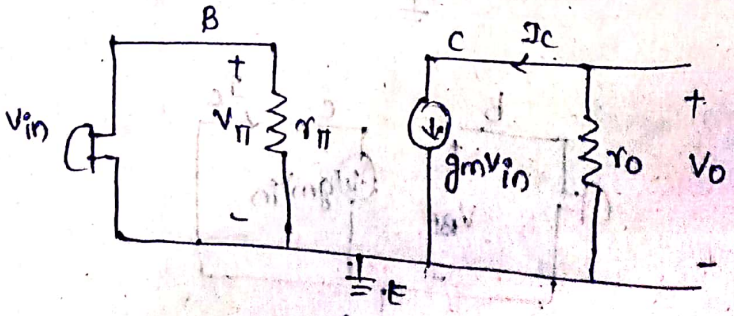
$r = \frac{V_{in}}{I_b} = \frac{V_{in}\beta}{g_m V_{in}} = \beta/g_m$



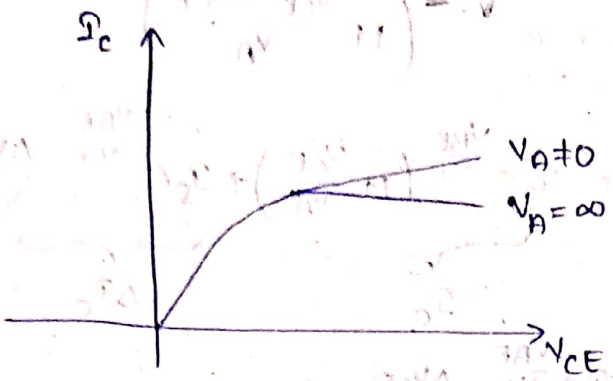
Early effect is zero



if early effect is present

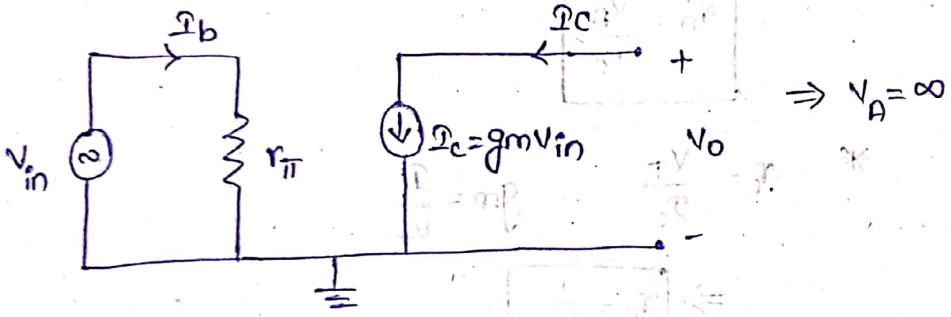


Consideration of Early effect on BJT:

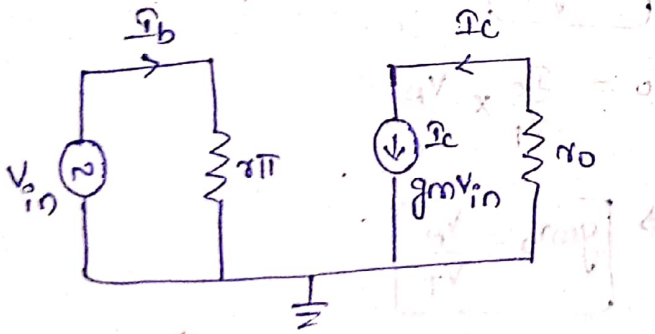


$$I_C = I_S e^{\frac{V_{BE}}{V_T}} \left(1 + \frac{V_{CE}}{V_A}\right)$$

$$I_S = \frac{A_E q n_i^2 D_n}{N_B W_B}$$

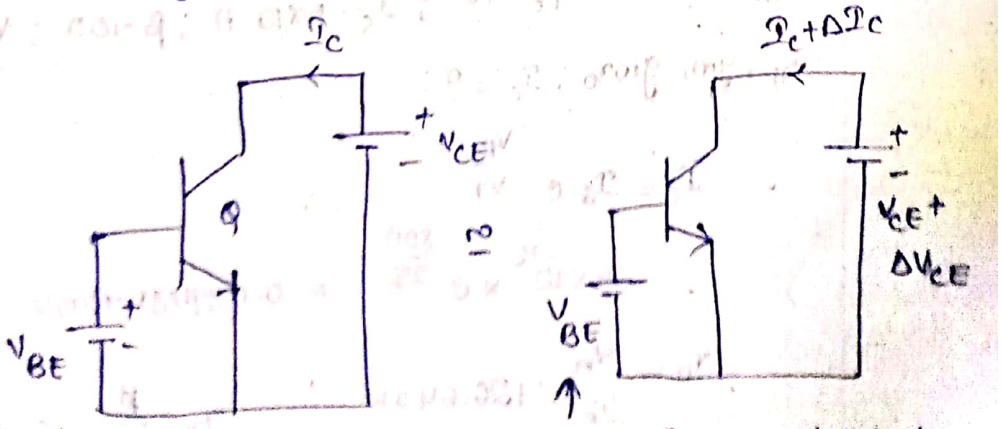


$\Rightarrow V_A = \infty$



$\Rightarrow V_A \neq 0$

$$A_V = -g_m r_o$$



change in V_{BE} leads to change in I_C & V_{CE}.

$$I_C + \Delta I_C = I_S e^{\frac{V_{BE}}{V_T}} \left(1 + \frac{V_{CE} + \Delta V_{CE}}{V_A}\right)$$

$$I_C + \Delta I_C = \underbrace{I_S e^{\frac{V_{BE}}{V_T}} \left(1 + \frac{V_{CE}}{V_A}\right)}_{I_C} + \underbrace{I_S e^{\frac{V_{BE}}{V_T}} \frac{\Delta V_{CE}}{V_A}}_{\Delta I_C}$$

$$\Delta I_C = I_S e^{\frac{V_{BE}}{V_T}} \frac{\Delta V_{CE}}{V_A}$$

$$r_O = \frac{\Delta V_{CE}}{\Delta I_C} = \frac{V_A}{I_S e^{\frac{V_{BE}}{V_T}}} = \frac{V_A}{I_C}$$

$$\boxed{r_O = \frac{V_A}{I_C}}$$

* $r_e = \frac{V_T}{I_C}$ $\quad g_m = \frac{I_C}{V_T}$

$$\Rightarrow \boxed{r_e = \frac{1}{g_m}}$$

* $g_m r_O = \frac{I_C}{V_T} \times \frac{V_A}{I_C}$

$$\Rightarrow \boxed{g_m r_O = \frac{V_A}{V_T}}$$

$V_{BE} = 800mV$

$V_{in} = 0.8V$; $V_{CE} = 1V$; $I_S = 5 \times 10^{-16} A$; $\beta = 100$; $V_A = 5V$

r_π, g_m, $g_m r_O$, $I_C = ?$

$$I_C = I_S e^{\frac{V_{BE}}{V_T}}$$

$$= 5 \times 10^{-16} \times e^{\frac{800}{25}} = 0.039481 \text{ Amps}$$

$$r_O = \frac{V_A}{I_C} = 126.64\,\Omega$$

$$g_m = 4.89\,mU$$

$$r_\pi = \frac{\beta}{g_m} = 12674.2\,\Omega$$

Scanned with OKEN Scanner