
WELCOME

THE PAIN YOU FEEL TODAY WILL BE THE STRENGTH YOU WILL FEEL TOMORROW

ANALOG ELECTRONICS

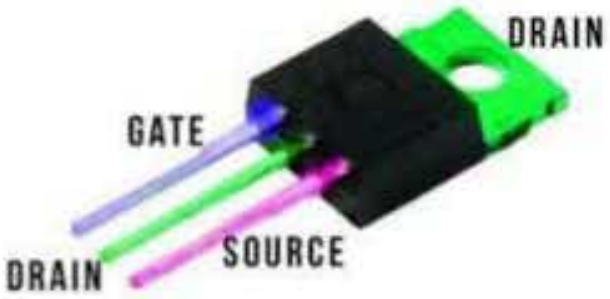
CHAPTER 3

MOSFET DC ANALYSIS AND ITS SMALL SIGNAL AMPLIFIERS

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Metal Oxide Semiconductor FET(MOSFET)





chapter 3

MOSFET Biasing and Its small signal Analysis

Introduction :-

* MOSFET stands for Metal Oxide Semiconductor Field Effect Transistor
* MOSFET is symmetrical device.
* MOSFET has 4 terminals :-
  1) Gate (G)
  2) Drain (D)
  3) Soure (S)
  4) Body (B)

Source :- Source is a terminal through which majority carriers enters into the semiconductor bar

Drain :- Drain is a terminal through which majority charge carriers leaves from the semiconductor bar

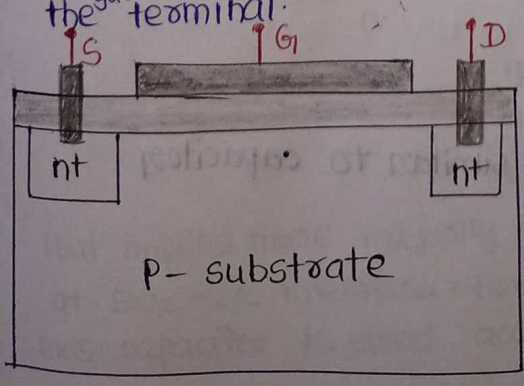
Gate :- Gate is a terminal which controls the flow of carriers from source to drain.

classification of MOSFETs :-

MOSFETs are broadly classified into 2 types :-
1) Depletion MOSFET (D-MOSFET)
2) Enhancement MOSFET (E-MOSFET)

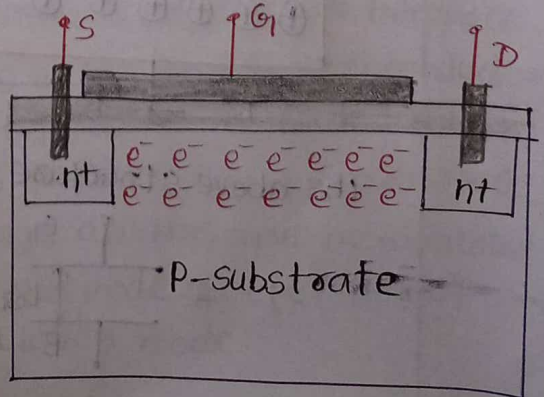
Enhancement MOSFET

In Enhancement MOSFET, the channel does not exist initially and is induced. i.e, the channel is developed by applying a voltage greater than threshold voltage, at the gate terminal.



Depletion MOSFET

on other hand, in depletion MOSFET, the channel is permanantly fabricated (by doping) at the time of construction of MOSFET itself.



How to create a channel in Enhancement MOSFET :-

Consider the following physical structure of MOSFET

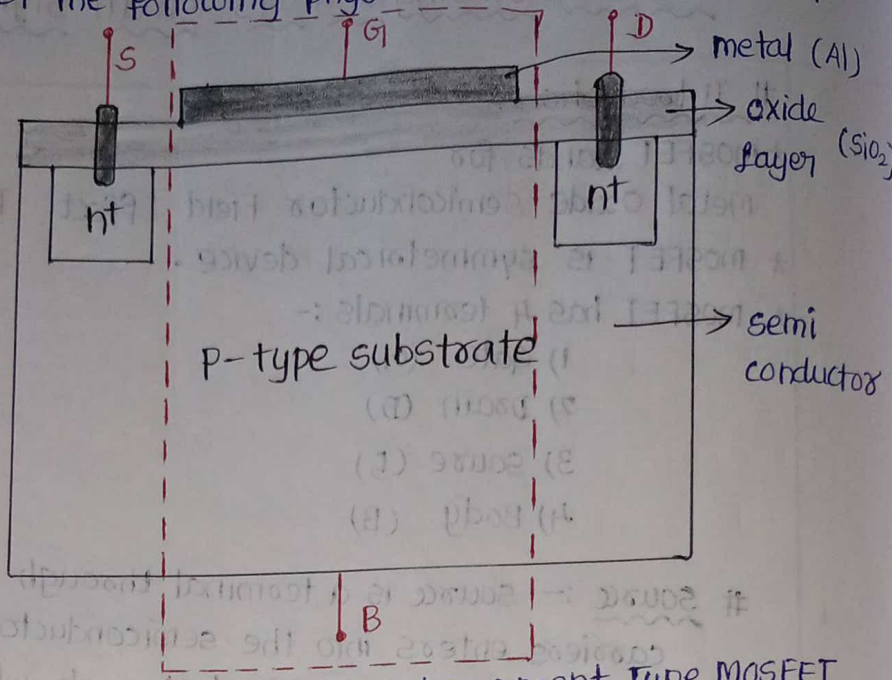


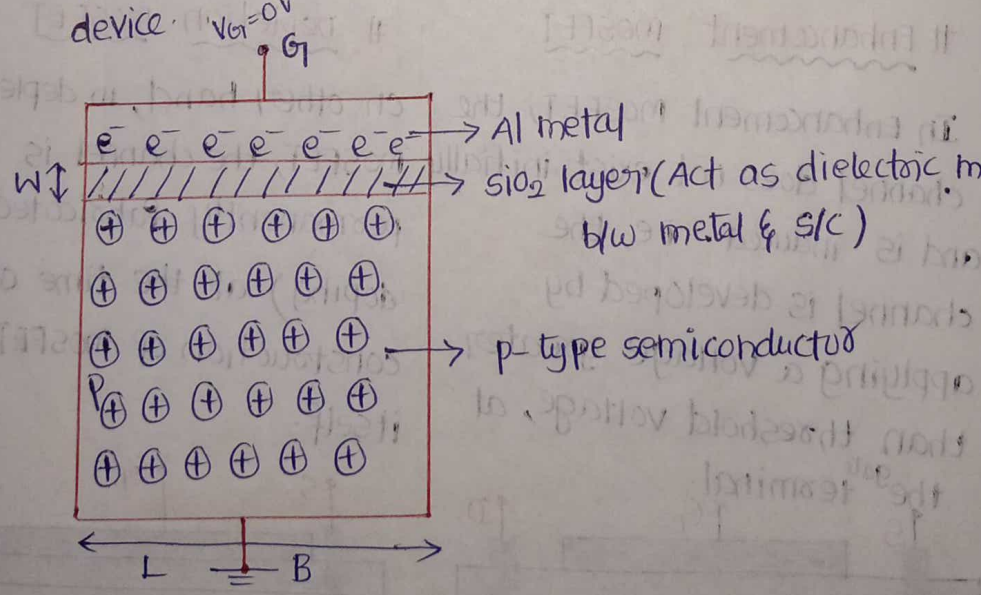
figure shows n-channel Enhancement Type MOSFET

Let cut of metal-oxide-semiconductor from above structure.

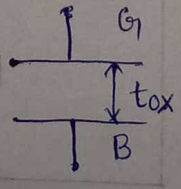
Now we apply different potentials across mos-structure and let's see what will happen.

case(i) When $V_G = 0V$

If we cut mos structure, we have the following device.



The above structure is similar to capacitor



capacitance of parallel plate capacitor.

$$C = \frac{A\epsilon}{d}$$

where A = area of the plate and
d = distance b/w the plates.

The mos capacitors also has 2 charged plates:
i) metal plate (-ve charged)
ii) P-type semiconductor (+ve plate)

∴ The capacitance of mos-capacitor is given by

$$C_{ox} = \frac{A\epsilon_{ox}}{t_{ox}}$$

t_{ox} = thickness of oxide layer and
ϵ_{ox} = permitivity of SiO_2

$$\epsilon_{ox} = \epsilon_0 \epsilon_{ox\cdot r}$$

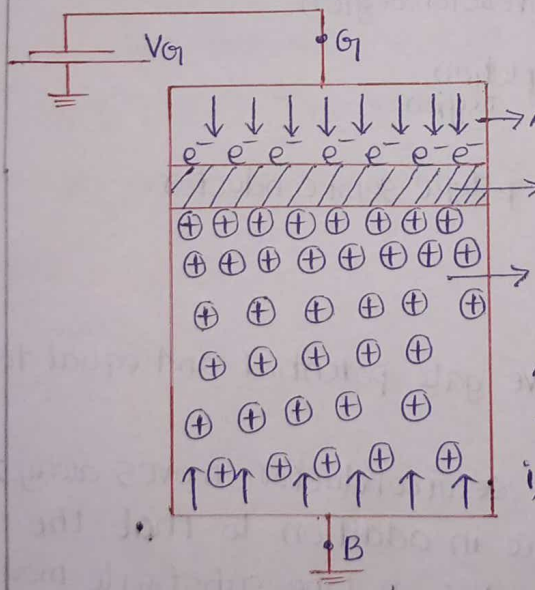
$$\epsilon_{ox\cdot r} = 3.7 \approx 4$$

$$\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m} = \frac{10^{-9}}{36\pi}$$

Area of plate A = WL

capacitance per unit area $C_{ox} = \frac{C_0}{A} = \frac{\epsilon_{ox}}{t_{ox}}$

case (ii) V_{GS} = -Ve :-



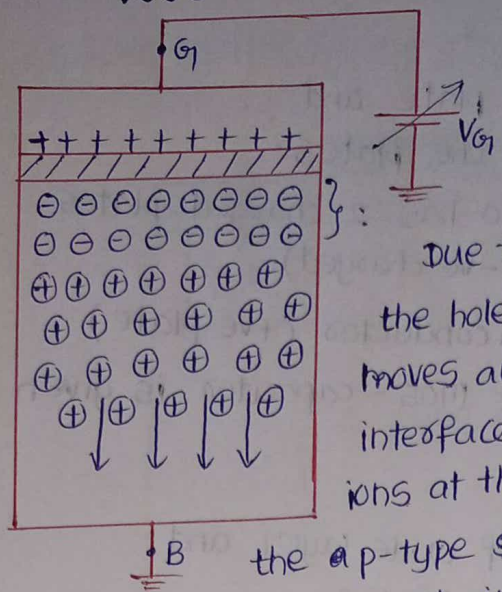
As we apply -ve potential at gate terminal,

i) electrons in the gate metal repelled by -ve potential and move towards metal-oxide interface

ii) Holes in the p-side semi conductor get repelled due to V_G and holes moves towards SiO_2 & S/C interface

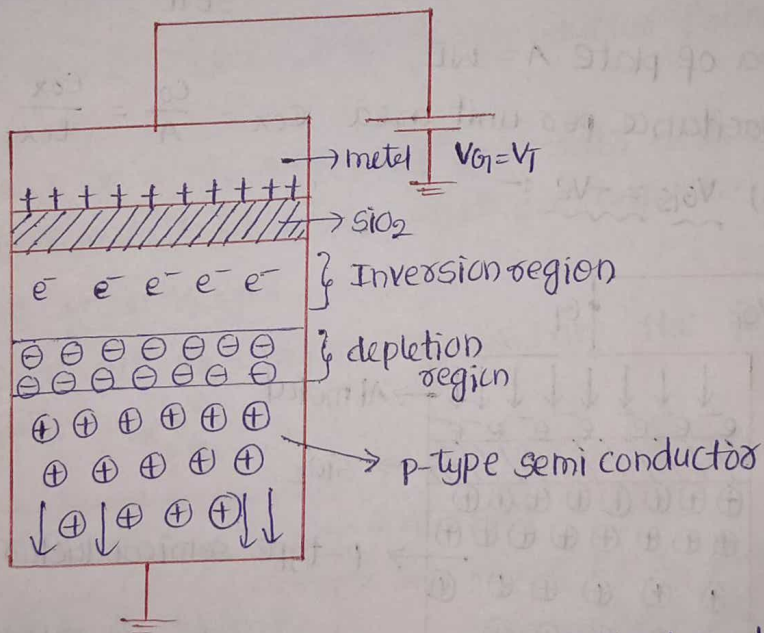
That implies more majority charge carriers are accumulated at SiO_2 - S/C interface. Hence this mode of operation of mos-capacitor is called accumulation mode.

case (iii) V_{GS} = +ve :- (small positive voltage)



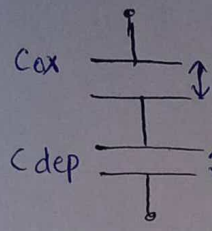
Due to application of +ve potential, the holes in the p-type semiconductor moves aways from the Si-O_2-S/C interface leaving behind -ve immobile ions at the SiO_2-S/C interface. Therefore the a p-type semiconductor is depleted off majority holes at SiO_2-S/C interface. And thence this mode of operation is called depletion mode.

case (iv) V_{GS} = +ve and $V_{GS} = V_T$ (Threshold Voltage)



Due to application of +ve gate potential and equal to threshold voltage :

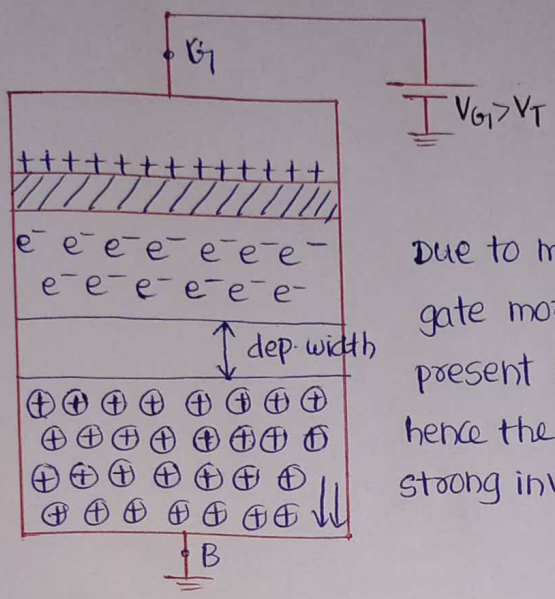
1) The holes in the p-type semiconductor moves aways from SiO_2-S/C interface in addition to that the minority carriers (e^-) in the p-type substrate move towards SiO_2-S/C interface.
2) Therefore here we have 2 capacitances
   1) due to SiO_2
   2) depletion region



$C_{eq} = \frac{C_{ox} C_{dep}}{C_{ox} C_{dep}}$ [series combination of capacitance]

Here in the p-type semiconductors, electrons are playing their role. charge is inverted and hence the mode is called inversion mode.

case (V) V_{GS} = +ve and $V_{GS} > V_t$:-

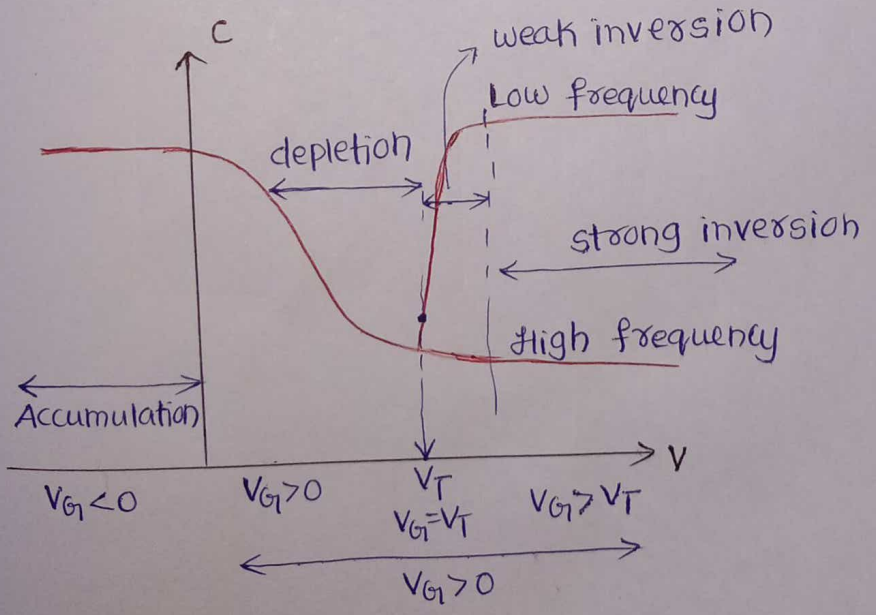


Due to more +ve potential at gate more no. of electrons are present at SiO_2-S/C interface and hence the mode is called strong inversion.

Threshold voltage :-

The threshold voltage of an mos capacitor is the gate voltage V_G, required to create inversion.

CV characteristics of MOS CAP :-

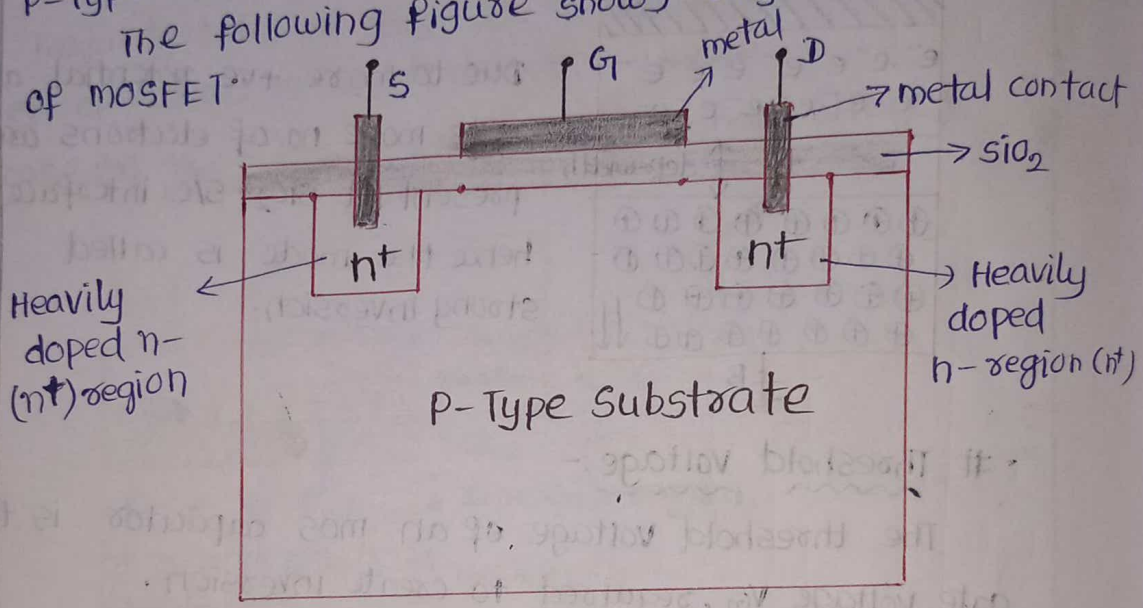


construction of a MOSFET :-

The construction of a MOSFET is a bit similar to the FET. An oxide layer is deposited on the substrate to which the gate terminal is connected. This oxide layer acts as an insulator (SiO_2 insulates from the substrate) and hence the MOSFET has another name as IGFET (Insulated gate field effect transistor).

In a construction of MOSFET, a lightly doped substrate, is diffused with a heavily doped region. Depending upon the substrate used, they are called as p-type and N-type MOSFETs.

The following figure shows constructional diagram of MOSFET.



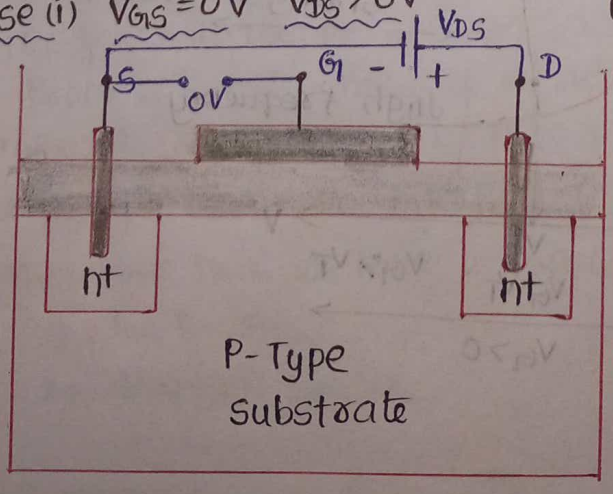
working :-

Enhancement MOSFET :-

N-channel Enhancement MOSFET :-

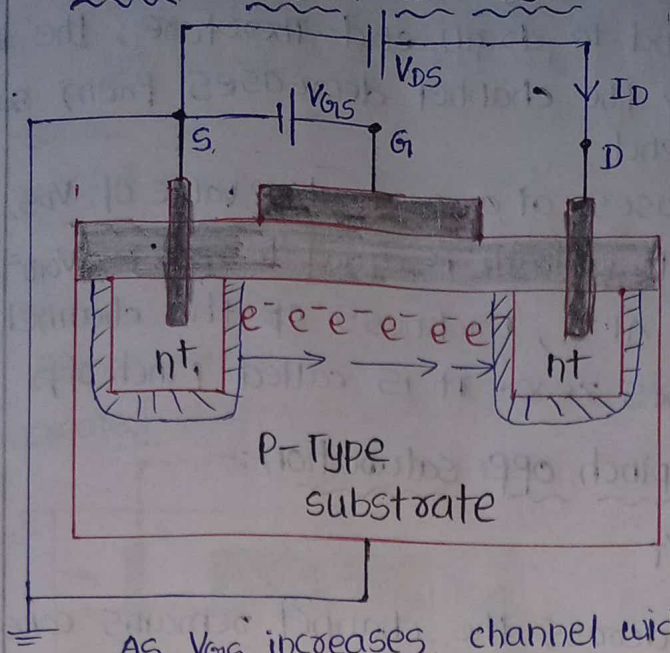
Enhancement MOSFET is simply called E-MOSFET. Lets apply a voltage V_{DS} b/w D and S.

case (i) $V_{GS} = 0V$ $V_{DS} > 0V$ $(0 < V_{GS} < V_T)$



There will be no current flow b/w drain & source as there is no channel b/w them.

case (ii) $V_{GS} > V_T$ and $V_{DS} > 0$:



When $V_{GS} > V_T$, positive gate voltage w.r.t source will charge the capacitor. Therefore, a channel is induced, and current b/w D & S.

As V_{GS} increases, channel width increases and therefore I_D increases.

points to be remember :-

Gate to source voltage V_{GS} and threshold voltage V_T are +ve for N-channel Enhancement MOSFET

N-channel Enhancement mosfet operates in enhancement mode only for +ve V_{GS} values.

In N-channel Enhancement mosfet body / substrate / bulk should be connected to ground or source terminal, whereas in integrated circuits it should be connected to most -ve values.

N-channel E-MOSFET will be ON for +ve V_{GS} values ($V_{GS} > V_T$) and it will be OFF for ($0 < V_{GS} < V_T$) and -ve V_{GS} values (i.e, $V_{GS} < V_T$)

channel acts like a resistor and the resistance of the channel is increases from source end to drain end. Therefore potential / voltage across the channel increases from source end to drain end.
i.e, Increases from 0 to V_{DS}.

The voltage b/w gate and channel decreasing from source end to drain end. (i.e, decreases from V_{GS} to $V_{GS} - V_{DS}$). Therefore, thickness of the channel decreases from source end to drain end.

The potential or voltage across the channel increases from source end to drain end. Therefore, the inversion charge across the channel decreases from source end to drain end.

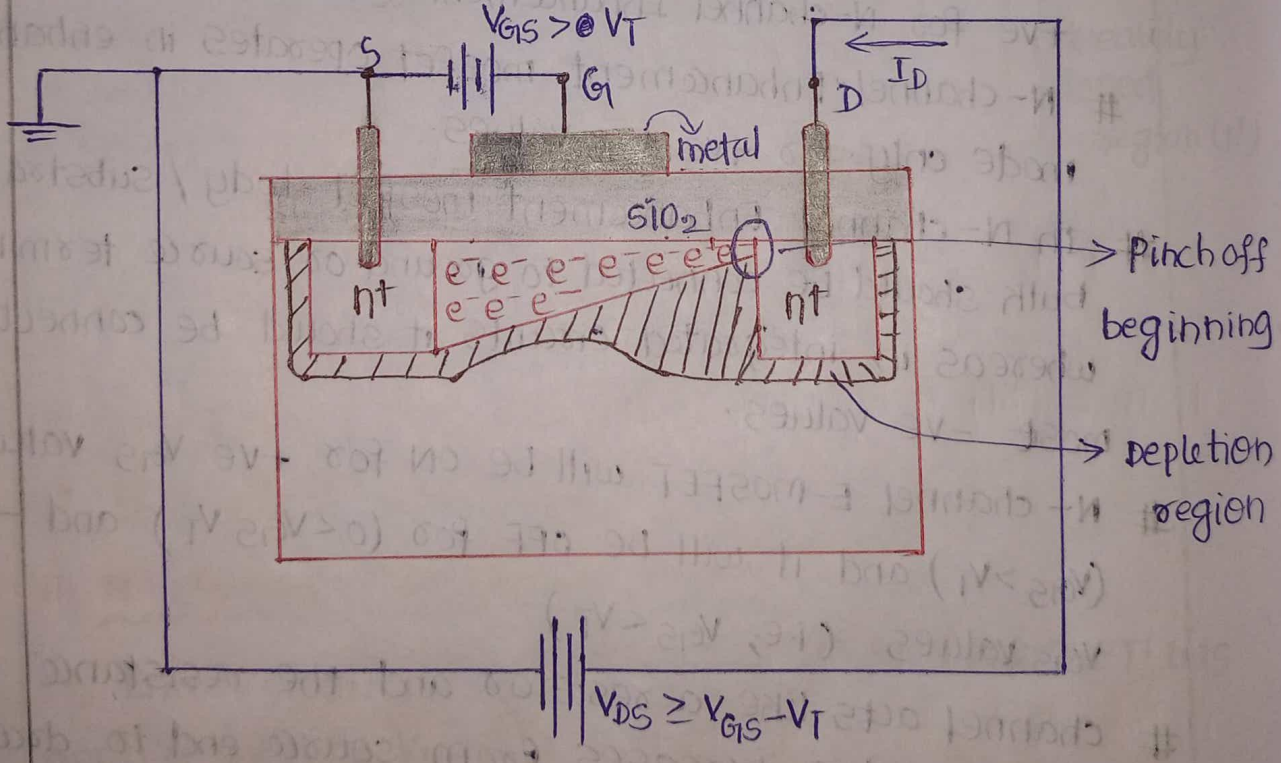
As V_{DS} is increases at a particular value of V_{DS}, the voltage b/w gate & drain is equal to V_T (i.e, $V_{GD} = V_{GS} - V_{DS} = V_T$). At V_T, thickness of the channel near to drain becomes zero. It is called pinch off.

condition for pinch off saturation :-

$$V_{DS} \geq V_{GS} - V_T$$

Electric field across the channel remains constant at pinch off. This pinch-off phenomenon is also called saturation.

When $V_{GS} > V_T$ and $V_{DS} \geq V_{GS} - V_T$:-

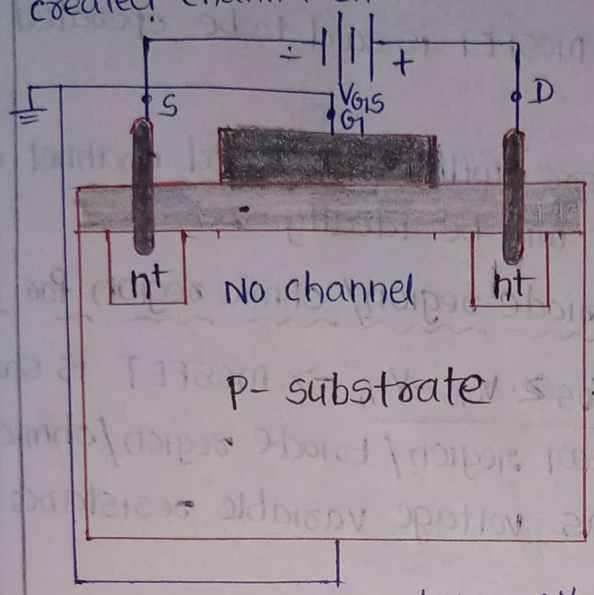


At pinch off / saturation, channel is in tapered shape.

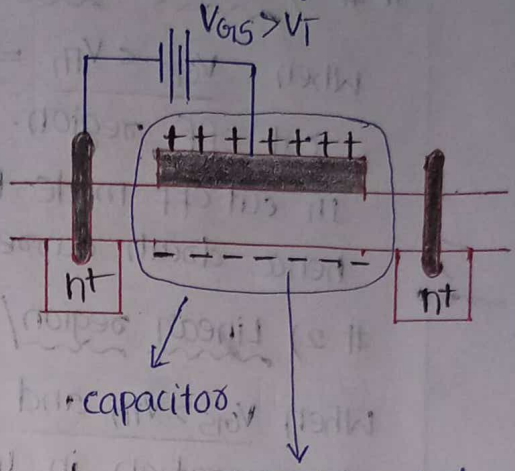
N- channel Enhancement Type MOSFET characteristics:-

Let set $V_{GS} = 0V$ and apply voltage V_{DS} b/w drain & source. Since there is no channel fabricated in an enhancement mosfet and no channel induced as $V_{GS} = 0V$ therefore $I_D = 0A$.

Let make V_{GS} some positive value. This positive value of V_{GS} charges the capacitor with gate plate +ve and channel -ve. Thus a channel is created b/w D & S. This created channel enables conduction b/w drain & source.

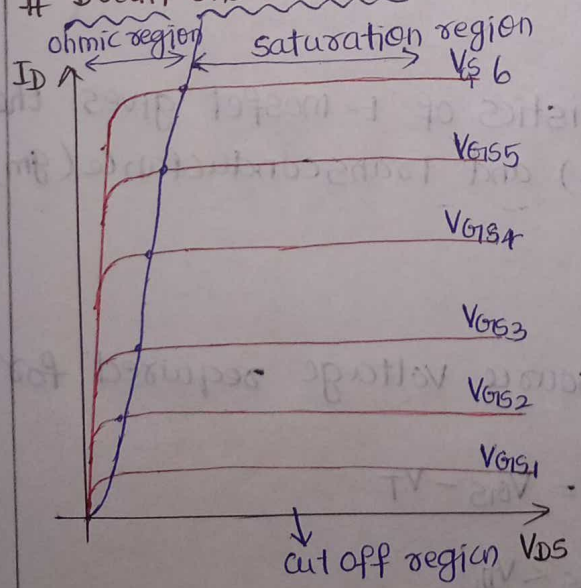


$V_{GS} < V_T$ / $V_{GS} = 0V$

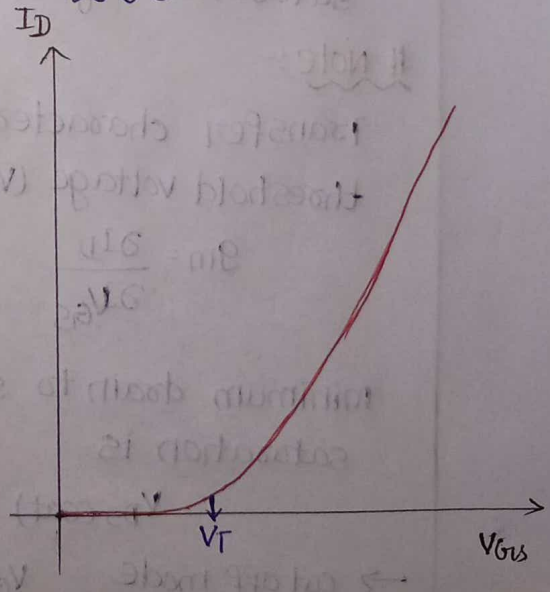


As we keep increasing V_{GS}, the channel penetrates more deeper into mosfet i.e, channel width increases or channel resistance decreases therefore drain current increases as shown in below figure.

Drain characteristics:



Transfer characteristics:-



Region of operation :-

From the operation of MOSFET, we can say there are 3 modes of operation

1) cut off region
2) Linear region / Triode region / ohmic region
3) Saturation region

1) cut off Region for NMOS :-

When $V_{GS} < V_{Th}$ ⇒ MOSFET is said to be operated in cut off region.

In cut off mode there will no induced channel and hence drain current will be ideally zero.

2) Linear region / Triode region / ohmic region for Nmos :-

When $V_{GS} > V_{Th}$ and $V_{DS} \geq V_{GS} - V_{Th}$ ⇒ MOSFET is said to be operation in linear region / triode region / ohmic region.

MOSFET can be used as voltage variable resistance in the linear region.

3) Saturation region for NMOS :-

When $V_{GS} > V_{Th}$ and $V_{DS} \geq V_{GS} - V_{Th}$ ⇒ MOSFET is said to operated in saturation region.

MOSFET can be used as ON switch & amplifier in the saturation region.

Note :-

Transfer characteristics of E-mosfet gives the threshold voltage (V_T) and transconductance (g_m).

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

minimum drain to source voltage required for saturation is

$$V_{DS(sat)} = V_{GS} - V_T$$

→ cut off mode $V_{GS} < V_{Th}$

→ Linear region $V_{GS} > V_{Th}$ and $V_{DS} < V_{GS} - V_T$

→ saturation region $V_{GS} > V_T$ and $V_{DS} \geq V_{GS} - V_T$

current equation in N-channel enhancement mosFET :-

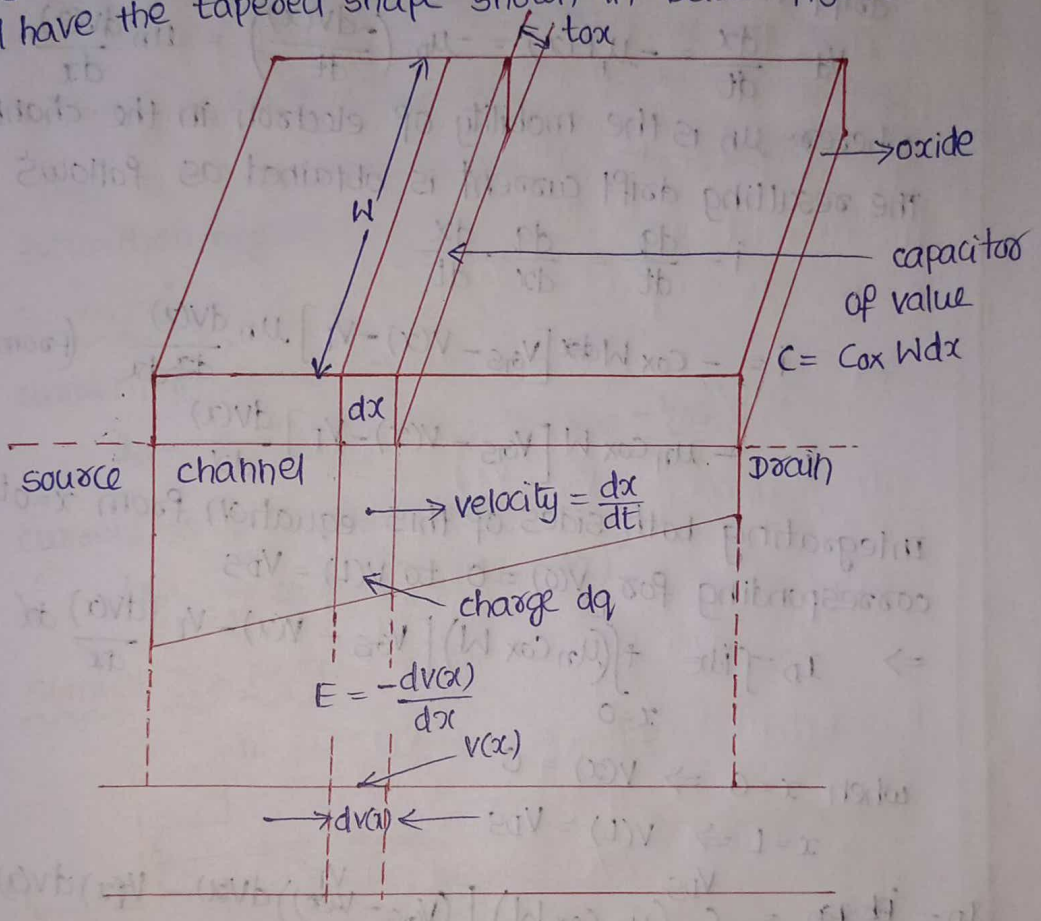
cut-off region :-

When $V_{GS} < V_T$,

The NMOS enhancement mosFET operation in cut off region and hence mosFET is operation in has no drain current $I_D = 0$

Linear region / Triode region / ohmic region :-

Now we shall consider operation in the triode region, for which the channel must be continuous and thus V_{GD} must be greater than V_T or $V_D < V_{GS} - V_T$. In this case the channel will have the tapered shape shown in below figure.



Recall that in the mosFET, the gate and the channel region form a parallel plate capacitor for which the oxide layer serves as the dielectric. If the capacitance per unit gate area is denoted Cox and the thickness of the oxide layer is tox, then

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

where ϵ_{ox} is the permitivity of the silicon oxide.

consider the infinitesimal strip of gate at distance x from the source. The capacitance of the strip is $C_{ox} W dx$. If the effective voltage responsible for including the channel at point x is $(V_{GS} - V(x) - V_T)$ where V(x) is the voltage in the channel at point x then the charge stored on this infinitesimal strip of the gate capacitance is

$$dq = -C_{ox} W dx \left[V_{GS} - V(x) - V_T\right] \longrightarrow (1)$$

At point x the field can be expressed as

$$E(x) = \frac{-dV(x)}{dx}$$

The electric field E(x) causes the electron charge dq to drift toward the drain with a velocity $\frac{dx}{dt}$

$$V_d = \frac{dx}{dt} = -\mu_n E(x) = -\mu_n \left(\frac{-dV(x)}{dx}\right) = \mu_n \frac{dV(x)}{dx} \longrightarrow (2)$$

where μ_n is the mobility of electron in the channel.

The resulting drift current is obtained as follows

$$i = \frac{dq}{dt} = \frac{dq}{dx} \cdot \frac{dx}{dt}$$

$$i = -C_{ox} W \left[V_{GS} - V(x) - V_T\right] \mu_n \frac{dV(x)}{dx} \quad \text{(From (1) \& (2))}$$

$$i = -\mu_n C_{ox} W \left[V_{GS} - V(x) - V_T\right] \frac{dV(x)}{dx}$$

Integrating both sides of this equation from x=0 to x=L corresponding for V(0) = 0 to V(L) = V_{DS}

$$\Rightarrow I_D = \int i\,dx = \int_{x=0}^{L} (\mu_n C_{ox} W) \left[V_{GS} - V(x) - V_T\right] \frac{dV(x)}{dx} dx$$

when $x = 0 \Rightarrow V(x) = 0$

$x = L \Rightarrow V(L) = V_{DS}$

$$I_D = \int_0^{V_{DS}} \left(\mu_n C_{ox} \frac{W}{L}\right) \left[\left(V_{GS} - V_T\right) dV(x) - V(x)\, dV(x)\right]$$

$$= \mu_n C_{ox} \frac{W}{L} \int_0^{V_{DS}} \left(V_{GS} - V_T\right) dV(x) - V(x)\, dV(x)$$

$$= \mu_n C_{ox} \frac{W}{L} \left[\left(V_{GS} - V_T\right)\left(V_{DS} - 0\right) - \frac{V_{DS}^2 - 0^2}{2}\right]$$

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[\left(V_{GS} - V_T\right)\left(V_{DS}\right) - \frac{V_{DS}^2}{2}\right]$$

This is the expression for $I_D - V_{DS}$ characteristic in the triode region.

saturation region :-

When $V_{GS} > V_T$ and $V_{DS} \geq V_{GS} - V_T$,
MOSFET is said to be in saturation.

The value of current at the edge of triode region or equivalently at the beginning of the saturation can be obtained by substituting $V_{DS} = V_{GS} - V_T$ in current eqn for triode eqn.

$$\Rightarrow I_D = \mu_n C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_T)(V_{GS} - V_T) - \frac{1}{2}(V_{GS} - V_T)^2\right]$$

$$\Rightarrow I_D = \mu_n C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_T)^2 - \frac{1}{2}(V_{GS} - V_T)^2\right]$$

$$\Rightarrow I_D = \mu_n C_{ox} \left(\frac{W}{L}\right) \left[\frac{1}{2}(V_{GS} - V_T)^2\right]$$

$$\Rightarrow I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_T)^2$$

This is the expression for $I_D - V_{DS}$ characteristic in the saturation region.

summary :-

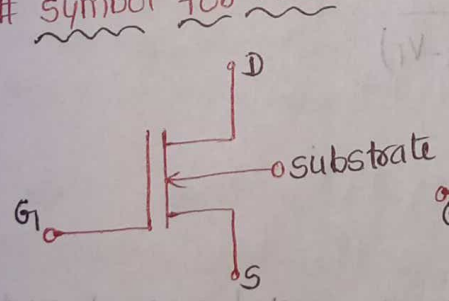
current in ohmic region :

$$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2}\right]$$

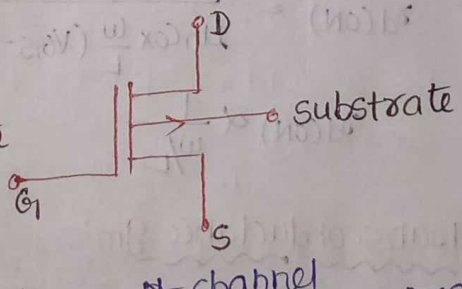
current in saturation region :

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_T)^2$$

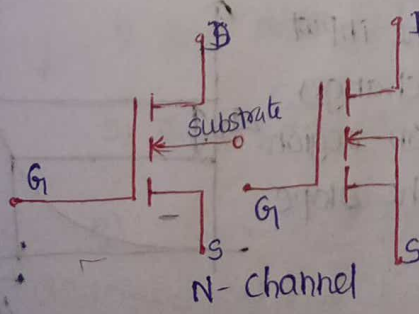
symbol for MOSFET



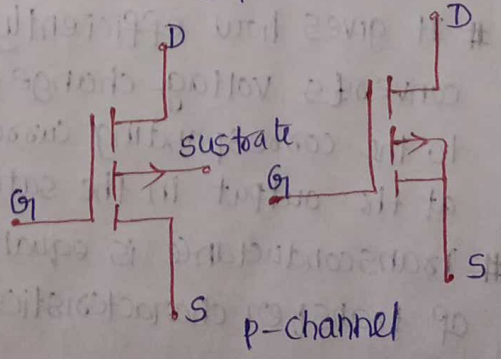
N-channel depletion MOSFET



P-channel depletion MOSFET



N-channel



P-channel

Enhancement MOSFET

Deep Triode region :-

Deep triode region is also a linear region but for small values of V_{DS}.

The condition for deep triode region is

$$V_{DS} < 2(V_{GS} - V_T)$$

$\Rightarrow$ current eqn for linear region is

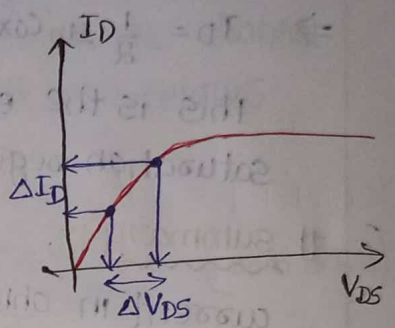
$$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right)\left((V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right)$$

$\Rightarrow$ current eqn for deep triode region

$$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_T)V_{DS}\right)$$

Drain ON resistance (r_d) :-

It is the resistance offered by MOSFET in the linear region for small values of V_{DS} (deep triode region)



For deep triode region, the current eqn is given as

$$I_D = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)V_{DS}$$

$$r_d = \frac{1}{\partial I_D / \partial V_{DS}}$$

$$\frac{\partial I_D}{\partial V_{DS}} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)$$

$$r_d = \frac{1}{\frac{\partial I_D}{\partial V_{DS}}} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)}$$

$$\therefore r_{d(ON)} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)}$$

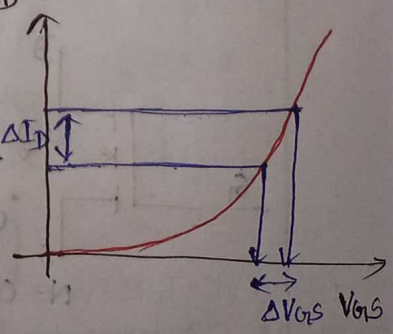
$$r_{d(ON)} \propto \frac{1}{W/L}$$

Transconductance g_m :-

Transconductance (g_m) is also called mutual conductance.

It gives how efficiently MOSFET converts voltage change at the input to the corresponding current changes at the output in the saturation region.

Transconductance is equal to the slope of transfer characteristics.



$$g_m = \frac{\Delta I_{DS}}{\Delta V_{GS}} = \frac{\partial I_D}{\partial V_{GS}}$$

current in saturation region of the MOSFET is given by

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS}-V_T)^2\right]$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_T)\times 2$$

$$\# \quad g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_T) \longrightarrow (1)$$

From current eqn

$$V_{GS}-V_T = \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}}$$

substitute $(V_{GS}-V_T)$ expression in g_m

$$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)\sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)}}$$

$$\# \quad g_m = \sqrt{2I_D\,\mu_n C_{ox}\left(\frac{W}{L}\right)} \longrightarrow (2)$$

From current eqn

$$\mu_n C_{ox}\left(\frac{W}{L}\right) = \frac{2I_D}{(V_{GS}-V_T)^2}$$

substituting above eqn in eqn (1)

$$\Rightarrow g_m = \frac{2I_D}{(V_{GS}-V_T)^2}(V_{GS}-V_T)$$

$$\Rightarrow g_m = \frac{2I_D}{(V_{GS}-V_T)}$$

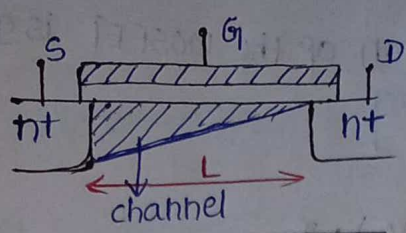
Expressions for transconductance :-

1) $g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_T)$

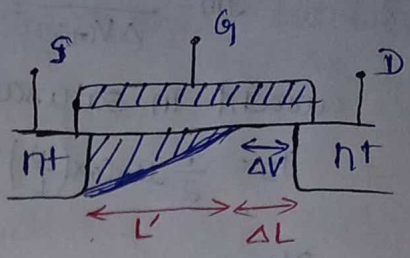
2) $g_m = \sqrt{2I_D\,\mu_n C_{ox}\left(\frac{W}{L}\right)}$

3) $g_m = \frac{2I_D}{V_{GS}-V_T}$

channel Length modulation :-



$V_{DS} = V_{GS} - V_T$

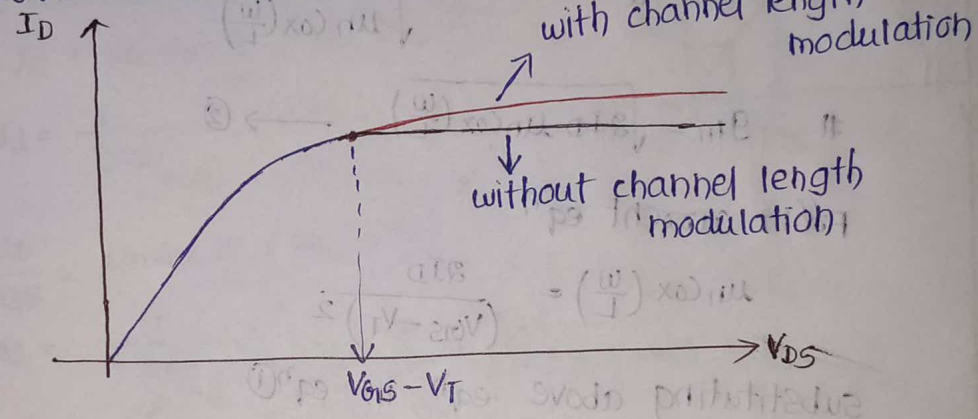


$V_{DS} > V_{GS} - V_T$

When we increase V_{DS} beyond $V_{GS} - V_T$ (over drive voltage) the channel at drain end completely pinched off and hence channel length decreases.

When the electrons entered the pinch off, it get highly accelerated. Therefore the rate of change of carriers increases. And hence I_D increases with increase in V_{DS} above the over drive voltage $(V_{GS} - V_T)$

drain characteristics :-



current eqn including channel length modulation :-

The current eqn for MOSFET in saturation region is given by

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_T)^2$$

Now channel length decreases. Effective channel length

$$L' = L - \Delta L \qquad \Delta L = \text{func}^n (V_{DS})$$

$$L' = L\left(1 - \frac{\Delta L}{L}\right)$$

$\frac{\Delta L}{L}$ → Normalised value

$$\frac{\Delta L}{L} \propto V_{DS} \Rightarrow \frac{\Delta L}{L} = \lambda V_{DS}$$

$$L' = L(1 - \lambda V_{DS}) \longrightarrow (1)$$

Current eqn including channel length modulation :-

$$I_D' = \frac{1}{2} \mu_n C_{ox} \frac{W}{L'} (V_{GS} - V_T)^2$$

Now substitute eq^n ① in above eq^n

$$I_D' = \frac{1}{2}\mu_n C_{ox}\frac{W}{L(1-\lambda V_{DS})}(V_{GS}-V_T)^2$$

$$I_D' = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(1-\lambda V_{DS})^{-1}(V_{GS}-V_T)^2$$

By taylor series expansion

$$(1-\lambda V_{DS})^{-1} = 1+\lambda V_{DS} + \underbrace{(\lambda V_{DS})^2 + (\lambda V_{DS})^3 + \cdots}_{\text{Neglecting all higher terms}}$$

$$(1-\lambda V_{DS})^{-1} = 1+\lambda V_{DS}$$

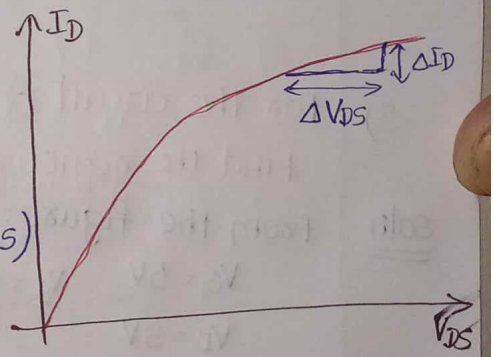
$$\Rightarrow I_D' = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(1+\lambda V_{DS})(V_{GS}-V_T)^2$$

$$\Rightarrow I_D' = \underbrace{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_T)^2}_{\text{current eq}^n \text{ without channel length modulation}}(1+\lambda V_{DS})$$

$$\Rightarrow I_D' = I_D(1+\lambda V_{DS})$$

output resistance :-

It is the o/p resistance offered by MOSFET in saturation region.



$$r_o = \frac{1}{\frac{\partial I_D}{\partial V_{DS}}}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

$$\frac{\partial I_D}{\partial V_{DS}} = \underbrace{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_T)^2}_{I_D \text{ (without C.L.M)}}\lambda$$

$$r_o = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{1}{I_D\lambda} = \frac{V_A}{I_D}$$

$$V_A = \frac{1}{\lambda}$$

Problems :-

1) For an N-channel Enhancement Type MOSFET $V_T = 0.7V$ $V_{GS} = 1.5V$. Find the region of operation for $V_{DS} = 2V$

Soln Given threshold voltage $V_T = 0.7V$

$V_{GS} = 1.5V$ $V_{DS} = 2V$

i) $V_{GS} > V_T \Rightarrow$ MOSFET is ON

Active mode

$V_{GS} - V_T = 1.5 - 0.7$

$\approx 0.8V$

Saturation mode

$V_{GS} - V_T = 1.5 - 0.7$

≈ 0.8

$V_{DS} > V_{GS} - V_T$

$\Rightarrow$ saturation mode

2) Repeat the above problem by changing V_{GS}. New $V_{GS} = 3V$

Soln $V_{GS} > V_T \Rightarrow$ MOSFET is ON $\because V_{GS} - V_T = 3 - 0.7 = 2.3$

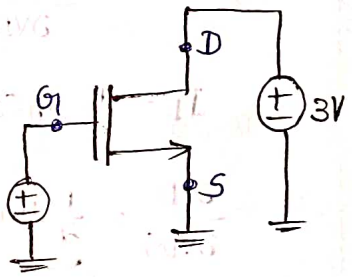
But $V_{DS} < V_{GS} - V_T \Rightarrow$ Linear region/triode region/ohmic region.

3) For the circuit shown in figure, MOSFET has $V_T = 0.6V$. Find the region of operation.

Soln From the figure:

$V_G = 5V$ $V_S = 0$

$V_D = 3V$



#conditions for Region of operation in terms of point potentials :

1) cut-off : $V_{GS} < V_T \Rightarrow V_G - V_S < V_T$

2) Linear region:

$V_{GS} > V_T$ & $V_{DS} < V_{GS} - V_T$

$V_G - V_S > T$ $V_D - V_S < V_G - V_S - V_T$

$V_D < V_G - V_T$

3) saturation region:-

$V_{GS} > V_T$ & $V_{DS} \geq V_{GS} - V_T$

$V_G - V_S > V_T$ $V_D - V_S \geq V_G - V_S - V_T$

$V_D \geq V_G - V_T$

Given $V_T = 0.6$

i) $V_{GS} = V_G - V_S = 5 > 0.6$ $(V_{GS} > V_T)$ → Transistor ON

ii) $V_D = 3V$ $V_G - V_T = 5 - 0.6 = 4.3V$

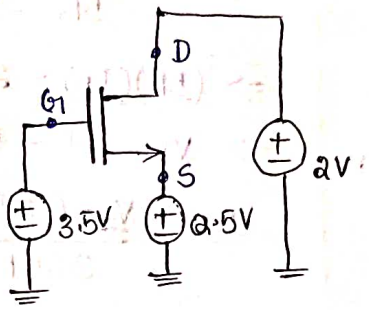
$V_D < V_G - V_T$ → Triode region.

4) For the circuit shown in figure MOSFET has $V_T = 0.6V$. Find the region of operation.

Soln From figure, $V_T = 0.6V$ (given)

$V_G = 3.5V$
$V_S = 0.5V$
$V_D = 2V$

$V_{GS} = V_G - V_S$
$= 3.5 - 0.5 = 3V$
$V_{DS} = V_D - V_S$
$= 2 - 0.5 = 1.5V$



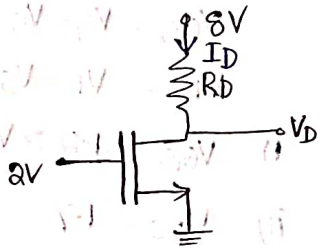
1) $V_{GS} > V_T \Rightarrow$ MOSFET ON

2) $V_{DS} = 1.5 < (V_{GS} - V_T) \Rightarrow$ Linear region

5) Find the maximum value of R_D for which transistor remains in saturation.

Device parameters:

$\mu_n C_{ox} \frac{W}{L} = 2mA/V^2$ $V_T = 1V$



Soln From ckt:

$V_G = 2V$ $V_S = 0V$ $V_T = 1V$ (given)

For saturation $V_{DS} \geq V_{GS} - V_T$

$\Rightarrow V_D \geq V_G - V_T$

And current eqn $I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_T)^2$

$I_D = \frac{1}{2}(2)(2-1)^2 = 1mA$

From the figure $I_D = \frac{8 - V_D}{R_D}$

$\Rightarrow I_D R_D = 8 - V_D$

$\Rightarrow V_D = 8 - I_D R_D = 8 - 1(R_D)$

For ~~saturatura~~ saturation mode

$V_D \geq V_G - V_T$

$\Rightarrow 8 - R_D(1m) \geq 2 - 1$ $R_D \leq 7K\Omega$

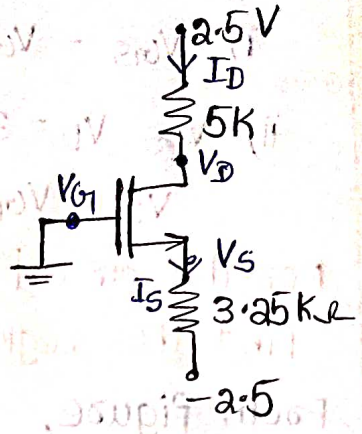
$8 - R_D(1) \geq 1$ $(R_D)_{max} = 7K\Omega$

$8 - 1 \geq R_D(1m)$

$R_D \leq 7K\Omega$

6) Find the region of operation and power dissipation by the transistor.

$I_D = 0.4mA \quad V_T = 0.6V$



Soln From the circuit

$I_D = I_S = 0.4mA, \quad V_{G1} = 0$

$$I_D = \frac{2.5 - V_D}{5K}$$

$$\Rightarrow (5K)(I_D) = 2.5 - V_D$$

$$\Rightarrow V_D = 2.5 - 5(0.4) = 2.5 - 2 = 0.5\ V$$

$$I_S = \frac{V_S - (-2.5)}{3.25K}$$

$$\Rightarrow (3.25K)(I_S) = V_S + 2.5$$

$$\Rightarrow V_S = (3.25K I_S) - 2.5 = (3.25)(0.4) - 2.5 = -1.2V$$

$$V_{GS} = V_{G1} - V_S = 0 - (-1.2) = 1.2V$$

$$V_{DS} = V_D - V_S = 0.5 - (-1.2) = 1.7V$$

i) $V_{GS} = 1.2 > V_T \Rightarrow$ MOSFET is ON

ii) $V_{DS} = 1.7 \qquad V_{GS} - V_T = 1.2 - 0.6 = 0.6$

$V_{DS} > V_{GS} - V_T \Rightarrow$ saturation mode

Power dissipation $= V_{DS} I_D = 1.7 \times (0.4mA) = 0.68\ mW$

Region of operation P-channel Enhancement MOSFET :-

i) $V_{sg} < |V_t|$ OFF (cut off mode)

ii) $V_{sd} < V_{sg} - |V_t|$ Linear / triode / ohmic region

iii) $V_{sd} \geq V_{sg} - |V_t|$ saturation region.

7) calculate the value of current in case of N mos for the parameters

$V_{TN} = 0.75\,V$ $W = 40\mu m$ $L = 4\mu m$ $\mu_n = 650\ cm^2/V\text{-}sec$ $t_{ox} = 450\,A^\circ$

$\epsilon_r = 3.9$ $V_{GS} = 2V_{TN}$ and NMOS is in saturation.

soln We knew that current eqn for saturation mode

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_{TN})^2$$

C_{ox} (capacitance per unit area) $= \dfrac{\epsilon_{ox}}{t_{ox}} = \dfrac{8.85\times10^{-14}\times3.9}{450\times10^{-8}}\ F/cm^2$

$\epsilon_o = 8.85\times10^{-12}\ F/m$ $\epsilon_{ox} = \epsilon_r\epsilon_o$

$= 8.85\times10^{-14}\ F/cm$

$t_{ox} = 450\,A^\circ = 450\times10^{-8}\ cm$

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L} = \frac{1}{2}\left(650\ \frac{cm^2}{V\cdot sec}\right)\times\left(\frac{8.85\times10^{-14}\times3.9}{450\times10^{-8}}\right)\left(\frac{40\,\mu m}{4\,\mu m}\right) = 2.49\times10^{-4}$$

$$I_D = 2.49\times10^{-4}\left(2(0.75)-0.75\right)^2$$

$$I_D = 2.49\times10^{-4}\times0.75^2$$

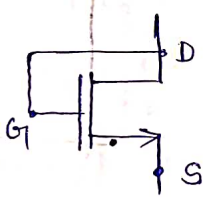
$$I_D = 1.400\times10^{-4}\,A = 0.14\ mA$$

8) The drain of n-channel MOSFET is shorted to gate so that $V_{GS} = V_{DS}$. If threshold voltage of MOSFET is 1V and $I_D = 1mA$; for $V_{GS} = 2V$ then what will be I_D if $V_{GS} = 3V$?

soln Given that,

1) $V_{GS} = V_{DS} = 2V$ $I_D = 1\,mA$

And $V_T = 1V$



$\Rightarrow V_{DS} = 2V$

$V_{GS} - V_T = 2-1 = 1V$

$V_{DS} > V_{GS} - V_T \Rightarrow$ saturation

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_T)^2$$

$$\Rightarrow 1m = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(2-1)^2$$

$$\Rightarrow \mu_n C_{ox}\frac{W}{L} = 2\ mA/V^2$$

when $V_{GS} = 3V$

$$\Rightarrow I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_T)^2 = \frac{1}{2}\times2\times(3-1)^2 = 4\,mA$$

When gate & drain are short circuited, MOSFET will be in saturation region.

9) When the V_{GS} of a MOSFET with $V_T = 400\,mV$ working in saturation is 900 mV, drain current is 1mA. If the channel length modulation is neglected and assuming saturation value of I_D when $V_{GS} = 1400\,mV$?

Soln Given $V_T = 400\,mV = 0.4V$

$V_{GS1} = 900\,mV = 0.9V$ | $V_{GS2} = 1400\,mV = 1.4mV$

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS1} - V_T)^2 \qquad I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS2} - V_T)^2$$

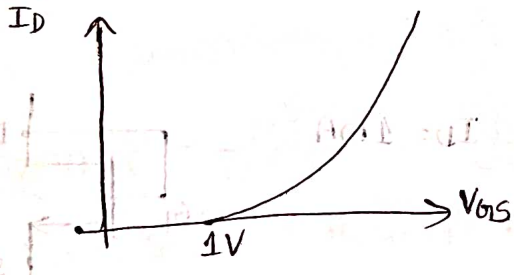
$$\frac{I_{D1}}{I_{D2}} = \frac{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS1} - V_T)^2}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS2} - V_T)^2}$$

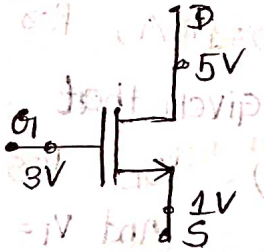
$$\frac{1mA}{I_{D2}} = \frac{(0.9-0.4)^2}{(1.4-0.4)^2}$$

$$\frac{1mA}{I_{D2}} = \left(\frac{0.5}{1}\right)^2$$

$$I_{D2} = \frac{1mA}{0.25} = 4mA$$

10) For nmos and its transfer curve shown in figure. Find Threshold voltage, region of operation.





Soln From transfer curve $V_T = 1V$ and from MOSFET,

$V_G = 3V \quad V_D = 5V \quad V_S = 1V$

$V_{GS} = 3 - 1 = 2V$

$V_{DS} = 5 - 1 = 4V$

$V_{GS} - V_T = 2 - 1 = 3V$

$V_{DS} > V_{GS} - V_T \Rightarrow$ saturation region

11) calculate the value of source to drain voltage to bias p-mos in saturation region.

$K_p = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right) = 0.2\ mA/V^2$ $I_D = 0.5mA$ & $V_{TP} = -0.5V$

soln since mosFET is to be biased in saturation

$V_{sg} > |V_t|$ and $V_{ds} \geq V_{sg} - |V_t|$

$I_D = K_p (V_{sg} - |V_t|)^2$

$\Rightarrow I_D = 0.2m(V_{sg} - 0.5)^2$

$\Rightarrow \frac{0.5m}{0.2m} = (V_{sg} - 0.5)^2$

$\Rightarrow 5 = 2(V_{sg} - 0.5)^2$

$\Rightarrow 5 = 2[V_{sg}^2 + 0.25 - V_{sg}]$

$\Rightarrow 2V_{sg}^2 - 2V_{sg} + 0.5 - 5 = 0$

$\Rightarrow 2V_{sg}^2 - 2V_{sg} - 4.5 = 0$

$V_{sg} = 2.08\ V$

$V_{sd} \geq V_{sg} - |V_{tp}|$

$V_{sd} \geq 2.08 - 0.5$

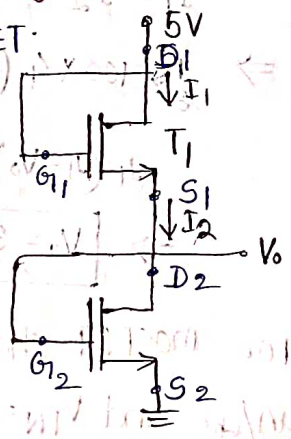
$V_{sd} \geq 1.58\ V$

$(V_{sd})_{min} = 1.58\ V$

*** 12) If both transistors T_1 & T_2 have threshold voltage of 1V. If device parameters K_1 & K_2 for T_1 & T_2 are 36μA/V² and 9μA/V², then find output voltage V_o

soln T_1, T_2 are N-channel Enhancement mosFET.

since Gate & drain are short circuited both mosFET's are in saturation



For mosFET-1

$V_{G_1} = 5$ $V_{S1} = V_o$

$I_{D_1} = K_1\left[(5 - V_o) - 1\right]^2$

For mosFET 2:-

$I_{D_2} = K_2\left[(V_o - 0) - 1\right]^2$

$I_{D_1} = I_{D_2}$ (from figure)

$\Rightarrow K_1\left[4 - V_o\right]^2 = K_2\left[V_o - 1\right]^2$

$\Rightarrow 36\mu(4 - V_o)^2 = 9\mu(V_o - 1)^2$

$\Rightarrow 4(V_o^2 + 16 - 8V_o) = (V_o^2 + 1 - 2V_o)$

$\Rightarrow 4V_o^2 + 64 - 32V_o = V_o^2 + 1 - 2V_o$

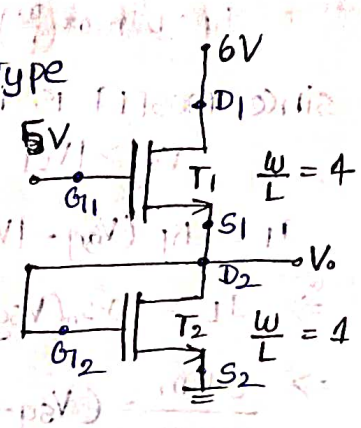
$\Rightarrow 3V_o^2 - 30V_o + 63 = 0$

$\Rightarrow V_o^2 - 10V_o + 21 = 0$

$V_o = 7V$

$V_o = 3V$ is suitable.

13) In the circuit shown below for mos : $\mu_n C_{ox} = 100\,\mu A/V^2$ and $V_T = 1V$. What is the value of V_o at source of upper transistor ?



Soln Both are n-channel Enhancement Type mosFETs.

T_a is in saturation mode.

$$I_a = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS_2} - V_T)^2$$

$$I_2 = \frac{1}{2} \times 100 \times (V_o - 1)^2\ \mu A \longrightarrow (1)$$

$$V_{G_1S_1} = V_{G_1} - V_{S_1} = 5 - V_o$$

$$V_{D_1V_{S_1}} = V_{D_1} - V_{S_2} = 6 - V_o$$

$V_{D_1} = 6V$ $[V_{G_1} = 5,\ V_{S_1} V_T = 1]$

$V_{D_1} = 6 > V_{G_1} - V_T \Rightarrow T_1$ is also in saturation.

$$\Rightarrow I_1 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{G_1S_1} - V_T)^2$$

$$\Rightarrow I_1 = \frac{1}{2} \times 100 \times (4)(5 - V_o - 1)^2 \longrightarrow (2)$$

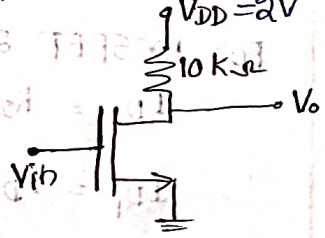
$$I_1 = I_2$$

$$\Rightarrow \frac{1}{2} \times 100 \times 4\,(5 - V_o - 1)^2 = \frac{1}{2} \times 100 \times (V_o - 1)^2$$

$$4(4 - V_o)^2 = (V_o - 1)^2$$

$$\Rightarrow \boxed{V_o = 3V}$$

*** 14) For mosFET shown in figure $\frac{W}{L} = 2$, $V_{DD} = 2V$, $\mu_n C_{ox} = 100\ \mu A/V^2$ and $V_{TN} = 0.5V$. Transistor m_1 switches from saturation to linear if value of V_{in} is



Soln saturation :

$$V_{DS} \geq V_{GS} - V_T$$

Linear $V_{DS} < V_{GS} - V_T$

Boundary of both regions :

$$V_{DS} = V_{GS} - V_T$$

$V_{DS} = V_o - 0 = V_o$ | $V_T = 0.5\,V$

$V_{GS} = V_{in} - 0 = V_{in}$

For saturation

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_T)^2$$

$$I_D = \frac{1}{2}\times 100 \times 2 \times (V_{in}-0.5)^2\ \mu A$$

From figure $I_D = \frac{2-V_o}{10K}$

$$\Rightarrow \frac{2-V_o}{10K} = 100\times(V_{in}-0.5)^2\times 10^{-6}$$

$$\Rightarrow 2-V_o = 10^2\times(V_{in}-0.5)^2\times 10^{-6}\times 10^4$$

$$\Rightarrow 2-V_o = V_{in}^2+0.25-V_{in}$$

$$\Rightarrow V_{in}^2-V_{in}+V_o-1.75=0$$

for edge of linear & saturation

$$V_{DS} = V_{GS}-V_T$$

$$\Rightarrow V_o = V_{in}-0.5$$

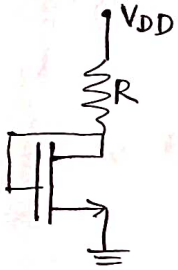
$$\Rightarrow V_{in}^2-V_{in}+V_{in}-0.5-1.75=0$$

$$\Rightarrow V_{in}^2 = 2.25$$

$$\Rightarrow V_{in} = \pm\sqrt{2.25}$$

$V_{in} = \sqrt{2.25} = 1.5V$

15) For n mos transistor shown in figure $V_T = 0.8V$. Neglect channel length modulation effect; when $V_D = 1.6V$ the I_D was found to be 0.5 mA. If V_D is adjusted to be 2V by changes R and V_{DD}, the new value of I_D (in mA) is ——



Soln MOSFET is in saturation region.

$V_{D_1} = V_{G_1} = 1.6V \quad V_S = 0 \quad V_T = 0.8V$

$V_{D_2} = V_{GS_2} = 2V \quad V_S = 0$

$$\frac{I_{D1}}{I_{D2}} = \frac{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS_1}-V_T)^2}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS_2}-V_T)^2}$$

$$\frac{0.5m}{I_2} = \frac{(1.6-0.8)^2}{(2-0.8)^2}$$

$$\frac{0.5m}{I_2} = \left(\frac{0.8}{1.2}\right)^2$$

$$\frac{0.5m}{I_2} = \left(\frac{2}{3}\right)^2$$

$$\frac{0.5m}{I_2} = \frac{4}{9}$$

$$0.5m\times 9 = 4I_2$$

$$I_2 = \frac{9}{4}\times 0.5\,m$$

$$I_2 = 1.125\ mA$$

16) The slope of I_D V/S V_{GS} curve of an NMOS in linear region is 10^{-3}/mho at $V_{DS} = 0.1$ V for same device neglecting channel length modulation slope of $\sqrt{I_D}$ V/S V_{GS} in $\sqrt{A}/V$ under saturation is approximately ——

soln In Linear region

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$\frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \left(\frac{W}{L}\right) V_{DS} = 10^{-3}$$

$$\mu_n C_{ox} \frac{W}{L} = \frac{10^{-3}}{0.1} = 0.01$$

For saturation

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

$$I_D = \frac{1}{2} \times 0.01 \times (V_{GS} - V_T)^2$$

$$\sqrt{I_D} = \sqrt{\frac{0.01}{2}} \times (V_{GS} - V_T)$$

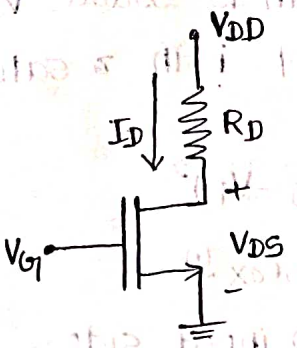
$$\frac{\partial \sqrt{I_D}}{\partial V_{GS}} = \sqrt{\frac{0.01}{2}} (1) = 0.0707$$

Biasing in MOS Circuits

DC biasing :-

1) DC load line :-

Consider the following MOSFET circuit.



Assume that given Nmos transistor is in saturation.

If Nmos in the saturation region, the drain to source ~~voltage~~ current is given by

$$I_D = K_n [V_{GS} - V_t]^2$$

where $K_n = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)$

By applying KVL on output loop,

$$-V_{DD} + R_D I_D + V_{DS} = 0$$

$$V_{DS} = V_{DD} - R_D I_D$$ represents a straight line and this is also called load line equation.

x-intercept :

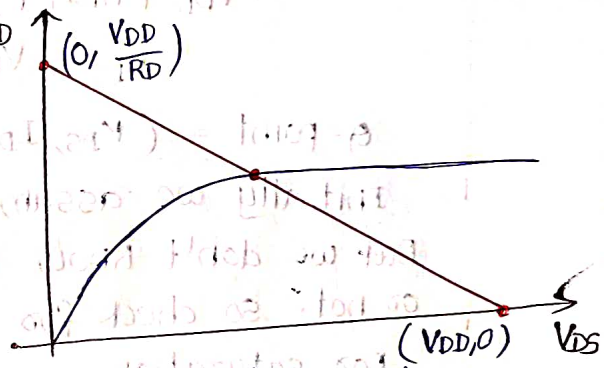
When $I_D = 0$

$\Rightarrow V_{DS} = V_{DD}$

y intercept

When $V_{DS} = 0$

$\Rightarrow I_D = \frac{V_{DD}}{R_D}$



By plotting load line & device characteristics, both are intersect at a point called operating point / Q-point.

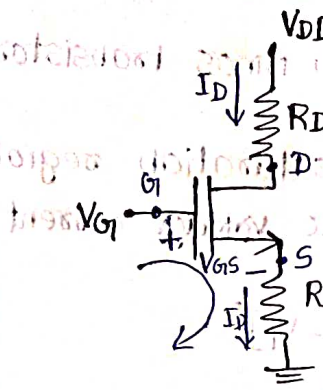
Biasing :-

We need to bias the transistor in such a way that the transistor should be in saturation mode.

(Here, transistor refers to MOSFET).

Biasing Techniques :-

1) Fixed Bias configuration :-



We need to find output drain to source current & drain to source voltage.

Assume MOSFET is in saturation region.

$$\Rightarrow I_D = K_n (V_{GS} - V_T)^2$$

$$K_n = \frac{1}{2} \mu_n C_{ox} \frac{W}{L}$$

Applying KVL on input side :-

$$-V_G + V_{GS} + R_S I_D = 0$$

$$I_D = \frac{V_G - V_{GS}}{R_S}$$

Now applying KVL on output side :-

$$-V_{DD} + R_D I_D + V_{DS} + R_S I_D = 0$$

$$V_{DS} = V_{DD} - I_D (R_S + R_S)$$

Q-point = (V_{DS}, I_D)

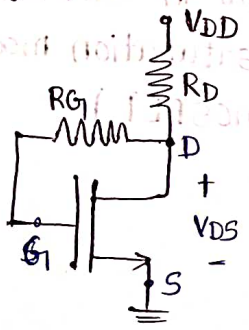
Initially we assumed MOSFET is in saturation mode. But we don't know MOSFET is actually in saturation or not. so check for saturation.

For saturation:

1) $V_{GS} > V_T$

2) $V_{DS} \geq V_{GS} - V_T$

2) Drain to Gate feedback resistance :-



since the gate is connected to drain, it confirms that MOSFET is in saturation region.

$$\Rightarrow I_D = K_n (V_{GS} - V_T)^2$$

$$K_n = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)$$

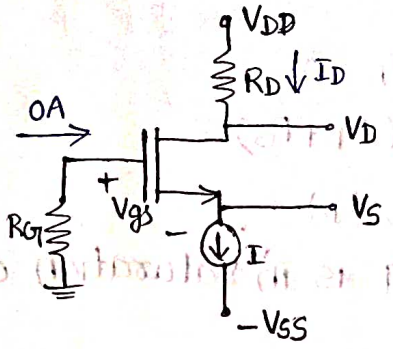
Apply KVL on o/p loop :-

$$-V_{DD} + R_D I_D + V_{DS} = 0$$

$$V_{DS} = V_{DD} - R_D I_D$$

Q-point = (V_{DS}, I_D)

3) constant current biasing :-



From the figure

$V_{GS} = V_G - V_S = -V_S$

$I_D = I$

Assume saturation mode.

$I_D = K_n (V_{GS} - V_T)^2$

where $K_n = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)$

$I_D = I = K_n (V_{GS} - V_T)^2$

$I = K_n (-V_S - V_T)^2$

$I = K_n (V_S + V_T)^2$

From above eqn we can obtain value of V_S.

From output side :

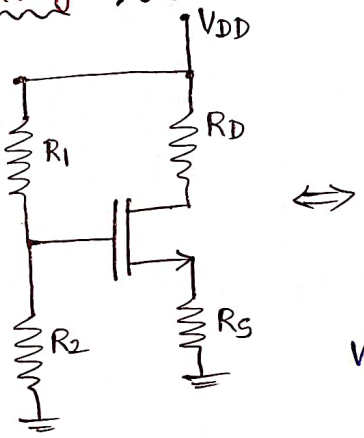
$$I_D = \frac{V_{DD} - V_D}{R_D}$$

$$\Rightarrow V_D = V_{DD} - I_D R_D$$

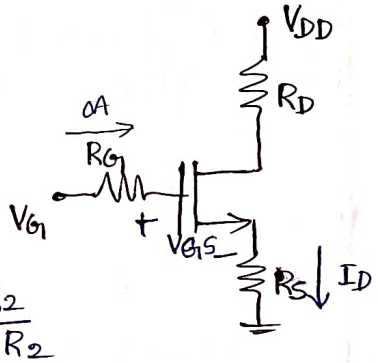
Now drain to source voltage :

$$V_{DS} = V_D - V_S$$
$$= V_{DD} - I_D R_D - V_S$$

4) voltage divider bias :-



Thevenin's equivalent ckt :-



$$V_G = \frac{V_{DD} \times R_2}{R_1 + R_2}$$

$$R_G = \frac{R_1 R_2}{R_1 + R_2}$$

Assume transistor is in saturation mode :-

$\Rightarrow I_D = K_n (V_{GS} - V_T)^2$ where $K_n = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)$

By KVL on input loop :-

$$-V_G + V_{GS} + R_S I_D = 0$$

$$V_{GS} = V_G - R_S I_D$$

$\Rightarrow I_D = K_n (V_{G1} - R_S I_D - V_T)^2$

Applying KVL on o/p side :-

$-V_{DD} + R_D I_D + V_{DS} + R_S I_D = 0$

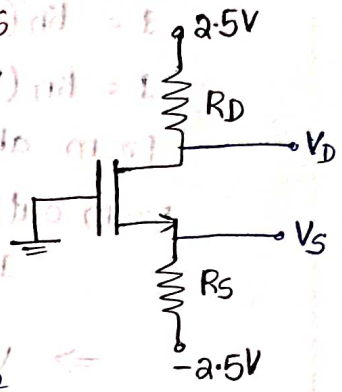
$V_{DS} = V_{DD} - I_D (R_D + R_S)$

operating point $= Q(V_{DS}, I_D)$

verify once gain MOSFET is in saturation or not.

Problems :-

1) Given $I_D = 0.4$ mA, $V_D = 0.5V$, $V_T = 0.7V$, $\mu_n C_{ox} = 100 \mu A/V^2$, $L = 1\mu m$ and $W = 32\mu m$. Find R_D & R_S



soln $\mu_n C_{ox} = 100 \mu A/V^2$

$L = 1\mu m \Rightarrow \frac{W}{L} = 32$

$W = 32\mu m$

$\mu_n C_{ox} \left(\frac{W}{L}\right) = 100 \times (32)\ \mu A/V^2$

$= 3200 \frac{\mu A}{V^2} = 3.2\ mA/V^2$

since $I_D = 0.4$ mA.

There are 2 possibilities { Linear region, saturation region.

Assume saturation region

$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_T)^2$

$0.4m = \frac{1}{2} (3.2m) (V_{GS} - 0.7)^2$

$0.4m = 1.6 (V_{GS} - V_T)^2$

$1 = 4 (V_{GS} - V_T)^2$

$4 [V_{GS} - 0.7]^2 = 1$

$4 [V_{GS} + 0.49 - 1.4 V_{GS}] = 1$

$V_{GS} - 1.4 V_{GS} + 0.49 = 0.25$

$V_{GS} - 1.4 V_{GS} + 0.24 = 0$

$V_{GS} = 1.2V$ (OR) $V_{GS} = 0.2V$

i) $V_{GS} = 1.2V$ $V_T = 0.7 \Rightarrow V_{GS} - V_T = 1.2 - 0.7 = 0.5V$

$V_{DS} = V_{GS} - V_T \Rightarrow$ saturation

$V_{GS} = V_G - V_S$

From ckt, $V_G = 0$

$\Rightarrow V_{GS} = -V_S$

$\Rightarrow V_S = -V_{GS} = -1.2V$

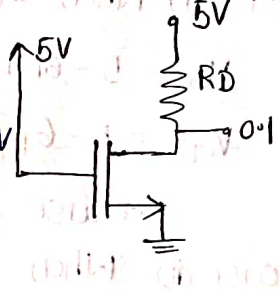
$$I_D = \frac{2.5 - V_D}{R_D}$$

$$\Rightarrow R_D = \frac{2.5 - V_D}{I_D} = \frac{2.5 - 0.5}{0.4mA} = \frac{2}{0.4} = 5K\Omega$$

$$I_D = I_S = \frac{V_S + 2.5}{R_S} = \frac{-1.2 + 2.5}{R_S}$$

$$\Rightarrow R_S = \frac{2.5 - 1.2}{I_D} = \frac{2.5 - 1.2}{0.4m} = \frac{1.3}{0.4m} = 3.25K\Omega$$

2) Given : $V_T = 1V$, $V_D = 0.1V$, $K_n'\left(\frac{W}{L}\right) = 1mA/V^2$ where $K_n' = C_{ox}\mu_n$. Find R_D.



soln Given

$V_G = 5V \quad V_S = 0V \quad V_D = 0.1 \quad V_T = 1V$

$V_{GS} = 5V$

$V_{DS} = 0.1$

$V_{GS} - V_T = 5 - 1 = 4V$

$V_{DS} < V_{GS} - V_T \Rightarrow$ Linear region.

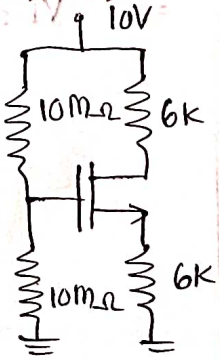
$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$= 1\left[(5-1)(0.1) - \frac{0.1^2}{2}\right] mA.$$

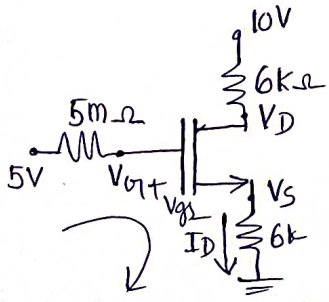
$$I_D = \left[0.4 - \frac{0.01}{2}\right] = 0.395\ mA$$

$$R_D = \frac{5 - 0.1}{I_D} = \frac{5 - 0.1}{0.395m} = 12.4K\Omega$$

3) Given: $V_t = 1V$ $K_n'\left(\frac{W}{L}\right) = 1mA/V^2$. Find I_D, I_S, V_D, V_S.



soln By Thevenin's theorem:



$$V_{Th} = \frac{10 \times 10M}{20M} = 5V$$

$$R_{Th} = \frac{(10m)(10m)}{20m} = 5m\Omega$$

Assume saturation.

KVL at bottom loop :-

$-5 + V_{GS} + 6K I_D = 0$

$V_{GS} = 5 - 6K I_D$

current in saturation:

$$I_D = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2$$

$$I_D = \frac{1}{2}(1m)(5 - 6K I_D - 1)^2$$

$$I_D = \frac{1}{2}(5 - 6I_D - 1)^2$$

$$2I_D = (4 - 6I_D)^2$$

$$\Rightarrow 16 + 36I_D^2 - 48I_D = 2I_D$$

$$\Rightarrow 36I_D^2 - 50I_D + 16 = 0$$

$$I_D = \frac{8}{9}mA \quad \text{or} \quad I_D = \frac{1}{2}mA$$

case (i) When $I_D = \frac{8}{9}mA$

$$V_{GS} = 5 - 6K I_D$$

$$V_{GS} = 5 - 6\left(\frac{8}{9}\right) = \frac{-1}{3} \text{ (Not true)}$$

Because for nNDS $V_{GS} > 0$

case (ii) When $I_D = \frac{1}{2}mA$

$$V_{GS} = 5 - 6K\left(\frac{1}{2}m\right) = 2V$$

$$V_{GS} = V_G - V_S = 2$$

$$V_G = 5V \Rightarrow 5 - V_S = 2$$

$$\boxed{V_S = 3V}$$

$$V_{DS} \geq V_{GS} - V_T \text{ (for saturation)}$$

$$\Rightarrow V_D - V_S \geq V_G - V_S - V_T$$

$$\Rightarrow V_D \geq V_G - V_T$$

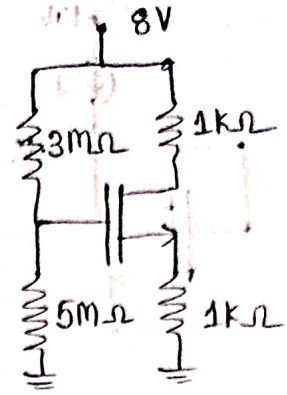
$$\Rightarrow V_D \geq 5 - 1 \qquad (V_D)_{min} = 4V$$

$$\Rightarrow V_D \geq 4V$$



4) Given: $V_t = 1V$, $K_n'\left(\frac{W}{L}\right) = 1mA/V^2$ Find I_D

soln By thevenin's theorem:-

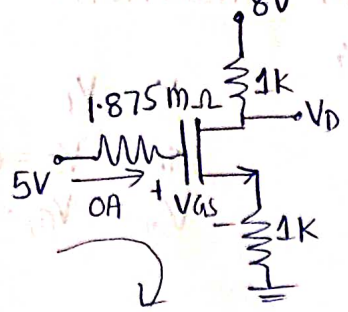


$V_{Th} = \frac{8 \times 5M}{8M} = 5V$

$R_{Th} = 3M \| 5M$

$= \frac{3 \times 5}{8}$

$= 1.875 M\Omega$



By KVL,

$-5 + V_{GS} + 1K\, I_D = 0$

$\Rightarrow V_{GS} = 5 - I_D$

Assume saturation region.

$\Rightarrow I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2$

$\Rightarrow 2I_D = 1(5 - I_D - 1)^2$

$\Rightarrow 2I_D = (4 - I_D)^2$

$\Rightarrow 2I_D = 16 + I_D^2 - 8I_D$

$\Rightarrow I_D^2 - 10I_D + 16 = 0$

$I_D = 8mA$ (OR)

$I_D = 2mA$

case (i) $I_D = 8mA$

$V_{GS} = 5 - 8 = -3V$ (Not True)

case (ii) $I_D = 2mA$

$V_{GS} = 5 - 2 = 3V$

check for saturation:-

$V_{GS} = 3V$

$V_G - V_S = 3V$

$5 - V_S = 3$

$V_S = 2V$

$I_D = \frac{8 - V_D}{1K}$

$I_D = 8 - V_D$

$V_D = 8 - I_D$

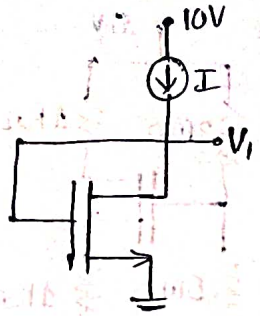
$V_D = 8 - 2 = 6V$

$V_{DS} = 6 - 2 = 4V$

$V_{GS} - V_T = 3 - 1 = 2V$

$V_{DS} > V_{GS} - V_T \Rightarrow$ It confirms saturation region.

5) Given $V_{GS} = 3V$, $V_t = 1V$, $I = 2mA$. Find V_1.



Soln Gate & drain are short circuit
$\Rightarrow$ MOSFET is in saturation.

$\Rightarrow V_{DS} \geq V_{GS} - V_T$

$\Rightarrow V_D \geq V_{GS} - V_T$

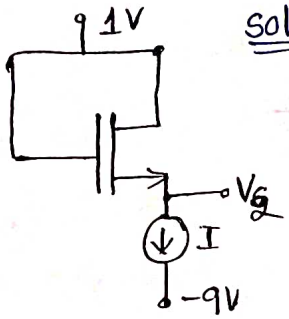
$\Rightarrow V_1 \geq V_G - V_T$

$\Rightarrow V_1 \geq 3 - 1$

$\Rightarrow V_1 \geq 2V$

$V_D = V_1$
since $V_S = 0$
$V_{GS} = V_G = 3V$

6) Given $V_{GS} = 3V$ $V_t = 1V$, $I = 2mA$ Find V_2



Soln $V_G = V_D = 1V$

MOSFET is in saturation

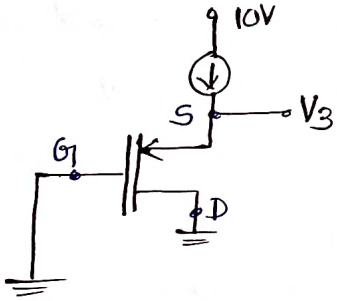
$V_{GS} = 3V$

$V_G - V_S = 3$

$V_G - 3 = V_S$

$V_S = 1 - 3 = -2V$

7) Given : $|V_{GS}| = 3V$, $V_t = -1V$, $I = 2mA$. Find V_3



Soln PMOS Transistor is in saturation.

$|V_{GS}| = 3V$ $V_S = V_3$

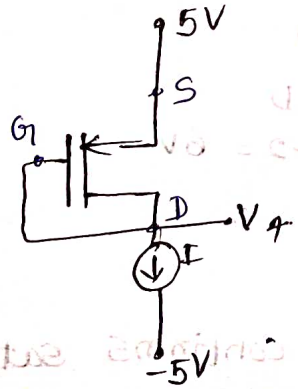
$V_G = 0V$

$-(V_G - V_S) = 3$

$0 + V_3 = 3$

$V_3 = 3V$

8) Given : $V_{GS} = -3V$, $V_t = -1V$ $I = 2mA$ Find V_4



Soln p mos is in saturation

$V_S = 5V$

$V_D = V_G$

$V_{SG} = 3$

$V_S - V_G = 3$

$V_G = V_S - 3 = 5 - 3 = 2V$

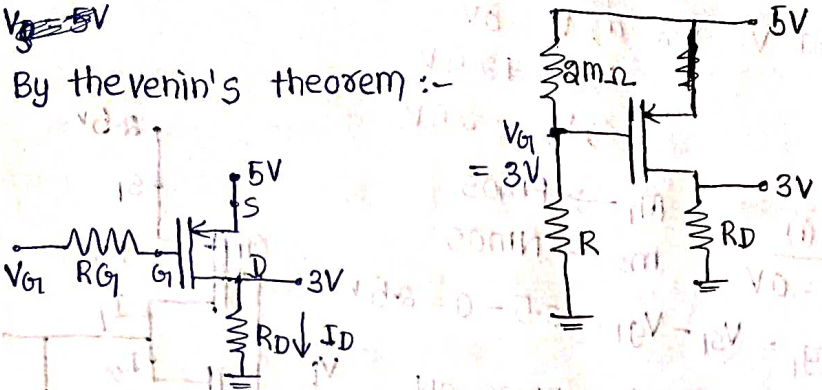
$V_4 = V_D = V_G = 2V$

9) Given : $K_p'\left(\frac{W}{L}\right) = 1\ mA/V^2$, $V_t = -1V$, $I_D = 0.5\ mA$. Find R, D.

Soln

$V_g = 5V$

By thevenin's theorem :-



$V_S = 5V$ $V_D = 3V$

$I_D = \frac{3}{R_D}$

$R_D = \frac{3}{I_D} = \frac{3}{0.5m} = 6\ K\Omega$

Assume saturation region:

$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(|V_{GS}| - |V_t|)^2$

$= \frac{1}{2}(1)\left(V_{SG_1} - |V_{tp}|\right)^2$

$= \frac{1}{2}(5 - V_{G_1} - 1)^2$

$0.5m = \frac{1}{2}(4 - V_{G_1})^2$

$1 = 16 + V_{G_1}^2 - 8V_{G_1}$

$V_{G_1}^2 - 8V_{G_1} + 15 = 0$

$V_{G_1} = 3V$ or $V_{G_1} = 5V$

i) when $V_{G_1} = 3V$

$V_{sg} = V_S - V_{G_1} = 5 - 3 = 2V$

$V_{sg} > |V_{tp}|$ $\Rightarrow$ condition satiespied

Then $V_{sd} = V_S - V_d = 5 - 3 = 2V$

$V_{sd} = V_{sg} - |V_t|$ $\Rightarrow$ saturation

By voltage division

$V_{G_1} = \frac{5R}{2+R}$

$\Rightarrow 3 = \frac{5R}{2+R}$

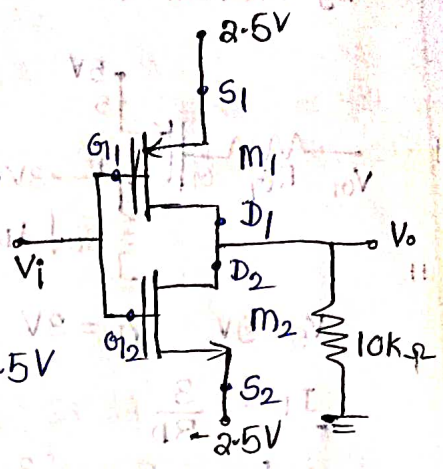
$\Rightarrow 6 + 3R = 5R$

$R = 3m\Omega$

$\Rightarrow$

10) Given: $(K_n)'\left(\frac{W}{L}\right) = (K_p)'\left(\frac{W}{L}\right) = 1\frac{mA}{V^2}$, $V_{tn} = 1V$, $V_{tp} = -1V$.

Find V_o for a) $V_i = 0V$
b) $V_i = +2.5V$
c) $V_i = -2.5V$



Soln

case (i) $V_i = 0V$ — $M_1 \rightarrow$ PMOS, $M_2 \rightarrow$ NMOS

$V_{S_1G_1} = V_{S_1} - V_{G_1} = 2.5 - 0 = 2.5V$

$V_{S_1G_1} > |V_{tp}| \Rightarrow$ PMOS ON

$V_{G_2S_2} = V_{G_2} - V_{S_2} = 0 + 2.5 = 2.5V$

$V_{G_2S_2} > V_{tn} \Rightarrow$ NMOS ON

Assume both MOSFETs are in saturation.

$\Rightarrow I_{D_1} = I_{D_2}$

$I_{D_1} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)\left(V_{S_1G_1} - |V_{tp}|\right)^2 = \frac{1}{2} \times 1 \times (2.5-1)^2$

$I_{D_1} = 1.125\ mA$

Since $I_{D_1} = I_{D_2} \Rightarrow I_{10k\Omega} = 0$

$\Rightarrow V_o = 0V$

$\Rightarrow V_{D_1} = V_{D_2} = 0$

$V_{S_1D_1} = V_{S_1} - V_{D_2} = 2.5V$

$V_{S_1G_1} - |V_{tp}| = 2.5 - 1 = 1.5V$

$V_{S_1D_1} > V_{S_1G_1} - |V_{tp}| \Rightarrow M_1$ confirms in saturation.

$V_{D_2S_2} = V_{D_2} - V_{S_2} = 0 - (-2.5) = 2.5V$

$V_{SG_2S_2} = |V_{tn}| = 2.5 - 1 = 1.5V$

$V_{D_2S_2} > V_{G_1S_1} - V_{tn} \Rightarrow M_2$ confirms in saturation.

case (ii) $V_i = 2.5V \Rightarrow V_{g_1} = V_{g_2} = 2.5V$

$V_{S_1g_1} = V_{S_1} - V_{g_1} = 2.5 - 2.5 = 0V$

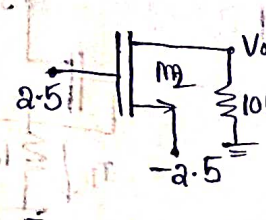
$V_{S_1g_1} < |V_{tp}| \Rightarrow$ PMOS OFF

$V_{g_2S_2} = V_{g_2} - V_{S_2} = 2.5 - (-2.5) = 5V$

$V_{g_2S_2} > V_{tn} \Rightarrow$ NMOS ON

Assume NMOS in saturation region.

m_1 OFF



Here $V_D = V_o$ = -ve and hence

$V_{DS} \neq V_{GS} - V_T \Rightarrow$ Linear region.

From ckt $I_D = \frac{-V_o}{10K}$

We knew that for linear region

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS}-V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] = \frac{-V_o}{10}$$

$V_{DS} = V_D - V_S = V_o - (-2.5) = V_o + 2.5$. $V_{GS} = V_G - V_S = 5V$

$$\Rightarrow I_D = 1\left[(5-1)(V_o+2.5) - \frac{(V_o+2.5)^2}{2}\right] = \frac{-V_o}{10K}$$

$$\Rightarrow 4(V_o+2.5) - \frac{1}{2}(V_o^2 + 6.25 + 5V_o) = \frac{-V_o}{10}$$

$$\Rightarrow 4V_o + 10 - 0.5V_o^2 - 3.125 - 2.5V_o = -0.1V_o$$

$$\Rightarrow -0.5V_o^2 + 1.6V_o + 6.875 = 0$$

$$0.5V_o^2 - 1.6V_o - 6.875 = 0$$

$V_o = 5.638\,V \quad V_o = -2.438\,V$

$V_o = -2.438$ V is valid.

case (iii) $V_i = -2.5V$ $V_{G1} = V_{G2} = -2.5V$

$V_{S1G1} = V_{S1} - V_{G1} = 2.5 - (-2.5) = 5V$

$|V_{tp}| = 1V$

$|V_{S1G1}| > |V_{tp}| \Rightarrow$ pmos ON

$V_{G2S2} = V_{G2} - V_{S2} = -2.5 + 2.5 = 0V$

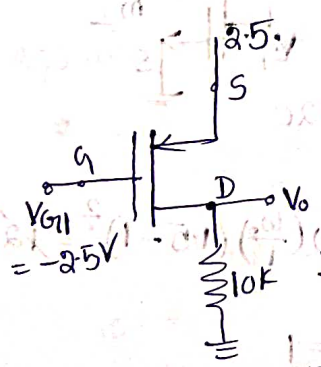
$V_{G2S2} < V_{tn} \Rightarrow$ NMOS OFF

~~$V_{G2S2} < |V_{tp}|$~~

$V_{SG1} - V_T = V_o + 2.5 - 1 > 2.5$

$V_{SD} = V_S - V_D < 2.5$

$\Rightarrow V_{SD} \neq V_{SG1} - V_T \Rightarrow$ Linear



Assume linear region:-

$$I_D = \mu_p C_{ox} \frac{W}{L}\left[(V_{SG_1} - |V_t|)(V_{SD}) - \frac{V_{SD}^2}{2}\right]$$

$$I_D = 1\left[(5-1)(2.5-V_o) - \frac{(2.5-V_o)^2}{2}\right] = \frac{V_o}{10K}$$

$$\Rightarrow 4(2.5-V_o) - \frac{1}{2}(V_o - 2.5)^2 = \frac{V_o}{10}$$

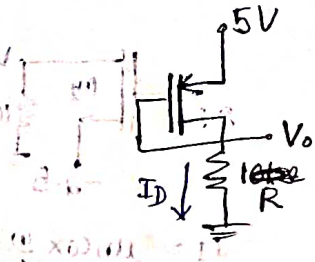
$$\Rightarrow 10 - 4V_o - 0.5V_o^2 - 3.125 + 2.5V_o = 0.1V_o$$

$$\Rightarrow +6.875 - 0.5V_o^2 - 1.6V_o = 0$$

$$\Rightarrow 0.5V_o^2 + 1.6V_o - 6.875 = 0$$

$V_o = 2.438\,V$ ✓

11) Given: $V_t = -0.7V$ $\mu_p C_{ox} = 60\,\mu A/V^2$ $L = 0.8\,\mu m$ $I_D = 115\,\mu A$
$V_D = 3.5V$. Find W, R



Soln Gate & drain are short circuited
$\Rightarrow$ PMOS is in saturation region

$I_D = \frac{V_o}{R}$ $\quad V_o = V_D = 3.5$

$R = \frac{V_o}{I_D}$

$R = \frac{3.5}{0.115\,m} = 30.4K\Omega$

$I_D = \frac{K_p}{2}(V_{GS} - |V_T|)^2$

$\frac{115}{115} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)(3.5 - 0.7)^2$

$115 = \frac{1}{2} \times 60 \times \frac{W}{0.8}(7.84)$

$W = \frac{115 \times 0.8}{30 \times 7.84}$

$V_{G1} = V_D = 3.5$

$I_D = \frac{K_{p1}}{2}(V_{SG1} - |V_T|)^2$

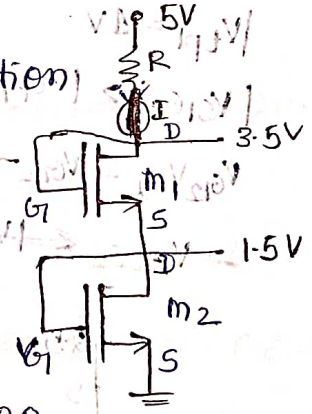
$115 = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_S - V_{G1} - |V_t|)^2$

$115 = \frac{1}{2} \times 60 \times \frac{W}{0.8}(5 - 3.5 - 0.7)^2$

$115 = \frac{1}{2} \times 60 \times \frac{W}{8} \times 6.4$

$W = \frac{115 \times 8 \times 2}{60 \times 6.4} = 4.79\,\mu m$

12) Given $V_t = 1V$, $K_n' = 120\,\mu A/V^2$ $I = 120\,\mu A$ $L_1 = L_2 = 1\,\mu m$
Find W_1, W_2, R



Soln Both MOSFETs m_1, m_2 are in saturation

$\Rightarrow I_{D1} = I_{D2} = I$

$I_{D1} = I_{D2}$

$\Rightarrow \frac{1}{2}\mu_n C_{ox}\left(\frac{W_1}{L_1}\right)(V_{GS1} - V_T)^2 =$

$\frac{1}{2}\mu_n C_{ox}\left(\frac{W_2}{L_2}\right)(V_{GS2} - V_T)^2 = 120$

$\Rightarrow \frac{1}{2}(120)\left(\frac{W_1}{1}\right)(3.5 - 1.5 - 1)^2 = \frac{1}{2}(120)\left(\frac{W_2}{1}\right)(1.5 - 1)^2 = 120$

$\Rightarrow \frac{1}{2}W_1(1)^2 = 1 \Rightarrow \frac{1}{2}W_2(0.5)^2 = 1$

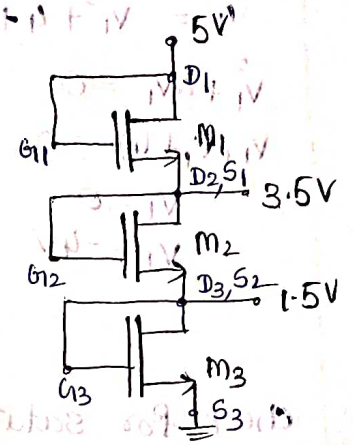
$\boxed{W_1 = 2\,\mu m} \Rightarrow W_2 = \frac{2}{0.25} = 8\,\mu m$

$$I_D = \frac{5-3.5}{R}$$

$$R = \frac{5-3.5}{I_D} = \frac{1.5}{0.12m} = 12.5K\Omega$$

13) Given: $V_t = 1V$ $K_n' = 120\mu A/V^2$ $L_1 = L_2 = L_3 = 1\mu m$ $I = 120\mu A$.

Find W_1, W_2, W_3.



Soln

$V_{G_1S_1} = 5 - 3.5 = 1.5V$

$V_{G_2S_2} = 3.5 - 1.5 = 2V$

$V_{G_3S_3} = 1.5V$

m_1, m_2, m_3 are in saturation.

$I_1 = I_2 = I_3 = 120\mu A$

$$I_1 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W_1}{L_1}\right)(V_{G_1S_1} - V_T)^2 = 120$$

$$\Rightarrow \frac{1}{2}(120)\left(\frac{W_1}{1}\right)(1.5-1)^2 = 120$$

$$W_1 = \frac{2}{0.5^2} = \frac{2}{0.25} = 8\mu m$$

$$I_2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W_2}{L_2}\right)(V_{G_2S_2} - V_T)^2 = 120$$

$$\Rightarrow \frac{1}{2}(120)\left(\frac{W_2}{1}\right)(2-1)^2 = 120$$

$$W_2 = 2\mu m$$

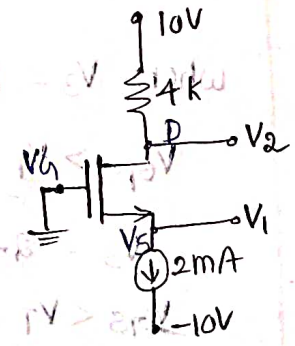
$$I_3 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W_3}{L_3}\right)(V_{G_3S_3} - V_T)^2 = 120$$

$$\Rightarrow \frac{1}{2}(120)\left(\frac{W_3}{1}\right)(1.5-1)^2 = 120$$

$$W_3 = \frac{2}{0.5^2} = \frac{2}{0.25} = 8\mu m$$

14) Given $|V_t| = 2V$, $K_n\left(\frac{W}{L}\right) = 1mA/V^2$ Find V_1 & V_2.

Soln Assume MOSFET is under saturation.



$$I = \frac{10 - V_2}{4k}$$

$$2m = \frac{10 - V_2}{4k}$$

$$10 - V_2 = 8$$

$$V_2 = 2V_2$$

$$V_{GS} = V_G - V_S = 0 - V_S$$

$$V_{GS} = -V_1$$

$$V_{DS} = V_D - V_S = V_2 - V_1 = 2 - V_1$$

For saturation

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2$$

$$2 = \frac{1}{2} \times 1 \times (-V_1 - 2)^2$$

$$4 = V_1^2 + 4 + 4V_1$$

$$V_1^2 + 4V_1 = 0$$

$$V_1(V_1 + 4) = 0$$

$$V_1 = 0$$

$$V_1 = -4V$$

case (i) $V_1 = 0 \Rightarrow V_S = 0$

$V_{GS} = V_G - V_S = 0V$

$V_{GS} < V_{th} \Rightarrow$ MOSFET OFF

$V_1 = 0$ is invalid

case (ii) $V_1 = -4V$ $V_S = -4V$

$V_{GS} = V_G - V_S = 0 - (-4) = 4V$

$V_{GS} > |V_{tn}|$ NMOS ON

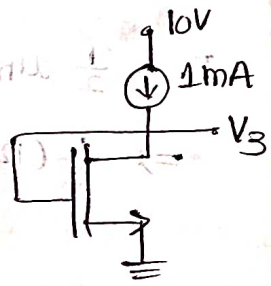
check for saturation:

$V_{DS} = V_D - V_S = 2 - 2 = 0V$

$V_{GS} - V_T = V_G - V_S - V_T = 4 - 2 = 2V$

$V_{DS} > V_{GS} - V_T \Rightarrow$ It is in saturation.

15) Given: $|V_t| = 2V$ $k_n'\left(\frac{W}{L}\right) = 1mA/V^2$ Find V_3.



soln It is in saturation.

$V_{G1} = V_D = V_3$ $V_S = 0V$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)^2$$

$$1m = \frac{1}{2}(1)(V_3 - 2)^2$$

$$2 = V_3^2 + 4 - 2V_3$$

$$V_3^2 - 2V_3 + 2 = 0$$

$$(V_3 - 2)^2 = 2$$

$$V_3 = \pm\sqrt{2} + 2$$

$$V_3 = 2 \pm \sqrt{2}$$

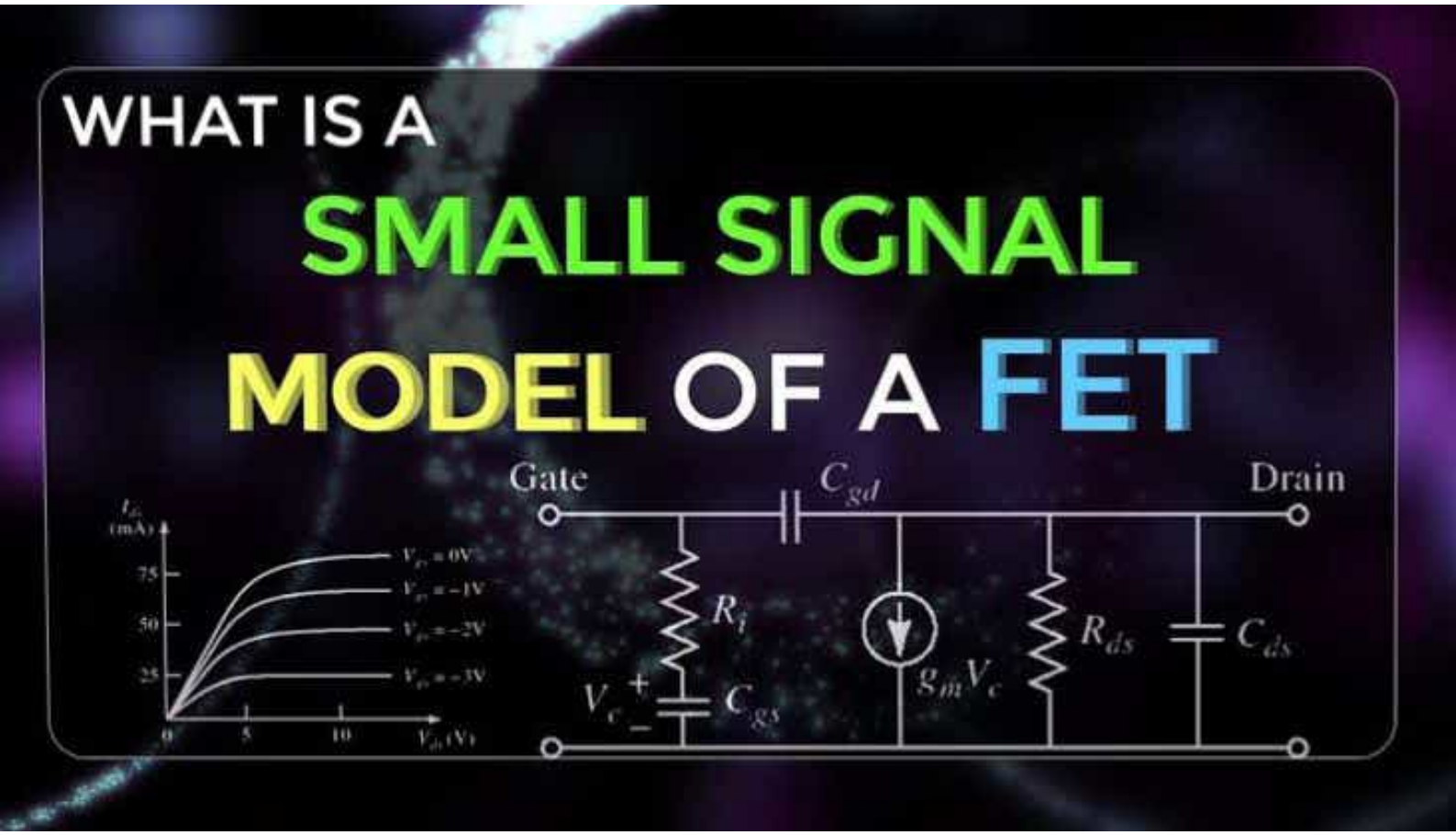
when $V_3 = 2 + \sqrt{2} = 3.414V$

$V_{GS} > V_T \Rightarrow$ satisfied

$V_3 = 2 - \sqrt{2} = 0.585V$

$V_{GS} < V_T \Rightarrow$ NOT satisfied

$\Rightarrow \boxed{V_3 = 3.414V}$


WHAT IS A
SMALL SIGNAL
MODEL OF A FET
Gate
Drain
C_{gd}
R_i
C_{gs}
V_c
$g_m V_c$
R_{ds}
C_{ds}
75
50
25
0
5
10

Small Signal Analysis of MOSFET :-

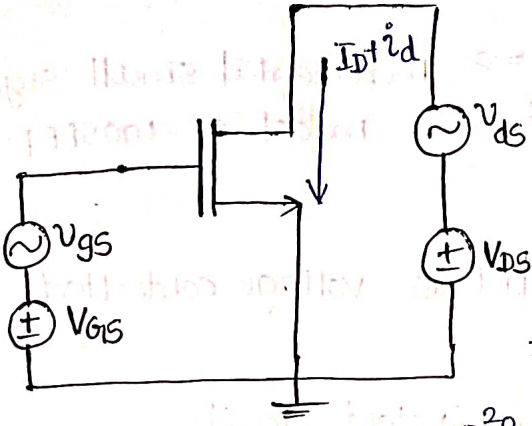
We knew that

drain current $I_{DS} = \mu_n C_{ox} \frac{W}{L}\left((V_{GS}-V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right)$

$\Rightarrow$ I_{DS} is a function of V_{GS}, V_{DS}

$\Rightarrow$ $I_{DS} = I_D = \text{func}^n(V_{GS}, V_{DS})$

consider the following NMOS common source MOSFET circuit.



Now drain current can be represented by

$I_D + i_d = \text{func}^n(V_{GS}+v_{gs}, V_{DS}+v_{ds})$

By taylor series expansion

$I_d + i_d =$

$f(V_{GS},V_{DS}) + \frac{\partial f}{\partial V_{GS}}\cdot v_{gs} + \frac{\partial f}{\partial V_{DS}} v_{ds} + \frac{\partial^2 f}{\partial V_{GS}^2}\cdot\frac{v_{gs}^2}{2} + \text{- - (higher order terms)}$

since v_{gs} & v_{ds} are so small, we can neglect 2nd & higher order terms.

$\Rightarrow$ $I_D + i_d = f(V_{GS}, V_{DS}) + \frac{\partial f}{\partial V_{GS}}\Big|_{I_D}\cdot v_{gs} + \frac{\partial f}{\partial V_{DS}}\Big|_{I_D}\cdot v_{ds}$

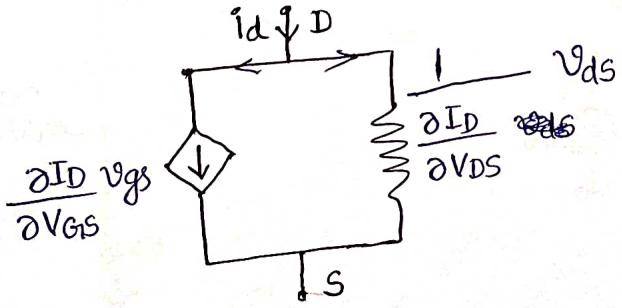
$\therefore$ $I_d = I_D + \frac{\partial I_D}{\partial V_{GS}} v_{gs} + \frac{\partial I_D}{\partial V_{DS}} v_{ds}$

$\Rightarrow$ $I_D + i_d = I_D + \frac{\partial I_D}{\partial V_{GS}} v_{gs} + \frac{\partial I_D}{\partial V_{DS}} v_{ds}$

$i_d = \frac{\partial I_D}{\partial V_{GS}} v_{gs} + \frac{\partial I_D}{\partial V_{DS}} v_{ds}$

i_d ↙ current — sum of 2 currents.

Therefore output of a MOSFET can be modelled as:-



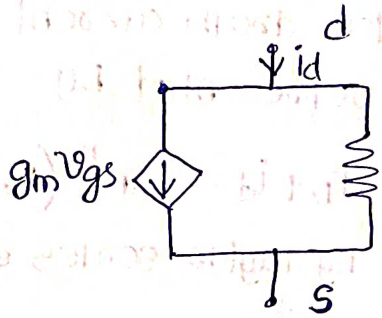
Now transconductance

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

output conductance $g_o = g_{ds} = \frac{\partial I_D}{\partial V_{DS}}$

output resistance $r_o = r_{ds} = \frac{1}{\partial I_D / \partial V_{DS}}$

Now output model can be modified as

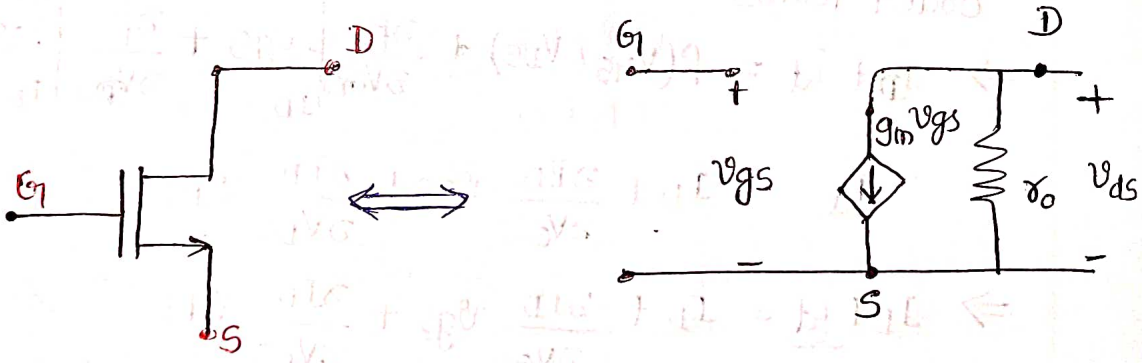


⇒ Incremental small signal model of MOSFET.

Therefore MOSFET can act as voltage controlled controlled source.

complete small signal equivalent circuit.

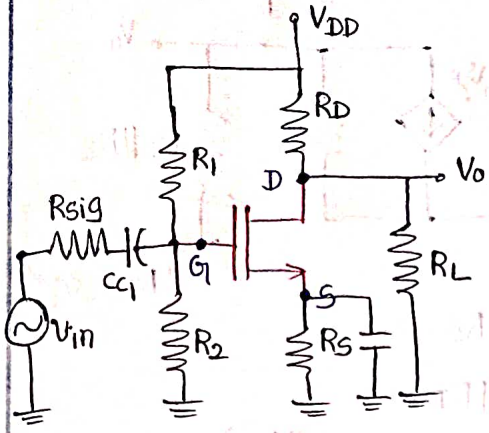
The input to the gate appears as an open circuit due to infinite resistance and output is already modelled above.



single stage MOSFET Amplifiers :—

1) common source Amplifier
2) common drain amplifier
3) common gate amplifier

1. common soure Amplifier :-

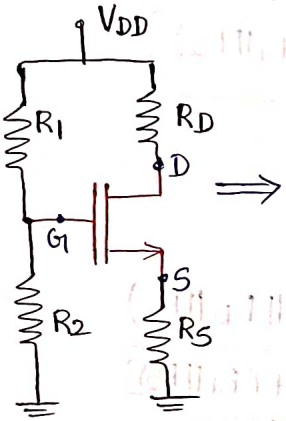


Input : Gate
output : drain
common terminal : source

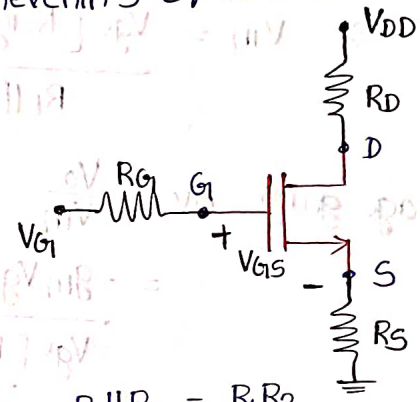
common source Amplifier

DC analysis :-

capacitors : open circuit
ac sources : Nullify



Thevenin's equivalent circuit :-



where $V_{G1} = \frac{V_{DD} R_2}{R_1 + R_2}$ $R_{G1} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$

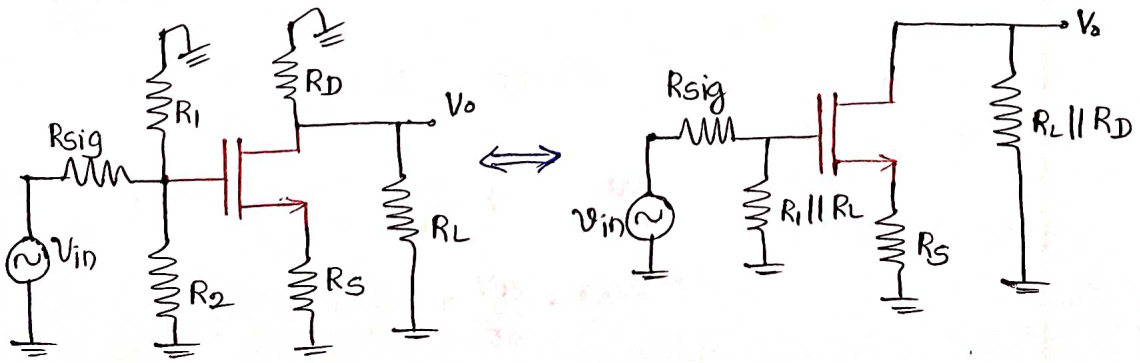
$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$ (Assume mosFET is in saturation)

Transconductance $g_m = \sqrt{2 I_D \mu_n C_{ox} \left(\frac{W}{L}\right)}$

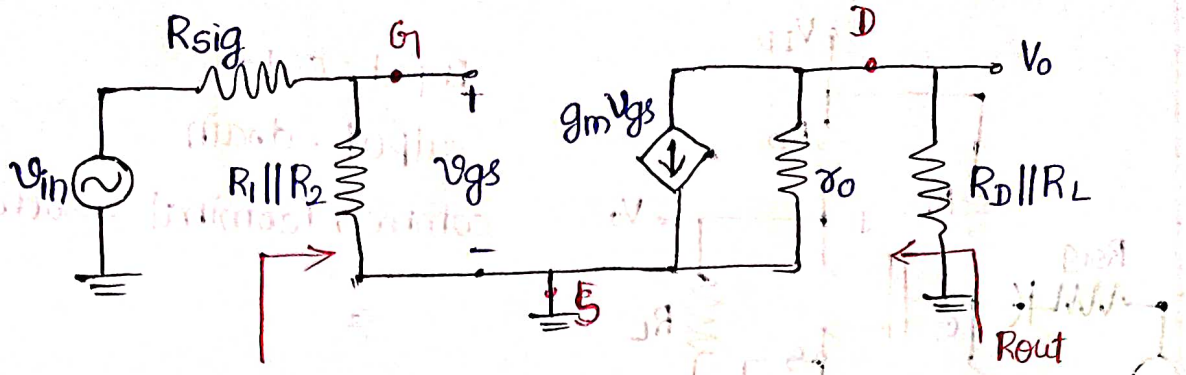
$r_o = \frac{V_A}{I_D}$

ac analysis :-

Thevenin's equivalent circuit :-



small signal equivalent model :-



Input resistance $R_{in} = R_1 \| R_2$

output resistance $R_o = r_o \| R_D$

output voltage $V_o = -g_m v_{gs} (r_o \| R_D \| R_L)$

Applying voltage division :

$$V_{gs} = \frac{v_{in} \times R_1 \| R_2}{R_{sig} + (R_1 \| R_2)}$$

$$\Rightarrow V_{in} = \frac{V_{gs} \left[R_{sig} + (R_1 \| R_2) \right]}{R_1 \| R_2}$$

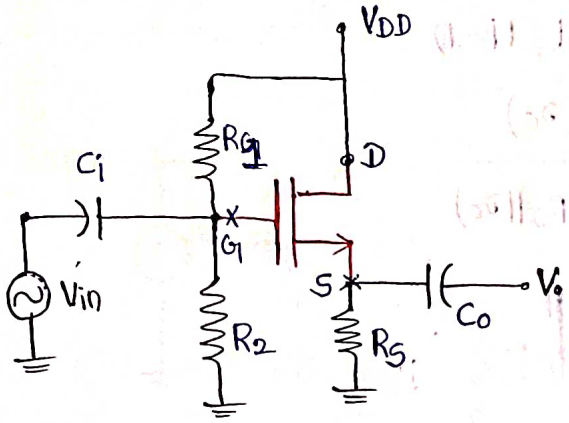
voltage gain $A_V = \frac{V_o}{V_{in}}$

$$= \frac{-g_m V_{gs} (r_o \| R_D \| R_L)}{\frac{V_{gs} \left[R_{sig} + (R_1 \| R_2) \right]}{R_1 \| R_2}}$$

$$A_V = \frac{-g_m (r_o \| R_D \| R_L)(R_1 \| R_2)}{R_{sig} + (R_1 \| R_2)}$$

2. common drain Amplifier

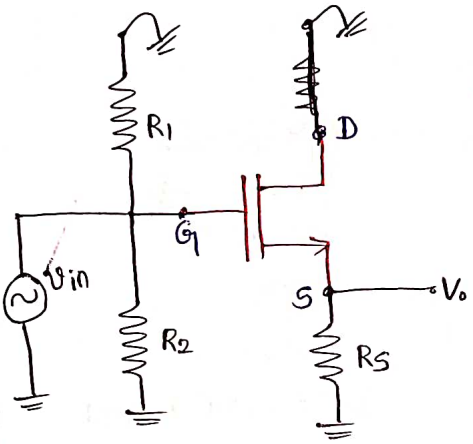
common drain amplifier is also called source follower



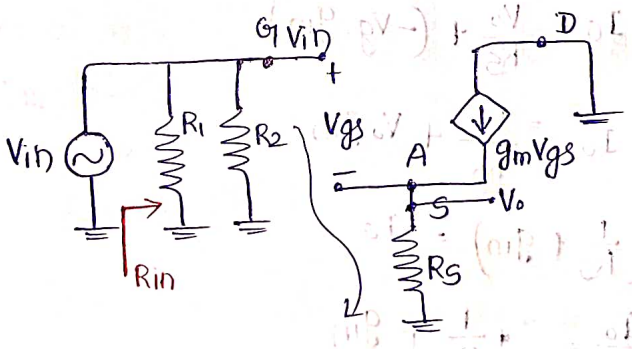
Input : Gate.
output : source
drain is grounded

ac analysis :-

ac equivalent circuit :-



ac equivalent model :-



Input impedance :-

$$R_{in} = R_1 \parallel R_2$$

Voltage gain :-

By KVL, $-V_{in} + V_{gs} + V_o = 0$

$$V_{gs} = V_{in} - V_o$$

KCL @ node A : $g_m V_{gs} = \frac{V_o}{R_S}$

$$\frac{V_o}{R_S} = g_m(V_{in} - V_o)$$

$$\frac{V_o}{R_S} + g_m V_o = V_{in} g_m$$

$$V_o\left(\frac{1}{R_S} + g_m\right) = V_{in} g_m$$

$$A_V = \frac{V_o}{V_{in}} = \frac{g_m}{\frac{1}{R_S} + g_m}$$

$$A_V = \frac{g_m R_S}{1 + g_m R_S}$$

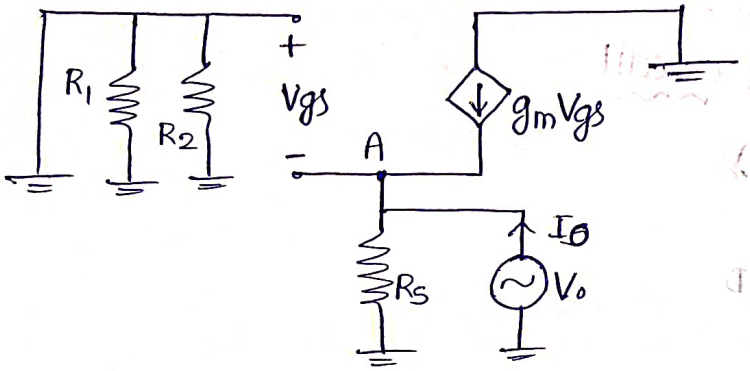
$$A_V = \frac{g_m R_S}{1 + g_m R_S}$$

If r_o is also present then

$$A_V = \frac{g_m (R_S \| r_o)}{1 + g_m (R_S \| r_o)}$$

output impedance:

$$R_o = \frac{V_o}{I_o}$$



From the ckt :-

$$V_{gs} = -V_o$$

KCL @ node A :

$$I_o + g_m V_{gs} = \frac{V_o}{R_S}$$

$$I_o = \frac{V_o}{R_S} + (-V_{gs} g_m)$$

$$I_o = \frac{V_o}{R_S} + V_o g_m$$

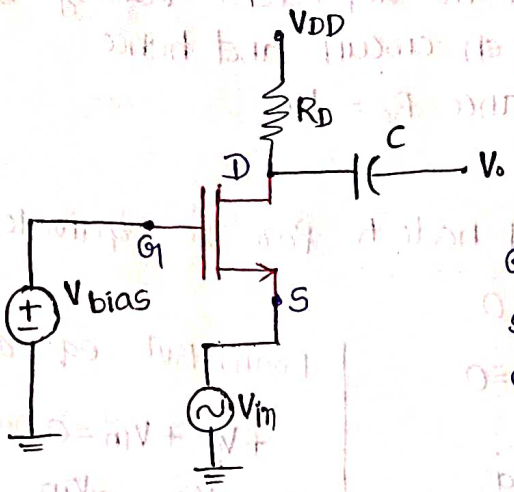
$$V_o \left(\frac{1}{R_S} + g_m\right) = I_o$$

$$\frac{I_o}{V_o} = \frac{1}{R_S} + g_m$$

$$\frac{1}{z_o} = \frac{1}{R_S} + \frac{1}{1/g_m}$$

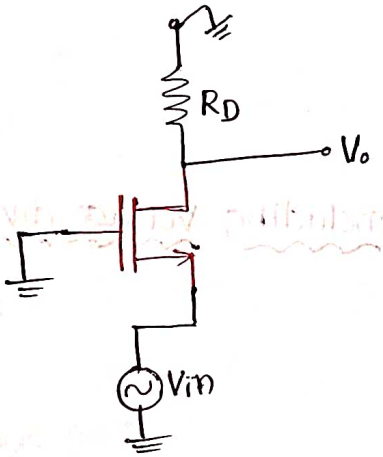
$$\Rightarrow z_o = (R_S \| 1/g_m)$$

#3 common gate amplifier :-

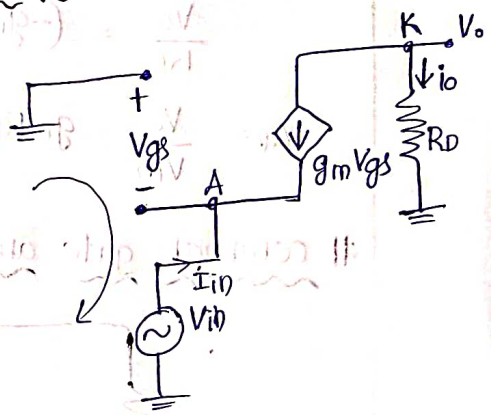


Gate is grounded
source : i/p
drain : o/p

ac equivalent circuit :-



ac equivalent circuit model :-



Input impedance :-

By KVL on input side,

$+V_{gs} + V_{in} = 0$

$V_{in} = -V_{gs} \rightarrow (1)$

By KCL at node A :-

$I_{in} + g_m V_{gs} = 0$

$I_{in} - g_m V_{in} = 0$ (from eq^n 1)

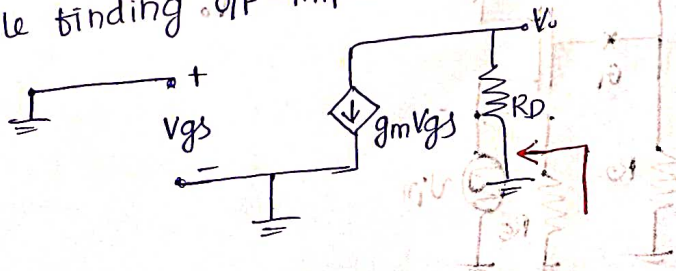
$I_{in} = g_m V_{in}$

$\frac{1}{g_m} = \frac{V_{in}}{I_{in}}$

$R_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{g_m}$

output impedance :-

While finding o/p impedance nullify the source.



When source is nullified then $V_{gs} = 0$ that implies the voltage $V_{gs} = 0$ and the dependent ~~voltage~~ ∞ current source become open circuit and hence

output impedance $R_o = R_D$

voltage gain :-

Applying KCL at node K for ac equivalent model :-

$\Rightarrow i_o + g_m V_{gs} = 0$

$\Rightarrow \frac{V_o}{R_D} + g_m V_{gs} = 0$

$\frac{V_o}{R_D} = -g_m V_{gs}$

$\frac{V_o}{R_D} = (-g_m)(-V_{in})$

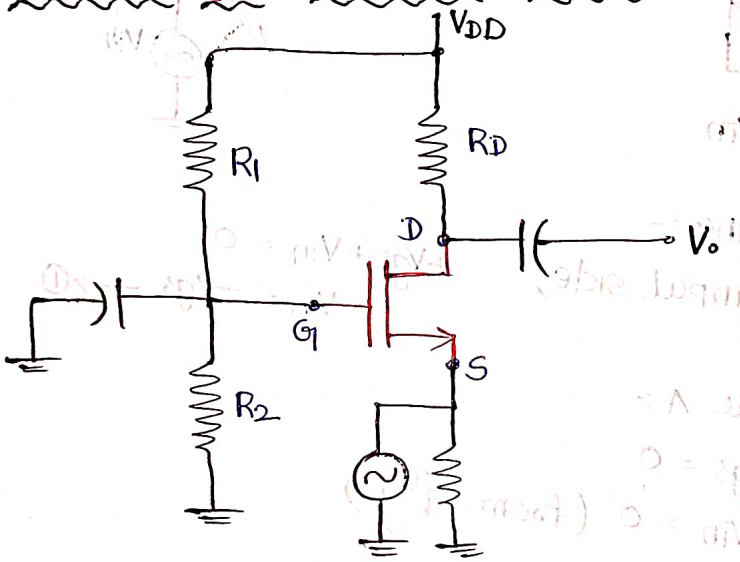
$A_v = \frac{V_o}{V_{in}} = g_m R_D$

From KVL eqn. of i/p side :-

$+V_{gs} + V_{in} = 0$

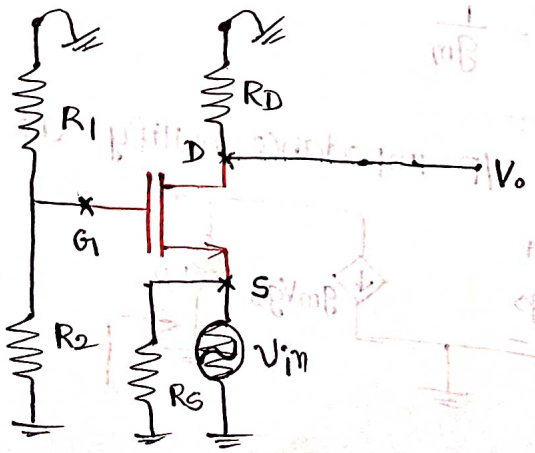
$V_{gs} = -V_{in}$

common gate amplifier including voltage division circuit :-

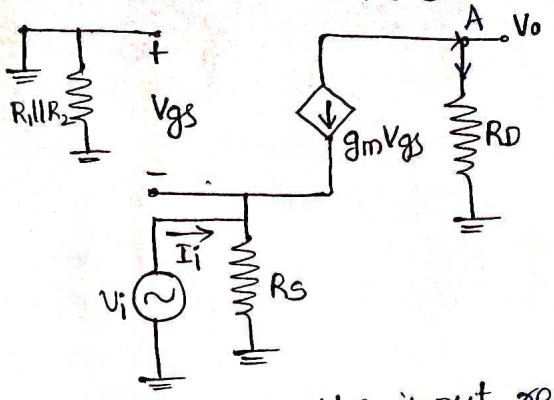


small signal analysis :-

ac equivalent ckt :-



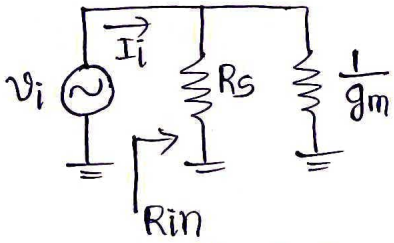
small signal equivalent circuit :-



Without Rs resistance, the input resistance Rin is $\frac{1}{g_m}$.
Now in addition to $\frac{1}{g_m}$ we have Rs.

∴ Input resistance :-

$$R_{in} = R_s \,||\, \frac{1}{g_m}$$



output impedance :

$$R_{out} = R_D$$

voltage gain :-

By KCL at node A :

$$\frac{V_o}{R_D} + g_m V_{gs} = 0$$

and from input KVL we have

$$V_{in} = -V_{gs}$$

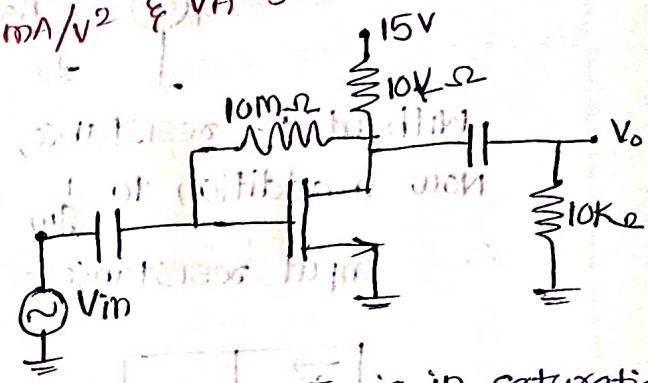
$$\frac{V_o}{R_D} = -g_m V_{gs}$$

$$\frac{V_o}{R_D} = g_m V_{in}$$

$$\frac{V_o}{V_{in}} = g_m R_D$$

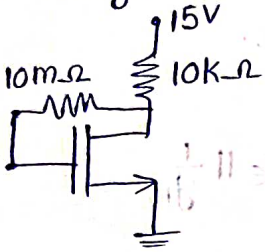
Problems

1) For the given circuit (common source Amplifier), the largest allowable input signal magnitude is _____. Assume that at the operating signal frequency, the capacitors act as short circuit. The following are the MOSFET parameters. $V_T = 1.5\,V$, $\mu_n C_{ox}\left(\frac{W}{L}\right) = 0.25\,mA/V^2$ & $V_A = 50\,V$



Soln

DC analysis :-



From the circuit it is clear that MOSFET is in saturation region.

Applying KVL to o/p loop :-

$$-15 + 10K\,I_D + V_{DS} = 0$$

$$V_{DS} = 15 - 10K\,I_D$$

$$V_G = V_D \Rightarrow V_{GS} = V_{DS}$$

$$\Rightarrow V_{GS} = 15 - 10K\,I_D$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2$$

$$= \frac{1}{2} \times 0.25\,(V_{GS} - 1.5)^2$$

$$I_D = \frac{1}{2} \times 0.25\,(15 - 10\,I_D - 1.5)^2$$

$$2\,I_D = \frac{1}{4}(13.5 - 10\,I_D)^2$$

$$8\,I_D = (182.25 + 100\,I_D^2 - 270\,I_D)$$

$$100\,I_D^2 - 278\,I_D + 182.25 = 0$$

$$I_D = 1.72\,mA \quad (OR)$$

$$I_D = 1.058\,mA$$

Now case (i) $I_D = 1.72\,mA$

$$V_{GS} = 15 - 10(1.72) = -ve \quad (Not\ valid)$$

case(ii) $V_{GS} = 15 - 10(1.058)$

$I_D = 1.058\,mA$

$= 4.42V$ (valid)

Therefore $I_D = 1.058\,mA$ &

$V_{GS} = 4.42$ volts

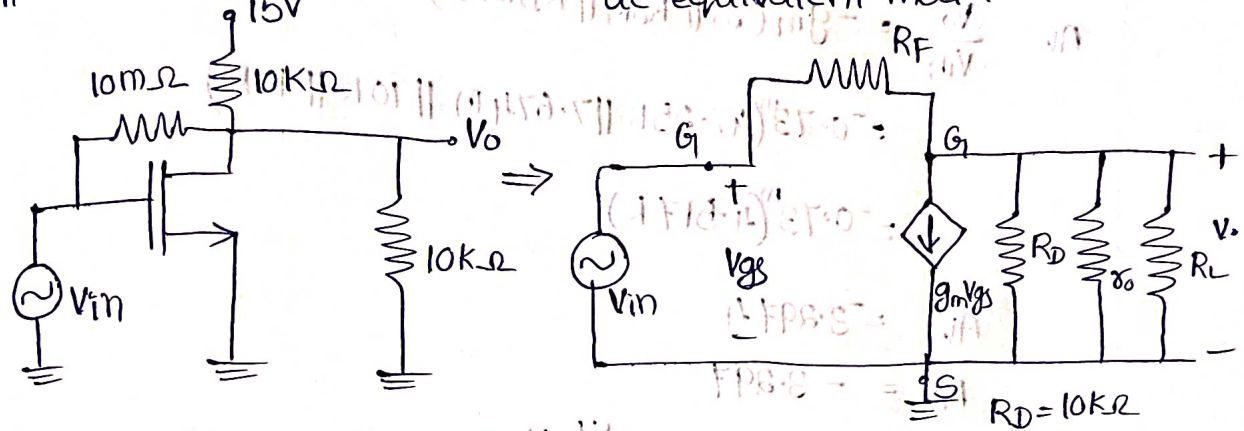
Transconductance $g_m = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)$

$= 0.25(4.42 - 1.5)$

$g_m = 0.73\,mS$

ac analysis :-

ac equivalent model :-



$r_o = \frac{V_A}{I_D} = \frac{50}{1.058} = 47.25\,K\Omega$

voltage gain without feed back resistance :- $A_V = \frac{V_{out}}{V_{in}}$

$V_{out} = -g_m V_{gs}(R_D \| r_o \| R_L)$

$A_V = \frac{V_{out}}{V_{gs}} = -g_m(R_D \| r_o \| R_L)$ $(V_{gs} = V_{in})$

$= -0.73(10K \| 47.25 \| 10K)$

$= -0.73(4.52k)$

$A_V = -3.2996$

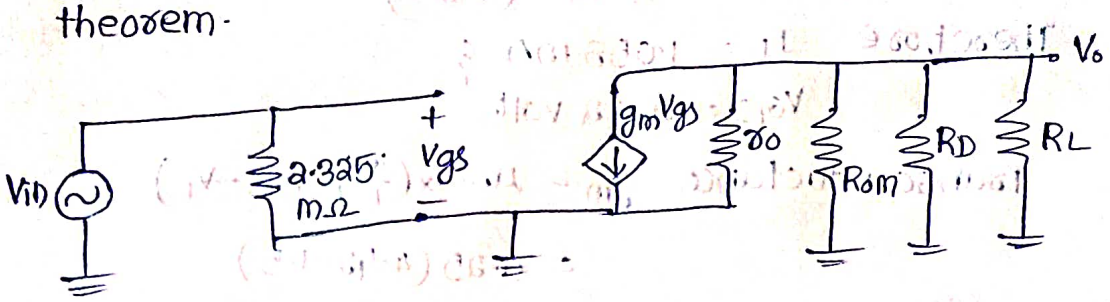
since due to presence of feed back resistance we need to apply miller's theorem.

By miller's theorem.

$R_{im} = \frac{R_f}{1 - A_V} = \frac{10}{1 - (-3.2996)}\,M\Omega = 2.325\,M\Omega$

$R_{om} = \frac{R_f}{1 - \frac{1}{A_V}} = \frac{10}{1 - \frac{1}{-3.2996}} = 7.674\,M\Omega$

Now redrawing ac equivalent circuit using miller's theorem.



$V_o = -g_m V_{gs} (r_o \| R_{om} \| R_D \| R_L)$ $\quad (V_{in} = V_{gs})$

$A_V = \frac{V_o}{V_{in}} = -g_m (r_o \| R_{om} \| R_D \| R_L)$

$= -0.73^m (47.25K \| 7.674M \| 10K \| 10K)$

$= -0.73^m (4.517K)$

$A_V = -3.2974$

$A_V = -3.297$

For saturation condition:

$v_{DS} \geq v_{GS} - V_T$

v_{DS} contains 2 components i) dc component V_{DS} & (ii) ac component v_o

v_{GS} consists a components i) dc component V_{GS} & (ii) ac component v_{in}

$\Rightarrow V_{DS} + v_o \geq V_{GS} + V_i - V_T$

$\Rightarrow V_{DS} + [-|A_V| V_{imax}] \geq V_{GS} + V_{imax} - V_T$

we have $V_{DS} = V_{GS}$

$-|A_V| V_{imax} \geq V_{imax} - V_T$

$V_T \geq V_{imax} + |A_V| V_{imax}$

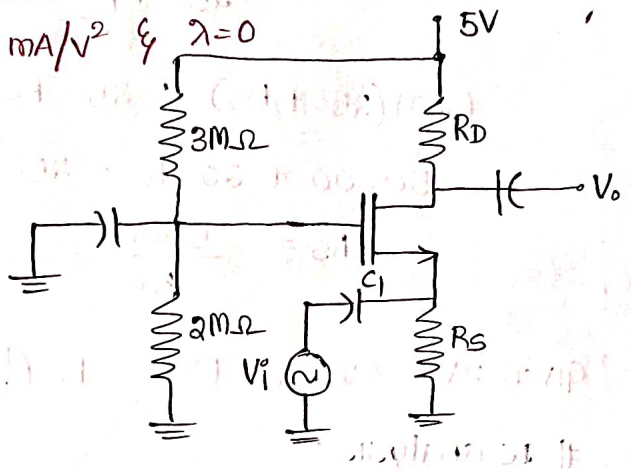
$V_T \geq V_{in}(1 + |A_V|)$

$V_{i(max)} \leq \frac{V_T}{1 + |A_V|}$

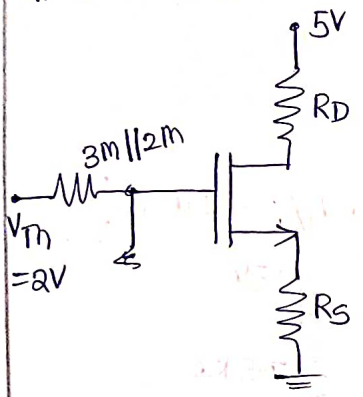
$V_{imax} \leq \frac{1.5}{1 + 3.2974} = 0.349$

$(V_i)_{max} \leq 0.349$ $\quad (V_i)_{max} = 0.349$ volts

2) For the given discrete common gate Amplifier, the voltage gain is 5 and input impedance is 200Ω. The power supplied by the 5V DC voltage is 5mW. The current drawn by voltage divider circuit is negligible. the required value of R_D & R_S to achieve desired voltage gain & input impedance are ____
Assume that at the operating signal frequency the capacitor act as a short circuit.
The following are the MOSFET parameters:
$V_T = 0.5V$, $\mu_n C_{ox}\left(\frac{W}{L}\right) = 8\,mA/V^2$ & $\lambda = 0$



Soln # DC analysis:-



$$V_{th} = \frac{5 \times 2M}{5M} = 2V$$

Given that
power supplied by 5 volts, $P = I_D \times 5$
$\Rightarrow 5mW = I_D \times 5$
$\Rightarrow I_D = 1mA$

For saturation region
$$I_D = \frac{1}{2} \times \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2$$

$\Rightarrow 1 = \frac{1}{2} \times 8 \times (V_{GS} - V_T)^2$

$\Rightarrow \frac{1}{4} = (V_{GS} - V_T)^2$

$\Rightarrow V_{GS} - V_T = \frac{1}{2}$

$$g_m = \frac{2I_D}{V_{GS} - V_T} = \frac{2 \times 1}{1/2} = 4\,mS$$

Given voltage $A_V = 5$
We knew that voltage gain of common gate amplifier
$A_V = g_m R_D$
$R_D = \frac{A_V}{g_m} = \frac{5}{4m} = 1.25\,K\Omega$

Input impedance of common gate Amplifier.

$$R_{in} = \frac{1}{g_m} \| R_S$$

$$R_{in} = \frac{1}{4m} \| R_S$$

$$200 = \frac{250 R_S}{250 + R_S}$$

$$200(250 + R_S) = 250 R_S$$

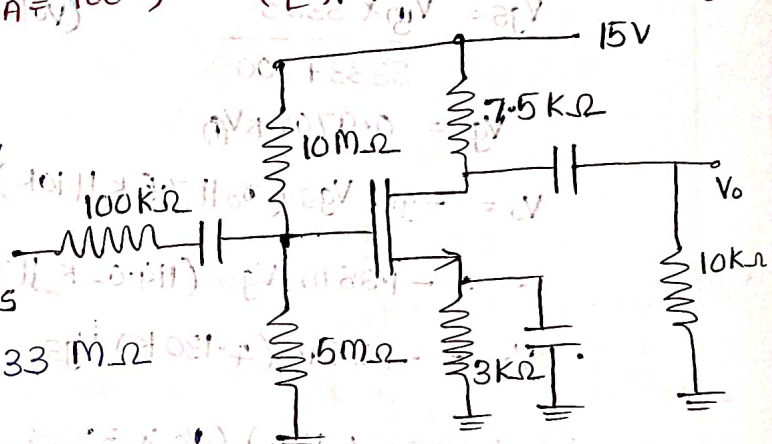
$$1000 + 4R_S = 5R_S$$

$$R_S = 1K\Omega$$

2) Given $V_t = 1V$, $V_A = 100V$, $K_n'\left(\frac{W}{L}\right) = 2 mA/V^2$ Find $\frac{V_o}{V_s}$

Soln

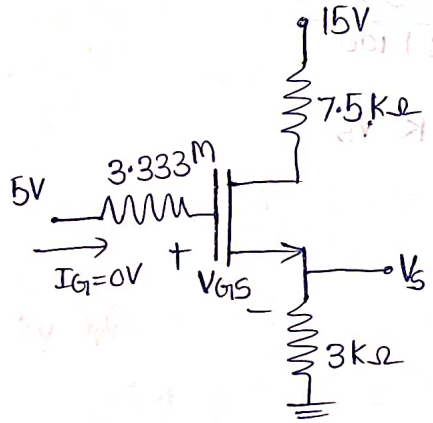
DC analysis :-



$$V_{G1} = \frac{15 \times 5M}{15M} = 5V$$

$$R_{G1} = 10m \| 5m$$

$$R_{G1} = \frac{10 \times 5}{15} = 3.333\ M\Omega$$



$$V_{GS} = V_{G1} - V_S$$

$$V_{GS} = 5 - 3I_D$$

For amplification MOSFET is in saturation

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2$$

$$I_D = \frac{1}{2} \times 2 \times (5 - 3I_D - 1)^2$$

$$I_D = (4 - 3I_D)^2$$

$$I_D = 16 + 9I_D^2 - 24I_D$$

$$9I_D^2 - 25I_D + 16 = 0$$

$$I_D = 1.77\ mA = \frac{16}{9}\ mA$$

$$I_D = 1mA$$

when $I_D = \frac{16}{9}mA$ $V_S = (3K)(\frac{16}{9}m) = \frac{16}{3}V = 5.333V$

$\Rightarrow V_{GS} = V_G - V_S = 5 - 5.333 = -ve$ (Not valid)

when $I_D = 1mA$ $V_S = (3K)(1m) = 3V$

$\Rightarrow V_{GS} = 2V$ and $V_{GS} > V_T$

$V_{DS} = 15 - 7.5K\, I_D$

$= 15 - 7.5(1)$

$V_{DS} = 7.5\,V$

$\Rightarrow V_{GS} - V_T = 3 - 1 = 2V$

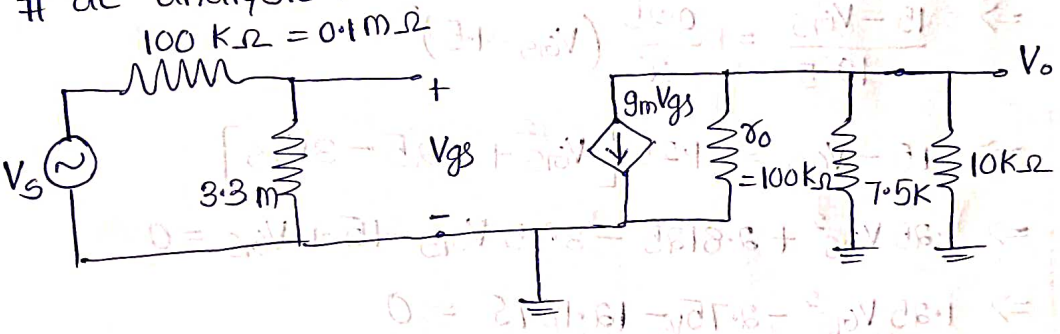
$V_{DS} > V_{GS} - V_T$.

$\Rightarrow$ It confirms mosFET is in saturation.

$$g_m = \frac{2I_D}{V_{GS} - V_T} = \frac{2 \times 1m}{2-1} = 2mA/V$$

$$r_o = \frac{V_A}{I_D} = \frac{100}{1mA} = 100K\Omega$$

ac analysis :-



$$V_{gs} = \frac{V_S \times 3.3m}{3.3m + 0.1m} = V_S\left(\frac{3.3}{3.4}\right) = 0.9705\,V_S$$

$$V_o = -g_m V_{gs}(100K \,||\, 7.5K \,||\, 10K)$$

$$= -(2m)(0.9705\,V_S)(4.109K)$$

$$\frac{V_o}{V_S} = -2 \times 0.9705 \times 4.109$$

$$\frac{V_o}{V_S} = -7.975$$

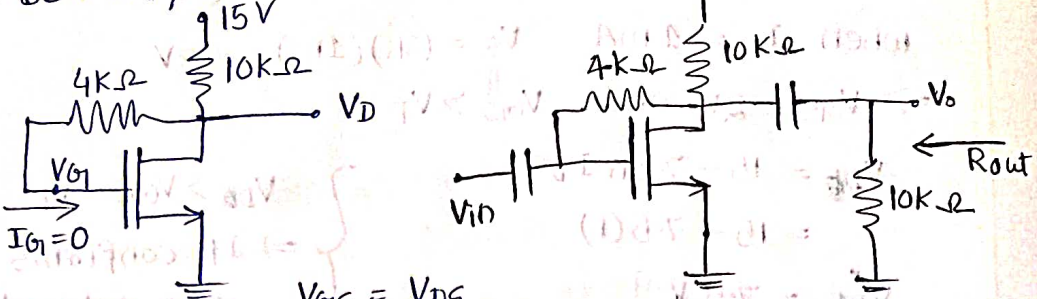
$R_{in} = 3.3\,m\Omega$

$R_{out} = 100K \,||\, 7.5K = 6.976\,K\Omega$

4) Given $V_t = 1.5V$ $V_A' = 50V$ $K_n'\left(\frac{W}{L}\right) = 0.25\,mA/V^2$ Find R_{out}

Soln

DC analysis:-



$$V_{GS} = V_{DS}$$

$$I_D = \frac{15 - V_{DS}}{10K} = \frac{15 - V_{GS}}{10K}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2$$

$$\Rightarrow \frac{15 - V_{GS}}{10K} = \frac{1}{2} \times 0.25m\,(V_{GS} - 1.5)^2$$

$$\Rightarrow \frac{15 - V_{GS}}{10\,5} = \frac{0.25}{2}(V_{GS} - 1.5)^2$$

$$\Rightarrow 15 - V_{GS} = 1.25\left[V_{GS}^2 + 2.25 - 3V_{GS}\right]$$

$$\Rightarrow 1.25\,V_{GS}^2 + 2.8125 - 3.75\,V_{GS} - 15 + V_{GS} = 0$$

$$\Rightarrow 1.25\,V_{GS}^2 - 2.75\,V_{GS} - 12.1875 = 0$$

$$\Rightarrow V_{GS}^2 - 2.2\,V_{GS} - 9.75 = 0$$

$V_{GS} = 4.410\ V$ (valid)

$V_{GS} = -2.210\ V$ (Not valid)

$$I_D = \frac{15 - V_{GS}}{10K} = \frac{15 - 4.41}{10\,K} = 1.059\ mA$$

$$g_m = \frac{2I_D}{V_{GS} - V_T} = \frac{2 \times 1.059}{4.41 - 1.5} = 0.7278\ mA/V$$

$$r_o = \frac{V_A}{I_D} = \frac{50}{1.059\,m} = 47.21\ K\Omega$$

we need to split the feedback resistance 4KΩ into input side & output side

$$R_{in\,m} = \frac{R_f}{1 - A_V} \qquad R_{out\,m} = \frac{R_f}{1 - \frac{1}{A_V}}$$

where A_V is the voltage gain without feedback resistance.

voltage gain without feedback resistance :-

ac analysis :- (Without Rf)

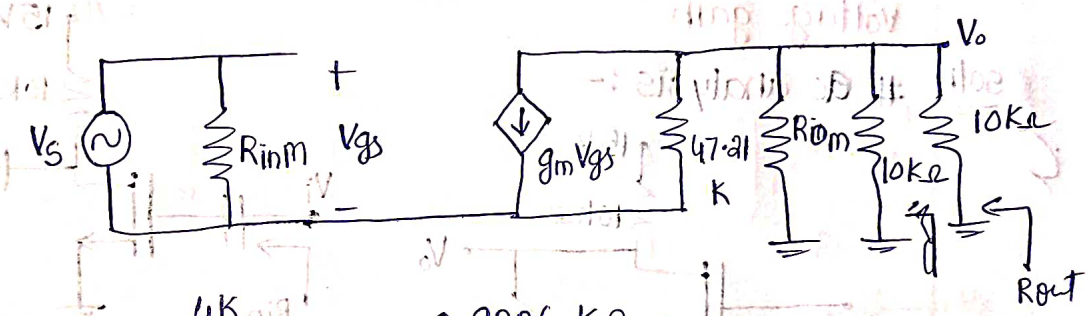


$V_o = -g_m V_{gs} (47.21K \parallel 10K \parallel 10K)$

$V_o = -(0.7278m) V_s (4.52K)$ $(V_{gs} = V_s)$

$A_V = \frac{V_o}{V_s} = -3.289$

ac equivalent circuit including Rf :-



$Rin\,m = \frac{4K}{1+3.289} = 0.9326\ K\Omega$

$Rom = \frac{4K}{1+\frac{1}{3.289}} = 3.067\ K\Omega$

$Rout = (47.21K) \parallel (3.067K) \parallel (10K) \parallel (10K)$

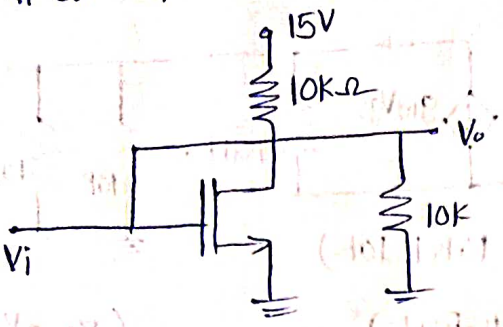
$= (47.21K) \parallel (3.067K) \parallel (5K)$

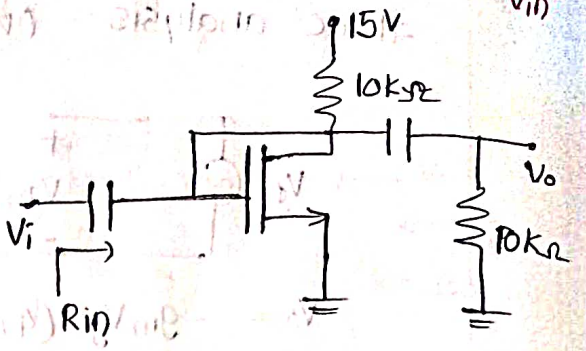
$= (47.21K) \parallel (1.9K)$

$Rout = 1.826\ K\Omega$

5) Given $V_t = 1.5V$, $V_A = 50V$, $K_n'\left(\frac{W}{L}\right) = 0.25\ mA/V^2$. Find $\frac{V_o}{V_{in}}$

soln # ac equivalent circuit :-





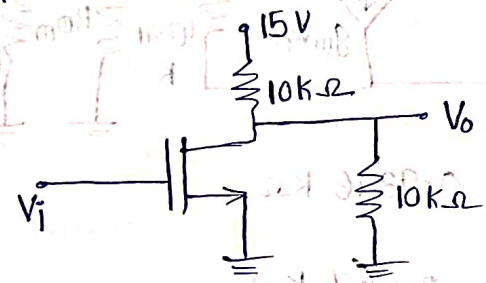
Input is directly shorted to output :-

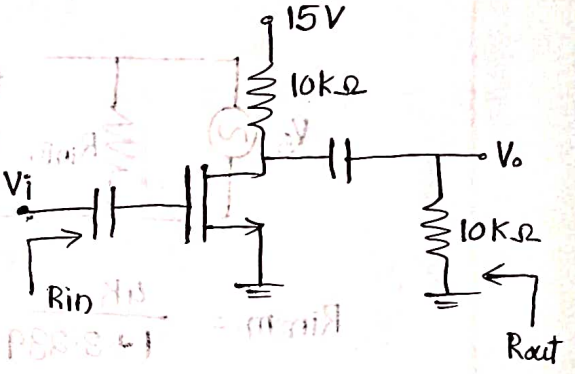
$\Rightarrow V_o = V_i$

$\Rightarrow \frac{V_o}{V_i} = 1$

6) Given :- $V_t = 1.5V$ $V_A = 50V$, $K_n'\left(\frac{W}{L}\right) = 0.25\ mA/V^2$. Find voltage gain.

soln # dc analysis :-



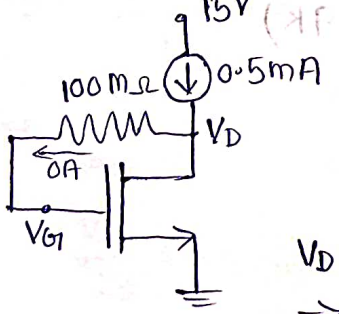


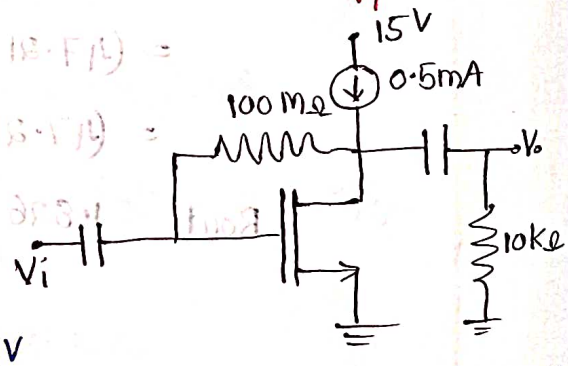
Here the MOSFET is OFF

$\Rightarrow \frac{V_o}{V_{in}} = 0$

7) Given $V_t = 0.9V$ $V_A = 50V$ $V_D = 2V$ Find $\frac{V_o}{V_i}$

soln # dc analysis :-





$V_D = V_{G1} = 2V$

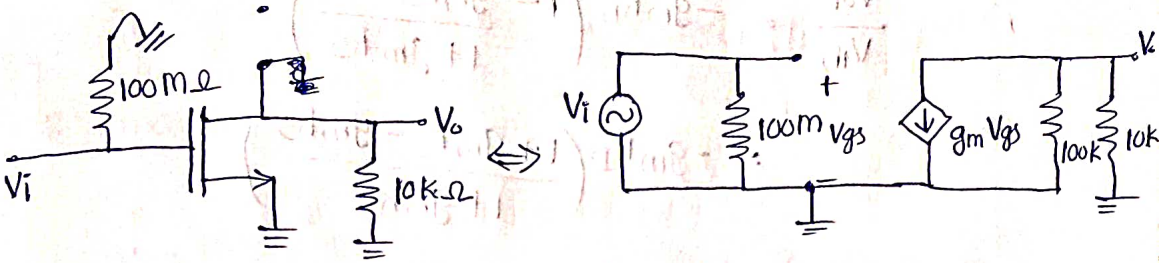
$\Rightarrow$ saturation

$I_D = 0.5mA$ $V_{GS} = V_G - V_S = 2$

$$g_m = \frac{2I_D}{V_{GS} - V_T} = \frac{2 \times 0.5}{2 - 0.9} = \frac{1}{1.1} = 0.909\ mA/V$$

$$r_o = \frac{V_A}{I_D} = \frac{50}{0.5mA} = 100\ K\Omega$$

ac analysis :- ~~without feedback resistance :-~~



$$V_o = -g_m V_{gs} (10K \,||\, 100K)$$

$$= -0.909^m \times V_{gs} \times (9.090\ K)$$

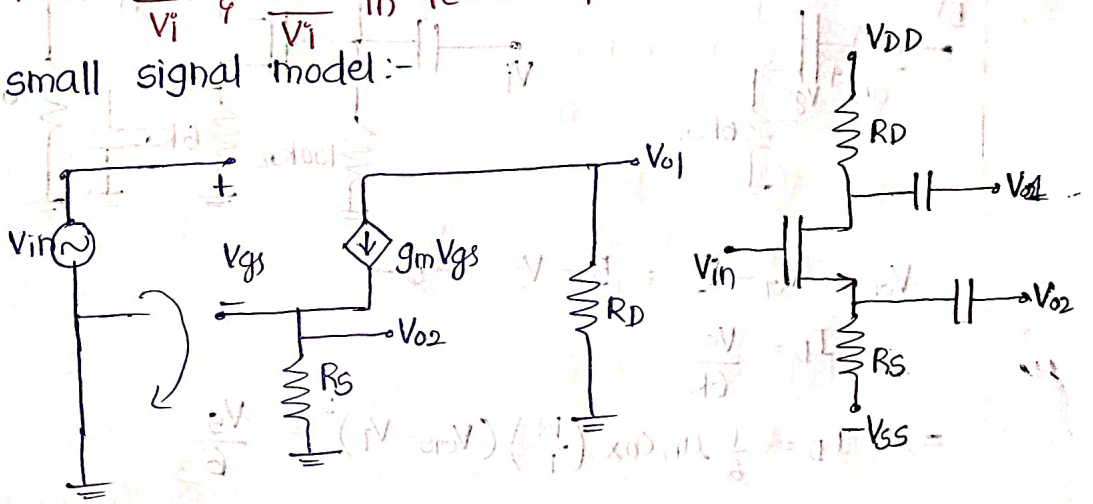
$$\frac{V_o}{V_{gs}} = -8.2628$$

$$V_{gs} = V_i$$

$$\Rightarrow A_V = \frac{V_o}{V_i} = -8.2628$$

8) Find $\frac{V_{o1}}{V_i}$ & $\frac{V_{o2}}{V_i}$ in terms of R_D & R_S

Soln small signal model :-



By KVL on i/p :-

$$-V_{in} + V_{gs} + V_{o2} = 0$$

$$V_{gs} = V_{in} - V_{o2}$$

$$V_{o2} = g_m V_{gs} R_S$$

$$V_{o2} = g_m R_S (V_{in} - V_{o2})$$

$$V_{o2} + g_m R_S V_{o2} = g_m R_S V_{in}$$

$$V_{o2} (1 + g_m R_S) = g_m R_S V_{in}$$

$$\frac{V_{o2}}{V_{in}} = \frac{g_m R_S}{1 + g_m R_S} \Rightarrow V_{o2} = \frac{g_m R_S}{1 + g_m R_S} V_{in}$$

$$V_{o1} = -g_m V_{gs} R_D$$

$$V_{o1} = -g_m R_D (V_{in} - V_{o2})$$

$$V_{o1} = -g_m R_D \left[V_{in} - \frac{g_m R_S}{1+g_m R_S} V_{in} \right]$$

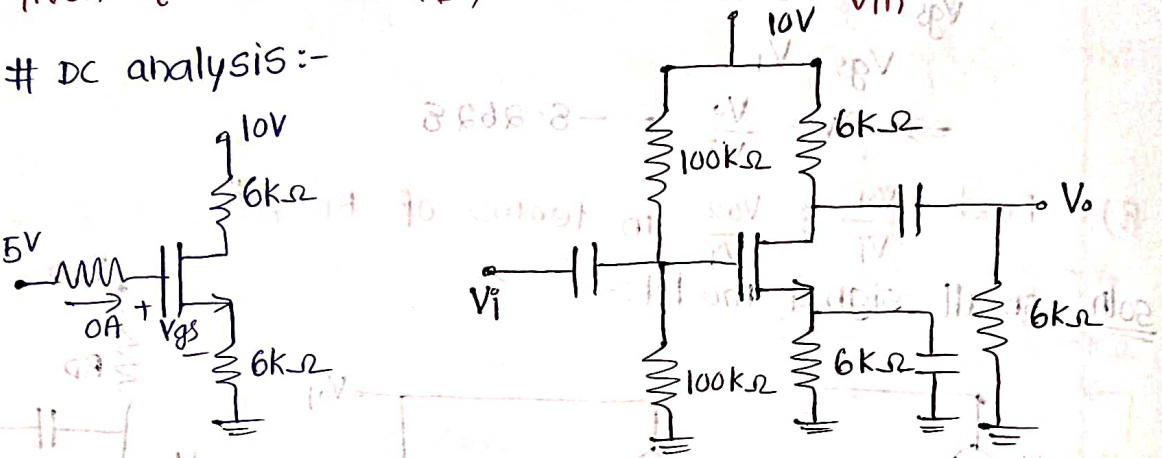
$$\frac{V_{o1}}{V_{in}} = -g_m R_D \left(1 - \frac{g_m R_S}{1+g_m R_S} \right)$$

$$= -g_m R_D \left(\frac{1+g_m R_S - g_m R_S}{1+g_m R_S} \right)$$

$$\frac{V_{o1}}{V_{in}} = \frac{-g_m R_D}{1+g_m R_S}$$

9) Given $V_t = 1V$ $K_n' \left(\frac{W}{L}\right) = 1 mA/V^2$ Find $\frac{V_o}{V_{in}}$

Soln # DC analysis :-



$$V_{GS} = V_G - V_S = 5 - V_S$$

$$I_D = \frac{V_S}{6K}$$

$$\Rightarrow I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_T)^2 = \frac{V_S}{6}$$

$$\Rightarrow 1 \times (5 - V_S - 1)^2 = \frac{V_S}{3}$$

$$\Rightarrow (4 - V_S)^2 = \frac{V_S}{3}$$

$$\Rightarrow V_S = 3(16 + V_S^2 - 8V_S)$$

$$\Rightarrow V_S = 48 + 3V_S^2 - 24V_S$$

$$\Rightarrow 3V_S^2 - 25V_S + 48 = 0$$

$V_S = \frac{16}{3} V \Rightarrow V_{GS} = V_G - V_S = 5 - \frac{16}{3} = -ve$ (Invalid)

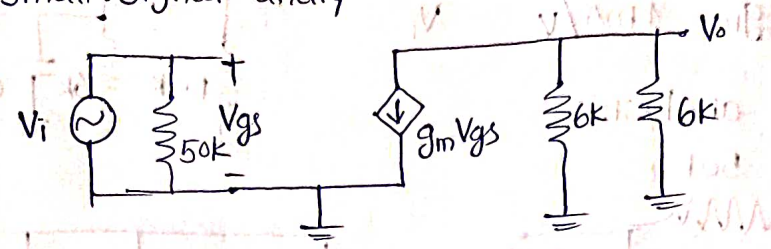
$V_S = 3V \Rightarrow V_{GS} = V_G - V_S = 5 - 3 = 2V$ (valid)

$V_S = 6K\, I_D$

$\Rightarrow I_D = \frac{V_S}{6K} = \frac{3}{6K} = 0.5\,mA$

$g_m = \frac{2I_D}{V_{GS} - V_T} = \frac{2 \times 0.5}{2-1} = 1\,mA/V$

small signal analysis:-



$V_i = V_{gs}$

$V_o = -g_m V_{gs} (6K \| 6K)$

$= -1\, V_{gs} (3K)$

$\frac{V_o}{V_{gs}} = -3$

$\frac{V_o}{V_i} = -3$

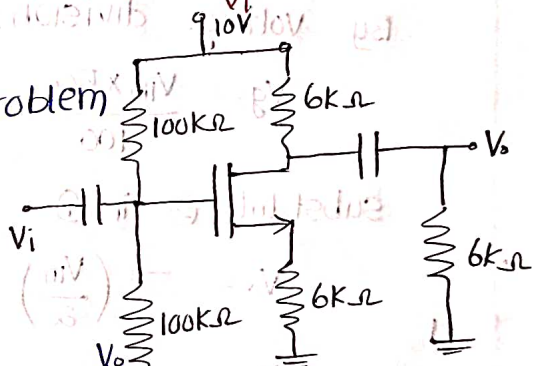
10) Given $V_t = 1V$ $K_n' \left(\frac{W}{L}\right) = 1mA/V^2$ Find $\frac{V_o}{V_i}$

Soln # DC analysis:-

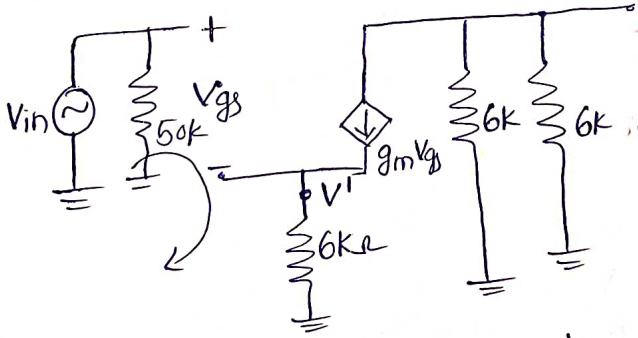
same as the previous problem

$I_D = 0.5\,mA$

$g_m = 1\,mA/V$



ac analysis:-



By KVL $-V_{in} + V_{gs} + V' = 0$

$V' = V_{in} - V_{gs}$

$6K\, g_m V_{gs} + V_{gs} = V_{in}$

$V_{in} = V_{gs}(6(1)+1) = 7V_{gs}$

$V_o = -g_m V_{gs} (6K \| 6K) = -1\, V_g (3) = -3V_{gs}$

$\frac{V_o}{V_{in}} = \frac{-3V_{gs}}{7V_{gs}} = -0.428$

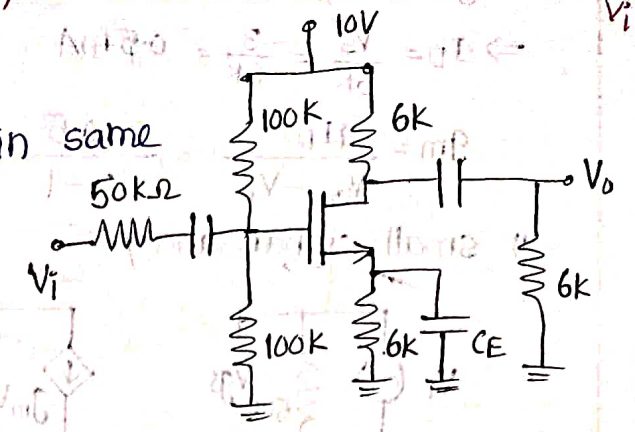
11) Given $V_t = 1V$, $K_n'(\frac{W}{L}) = 1mA/V^2$ Find the value of $\frac{V_o}{V_i}$

Soln # DC analysis:-

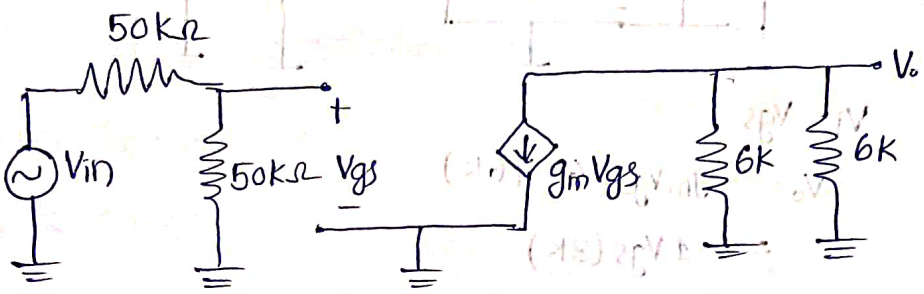
DC analysis remain same

$I_D = 0.5\ mA$

$g_m = 1\ mA/V$



ac analysis:



$V_o = -g_m V_{gs} (6K \parallel 6K)$

$= -1m\ V_{gs} (3K)$

$V_o = -3 V_{gs} \rightarrow (1)$

By voltage division:-

$V_{gs} = \frac{V_{in} \times 50}{100} = \frac{V_{in}}{2} \rightarrow (2)$

Substitute (2) in (1)

$V_o = -3\left(\frac{V_{in}}{2}\right)$

$A_V = \frac{V_o}{V_{in}} = -1.5$

12) An NMOS transistor has $\mu_n C_{ox} = 60\mu A/V^2$ $\frac{W}{L} = 40V$

$V_t = 1V$ and $V_A = 15V$. Find g_m & r_o when

a) bias voltage $V_{GS} = 1.5V$

b) bias current $I_D = 0.5mA$

$\mu_n C_{ox} \frac{W}{L} = 60 \times 40 \times 10^{-6}$

$= 2.4\ mA/V^2$

Soln a) $V_{GS} = 1.5V$

$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$

$= \frac{1}{2} \times 2.4\ (1.5-1)^2$

$I_D = 1.2 \times (0.5)^2 = 0.3\ mA$

$$g_m = \frac{2I_D}{V_{GS} - V_T} = \frac{2 \times 0.3}{1.5 - 1} = 1.2 \text{ mA/V}^2$$

$$r_o = \frac{V_A}{I_D} = \frac{15}{0.3m} = 50 \text{ K}\Omega$$

b) $I_D = 0.5$ mA $\qquad r_D = \frac{V_A}{I_D} = \frac{15}{0.5} = 30\text{K}\Omega$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

$$2 \times 0.5 = 2.4 (V_{GS} - 1)^2$$

$$V_{GS} - 1 = \sqrt{\frac{1}{2.4}}$$

$$V_{GS} = 1 + \sqrt{\frac{1}{2.4}} = 1.645 \text{ volts}$$

$$g_m = \frac{2I_D}{V_{GS} - V_T} = \frac{2 \times 0.5}{1.645 - 1} = 1.55 \text{ mA/V}$$

13) A MOSFET is to operate at $I_D = 0.1$ mA and is to have $g_m = 1$ mA/V. If $K_n' = 50\ \mu\text{A/V}^2$, Find the required $\left(\frac{W}{L}\right)$ ratio as the over drive voltage?

soln $I_D = 0.1$ mA

$g_m = 1$ mA/V

$$g_m = \sqrt{2 I_D \mu_n C_{ox} \left(\frac{W}{L}\right)}$$

$$g_m^2 = 2 I_D \mu_n C_{ox} \frac{W}{L}$$

$$\frac{W}{L} = \frac{g_m^2}{2 I_D \mu_n C_{ox}} = \frac{1}{2 \times 0.1_m \times 50} = 0.1 \times 10^3 = 100$$

$$g_m = \frac{2I_D}{V_{GS} - V_T}$$

$$\underbrace{V_{GS} - V_T}_{\text{over drive voltage.}} = \frac{2I_D}{g_m} = \frac{2 \times 0.1}{1} = 0.2\text{V}$$

14) For a fabrication process for which $\mu_p = 0.4\mu_n$ find the ratio of width of PMOS to the width of NMOS so that the two devices have equal g_m for same bias condition two have equal channel length?

Soln Given the both have same biasing condition

$$\Rightarrow I_{DP} = I_{Dn}$$

They have same transconductance g_m

$$g_{mp} = g_{mn}$$

$$\Rightarrow \sqrt{2 I_{D_p} \mu_p C_{ox} \frac{W_1}{L}} = \sqrt{2 I_{D_n} \mu_n C_{ox} \frac{W_2}{L}}$$

$$\Rightarrow 2 I_{Dp} \mu_p C_{ox} \frac{W_1}{L} = 2 I_{Dn} \mu_n C_{ox} \frac{W_2}{L}$$

$$\Rightarrow \mu_p W_1 = \mu_n W_2$$

$$\Rightarrow \frac{W_1}{W_2} = \frac{\mu_n}{\mu_p}$$

Given $\mu_p = 0.4\,\mu_n \Rightarrow \frac{\mu_n}{\mu_p} = \frac{1}{0.4}$

$$\frac{W_1}{W_2} = \frac{1}{0.4} = 2.5$$

15) calculate Avs, Rin, Ro for common source amplifier given if $K_n' \left(\frac{W}{L}\right) = 1\,mA/V^2$ and $V_t = 1V$ $V_A = 50V$

Soln # DC analysis :-

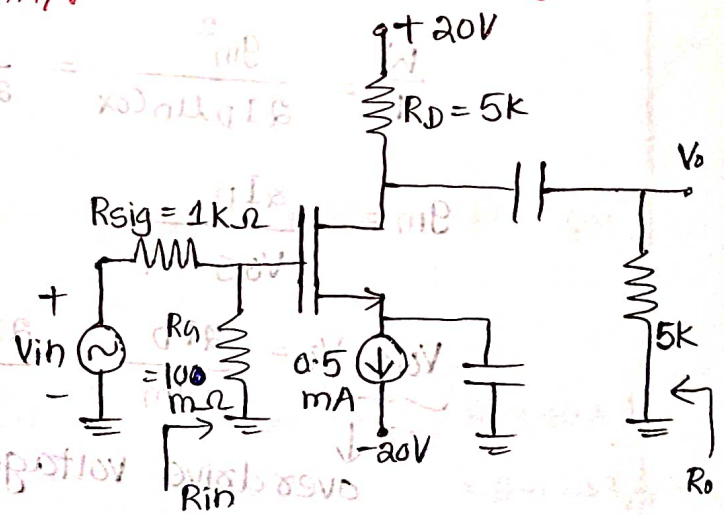
$I_D = 0.5\,mA$

$$g_m = \frac{2 I_D}{V_{GS} - V_T}$$

$$= \sqrt{2 I_D \mu_n C_{ox} \left(\frac{W}{L}\right)}$$

$$= \sqrt{2 \times 0.5 \times 1}$$

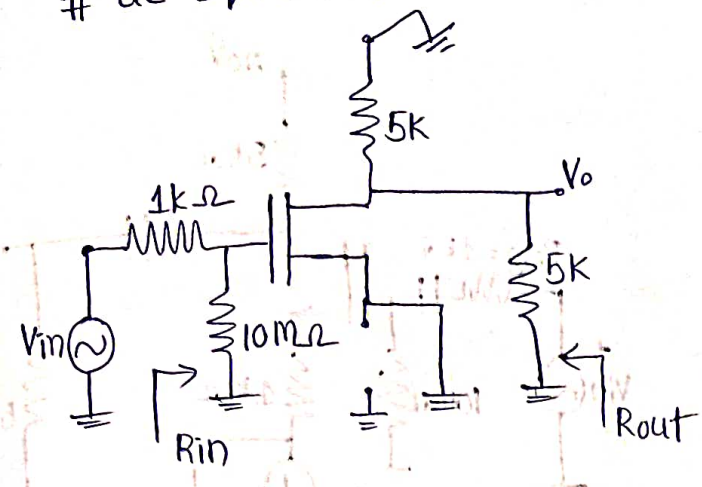
$g_m = 1\,mA/V$



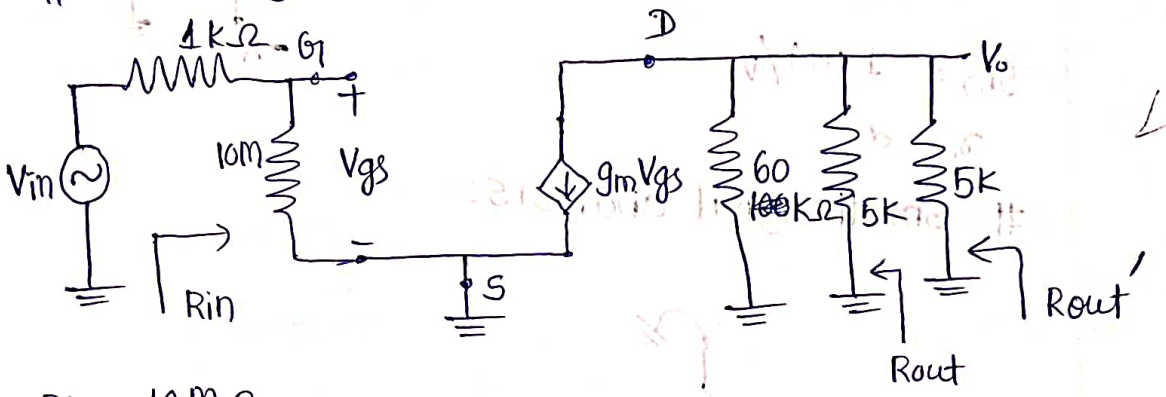
$$r_o = \frac{V_A}{I_D} = \frac{50}{0.5} = 60\,k\Omega$$

ac analysis :-

ac equivalent circuit :-



small signal equivalent model :-



$R_{in} = 10M\Omega$

$R_{out}' = 100K \parallel 5K \parallel 5K$

$= 60K \parallel 2.5K$

$= 2.4K\Omega$

$R_{out} = 60K \parallel 5K$

$= 4.615K\Omega$

$V_{gs} = \dfrac{V_{in} \times 10M}{10M + 1K}$ (voltage division rule)

$10M >>> 1K$

$\Rightarrow V_{gs} = \dfrac{V_{in} \times 10M}{10M} = V_{in}$

$V_o = -g_m V_{gs} (60K \parallel 5K \parallel 5K)$

$= -1m \times V_{gs} (2.4K)$

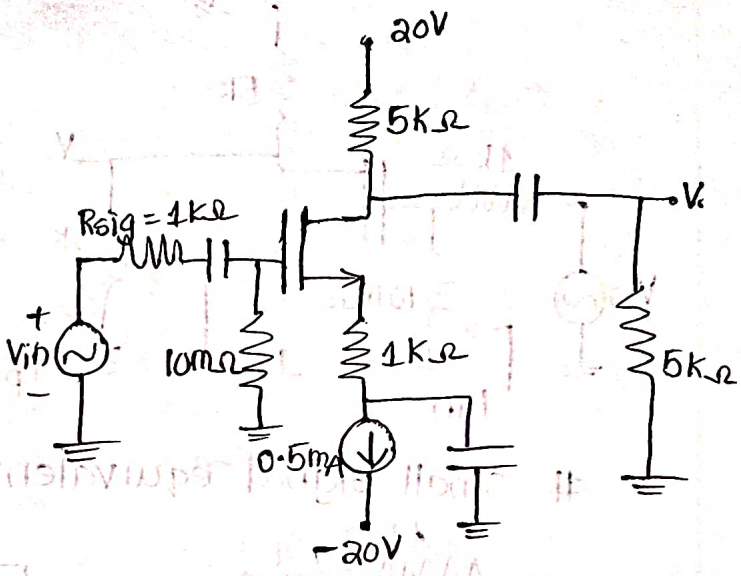
$\dfrac{V_o}{V_{gs}} = -2.4$

$A_{VS} = \dfrac{V_o}{V_{in}} = -2.4$

16) Calculate A_{VS}, R_{in}, R_o in the common source amplifier and source resistance, If $k_n\left(\frac{W}{L}\right) = 1mA/V^2$ and $V_t = 1V$ (given $V_A = \infty$)

Soln

DC analysis :-



$I_D = 0.5\,mA$

$$g_m = \frac{2I_D}{V_{GS} - V_T}$$

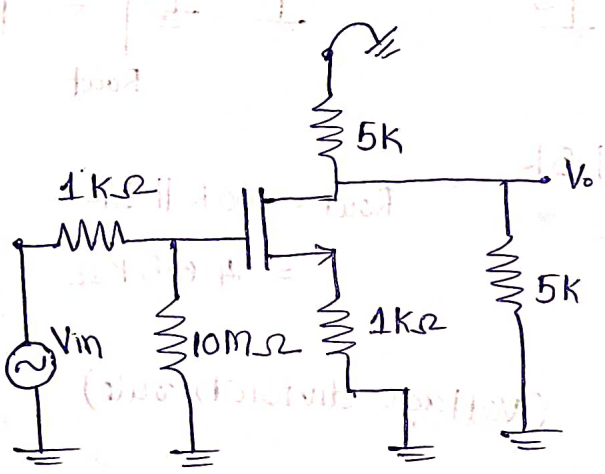
$$= \sqrt{\frac{1}{2} I_D \mu_n C_{ox} \frac{W}{L}}$$

$$= \sqrt{\frac{2}{2} \times 0.5 \times 1}$$

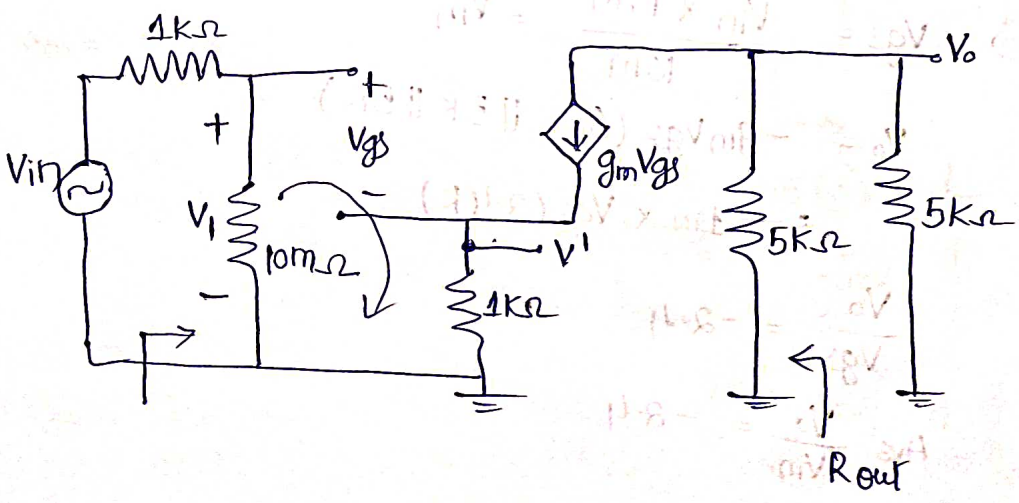
$g_m = 1\,mA/V$

$r_o = \infty$

small signal analysis :-



small signal model :-



$V_1 = \frac{V_{in} \times 10M}{10M + 1K}$ (voltage division rule)

By KVL,

$-V_1 + V_{gs} + V' = 0$

$V_{gs} = V_1 - V'$

$V_{gs} = V_1 - g_m V_{gs} 1K$

$V_{gs} = V_1 - 1m\, V_{gs} 1K$

$2V_{gs} = V_1$

$V_{gs} = \frac{V_1}{2} \rightarrow (1)$

$V_o = -g_m V_{gs} (5K \parallel 5K)$

$= -1m\, V_{gs} (2.5K)$

$V_o = -2.5\, V_g$

$V_o = -2.5 \frac{V_1}{2}$

$V_o = -1.25\, V_1$

$V_o = -1.25 \left[\frac{V_{in}\, 10M}{10M + 1K}\right]$

since $10M >>> 1K$

$10M + 1K \approx 10M$

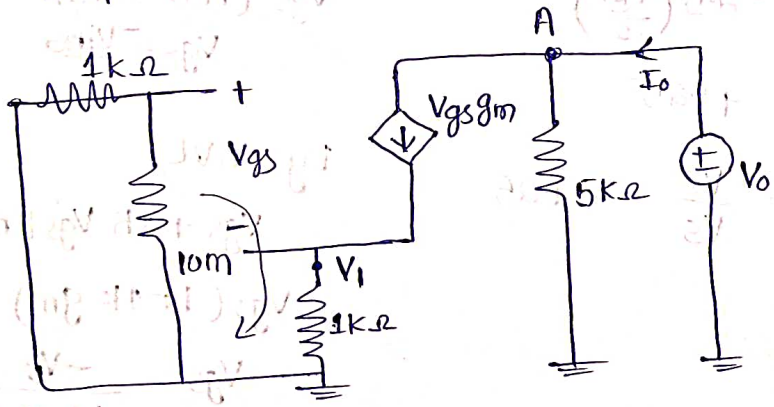
$V_o = -1.25 \left[\frac{V_{in}\, 10M}{10M}\right]$

$V_o = -1.25\, V_{in}$

$A_{VS} = \frac{V_o}{V_{in}} = -1.25$

Input resistance $R_{in} = 10$ mohm

output resistance:-



KCL @ node A:

$I_o = \frac{V_o}{5K} + V_{gs} g_m$

By KVL,

$V_{gs} + 1K\, g_m V_{gs} = 0$

$\Rightarrow V_{gs} (1 + 1K\, g_m) = 0$

$\boxed{V_{gs} = 0}$

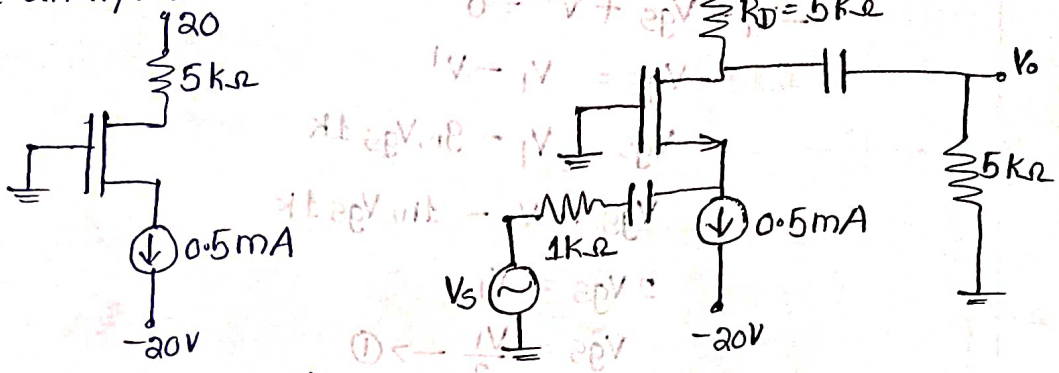
$\Rightarrow I_o = \frac{V_o}{5K} + V_{gs} g_m$

$\Rightarrow \frac{V_o}{I_o} = R_{out} = 5K\Omega$

17) Find A_v, R_{in}, R_o for common gate amplifier given if $K_n'\left(\frac{W}{L}\right) = 1mA/V^2$ $V_t = 1V$ and $V_A = \infty$

Soln

DC analysis :-

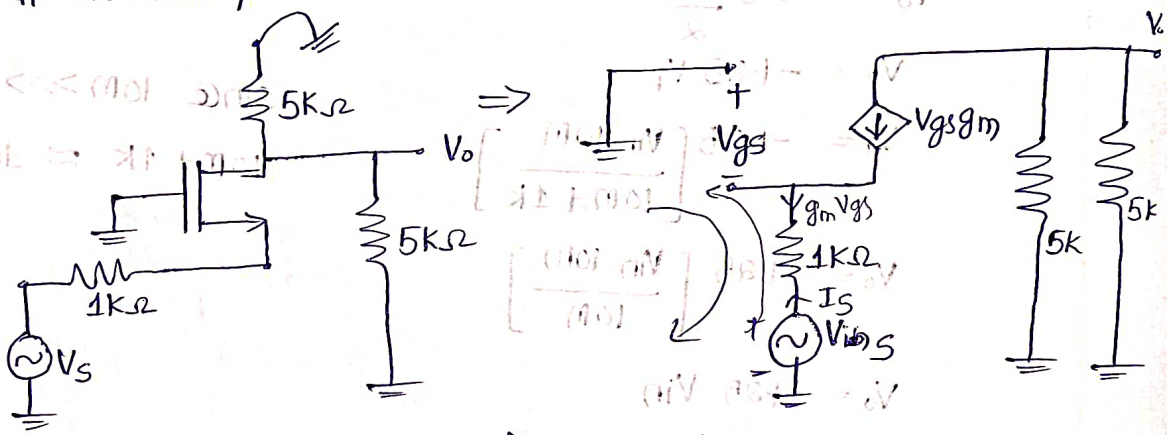


From the above ckt, $I_D = 0.5mA$

$$g_m = \sqrt{2 I_D \mu_n C_{ox} \frac{W}{L}} = \sqrt{2 \times 0.5 \times 1} = 1mA/V$$

$$r_o = \frac{V_A}{I_D} = \infty$$

ac analysis :-



$$V_o = -g_m V_{gs}(5K \| 5K)$$
$$= -1^m V_{gs}(2.5K)$$
$$V_o = -2.5 V_{gs}$$
$$\Rightarrow V_o = -2.5\left(\frac{-V_{in}}{2}\right)$$
$$\Rightarrow \frac{V_o}{V_S} = +1.25$$
$$A_V = \frac{V_o}{V_S} = +1.25$$

By KVL,

$$V_{gs} + 1K(V_{gs} g_m) = -V_{in}$$
$$V_{gs} + 1K(V_g 1m) = -V_{in}$$
$$V_{gs}(1+1) = V_{in}$$
$$V_{gs} = \frac{-V_{in}}{2}$$

By KVL,

$$V_{gs} + 1K\, V_{gs} g_m + V_S = 0$$
$$V_{gs}(1 + 1K\, g_m) = -V_S$$
$$V_{gs} = \frac{-V_S}{1 + 1K(1m)}$$
$$= \frac{-V_S}{2}$$

By KVL on i/p side from bottom to top:-

$$-V_s - g_m V_{gs} 1K - V_{gs} = 0$$

$$V_s = -V_{gs}[1 + g_m 1K]$$

$$R_{in} = \frac{V_s}{I_s} = \frac{-V_{gs}(1 + g_m 1K)}{-V_{gs} g_m} \quad (I_s = -g_m V_{gs})$$

$$R_{in} = \frac{(1 + g_m 1K)}{g_m}$$

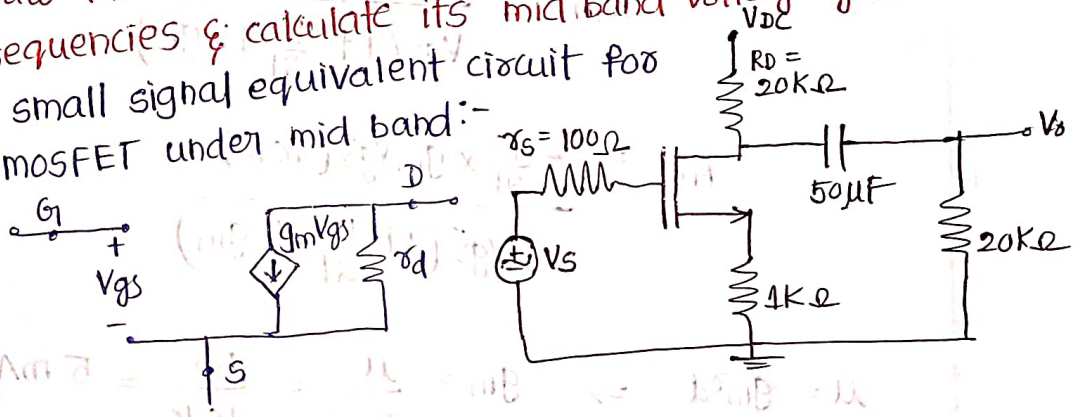
$$R_{in} = \frac{1}{g_m} + 1K\Omega \quad (\text{Including source resistance})$$

$$R_{in} = \frac{1}{1m} + 1K\Omega = 1K + 1K = 2K\Omega \quad (\text{Including source resistance})$$

$$R_{in}' = R_{in} - 1K = 2K - 1K = 1K\Omega \quad (\text{Excluding source resistance})$$

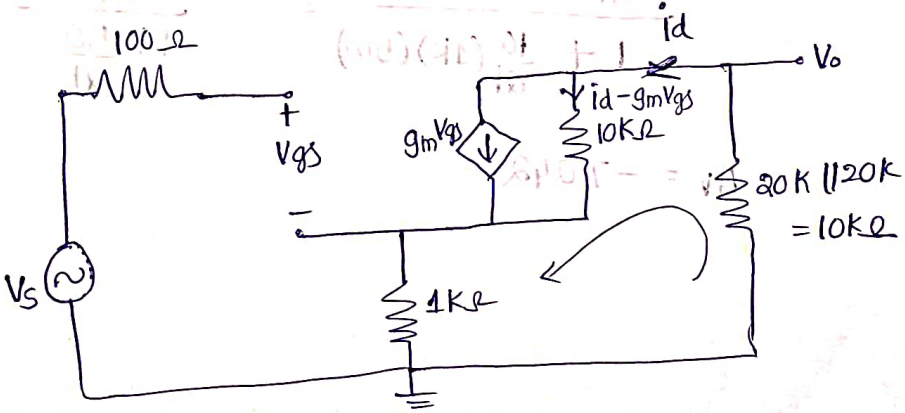
18) In the MOSFET amplifier shown in figure below has $\mu = 50$, $r_d = 10K\Omega$ $C_{gs} = 5PF$. $C_{gd} = 1PF$ and $C_{ds} = 2PF$. Draw the small signal equivalent circuit for midband frequencies & calculate its mid band voltage gain.

Soln # small signal equivalent circuit for MOSFET under mid band:-



For given ckt:-

small signal equivalent model:-



$$V_o = -i_d(10K\Omega)$$

By KVL, $10K\, i_d + 10K(i_d - g_m V_{gs}) + 1K\, i_d = 0$

$$21K\,i_d = 10K\,g_m V_{gs}$$

$$21\,i_d = 10\,g_m V_{gs} \Rightarrow i_d = \frac{10}{21} g_m V_{gs} \longrightarrow (1)$$

From input :-

$$-V_s + V_{gs} + 1K\,i_d = 0$$

$$i_d = \frac{V_s - V_{gs}}{1K} \longrightarrow (2)$$

From (1) & (2)

$$\frac{V_s - V_{gs}}{1K} = \frac{10}{21} g_m V_{gs}$$

$$V_s - V_{gs} = \frac{10}{21} g_m V_{gs} 1K$$

$$V_s = \frac{10}{21} 1K\, g_m V_{gs} + V_{gs}$$

$$V_s = V_{gs}\left(1 + \frac{10}{21} 1K\, g_m\right) \longrightarrow (3)$$

Voltage gain :-

$$A_V = \frac{V_o}{V_{in}} = \frac{-i_d (10K\Omega)}{V_{gs}\left(1 + \frac{10}{21} 1K\, g_m\right)}$$

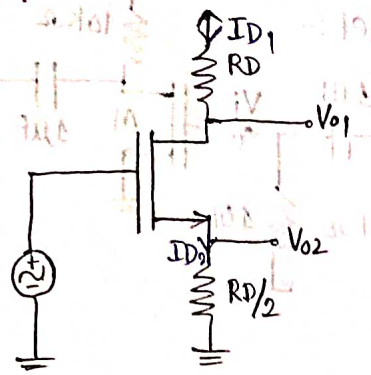
$$A_V = \frac{-\frac{10}{21} \times g_m V_{gs} (10K)}{V_{gs}\left(1 + \frac{10}{21} 1K\, g_m\right)}$$

$$\mu = g_m r_d \Rightarrow g_m = \frac{\mu}{r_d} = \frac{50}{10K} = 5\ mA/V$$

$$A_V = \frac{\frac{-10}{21} \times 5m \times 10K}{1 + \frac{10}{21}(1K)(5m)} = \frac{-\frac{500}{21}}{1 + \frac{50}{21}} = \frac{500}{71}$$

$$A_V = -7.042$$

19) In the MOSFET amplifier of the figure is the signal o/p V_1 & V_2 obey the _____ relationship



Soln: current flow through drain & source terminals are same for MOSFET

$$\Rightarrow I_{D1} = I_{D2}$$

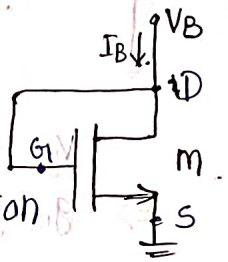
$$\Rightarrow \frac{-V_{o1}}{R_D} = \frac{V_{o2}}{R_D/2}$$

$$\Rightarrow \frac{-V_{o1}}{R_D} = \frac{2V_{o2}}{R_D}$$

$$\Rightarrow V_{o1} = -2V_{o2}$$

20) The small signal resistance (i.e., $\frac{dV_B}{dI_B}$) in KΩ offered by the n-channel MOSFET m shown in figure below, at a bias point of $V_B = 2$ volts (device data for m: $k_n = \mu_n C_{ox} \frac{W}{L} = 40\mu A/V^2$) and $V_{TN} = 1V$) neglect body effect & channel length modulation effects:-

Soln In given figure



$$V_{G1} = V_D = V_B \text{ & } V_S = 0V$$

$$V_{GS} = V_B$$

MOSFET is in saturation

For saturation we have

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2$$

$$I_D = \frac{k_n}{2}(V_B - V_T)^2$$

$$\frac{\partial I_D}{\partial V_B} = \frac{k_n}{2}[2(V_B - V_T)] = k_n(V_B - V_T)$$

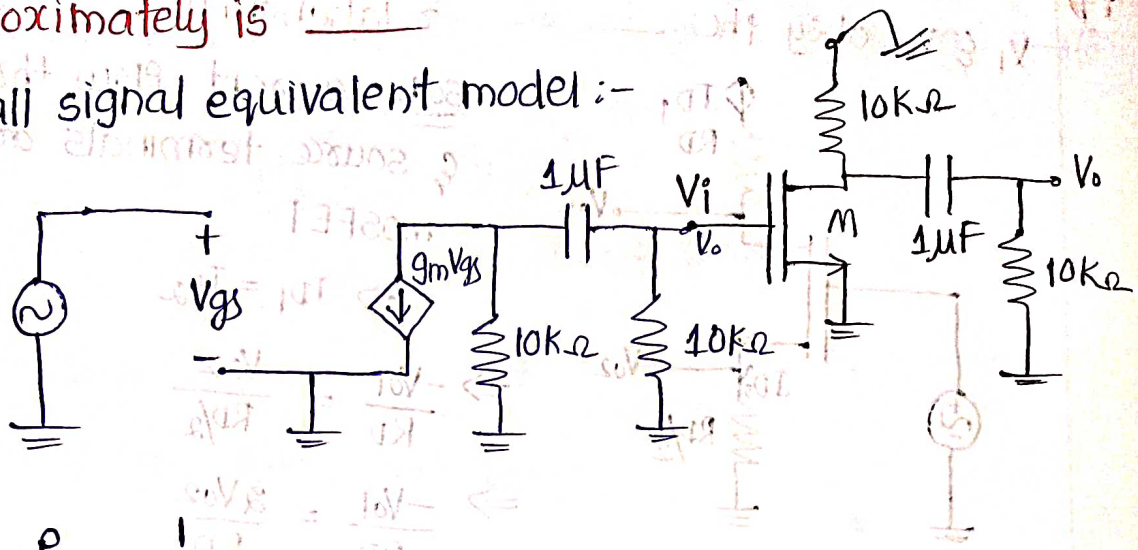
$$\Rightarrow \frac{\partial V_B}{\partial I_D} = \frac{1}{k_n(V_B - V_T)} = \frac{1}{40\times10^{-6}\times(2-1)} = \frac{1}{40\times10^{-6}}$$

$$\frac{\partial V_B}{\partial I_D} = 25K\Omega$$

21) The ac schematic of a NMOS common source stage is shown in the figure below, where part of the biasing circuit has been omitted for simplicity. For the n-channel MOSFET m, the transconductance $g_m = 1mA/V$ and body effect & channel length modulation effect are to be

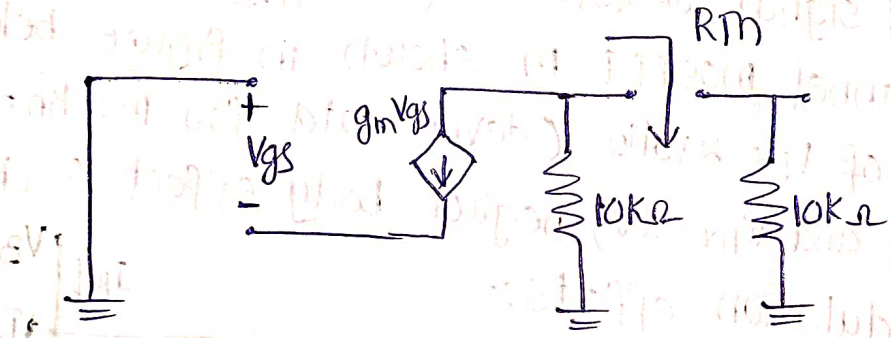
neglected. The lower cutoff frequency in Hz of circuit approximately is ____

soln small signal equivalent model :-



$$f_L = \frac{1}{2\pi RC}$$

we need R across 1μF capacitor



$V_{gs} = 0\ V$

$\Rightarrow g_m V_{gs} = 0A$ (open circuit)

$R_{Th} = 10K + 10K = 20K\Omega \qquad C = 1\mu F$

$$f_L = \frac{1}{2\pi RC} = \frac{1}{2 \times 3.14 \times 20 \times 10^3 \times 1 \times 10^{-6}}$$

$$f_L = 7.96\ Hz \simeq 8\ Hz$$