



WELCOME

THE PAIN YOU FEEL TODAY WILL BE THE
STRENGTH YOU WILL FEEL TOMORROW

ANALOG ELECTRONICS

CHAPTER 4

MOSFET :-

**FREQUENCY RESPONSE
MULTISTAGE AMPLIFIERS &
DIFFERENTIAL AMPLIFIER**

By :-

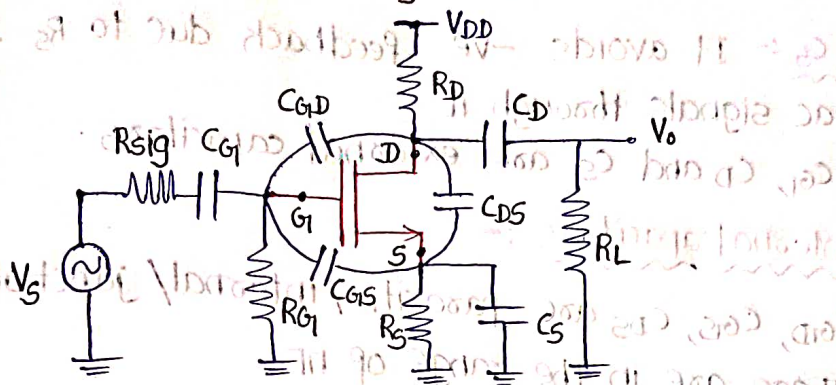
Dhamu (D²)

Chapter - 4

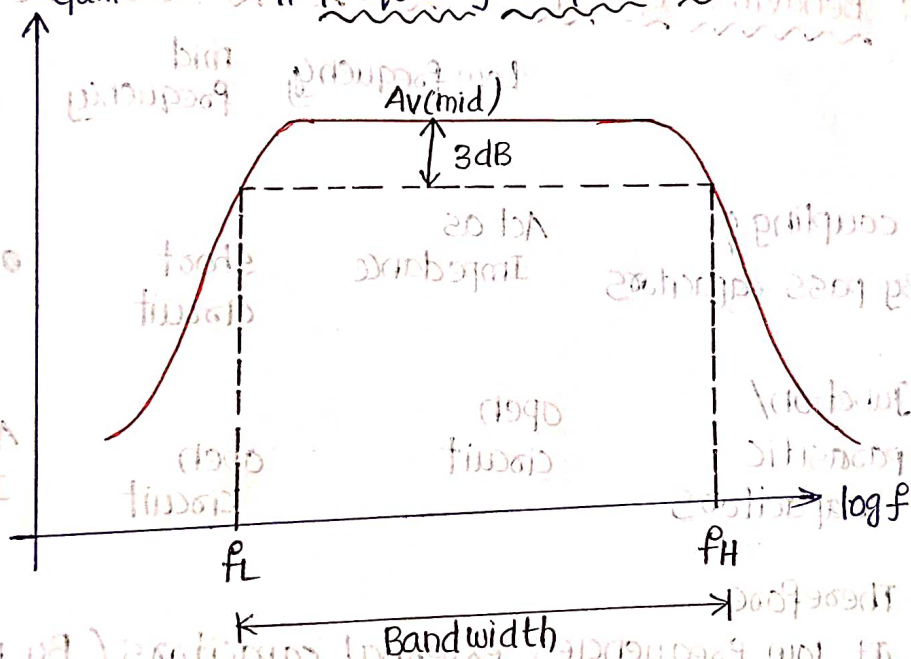
MOSFET: Frequency Response, multi-stage & Differential Amplifiers

Frequency response of MOSFET:-

consider the following common source Amplifier.



Frequency response plot of Amplifier:-



External capacitors & their functionality, in CS Amplifier:-

1. C_{G1} :- It is a coupling capacitor. It blocks dc signal which enters from source to input stage of Amplifier.

In dc analysis, it will act as open circuit and it isolates input stage of the amplifier from source.

In ac analysis it will act as short circuit and it couples the input stage of the amplifier to the source.

#2. C_D :- It blocks dc signals entering from the output stage of the amplifier to the load.

It isolates o/p stage of amplifier from the load in dc point of view i.e, it act as open circuit.

In ac analysis it will act as short circuit and it couples the o/p stage of the amplifier to the load.

#3. C_S :- It avoids -ve feedback due to R_S . It bypass ac signals through it.

C_{G1} , C_D and C_S are external capacitors.

Internal capacitors :-

C_{GD} , C_{GS} , C_{DS} are parasitic/internal/junction capacitors.

These are in the range of nF.

Behaviour of capacitances at different frequencies:-

	Low frequency	mid frequency	High frequency
coupling & By pass capacitors	Act as Impedance	short circuit	● short circuit.
Junction/ parasitic capacitors	open circuit	open circuit	Act as Impedance

Therefore

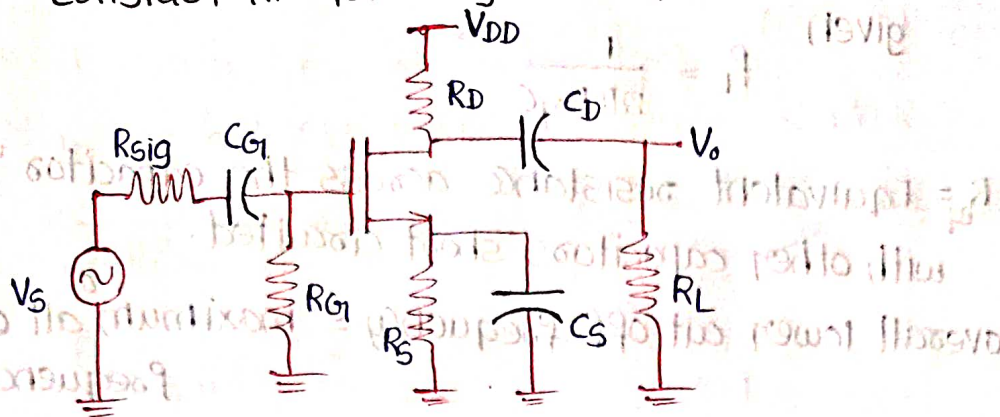
At low frequencies, external capacitors (By pass capacitors & coupling capacitors) are responsible for gain reduction.

At high frequency, internal capacitors (Junction capacitances C_{GD} , C_{GS} , C_{DS}) are responsible for gain reduction.

There are some internal capacitances like wire and lead capacitances.

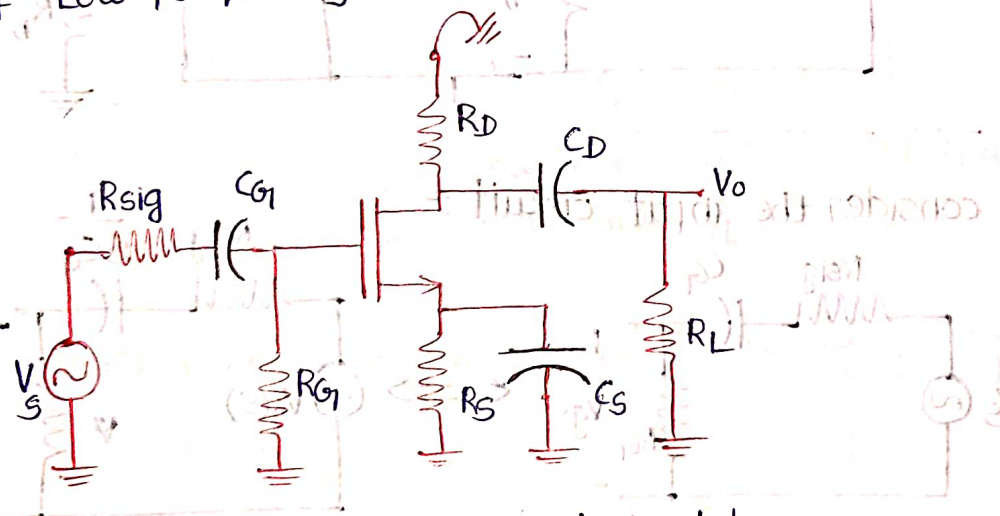
Low frequency response of MOSFET:

consider the following CS Amplifier

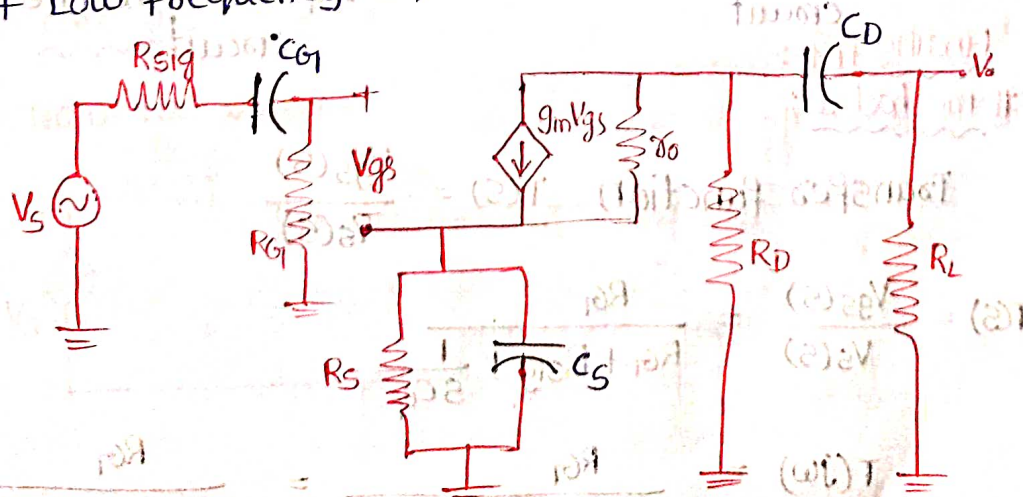


We know that under low frequency analysis, external capacitors are responsible for gain reduction. Therefore consider all external capacitances (C_{G1}, C_S, C_D) and neglect all internal capacitances (C_{G1S}, C_{G1D}, C_{DS})

Low frequency equivalent circuit:-



Low frequency equivalent model:-



We knew that

Lower cutoff frequency due to capacitor 'C' is given

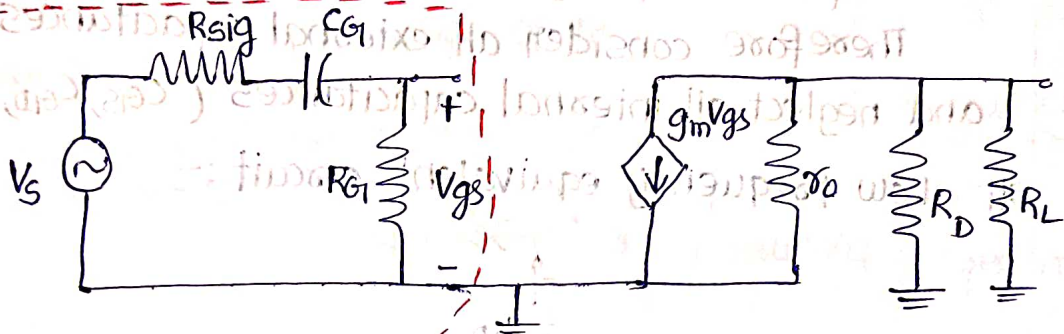
$$f_L = \frac{1}{2\pi R_{eq}C}$$

R_{eq} = Equivalent resistance across the capacitor 'C' with other capacitors short circuited.

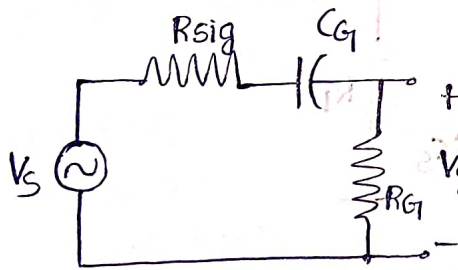
overall lower cut off frequency = maximum ^{of} all obtained frequencies.

case (i) consider C_G and short circuit C_D & C_S :-

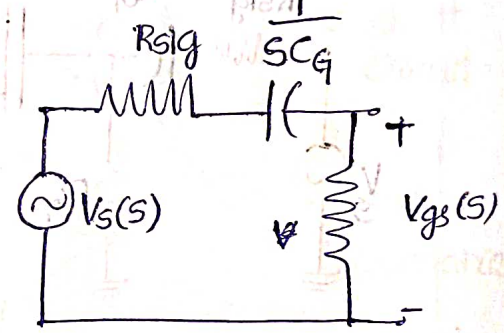
Now the equivalent circuit became



consider the input circuit :-



Time domain equivalent circuit



Laplace domain equivalent circuit.

Finding f_{L1} :-

method 1:

Transfer function $T(s) = \frac{V_{GS}(s)}{V_s(s)}$

$$T(s) = \frac{V_{GS}(s)}{V_s(s)} = \frac{R_{G1}}{R_{G1} + R_{sig} + \frac{1}{sC_G}}$$

$$T(j\omega) = \frac{R_{G1}}{R_{G1} + R_{sig} + \frac{1}{j\omega C_G}} = \frac{R_{G1}}{R_{G1} + R_{sig} + \frac{1}{j\omega C_G}}$$

$$T(f) = \frac{R_G}{R_G + R_{G1}} \cdot \frac{1}{1 + \frac{1}{j\omega C_{G1}(R_G + R_{sig})}}$$

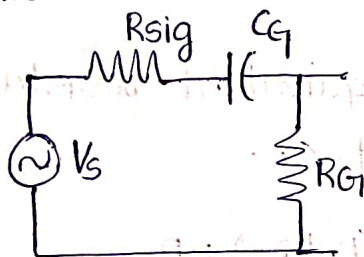
In the denominator we have the term

$\frac{1}{j\omega C_{G1}(R_G + R_{sig})}$ comparing with $\frac{f_L}{jf}$ we get

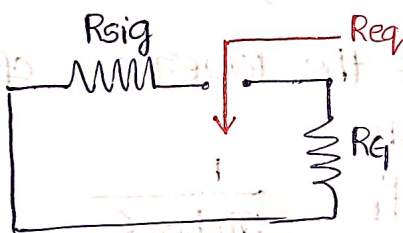
$$f_L = \frac{1}{2\pi C_{G1}(R_G + R_{sig})}$$

method 2:-

consider the input circuit



We need thevenin's equivalent resistance across C_G capacitor. so open circuit C_G and nullify independent source V_s .



$$R_{eq} = R_{sig} + R_G$$

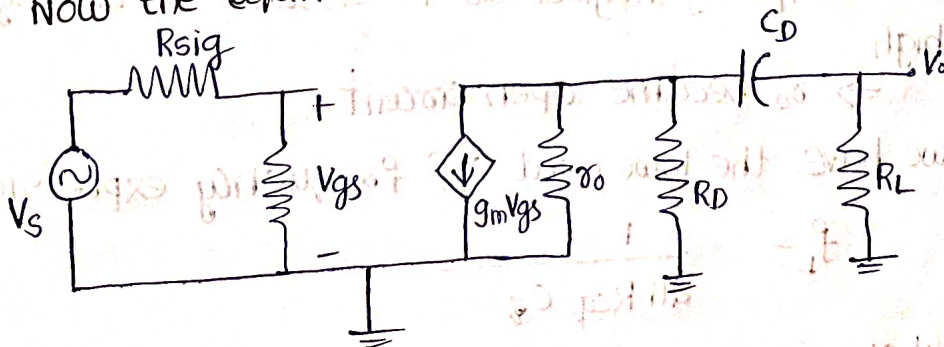
we have lower cut off frequency expression $f_L = \frac{1}{2\pi R_{eq} C}$

$\therefore$ Lower cut off frequency due to C_{G1} is given by

$$f_L = \frac{1}{2\pi (R_G + R_{sig}) C_{G1}}$$

case (ii) consider C_D and shoot circuit C_{G1} & C_s :-

Now the equivalent circuit became.

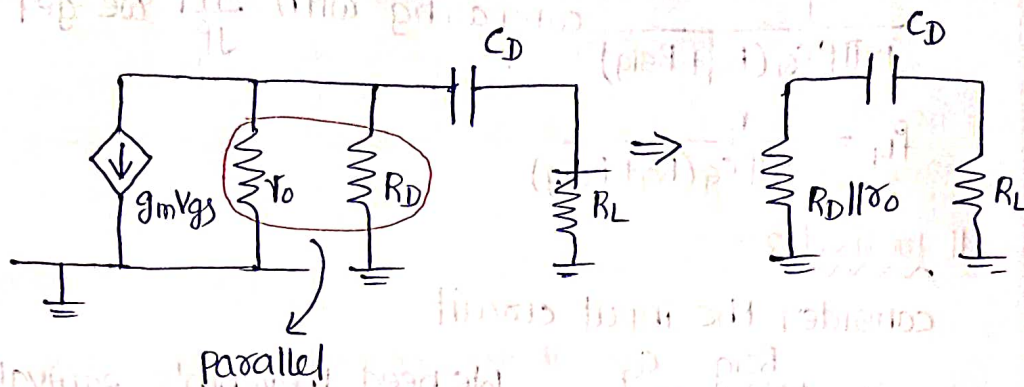


consider circuit on output side:

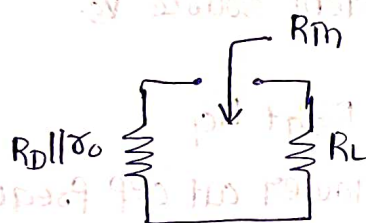
Nullify the ac source V_s .

$$\Rightarrow V_{gs} = 0V$$

$\Rightarrow g_m V_{gs} = 0$ (dependent current source became open circuit)



Now we need thevenin's equivalent resistance across C_D capacitor. so open circuit C_D .



$$R_m = (R_D \parallel r_o) + R_L$$

we have the lower cut off frequency expression:

$$f_L = \frac{1}{2\pi R_{eq} C}$$

~~Low~~ Lower cut off frequency due to C_D is given as

$$f_{L2} = \frac{1}{2\pi ((R_D \parallel r_o) + R_L) C_D}$$

case (iii) consider C_S and short circuit C_G & C_D :-

For simplicity neglect r_o i.e, assume r_o is very high

$\Rightarrow r_o$ became open circuit

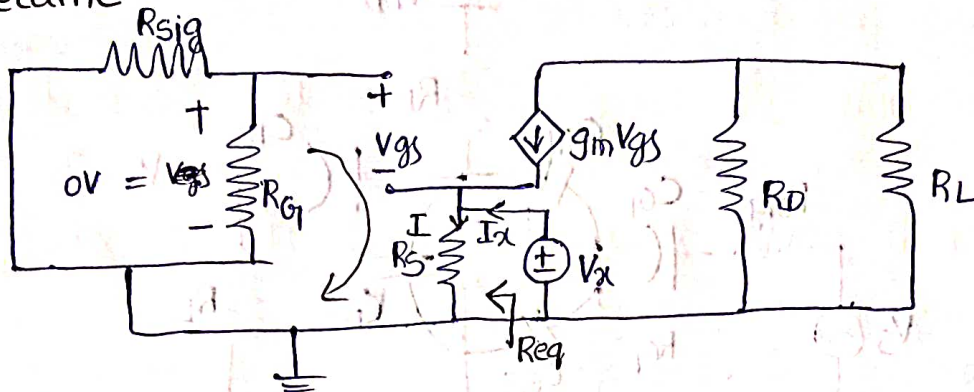
we have the lower cut off frequency expression

$$f_L = \frac{1}{2\pi R_{eq} C_S}$$

when $C = C_S$ we have

$$f_{L3} = \frac{1}{2\pi R_{eq} C_S}$$

We need to find R_{eq} (Equivalent resistance across C_s)
Nullify the source V_s now our small signal model became



$$R_{eq} = \frac{V_x}{I_x}$$

since there is no source on i/p side $V_{gs} = 0$

By KVL,

$$V_{gs} + V_x = 0$$

$$V_{gs} = -V_x$$

$$I = I_x + g_m V_{gs}$$

$$I = \frac{V_x}{R_s} = I_x + g_m V_{gs}$$

$$\frac{V_x}{R_s} = I_x - g_m V_x$$

$$V_x \left(\frac{1}{R_s} + g_m \right) = I_x$$

$$\frac{V_x}{I_x} = \frac{1}{\frac{1}{R_s} + g_m}$$

$$R_{eq} = \frac{V_x}{I_x} = (R_s \parallel \frac{1}{g_m})$$

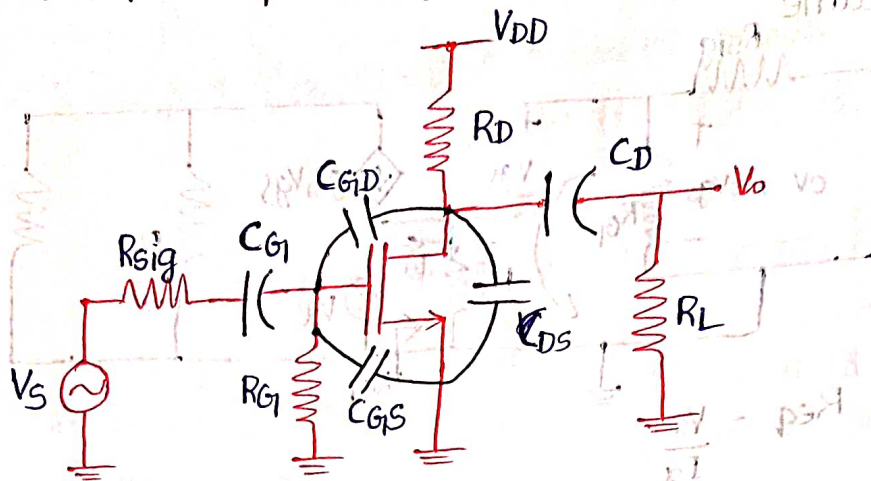
$$f_{L3} = \frac{1}{2\pi (R_s \parallel \frac{1}{g_m}) C_s}$$

overall lower cut off frequency

$$f_L = \max(f_{L1}, f_{L2}, f_{L3})$$

High frequency analysis :-

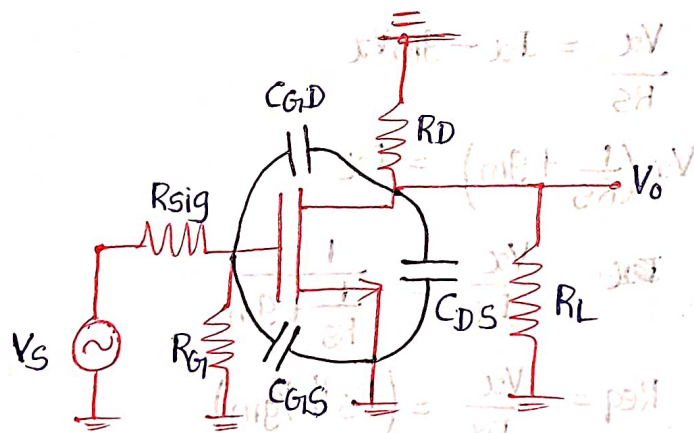
consider the following CS Amplifier



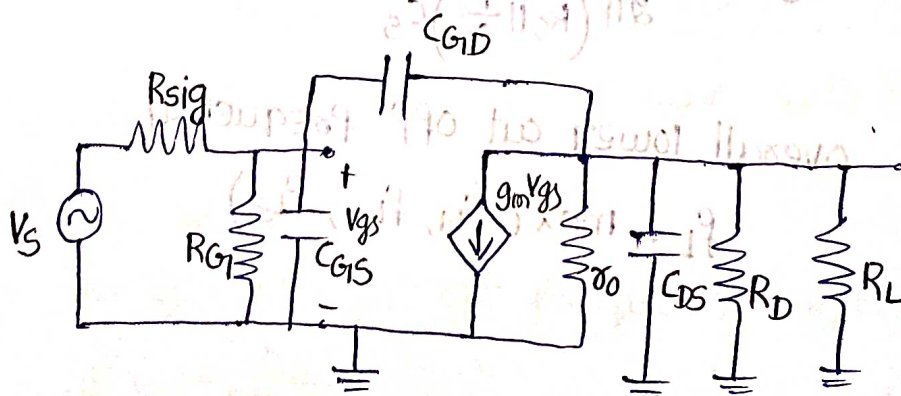
under high frequency analysis :

External capacitors are short circuited & internal capacitances are act as impedances.

High frequency equivalent circuit of CS Amplifier



High frequency equivalent model of CS Amplifier



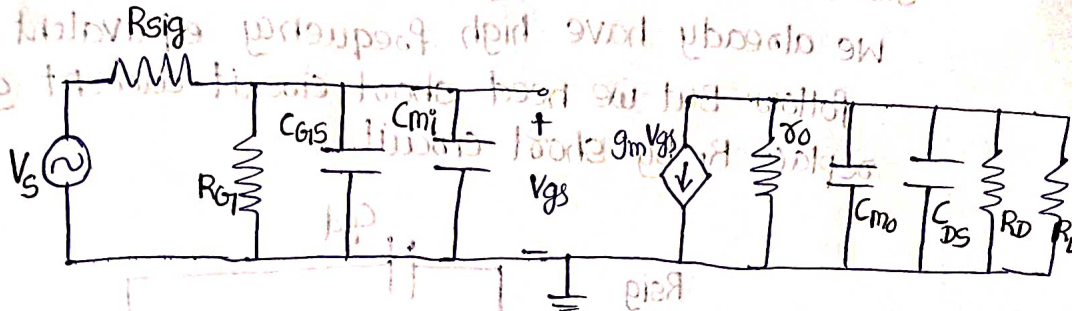
But there is a capacitance connecting input & output. we need to resolve that capacitance into input side & output side by miller theorem.

miller Theorem :

$$C_{mi} = C_{GD}(1 - A_v)$$

$$C_{mo} = C_{GD}(1 - \frac{1}{A_v})$$

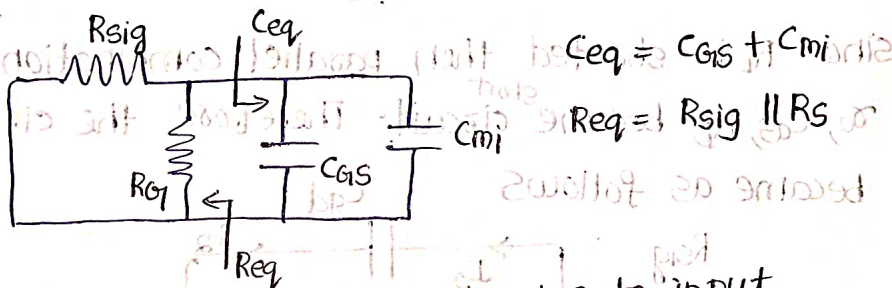
Now equivalent circuit become



We knew that higher cut off frequency $f_H = \frac{1}{2\pi R_{eq} C_{eq}}$

case (i) consider input side :-

short circuit the supply..

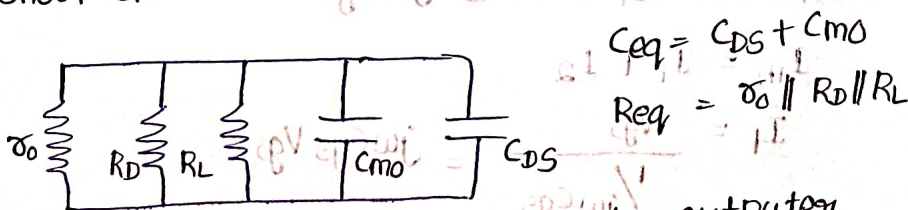


Higher cut off frequency due to input

$$f_{H1} = \frac{1}{2\pi (R_{sig} || R_S) (C_{GS} + C_{mi})}$$

case (ii) consider output side :-

short circuit the supply $\Rightarrow V_{GS} = 0 \Rightarrow g_m V_{GS} = \text{open circuit}$



Higher cut off frequency due to output

$$f_{H2} = \frac{1}{2\pi (r_o || R_D || R_L) (C_{mo} + C_{DS})}$$

overall higher cut off frequency $f_H = \min(f_{H1}, f_{H2})$

Unity gain bandwidth

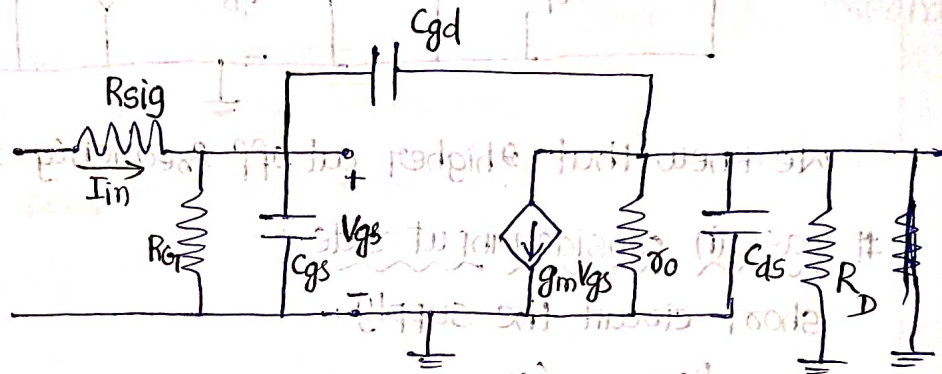
Let f_T be the unity gain frequency.

unity gain frequency :-

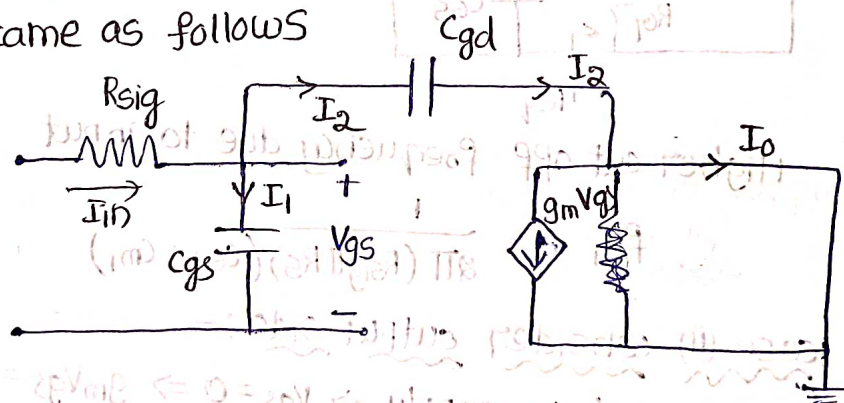
unity gain frequency f_T is the frequency at which gain becomes 1.

To derive f_T , we need to find out common source short circuit current gain.

We already have high frequency equivalent model as follow. But we need short circuit current gain so replace R_L by short circuit.



Since R_L is shorted then parallel combination of ∞ , C_{ds} , R_D become short circuit. Therefore the circuit became as follows



Assume R_{sig} is very high.

$$I_{in} = I_1 + I_2$$

$$I_1 = \frac{V_{gs}}{1/j\omega C_{gs}} = j\omega C_{gs} V_{gs}$$

$$I_2 = \frac{V_{gs}}{1/j\omega C_{gd}} = j\omega C_{gd} V_{gs}$$

$$I_{in} = I_1 + I_2 = j\omega C_{gs} V_{gs} + j\omega C_{gd} V_{gs} = j\omega (C_{gs} + C_{gd}) V_{gs}$$

KCL at output we have

$$I_2 = g_m V_{gs} + I_o$$

$$I_o = I_2 - g_m V_{gs}$$

$$= j\omega C_{gd} V_{gs} - g_m V_{gs}$$

$$I_o = -V_{gs} (g_m - j\omega C_{gd})$$

$$A_I = \frac{I_o}{I_i} = \frac{-V_{gs} (g_m - j\omega C_{gd})}{j\omega (C_{gs} + C_{gd}) V_{gs}} = -\frac{g_m}{j\omega (C_{gs} + C_{gd})}$$

$$A_I = \frac{-(g_m - j\omega C_{gd})}{j\omega (C_{gs} + C_{gd})}$$

If $g_m \gg j\omega C_{gd}$

$$\Rightarrow A_I = \frac{-g_m}{j\omega (C_{gs} + C_{gd})}$$

we need $|A_I| = 1$

$$\Rightarrow \left| \frac{-g_m}{j\omega_T (C_{gs} + C_{gd})} \right| = 1$$

$$\Rightarrow \frac{g_m}{\omega_T (C_{gs} + C_{gd})} = 1$$

$$\Rightarrow g_m = \omega_T (C_{gs} + C_{gd})$$

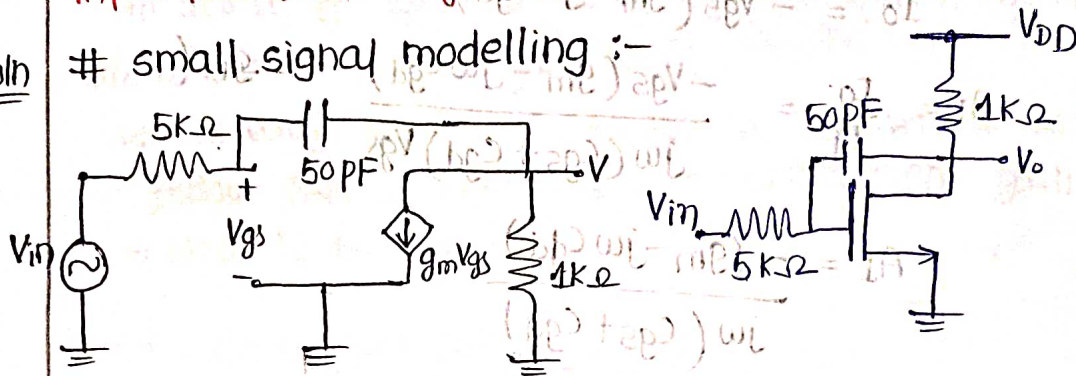
$$\Rightarrow g_m = 2\pi f_T (C_{gs} + C_{gd})$$

$$\Rightarrow f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})}$$

Problems :- $\frac{1}{s} \cdot \frac{1}{s} \cdot \frac{1}{s} \cdot \frac{1}{s} \cdot \frac{1}{s} = \frac{1}{s^5}$

- 1) In the circuit shown in the figure, M_1 is in saturation and has transconductance $g_m = 0.01$ siemens. Ignoring internal parasitic capacitances and assuming the channel length modulation λ to be zero, the small signal input pole frequency (in kHz) is _____

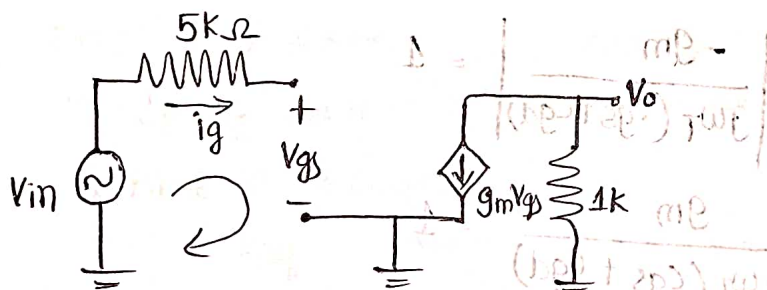
Soln # small signal modelling :-



small signal input = cut off frequency on pole frequency

voltage gain without feedback capacitance 50 pF :-

small signal model without 50 pF :-



KVL on i/p side :-

$$-V_{in} + 5k \cdot i_g + V_{gs} = 0 \quad (i_g = 0)$$

$$\Rightarrow V_{in} = V_{gs}$$

$$V_o = -g_m V_{gs} (1k)$$

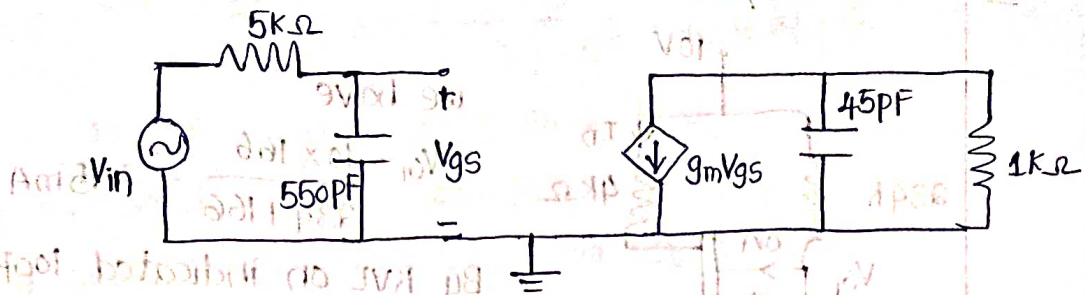
$$A_v' = \frac{V_o}{V_{in}} = \frac{-g_m V_{gs} (1000)}{V_{gs}} = -0.01 \times 1000 = -10$$

By miller's theorem

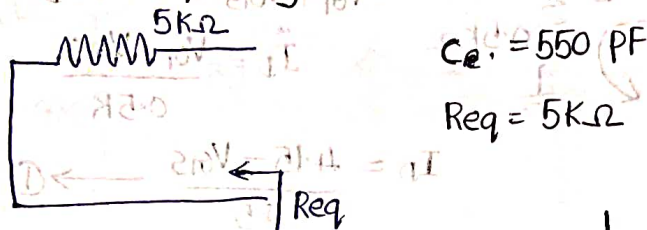
$$C_{mi} = C(1 - A_v) = 50(1 + 10) = 550 \text{ pF}$$

$$C_{mo} = C\left(1 - \frac{1}{A_v}\right) = 50\left(1 - \frac{1}{10}\right) = 45 \text{ pF}$$

small signal modelling including miller's effect:-



For input frequency we need Req across 550 pF



$$C_e = 550 \text{ pF}$$

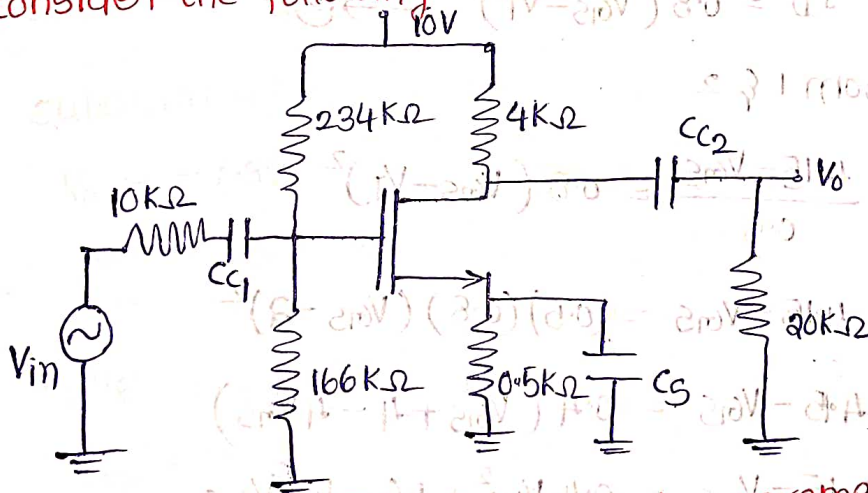
$$R_{eq} = 5 \text{ k}\Omega$$

Input cut off frequency $f_i = \frac{1}{2\pi R_{eq} C_i}$

$$f_i = \frac{1}{2 \times 3.14 \times 5000 \times 550 \times 10^{-12}}$$

$$f_i = 57.8745 \text{ kHz}$$

a) consider the following circuit



For the circuit above, the transistor parameters are $k_n = 0.8 \text{ mA/V}^2$, $V_{TN} = 2\text{V}$, $\lambda = 0$, $C_{gs} = 100 \text{ pF}$ and $C_{gd} = 20 \text{ pF}$

determine

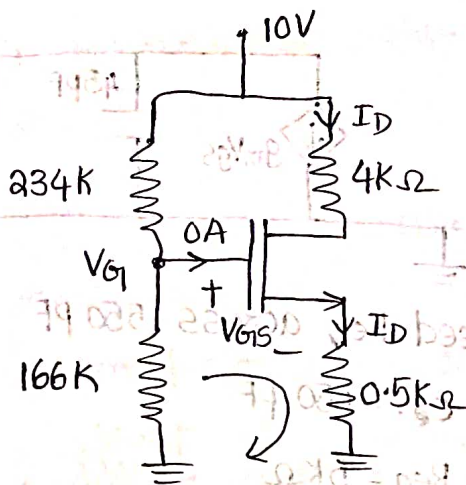
a) midband voltage gain

b) miller capacitance

c) the upper 3-dB frequency

assume $k_n = \frac{1}{2} \mu_n C_{ox} \frac{W}{L}$ and C_{c1}, C_{c2}, C_s are very high capacitances.

Soln # DC analysis:-



we have

$$V_{G1} = \frac{10 \times 166}{234 + 166} = 4.15 \text{ mA}$$

By KVL on indicated loop,

$$-V_{G1} + V_{GS} + 0.5K I_D = 0$$

$$I_D = \frac{V_{G1} - V_{GS}}{0.5K}$$

$$I_D = \frac{4.15 - V_{GS}}{0.5} \rightarrow \textcircled{1}$$

we know that current eqⁿ in saturation region

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

$$I_D = K_n (V_{GS} - V_T)^2$$

$$I_D = 0.8 (V_{GS} - V_T)^2 \rightarrow \textcircled{2}$$

From 1 & 2

$$\Rightarrow \frac{4.15 - V_{GS}}{0.5} = 0.8 (V_{GS} - V_T)^2$$

$$\Rightarrow 4.15 - V_{GS} = (0.5)(0.8)(V_{GS} - 2)^2$$

$$\Rightarrow 4.15 - V_{GS} = 0.4 (V_{GS}^2 + 4 - 4V_{GS})$$

$$\Rightarrow 4.15 - V_{GS} = 0.4 V_{GS}^2 + 1.6 - 1.6 V_{GS}$$

$$\Rightarrow 0.4 V_{GS}^2 - 0.6 V_{GS} - 2.55 = 0$$

$$V_{GS1} = 3.3839 \text{ V}$$

$$V_{GS2} = -1.8839 \text{ V} \rightarrow \text{Not valid}$$

$$V_{GS1} = 3.384 \text{ V}$$

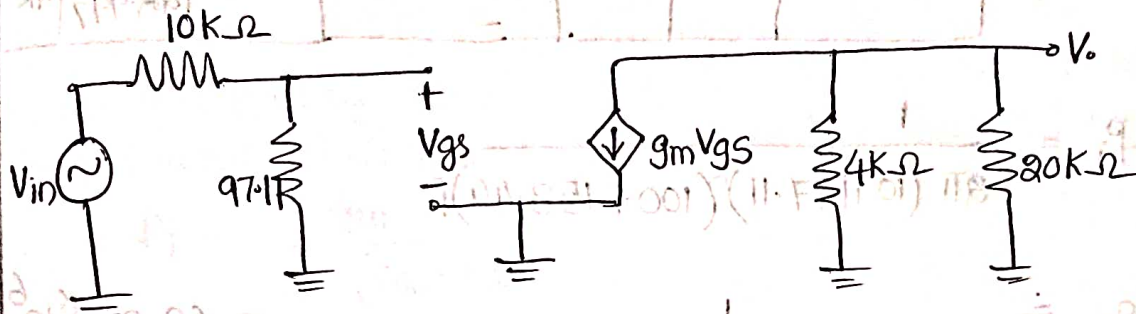
$$I_D = 0.8 (3.384 - 2)^2 = 1.53 \text{ mA}$$

$$g_m = \frac{2I_D}{V_{GS} - V_T} = \frac{2 \times 1.53}{3.384 - 2} = 2.21 \text{ mS}$$

$r_o = \infty$ (open circuit) since $\lambda = 0$

a) mid band voltage gain:-

small signal model at mid frequency:-



$$V_o = -g_m V_{GS} (4k \parallel 20k)$$

$$V_o = -2.21 \times V_{GS} \times (3.33) = -7.3593 V_{GS} \longrightarrow (i)$$

From input side:-

$$V_{GS} = \frac{V_{in} \times 97.11}{97.11 + 10} = 0.9066 V_{in} \longrightarrow (ii)$$

substituting (ii) in (i)

$$V_o = -7.3593 (0.9066 V_{in})$$

$$A_v = \frac{V_o}{V_{in}} = -6.672$$

b) miller capacitance:

$$C_{mi} = C(1 - A_v) = C_{gd}(1 - A_v)$$

$$C_{mi} = 20(1 + 6.672)$$

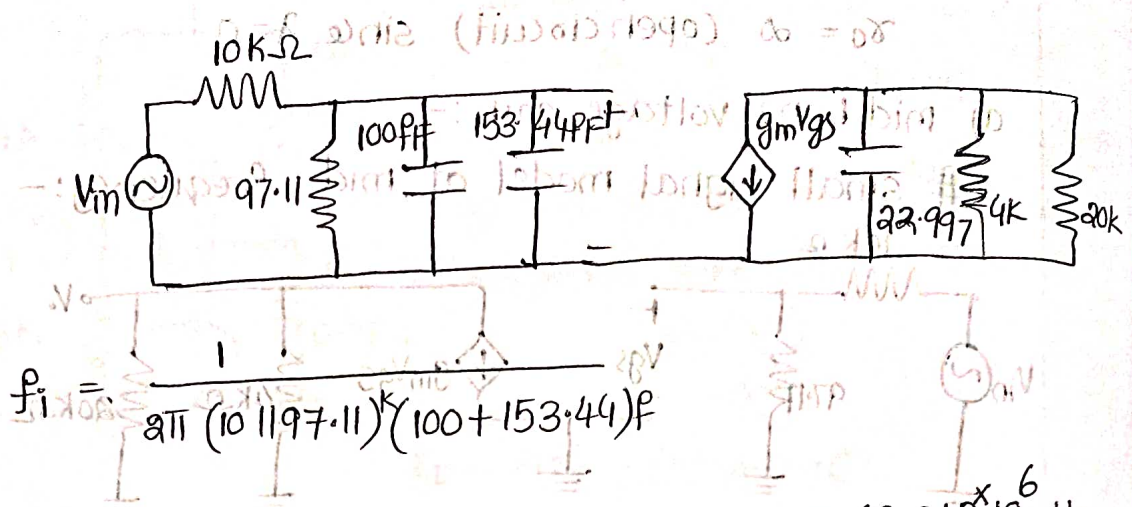
$$C_{mi} = 153.44 \text{ pF}$$

$$C_{mo} = C \left(1 - \frac{1}{A_v}\right) = C_{gd} \left(1 - \frac{1}{A_v}\right)$$

$$C_{mo} = 20 \left(1 + \frac{1}{6.672}\right)$$

$$C_{mo} = 22.997 \text{ pF}$$

c) High frequency analysis:
small signal equivalent circuit @ high frequency:-



$$f_i = \frac{1}{2\pi (10 \parallel 97.11) (100 + 153.44) \text{ pF}}$$

$$f_i = \frac{1}{2\pi (9.06) \times 10^3 \times (253.44) \times 10^{-15}} = 69.313 \times 10^6 \text{ Hz}$$

$$f_o = \frac{1}{2\pi (4\text{k} \parallel 20\text{k}) (22.997 \text{ pF})}$$

$$f_o = \frac{1}{2\pi \times 3.33\text{k} \times 22.997} = 2.08 \times 10^9 \text{ Hz}$$

overall upper cut off frequency

$$f = \min(f_i, f_o) = 69.313 \times 10^6 \text{ Hz}$$

3) Determine the unity-gain bandwidth of a FET
consider an n-channel MOSFET with parameters
 $k_n = 1.5 \text{ mA/V}^2$, $V_{TN} = 0.4 \text{ V}$, $\lambda = 0$, $C_{gd} = 10 \text{ pF}$ and $C_{gs} = 50 \text{ pF}$
Assume that transistor is biased at $V_{GS} = 0.8 \text{ V}$

Soln

$$K_n = \frac{1}{2} \mu_n C_{ox} \frac{W}{L}$$

$$2K_n = \mu_n C_{ox} \frac{W}{L}$$

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TN})$$

$$= 2K_n (V_{GS} - V_{TN})$$

$$= 2 \times 1.5 (0.8 - 0.4)$$

$$g_m = 1.2 \text{ mA/V}$$

unity gain frequency

$$f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})} = \frac{1.2 \times 10^{-3}}{2 \times \pi \times (10 + 50) \times 10^{-15}}$$

$$f_T = 3.18 \times 10^9 \text{ Hz}$$

$$f_T = 3.18 \text{ GHz}$$

4) The parameters of MOSFET are $k_n = 1.2 \text{ mA/V}^2$, $V_{TN} = 0.5 \text{ V}$, $\lambda = 0$, $C_{gd} = 8 \text{ fF}$ and $C_{gs} = 60 \text{ fF}$. The unity gain frequency is found to be $f_T = 3 \text{ GHz}$. Determine the transconductance and the bias current of MOSFET.

Soln

$$f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})}$$

$$g_m = f_T \times 2\pi \times (C_{gs} + C_{gd})$$

$$= 3 \times 10^9 \times 2 \times \pi \times (8 + 60) \times 10^{-15}$$

$$g_m = 1.282 \text{ mA/V}$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

$$I_D = k_n (V_{GS} - V_T)^2$$

we have $g_m = 2k_n (V_{GS} - V_T)$

$$V_{GS} - V_T = \frac{g_m}{2k_n} = \frac{1.282}{2 \times 1.2} = 0.534$$

$$V_{GS} = \frac{g_m}{2k_n}$$

$$\therefore I_D = k_n (V_{GS} - V_T)^2$$

$$= 1.2 \times (0.534)^2$$

$$I_D = 0.342 \text{ mA}$$

multistage amplifiers

Before understanding multistage amplifiers, let us understand common gate amplifier with active load. Active load means load resistance is not a passive resistor but it is another transistor. Transistor is an active device.

In multistage amplifiers the output of one transistor is acting as input to another transistor. Transistor itself acting as load of another transistor.

Body effect on Amplifier:-

Usually source and body are short circuited in MOSFET. But if we apply a voltage at body terminal then electric field changes, which results in voltage required for inversion also changes.

$\Rightarrow V_T$ (Threshold voltage) changes.

We knew that

in saturation region

Drain current $I_D \propto (V_{GS} - V_T)^2$

Since V_T changes I_D also changes.

We have transconductance

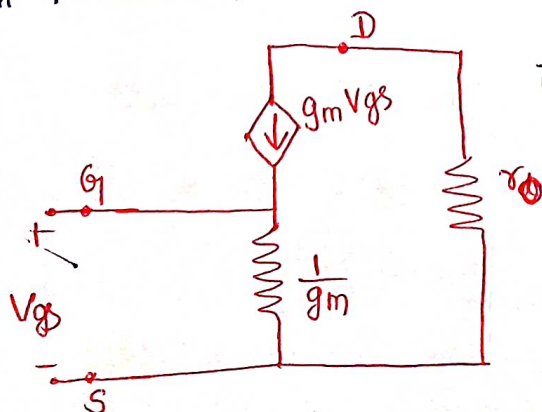
$$g_m = \frac{\partial I_D}{\partial V_{GS}} \text{ also changes}$$

$$g_{mb} = \frac{\partial I_D}{\partial V_T} \text{ also changes}$$

($g_{mb} \rightarrow$ Transconductance w.r.t. body terminal)

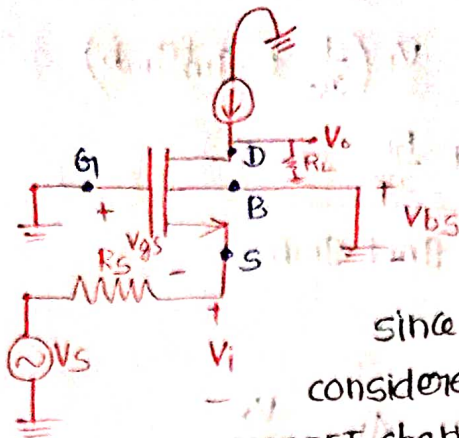
$\rightarrow$ Transconductance by varying body potential

T-model for MOSFET:-



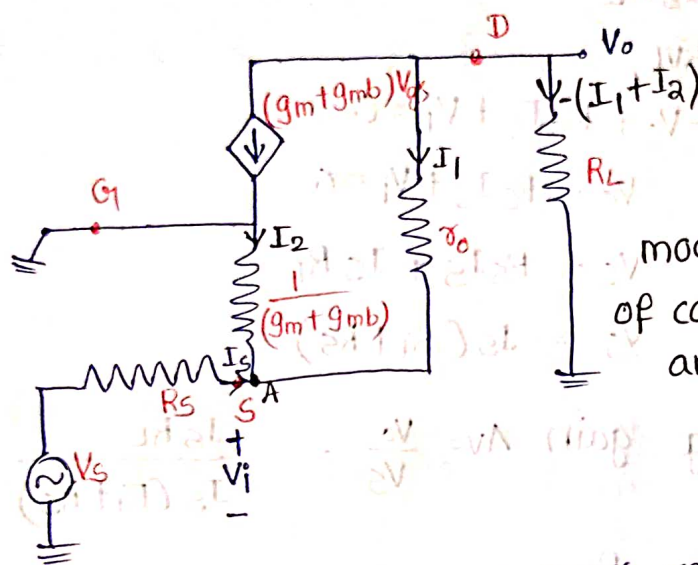
T model of MOSFET without Body effect.

common gate Amplifier including body effect:-



Since G & B are connected together we have $V_{gs} = V_{bs}$

Since body terminal also considered the modelling of MOSFET changes



modified T-model of common source amplifier

1) Input resistance R_i (Ignore source resistance)

$$R_i = \frac{V_i}{I_S}$$

Applying KCL at Node A:

$$I_S + I_2 + I_1 = 0$$

$$I_S = -I_2 - I_1$$

$$I_1 = \frac{V_0 - V_i}{r_o} \quad I_2 = \frac{0 - V_i}{\frac{1}{(g_m + g_{mb})}} \Rightarrow I_2 = -(g_m + g_{mb}) V_i$$

$$\Rightarrow I_S = (g_m + g_{mb}) V_i - \left(\frac{V_0 - V_i}{r_o} \right)$$

$$I_S = (g_m + g_{mb}) V_i + \left(\frac{V_i - V_0}{r_o} \right)$$

$$I_S = (g_m + g_{mb}) V_i + \frac{V_i}{r_o} + \frac{I_S R_L}{r_o}$$

$$V_0 = -(I_1 + I_2) R_L$$

$$V_0 = +I_S R_L$$

$$I_S = V_i \left(\frac{1}{r_{o1}} + g_m + g_{mb} \right) - I_S \frac{R_L}{r_{o1}}$$

$$I_S \left(1 + \frac{R_L}{r_{o1}} \right) = V_i \left(\frac{1}{r_{o1}} + g_m + g_{mb} \right)$$

$$\frac{V_i}{I_S} = \frac{1 + \frac{R_L}{r_{o1}}}{\frac{1}{r_{o1}} + g_m + g_{mb}}$$

a) voltage gain:

$$\text{voltage gain } A_v = \frac{V_o}{V_i}$$

$$V_o = I_S R_L$$

By KVL,

$$-V_S + R_S I_S + V_i = 0$$

$$V_S = R_S I_S + V_i$$

$$V_S = R_S I_S + I_S R_i$$

$$V_S = I_S (R_i + R_S)$$

$$\text{voltage gain } A_v = \frac{V_o}{V_S} = \frac{I_S R_L}{I_S (R_i + R_S)}$$

$$A_v = \frac{R_L}{R_i + R_S}$$

$$A_v = \frac{R_L}{R_S + \frac{1 + \frac{R_L}{r_{o1}}}{\frac{1}{r_{o1}} + g_m + g_{mb}}}$$

open circuit voltage gain ($R_L \rightarrow \infty$)

$$A_v = \frac{R_L}{R_S + \frac{1 + \frac{R_L}{r_{o1}}}{\frac{1}{r_{o1}} + g_m + g_{mb}}}$$

$$A_v = \frac{1}{\frac{R_S}{R_L} + \frac{\frac{1}{R_L} + \frac{1}{r_{o1}}}{\frac{1}{r_{o1}} + g_m + g_{mb}}} \quad \left[\begin{array}{l} \text{Dividing numerator} \\ \& \text{denominator by} \\ R_L \end{array} \right]$$

$$A_v = \frac{1}{\frac{R_S}{R_L} + \frac{\frac{1}{R_L} + \frac{1}{r_{o1}}}{\frac{1}{r_{o1}} + g_m + g_{mb}}}$$

$$A_v = \frac{I_1}{V_{i_0}} \quad \text{as } R_L \rightarrow \infty$$

$$\frac{R_S}{R_L} \rightarrow 0 \text{ and } \frac{1}{R_L} \rightarrow 0$$

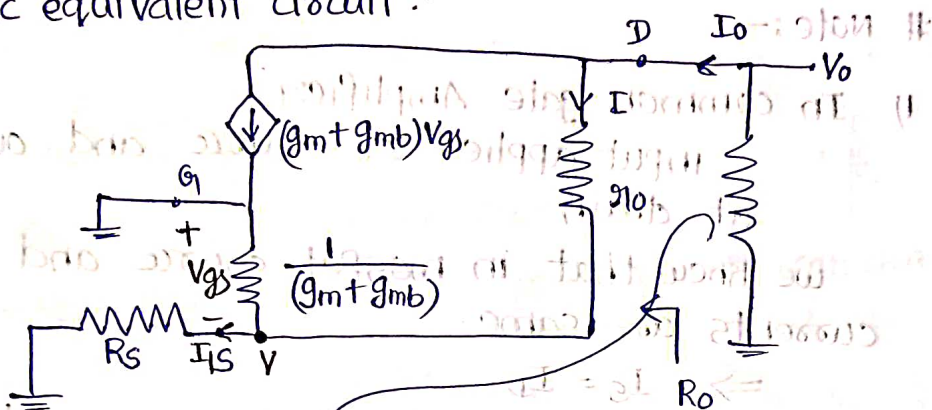
$$A_v = \frac{\frac{1}{r_{i_0}} + g_m + g_{mb}}{\frac{1}{r_{i_0}}}$$

$$A_v = \frac{\frac{1}{r_{i_0}} + g_m + g_{mb}}{\frac{1}{r_{i_0}}}$$

$$A_v = 1 + (g_m + g_{mb}) r_{i_0}$$

3) output resistance $R_o = \frac{V_o}{I_o} \Big|_{V_S=0}$

AC equivalent circuit :-



From figure :

$$I_o = I + (g_m + g_{mb}) V_{gs} \quad (V_{gs} = 0 - V)$$

$$I_o = I + (g_m + g_{mb})(0 - V)$$

$$I_1 = I + (g_m + g_{mb}) V_{gs} = \frac{V}{R_S}$$

$$I + (g_m + g_{mb})(-V) = \frac{V}{R_S}$$

$$I = V \left[\frac{1}{R_S} + (g_m + g_{mb}) \right]$$

$$I_o = V \left(\frac{1}{R_S} + (g_m + g_{mb}) \right) - V(g_m + g_{mb})$$

$$I_o = \frac{V}{R_S} + V(g_m + g_{mb}) - V(g_m + g_{mb})$$

$$I_o = \frac{V}{R_S} \quad \Rightarrow \quad V = I_o R_S$$

By KVL,

$$-V_o + r_o I + V = 0$$

$$V_o = r_o I + V$$

$$V_o = V + r_o \left(\frac{1}{R_S} + g_m + g_{mb} \right) V = V_A$$

$$V_o = V \left[1 + \frac{r_o}{R_S} + (g_m + g_{mb}) r_o \right] \quad \text{--- (2)}$$

$$\frac{2}{1} \Rightarrow \frac{V_o}{I_o} = \frac{V \left(1 + \frac{r_o}{R_S} + (g_m + g_{mb}) r_o \right)}{V/R_S}$$

$$R_o = \frac{V_o}{I_o} = R_S \left[1 + \frac{r_o}{R_S} + (g_m + g_{mb}) r_o \right]$$

Note: -

- 1) In common gate Amplifier, input applied at source and output taken at drain

we knew that in mosfet source and drain currents are same.

$$\Rightarrow I_S = I_D$$

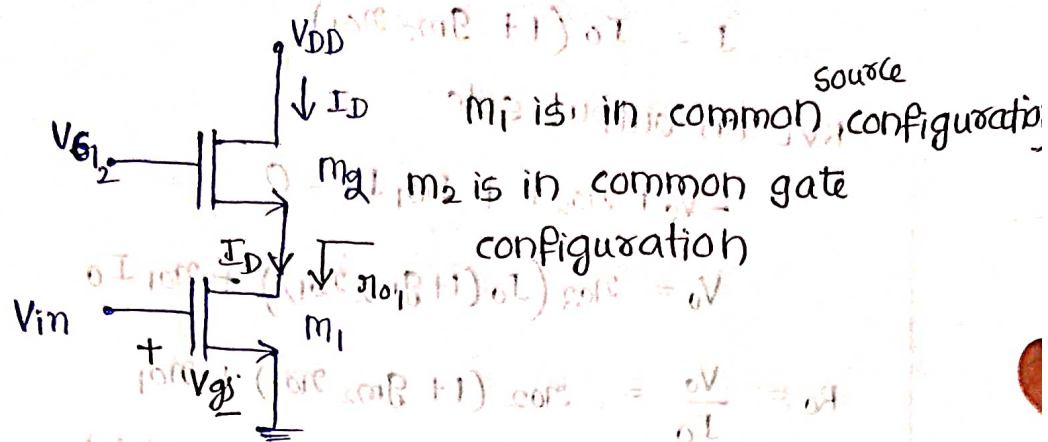
$\Rightarrow$ common gate Amplifier act as current buffer

- a) In common gate amplifier: high output impedance and low input impedance.

MOS cascode Amplifier :-

To increase the bandwidth, we use cascode connection

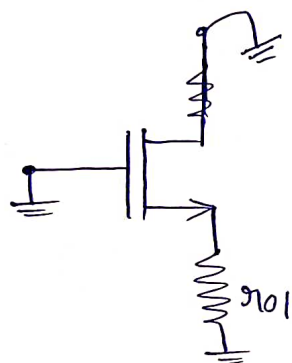
common source - common gate cascode connection :-



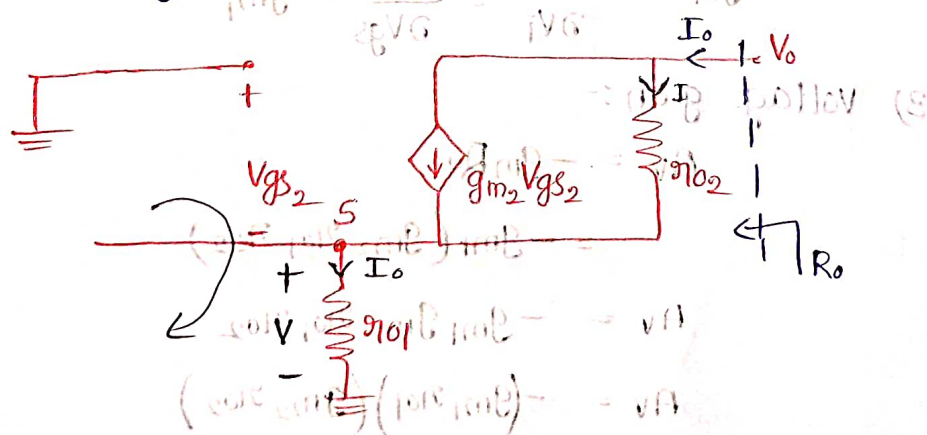
The output of m_1 is input of m_2 .

$\Rightarrow r_{o1}$ act as input to m_2 .

Therefore the cascode (CS-CG) amplifier can be drawn as



small signal modelling :-



1) output resistance $R_o = \frac{V_o}{I_o}$

By KVL,

$$V_{gs2} + V = 0$$

$$V_{gs2} = -V = -r_{o1} I_o$$

By KCL,

$$I_0 = g_{m2} V_{gs2} + I$$

$$I_0 = g_{m2} (-r_{o1} I_0) + I$$

$$I = I_0 (1 + g_{m2} r_{o1})$$

KVL on output side:-

$$-V_o + r_{o2} I + r_{o1} I_0 = 0$$

$$V_o = r_{o2} (I_0 (1 + g_{m2} r_{o1})) + r_{o1} I_0$$

$$R_o = \frac{V_o}{I_0} = r_{o2} (1 + g_{m2} r_{o1}) + r_{o1}$$

$$R_o = r_{o1} + r_{o2} + g_{m2} r_{o1} r_{o2} \quad ***$$

$$[R_o \approx g_{m2} r_{o1} r_{o2}]$$

a) overall transconductance :

$$g_m = \frac{\partial I_{out}}{\partial V_i}$$

$$I_{out} = I_D$$

$$V_i = V_{gs}$$

$$g_m = \frac{\partial I_{out}}{\partial V_i} = \frac{\partial I_D}{\partial V_{gs}} = g_{m1}$$

3) voltage gain:-

$$A_v = -g_m R_o$$

$$= -g_{m1} (g_{m2} r_{o1} r_{o2})$$

$$A_v = -g_{m1} g_{m2} r_{o1} r_{o2}$$

$$A_v = -(g_{m1} r_{o1}) (g_{m2} r_{o2})$$

#95 A depletion type N-channel MOSFET is biased in its linear region for use as a voltage controlled resistor.

Assume threshold voltage $V_{TN} = -0.5V$, $V_{GS} = 2V$, $V_{DS} = 5V$

$\frac{W}{L} = 100$, $C_{ox} = 10^{-8} \text{ F/cm}^2$ and $\mu_n = 800 \text{ cm}^2/\text{V-sec}$. The value of resistance of voltage controlled resistor (in Ω) is _____

Soln

For linear region

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

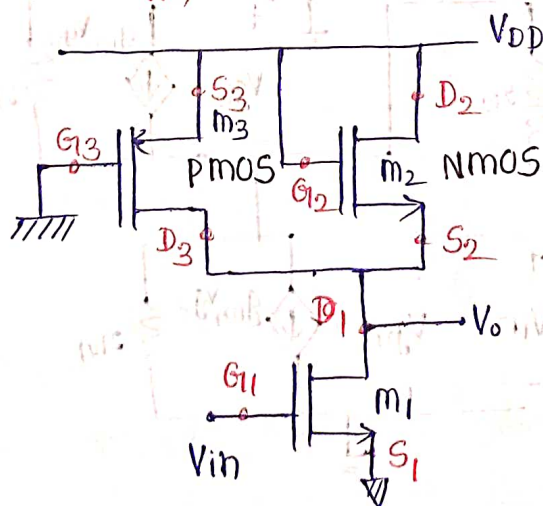
$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \left(\mu_n C_{ox} \frac{W}{L} \right) \left[(V_{GS} - V_T) - V_{DS} \right]$$

$$g_{ds} \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)$$

$$r_d = \frac{1}{g_{ds}} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)}$$

$$r_d = \frac{1}{800 \times 10^{-8} \times 100 \times (2 + 0.5)} = 500 \Omega$$

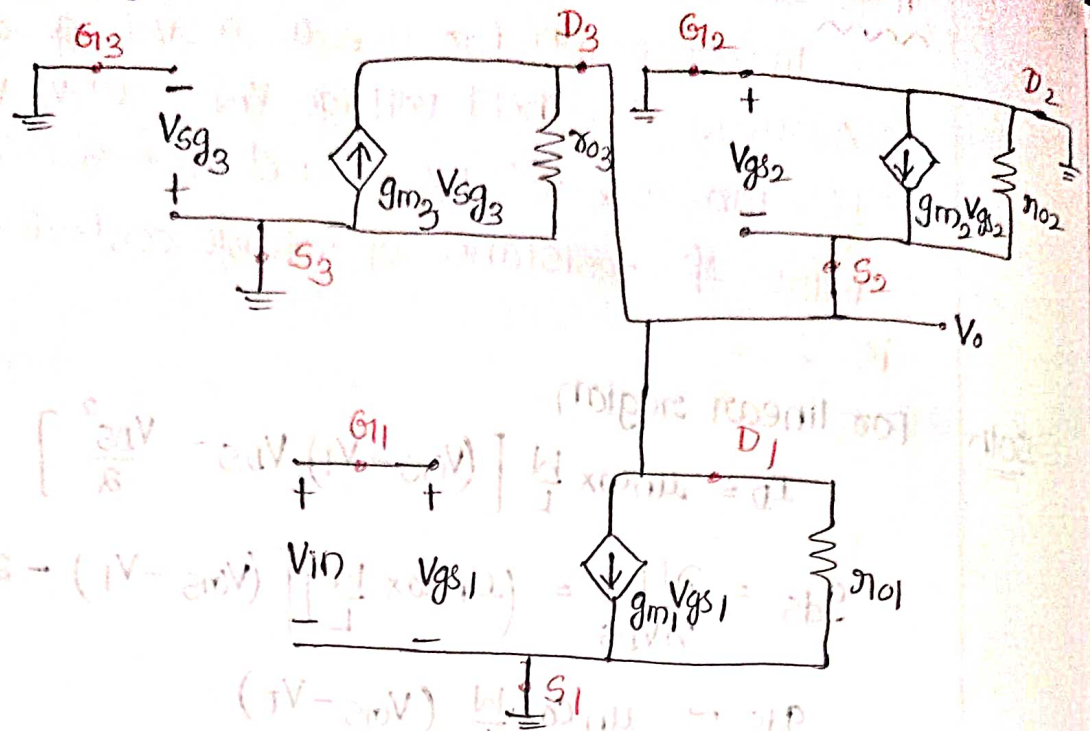
#96 In the circuit shown, the channel length modulation is non zero. Also the transistor operates in saturation and have negligible body effect. At small signal voltage gain $\left(\frac{V_o}{V_{in}} \right)$ of the circuit is _____



Soln

Since all MOSFET's are operated in saturation, so each MOSFET can be replaced with small signal model.

small signal model:-



From circuit:-

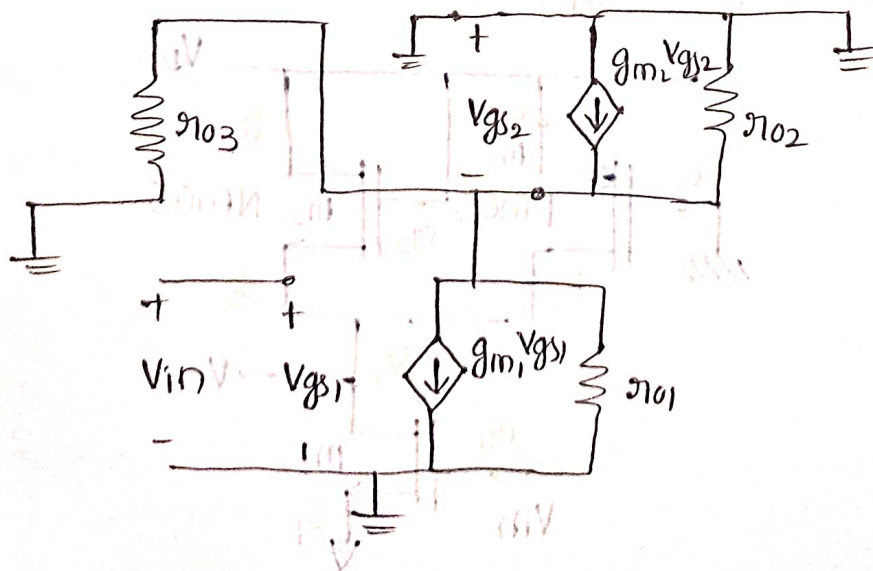
$$V_{sg3} = 0$$

$\Rightarrow g_{m3} V_{sg3} = 0$ (open circuited) only r_{o3} remained

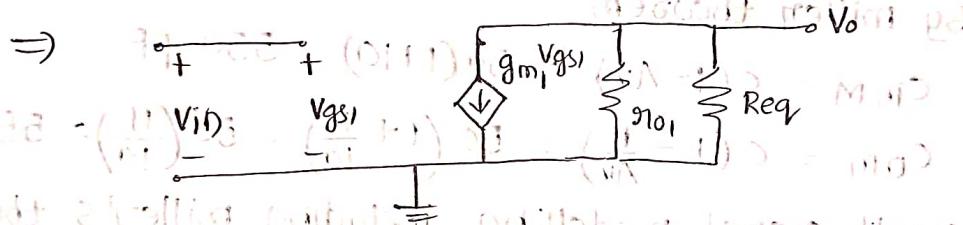
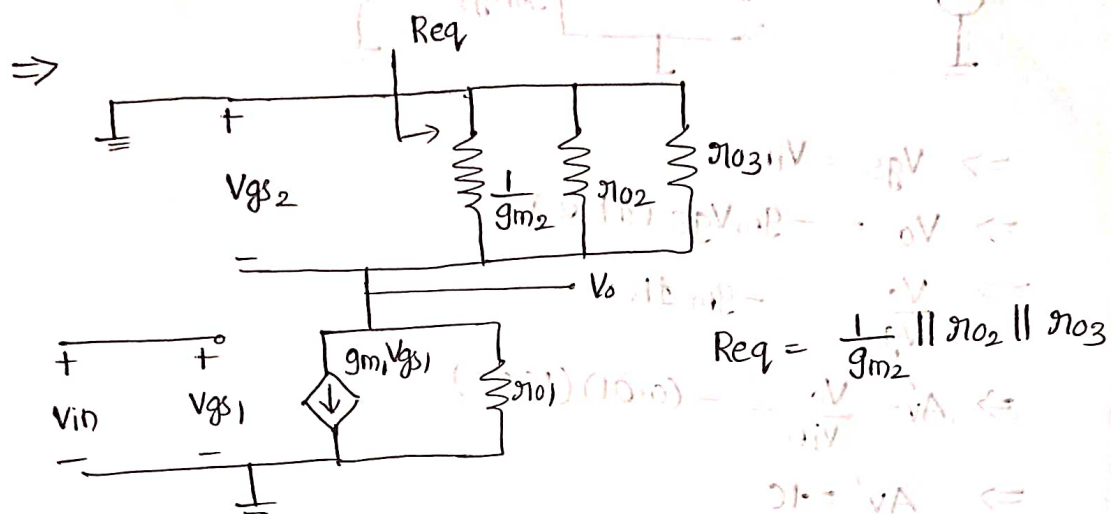
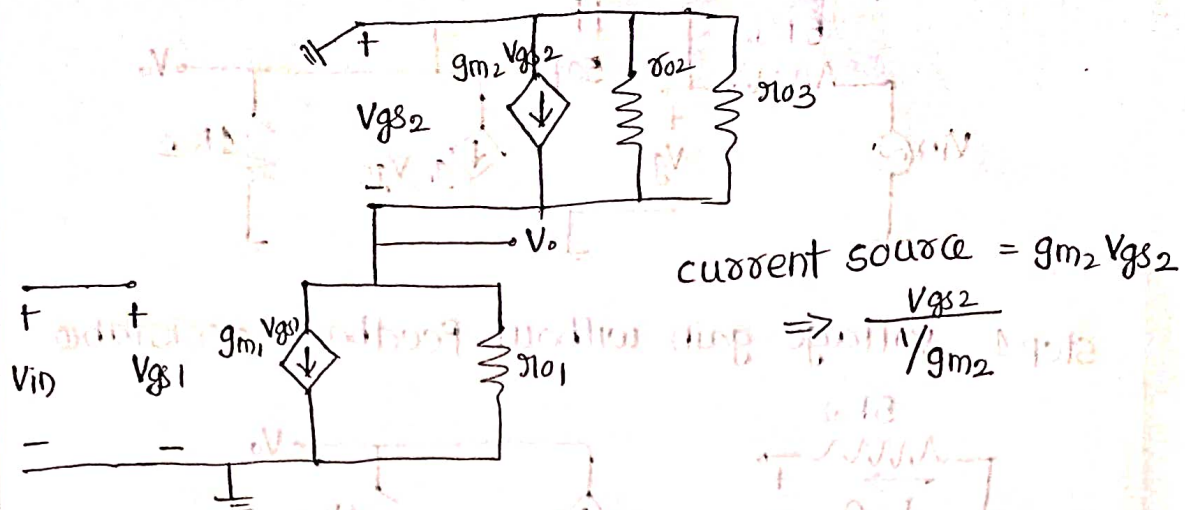
$$V_{gs2} = 0$$

$\Rightarrow g_{m2} V_{gs2} = 0$ (open circuited)

The circuit become



$$\Rightarrow r_{o2} \parallel r_{o3}$$

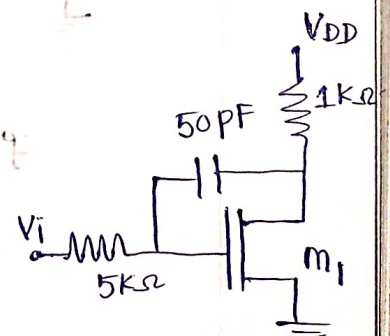


$$V_o = -g_{m1} V_{gs1} (r_{O1} \parallel Req)$$

$$\frac{V_o}{V_{gs1}} = -g_{m1} (r_{O1} \parallel \frac{1}{g_{m2}} \parallel r_{O2} \parallel n_{O3})$$

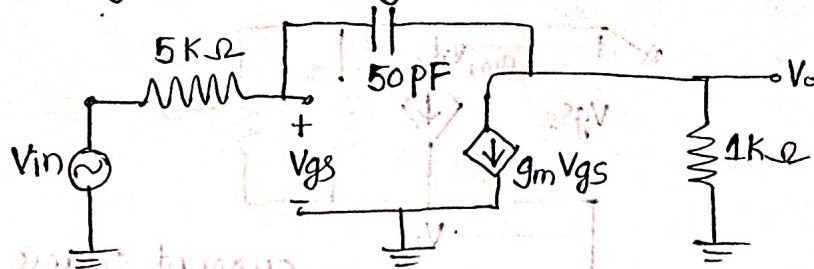
$$A_v = -g_{m1} (r_{O1} \parallel r_{O2} \parallel n_{O3} \parallel \frac{1}{g_{m2}})$$

97 In the circuit shown in the figure, Transistor m_1 is in saturation and has transconductance $g_m = 0.01$ Siemens. Ignoring parasitic capacitances and assuming the channel length modulation λ to be zero, the small signal input pole frequency (in Hz) is _____

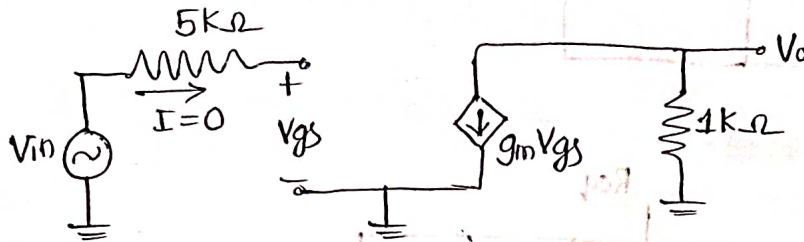


Soln

small signal modelling :-



step 1: voltage gain without feedback resistance



$$\Rightarrow V_{gs} = V_{in}$$

$$\Rightarrow V_o = -g_m V_{gs} (1k\Omega)$$

$$\Rightarrow \frac{V_o}{V_{gs}} = -g_m 1k$$

$$\Rightarrow A_v' = \frac{V_o}{V_{in}} = -(0.01)(1000)$$

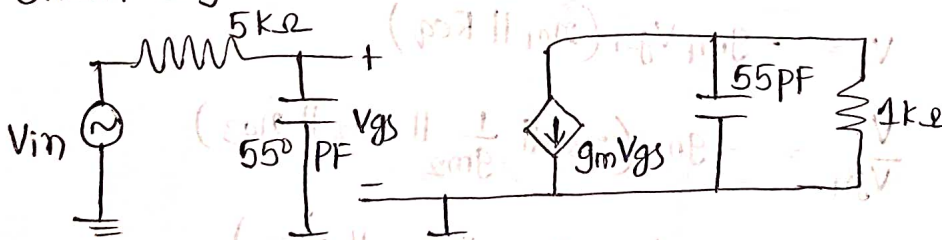
$$\Rightarrow A_v' = -10$$

By miller's theorem

$$C_{inM} = C(1 - A_v) = 50(1 + 10) = 550 \text{ pF}$$

$$C_{oM} = C(1 - \frac{1}{A_v}) = 50(1 + \frac{1}{10}) = 50(\frac{11}{10}) = 55 \text{ pF}$$

small signal modelling including miller's theorem



$$R = 5k\Omega$$

$$C = 550 \text{ pF}$$

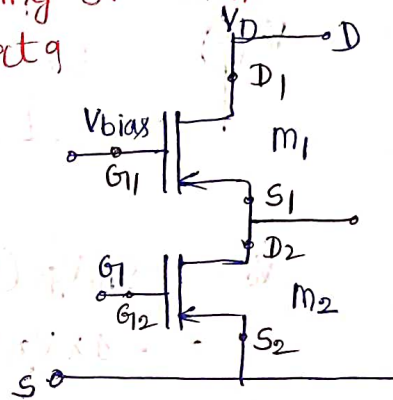
$$f_L = \frac{1}{2\pi RC}$$

$$= \frac{1}{2 \times 3.14 \times 5 \times 10^3 \times 550 \times 10^{-12}}$$

$$f_L = 57.8745 \text{ kHz}$$

#Q8 Two identical PMOS transistors are connected as shown below. The circuit is used as an amplifier with the input connected b/w G_1 and S terminals and the output taken b/w D and S terminals. V_{bias} and V_D are so adjusted that both transistors are in saturation. The transconductance of the combination is defined as $\frac{\partial I_D}{\partial V_{G1S}}$ while the output resistance is $r_o = \frac{\partial V_{G1S}}{\partial I_D}$ where I_D is the current flowing into the gain of m_2 . Let g_{m1}, g_{m2} be the transconductances & r_{o1} & r_{o2} be output resistances of transistor m_1 & m_2 respectively. Which of the following statement about estimates for g_m & r_o is correct?

- a) $g_m = g_{m1} g_{m2} r_{o2}$ $r_o = r_{o1} + r_{o2}$
 b) $g_m = g_{m1} + g_{m2}$ $r_o = r_{o1} + r_{o2}$
 c) $g_m = g_{m2}$ $r_o = r_{o1} g_{m2} r_{o2}$
 d) $g_m = g_{m2}$ $r_o = r_{o2}$



Soln

m_2 = common source Amplifier

m_1 = common Gate Amplifier

Transconductance due to transistor @ input

$$\Rightarrow g_m = g_{m2}$$

$$r_o = g_{m2} r_{o1} r_{o2}$$

cascode:

Transconductance

g_m = Transconductance of transistor connected at input terminal

r_o :

$$r_o = g_{m(o/p)} r_{o1} r_{o2}$$

$\rightarrow$ Transconductance of transistor connected to output.

#99: In the circuit shown below figure out voltage gain

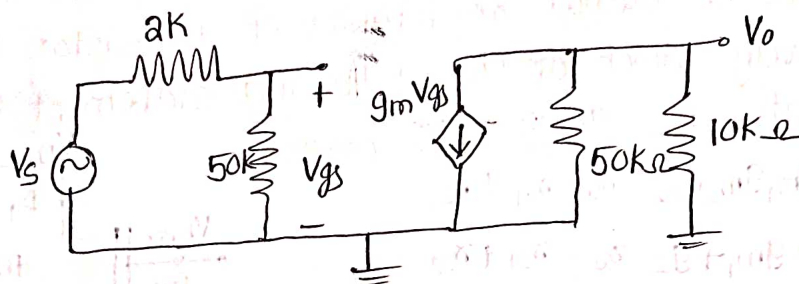
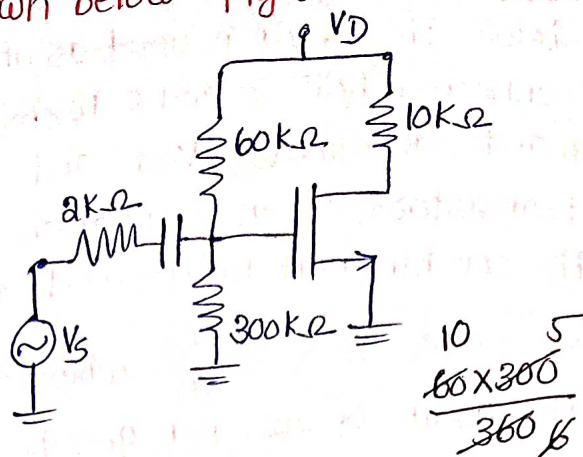
$$\frac{V_o}{V_s}$$

$$g_m = 1 \text{ mA/V}$$

$$r_o = 50 \text{ k}\Omega$$

soln

small signal modelling :-



$$V_o = -g_m V_{gs} (50 \text{ k}\Omega \parallel 10 \text{ k}\Omega)$$

$$= -1 \times V_{gs} \times \left(\frac{50 \times 10}{60} \right)$$

$$V_o = -\frac{V_{gs} \times 50}{6}$$

$$V_{gs} = \frac{V_s \times 50}{52} = \frac{V_s \times 25}{26}$$

$$V_o = -\left(\frac{V_s \times 25}{26} \right) \left(\frac{50}{6} \right)$$

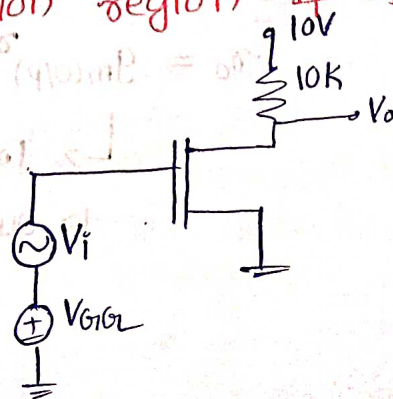
$$\frac{V_o}{V_s} = \frac{-25 \times 50}{26 \times 6} = -8.012$$

#910 For the circuit shown below, the transistor parameters $V_{th} = 2\text{V}$, $k_n = 0.5 \text{ mA/V}^2$ and $\lambda = 0$. The transistor is in saturation region.

i) Find V_{gs}

ii) Find g_m & r_o

iii) Find voltage gain



soln

DC analysis

Given that transistor is in saturation mode

$$\Rightarrow I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \quad K_n = \frac{1}{2} \mu_n C_{ox} \frac{W}{L}$$

$$0.4 = \frac{1}{2} \times 0.5 (V_{GS} - 2)^2$$

$$(V_{GS} - 2)^2 = 0.8$$

$$V_{GS} = 2 + \sqrt{0.8}$$

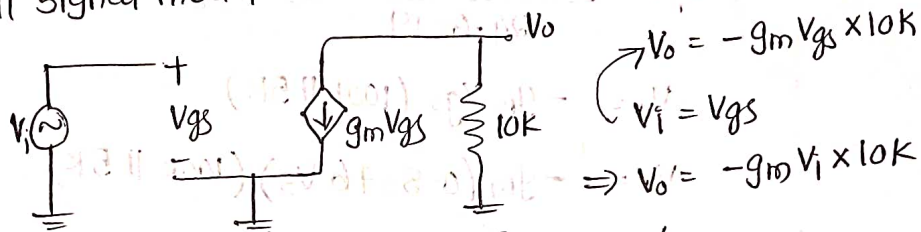
$$V_{GS} = 2.89 \text{ V}$$

$$V_{GS} = V_{G1} = 2.89$$

$$g_m = \frac{2I_D}{V_{GS} - V_T} = \frac{2 \times 0.4}{0.89} = 0.89 \text{ mA/V}^2$$

$$r_o = \infty$$

small signal model:



$$\Rightarrow \frac{V_o}{V_i} = -g_m (10k) = -0.89 \times 10^{-3} \times 10 \times 10^3 = -8.9$$

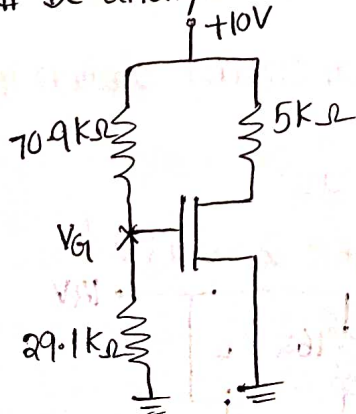
q11: consider the common source amplifier, the transistor parameters are $V_{th} = 1.5 \text{ V}$, $K_n = \mu_n C_{ox} \frac{W}{L} = 0.5 \text{ mA/V}^2$, $\lambda = 0.01 \text{ V}^{-1}$. Find

i) The small signal voltage gain

ii) Input & output impedance

soln

DC analysis



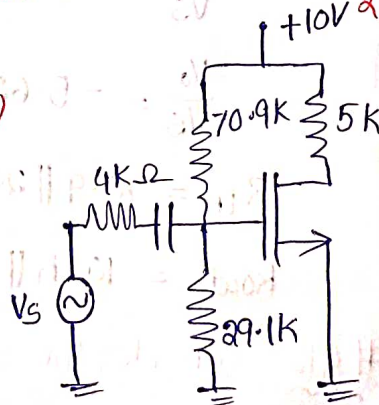
$$V_{G1} = \frac{10 \times 29.1}{70.9 + 29.1} = 2.91 \text{ V}$$

$$V_S = 0$$

$$\Rightarrow V_{GS} = V_{G1} - V_S = 2.91 \text{ V}$$

$$I_D = \mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 = 0.5 (2.91 - 1.5)^2$$

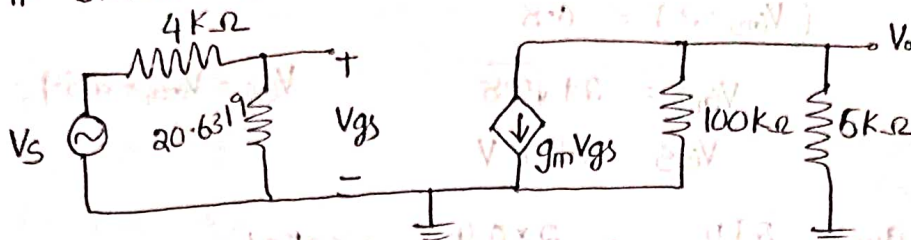
$$I_D = 0.994 \text{ mA} \approx 1 \text{ mA}$$



$$g_m = \frac{2I_D}{V_{GS} - V_T} = \frac{2(0.994)}{2.91 - 1.5} = 1.4099 \approx 1.41 \text{ mA/V}$$

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.01 \times 1} = 100 \text{ k}\Omega$$

small signal modelling:



$$70.9 \parallel 29.1 = \frac{70.9 \times 29.1}{100} = 20.6319 \text{ k}\Omega$$

$$V_{GS} = \frac{V_S \times 20.6319}{24.6319} \Rightarrow V_{GS} = 0.8376 V_S$$

$$V_O = -g_m V_{GS} (100 \text{ k}\Omega \parallel 5 \text{ k}\Omega)$$

$$V_O = -g_m (0.8376 V_S) (100 \text{ k}\Omega \parallel 5 \text{ k}\Omega)$$

$$\frac{V_O}{V_S} = -g_m (0.8376) (100 \text{ k}\Omega \parallel 5 \text{ k}\Omega)$$

$$\frac{V_O}{V_S} = -1.41 \times 0.8376 \times (100 \parallel 5 \text{ k})$$

$$\frac{V_O}{V_S} = -1.41 \times 0.8376 \times 4.76$$

$$\frac{V_O}{V_S} = -5.62$$

$$R_{in} = 70.9 \parallel 29.1 = 20.6319 \text{ k}\Omega$$

$$R_{out} = 100 \text{ k}\Omega \parallel 5 \text{ k}\Omega = 4.76 \text{ k}\Omega$$

Q12 consider the source follower circuit shown in figure.

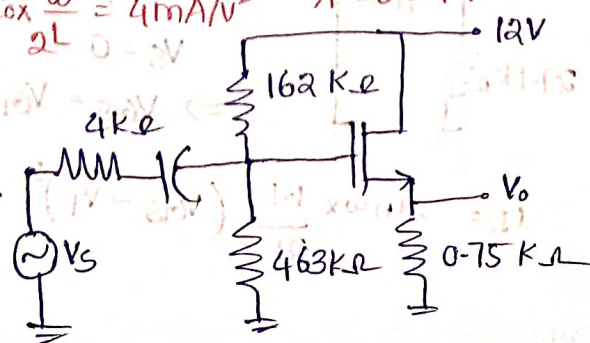
The transistor parameters are

$$V_{th} = 1.5 \text{ V} \quad K_n = \mu_n C_{ox} \frac{W}{L} = 4 \text{ mA/V}^2 \quad \lambda = 0.01 \text{ V}^{-1}$$

Find 1) g_m

$$2) A_v = \frac{V_O}{V_S}$$

$$3) R_o$$



DC analysis :

$$V_{G1} = \frac{12 \times 463}{463 + 162} = 8.8896 \text{ V}$$

By KVL,

$$-V_{G1} + V_{GS} + 0.75 \text{ K} \cdot I_D = 0$$

$$V_{GS} = V_{G1} - 0.75 I_D$$

We knew that

$$I_D = \mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2$$

$$I_D = 4 (V_{G1} - 0.75 I_D - V_T)^2$$

$$I_D = 4 (8.8896 - 0.75 I_D - 1.5)^2$$

$$0.25 I_D = (7.3896 - 0.75 I_D)^2$$

$$0.25 I_D = 54.606 + 0.5625 I_D^2 - 11.0844 I_D$$

$$0.5625 I_D^2 - 11.3344 I_D + 54.606 = 0$$

 ~~I_D~~

$$0.5625 I_D^2 - 11.3344 I_D + 54.606 = 0$$

$$I_{D1} = 12.179 \text{ mA}$$

$$I_{D2} = 7.970 \text{ mA}$$

$$V_{DS} = V_D - V_S$$

$$V_D = 12 \text{ V}$$

$$V_S = 0.75 I_D$$

$$V_{DS} = 12 - 0.75 I_D$$

$$V_{DS1} = 12 - 0.75 (12.179) = 2.86 \text{ V}$$

$$V_{DS2} = 12 - 0.75 (7.97) = 6.022 \text{ V}$$

$$V_{GS1} = V_{G1} - 0.75 (12.179) = 8.8896 - \left(\frac{3}{4} \times 12.179\right) = -0.2446$$

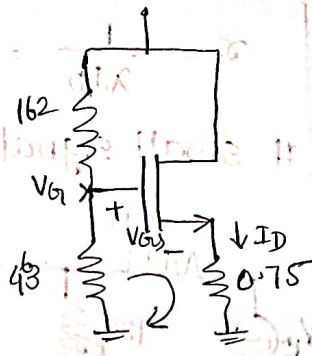
$$V_{GS2} = V_{G1} - 0.75 (7.97) = 8.8896 - \left(\frac{3}{4} \times 7.97\right) = 2.9121$$

$$V_{GS2} = 2.9121 \rightarrow \text{valid}$$

$$V_{DS2} = 6.022 \rightarrow \text{valid}$$

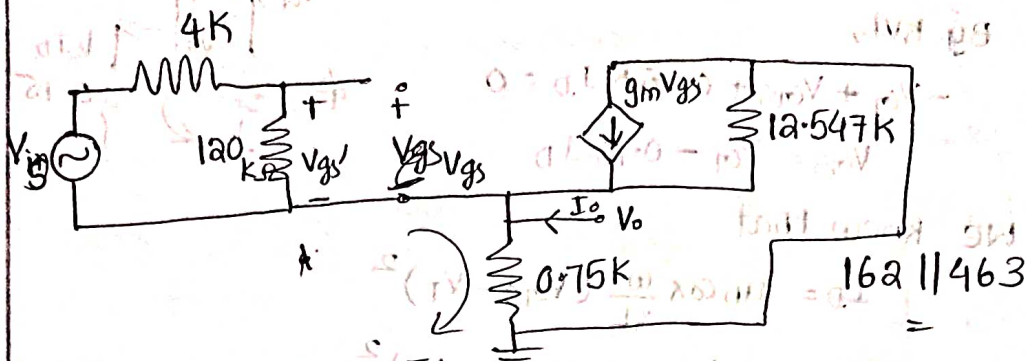
$$I_D = 7.97 \text{ mA}$$

$$g_m = \frac{2I_D}{V_{GS} - V_T} = \frac{2 \times 7.97}{2.9121 - 1.5} = 11.29 \text{ mA/V}$$



$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.01 \times 7.97} = 12.547 \text{ k}\Omega$$

small signal modelling:



$$V_o = -g_m V_{gs'} (0.75 \parallel 12.547)$$

$$V_o = 11.29 V_{gs'} \left(\frac{0.75 \times 12.547}{0.75 + 12.547} \right)$$

$$V_o = 7.989 V_{gs'}$$

$$V_{gs'} = \frac{V_s \times 120}{124} = 0.967 V_s$$

$$V_o = 7.989 (0.967 V_s)$$

$$\frac{V_o}{V_s} = 7.989 \times 0.967$$

By KVL,

$$V_{gs'} = V_{gs} + V_o$$

$$= V_{gs} + 7.989 V_{gs'}$$

$$V_{gs'} = \frac{1}{1 + 7.989} V_{gs}$$

$$V_o = 7.989 V_{gs'}$$

$$V_{gs'} = V_{gs} + V_o$$

$$V_{gs'} = V_{gs} + 7.989 V_{gs'}$$

$$V_{gs'} = \frac{1}{1 + 7.989} V_{gs}$$

$$0.967 V_s = V_{gs} (1 + 7.989)$$

$$V_S = \frac{V_{GS} (8.989)}{0.967}$$

$$\Rightarrow V_O = 7.989 V_{GS}$$

$$\frac{V_O}{V_S} = \frac{7.989 \times 0.967}{8.989}$$

$$A_v = \frac{V_O}{V_S} = 0.859 = 0.86$$

output resistance:

$$\text{set } V_S = 0 \Rightarrow V_{GS}' = 0$$

By KVL on input sides

$$V_{GS} + V_O = 0$$

$$V_{GS} = -V_O$$

By KCL at V_O :-

$$I_O + g_m V_{GS} = \frac{V_O}{0.75} + \frac{V_O}{80}$$

$$I_O - g_m V_O = \frac{V_O}{0.75} + \frac{V_O}{12.547}$$

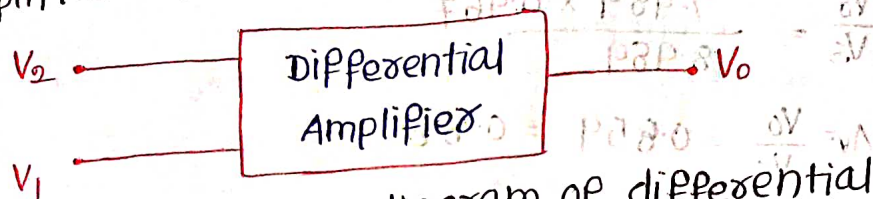
$$V_O \left[g_m + \frac{1}{0.75} + \frac{1}{12.547} \right] = I_O$$

$$R_o = \frac{V_O}{I_O} = \frac{1}{g_m + \frac{1}{0.75} + \frac{1}{12.547}}$$

$$R_o = \frac{1}{11.29 + \frac{1}{0.75} + \frac{1}{12.547}} = 78.72 \Omega$$

Differential Amplifiers in MOSFET

Differential Amplifier is an electronic circuit that amplifies difference b/w the input signals.



simple block diagram of differential amplifier

In differential amplifier, we have a kinds of input signals

- 1) Differential mode signal component: $V_{id} = V_2 - V_1$
- 2) common mode signal component: $V_{cm} = \frac{1}{2}(V_1 + V_2)$

- Differential mode signal component is a signal of interest. In differential amplifier we need to amplify this differential mode signal component.
- common mode signal component is typically a reference or noise level which is not desired. We don't want to amplify the common mode signal component.
- The output of differential amplifier is of the form

$$V_o = A_d V_{id} + A_{cm} V_{cm}$$

where V_{id} : differential mode signal component
 V_{cm} = common mode signal component
 A_d = Differential gain
 A_{cm} = common mode gain.

In general

A_d should be very high
 A_{cm} should be very less.

common mode rejection ratio: (CMRR)

Differential to common mode power gain ratio

$$\text{CMRR (in dB)} = 20 \log_{10} \left(\frac{A_d}{A_{cm}} \right)$$

cmRR should be as high as possible.

↳ This can be achieved only when A_d is high and A_{cm} must be low.

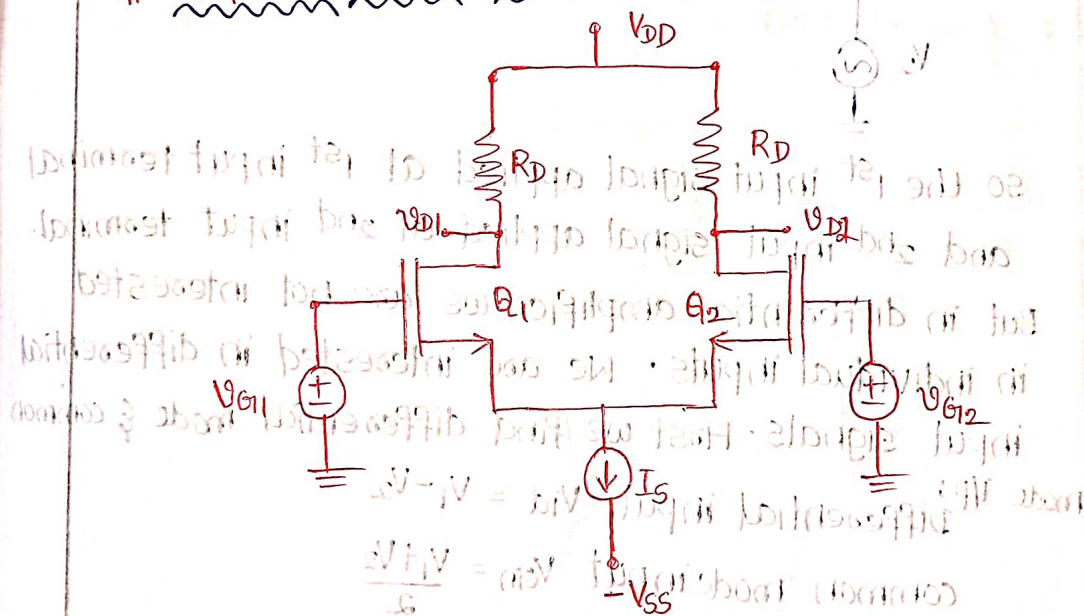
Ideally cmRR tends to infinity as A_{cm} tends to zero. But practically cmRR should be very high.

Advantages of differential amplifier:-

If there is a noise signal that is common to both inputs and outputs, so it will be cancelled.

⇒ Differential amplifier rejects circuit noise and power supply noise.

Implementation of mos differential Amplifier:-



For implementation of mos differential Amplifier, 2

mos transistors Q_1 and Q_2 are perfectly matched:

i) mos devices should be fabricated using same technology.

(i.e., same k_n' , C_{ox} and μ)

ii) mos transistors have same threshold voltage V_{th} .

iii) mos transistors have same W and L .
(same dimensions)

Two circuits arranged symmetrically:

i) same load resistance R_D

ii) source terminals of both devices join together

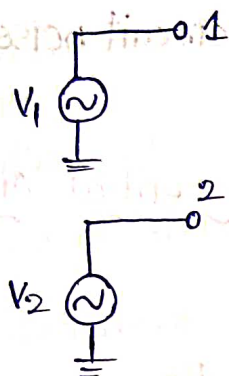
iii) Both devices are bias with equal gate voltage V_{GS} .

- Devices are biased using constant current source (I_{SS})
- FET's should not enter ohmic region of operation. That's why we biased both transistors, are biased using constant source.

signals in Differential Amplifier

Input signals :-

We have 2 inputs in signals in differential amplifier



so the 1st input signal applied at 1st input terminal and 2nd input signal applied at 2nd input terminal.

But in differential amplifier we are not interested in individual inputs. We are interested in differential input signals. First we find differential mode & common mode I/P:

Differential input $V_{id} = V_1 - V_2$

common mode input $V_{cm} = \frac{V_1 + V_2}{2}$

Now we split it into two parts: $\frac{V_{id}}{2}$, $-\frac{V_{id}}{2}$

The one part of splitted differential input applied at one terminal and 2nd part of splitted differential input at 2nd input terminal. The splitted differential input signal is superimposed on common mode signal, If common mode is present.

If common mode signal present then

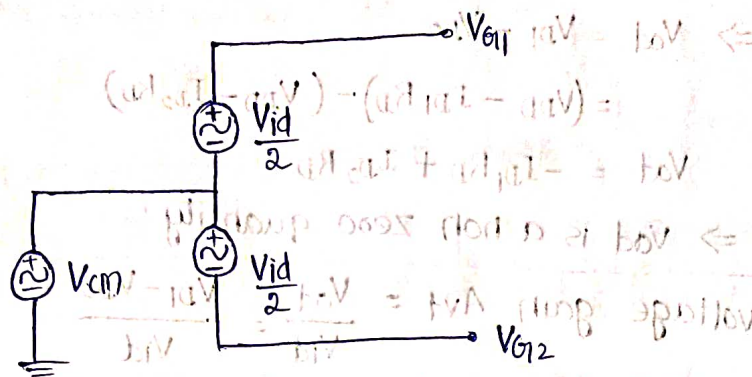
$$V_{o1} = V_{cm} + \frac{V_{id}}{2}$$

$$V_{o2} = V_{cm} - \frac{V_{id}}{2}$$

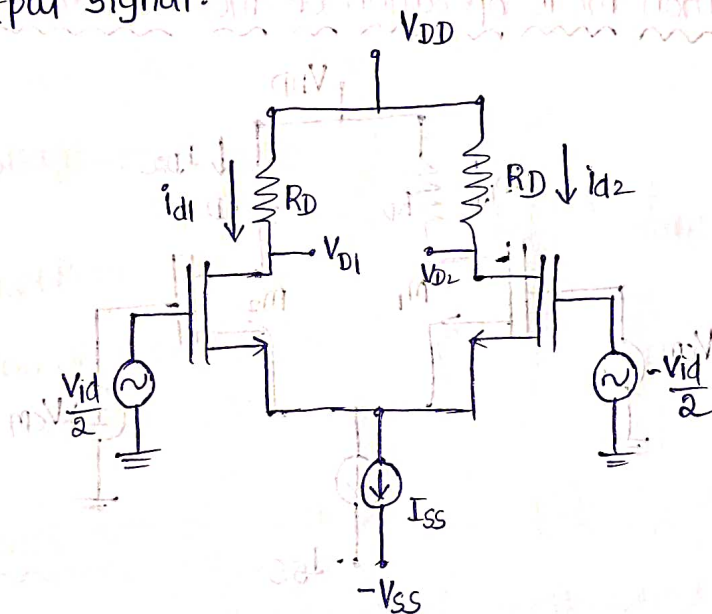
iii If common mode signal is absent then,

$$V_{G1} = \frac{V_{id}}{2}$$

$$V_{G2} = -\frac{V_{id}}{2}$$



output signal:-



Individual outputs } :-

By KVL along each device:-

Device 1:-

$$-V_{DD} + R_D I_{D1} + V_{D1} = 0$$

$$V_{D1} = V_{DD} - R_D I_{D1}$$

$$0 = -V_{DD} + R_D I_{D2} + V_{D2} = 0$$

$$V_{D2} = V_{DD} - R_D I_{D2}$$

Individual outputs :

$$V_{D1} = V_{DD} - I_{D1} R_D$$

$$V_{D2} = V_{DD} - I_{D2} R_D$$

In differential amplifiers we are interested in differential output

$$V_{od} = V_{D1} - V_{D2}$$

Differential current output $I_{od} = I_{D1} - I_{D2}$

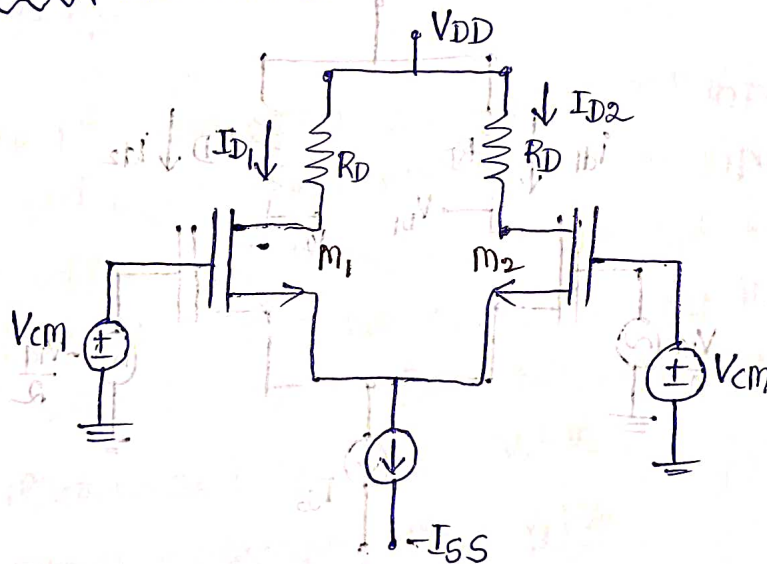
$$\Rightarrow V_{od} = V_{D1} - V_{D2} \\ = (V_{DD} - I_{D1} R_D) - (V_{DD} - I_{D2} R_D)$$

$$V_{od} = -I_{D1} R_D + I_{D2} R_D$$

$\Rightarrow V_{od}$ is a non zero quantity.

$$\text{voltage gain, } A_{vd} = \frac{V_{od}}{V_{id}} = \frac{V_{D1} - V_{D2}}{V_{id}}$$

common mode operation of mos differential amplifier:



[since inputs on both sides are same.]

$$I_{D1} = I_{D2} = \frac{I_{SS}}{2}$$

consider the case when two gate terminals are joined together and connected to a common mode (V_{cm}).

$$\Rightarrow V_{G1} = V_{G2} = V_{cm}$$

Differential input voltage $V_{id} = V_{G1} - V_{G2} = 0$

current I_{SS} will divide equally divided b/w two transistors.

$$\Rightarrow I_{D1} = I_{D2} = \frac{I_{SS}}{2}$$

output voltages of individual devices :

$$V_{D1} = V_{DD} - R_D I_{D1} = V_{DD} - R_D \frac{I_{SS}}{2}$$

$$V_{D2} = V_{DD} - R_D I_{D2} = V_{DD} - R_D \frac{I_{SS}}{2}$$

$$\Rightarrow V_{D1} = V_{D2}$$

output voltage in common mode :

$$V_{ocm} = V_{D1} - V_{D2}$$

$$= \left(V_{DD} - R_D \frac{I_{SS}}{2} \right) - \left(V_{DD} - R_D \frac{I_{SS}}{2} \right)$$

$$= V_{DD} - R_D \frac{I_{SS}}{2} - V_{DD} + R_D \frac{I_{SS}}{2}$$

$$V_{ocm} = 0V$$

$$\text{voltage gain } A_{cm} = \frac{V_{ocm}}{V_{icm}} = 0$$

$\Rightarrow$ Amplifier does not respond to common signal

common mode rejection ratio

$$CMRR = \frac{A_d}{A_{cm}} = \infty$$

minimum common-mode output voltage :-

We need to find minimum common-mode output voltage for safe operation of differential amplifier.

In common mode, output voltages are given by

$$V_{D1} = V_{D2} = V_{DD} - \frac{I_{SS}}{2} R_D$$

In order to maintain M_1 and M_2 in saturation, the common mode output cannot fall below a certain level.

For saturation mode :

$$V_{DS} \geq V_{GS} - V_{TH}$$

$$V_D - V_S \geq V_G - V_S - V_{TH}$$

$$V_D \geq V_G - V_{TH}$$

$$\Rightarrow V_{DD} - R_D \frac{I_{SS}}{2} \geq V_{cm} - V_{TH}$$

$$(\because V_D = V_{DD} - R_D \frac{I_{SS}}{2} \quad V_{G1} = V_{cm})$$

Here V_{DD} is fixed power supply

I_{SS} is the constant current source } fixed

V_{cm} is the common mode i/p and } parameters

V_{TH} is threshold voltage

so, we need to choose R_D such that mos device remains in saturation mode

$$\Rightarrow V_{DD} - V_{cm} + V_{TH} \geq R_D \frac{I_{SS}}{2}$$

$$\Rightarrow \frac{2(V_{DD} - V_{cm} + V_{TH})}{I_{SS}} \geq R_D$$

$$\Rightarrow R_D \leq \frac{2(V_{DD} - V_{cm} + V_{TH})}{I_{SS}}$$

$$(R_D)_{\max} = \frac{2(V_{DD} - V_{cm} + V_{TH})}{I_{SS}}$$

If R_D increases the voltage across R_D ($R_D \frac{I_{SS}}{2}$) also increases as a result V_D decreases.

$\Rightarrow$ MOSFET may enter into linear region

Q13: A mos differential amplifier is driven with an

common level of 1.6V. If $I_{SS} = 0.5 \text{ mA}$, $V_{TH} = 0.5 \text{ V}$ and

$V_{DD} = 1.8 \text{ V}$. What is the allowable load resistance R_D ?

Soln

$$(R_D) \leq \frac{2(V_{DD} - V_{cm} + V_{TH})}{I_{SS}} \quad V_{DD} = 1.8 \text{ V}$$

$$\leq \frac{2(1.8 - 1.6 + 0.5)}{0.5 \text{ mA}} \quad V_{cm} = 1.6 \text{ V}$$

$$R_D \leq 2.8 \text{ k}\Omega \quad I_{SS} = 0.5 \text{ mA}$$

$$V_{TH} = 0.5 \text{ V}$$

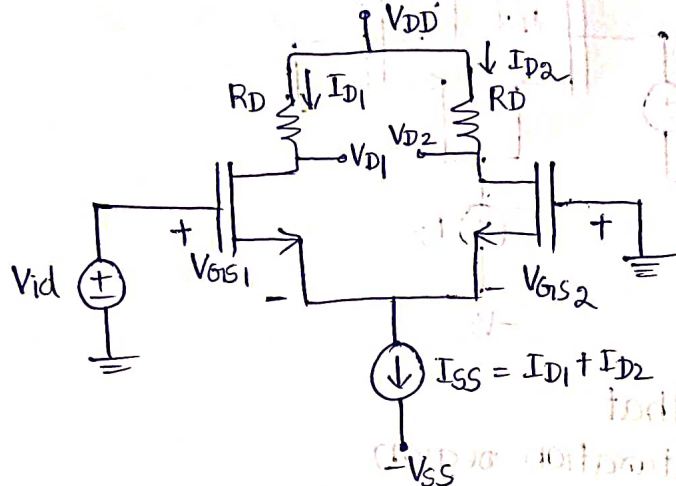
Differential mode operation

If differential input V_{id} is applied to differential amplifier

i.e., $V_{id} \neq 0$

$$\text{Let } V_{id} = V_{GS1} - V_{GS2} > 0$$

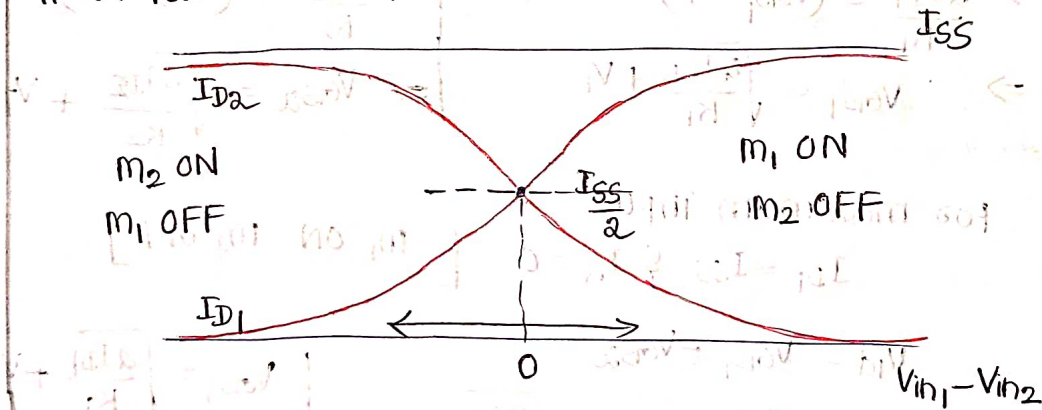
$$\Rightarrow V_{GS1} > V_{GS2}$$



V_{id} applied to g_1 and g_2 is grounded

$$\Rightarrow I_{D1} > I_{D2}$$

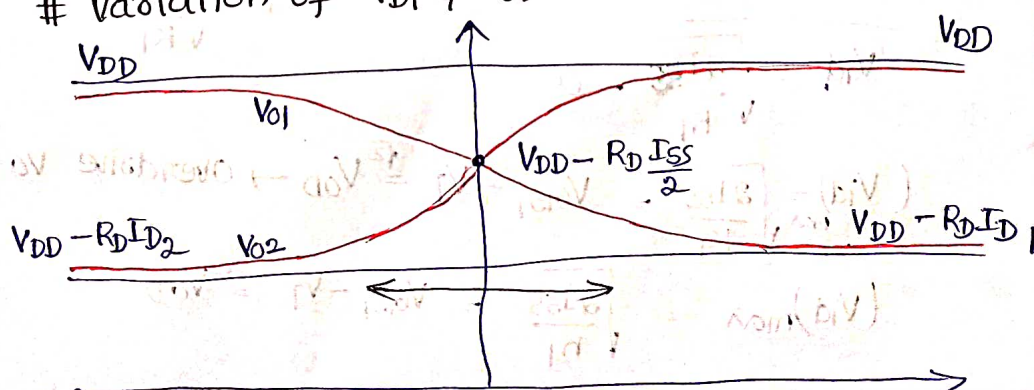
variations of I_{D1} & I_{D2} w.r.t $V_{in1} - V_{in2}$



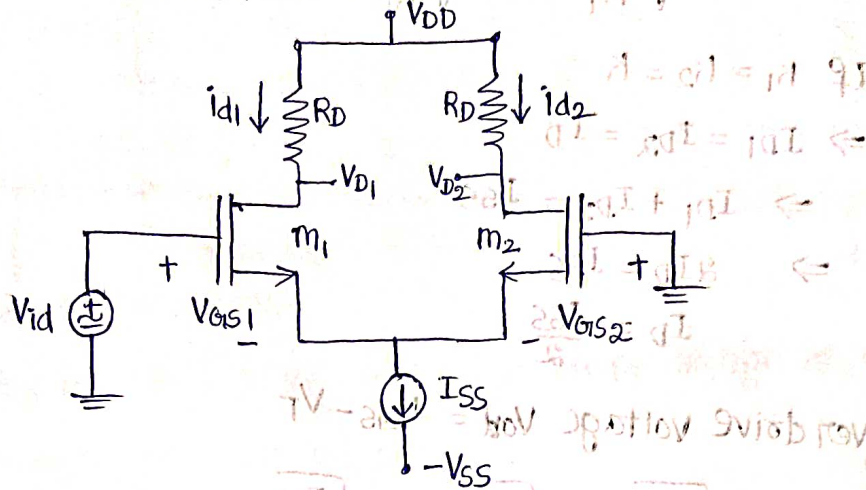
The sum of currents I_{D1} & I_{D2} at any point is I_{SS}

$$\Rightarrow I_{D1} + I_{D2} = I_{SS}$$

variation of V_{D1} & V_{D2} w.r.t $V_{in1} - V_{in2}$



chapter 4

MOS - Differential Amplifier (conti)# High Differential input : $V_{id} = \frac{V_{D1} - V_{D2}}{1} = bV$ 

For amplification purpose, MOSFET must be in saturation mode.

Therefore the current flowing through MOSFET in saturation region is given by

$$I_{D1} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS1} - V_T)^2 = \frac{K_1}{2} (V_{GS1} - V_T)^2$$

$$\Rightarrow \frac{2I_{D1}}{K_1} = (V_{GS1} - V_T)^2$$

$$\Rightarrow V_{GS1} = \sqrt{\frac{2I_{D1}}{K_1}} + V_T \rightarrow \textcircled{1}$$

$$I_{D2} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS2} - V_T)^2 = \frac{K_2}{2} (V_{GS2} - V_T)^2$$

$$\Rightarrow \frac{2I_{D2}}{K_2} = (V_{GS2} - V_T)^2$$

$$\Rightarrow V_{GS2} = \sqrt{\frac{2I_{D2}}{K_2}} + V_T \rightarrow \textcircled{2}$$

For maximum condition

$$I_{D1} = I_{SS} \text{ and } I_{D2} = 0$$

$\Rightarrow m_1$ is ON and m_2 is OFF

Differential input

$$V_{id} = V_{GS1} - V_{GS2}$$

$$V_{id} = \left(\sqrt{\frac{2I_{D1}}{K_1}} + V_T \right) - \left(\sqrt{\frac{2I_{D2}}{K_2}} + V_T \right)$$

$$V_{id} = \sqrt{\frac{2I_{D1}}{K_1}} - \sqrt{\frac{2I_{D2}}{K_2}}$$

since $I_{D2} = 0$

$$\Rightarrow V_{id} = \sqrt{\frac{2I_{D1}}{K_1}} = \sqrt{2} \sqrt{\frac{I_{D1}}{K_1}}$$

If $K_1 = K_2 = K$

$$\Rightarrow I_{D1} = I_{D2} = I_D$$

$$\Rightarrow I_{D1} + I_{D2} = I_{SS}$$

$$\Rightarrow 2I_D = I_{SS}$$

$$I_D = \frac{I_{SS}}{2}$$

over drive voltage $V_{OD} = V_{GS} - V_T$

$$V_{GS} - V_T = \sqrt{\frac{2I_D}{K}} = \sqrt{\frac{2(\frac{I_{SS}}{2})}{K}} = \sqrt{\frac{I_{SS}}{K}}$$

$$\Rightarrow V_{id} = \sqrt{2} \sqrt{\frac{I_{D1}}{K_1}} = \sqrt{2} \sqrt{\frac{I_{SS}}{K}} = \sqrt{2} V_{OD}$$

$$\Rightarrow V_{id} = \sqrt{2} V_{OD}$$

$$V_{OD} = \sqrt{\frac{I_{SS}}{K}}$$

If $V_{id} = V_{G1} - V_{G2} < 0$

$$\text{Then } V_{id} = \sqrt{\frac{2I_{D1}}{K_1}} - \sqrt{\frac{2I_{D2}}{K_2}}$$

since $I_{D1} = 0$

$$\Rightarrow V_{id} = -\sqrt{\frac{2I_{D2}}{K_2}}$$

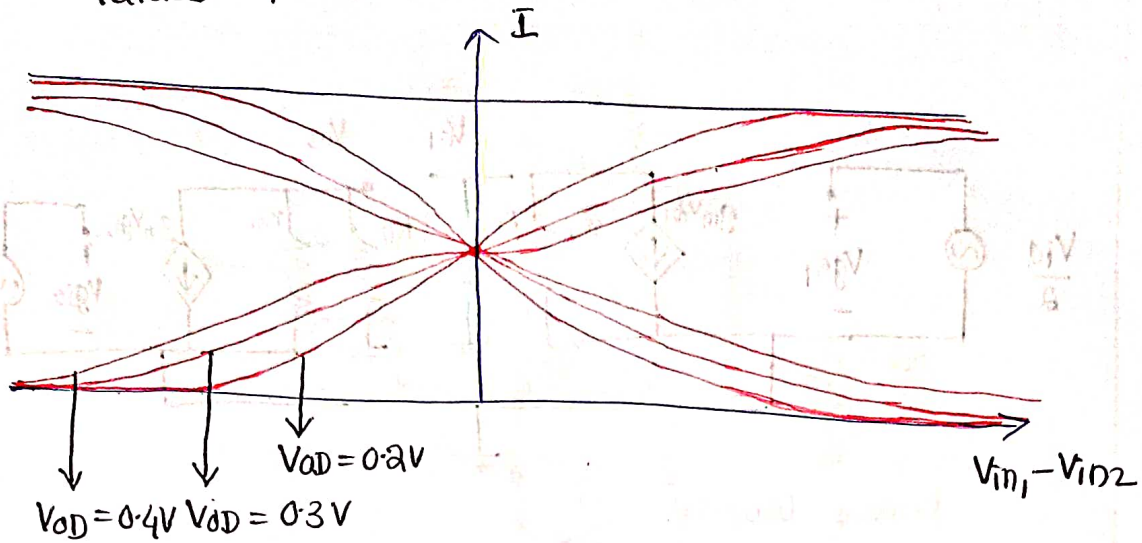
$$V_{id} = -\sqrt{2} V_{OD}$$

$$\Rightarrow -\sqrt{2} V_{OD} < V_{id} < \sqrt{2} V_{OD}$$

To steer the current completely to one side of the pair, a difference input voltage V_{id} of at least

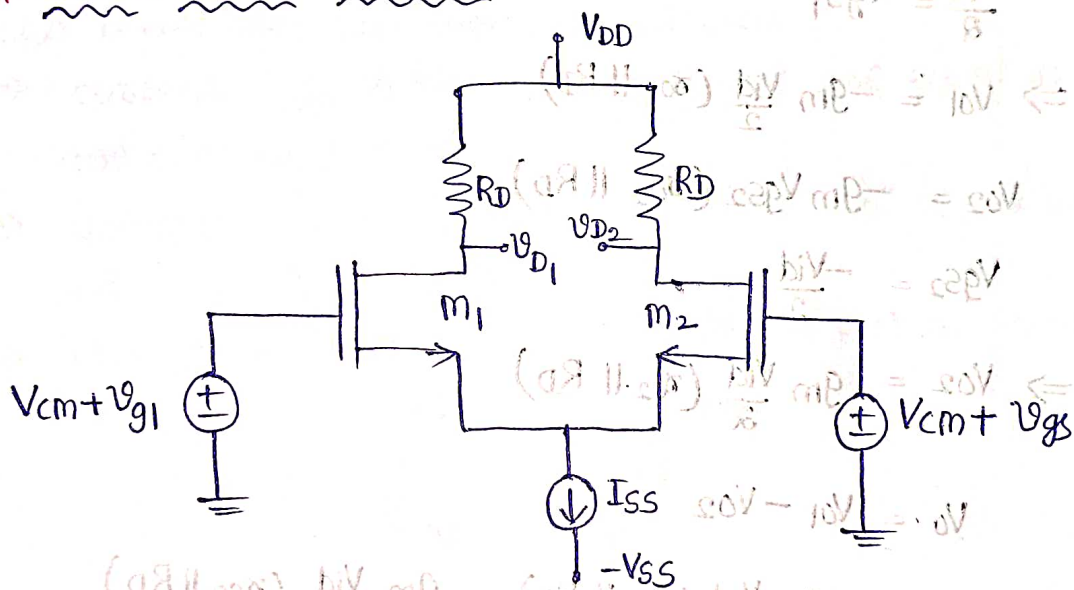
$$\sqrt{2} V_{OD} \text{ or } \sqrt{\frac{2I_{SS}}{K}} \text{ is needed.}$$

Differential amplifier characteristics for different values of V_{OD}



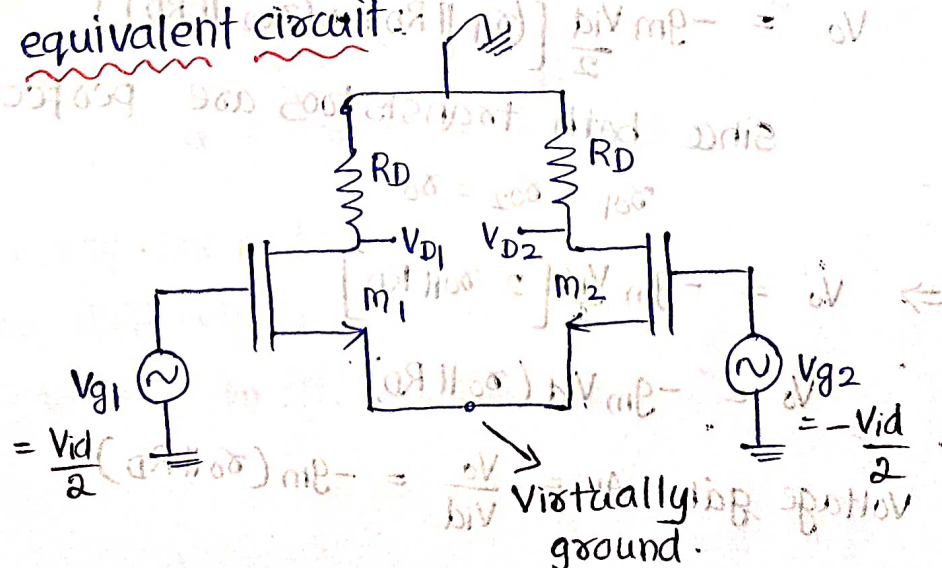
By increasing V_{OD} we can increase range of $V_{in1} - V_{in2}$.

small signal Analysis:-

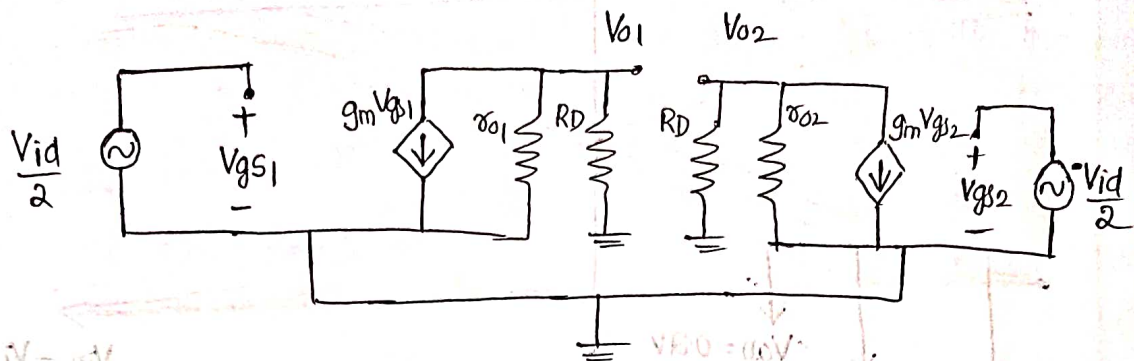


Differential Amplifier

ac equivalent circuit:-



small signal modelling



$$V_{01} = -g_m V_{gs1} (r_{o1} \parallel R_D)$$

$$\frac{V_{id}}{2} = V_{gs1}$$

$$\Rightarrow V_{01} = -g_m \frac{V_{id}}{2} (r_{o1} \parallel R_D)$$

$$V_{02} = -g_m V_{gs2} (r_{o2} \parallel R_D)$$

$$V_{gs2} = -\frac{V_{id}}{2}$$

$$\Rightarrow V_{02} = g_m \frac{V_{id}}{2} (r_{o2} \parallel R_D)$$

$$V_o = V_{01} - V_{02}$$

$$= -g_m \frac{V_{id}}{2} (r_{o1} \parallel R_D) - g_m \frac{V_{id}}{2} (r_{o2} \parallel R_D)$$

$$V_o = -g_m \frac{V_{id}}{2} [(r_{o1} \parallel R_D) + (r_{o2} \parallel R_D)]$$

Since both transistors are perfectly matched

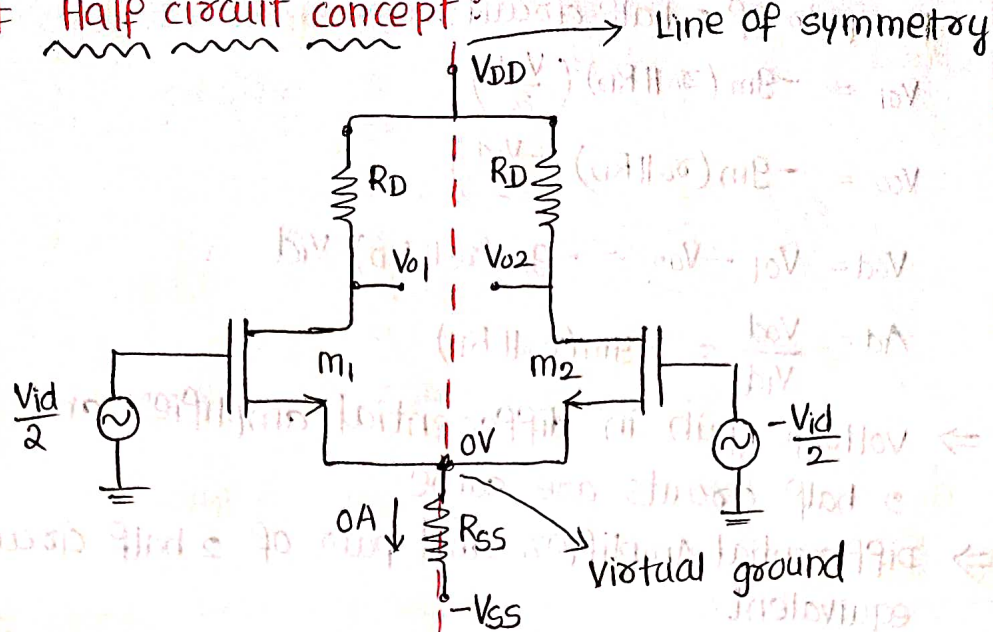
$$r_{o1} = r_{o2} = r_o$$

$$\Rightarrow V_o = -g_m \frac{V_{id}}{2} [2 r_o \parallel R_D]$$

$$V_o = -g_m V_{id} (r_o \parallel R_D)$$

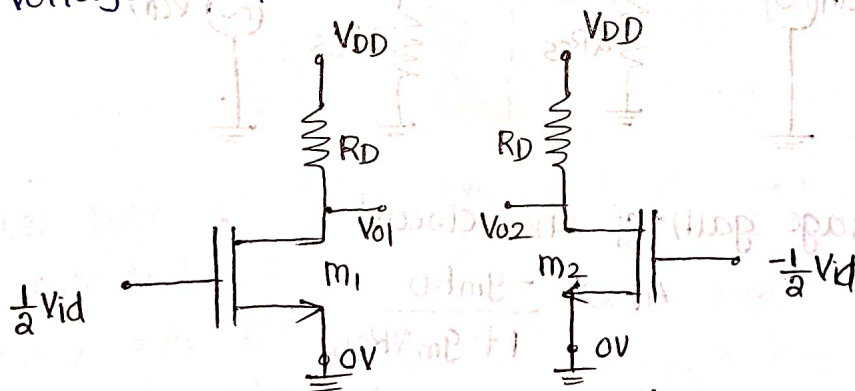
$$\text{voltage gain } A_v = \frac{V_o}{V_{id}} = -g_m (r_o \parallel R_D)$$

Half circuit concept



Because of the symmetry, the differential mode circuit also break into two identical half circuits.

- >> currents about the symmetry line are equal in value and opposite in sign.
- >> voltages about the symmetry line are equal in value and opposite in sign.
- >> voltage at symmetry line is zero (virtual ground)



a symmetrical circuits :

we already knew that
for differential amplifier

$$V_{o1} = -g_m \frac{V_{id}}{2} (\tau_o \parallel R_D)$$

$$V_{o2} = g_m \frac{V_{id}}{2} (\tau_o \parallel R_D) \text{ and hence}$$

$$V_{od} = V_{o1} - V_{o2} = -g_m (\tau_o \parallel R_D) V_{id}$$

$$A_d = \frac{V_{od}}{V_{id}} = -g_m (\tau_o \parallel R_D)$$

For pair of 2 half circuits :

$$V_{o1} = -g_m (\tau_{o1} \parallel R_D) \left(\frac{V_{id}}{2} \right)$$

$$V_{o2} = -g_m (\tau_{o1} \parallel R_D) \left(\frac{-V_{id}}{2} \right)$$

$$V_{od} = V_{o1} - V_{o2} = -g_m (\tau_{o1} \parallel R_D) V_{id}$$

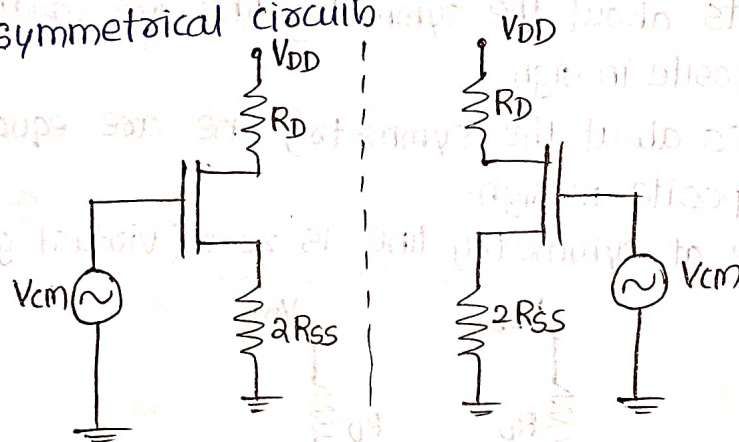
$$A_d = \frac{V_{od}}{V_{id}} = -g_m (\tau_{o1} \parallel R_D)$$

⇒ voltage gain in differential amplifier and pair of 2 half circuits are same.

⇒ Differential Amplifier and pair of 2 half circuits are equivalent.

common mode rejection ratio (CMRR) :-

The common mode circuit can also be splitted into 2 symmetrical circuits



voltage gain of one circuit :

$$A_v = \frac{-g_m R_D}{1 + g_m 2R_{SS}}$$

$$A_v = \frac{-R_D}{\frac{1}{g_m} + 2R_{SS}}$$

$$2R_{SS} \gg \frac{1}{g_m}$$

$$\therefore A_v = \frac{-R_D}{2R_{SS}}$$

voltage gain of differential mode for one circuit

$$A_v = \frac{-g_m R_D}{2}$$

common mode rejection ratio

$$CMRR = \frac{A_d}{A_{cm}}$$

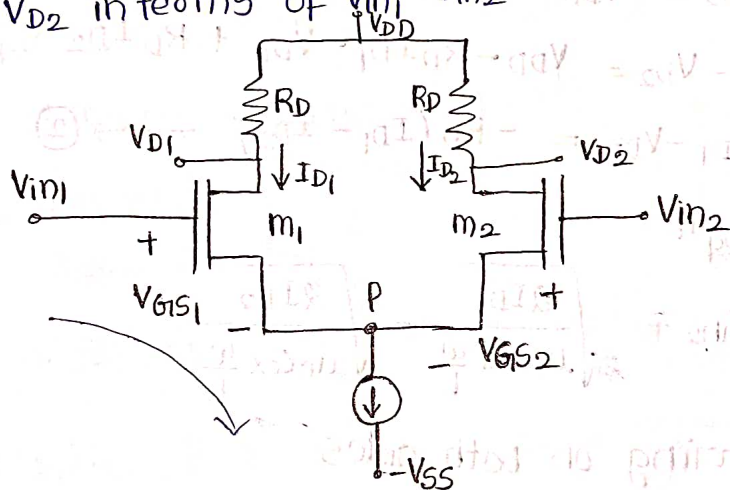
$$= \frac{-\frac{g_m R_D}{2}}{\frac{-R_D}{2R_{SS}}}$$

$$= \frac{-\frac{g_m R_D}{2}}{\frac{-R_D}{2R_{SS}}} \times \frac{2R_{SS}}{-R_D}$$

$$CMRR = +g_m R_{SS}$$

Large signal analysis of MOS differential amplifier:

In large signal analysis we need to find an eqⁿ for $V_{D1} - V_{D2}$ in terms of $V_{in1} - V_{in2}$.



Let both transistors are ON:

potential at P:

From left side:

$$-V_{in1} + V_{GS1} + V_P = 0$$

$$V_P = V_{in1} - V_{GS1}$$

From right side:

$$-V_{in2} + V_{GS2} + V_P = 0$$

$$V_P = V_{in2} - V_{GS2}$$

$$V_P = V_{in1} - V_{GS1} = V_{in2} - V_{GS2}$$

$$V_{in1} - V_{in2} = V_{GS1} - V_{GS2}$$

$$I_{D1} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS1} - V_{Th})^2$$

$$I_{D2} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS2} - V_{Th})^2$$

$$V_{GS1} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} \frac{W}{L}}} + V_{Th} \quad V_{GS2} = \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} \frac{W}{L}}} + V_{Th}$$

$$V_{in1} - V_{in2} = V_{GS1} - V_{GS2}$$

$$= \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} \frac{W}{L}}} + V_{Th} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} \frac{W}{L}}} - V_{Th}$$

$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} \frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} \frac{W}{L}}} \longrightarrow \textcircled{1}$$

And

$$V_{D1} = V_{DD} - R_D I_{D1}$$

$$V_{D2} = V_{DD} - R_D I_{D2}$$

$$V_{D1} - V_{D2} = V_{DD} - R_D I_{D1} - V_{DD} + R_D I_{D2}$$

$$V_{D1} - V_{D2} = -R_D (I_{D1} - I_{D2}) \longrightarrow \textcircled{2}$$

From eqⁿ

$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} \frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} \frac{W}{L}}}$$

squaring on both sides

$$(V_{in1} - V_{in2})^2 = \left[\sqrt{\frac{2I_{D1}}{\mu_n C_{ox} \frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} \frac{W}{L}}} \right]^2$$

$$(V_{in1} - V_{in2})^2 = \frac{2I_{D1}}{\mu_n C_{ox} \frac{W}{L}} + \frac{2I_{D2}}{\mu_n C_{ox} \frac{W}{L}} - 2 \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} \frac{W}{L}}} \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} \frac{W}{L}}}$$

$$(V_{in1} - V_{in2})^2 = \frac{2}{\mu_n C_{ox} \frac{W}{L}} (I_{D1} + I_{D2}) - \frac{2(2)}{\mu_n C_{ox} \frac{W}{L}} \sqrt{I_{D1} I_{D2}} \longrightarrow \textcircled{3}$$

we have

$$\begin{cases} I_{D1} + I_{D2} = I_{SS} \\ I_{D2} = I_{SS} - I_{D1} \end{cases} \text{ (from ckt)} \longrightarrow \textcircled{4}$$

$$I_{D1} = I_{SS} - I_{D2} \longrightarrow \textcircled{5}$$

From eqⁿ 3.

$$(V_{in1} - V_{in2})^2 = \frac{2}{\mu_n C_{ox} \frac{W}{L}} (I_{D1} + I_{D2}) - \frac{2}{\mu_n C_{ox} \frac{W}{L}} 2\sqrt{I_{D1} I_{D2}}$$

$$4(V_{in1} - V_{in2})^2 = \frac{2}{\mu_n C_{ox} \frac{W}{L}} (I_{SS} - 2\sqrt{I_{D1} I_{D2}})$$

$$\mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 = 2I_{SS} - 4\sqrt{I_{D1} I_{D2}}$$

$$4\sqrt{I_{D1} I_{D2}} = 2I_{SS} - \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2$$

squaring on both sides

$$16 I_{D1} I_{D2} = \left[2I_{SS} - \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 \right]^2$$

Now substitute

$$I_{D2} = I_{SS} - I_{D1}$$

$$\Rightarrow 16 (I_{D1}) (I_{SS} - I_{D1}) = \left[2I_{SS} - \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 \right]^2$$

$$\Rightarrow 16 I_{D1} I_{SS} - 16 I_{D1}^2 + \left[2I_{SS} - \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 \right]^2 = 0$$

$$\Rightarrow 16 I_{D1}^2 - 16 I_{D1} I_{SS} + \left[2I_{SS} - \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 \right]^2 = 0$$

$$I_{D1} = \frac{16 I_{SS} \pm \sqrt{16 I_{SS}^2 - 4 \left[2I_{SS} - \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 \right]^2}}{2(16)}$$

$$I_{D1} = \frac{I_{SS}}{2} \pm \frac{\sqrt{16}}{2 \times 16} \sqrt{16 I_{SS}^2 - 4 \left(\mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 - 2I_{SS} \right)^2}$$

$$I_{D1} = \frac{I_{SS}}{2} \pm \frac{1}{8} \sqrt{4 I_{SS}^2 - \left(\mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 - 2I_{SS} \right)^2}$$

$$I_{D1} = \frac{I_{SS}}{2} \pm \frac{1}{4} \sqrt{4 I_{SS}^2 - \left[\mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 - 2I_{SS} \right]^2}$$

I_{D1} comes out +ve when we consider +ve in b/w.

$$\Rightarrow I_{D1} = \frac{I_{SS}}{2} + \frac{1}{4} \sqrt{4I_{SS}^2 - \left[\mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 \right]^2 - 4I_{SS}^2 + 2(2I_{SS}) \left(\mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 \right)}$$

$$= \frac{I_{SS}}{2} + \frac{1}{4} \sqrt{4I_{SS} \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 - \left[\mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 \right]^2}$$

$$I_{D1} = \frac{I_{SS}}{2} + \frac{V_{in1} - V_{in2}}{4} \sqrt{\mu_n C_{ox} \frac{W}{L} \left(4I_{SS} - \left(\mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 \right) \right)}$$

$$= \frac{I_{SS}}{2} + \frac{1}{4} \sqrt{\mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 \left[4I_{SS} - \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 \right]}$$

$$I_{D1} = \frac{I_{SS}}{2} + \frac{V_{in1} - V_{in2}}{4} \sqrt{\mu_n C_{ox} \frac{W}{L} \left(4I_{SS} - \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 \right)}$$

similarly

$$I_{D2} = \frac{I_{SS}}{2} + \frac{V_{in2} - V_{in1}}{4} \sqrt{\mu_n C_{ox} \frac{W}{L} \left(4I_{SS} - \mu_n C_{ox} \frac{W}{L} (V_{in2} - V_{in1})^2 \right)}$$

$$\Rightarrow I_{D1} - I_{D2}$$

$$= \frac{1}{4} \left[\frac{V_{in1} - V_{in2}}{4} \sqrt{\mu_n C_{ox} \frac{W}{L} \left(4I_{SS} - \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 \right)} \right.$$

$$\left. - \frac{V_{in2} - V_{in1}}{4} \sqrt{\mu_n C_{ox} \frac{W}{L} \left(4I_{SS} - \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2})^2 \right)} \right]$$

$$= \frac{V_{in1} - V_{in2}}{4} \left[\sqrt{\left(\mu_n C_{ox} \frac{W}{L} \right)^2 \left(\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - (V_{in1} - V_{in2})^2 \right)} + \right.$$

$$\left. \sqrt{\left(\mu_n C_{ox} \frac{W}{L} \right)^2 \left(\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - (V_{in1} - V_{in2})^2 \right)} \right]$$

$$I_{D1} - I_{D2}$$

$$= \mu_n C_{ox} \frac{W}{L} \left(\frac{V_{in1} - V_{in2}}{2} \right)$$

$$\left[\sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - (V_{in1} - V_{in2})^2} + \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - (V_{in1} - V_{in2})^2} \right]$$

$$I_{D1} - I_{D2} = \mu_n C_{ox} \frac{W}{L} \left(\frac{V_{in1} - V_{in2}}{2} \right) \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - (V_{in1} - V_{in2})^2}$$

$$I_{D1} - I_{D2} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2}) \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - (V_{in1} - V_{in2})^2} \rightarrow (6)$$

$$I_{D1} - I_{D2} = 0 \text{ when } V_{in1} - V_{in2} = 0$$

$$\Rightarrow \left. \begin{array}{l} V_{in1} = V_{in2} \\ V_{o1} - V_{o2} = 0 \end{array} \right\} \text{ common mode}$$

If only one transistor is ON

$$\text{when } V_{in1} - V_{in2} = \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}}}$$

In above expression (eqⁿ 6)

$$\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}} \ggggg (V_{in1} - V_{in2})^2$$

$$\Rightarrow I_{D1} - I_{D2} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2}) \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}}}$$

$$V_{o1} - V_{o2} = -R_D \left[\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{in2}) \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} \right]$$

$$V_{o1} - V_{o2} = -R_D (V_{in1} - V_{in2}) \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} \times \frac{1}{4} \left(\mu_n C_{ox} \frac{W}{L} \right)^2$$

$$V_{O1} - V_{O2} = -R_D (V_{in1} - V_{in2}) \sqrt{4I_{SS} \left(\mu_n C_{ox} \frac{W}{L} \right)} \Rightarrow y = mx$$

Large signal voltage gain of differential amplifier:

$$A_v = \frac{V_{o1} - V_{o2}}{V_{in1} - V_{in2}} = -R_D \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}}$$

$$\text{slope} = -R_D \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}}$$

If we increase R_D then there is a chance to both transistors are enter into ohmic region

! Thank you !

