



WELCOME

"When you reach the end of your rope, tie a knot in it and hang on." -Franklin D. Roosevelt

ANALOG ELECTRONICS

CHAPTER 5

CURRENT MIRRORS

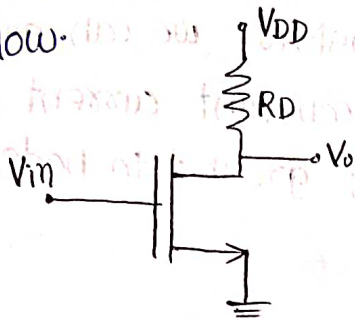
By
DHAMU (D²)

chapter 5

Current Mirrors

concept of Active Loads :-

consider a common source amplifier as shown below.



voltage gain of common source amplifier is

$$A_v = -g_m (\tau_o \parallel R_D)$$

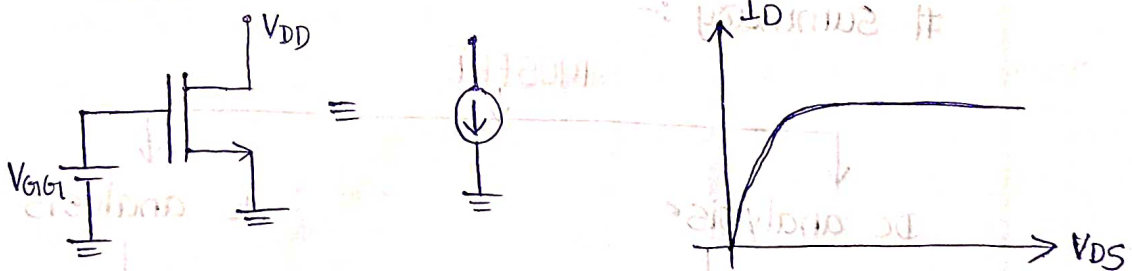
if $\lambda \neq 0$

In common source amplifier we have passive resistance R_D which occupies more space and hence we can't able to fabricate such an amplifier with passive load on integrated circuit chips.

Let us ^{try to} overcome problem of passive resistance.

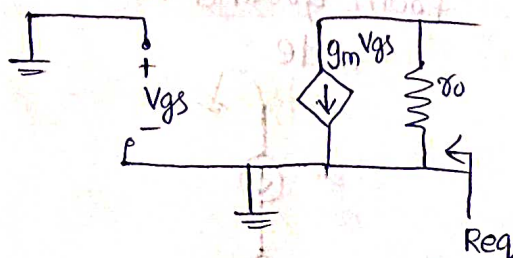
In saturation region,

MOSFET can act as constant current source.



In above NMOS transistor, we can say that N-mos device can acts as constant current source in dc analysis where current directed from node to ground.

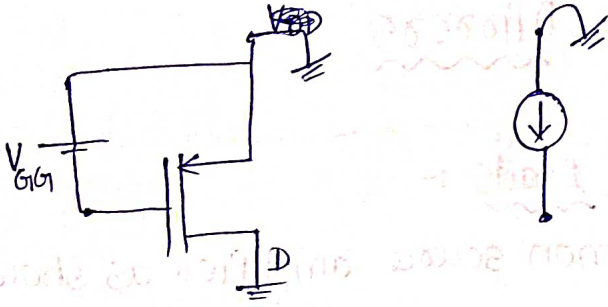
ac analysis:



$$R_{eq} = r_o$$

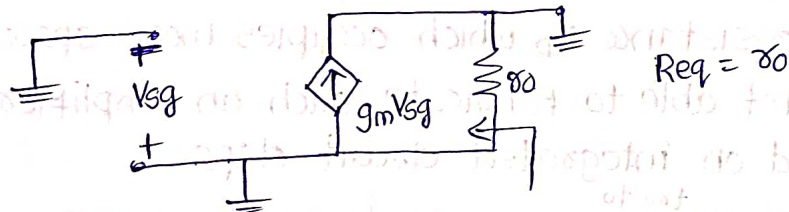
under ac analysis MOSFET can act as resistor of value r_o .

Pmos transistor :-



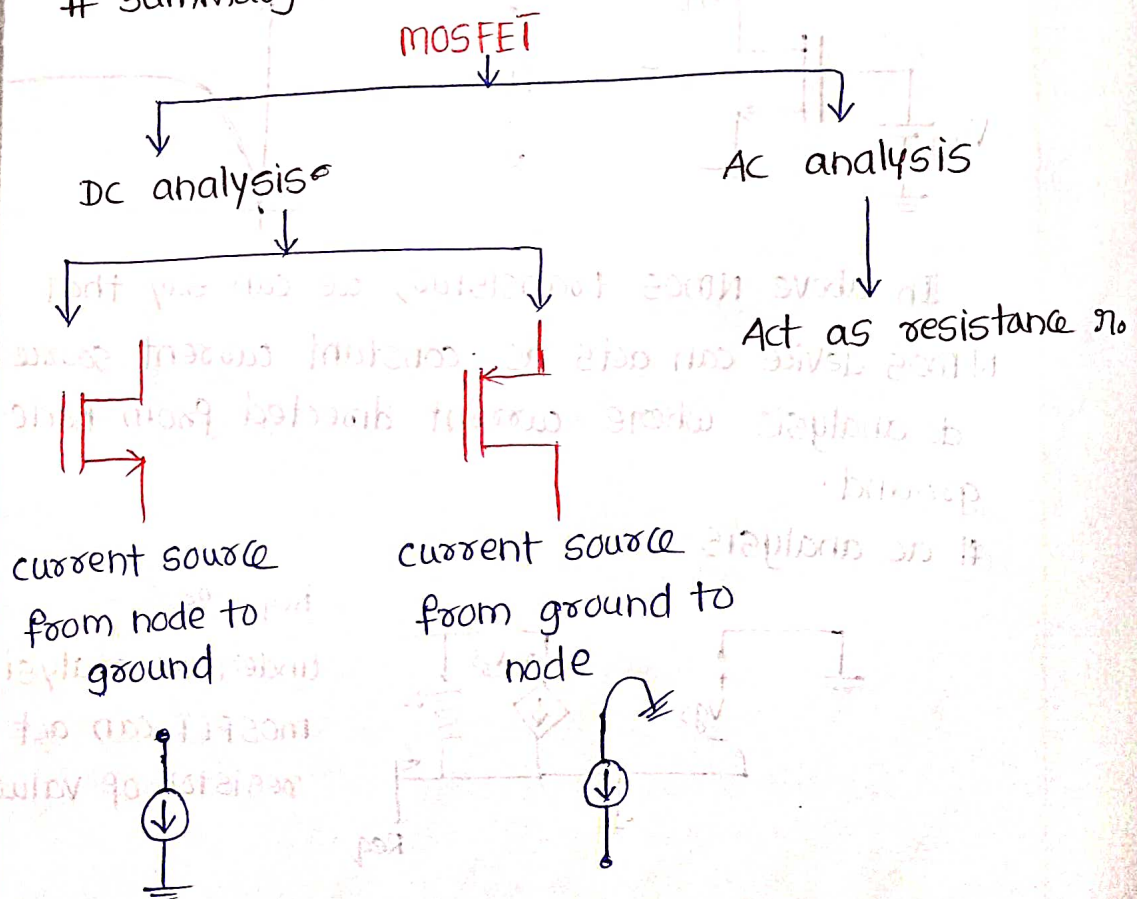
From above p-mos transistor we can say that pmos device can act as constant current source where current is directed from ground to node in dc analysis:

ac analysis:

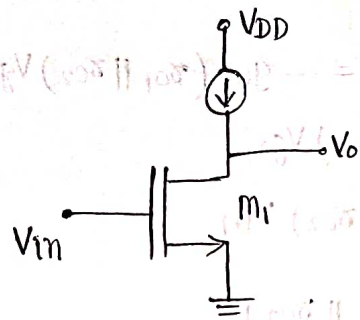


under ac analysis pmos is also act as a resistor of value r_o .

summary :-

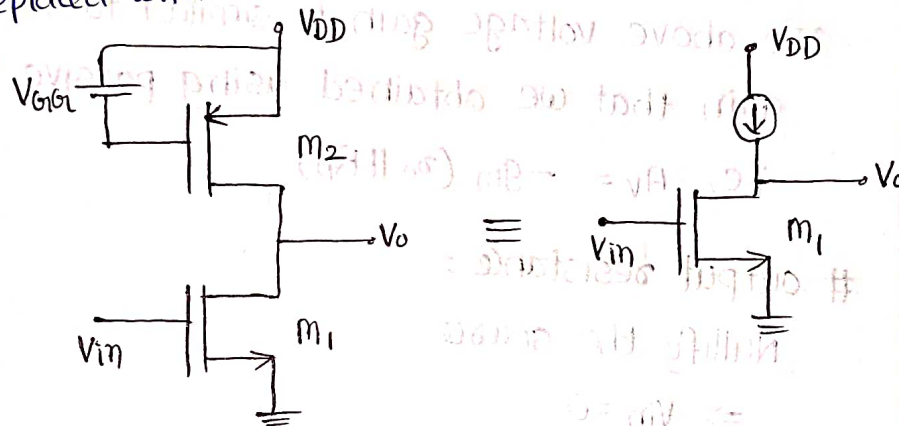


common source Amplifier with current source load.



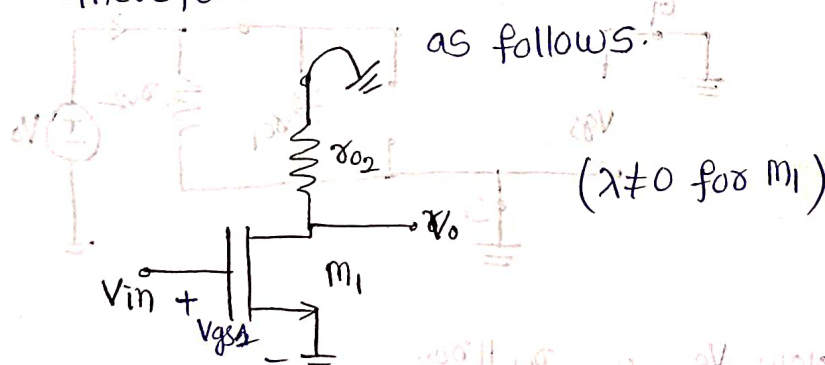
consider the common source amplifier with current source as shown in adjacent figure.

From the figure we can noticed that the current is entering into the node. so the current source can be replaced with pmos transistor.

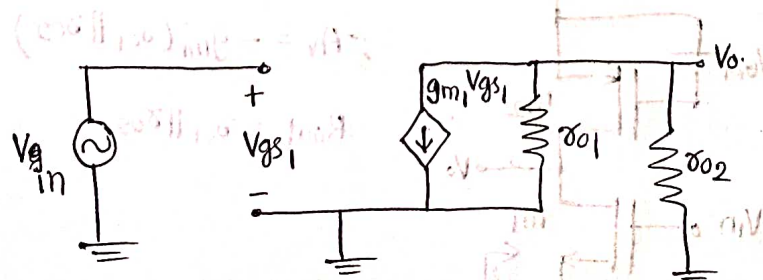


In ac analysis, the pmos transistor act as resistor of value r_o .

Therefore the ac equivalent circuit can be drawn as follows.



Now ac equivalent model:



From ac equivalent model,

we have

$$V_{in} = V_{gs1} \text{ and } V_o = -g_{m1}(\tau_{o1} \parallel \tau_{o2})V_{gs1}$$

$$\Rightarrow V_o = -g_{m1}(\tau_{o1} \parallel \tau_{o2})V_{gs1}$$

$$\Rightarrow V_o = -g_{m1}(\tau_{o1} \parallel \tau_{o2})V_{in}$$

$$\Rightarrow \frac{V_o}{V_{in}} = -g_{m1}(\tau_{o1} \parallel \tau_{o2})$$

$$\Rightarrow A_v = \frac{V_o}{V_{in}} = -g_{m1}(\tau_{o1} \parallel \tau_{o2})$$

The above voltage gain is similar to the voltage gain that we obtained using passive load

$$\text{i.e., } A_v = -g_m(\tau_o \parallel R_D)$$

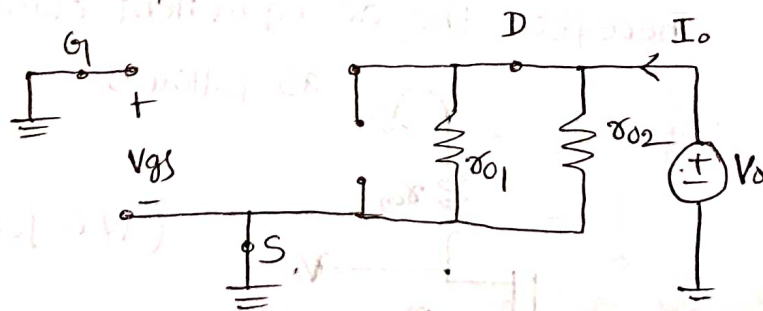
output resistance :

Nullify the source

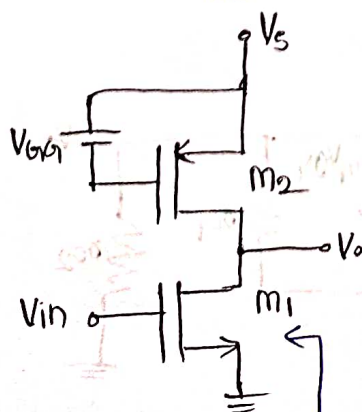
$$\Rightarrow V_{in} = 0$$

$$\text{If } V_{in} = 0 \text{ then } V_{gs1} = 0V$$

$$\Rightarrow g_{m1}V_{gs1} = 0 \text{ [open circuit]}$$



$$\text{Now } \frac{V_o}{I_o} = R_o = \tau_{o1} \parallel \tau_{o2}$$

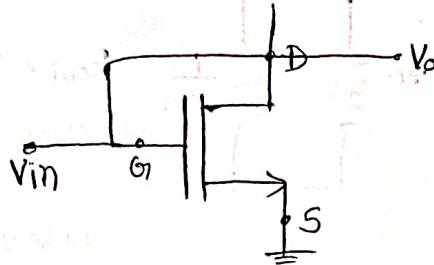


$$A_v = -g_{m1}(\tau_{o1} \parallel \tau_{o2})$$

$$R_{out} = \tau_{o1} \parallel \tau_{o2}$$

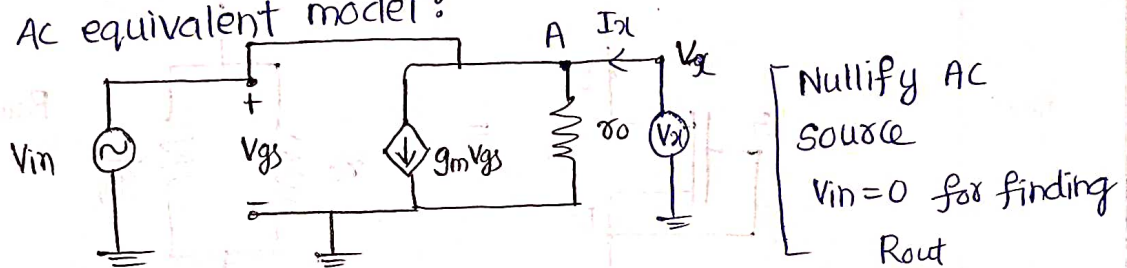
Diode connected mos Transistor :-

If Gate and drain are short circuited then the mos device is called diode connected mos device / mos transistor.



Let us analyse how diode connected mos device behaves under ac analysis.

AC equivalent model :-



Let us calculate output resistance.

By KVL at node A :

$$I_x = \frac{V_x}{r_o} + g_m V_{gs}$$

The voltage source V_x is same as V_{gs}

$$\Rightarrow V_{gs} = V_x$$

$$\Rightarrow I_x = \frac{V_x}{r_o} + g_m V_x$$

$$\Rightarrow V_x \left(\frac{1}{r_o} + g_m \right) = I_x$$

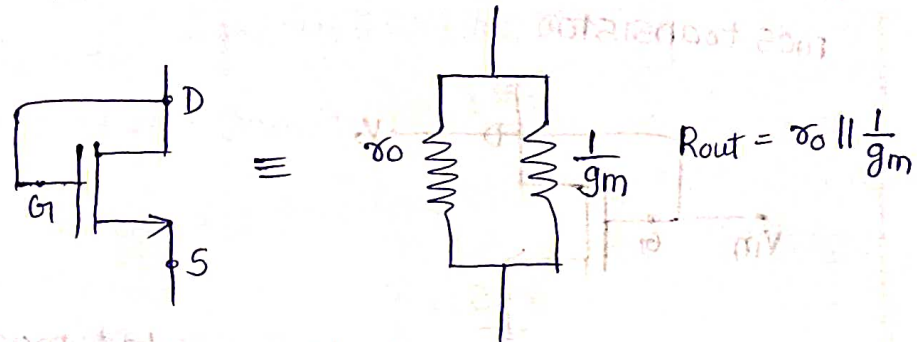
$$\Rightarrow \frac{V_x}{I_x} = \frac{1}{\frac{1}{r_o} + g_m}$$

$$\frac{V_x}{I_x} = \frac{r_o}{1 + g_m r_o}$$

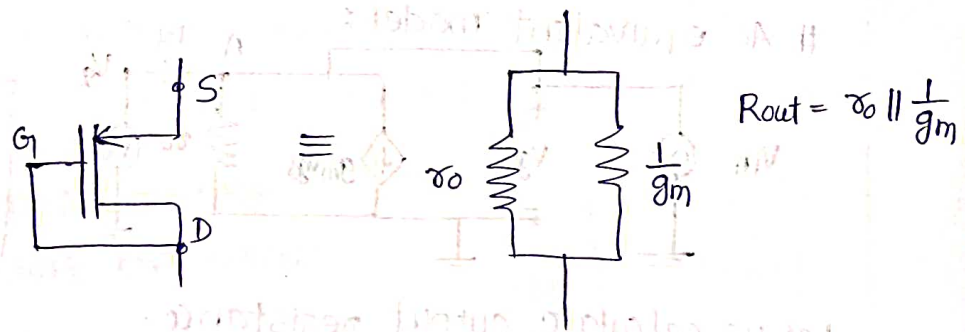
$$\frac{V_x}{I_x} = \frac{r_o \times \frac{1}{g_m}}{r_o + \frac{1}{g_m}}$$

$$R_{out} = \frac{V_x}{I_x} = r_o \parallel \frac{1}{g_m}$$

Therefore the diode connected mos device can act as resistance of values $R_{out} = \frac{1}{g_m} \parallel r_o$ in ac analysis.

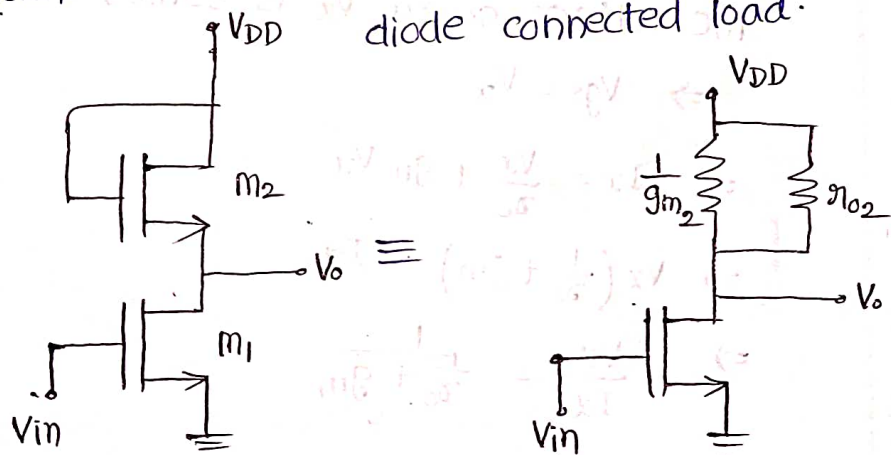


similarly pmos device also behaves as same.



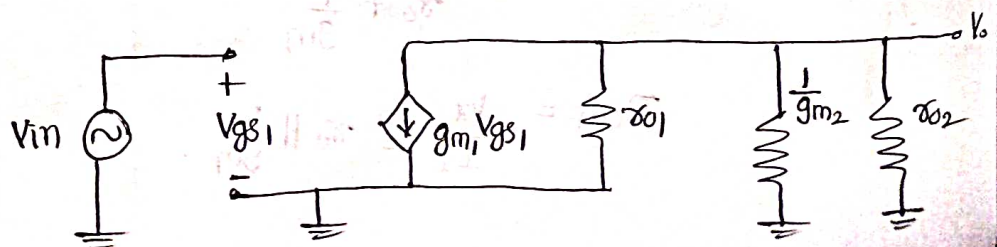
common source Amplifier with diode connected load:

consider NMOS common source amplifier with diode connected load.



Assume $\lambda \neq 0$ for both transistors.

ac equivalent model:



From the circuit shown,

$$V_{GS1} = V_{in}$$

$$V_{out} = -g_{m1} V_{GS1} (\tau_{o1} \parallel \tau_{o2} \parallel \frac{1}{g_{m2}})$$

$$\Rightarrow V_{out} = -g_{m1} V_{in} (\tau_{o1} \parallel \tau_{o2} \parallel \frac{1}{g_{m2}})$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = -g_{m1} (\tau_{o1} \parallel \tau_{o2} \parallel \frac{1}{g_{m2}})$$

$$\text{voltage gain } A_v = \frac{V_{out}}{V_{in}} = -g_{m1} (\tau_{o1} \parallel \tau_{o2} \parallel \frac{1}{g_{m2}})$$

when $\lambda_1 = \lambda_2 = 0$ then

voltage gain

$$A_v = \frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{g_{m2}}$$

$$g_m = \sqrt{2 I_D \mu_n C_{ox} \frac{W}{L}}$$

$$\Rightarrow A_v = - \frac{\sqrt{2 I_{D1} \mu_n C_{ox} \left(\frac{W}{L}\right)_1}}{\sqrt{2 I_{D2} \mu_n C_{ox} \left(\frac{W}{L}\right)_2}}$$

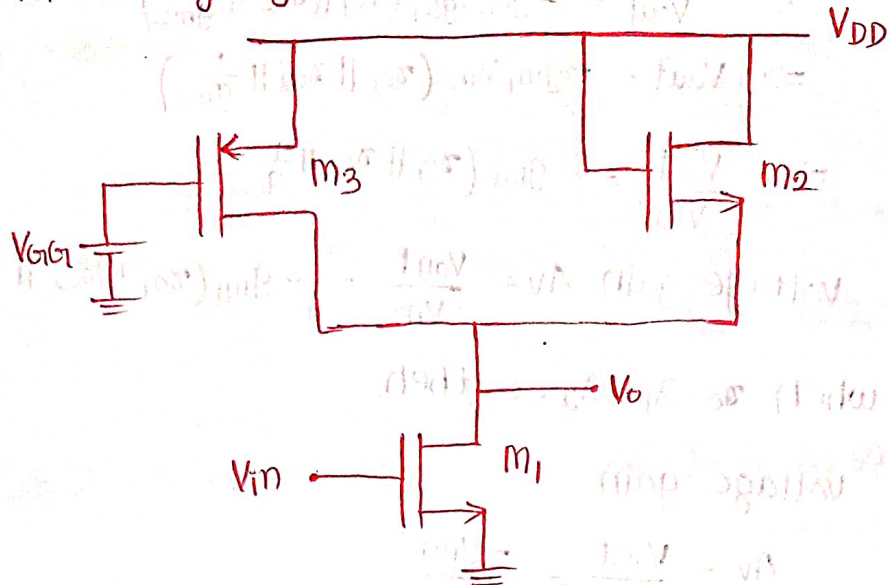
Since $I_{D1} = I_{D2}$

$$A_v = - \frac{\sqrt{\left(\frac{W}{L}\right)_1}}{\sqrt{\left(\frac{W}{L}\right)_2}}$$

For diode connected common source amplifier,
if $\lambda_1 = \lambda_2 = 0$ then voltage gain completely depends
upon $\frac{W}{L}$ ratios of both the transistors.

questions :-

- 1) Find the voltage gain of the circuit shown below.



soln

The above circuit has 3 MOSFETs.

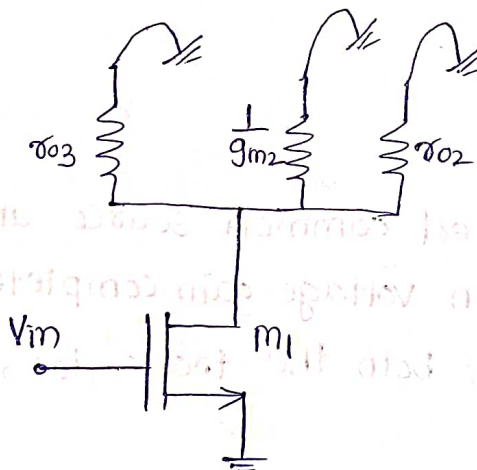
m_1 is reference MOSFET

m_2 is diode connected MOSFET

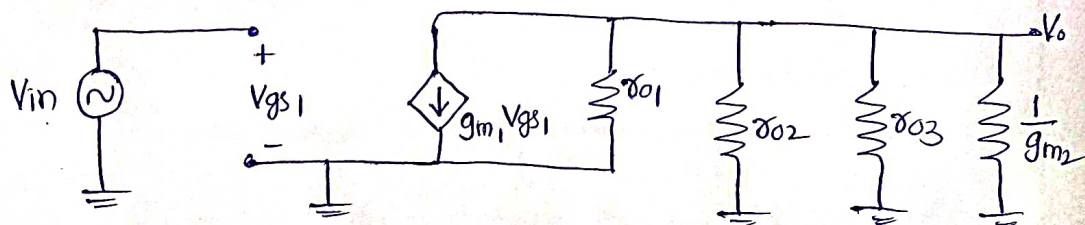
m_3 is current source connected MOSFET

$\Rightarrow m_2$ act as resistance $R_2 = \frac{1}{g_{m2}} \parallel r_{o2}$

$\Rightarrow m_3$ act as resistance $R_3 = r_{o3}$



ac analysis :-



For ac equivalent model :

$$V_o = -g_{m1} V_{gs1} \left(r_{o1} \parallel r_{o2} \parallel r_{o3} \parallel \frac{1}{g_{m2}} \right)$$

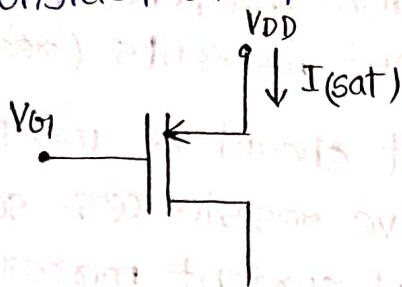
And $V_{in} = V_{gs1}$

$$\Rightarrow V_o = -g_{m1} V_{in} \left(r_{o1} \parallel r_{o2} \parallel r_{o3} \parallel \frac{1}{g_{m2}} \right)$$

$$\Rightarrow \text{voltage gain } A_v = \frac{V_o}{V_{in}} = -g_{m1} \left(r_{o1} \parallel r_{o2} \parallel r_{o3} \parallel \frac{1}{g_{m2}} \right)$$

Why we need current mirror...?

*1. consider the following common source circuit



For saturation region,

the MOSFET current eqⁿ is given by

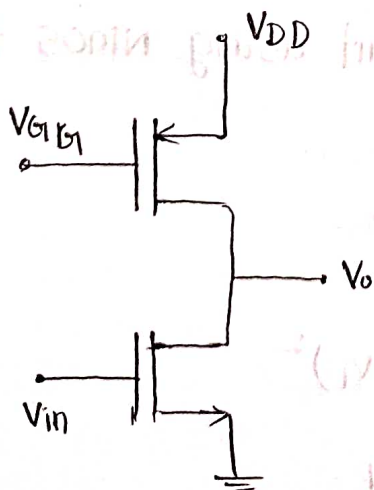
$$I_{sat} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

Temperature dependent

Temperature dependent

$\Rightarrow I_{sat}$ changes with change in temperature which is not desirable.

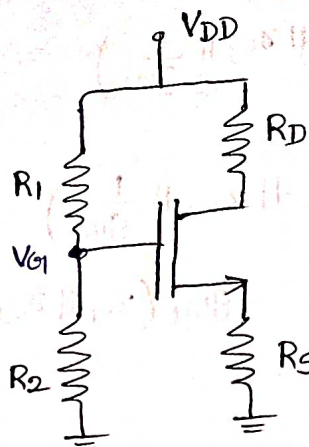
*2.



As no. of MOSFET's increases, the power supply is need to supply for each and every transistor.

Instead of that we use voltage divider bias.

* 3.



Assume the MOSFET is in saturation mode.

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

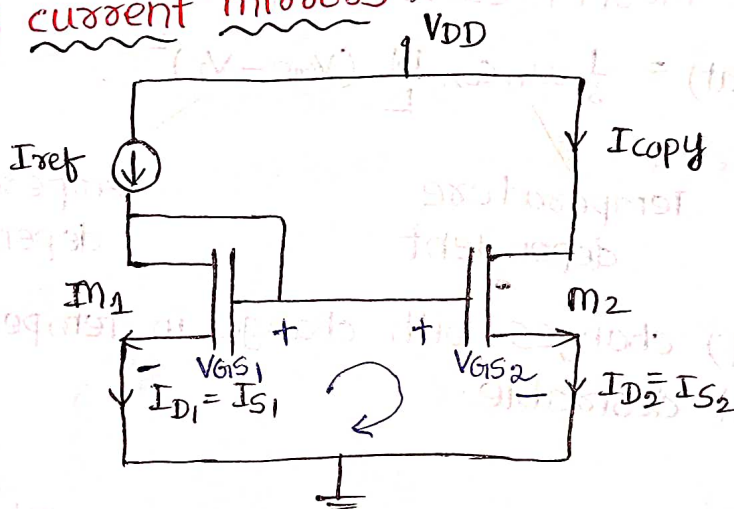
$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left[\frac{V_{DD} R_2}{R_1 + R_2} - V_G - V_T \right]^2$$

$$I_D = \text{function}(\mu_n, V_T, R_1, R_2)$$

⇒ Drain current here also independent on temperature and passive elements (resistance)

But we need drain current should be independent of temperature and passive resistances. So, we need a special circuitry called current mirrors.

MOS current mirrors :-



The current mirror circuit using NMOS transistor is shown above.

For saturation mode

$$I_1 = \frac{1}{2} \mu_n C_{ox} \frac{W_1}{L_1} (V_{GS1} - V_T)^2$$

$$I_{D2} = \frac{1}{2} \mu_n C_{ox} \frac{W_2}{L_2} (V_{GS2} - V_T)^2$$

By KVL for bottom loop:

$$-V_{GS1} + V_{GS2} = 0$$

$$V_{GS1} = V_{GS2} = V_{GS}$$

$$\Rightarrow I_{D1} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{GS} - V_T)^2$$

$$I_{D2} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_2 (V_{GS} - V_T)^2$$

Dividing I_{D1} by I_{D2} :

$$\frac{I_{D1}}{I_{D2}} = \frac{\frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{GS} - V_T)^2}{\frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_2 (V_{GS} - V_T)^2}$$

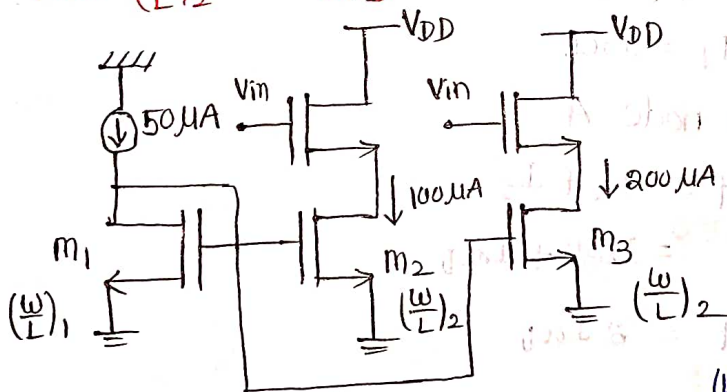
$$\Rightarrow \frac{I_{D1}}{I_{D2}} = \frac{(W/L)_1}{(W/L)_2}$$

Since $I_{D1} = I_{ref}$ and $I_{D2} = I_{copy}$

we have

$$\frac{I_{ref}}{I_{copy}} = \frac{(W/L)_1}{(W/L)_2}$$

#92: A circuit includes 2 source followers biased to $100\mu A$ and $200\mu A$ we have reference current of $50\mu A$. Find $(W/L)_2$ and $(W/L)_3$ w.r.t $(W/L)_1$.



Soln

$$\frac{I_{m1}}{I_{m2}} = \frac{(W/L)_1}{(W/L)_2}$$

$$\frac{50\mu A}{100\mu A} = \frac{(W/L)_1}{(W/L)_2}$$

$$(W/L)_2 = 2 \times (W/L)_1$$

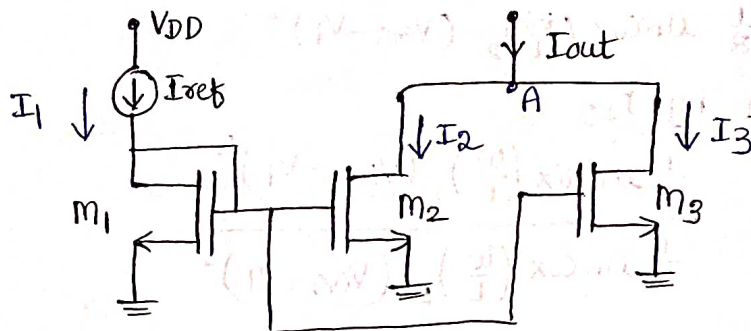
$$\frac{I_{m1}}{I_{m3}} = \frac{(W/L)_1}{(W/L)_3}$$

$$\frac{50\mu A}{200\mu A} = \frac{(W/L)_1}{(W/L)_3}$$

$$(W/L)_3 = 4 \times (W/L)_1$$

$\Rightarrow (W/L)$ ratio of 2nd mosfet is twice of (W/L) ratio of 1st mosfet
 $\Rightarrow (W/L)$ ratio of 3rd mosfet is thrice of (W/L) ratio of 1st mosfet

Q: 3) Find I_{out} if m_1 , m_2 and m_3 are identical



Soln

It is given that 3 MOSFETs m_1 , m_2 and m_3 are identical

$$\Rightarrow \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3$$

From current mirror principle:

$$\frac{I_1}{I_2} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2} = 1$$

$$I_2 = I_1 = I_{ref}$$

$$\text{and } \frac{I_1}{I_3} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_3} = 1$$

$$I_3 = I_1 = I_{ref}$$

By KCL at node A

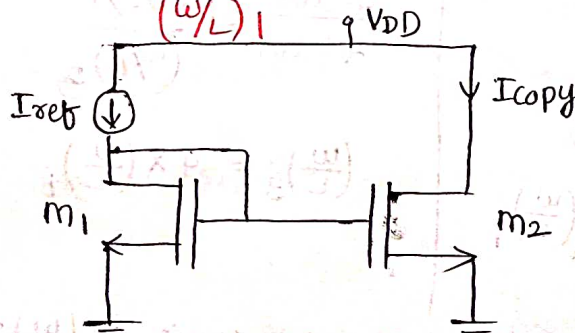
$$\Rightarrow I_{out} = I_2 + I_3$$

$$= I_{ref} + I_{ref}$$

$$\Rightarrow I_{out} = 2 I_{ref}$$

Q4) For given circuit $I_{copy} = \frac{I_{ref}}{2}$

$$\text{Find } \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} = \underline{\hspace{2cm}}$$



soln

From current mirror principle :-

$$\frac{I_{ref}}{I_{copy}} = \frac{(\omega/L)_1}{(\frac{\omega}{L})_2}$$

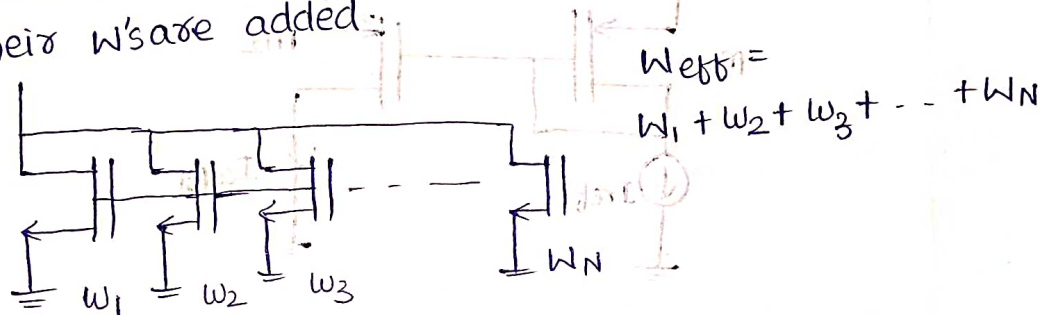
$$\frac{I_{\text{ref}}}{I_{\text{ref}}/2} = \frac{(W/L)_1}{(W/L)_2}$$

$$2 = \frac{(w/L)_1}{(w/L)_2}$$

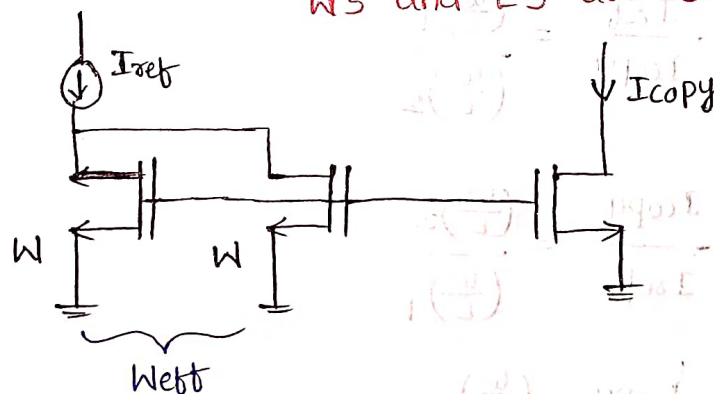
$$\frac{(w/L)_2}{(w/L)_1} = \frac{1}{2}$$

Note :

Note: If MOSFETs are connected in parallel as shown below, if their channel lengths L are same then their W 's are added:



#q5: Find I_{copy} in terms of I_{ref} . Assume their W 's and L 's are same



soln

$$W_{\text{eff}} = w + w = 2w$$

current mirror principle:

$$\frac{I_{\text{ref}}}{I_{\text{copy}}} = \frac{(W/L)_1}{(W/L)_2}$$

when their L 's are equal then

$$\frac{I_{\text{ref}}}{I_{\text{copy}}} = \frac{W_1}{L} \times \frac{L}{W_2}$$

$$\frac{I_{ref}}{I_{copy}} = \frac{W_1}{W_2}$$

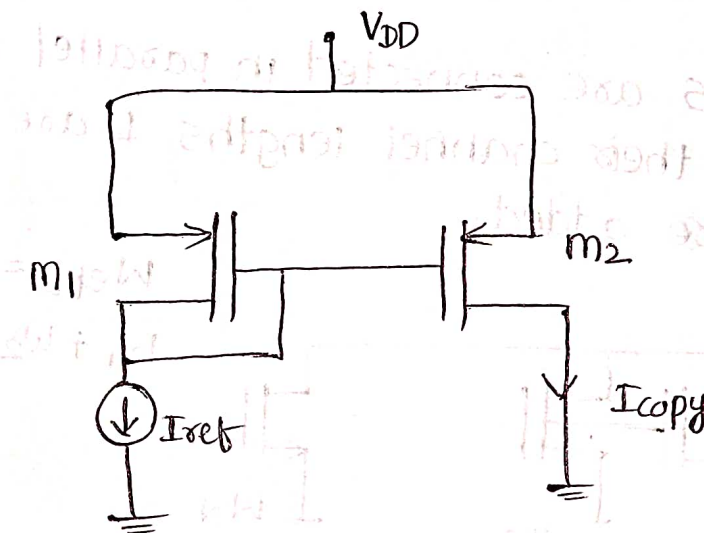
$\Rightarrow$ since $W_1 = 2W$ and $W_2 = W$

$$\Rightarrow \frac{I_{ref}}{I_{copy}} = \frac{2W}{W}$$

$$\Rightarrow I_{ref} = 2I_{copy}$$

$$\Rightarrow I_{copy} = \frac{I_{ref}}{2}$$

pmos current mirror :-

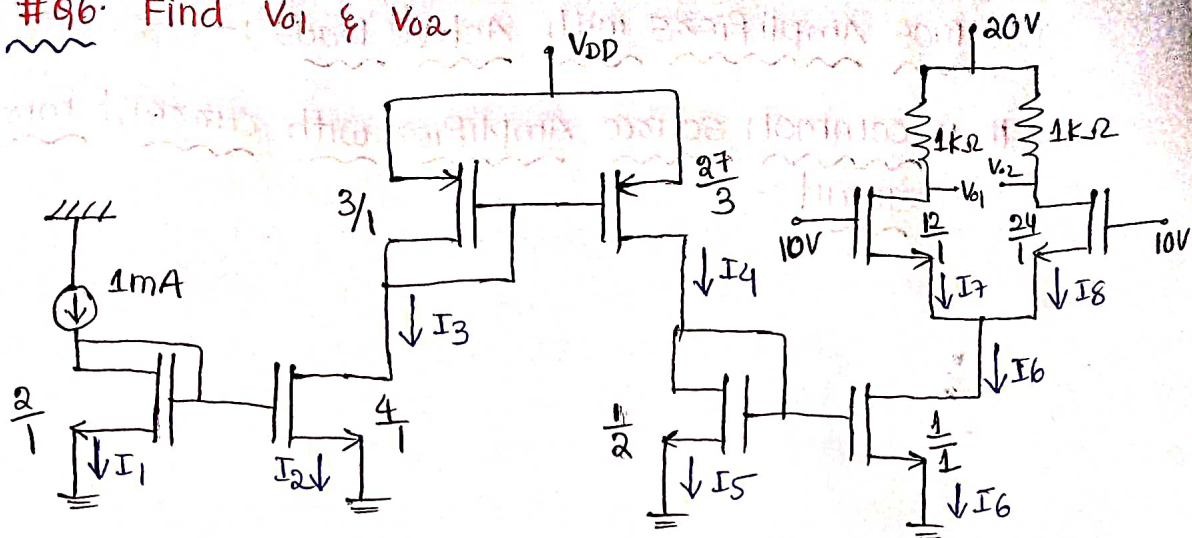


Principle of current mirror:

$$\frac{I_{ref}}{I_{copy}} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}$$

$$\frac{I_{copy}}{I_{ref}} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}$$

$$I_{copy} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} \times I_{ref}$$

#96. Find V_{o1} & V_{o2} soln

From current mirror principle

$$\frac{I_1}{I_2} = \frac{2}{1}$$

$$I_1 = \frac{1}{2} I_2$$

$$I_2 = 2I_1 = 2\text{mA}$$

$$I_3 = I_2 = 2\text{mA}$$

Again from current mirror principle

$$\frac{I_4}{I_3} = \frac{27/3}{3/1}$$

$$\frac{I_4}{I_3} = \frac{27}{3} \times \frac{1}{3}$$

$$I_4 = 3I_3 = 3 \times 2 = 6\text{mA}$$

$$I_5 = I_4 = 6\text{mA}$$

$$\Rightarrow \frac{I_6}{I_5} = \frac{1}{2}$$

$$\Rightarrow I_6 = 2I_5 = 2 \times 6 = 12\text{mA}$$

$$I_7 + I_8 = I_6$$

$$I_7 = \frac{12 \times \frac{12}{1}}{36} = 4\text{mA}$$

$$I_8 = \frac{12 \times 24}{36} = 8\text{mA}$$

 $\Rightarrow$ By KVL,

$$-20 + 1\text{k} I_7 + V_{o1} = 0$$

$$V_{o1} = 20 - 1(I_7) = 20 - 4 = 16\text{V}$$

$$-20 + 1\text{k} I_8 + V_{o2} = 0$$

$$V_{o2} = 20 - 1\text{k} I_8$$

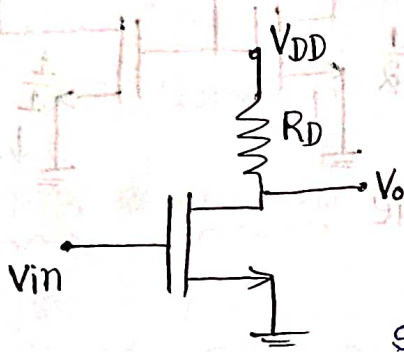
$$= 20 - 1(8)$$

$$= 12\text{V}$$

MOS Amplifiers with Active loads :-

1) Common source Amplifier with current mirror circuit :-

Step 1: Common source Amplifier with resistive load :-



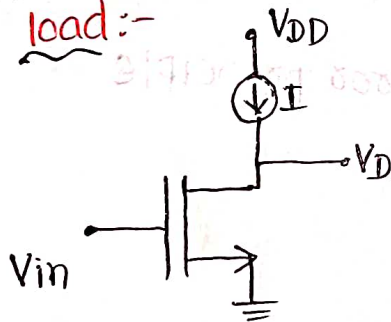
Voltage gain:

$$A_v = -g_m (R_D || r_o)$$

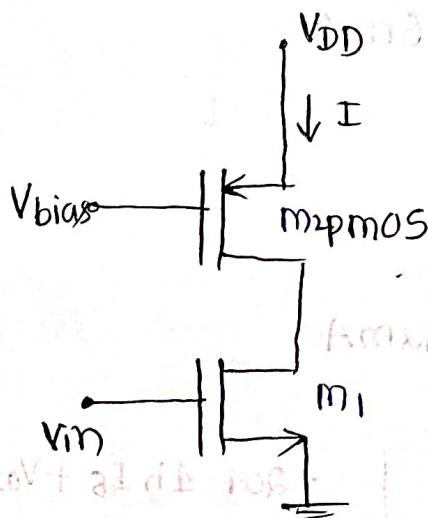
Drawback:

Passive resistances occupies more space and hence it cannot be fabricated on IC ships.

Step 2: Common source Amplifier with current load



The constant current source can be obtained by biasing another PMOS transistor in saturation region.



Voltage gain:

$$A_v = -g_m (r_{o1} || r_{o2})$$

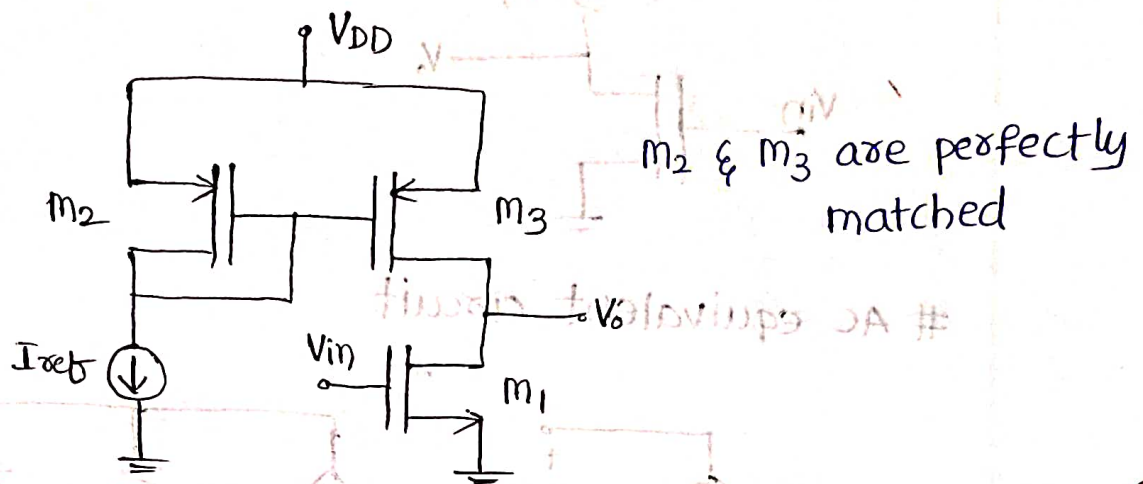
Drawback:

The current flowing through the circuit is function of V_{bias} & temperature.

To avoid and overcome all above drawback, we need to common source Amplifier using current mirror.

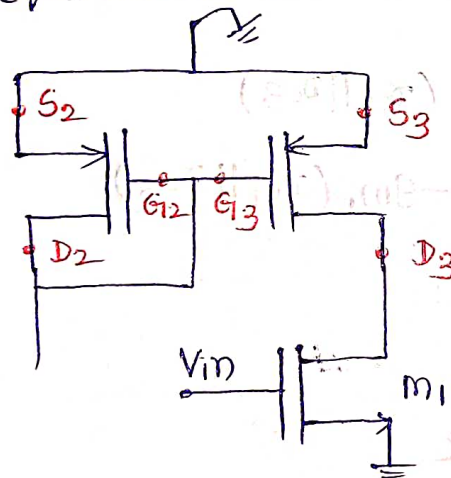
step 3: common source Amplifier with current mirror:-

consider the following CS Amplifier with current mirror load.

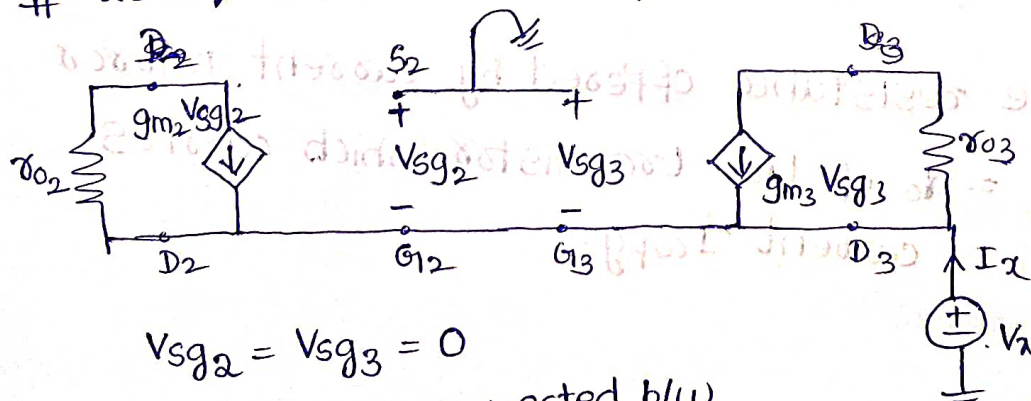


Firstly let us figure the resistance offered by the current mirror circuit.

ac equivalent circuit of current mirror:-



ac equivalent model of current mirror:

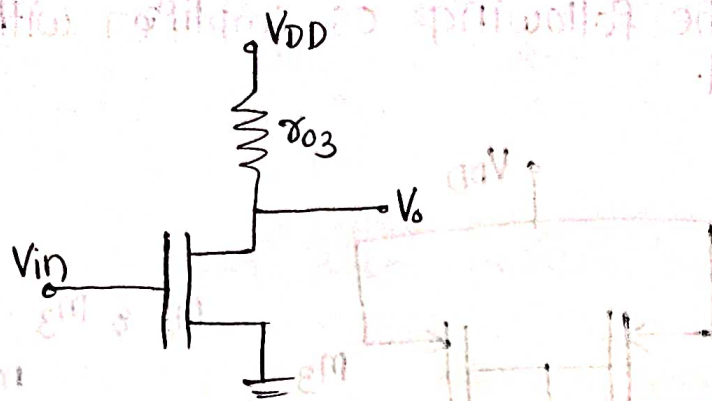


$$V_{sg2} = V_{sg3} = 0$$

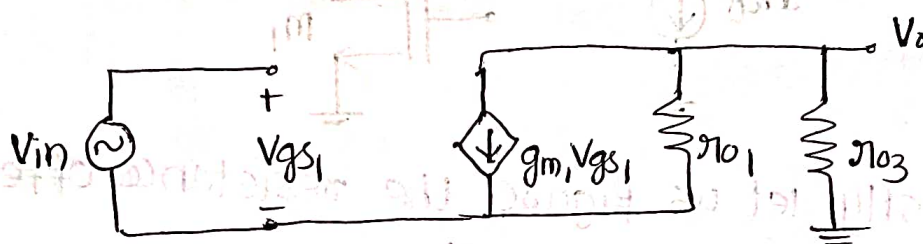
Both are connected b/w grounds.

$$\Rightarrow g_{m2} V_{sg2} = g_{m3} V_{sg3} = 0 \text{ [open circuit]}$$

Now CS Amplifier become as follow:



AC equivalent circuit



$$V_o = -g_{m1} V_{gs1} (r_{O1} \parallel r_{O3})$$

$$\text{And } V_{gs1} = V_{in}$$

$$\Rightarrow V_o = -g_{m1} V_{in} (r_{O1} \parallel r_{O3})$$

$$\Rightarrow A_v = \frac{V_o}{V_{in}} = -g_{m1} (r_{O1} \parallel r_{O3})$$

Input resistance:

$$R_{in} = \infty$$

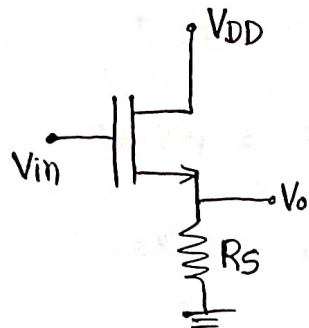
output resistance

$$R_{out} = r_{O1} \parallel r_{O2}$$

The resistance offered by current mirror
 = r_o of the transistor which carries
 current I_{copy} .

a. common drain amplifier:-

step 1: common drain Amplifier using resistive load:-



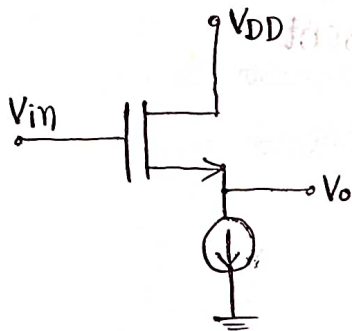
voltage gain:-

$$A_v = \frac{g_m R_s}{1 + g_m R_s}$$

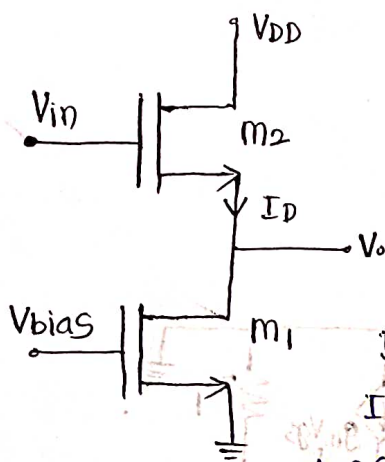
drawback:-

The passive resistive element occupies more space and hence it can't be fabricated on integrated circuit chips.

step 2: common drain Amplifier using current source load:-



The current source can be obtained by another NMOS transistor. Because we need current direction directed from node to ground. We need to bias the NMOS transistor in saturation region.



voltage gain of current source load

$$A_v = \frac{+g_{m2} (r_{o1} \parallel r_{o2})}{1 + g_{m2} (r_{o1} \parallel r_{o2})}$$

drawback:

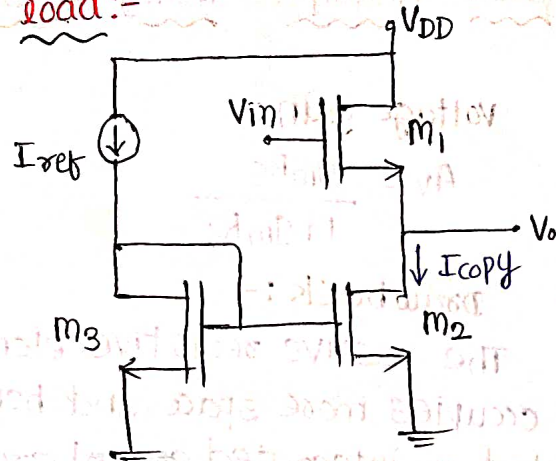
In the common drain current source load the current is function of Vbias and temperature. This is not desirable.

$$I = \text{func}^n (V_{\text{bias}}, \text{Temperature})$$

so, we need to design cd amplifier using current mirror load.

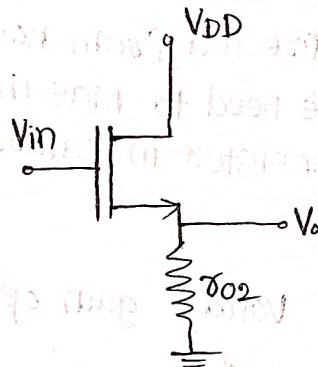
step 3: common drain amplifier using current mirror

load:-

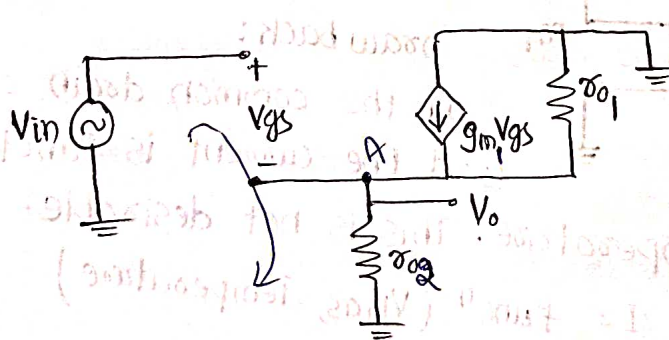


Assume m_2 and m_3 are perfectly matched.

We know that,
the resistance offered by the ^{mirror} current source
= the resistance of mos transistor which
carries I_{copy} current
= r_{o2}



AC equivalent circuit :-



From the circuit by KVL,

$$-V_{in} + V_{gs} + V_o = 0$$

$$V_{gs} = -V_o + V_{in}$$

r_{o1} and r_{o2} are in parallel

KCL @ node A:

$$g_m V_{gs} = \frac{V_o}{r_{o1} \parallel r_{o2}}$$

$$g_m (V_{in} - V_o) = \frac{V_o}{r_{o1} \parallel r_{o2}}$$

$$g_m V_{in} = g_m V_o + \frac{V_o}{r_{o1} \parallel r_{o2}}$$

$$g_m V_{in} = V_o \left(g_m + \frac{1}{r_{o1} \parallel r_{o2}} \right)$$

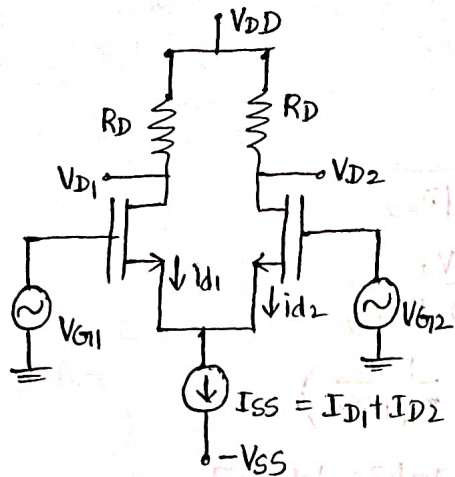
$$g_m V_{in} = V_o \left[\frac{g_m (r_{o1} \parallel r_{o2}) + 1}{r_{o1} \parallel r_{o2}} \right]$$

$$A_v = \frac{V_o}{V_{in}} = \frac{g_m (r_{o1} \parallel r_{o2})}{1 + g_m (r_{o1} \parallel r_{o2})}$$

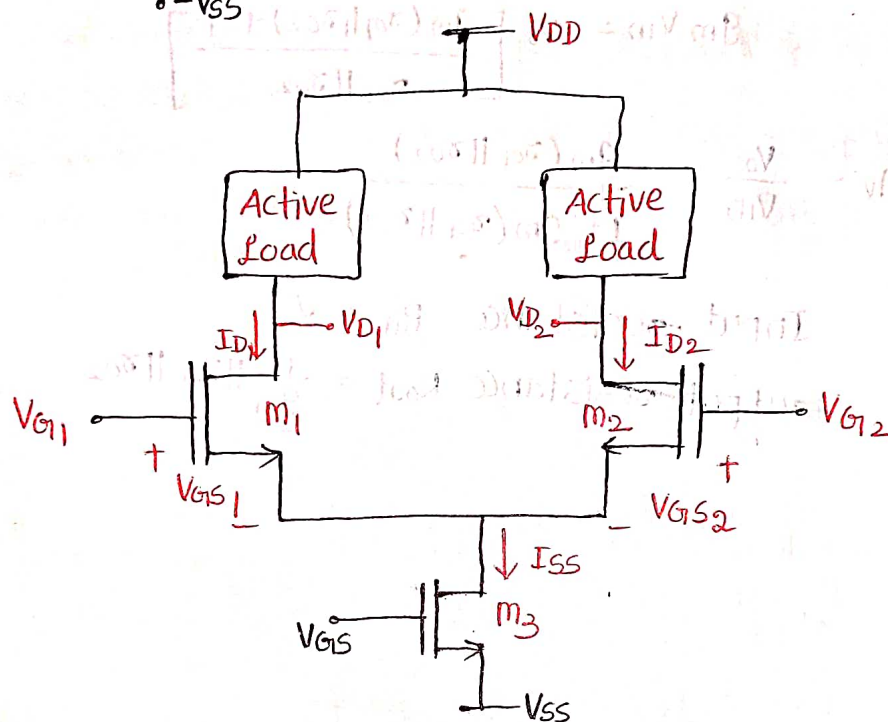
Input resistance $R_{in} = \infty$

output resistance $R_{out} = \frac{1}{g_m} \parallel r_{o1} \parallel r_{o2}$

MOS differential Amplifier with current mirror load



Adjacent figure shows the mos differential amplifier with current ~~mirror~~ source and passive load.



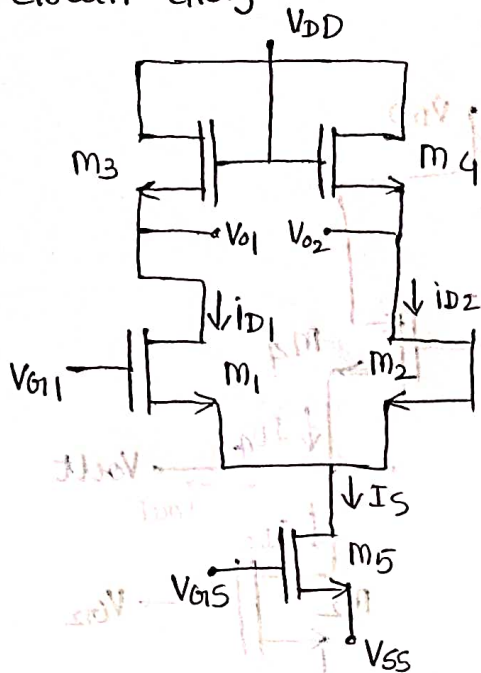
The above circuit shows mos differential amplifier with active loads.

Active Load Advantages:

- 1) Fabrication of active resistors occupy less area on silicon as compared to passive resistors, so a lot of area saving in a IC is possible with use of active resistors.
- 2) In these days, when no. of devices is very large in ICs this area saving per device is highly helpful, not only in just cost reduction but also offers possibility of adding more circuits/ functionality in a single chip.

Step 1: Diode connected Load Differential Amplifier:

circuit diagram:-



Assume that m_1, m_2 are perfectly matched and m_3, m_4 are perfectly matched.

Then

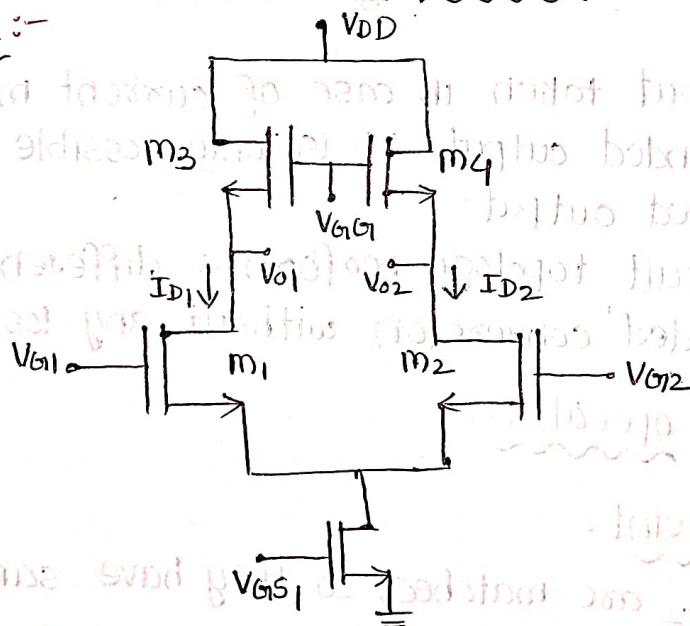
Double ended voltage gain is given by

$$A_{vd} = -g_{m1} \left(r_{o1} \parallel \frac{1}{g_{m3}} \parallel r_{o3} \right)$$

single ended voltage gain is given by

$$A_{vs} = -\frac{g_{m1}}{2} \left(r_{o1} \parallel \frac{1}{g_{m3}} \parallel r_{o3} \right)$$

Step 2: mos differential Amplifier with current source @ load:-



Assume that m_1 & m_2 are perfectly matched, m_3 & m_4 are perfectly matched.

Then,

Double ended voltage gain is given by

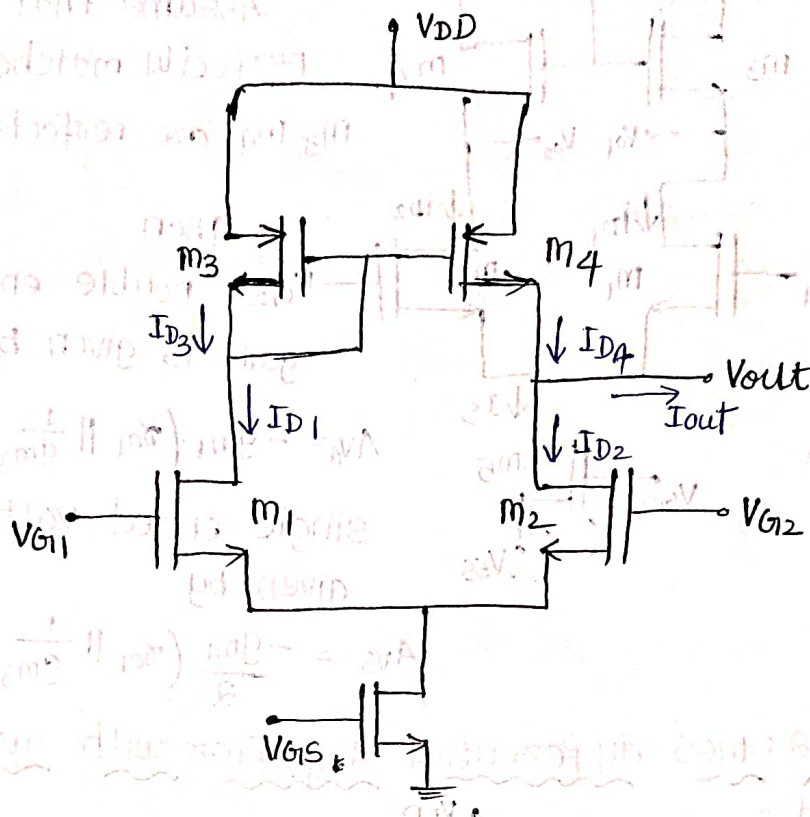
$$A_{vd} = -g_{m1} (r_{o1} \parallel r_{o3})$$

single ended voltage gain is given by

$$A_{vs} = -\frac{g_{m1}}{2} (r_{o1} \parallel r_{o3})$$

step 3: mos differential amplifier with current
mirror load:

circuit diagram:



The output taken in case of current mirror load is single ended output. It is only possible to take single ended output.

This circuit topology performs differential to single ended conversion without any loss of gain

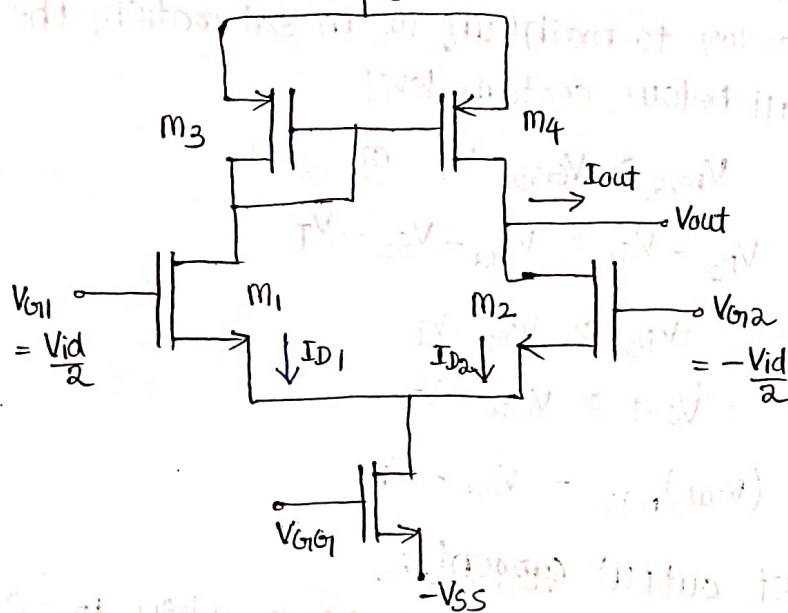
circuit operation:-

quiescent point:

- 1) m_1 and m_2 are matched, so they have same current.
- 2) The current of m_1 also flows through m_3
- 3) The current of m_3 is mirrored into m_4 .
- 4) In zero signal conditions (i.e., under dc biasing) all currents are same
 $\Rightarrow I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_D$
- 5) The currents of m_2 and m_4 are balanced out
- 6) output current is zero.

If V_{id} is applied to differential amplifier i.e, $V_{id} \neq 0$

Let $V_{G1} > V_{G2}$



- 1) I_{D1} increases by ΔI and I_{D2} decreases by same amount.

$$\text{Let } I_{D1} = I_D + \Delta I \quad I_{D2} = I_D - \Delta I$$

- 2) ΔI increase is mirrored through m_3 - m_4 as an increase in I_{D4}

$$I_{D4} = I_D + \Delta I$$

- 3) The current at output node

$$I_{out} = I_{D4} - I_{D2}$$

$$= I_{D4} + \Delta I - (I_D - \Delta I)$$

$$I_{out} = 2\Delta I$$

Large signal Analysis:-

Input signals :

$$V_{id} = V_{G1} - V_{G2}$$

$$V_{G1} = \frac{V_{id}}{2} \quad V_{G2} = -\frac{V_{id}}{2}$$

output dc currents :

$$i_{d1} = i_{d3} = i_{d2} = i_{d4} \quad (\text{q-point})$$

output dc voltage :

$$V_{DA} = V_{DD} - V_{DS4} = V_{DD} - V_{GS4}$$

output voltage limits :

1) smallest output voltage :-

In order to maintain m_2 in saturation, the output cannot fall below certain level

$$V_{DS2} \geq V_{GS2} - V_T \quad \text{or}$$

$$V_{D2} - V_{S2} \geq V_{G12} - V_{S2} - V_T$$

$$\Rightarrow V_{D2} \geq V_{G12} - V_T$$

$$\Rightarrow V_{out} \geq V_{G12} - V_T$$

$$(V_{out})_{\min} = V_{G12} - V_T$$

a) Highest output voltage :-

Highest output voltage occurs when $I_{D2} = 0$ $I_{D1} = I_{SS}$

In order to maintain m_4 in saturation, the output voltage cannot increase above a certain level

$$V_{SD4} \geq V_{SG14} - V_{T4}$$

$$V_{DD} - V_{out} \geq V_{SG14} - V_{T4}$$

$$\Rightarrow V_{out} \leq V_{DD} - V_{SG13} + V_{T4}$$

~~Since $V_{GS3} = V_G$~~ (since $V_{SG14} = V_{SG13}$ above expression is modified.)

$$V_{out} \leq V_{DD} - \sqrt{\frac{2I_{D3}}{K_p'}} - V_{T3} + V_{T4}$$

$\Rightarrow$ since m_3 & m_4 are matched devices $V_{T3} = V_{T4}$

$$\Rightarrow 0 = -V_{T3} + V_{T4}$$

$$-V_{T3} + V_{T4} = 0$$

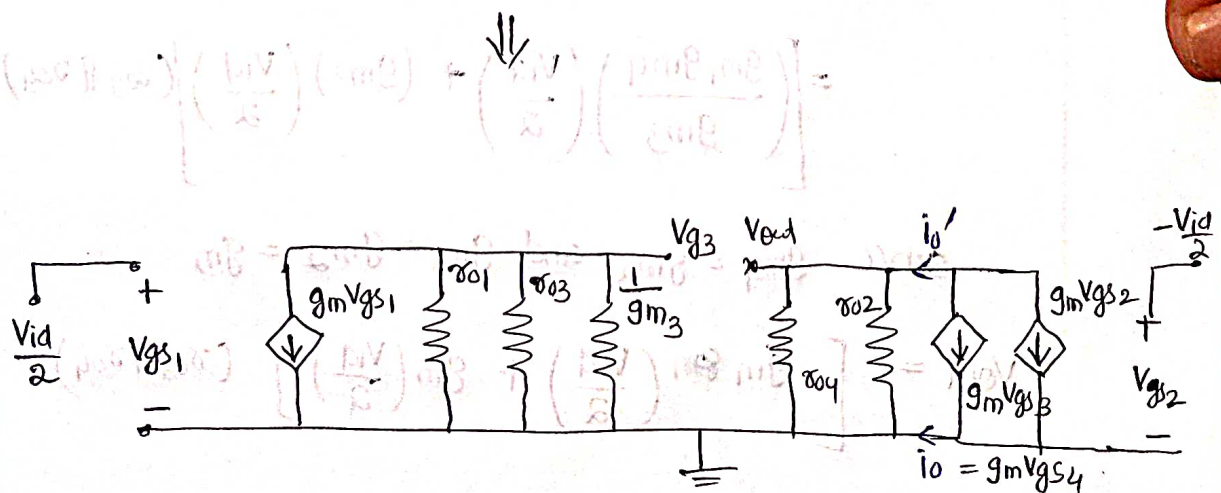
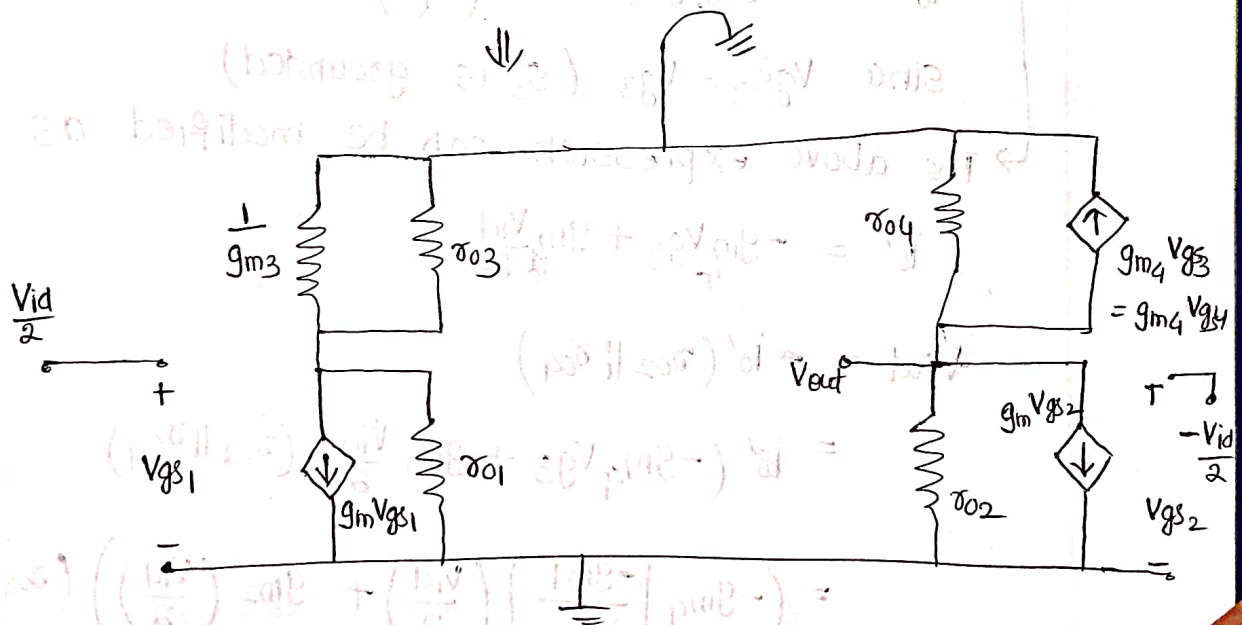
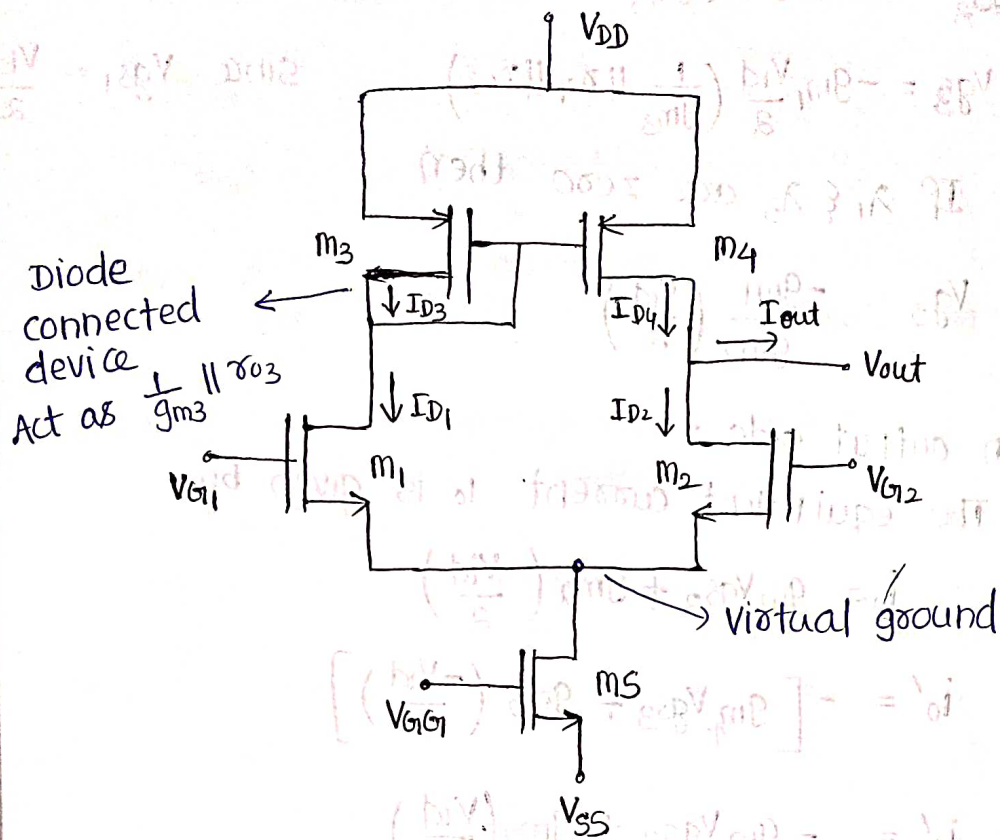
$$\Rightarrow V_{out} \leq V_{DD} - \sqrt{\frac{2I_3}{K_p'}}$$

maximum output voltage

$$\left[V_{out} \leq V_{DD} - \sqrt{\frac{2I_3}{K_p'}} \right]$$

$$(V_{out})_{\max} = V_{DD} - \sqrt{\frac{2I_{D3}}{K_{p3}}}$$

Ac equivalent models :-



$$V_{gs3} = -g_{m1} V_{gs1} \left(\frac{1}{g_{m3}} \parallel r_{o1} \parallel r_{o3} \right)$$

$$\Rightarrow V_{gs3} = -g_{m1} \frac{V_{id}}{2} \left(\frac{1}{g_{m3}} \parallel r_{o1} \parallel r_{o3} \right) \quad \text{since } V_{gs1} = \frac{V_{id}}{2}$$

If λ_1 & λ_3 are zero then

$$V_{gs3} = \frac{-g_{m1}}{g_{m3}} \left(\frac{V_{id}}{2} \right)$$

on output side:

The equivalent current i_o is given by

$$i_o = g_{m4} V_{gs3} + g_{m2} \left(\frac{-V_{id}}{2} \right)$$

$$i_o' = - \left[g_{m4} V_{gs3} + g_{m2} \left(\frac{-V_{id}}{2} \right) \right]$$

$$i_o' = -g_{m4} V_{gs3} + g_{m2} \left(\frac{V_{id}}{2} \right)$$

since $V_{gs3} = V_{gs}$ (S_3 is grounded)

→ The above expression can be modified as

$$i_o' = -g_{m4} V_{gs} + g_{m2} \frac{V_{id}}{2}$$

$$V_{out} = i_o' (r_{o2} \parallel r_{o4})$$

$$= i_o' \left(-g_{m4} V_{gs} + g_{m2} \frac{V_{id}}{2} \right) (r_{o2} \parallel r_{o4})$$

$$= \left(-g_{m4} \left[\frac{-g_{m1}}{g_{m3}} \right] \left(\frac{V_{id}}{2} \right) + g_{m2} \left(\frac{V_{id}}{2} \right) \right) (r_{o2} \parallel r_{o4})$$

$$= \left[\left(\frac{g_{m1} g_{m4}}{g_{m3}} \right) \left(\frac{V_{id}}{2} \right) + g_{m2} \left(\frac{V_{id}}{2} \right) \right] (r_{o2} \parallel r_{o4})$$

since $g_{m4} = g_{m3}$ and $g_{m1} = g_{m2} = g_m$

$$V_{out} = \left[g_m \left(\frac{V_{id}}{2} \right) + g_m \left(\frac{V_{id}}{2} \right) \right] (r_{o2} \parallel r_{o4})$$

$$V_{out} = g_m \left(\frac{V_{id}}{2} \right) (2) (r_{o2} \parallel r_{o4})$$

$$V_{out} = g_m V_{id} (r_{o2} \parallel r_{o4})$$

$$V_{out} = g_{m1} V_{id} (r_{o2} \parallel r_{o4})$$

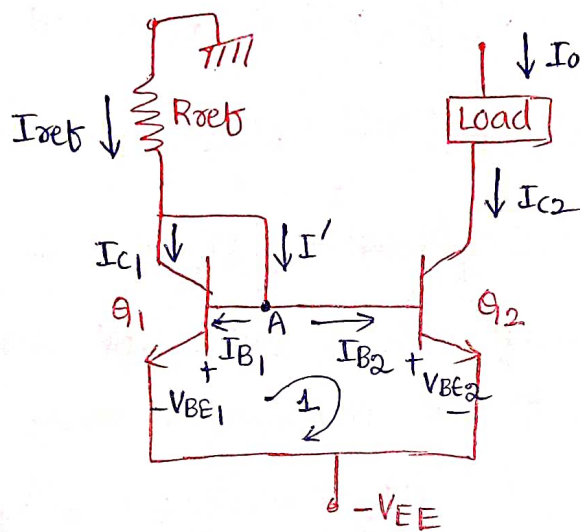
$$A_d = \frac{V_{out}}{V_{id}} = g_{m1} (r_{o2} \parallel r_{o4}) = \frac{g_{m1}}{g_{ds2} + g_{ds4}}$$

$$R_{out} \text{ (output resistance)} = r_{o1} \parallel r_{o3}$$

current mirrors in BJT

current mirror circuit is the circuit which is mirror for current. current mirror means input current and output current are mirror images. i.e., output current is identical as input current. The purpose of the current mirror is used to generate identical currents in the different parts of the circuit and it can also be used to implement constant current biasing.

circuit diagram:



Assume Q_1 and Q_2 are identical.

Applying KVL along path 1:

$$-V_{BE1} + V_{BE2} = 0$$

$$V_{BE1} = V_{BE2}$$

$\Rightarrow$ Base-emitter potential drops of both transistors are same, because both are identical

We know that

$$I_E \propto e^{V_{BE}/\eta V_T}$$

Since V_{BE} is same for both transistors their emitter & base currents are same

$$I_{E1} = I_{E2} \text{ and}$$

$$I_{B1} = I_{B2}$$

By applying KCL at node A:

$$I' = I_{B1} + I_{B2}$$

Since $I_{B1} = I_{B2} = I_B$

$$\Rightarrow I' = 2I_B$$

$$\Rightarrow I' = \frac{2I_{C2}}{\beta}$$

And $I_{ref} = I_{C1} + I'$

Since $I_{C1} = I_{C2}$

$$= I_{C2} + \frac{2I_{C2}}{\beta}$$

$$I_{ref} = I_{C2} \left(1 + \frac{2}{\beta}\right)$$

Since $I_{C2} = I_0$

$$I_{ref} = I_0 \left(1 + \frac{2}{\beta}\right)$$

$$I_0 = \frac{I_{ref}}{1 + \frac{2}{\beta}}$$

If β is very large then $I_0 = I_{ref}$

$\Rightarrow$ If transistor Q_2 is

* npn then it is called current sink (Absorbs current)

* pnp then it is called current source (delivers current)

Drawback:

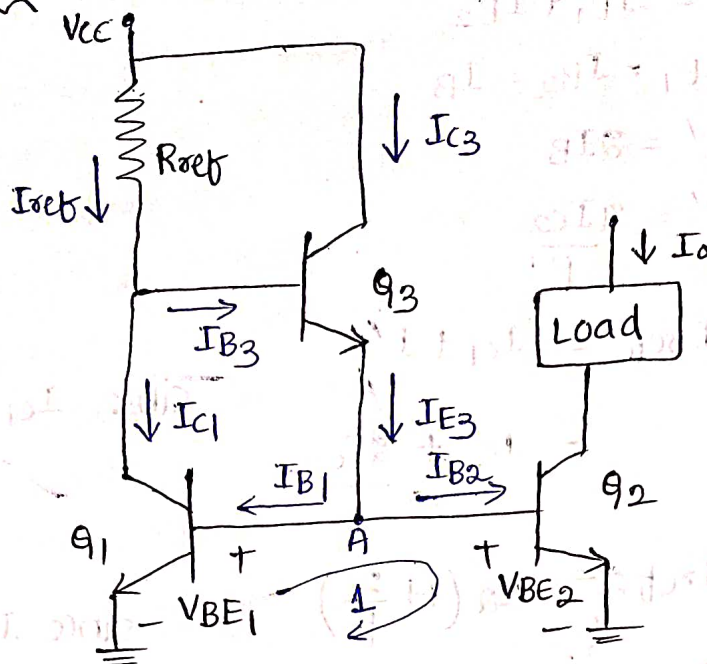
The output current eqⁿ in current mirror circuit is given by

$$I_0 = \frac{I_{ref}}{1 + \frac{2}{\beta}}$$

If β is large then only $I_0 = I_{ref}$

But if β is not large enough then $I_0 < I_{ref}$

modified current mirror circuit:



Assume Q_1 and Q_2 are identical

$$\Rightarrow \beta_1 = \beta_2 = \beta$$

Identical transistors does not mean currents are identical. If their base emitter potential drops are same, then their corresponding currents are same.

Applying KVL along path 1:

$$-V_{BE1} + V_{BE2} = 0$$

$$\Rightarrow V_{BE1} = V_{BE2}$$

Applying KCL at node A:

$$I_{E3} = I_{B1} + I_{B2} \Rightarrow I_{E3} = 2I_B$$

$$I_{B3} = \frac{I_{E3}}{1 + \beta_3} = \frac{2I_B}{1 + \beta_3}$$

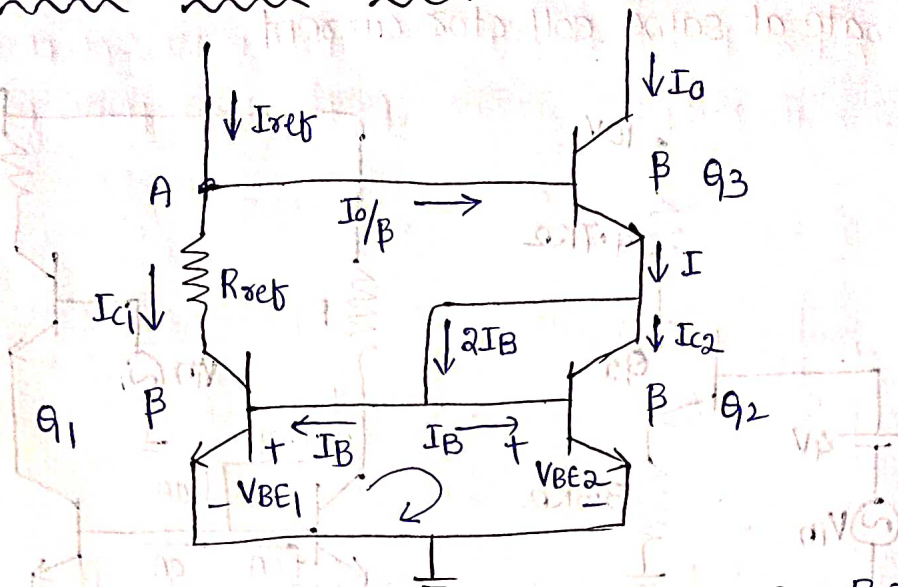
$$\text{For transistor } Q_2 \quad I_B = \frac{I_o}{\beta}$$

$$\Rightarrow I_{B3} = \frac{2\left(\frac{I_o}{\beta}\right)}{1 + \beta_3} = \frac{2}{\beta} \frac{I_o}{1 + \beta_3}$$

$$\text{Since } I_{ref} = I_{B3} + I_{C1} \quad I_{C1} = I_{C2} = I_o$$

$$I_{ref} = \frac{2I_o}{\beta(1 + \beta_3)} + I_o = I_o \left(1 + \frac{2}{\beta(1 + \beta_3)} \right)$$

$$I_o = \frac{I_{ref}}{1 + \frac{2}{\beta(1 + \beta_3)}}$$

Wilson current source :-

All 3 transistors are identical. $\beta_1 = \beta_2 = \beta_3 = \beta$

$$\Rightarrow V_{BE1} = V_{BE2} \text{ (By KVL)}$$

From transistor Q_3

$$I = \frac{I_0}{\beta} + I_0 = I_0 \left(1 + \frac{1}{\beta}\right)$$

$$I = I_{C2} + 2I_B$$

$$I = I_{C2} + 2 \frac{I_{C2}}{\beta} \quad I_{C1} = I_{C2} = I_C$$

$$I = I_C \left(1 + \frac{2}{\beta}\right) \Rightarrow I_C = \frac{I}{1 + \frac{2}{\beta}} = \frac{I_0 \left(1 + \frac{1}{\beta}\right)}{1 + \frac{2}{\beta}}$$

KCL at node A:

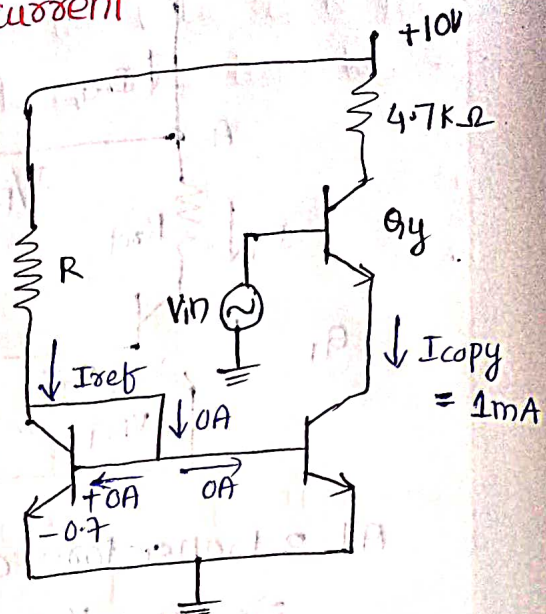
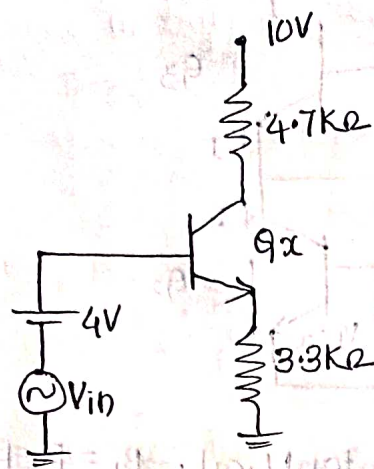
$$I_{ref} = I_{C1} + \frac{I_0}{\beta} = I_C + \frac{I_0}{\beta}$$

$$\Rightarrow I_{ref} = \frac{I_0 \left(1 + \frac{1}{\beta}\right)}{1 + \frac{2}{\beta}} + \frac{I_0}{\beta}$$

$$I_{ref} = I_0 \left(\frac{1 + \frac{1}{\beta}}{1 + \frac{2}{\beta}} + \frac{1}{\beta} \right)$$

$$I_0 = \frac{I_{ref}}{\frac{1}{\beta} + \frac{1 + \frac{1}{\beta}}{1 + \frac{2}{\beta}}} = \frac{I_{ref}}{\frac{1}{\beta} + \frac{1 + \beta}{2 + \beta}}$$

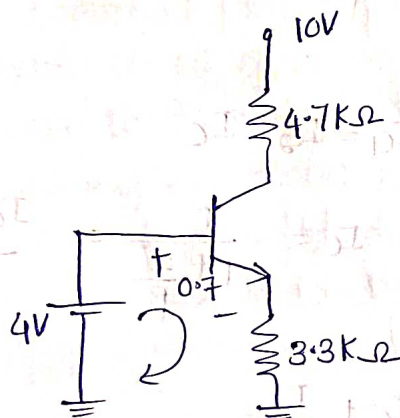
Q7 Find the value of R if transistor Q_x and Q_y operate at same collector current



soln

consider Q_x :

since we are performing dc analysis, ac sources are short circuit and assume β is high



By KVL,

$$-4 + 0.7 + 3.3 I_E = 0$$

$$I_E = \frac{4 - 0.7}{3.3} = 1 \text{ mA}$$

since β is very high

$$I_{C_x} = I_{E_x} = 1 \text{ mA}$$

consider Q_y :-

From current mirror principle:

$$I_{copy} = \frac{I_{ref}}{1 + \frac{2}{\beta}}$$

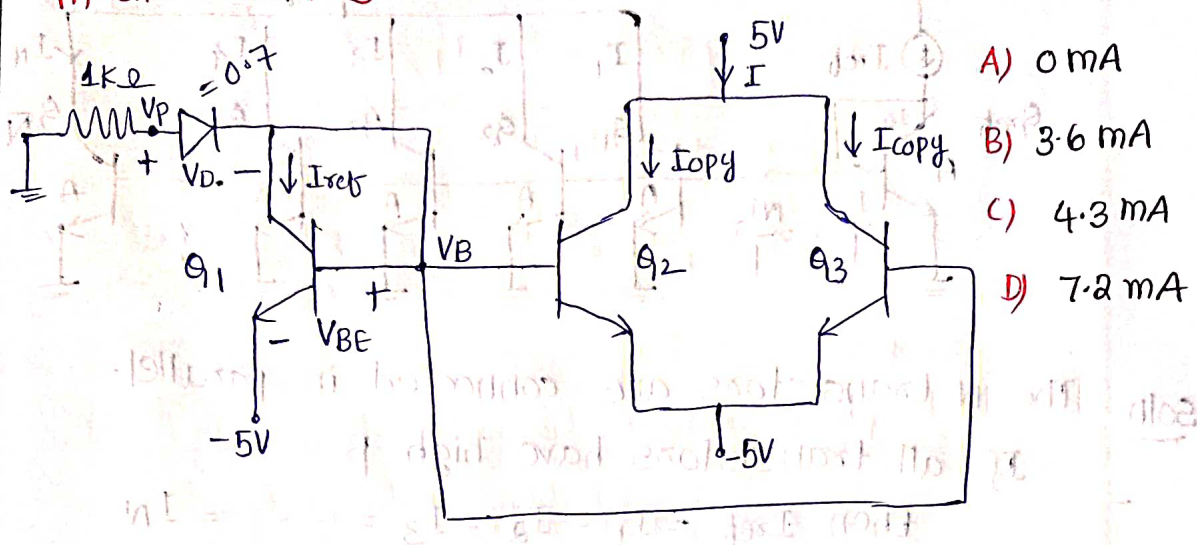
$$\text{since } \beta \text{ is large } I_{copy} = I_{ref} = 1 \text{ mA}$$

By KVL,

$$-10 + R I_{ref} + 0.7 = 0$$

$$R = \frac{10 - 0.7}{I_{ref}} = 9.3 \text{ k}\Omega$$

Q8: For the given circuit, the transistors are perfectly matched and β of the transistor is very high. If the forward voltage drop of diode is $0.7V$ then current I in the circuit is _____



- A) 0 mA
B) 3.6 mA
C) 4.3 mA
D) 7.2 mA

Soln

For Q_1

$$V_E = -5V$$

$$V_{BE} = 0.7$$

$$V_B - V_E = 0.7$$

$$V_B = 0.7 + V_E = 0.7 + (-5)$$

$$V_B = -4.3V$$

Now the diode P side connected to ground and n side is connected to $-4.3V$ and hence voltage across the diode is

$$V_D = V_P - V_n = 0 - (-4.3) = 4.3 > V_{\gamma}$$

$\Rightarrow$ Diode is ON. It is replace by $0.7V$.

Finding potential at V_p :

$$-V_p + 0.7 + (-4.3) = 0$$

$$-V_p = 4.3 - 0.7$$

$$V_p = -3.6V$$

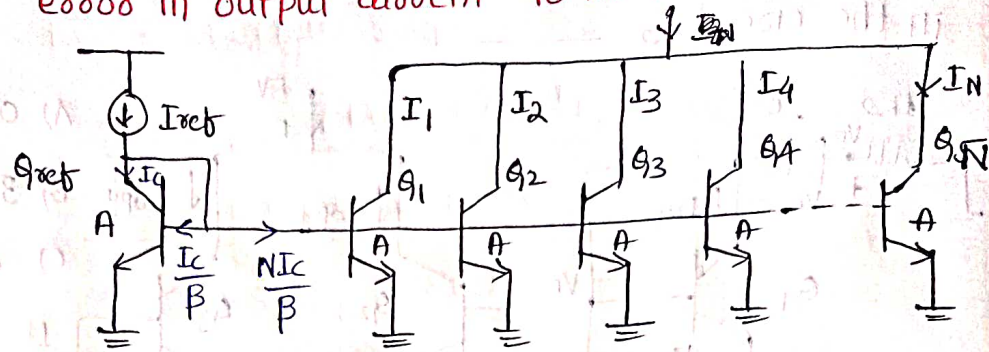
$$I_{4k\Omega} = \frac{0 - (-3.6)}{4k} = 3.6mA$$

$$\Rightarrow I_{ref} = 3.6mA$$

$$I_{copy} = 3.6mA$$

$$I = 2 \times I_{copy} = 2 \times 3.6 = 7.2mA$$

#99: For the given circuit assume all transistors are matched and β is 100. The value of N for the error in output current to be less than 10% —



Soln

The N transistors are connected in parallel.

If all transistors have high β

then $I_{ref} = I_1 = I_2 = I_3 = \dots = I_N$

$$I_{\text{ref}} = I_C + \frac{I_C}{\beta} + N \frac{I_C}{\beta}$$

$$I_{\text{ref}} = \frac{I_C}{\beta} (1 + N) + I_C$$

$$I_C = \frac{I_{\text{ref.}}}{1 + \frac{N+1}{\beta}}$$

It is given that error must be less than 10%.

$$I_N > I_{ref} - \frac{10}{100} I_{ref}$$

$$I_N > 0.9 I_{ref}$$

$$\frac{I_{\text{ref}}}{1 + \frac{N+1}{100}} = 0.9 I_{\text{ref}}$$

$$\cancel{I_{ref}} = \frac{101 + N}{100} \times 0.9 \cancel{I_{ref}}$$

$$N = \frac{100 - 90.9}{0.9}$$

$$N = 10 \cdot 1$$

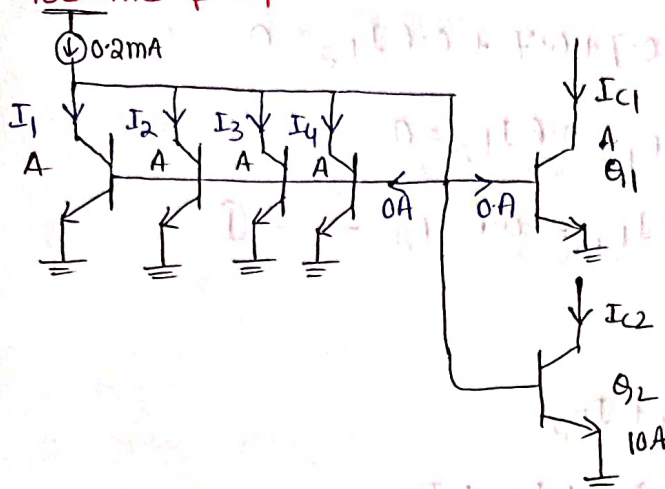
$$N=10$$

$$\text{Exet } \frac{100}{0.9} = 100 + N$$

$$N = \frac{100}{0.9} \approx 101$$

Q10: For the given transistor circuit, the emitter area of Q_2 is 10 times of other transistor. The current I_{C1} and I_{C2} are _____

Assume β of each transistor is very high



Soln

$$I_1 = I_2 = I_3 = I_4 = \frac{0.2}{4} = 50 \mu A$$

$$I_{C(\text{ref})} = 50 \mu A$$

collector current

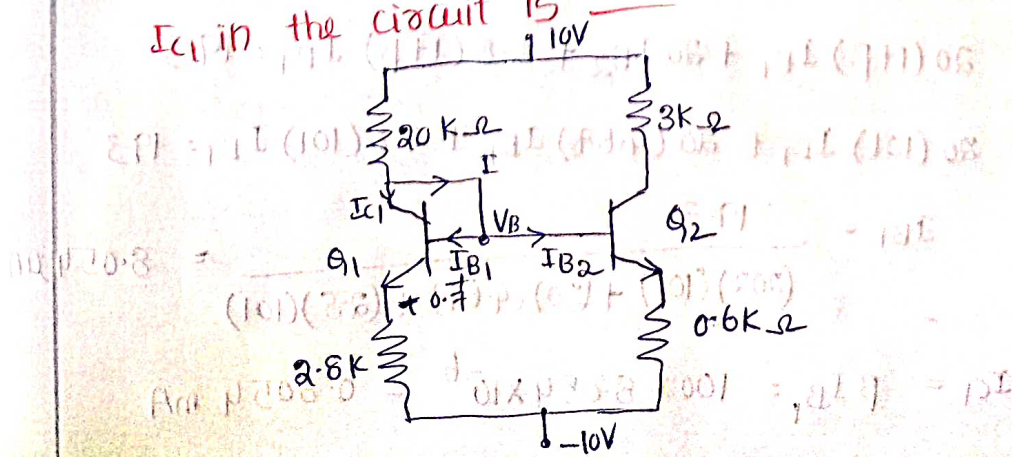
$$I_C = \frac{I_S}{I_{S(\text{ref})}} \times I_{C(\text{ref})}$$

$I_S \rightarrow$ saturation current

$$I_{C1} = \frac{I_{S1}}{I_{S(\text{ref})}} \times I_{C(\text{ref})} = I_{C(\text{ref})} = 50 \mu A = 0.05 \text{ mA}$$

$$I_{C2} = \frac{I_{S2}}{I_{S(\text{ref})}} \times I_{C(\text{ref})} = \frac{10 I_{S(\text{ref})}}{I_{S(\text{ref})}} \times I_{C(\text{ref})} = 10 \times 50 = 500 \mu A = 0.5 \text{ mA}$$

Q11 For the given circuit, assume both transistors are matched perfectly and $V_{BE} = 0.7V$ and $\beta = 100$. The current I_{C1} in the circuit is _____



Soln Potential at point B:

$$-V_B + 0.7 + 2.8 I_{E1} - 10 = 0$$

KVL @ bottom loop:-

$$-2.8 I_{E1} - 0.7 + 0.7 + 0.6 I_{E2} = 0$$

$$-2.8 I_{E1} + 0.6 I_{E2} = 0$$

$$2.8 I_{E1} = 0.6 I_{E2} \longrightarrow \textcircled{1}$$

By KCL:

$$I = I_{B1} + I_{B2}$$

$$I_{ref} = I_{C1} + I_{B1} + I_{B2}$$

$$I_{ref} = \beta I_{B1} + I_{B1} + I_{B2}$$

$$I_{ref} = (1 + \beta) I_{B1} + I_{B2} \longrightarrow \textcircled{2}$$

from eqⁿ ①

$$2.8 I_{E1} = 0.6 I_{E2}$$

$$2.8 (1 + \beta) I_{B1} = 0.6 (1 + \beta) I_{B2}$$

$$I_{B2} = 4.67 I_{B1} \longrightarrow \textcircled{3}$$

By KVL from top to bottom:

$$-10 + 20 I_{ref} + 0.7 + 2.8 I_{E1} - 10 = 0$$

$$20 I_{ref} + 2.8 I_{E1} = 19.3$$

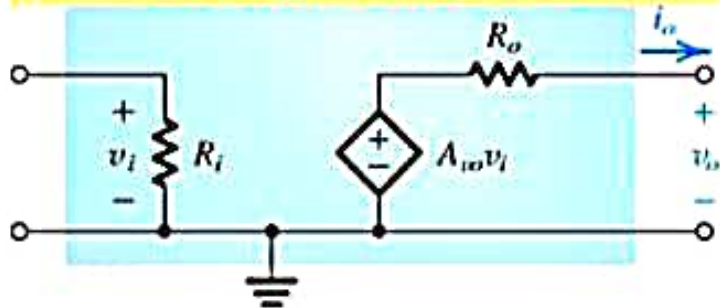
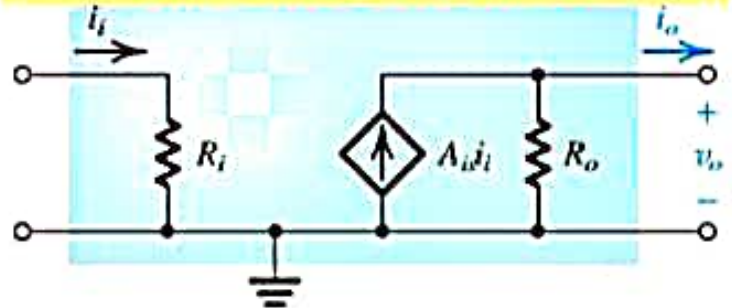
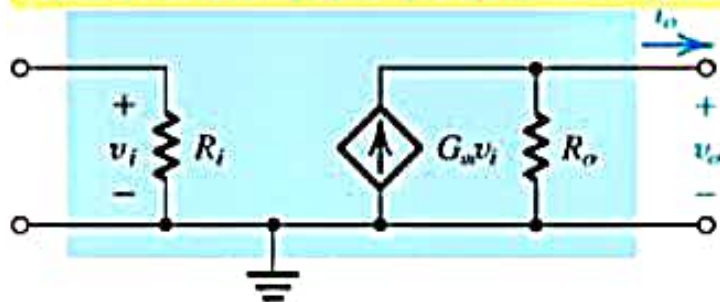
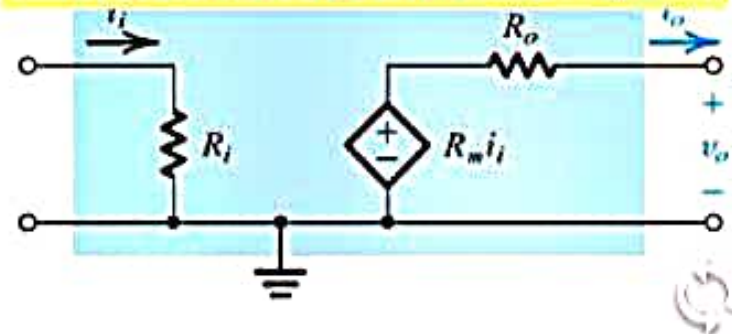
$$20 ((1 + \beta) I_{B1} + I_{B2}) + 2.8 I_{E1} = 19.3$$

$$20 (1 + \beta) I_{B1} + 20 I_{B2} + 2.8 (1 + \beta) I_{B1} = 19.3$$

$$20 (101) I_{B1} + 20 (4.67) I_{B1} + 2.8 (101) I_{B1} = 19.3$$

$$I_{B1} = \frac{19.3}{(202)(101) + (20)(4.67) + (2.8)(101)} = 8.054 \mu A$$

$$I_{C1} = \beta I_{B1} = 100 \times 8.054 \times 10^{-6} = 0.8054 \text{ mA}$$

voltage amplifier**current amplifier****transconductance amp.****transresistance amp.**

NOTE :-

Hi friends....

This is a miscellaneous concept based on types of Amplifiers...

Sir taught to section 1 and section 2 peoples so I include that concept here....

Thank you.....

Miscellaneous concepts

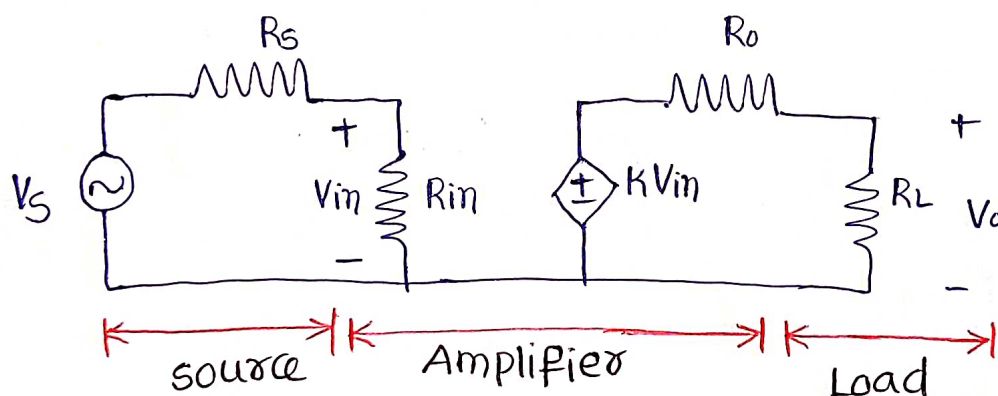
Types of Amplifier:

There are generally 4 kinds of amplifiers. They are

- 1) voltage Amplifier
- 2) current Amplifier
- 3) Transconductance Amplifier
- 4) Transresistance Amplifier

1) voltage Amplifier:

circuit diagram:



$KV_{in} \rightarrow$ dependent voltage source

And dependent voltage source has its value depend on input voltage V_{in}

$KV_{in} \rightarrow$ voltage controlled voltage source (VCVS)

$\Rightarrow$ voltage Amplifier is also called as voltage controlled voltage source.

Input side:

By voltage division:

$$V_{in} = \frac{V_s \times R_{in}}{R_s + R_{in}}$$

output side :

voltage division:

$$V_o = K V_{in} \times \frac{R}{R_L + R_o}$$

for maximum V_o , V_{in} should be maximum

$$V_{in(max)} = V_s$$

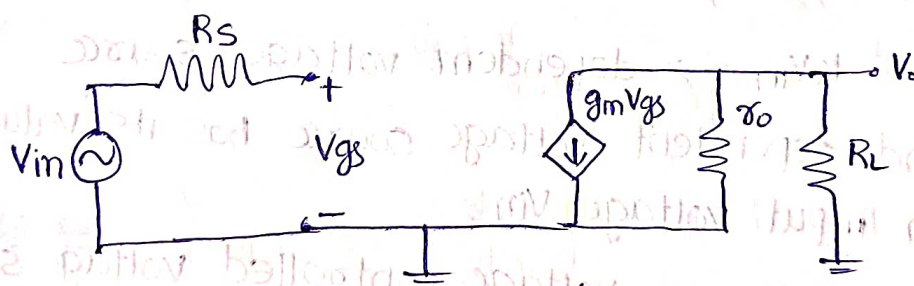
This will happen $R_{in} \rightarrow \infty$

$$\Rightarrow V_{in} = V_s \frac{R_{in}}{R_s + R_{in}}$$

$$V_{in} = \frac{V_s}{\left(\frac{R_s}{R_{in}}\right) + 1}$$

As $R_{in} \rightarrow \infty$ then $V_{in} = V_s = V_{in(max)}$

For voltage amplifier R_{in} should be as high as possible. This kind of behaviour we observed in MOSFET Amplifier.



For mosfet as shown above $R_{in} \rightarrow \infty$

$\Rightarrow$ Gate and source terminals are opened.

For maximum V_{out} , $R_o \rightarrow 0$

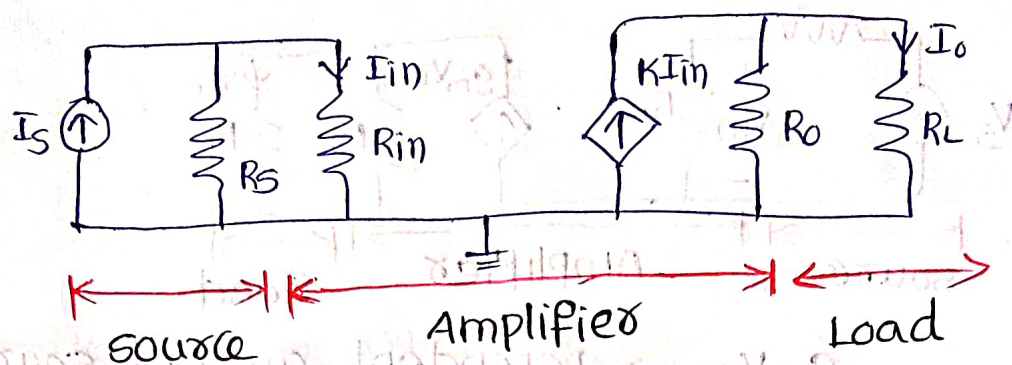
Requirements for voltage amplifier:

Input resistance $\rightarrow$ High

Output resistance $\rightarrow$ Low

2 current Amplifier:

circuit diagram:



$K I_{in} \rightarrow$ dependent current source.

The dependent current source has its value depends on input current I_{in}

$K I_{in} \rightarrow$ current controlled current source (CCCS)

Input side:

current division:

$$I_{in} = \frac{I_s \times R_s}{R_s + R_{in}}$$

output side

current division:

$$I_o = \frac{K I_{in} \times R_o}{R_o + R_L}$$

for I_o to be maximum $\rightarrow I_{in}$ should be maximum.

$$I_{in(max)} = I_s$$

For $I_{in(max)} = I_s$ R_{in} should be zero.

For I_o to be maximum. $R_o \rightarrow \infty$

$$I_o = \frac{K I_{in} \times R_o}{R_o + R_L} = \frac{K I_{in}}{1 + \frac{R_L}{R_o}} = K I_{in}$$

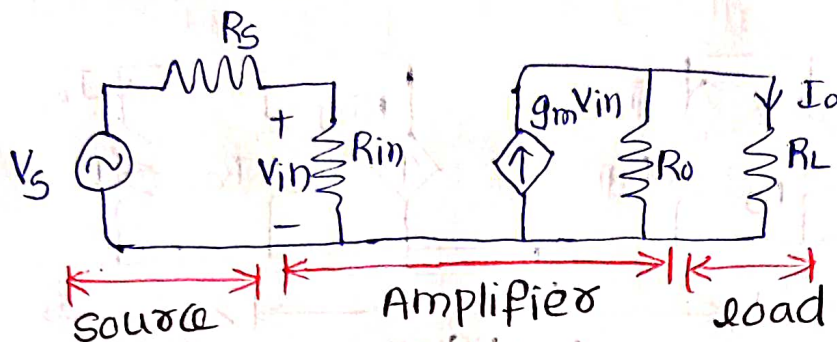
For current Amplifier:

Input resistance $\rightarrow$ Low

output resistance $\rightarrow$ High.

3. Transconductance Amplifier:

circuit diagram:-



$g_m V_{in} \rightarrow$ dependent current source

For dependent current source, it depends on input voltage

$\Rightarrow g_m V_{in} \rightarrow$ voltage controlled current source

Input side:

voltage division:

$$V_{in} = \frac{V_s \times R_{in}}{R_s + R_{in}}$$

output side:

current division

$$I_o = \frac{g_m V_{in} \times R_o}{R_o + R_L}$$

for maximum I_o , V_{in} should be maximum.

$$V_{in} = \frac{V_s R_{in}}{R_s + R_{in}} = \frac{V_s}{1 + \frac{R_s}{R_{in}}} = V_s \quad (\text{when } R_{in} \rightarrow \infty)$$

For maximum I_o ,

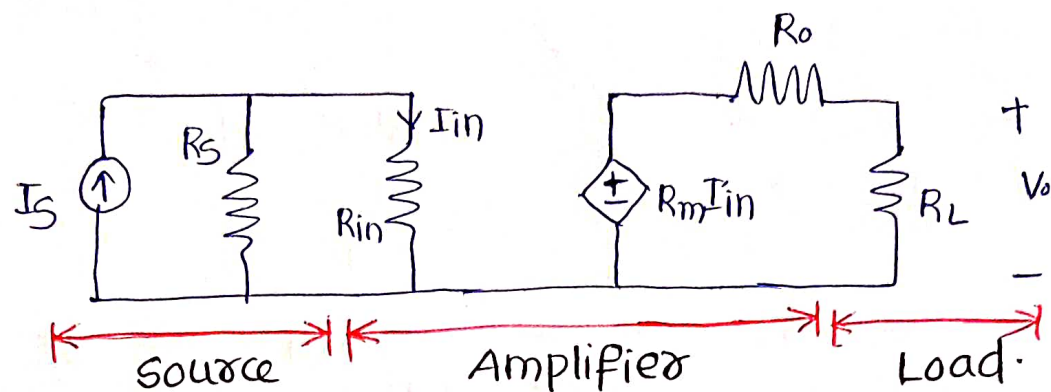
$$I_o = \frac{g_m V_{in} \times R_o}{R_o + R_L} = \frac{g_m V_{in}}{1 + \frac{R_L}{R_o}} = g_m V_{in} \quad (\text{when } R_o \rightarrow \infty)$$

Requirements for transconductance amplifier

- 1) High input resistance
- 2) High output resistance

#.4) Transresistance Amplifier:-

circuit diagram:



$R_m I_{in} \rightarrow$ dependent voltage source

For dependent voltage source,
it depends on input voltage.

$\Rightarrow R_m I_{in} \rightarrow$ current controlled voltage source.

Input side:

~~For~~ current division:

$$I_{in} = I_S \times \frac{R_S}{R_S + R_{in}}$$

output side:

voltage division:

$$V_o = \frac{R_m I_{in} \times R_L}{R_o + R_L}$$

For maximum V_o , I_{in} should be maximum.

For maximum I_{in}

$$I_{in} = I_S \times \frac{R_S}{R_S + R_{in}} = I_S \quad (\text{when } R_{in} \rightarrow 0)$$

For maximum V_o

$$V_o = \frac{R_m I_{in} \times R_L}{R_o + R_L} = R_m I_{in} \quad (\text{when } R_o \rightarrow 0)$$

Requirements for transconductance amplifier:

- 1) Low input resistance
- 2) Low output resistance.

