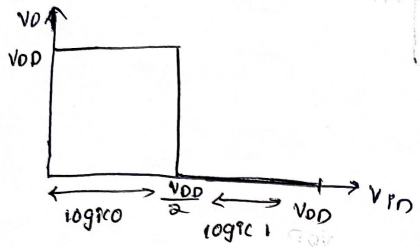
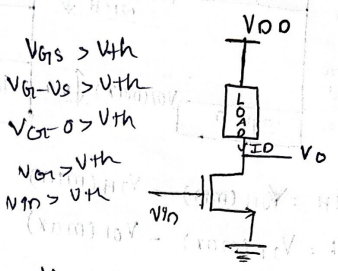
Unit 4 - CMOS CIRCUITS

CMOS :- complementary metal oxide semiconductor
↳ combination of pmos and nmos

NMOS inverter :-

ideal voltage transfer characteristics :-





$V_o = V_{DD} - I_D z$

$V_{in} = 0 \Rightarrow V_o = V_{DD}$ (high)

$V_{in} \neq 0 \Rightarrow V_o = V_{DD} - I_D z$ (low)

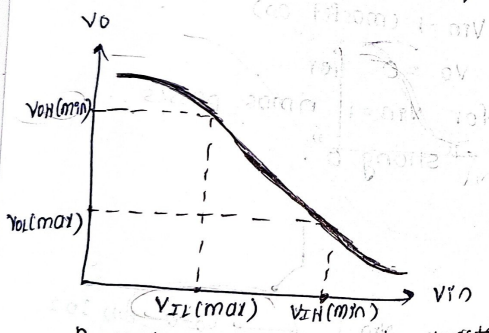
Practical voltage transfer characteristics

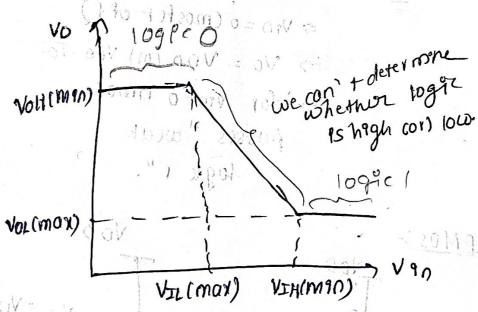
$V_{OH}(min)$ = min o/p voltage for logic high = 5V.

$V_{OL}(max)$ = max o/p voltage for logic low = 1.2V

$V_{IH}(min)$ = min i/p voltage for logic high = 4V

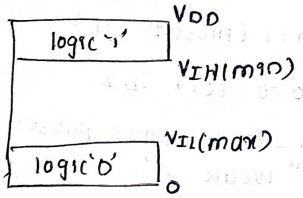
$V_{IL}(max)$ = max i/p voltage for logic low = 1.6 V



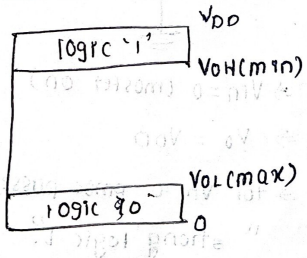


Practical voltage transfer characteristics

For input



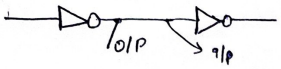
For output



⇒ Noise margin :-

* Noise margin should be high for better functionality.

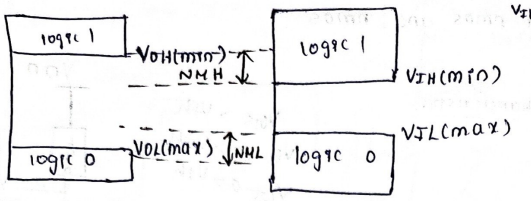
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$V_{OH(min)} = 3$ noise will be dr added

⇒ 1 is added to 3 (or) subtracted

⇒ 3.1 — logic 1



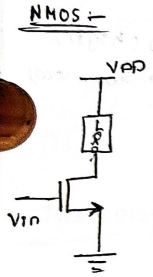
$V_{IH(min)} = 2$

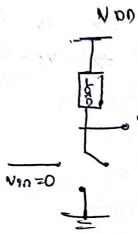
⇒ we will get logic 1 for 3.1, 4, 5, 6 o/p's etc

$NMH = V_{OH(min)} - V_{IH(min)}$

$NML = V_{IL(max)} - V_{OL(max)}$

NMOS :-

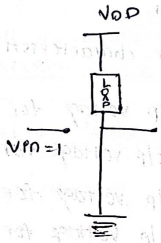




⇒ $V_{in} = 0$ (mosfet off)

⇒ $V_O = V_{DD}$ (or) $V_{DD} - I_D Z$

⇒ for $V_{in} = 0$ nmos passes "weak logic 1".



⇒ nmos passes strong 0.

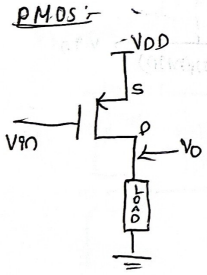
⇒ pmos passes strong 1.

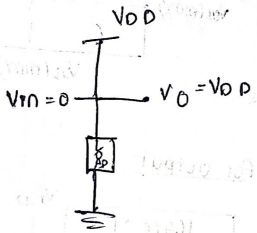
⇒ $V_{in} = 1$ (mosfet on)

⇒ $V_O = 0$

⇒ for $V_{in} = 1$ nmos passes "strong 0".

PMOS :-

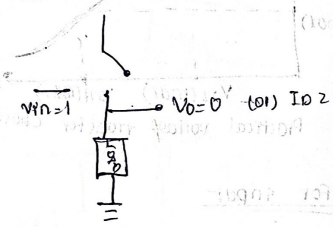




⇒ $V_{in} = 0$ (mosfet on)

⇒ $V_O = V_{DD}$

⇒ for $V_{in} = 0$ pmos passes "strong logic 1".

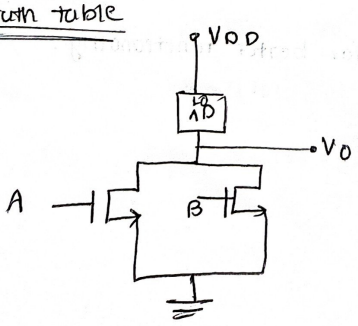


⇒ $V_{in} = 1$ (mosfet off)

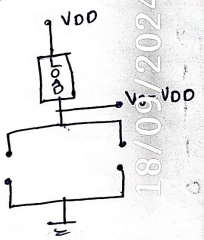
⇒ $V_O = 0$ (or) $I_D Z$

⇒ for $V_{in} = 1$ pmos passes "weak 0"

⇒ Verify truth table



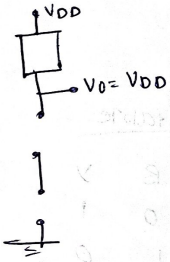
Case 1 :- A = 0, B = 0



Truth table :

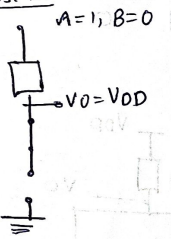
⇒ Case 1 :-

A = 0, B = 0



Case 2 :-

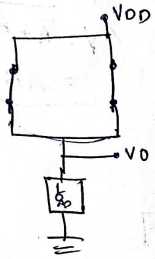
A = 1, B = 0



for PMOS

Case 1 :-

A = 0, B = 0

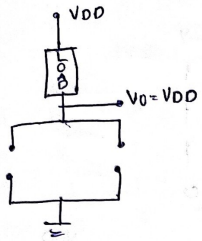


$V_O = V_{DD}$

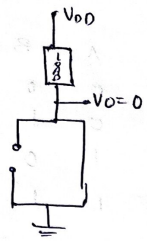
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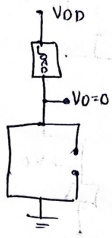
case i :- A=0, B=0



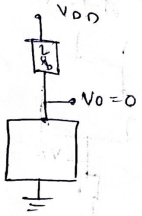
case ii A=0, B=1



case iii :- A=1, B=0



case iv :- A=1, B=1



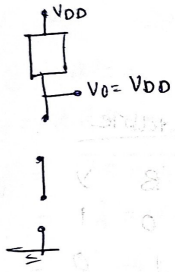
Truth table :

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

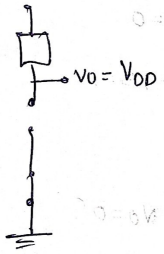
$Y = \overline{A+B}$

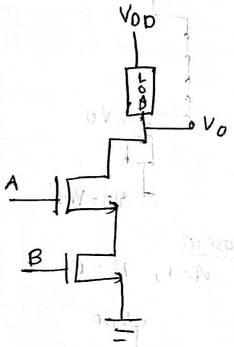
$V_0 = \overline{A+B}$

⇒ case i :- A=0, B=0



case ii A=0, B=1



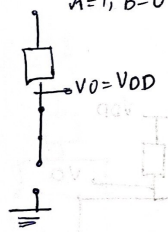


$V_0 = \overline{A \cdot B}$

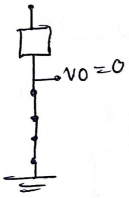
Truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

case iii A=1, B=0

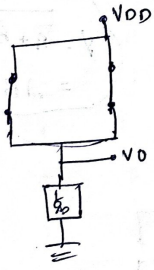


case iv :- A=1, B=1



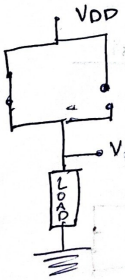
for PMOS

case i :- A=0, B=0

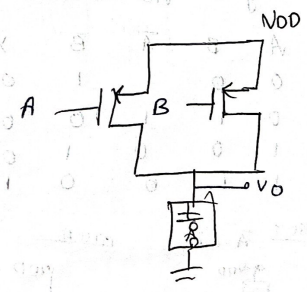


$V_0 = V_{DD}$

case ii A=0, B=1

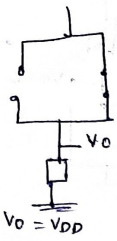


$V_0 = V_{DD}$

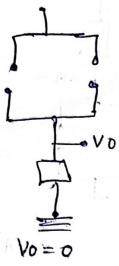


$V_0 = \overline{A \cdot B}$

case iii: A=1, B=0



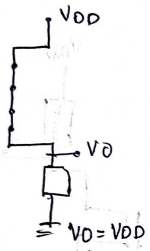
case iv: A=1, B=1



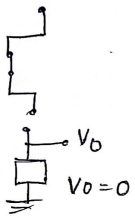
Truth table

A	B	y
0	0	1
0	1	1
1	0	1
1	1	0

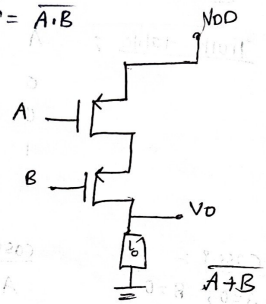
⇒ case i: A=0, B=0



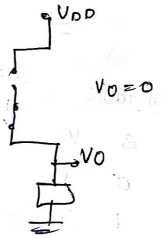
case ii: A=0, B=1



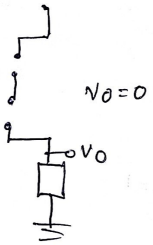
$Y = \overline{A \cdot B}$



case iii: A=1, B=0



case iv: A=1, B=1



Truth table

A	B	y
0	0	1
0	1	0
1	0	0
1	1	0

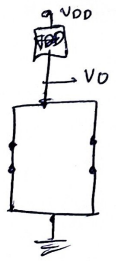
⇒ AND gate:

$y = AB$

$\bar{y} = \overline{AB} = \bar{A} + \bar{B}$

A	B	$\bar{A}$	$\bar{B}$	y
0	0	1	1	0
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

case i: $\bar{A}=1$ $\bar{B}=1$



case ii

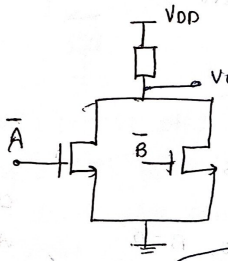


case iii



case iv





$y = \overline{\bar{A} + \bar{B}}$

$= AB$

⇒ OR gate

$y = A + B$

$\bar{y} = \overline{A+B} = \bar{A} \cdot \bar{B}$

A	B	$\bar{A}$	$\bar{B}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0	0

case i:



case



⇒ $y = A \oplus B$ (XOR

$y = A \oplus B = \bar{A}B +$

$\bar{y} = \overline{\bar{A}B + A\bar{B}}$

$= \overline{\bar{A}B} \cdot \overline{B\bar{A}}$

$= (A + \bar{B}) \cdot (B +$

$= AB + \bar{A}\bar{B}$

case i



case ii



A	B	$\bar{A}$	$\bar{B}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0	0

⇒ OR gate

$y = A + B$

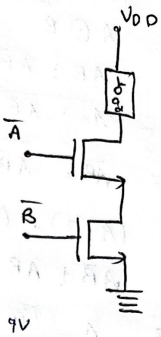
$\bar{y} = \overline{A+B} = \bar{A} \cdot \bar{B}$

A	B	$\bar{A}$	$\bar{B}$	Y
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

$Y = \overline{\bar{A} \cdot \bar{B}}$

$= \bar{\bar{A}} + \bar{\bar{B}}$

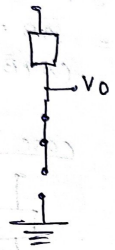
$Y = A + B$



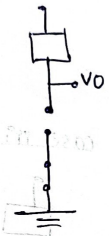
case i :—



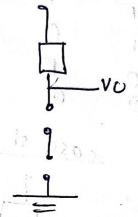
case ii



case iii



case iv



⇒ $y = A \oplus B$ (XOR gate)

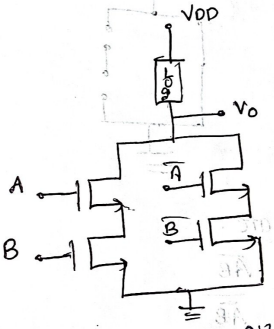
$y = A \oplus B = \bar{A}B + A\bar{B}$

$\bar{y} = \overline{\bar{A}B + A\bar{B}}$

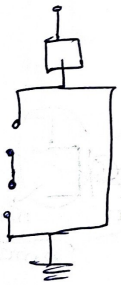
$= \overline{\bar{A}B} \cdot \overline{\bar{B}A}$

$= (A + \bar{B}) \cdot (B + \bar{A})$

$= AB + \bar{A}\bar{B}$



case i



case ii



case iii



case iv



A	B	$\bar{A}$	$\bar{B}$	Y
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	0

$y = \overline{AB + \bar{A}\bar{B}}$

$= \cancel{\bar{A} \cdot \bar{B} \cdot (A+B)}$

$= \overline{AB} \cdot \overline{\bar{A}\bar{B}}$

$= (\bar{A} + \bar{B}) \cdot (A + B)$

$= A\bar{A} + \bar{A}B + A\bar{B} + B\bar{B}$

$= A\bar{B} + \bar{A}B$

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⇒ XNOR gate.

$y = A \odot B$

$y = A\bar{B} + \bar{A}B$

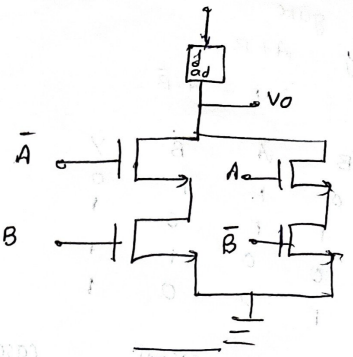
$\bar{y} = \overline{A\bar{B} + \bar{A}B}$

$= \overline{A\bar{B}} \cdot \overline{\bar{A}B}$

$= (\bar{A}+B) \cdot (A+\bar{B})$

$= A\bar{B} + \bar{A}B$

A	B	$\bar{A}$	$\bar{B}$	y
0	0	1	1	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1



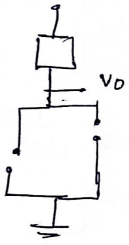
$y = A\bar{B} + \bar{A}B$

$= \overline{A\bar{B}} \cdot \overline{\bar{A}B}$

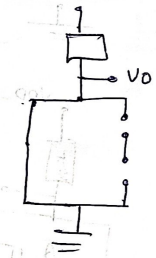
$= (A+\bar{B}) \cdot (\bar{A}+B)$

$= AB + \bar{A}\bar{B}$

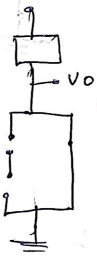
case 1



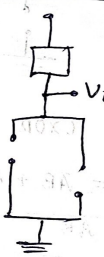
case 2



case 3



case 4



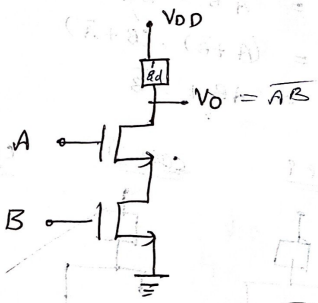
⇒ NAND gate.

$y = \overline{AB}$

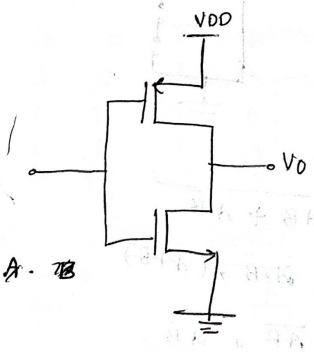
$\bar{y} = \overline{\bar{A}\bar{B}}$

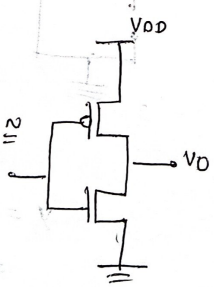
$= [illegible]$

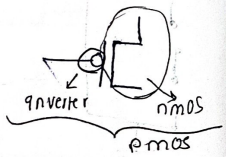
$\bar{y} = AB$

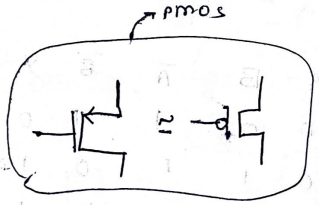


⇒ CMOS :-





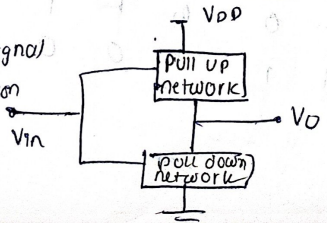




cmos → combination of pmos & nmos

⇒ both nmos & pmos have common i/p signal

⇒ In pull up network we always have combination of pmos and in pull down ntk we always have combination of nmos



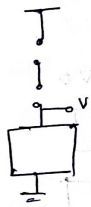
① Implementing

$y = AB$

$\bar{y} = A\bar{B}$

A	B	$\bar{A}$
0	0	1
0	1	1
1	0	0
1	1	0

case 1



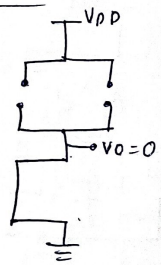
② OR with

$y = A + B$

$\bar{y} = \overline{A+B}$

A	B	
0	0	1
0	1	
1	0	
1	1	

case 1



③ NAND with

$y = \overline{AB}$

$\bar{y} = \overline{\overline{AB}} =$

A	B	
0	0	1
0		
1		

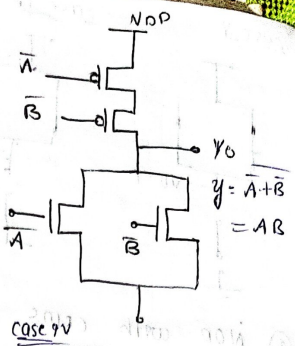
18/09/2024 22:55

① Implementing AND with CMOS :-

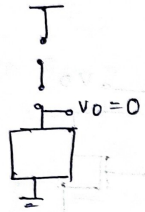
$y = AB$

$\bar{y} = \overline{AB} = \bar{A} + \bar{B}$

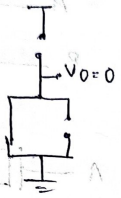
A	B	$\bar{A}$	$\bar{B}$	y
0	0	1	1	0
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1



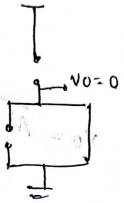
case I



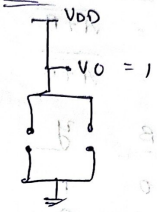
case II



case III



case IV

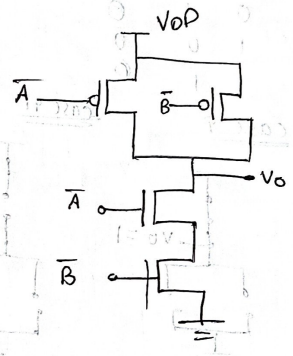


② OR with CMOS

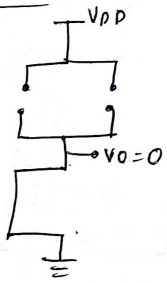
$y = A + B$

$\bar{y} = \overline{A+B} = \bar{A}.\bar{B}$

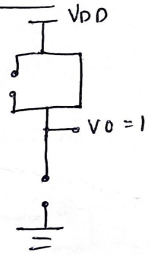
A	B	$\bar{A}$	$\bar{B}$	y
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1



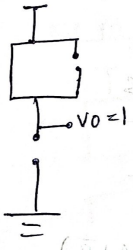
case I



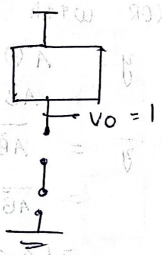
case II



case III



case IV

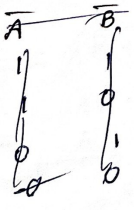


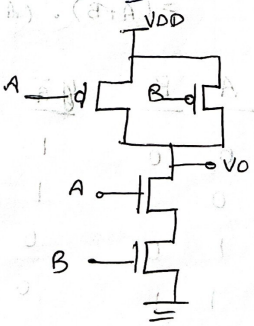
③ NAND with CMOS :-

$y = \overline{AB}$

$\bar{y} = \overline{\overline{AB}} = AB$

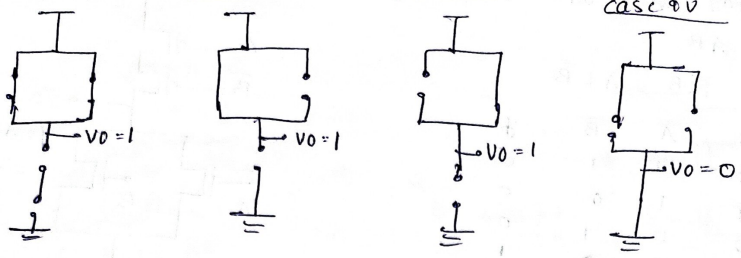
A	B	y
0	0	1
0	1	1
1	0	1
1	1	0





$y = \overline{AB}$

case 1 | case 11 | case 111 | case IV



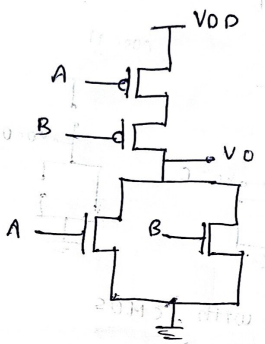
④ NOR with CMOS

$y = \overline{A+B}$

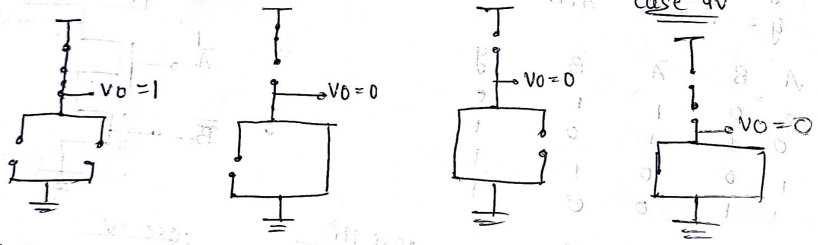
$\bar{y} = \overline{\overline{A+B}} = A+B$

A	B	y
0	0	1
0	1	0
1	0	0
1	1	0

$V_0 = \overline{A+B}$



case 1 | case 11 | case 111 | case IV



⑤ XOR with CMOS

$y = A \oplus B$

$= A\bar{B} + \bar{A}B$

$\bar{y} = \overline{A\bar{B} + \bar{A}B}$

$= \overline{A\bar{B}} \cdot \overline{\bar{A}B}$

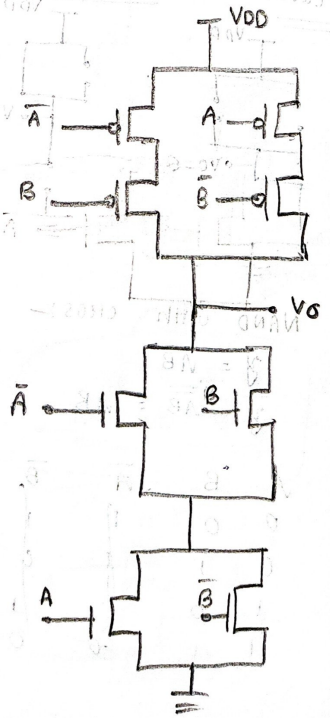
$= (\bar{A}+B) \cdot (A+\bar{B})$

A	B	$\bar{A}$	$\bar{B}$	y
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	0

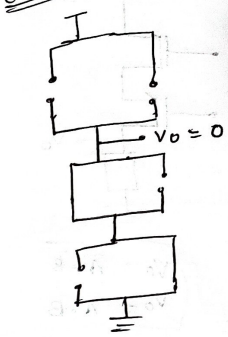
$V_0 = \overline{(\bar{A}+B) \cdot (A+\bar{B})}$

$= \overline{\bar{A}+B} + \overline{(A+\bar{B})}$

$= (A \cdot \bar{B}) + (\bar{A} \cdot B)$



case 1



⑥ XNOR with CMOS

$y = A \odot B$

$= AB + \bar{A}\bar{B}$

$\bar{y} = \overline{AB + \bar{A}\bar{B}}$

$= \overline{AB} \cdot \overline{\bar{A}\bar{B}}$

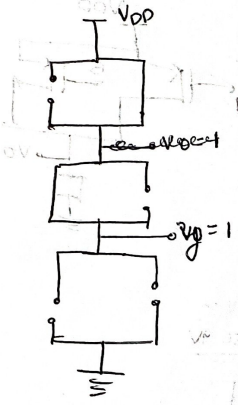
$= (\bar{A}+\bar{B}) \cdot (A+$

$= A\bar{A} + A\bar{B} + A\bar{B}+$

$= \bar{A}B + A\bar{B}$

A	B	$\bar{A}$	$\bar{B}$	
0	0	1	1	
0	1	1	0	
1	0	0	1	
1	1	0	0	

case 1 | case



$y = \overline{\bar{A}B +$

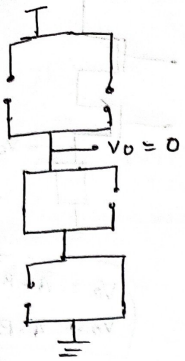
$= \overline{\bar{A}B} \cdot$

$= (A+\bar{B})$

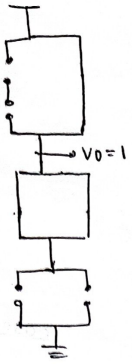
$= A\bar{A}$

$= A\bar{B}$

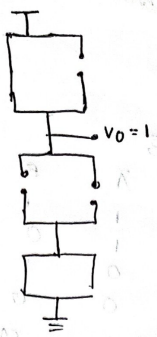
case १



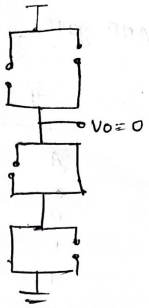
case २



case ३



case ४



⑥ XNOR with CMOS

$y = A \odot B$

$= AB + \bar{A}\bar{B}$

$\bar{y} = \overline{AB + \bar{A}\bar{B}}$

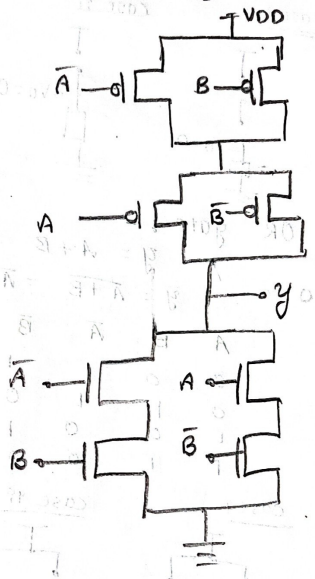
$= \overline{AB} \cdot \overline{\bar{A}\bar{B}}$

$= (\bar{A}+\bar{B}) \cdot (A+B)$

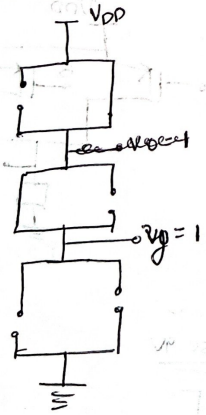
$= A\bar{A} + \bar{A}B + A\bar{B} + B\bar{B}$

$= \bar{A}B + A\bar{B}$

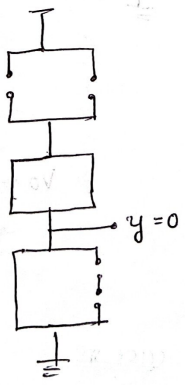
A	B	$\bar{A}$	$\bar{B}$	y
0	0	1	1	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1



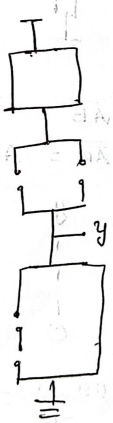
case १



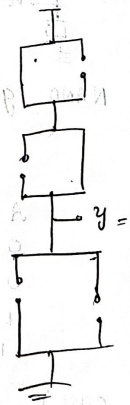
case २



case ३



case ४



$y = \overline{\bar{A}B + A\bar{B}}$

$= \overline{\bar{A}B} \cdot \overline{A\bar{B}}$

$= (A+\bar{B}) \cdot (\bar{A}+B)$

$= A\bar{A} + AB + \bar{B}\bar{A} + B\bar{B}$

$= AB + \bar{A}\bar{B}$

Implementing gates with PMOS :-

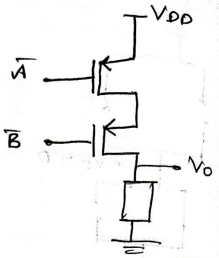
① AND gate

$y = AB$

$\bar{y} = \overline{AB}$

$= \bar{A} + \bar{B}$

A	B	$\bar{A}$	$\bar{B}$	y
0	0	1	1	0
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1



$V_o = \bar{A} + \bar{B}$

$V_o \neq A \cdot B$

case 1 : $V_o = 0$

case 2 : $V_o = 0$

case 3 : $V_o = 0$

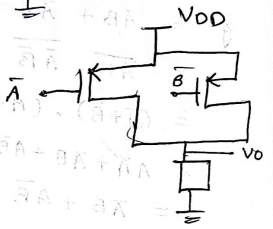
case 4 : $V_o = 1$

② OR gate :-

$y = A + B$

$\bar{y} = \overline{A+B} = \bar{A} \cdot \bar{B}$

A	B	$\bar{A}$	$\bar{B}$	y
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1



$V_o = \overline{\bar{A} \cdot \bar{B}}$

$= \bar{\bar{A}} + \bar{\bar{B}}$

$= A + B$

case 1 : $V_o = 0$

case 2 : $V_o = 1$

case 3 : $V_o = 1$

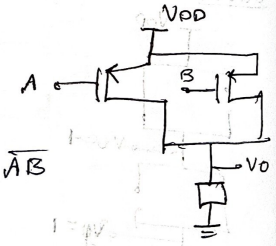
case 4 : $V_o = 1$

③ NAND gate :-

$y = \overline{AB}$

$\bar{y} = \overline{\overline{AB}} = AB$

A	B	y
0	0	1
0	1	1
1	0	1
1	1	0



$V_o = \overline{AB}$

case 1 : $V_o = 1$

case 2 : $V_o = 1$

case 3 : $V_o = 1$

case 4 : $V_o = 0$

④ NOR gate :-

$y = \overline{A + B}$

$\bar{y} = \overline{\overline{A+B}} = A$

A	B	
0	0	
0	1	
1	0	
1	1	

case 1 : $V_o = 1$

case 2 :

⑤ XOR gate :-

$\bar{y} = \overline{A\bar{B} + \bar{A}B} =$

A	B	$\bar{A}$	
0	0	1	
0	1	1	
1	0	0	
1	1	0	

case 1 : $V_o = 0$

case 2 :

⑥ XNOR gate :-

$\bar{y} = \overline{AB + \bar{A}\bar{B}}$

A	B	$\bar{A}$	
0	0	1	
0	1	1	
1	0	0	
1	1	0	

case 1 : $V_o = 1$

case 2 :

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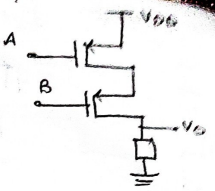
4) NOR gate :-

$y = \overline{A+B}$

$\bar{y} = \overline{\overline{A+B}} = A+B$

A	B	y
0	0	1
0	1	0
1	0	0
1	1	0

$V_o = \overline{A+B}$



case 1 : $V_o = 1$

case 2 : $V_o = 0$

case 3 : $V_o = 0$

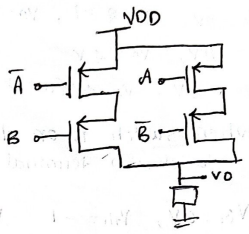
case 4 : $V_o = 0$

5) XOR gate :-

$\bar{y} = A\bar{B} + \bar{A}B = \overline{A\bar{B}} \cdot \overline{\bar{A}B}$

$= (\bar{A}+B) \cdot (A+\bar{B})$

A	B	$\bar{A}$	$\bar{B}$	y
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	0



case 1 : VDD, $V_o = 0$

case 2 : VDD, $V_o = 1$

case 3 : VDD, $V_o = 1$

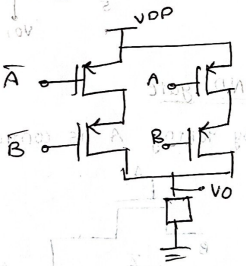
case 4 : $V_o = 0$

6) XNOR gate :-

$\bar{y} = \overline{AB + \bar{A}\bar{B}} = \overline{AB} \cdot \overline{\bar{A}\bar{B}}$

$= (\bar{A}+\bar{B}) \cdot (A+B)$

A	B	$\bar{A}$	$\bar{B}$	y
0	0	1	1	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1



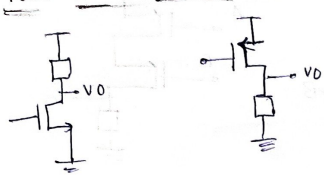
Case 1 : VDD, $V_o = 1$

case 2 : VDD, $V_o = 0$

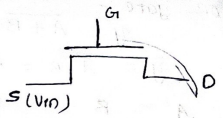
case 3 : VDD, $V_o = 0$

case 4 : VDD, $V_o = 1$

Pass transistor logic :- (PTL) :-



In both the cases we are getting whatever voltage present at source has o/p V_o.



$V_o = \min(V_G - V_T, V_{in})$

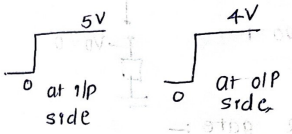
Let $V_T = 1V$ $V_{GS} \geq V_t$ (mosfet on)

1) $V_S = 0$, $V_G - V_S \geq V_{th}$
$5 - 0 \geq V_{th}$
$V_o = 0V$

2) $V_S = 3V$, $5 - 3 \geq 1$, $V_o = 3V$

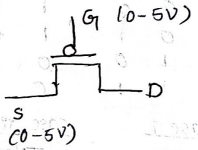
3) $V_S = 4V$, $V_o = 4V$

4) $V_S = 5V$, $V_o = 4V$ (weak logic 1 at o/p)



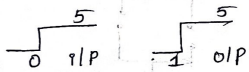
⇒ nmos passes weak logic 1.

⇒ when switch is on the voltage at i/p (source) will be passed to drain terminal is called pass transistor logic.



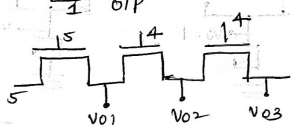
⇒ $V_G = 0V$, $V_{th} = -1$ $V_{sg} \geq |V_t|$

1) $V_S = 5$
$5 - 0 > 1$ $V_o = 5$



⇒ pmos passes weak logic '0'.

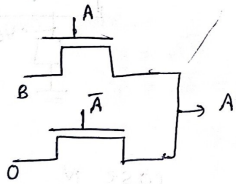
⇒ Find o/p



$V_{o1} = 4$
$V_{o2} = 3$
$V_{o3} = 3$

⇒ AND gate

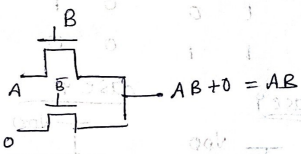
By taking A as control pin :-



$AB + 0 = AB$

A	B	y
0	0	0
0	1	0
1	0	0
1	1	1

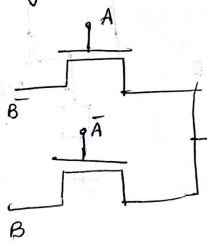
By taking B as control pin :-



$AB + 0 = AB$

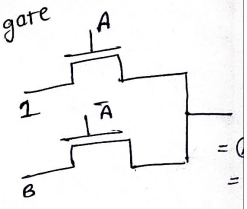
A	B	y
0	0	0
0	1	1
1	0	1
1	1	0

⇒ XOR gate :-

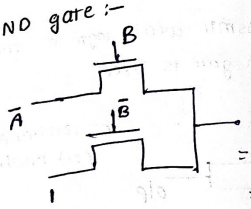


$A\bar{B} + \bar{A}B$

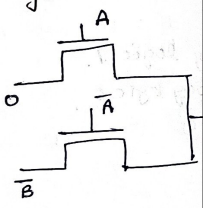
⇒ OR gate



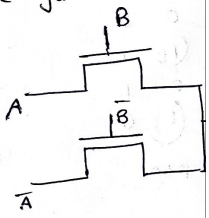
⇒ NAND gate :-



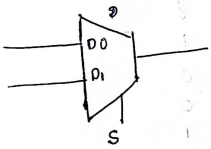
⇒ NOR gate :-



⇒ XNOR gate :-

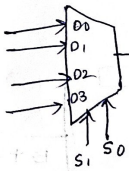


2x1 MUX with PTL :-



$y = \bar{S}D_0$

4x1 MUX with PTL :-



$y =$

$y = \bar{S_0}\bar{S_1}D_0 + \bar{S_0}S_1D_1 + S$

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G

D

VT, Vrn)

4V

at o/p
srde

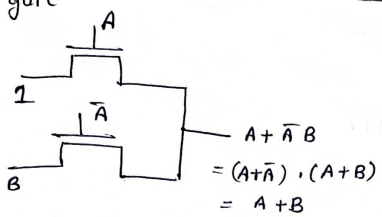
weak logic 1,
be passed

(0-5V)

D

D = AB

⇒ OR gate



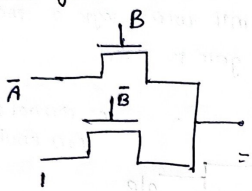
$A + \bar{A}B$

$= (A+\bar{A}) \cdot (A+B)$

$= A + B$

A	B	y
0	0	0
0	1	1
1	0	1
1	1	1

⇒ NAND gate :-



$\bar{A}B + \bar{B}$

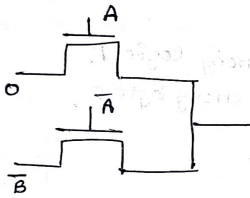
$= (\bar{A}+\bar{B}) \cdot (B+\bar{B})$

$= \bar{A}+\bar{B} = \overline{AB}$

A	B	y
0	0	1
0	1	1
1	0	1
1	1	0

$\bar{A} \cdot B$ A

⇒ NOR gate :-

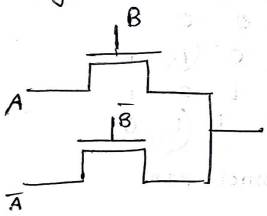


$\bar{A} \cdot \bar{B} = \overline{A+B}$

$\bar{A}+B$

A	B	y
0	0	1
0	1	0
1	0	0
1	1	0

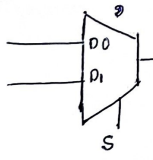
⇒ XNOR gate :-



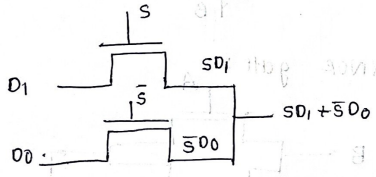
$AB + \bar{A}\bar{B}$

A	B	y
0	0	1
0	1	0
1	0	0
1	1	1

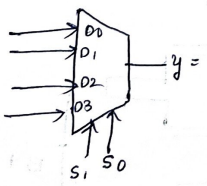
2x1 MUX with PTL :-

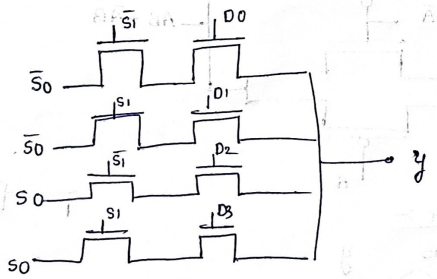


$y = \bar{S}D_0 + SD_1$



4x1 MUX with PTL :-

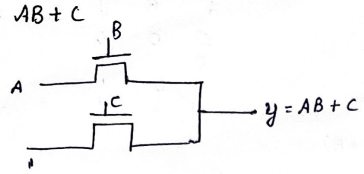




$y = \bar{S_0}\bar{S_1}D_0 + \bar{S_0}S_1D_1 + S_0\bar{S_1}D_2 + S_0S_1D_3$

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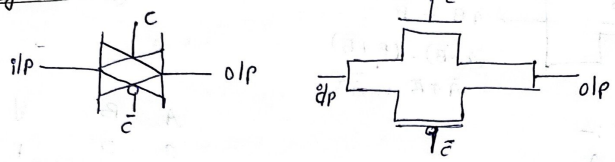
④ $y = AB + C$



Transmission Gate :—

* It is combination of pmos and nmos.
* pmos transmit weak logic 1 and pmos transmit weak logic 0 inorder to overcome this disadvantage transmission gate is used.

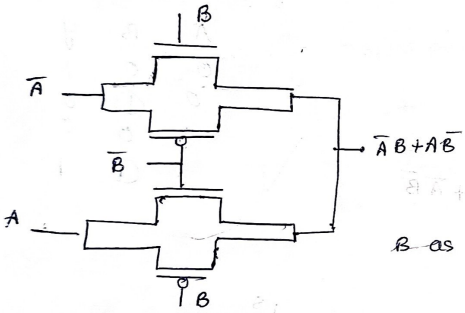
Symbol :—



C = control pin (or) enable pin

* If C = 1 both nmos and pmos will be ON
  - ⇒ If i/p = 1, pmos is going to transmit strong logic 1.
  - ⇒ If i/p = 0, nmos is going to transmit strong logic 0.

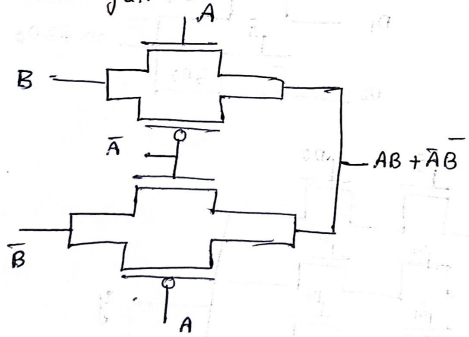
① XOR gate :—



A	B	y
0	0	0
0	(1)	1
1	0	1
1	(1)	0

B as control pin

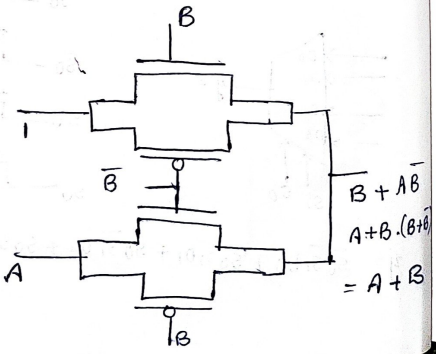
② XNOR gate :—



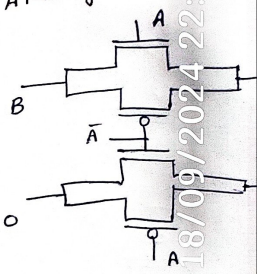
A	B	y
0	0	1
0	1	0
1	0	0
1	1	1

③ OR gate :—

A	B	y
0	(0)	0
0	(1)	1
1	(0)	1
1	(1)	1



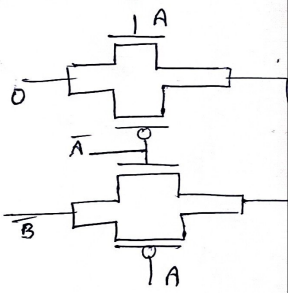
④ AND gate :—



⑤ NAND gate :—

A	B	y
0	0	1
0	(1)	1
1	0	1
1	(1)	0

⑥ NOR gate :—



cmos power consumpt

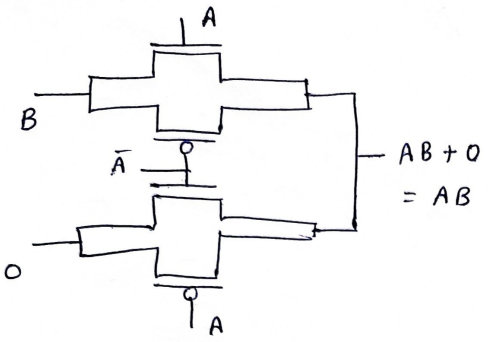
Static power :— mosfet
mosfet will co

Dynamic power : mosfet is

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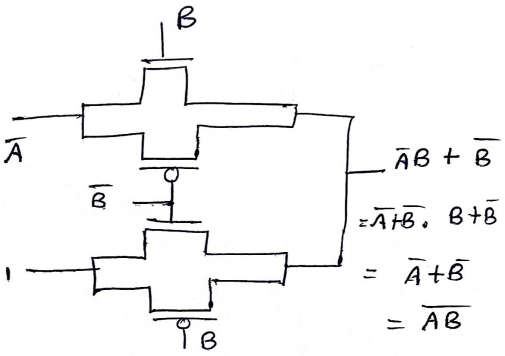
④ AND gate :-



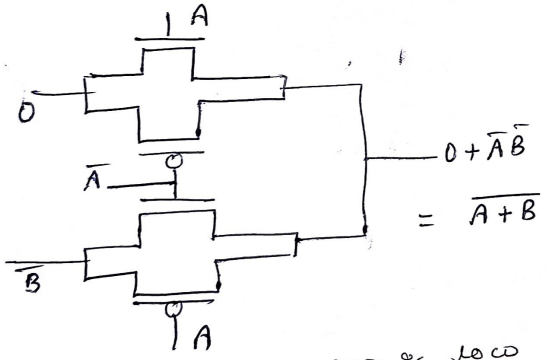
A	B	y
0	0	0
0	1	0
(1)	0	0
(1)	1	1

⑤ NAND gate :-

A	B	y
0	0	1
0	(1)	1
1	0	1
1	(1)	0



⑥ NOR gate :-



A	B	y
0	0	1
0	1	0
(1)	0	0
(1)	1	0

nmos & pmos → will be considered → to pmos

power consumption is more

cmos & power consumption is less

Static power :- mosfet is not working, leakage current will be there

mosfet will consumed power called

Dynamic power : mosfet is working