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6. BJT - Differential Amplifiers And Current mirrors

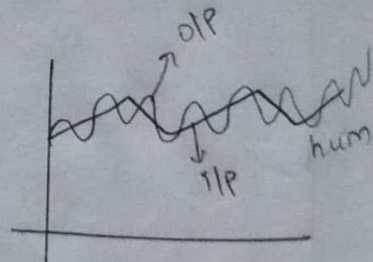
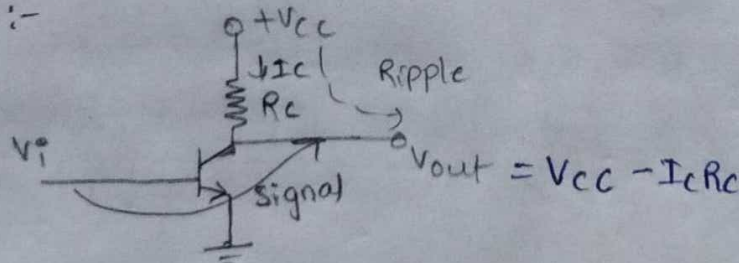
* Topics:-

- ⇒ Design of various configuration BJT (CE, CB and CC) amplifiers using current mirrors.
- ⇒ Design of a differential amplifier with BJT using active load, using current mirrors.
- ⇒ Design of single stage and two stage opamp.

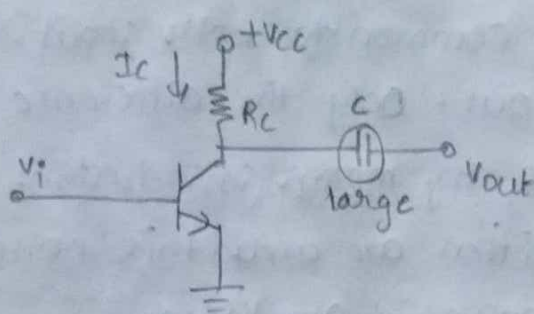
* Introduction:-

- ⇒ Differential Amplifiers is an advanced amplifier and is available in the form of "IC"
- ⇒ Integrated circuits = All the ~~silicon chips~~ ^{of discrete values} are integrated in the form of single chip [silicon chip]. which is more economical and convenient to use.
- ⇒ For the desired performance, few resistors, capacitors are required. But they have a complete circuit on the chip.
- * ⇒ In ICs, large value capacitors are difficult to fabricate. Because it requires more spaces. E.g. capacitors having higher than 10pF like C_c, C_B, C_E [in μF range]. They are completely avoided.

⇒ CE:-



- ⇒ Due to supply voltage some ripples will present.
- ⇒ Input signal coming from input
- ⇒ To suppress the hum in the CE, higher capacitor is connected at the output terminal.



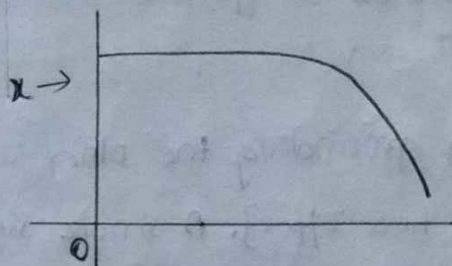
⇒ This output is independent on V_{CC} . Because of higher capacitor (C_C).

⇒ To fabricate large capacitor, it requires more area (on more silicon space is required in IC).

* ⇒ To make the output voltage (V_{out}) is independent on V_{CC} without using capacitor. Then we go for Differential Amplifier.

Conventional Amplifier to go for → Differential Amplifier

⇒ Differential Amplifier is a direct coupled Amplifier without any capacitor.



⇒ Frequency response is different. Hence This Amplifier works at low frequencies.

⇒ They will work uniformly from several Hz to few KHz.

⇒ So, there is no restrictions at low frequencies. Because the dc signal also amplified at direct coupled Amplifier.

* Differential Amplifier:- (D.A)

⇒ These are composite Amplifiers. [means mixed (or) two circuits are connected together].

⇒ In Differential Amplifier, we are using two inputs. means Two signals at the two different inputs can applied simultaneously.

⇒ It is also called "Difference Amplifier".

⇒ Most of the ~~types~~ times, it is called differential Amplifier

** because when we apply two signals, the difference of the two signals is Amplified. The amplified signal is available at the output. It is function of "D.A".

→ Any signal which is common to both inputs that will be automatically filtered out. Only the difference is Amplified.

Eg:- 1) Noise → generated by motors in industrial Areas.

→ If conventional amplifiers are used, this noise signal is picked ~~but~~ up, The noise is Amplified.

→ If p is voice. Along with voice, the noise is also amplified.

→ So, extra precautions are taken to prevent the noise.

Advantage of D.A. → But if Differential Amplifiers are used, the noise will automatically rejected because D.A will amplifies only the difference of two Inputs which is common to both inputs will be rejected.

This is the basics of Differential Amplifier.

* Features of Differential Amplifier:-

1) Difference of two Signals can be Amplified.

i.e., $V_{i1} - V_{i2}$

2) Single signal Amplifier :- by grounding the other input signal source [Because D.A has two I/p s]. A single signal Amplifier is formed [or it can be used Single signal Amplifier].

3) Direct Coupled:- used to amplifier very low frequency signal [including 0Hz] means dc signal is also amplified.

$\omega = 0$, $DC \rightarrow 0Hz$.

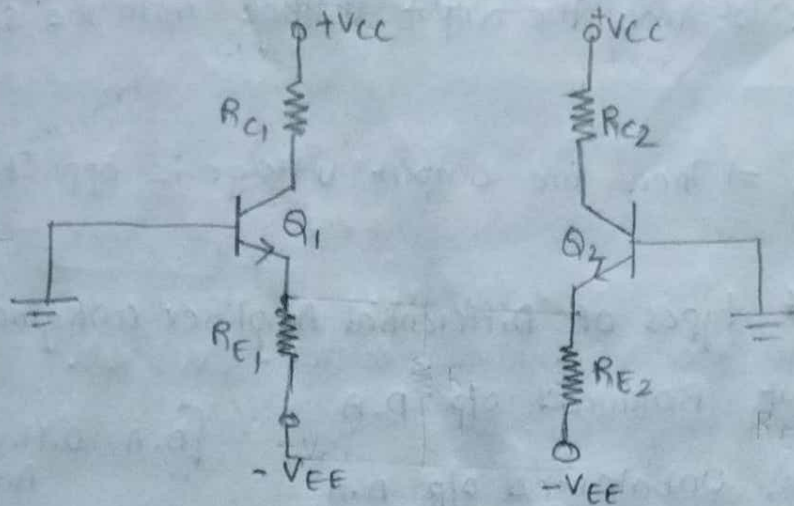
4) The operational amplifiers are widely used nowadays. The Differential Amplifier is the first stage of Operational Amplifier [op-Amplifier].

5) The Input impedance of Differential Amplifier is very high

* How to develop Differential Amplifier:-

let us consider two Emitter biased circuits. [It requires dual supply].

→ two transistors (Q_1, Q_2) have identical characteristics.



- ⇒ $RE_1 = RE_2$ and $RC_1 = RC_2$
- ⇒ The magnitude of $+V_{CC}$ = magnitude of $-V_{EE}$.
- Eg:- If $+V_{CC} = 12V$ then $V_{EE} = -12V$

* ⇒ The voltages are measured with respect to ground only.

⇒ TO make Differential Amplifier:-

- 1) ⇒ The two emitter biased circuits are connected together.
- 2) ⇒ The supply voltages are made common.
- 3) ⇒ Two RE resistor are connected together

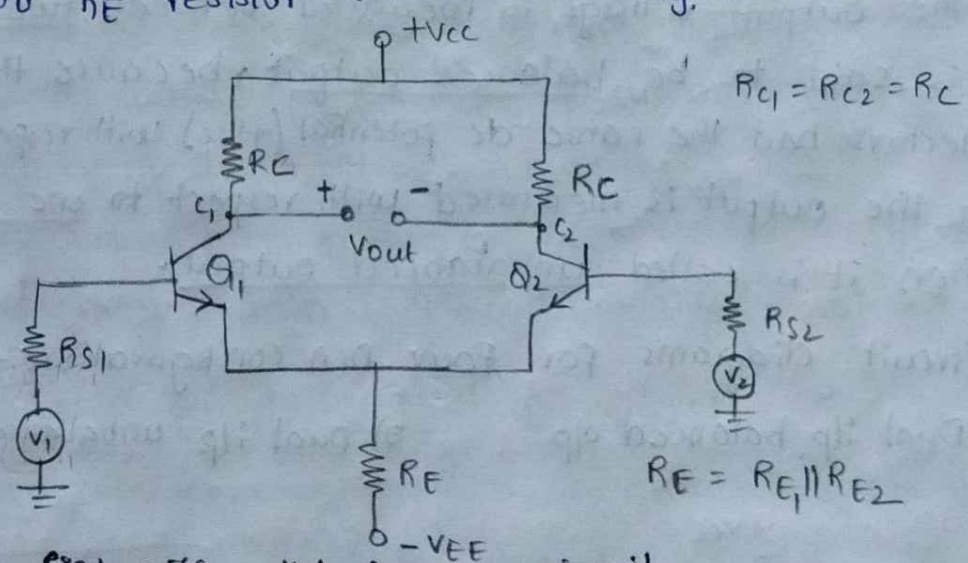


Fig:- Differential Amplifier circuit

- 4) ⇒ Two Inputs signals (V_1, V_2) at the base of Q_1 and at the base of Q_2
 - 5) ⇒ The Output is taken between two collectors
- ⇒ Ideally $V_{out} = 0$, when two inputs are equal

i.e., $V_0 = A(V_1 - V_2)$

$V_0 = A(V - V)$

∴ $V_0 = 0$

⇒ when $V_1 > V_2$ ⇒ Then the output voltage with the same polarity.

⇒ when $V_1 < V_2$ ⇒ Then the output voltage is opposite polarity.

⇒ There are 4 types of Differential Amplifier configurations:-

1) Dual input Balanced o/p D.A

2) Dual i/p Unbalanced o/p D.A

3) single i/p balanced o/p D.A

4) single i/p unbalanced o/p D.A

[D.A = Differential Amplifier]

⇒ These four configurations defined by

* No. of i/p signals are used

explanation

* The way of o/p is measured. [if we are using two input signals, The configuration is said to be dual input. Otherwise single input].

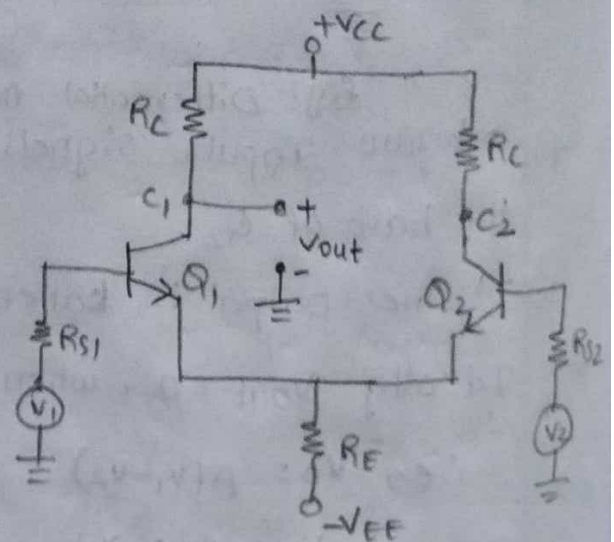
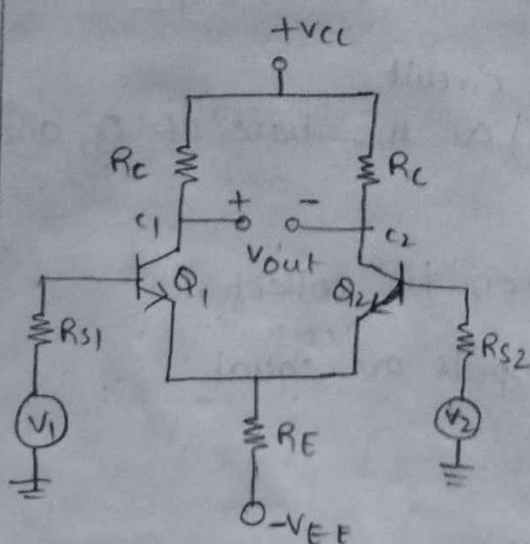
explanation

* The Output voltage is measured between two collectors. it is said to be balanced output, because the both collectors had the same dc potential ($+V_{CC}$) with respect to ground. If the output is measured with respect to one collector then it is called unbalanced output.

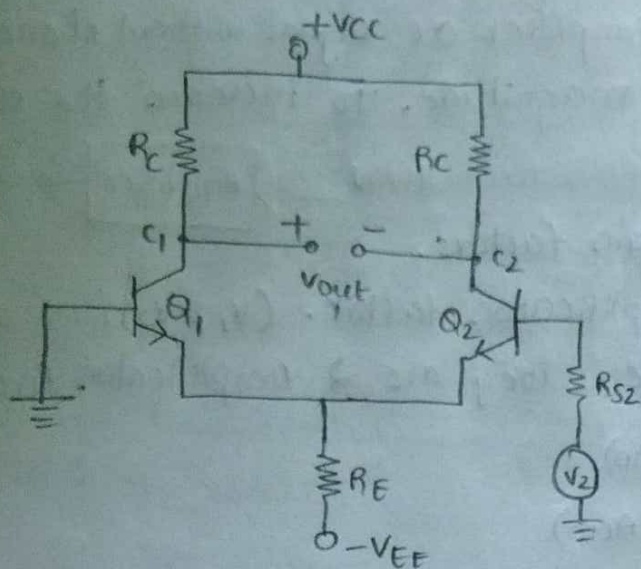
* Circuit diagrams for four D.A configurations:-

1) Dual i/p balanced o/p

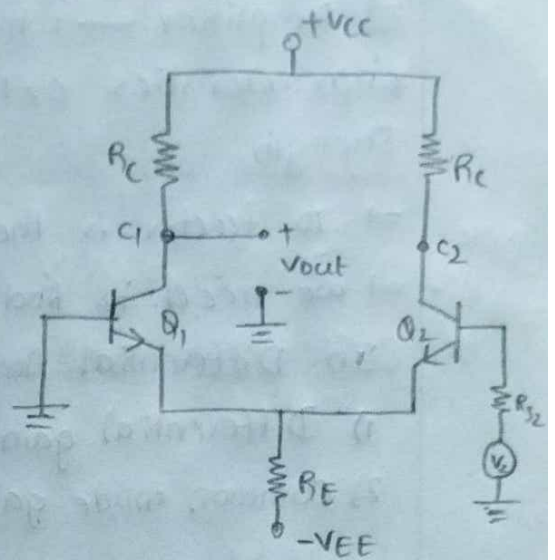
2) Dual i/p unbalanced o/p



3) Single i/p balanced o/p



4) Single i/p unbalanced o/p



* Conclusion:-

- ⇒ The differential Amplifier is also called as multi-stage Amplifier. Because it provides high gain. using successive stages of D.A.
- Multi-stage Amplifier:- no. of amplifiers are connected in cascade.
- purpose:- to increase the gain.
- ⇒ The advantage of direct coupled, It removes the lower cutoff frequencies imposed by the coupling capacitor (C_c). They are capable of Amplifying dc as well as Ac i/p signal.
- ⇒ There is no need of C_c capacitor
- ⇒ It is capable of amplifying difference of two i/p signals and the common in both will be automatically rejected.

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Analysis Of Differential Amplifiers:-

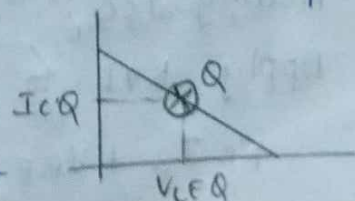
⇒ If we consider any Amplifiers, there are 2 ways of Analysis:

- 1) DC Analysis
- 2) AC Analysis.

1) DC Analysis:-

⇒ In DC Analysis, the parameter used to find is operating point, (V_{CEQ}, I_{CQ}).

where I_{CQ} = collector current at the operating point



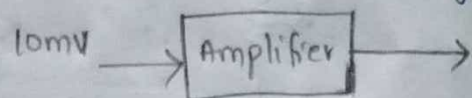
V_{CEQ} = drop across the resistor b/w two collectors

⇒ we use the value of R_C (or) R_E .

⇒ It is applicable for "All type of D.A".

2) AC Analysis:-

⇒ Amplifier — which Amplifies ac signal without changing its characteristics except magnitude. to increase the signal strength



⇒ To factor is the gain factors.

⇒ we need to find Amplification factor. (V_1 & V_2).

In Differential Amplifiers, They are 2 Amplification factors

1) Differential gain (A_D)

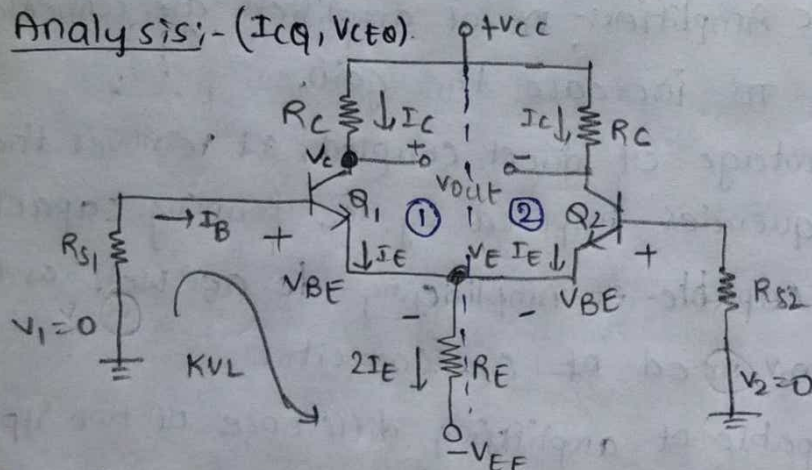
2) Common mode gain (A_{cm}).

$$V_o = A_D V_d + A_{cm} V_c$$

⇒ V_1 and V_2 [two inputs] are not identical.

* Dual input, Balanced output Differential Amplifier:-

⇒ DC Analysis:- (I_{CQ}, V_{CEQ}).



⇒ for dc analysis, ac sources V_1 & V_2 is connected to ground [$V_1=0, V_2=0$].

⇒ R_{S1}, R_{S2} — internal resistance of input signal

⇒ ① and ② are symmetrical because both transistors are identical.

⇒ Operating point (I_{CQ}, V_{CEQ}) can be found for 1 transistor (Q1).

Finding I_{CQ} :-

Apply KVL to the base to emitter loop 'Q1':-

$$R_S I_B + V_{BE} + 2 I_E R_E - V_{EE} = 0$$

$$R_S I_B + 2 I_E R_E = V_{EE} - V_{BE}$$

$$R_S \frac{I_C}{\beta} + 2 I_C R_E = V_{EE} - V_{BE}$$

$$\begin{cases} I_C = \beta I_B \\ \Rightarrow I_B = \frac{I_C}{\beta} \\ I_C \approx I_E \end{cases}$$

$$I_C \left[\frac{R_S}{\beta} + 2R_E \right] = V_{EE} - V_{BE}$$

$$\Rightarrow I_C = I_E = \frac{V_{EE} - V_{BE}}{2R_E + R_S/\beta}$$

$V_{BE} = 0.6 \text{ V}$ for Si and 0.2 V for Ge and

$\frac{R_S}{\beta} \ll 2R_E$ [internal resistance is very low (it is in series)]

$$\therefore I_E = I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E} \rightarrow (1)$$

Finding V_{CEQ} :-

$$V_{CE} = V_C - V_E$$

Apply KVL to loop,

$$0 + V_{BE} + V_E = 0$$

$$\therefore V_E \cong -V_{BE}$$

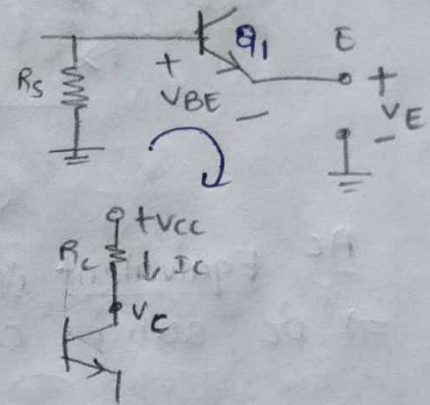
$$V_C = V_{CC} - I_C R_C$$

$$\therefore V_{CEQ} = V_C - V_E$$

$$= V_{CC} - I_C R_C - (-V_{BE})$$

$$\therefore V_{CEQ} = V_{CC} + V_{BE} - I_C R_C \rightarrow (2)$$

$Q(V_{CEQ}, I_{CQ})$ = Operating point of D.A.



Eg:- Let $R_C = 2.2 \text{ k}\Omega$, $R_E = 4.7 \text{ k}\Omega$, $R_{in1} = R_{in2} = 50 \Omega$, $+V_{CC} = 10 \text{ V}$, $-V_{EE} = -10 \text{ V}$, $\beta = 100$, $V_{BE} = 0.7 \text{ V}$ are the specification for Dual 'lp and balanced o/p D.A. Determine the operating point of two transistors.

Sol:-

$$1) I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E + \frac{R_S}{\beta}} = \frac{10 - 0.7}{2(4.7 \times 10^3) + \frac{50}{100}} = \frac{9.3}{9400.5}$$

$$\therefore I_{CQ} = 0.9893 \text{ mA}$$

$$2) V_{CEQ} = V_{CC} + V_{BE} - I_C R_C$$

$$= 10 + 0.7 - (0.9893 \times 10^{-3})(2.27 \times 10^3)$$

$$\therefore V_{CEQ} = 8.454 \text{ V}$$

* CMRR - common mode Rejection Ratio.

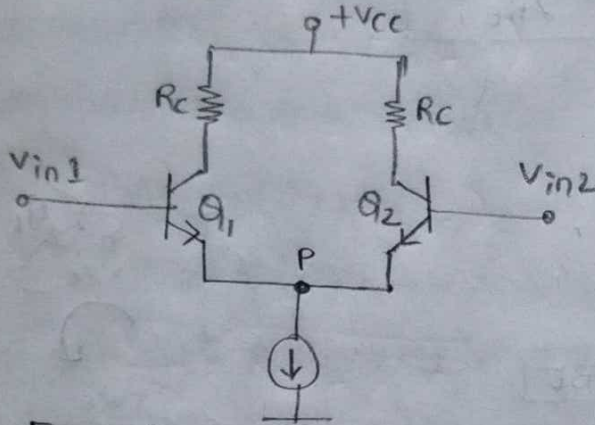
⇒ we know that the analysis of CE, CC and CB, we used h-parameter model.

⇒ we use analysis for Differential Analysis using π -model.

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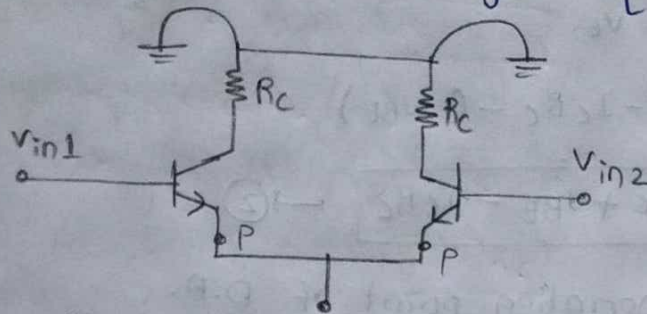
Small Signal Analysis Of D.A:-

* Differential Amplifier Circuit:-

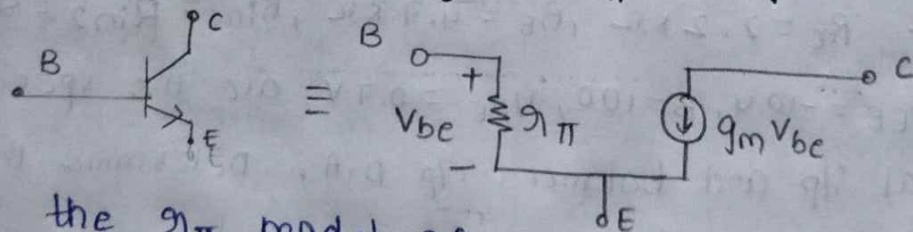


Ac Equivalent circuit:-

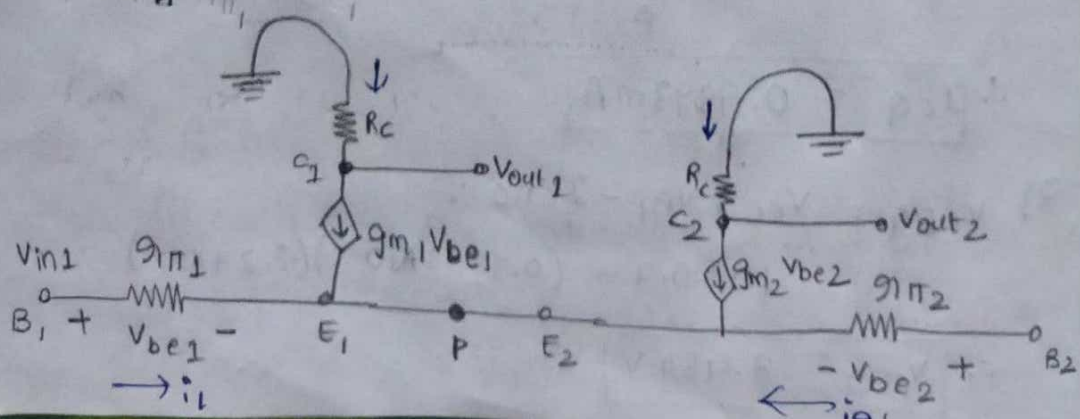
⇒ DC sources connected to ground [$V_{cc} = S.c$ & $I = O.c$].



Now replacing transistor by its π -model



we get the π model of D.A Amplifier



* Parameters:-

1. differential gain (A_d):
Applying KCL at node 'p',

In A_d , I_{E1} and $-I_{E2}$ are equal. Hence R_E is not considered.

$$i_1 + i_2 + g_{m1}V_{be1} + g_{m2}V_{be2} = 0$$

$$\left[\because i_1 = \frac{V_{be1}}{r_{\pi1}} \right]$$

$$\frac{V_{be1}}{r_{\pi1}} + \frac{V_{be2}}{r_{\pi2}} + g_{m1}V_{be1} + g_{m2}V_{be2} = 0$$

$$\left[i_2 = \frac{V_{be2}}{r_{\pi2}} \right]$$

let us take $r_{\pi1} = r_{\pi2} = r_{\pi}$ and

$$g_{m1} = g_{m2} = g_m$$

let $V_{in1} = -V_{in2}$ [$\because V_{in1}$ & V_{in2} are 180° out of phase].
 $\Rightarrow$ from the circuit $V_{in1} = V_{be1}$ &
 $V_{in2} = -V_{be2}$

$$V_{out1} = -g_{m1}V_{be1}R_C = -g_m R_C V_{in1}$$

$$V_{out2} = -g_{m2}V_{be2}R_C = -g_m R_C V_{in2}$$

Output voltage $V_o = V_{out1} - V_{out2}$ [Between two collectors o/p].

$$A_d = \frac{V_{out1} - V_{out2}}{V_{in1} - V_{in2}} = \frac{-g_m R_C V_{in1} - (-g_m R_C V_{in2})}{V_{in1} - V_{in2}}$$

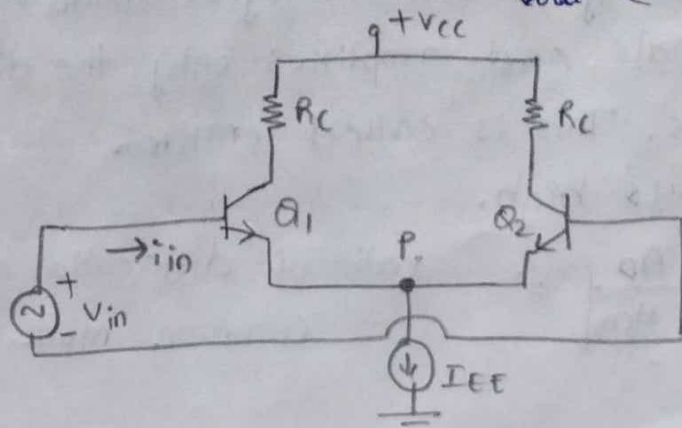
$$= \frac{-g_m R_C [V_{in1} - V_{in2}]}{(V_{in1} - V_{in2})} = -g_m R_C$$

$\therefore$ Differential ^{voltage} gain (A_d) = $-g_m R_C$ [$-ve$ indicates 180° phase difference b/w i/p & o/p]

It is the differential voltage gain for Balanced o/p.

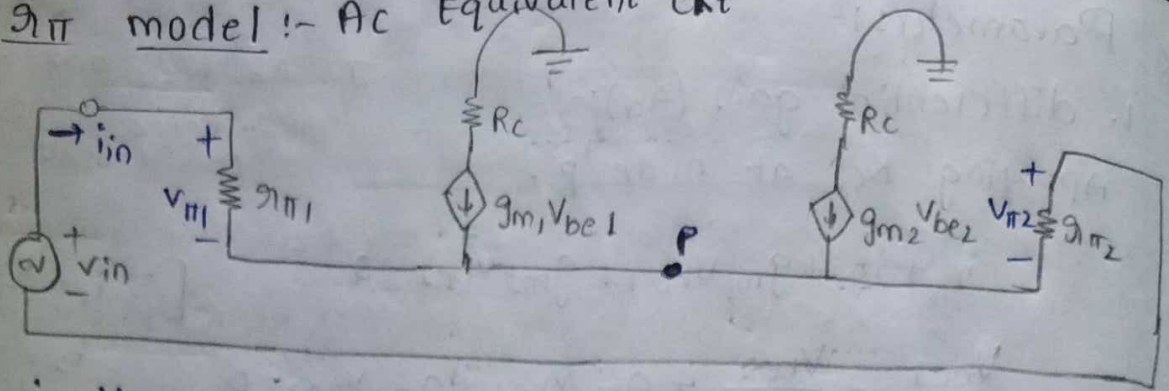
$\Rightarrow$ for unbalanced o/p, $A_d = \frac{-g_m R_C}{2}$

2) Input Resistance (R_i):- $\frac{V_{in}}{I_{in}}$ ($R_i = \frac{V_{in}}{I_{in}}$)



R_E requires more space
Hence we use current Source.

π model :- Ac Equivalent ckt



$$\therefore V_{in} = V_{\pi 1} - V_{\pi 2}$$

$$= g_{\pi 1} i_{in} - (-g_{\pi 2} i_{in})$$

$$= g_{\pi 1} i_{in} + g_{\pi 2} i_{in}$$

$$V_{in} = i_{in} (g_{\pi 1} + g_{\pi 2})$$

$$\Rightarrow V_{in} = i_{in} (2g_{\pi})$$

$$\text{let } g_{\pi 1} + g_{\pi 2} = g_{\pi}$$

$$\Rightarrow \boxed{\frac{V_{in}}{i_{in}} = R_{in} = 2g_{\pi}}$$

For dual input D.A $\boxed{R_i = 2g_{\pi}}$

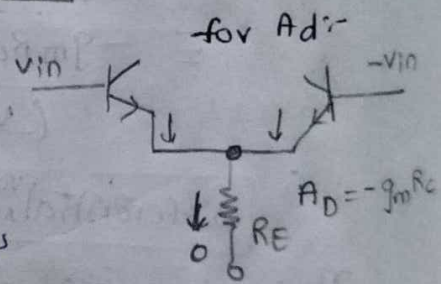
for single i/p D.A $\boxed{R_i = g_{\pi}}$

where, $g_{\pi} = h_{ie}$

3) Output Resistance (R_o)

for balanced o/p & dual i/p $\boxed{R_o = 2R_C}$

for single i/p D.A $\boxed{R_o = R_C}$



* Note:-

for CE

$$A_v = \frac{-h_{fe} R_L}{h_{ie}}$$

without bypass

$$A_v = \frac{-h_{fe} R_L}{h_{ie} + (1 + h_{fe}) R_E}$$

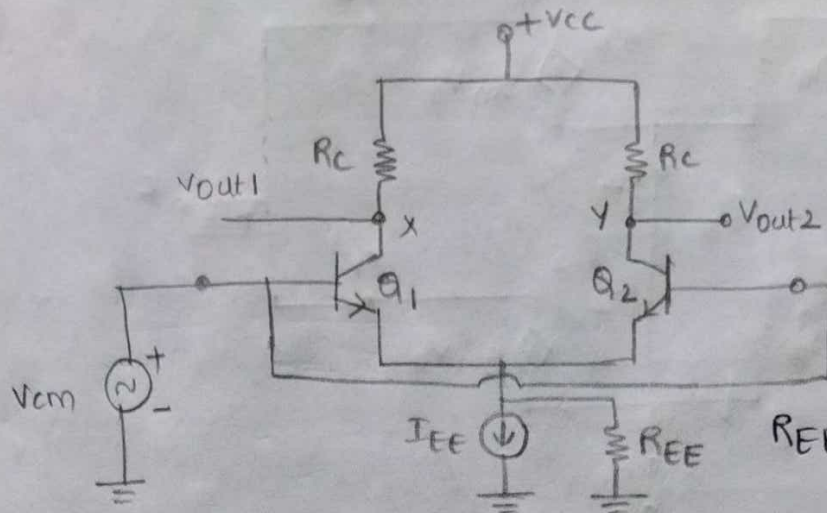
4) CMRR:- common mode Rejection Ratio.

$\Rightarrow$ It is the ability of D.A to reject ^{common} mode signal for both input signals and amplifies only the difference b/w two signals. This is called "CMRR".

$\Rightarrow$ It is always high.

$$CMRR = \left| \frac{A_D}{A_{cm}} \right| = \text{ratio of differential gain to the common mode gain.}$$

Now applying a common signal to both the input terminals



Both inputs are in-phase.

$$\downarrow I_{E1} + I_{E2} \downarrow$$

⇒ Hence current flows through R_{EE} .

R_{EE} : Output impedance of I_{EE} .

Ideally, $V_{out} = 0$ [Both inputs are same].

But practically, some finite value is given. If any changes are given, the system will respond.

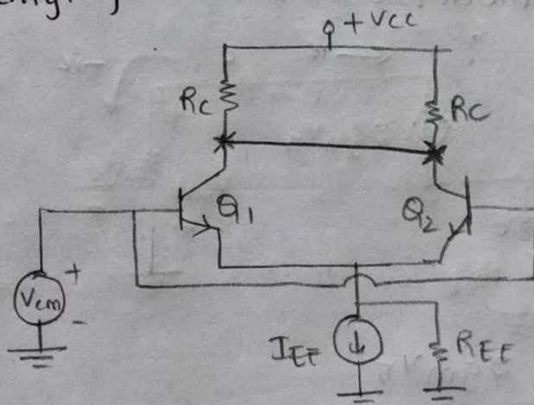
∴ point 'x' & 'y' are having equal potential [Ideally].

modifying the circuit

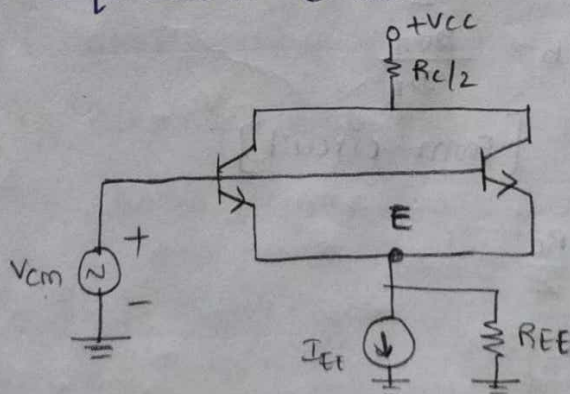
$$V_{out} = V_{out1} - V_{out2} = 0$$

$$[\because V_{out1} = V_{out2}]$$

Ideal case



The equivalent circuit

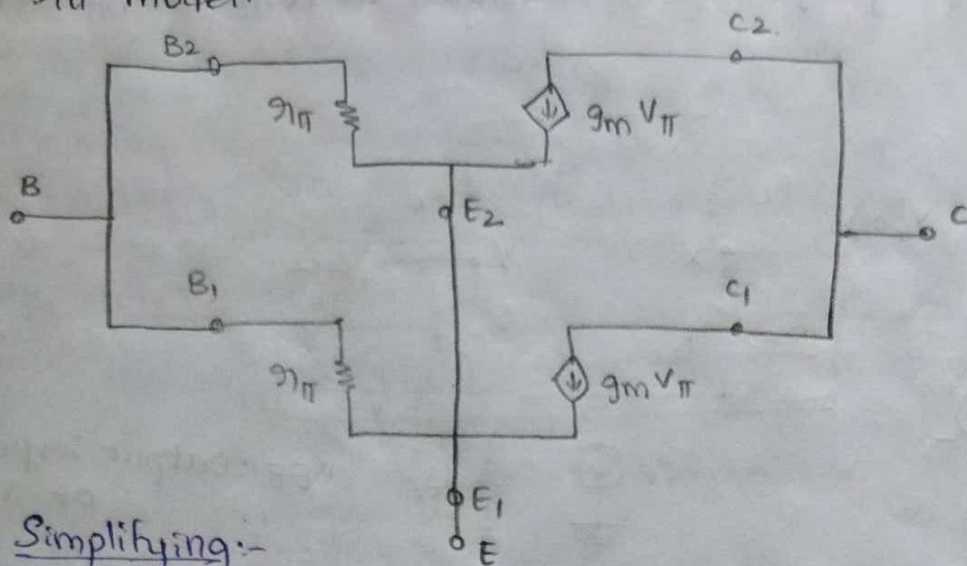


$$R_c \parallel R_c$$

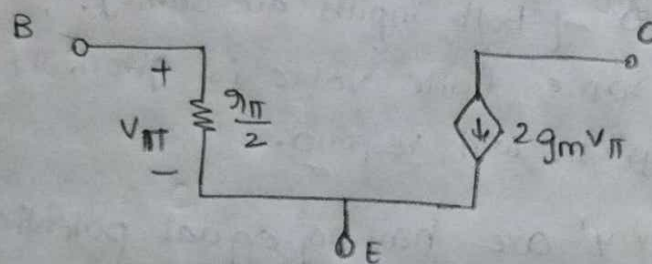
$$= \frac{R_c \times R_c}{2R_c} = \frac{R_c}{2}$$

The π model

π model:-



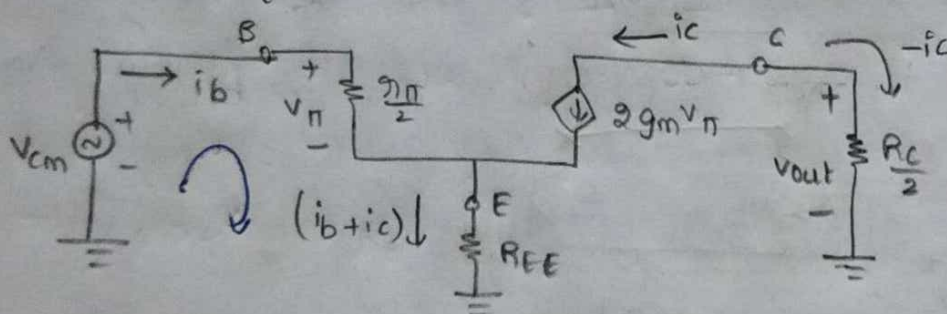
Simplifying:-



$$r_{\pi} || r_{\pi} = \frac{r_{\pi} \times r_{\pi}}{2r_{\pi}} = \frac{r_{\pi}}{2}$$

$$g_m V_{\pi} + g_m V_{\pi} = 2g_m V_{\pi}$$

Final Equivalent model circuit:-



We know $i_c = 2g_m V_{\pi}$

$$V_{\pi} = i_b \times \frac{r_{\pi}}{2}$$

$$\Rightarrow i_b = \frac{2V_{\pi}}{r_{\pi}}$$

Here $V_{out} = -i_c \frac{R_C}{2}$ [from circuit]

$$= -2g_m V_{\pi} \frac{R_C}{2}$$

$$\therefore V_{out} = -g_m R_C V_{\pi}$$

But $A_{cm} = \frac{V_{out}}{V_{cm}} \rightarrow \text{①}$

Apply KVL to loop

$$-V_{cm} + i_b \frac{r_{\pi}}{2} + (i_c + i_b) R_{EE} = 0$$

$$\Rightarrow V_{cm} = i_b \frac{r_{\pi}}{2} + (i_c + i_b) R_{EE}$$

$$\Rightarrow V_{cm} = i_b \left(\frac{r_{\pi}}{2} + R_{EE} \right) + i_c R_{EE}$$

$$\text{But } i_b = \frac{2V_{\pi}}{r_{\pi}}$$

$$= \frac{2V_{\pi}}{r_{\pi}} \left(\frac{r_{\pi}}{2} + R_{EE} \right) + 2g_m V_{\pi} R_{EE}$$

$$i_c = 2g_m V_{\pi}$$

$$= V_{\pi} \left[1 + \frac{2R_{EE}}{r_{\pi}} + 2g_m R_{EE} \right]$$

$$= V_{\pi} \left[1 + 2R_{EE} \left(\frac{1}{r_{\pi}} + g_m \right) \right]$$

$$\frac{1}{r_{\pi}} \ll g_m$$

Here $\frac{1}{r_{\pi}}$ is neglected.

$$\therefore V_{cm} = V_{\pi} [1 + 2g_m R_{EE}]$$

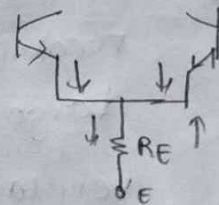
5) common mode gain (A_{cm}):-

$$A_{cm} = \frac{V_{out}}{V_{cm}}$$

$$= \frac{-g_m R_c V_{\pi}}{V_{\pi} (1 + 2g_m R_{EE})}$$

$$[R_{EE} = R_E]$$

$$\therefore A_{cm} = \frac{-g_m R_c}{1 + 2g_m R_E}$$



4) CMRR:-

$$CMRR = \frac{A_d}{A_{cm}} = \frac{-g_m R_c}{\frac{-g_m R_c}{1 + 2g_m R_{EE}}} = (1 + 2g_m R_{EE})$$

[Ideally $CMRR = \infty$].

$$\therefore CMRR = 1 + 2g_m R_{EE} \approx 2g_m R_{EE}$$

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To improve CMRR, If $R_E \uparrow$ ses $\rightarrow$ drop across $R_E \uparrow$ ses. Then

$I_{CQ} \downarrow$ ses $\rightarrow$ gain (A_d) is reduced.

$$\text{We know } CMRR = \frac{A_d}{A_{cm}}$$

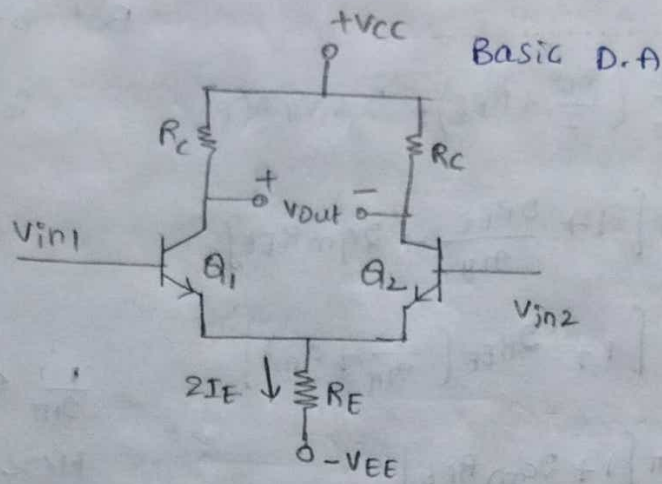
$\Rightarrow R_E \uparrow$ ses $\rightarrow$ CMRR $\downarrow$ ses

* Circuit for Improving CMRR:-

To increase CMRR, we have 4 ways:-

1. constant current Bias
2. current mirror circuit
3. wilson current source
4. widlar current source

1. Constant Current Bias: [used Even R_E is, I_{CQ} should be constant]



Note:-

$\Rightarrow R_E$ cannot be very high.
If R_E very high Then I_{CQ} ↓ ses.

$\Rightarrow$ In the R_E is replaced by constant current source (I_{EE}).
Because R_E is replaced by transistor and a constant current source is fabricated due to transistor.

$\Rightarrow$ Because "IC" are designed using transistors [many no. of transistor].

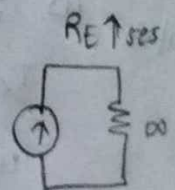
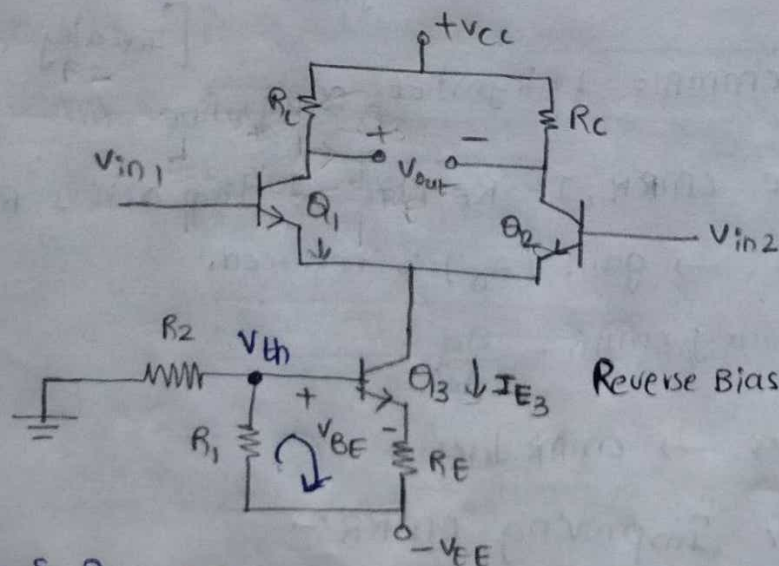
Eg:- Small scale IC — 10-100 transistors in single chip

medium scale IC — 100-1000 transistors " "

large scale IC — 1000-10,000 transistors " "

very large scale IC [VLSI] — millions of transistors in a single chip.

$\Rightarrow$ replacing R_E with constant current source [Bias]:-



R_1 & R_2 are used for voltage divider Bias

Thevenin's voltage $V_{th} = \frac{R_1}{R_1 + R_2} |V_{EE}|$

Applying KVL to the loop,

$$-V_{th} + V_{BE} + I_{E3} R_E = 0$$

$$\Rightarrow I_{E3} R_E = V_{th} - V_{BE}$$

$$I_{E3} = \frac{V_{th} - V_{BE}}{R_E} \rightarrow \textcircled{1}$$

Total current [or Tail current] = $2I_E = I_T$

$$\Rightarrow I_E = \frac{I_T}{2}$$

$$\Rightarrow I_{C1} = I_{C2} = \frac{I_T}{2}$$

$$I_T = \frac{1}{2} I_{E3}$$

For every $^{\circ}C$,

2.5 mV decreases

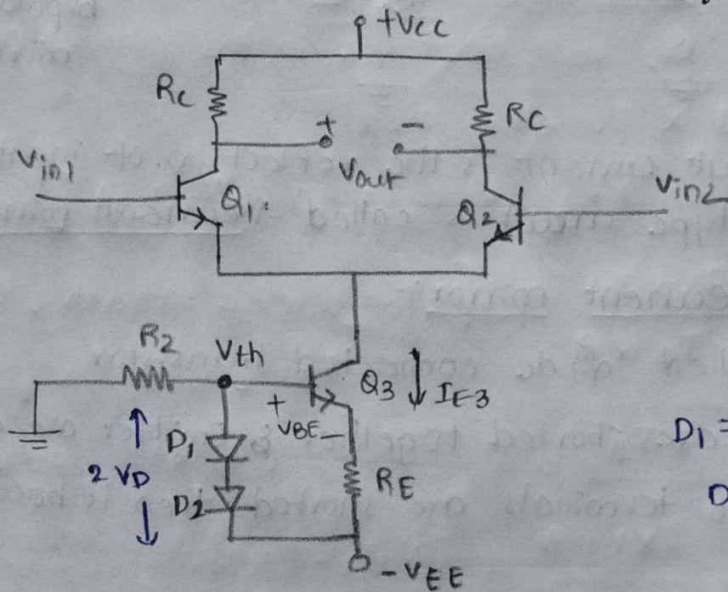
V_{BE} value

$\Rightarrow$ This variation changes I_{E3}

Drawback in ckt

$\Rightarrow$ If R_1 is replaced with two diodes, such type of circuit is called "diode compensation technique".

overcome the drawback



$$D_1 = 0.7V$$

$$D_2 = 0.7V$$

$$D_1 = D_2 = D$$

V_D = Voltage drop across one diode

The characteristic of emitter base junction of Q_3 and the same characteristics of diode is chosen.

So, any variation occurred will be compensated.

$$\textcircled{1} \Rightarrow I_{E3} = \frac{2V_D - V_{BE}}{R_E} \quad [V_D = V_{BE}]$$

$$I_{E3} = \frac{2V_D - V_D}{R_E}$$

$$\therefore \boxed{I_{E3} = \frac{V_D}{R_E}}$$

finding R_2 :

$$R_2 = \frac{V_{EE} - 2V_D}{I_E}$$

$$[V_D = 0.7]$$

$$\therefore \boxed{R_2 = \frac{V_{EE} - 1.4}{I_E}}$$

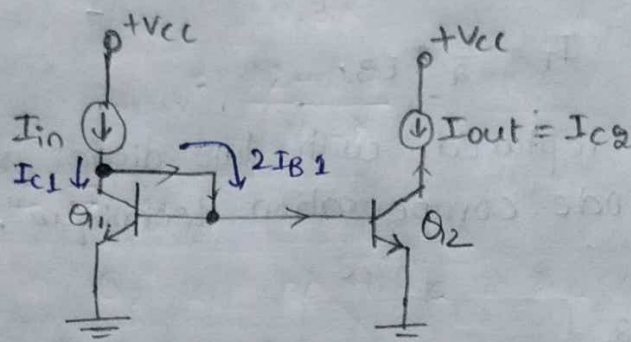
This is called Constant current Bias

2. Current mirror [~~constant~~]:- [mirror image]

⇒ The current mirror circuit producing an output current which is equal to an input current.

[The input given is same reflected at the o/p].

⇒ R_E is replaced with current mirror.



This is the
"bipolar current
mirror circuit".

⇒ The output current is the reflection of input current. Hence, this type circuit is called "current mirror".

Analysis of Current mirror:-

⇒ Q_1 is called diode connected transistor

[∵ The base are shorted together & emitter are grounded].

⇒ If any two terminals are shorted then it becomes one terminal.

Hence Q_1 contains only two terminals. so, it is called diode connected transistor.

From ckt ⇒ $V_{BE2} = V_{BE1}$ [because 2 bases are connected and 2 emitters are grounded.]

$$I_{B2} = I_{C1}$$

$$\Rightarrow I_{C2} = I_{C1} \rightarrow \textcircled{1}$$

Apply KCL at transistor Q_1 [at Q_1]:-

$$I_{in1} = I_{C1} + 2I_{B1}$$

$$= I_{C1} + 2 \frac{I_{C1}}{\beta}$$

$$I_{in1} = I_{C1} \left(1 + \frac{2}{\beta} \right)$$

$$\Rightarrow I_{C1} = \frac{I_{in1}}{\left(1 + \frac{2}{\beta} \right)} \rightarrow \textcircled{2}$$

$$\left[\because \text{In CE conf?}:- \right. \\ \left. I_C = \beta I_B \right]$$

Output current $I_{C2} = I_{out}$

$$\Rightarrow I_{C2} = I_{C1} = I_{out} = \frac{I_{in}}{(1 + \frac{2}{\beta})}$$

But $I_{C2} = I_{C1}$

$$\therefore I_{out} = \frac{I_{in}}{(1 + \frac{2}{\beta})}$$

β is very large,

$\Rightarrow \frac{1}{\beta}$ is very small.

Then $\frac{2}{\beta}$ is neglected.

$$\therefore I_{out} \approx I_{in}$$

[Hence I_{out} is the reflection of I_{in} current].

This is called current mirror.

→ Application of current mirror:-

→ This is current mirror is used as a load in IC [IC 741] Amplifiers. [Because it occupies less area].

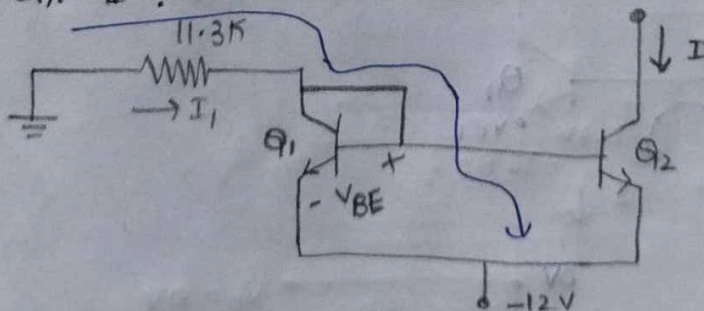
→ In order to increase voltage gain [$A_v = \frac{h_{fe} R_L}{h_{ie}}$], we are using current mirror. Because, In D. gain $A_d = -g_m R_c$. In place of R_c we use current mirror which provides output resistance, Hence voltage gain also increases.

→ To bias an differential amplifier, the current mirror has a load that is called "Active load".

Date
26/01/22

Problem 1:-

1. In the circuit shown, transistor have large β . Calculate current I ?



i) Transistors are identical

ii) Emitter Junction area of 'Q2' is twice to the Emitter Junction area of 'Q1'?

Sol:- i) As two transistors are identical and it is a current mirror circuit

→ We know that In current mirror, Output current reflect the input current.

$$\therefore I \approx I_1$$

Apply KVL to the loop,

$$0 + 11.3K(I_1) + 0 + V_{BE} - 12 = 0$$

$$11.3K I_1 = 12 - V_{BE}$$

$$\Rightarrow I_1 = \frac{12 - V_{BE}}{11.3K}$$

$$[\because V_{BE} = 0.7]$$

$$= \frac{12 - 0.7}{11.3K} = \frac{11.3}{11.3K}$$

$$\therefore \boxed{I \approx I_1 = 1mA}$$

ii) current in ' Q_2 ' will be twice in the current of ' Q_1 '.

$$\boxed{I \propto \text{Junction area}}$$

Because we know that $I = I_0(e^{V/V_T} - 1)$ [diode current eq.]

$$\therefore I \propto I_0$$

$$\Rightarrow I_0 \propto A$$

[I_0 = reverse saturation current]

$$I_0 = e A n_i^2 \left[\frac{1}{N_D} + \frac{1}{N_A} \right]$$

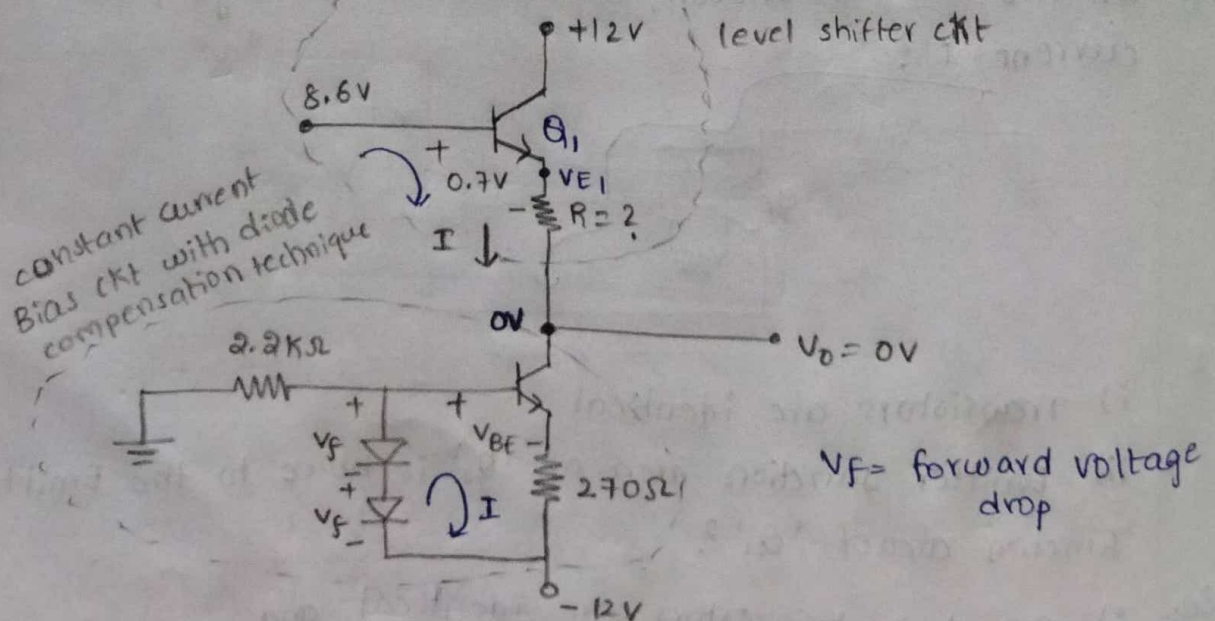
$$(I_0 \propto A) \quad A = \text{Junction Area}$$

$$\therefore \boxed{I = 2 I_1}$$

$$\Rightarrow I = 2 \times 1mA \quad [\because I_1 = 1mA]$$

$$\therefore \boxed{I = 2mA}$$

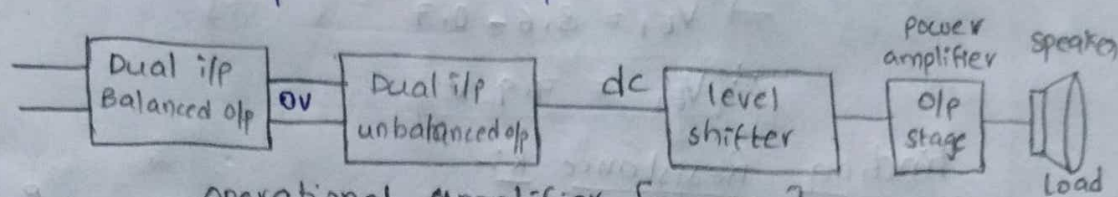
P2:- In the circuit shown, calculate the value of resistance R ? for $V_0 = 0V$.



Sol:- Assume the forward diode voltage drop,
 $V_D = V_{BE} = 0.7V$ and $\beta = \text{very large}$

The given is a constant current bias circuit with diode compensation technique

⇒ The given circuit is a level shifter circuit. It is used in internal circuit of operational amplifier.

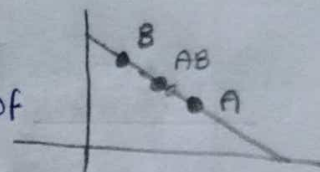


⇒ In ^{operational amplifier [op-Amp]} Output stage, we always connect to power amplifier.

⇒ The dc Component is directly given to output stage.

⇒ The power amplifier is basically classified based on location of operating point.

* If the operating point located in the middle of the load line — class A power Amplifier



* If the operating point is near to cutoff or near to saturation It is called — class B power Amplifier

* If the operating point is located b/w A and B. Then it is called — class AB power Amplifier.

⇒ If dc component connected to output stage, then the Output performance will change.

So, we need to shift the dc component to 0V.

For that purpose we are using "level shifter circuit".

⇒ The level shifter will completely removes the dc component and shifted to 0V. Then the level shifter is connected to Power amplifier [output stage].

⇒ Finding I:-

Apply KVL to the loop,

$$-V_f - V_f + V_{BE} + 270I = 0$$

$$[\because V_D = V_{BE} = 0.7]$$

$$\Rightarrow -0.7 - 0.7 + 0.7 + 270I = 0$$

$$\Rightarrow I = \frac{0.7}{270} = 2.59 \text{ mA}$$

$$\therefore \boxed{I = 2.59 \text{ mA}}$$

In the circuit, Base currents are negligible. So, the (I) current flows through Resistor R.

finding V_{E1} :-

Apply KVL at level shift circuit,

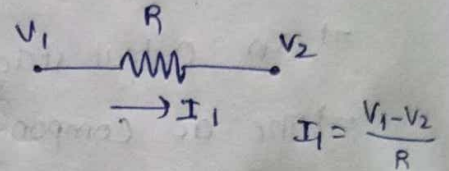
$$-8.6V + 0.7 + V_{E1} = 0$$

$$\Rightarrow V_{E1} = 8.6 - 0.7$$

$$\therefore \boxed{V_{E1} = 7.9V}$$

finding Resistance R :-

$$\text{current } I = \frac{V_1 - V_2}{R}$$



$$\Rightarrow I = \frac{V_{E1} - V_0}{R} = \frac{7.9 - 0}{R}$$

$$\Rightarrow I = \frac{7.9}{R} \quad \text{[But } I = 2.59 \text{ mA}]$$

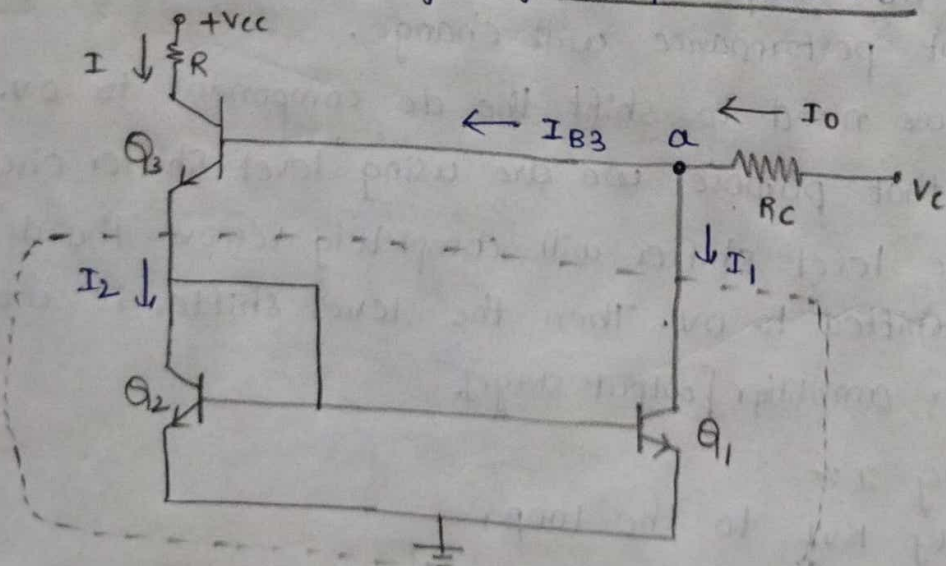
$$\Rightarrow R = \frac{7.9}{I} = \frac{7.9}{2.59 \times 10^{-3}}$$

$$\therefore \boxed{R = 3.05 \text{ K}\Omega}$$

3. Wilson Current Source:-

$\Rightarrow$ It provides output current equals to Input current.

$\Rightarrow$ It also exhibits very high output resistance.



$$\therefore \boxed{I = I_0}$$

$\Rightarrow$ By observing the ckt,

Transistors Q_1 and Q_2 forms a current mirror

$$\therefore I_{out} = \frac{I_{in}}{(1 + \frac{2}{\beta})}$$

But

$$\Rightarrow \boxed{I_1 = \frac{I_2}{(1 + \frac{2}{\beta})}} \quad \text{--- } \textcircled{1}$$

Apply KCL @ node 'a',

$$I_0 = I_1 + I_{B3} \longrightarrow (2)$$

But $I_2 =$ Emitter current of ' Q_3 '.

we know $I_E = I_B + I_C$ [common eqⁿ in all configurations
CE, CB, CC]

$$= \frac{I_C}{\beta} + I_C$$

$$= I_C \left(1 + \frac{1}{\beta}\right)$$

$$\Rightarrow I_E = I_C \left(\frac{1+\beta}{\beta}\right)$$

But $I_2 = I_E = \frac{(1+\beta)I_C}{\beta}$

[collector current
 $I_C = I$]

$$\therefore \boxed{I_2 = \frac{(1+\beta)I}{\beta}}$$

substitute value of I_2 in eq (1), we get

$$\textcircled{1} \Rightarrow I_1 = \frac{\frac{(1+\beta)I}{\beta}}{\left(1 + \frac{2}{\beta}\right)} = \frac{(1+\beta)I}{\beta \left(1 + \frac{2}{\beta}\right)} = \frac{I \left(1 + \frac{1}{\beta}\right)}{\beta \left(1 + \frac{2}{\beta}\right)}$$

$$\therefore \boxed{I_1 = I \frac{\left(1 + \frac{1}{\beta}\right)}{\left(1 + \frac{2}{\beta}\right)}} \longrightarrow (3)$$

put eq (3) in eq (2), we get

$$I_0 = I_{B3} + I_1$$

$$\Rightarrow I_0 = \frac{I}{\beta} + I \frac{\left(1 + \frac{1}{\beta}\right)}{\left(1 + \frac{2}{\beta}\right)}$$

[$\therefore$ In CE eqⁿ]
 $I_B = \frac{I_C}{\beta}$]

$$\Rightarrow \boxed{I_0 = I \left[\frac{1}{\beta} + \frac{1 + \frac{1}{\beta}}{1 + \frac{2}{\beta}} \right]}$$

$$\therefore \boxed{I = \frac{I_0}{\left(\frac{1}{\beta} + \frac{1 + \frac{1}{\beta}}{1 + \frac{2}{\beta}} \right)}} \quad \text{***}$$

If β is very large, Then $\frac{1}{\beta}$ is very low.

i.e., $\frac{1}{\beta}$ and $\frac{2}{\beta}$ are negligible

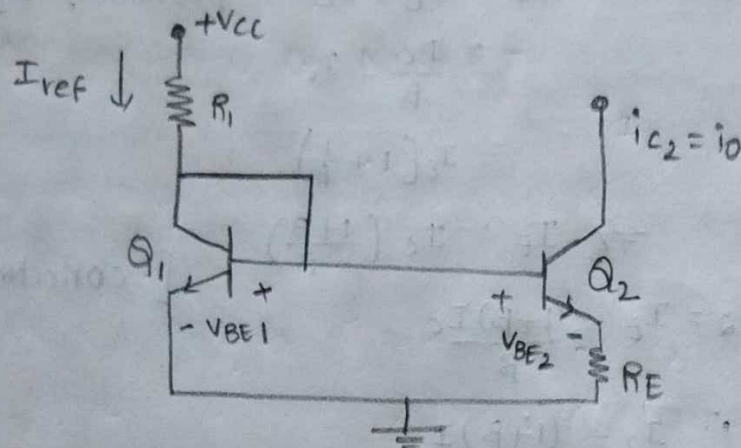
$$\Rightarrow I = \frac{I_0}{0+1} = I_0$$

$$\therefore \boxed{I \simeq I_0}$$

4. Widlar current Source:-

⇒ TO require low current source Then we use widlar current source.

⇒ Used for low current source [I_{ref}]



⇒ TO get low current source [I_{ref}].

1. R_1 should be very very high, Then I_{ref} ↓ses. Then we use it for low current source.

But practically it is difficult, because we are using R_E at ' Q_2 '. Due to this R_E , V_{BE2} ↓ses.

we know ↓ $V_{BE} = V_{BE2}$ ↓ses

⇒ If V_{BE} ↓ses Then $i_{c2} = i_o$ will becomes less.

Unit 1 - MOSFET Amplifier

1. Introduction to MOSFET Amplifier

2. Common Source Amplifier

3. Differential Amplifier

4. CMOS Amplifier

5. BJT Amplifier

6. Summary