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SECTION: _____

MAX. 10 MARKS



Unit-1 MOSFET

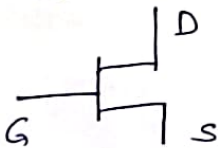
- * Transistor is a 3 terminal device (collector, base, emitter).
- * Due to the varying input, the transistor produces output current. So, it is a current controlled current device (CCCD).
- * The o/p current produces with function of i/p voltage. It is called "voltage controlled current device" (VCCD).

* BJT

o/p current $I_C = \beta I_B + (1 + \beta) I_{CO}$

where $I_{CO} \rightarrow$ reverse saturation current

FET



o/p current $I_D = I_{DS} = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$

where $I_D \rightarrow$ Drain current

$I_{DS} \rightarrow$ Drain Source current

* FET (Field effect transistor).

There are 2 types of FET.



JFET is not widely used now a days.
JFET is Junction field effect transistor.

MOSFET

Metal oxide semiconductor Field effect transistor. They are 2 types of MOSFET.

- 1) Enhancement MOSFET (E-MOSFET)
- 2) Depletion MOSFET (D-MOSFET)

In E-MOSFET - We need to create the channel.

In D-MOSFET - ~~we need~~ ^{not} the channel is already there.

* The path where carriers are moving from source to drain is called channel.

* In JFET, Gate to channel there is a junction i.e. Reverse biased which makes $I_G = 0$ but practically due to Reverse biased junction $I_G \neq 0$ due to small leakage current present. Due to this reason we give more priority to MOSFET compared to JFET.

MOSFET

* MOSFET stands for Metal oxide semiconductor field effect transistor.

* It operates in 2 modes.

- a) Enhancement mode MOSFET [EMOS]
- b) Depletion mode MOSFET [DMOS]

* Among the two compared E-MOSFET is difficult as we need to create the channel.

E-Mos

* It is of 2 types. They are

- 1) n-channel E-Mos
- 2) P-channel E-Mos.

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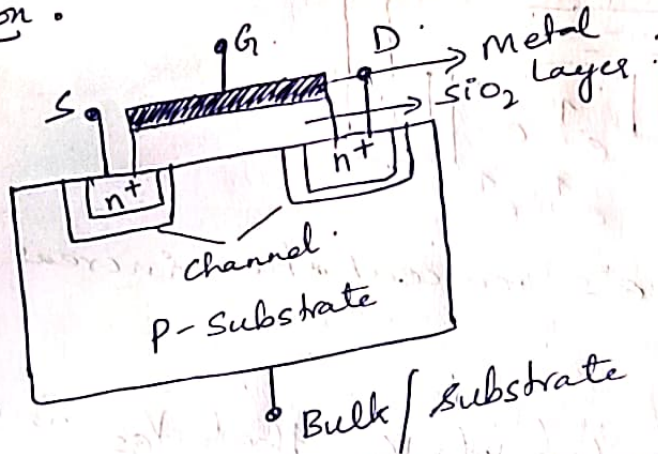
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E-MOS (n-channel)

Construction :-



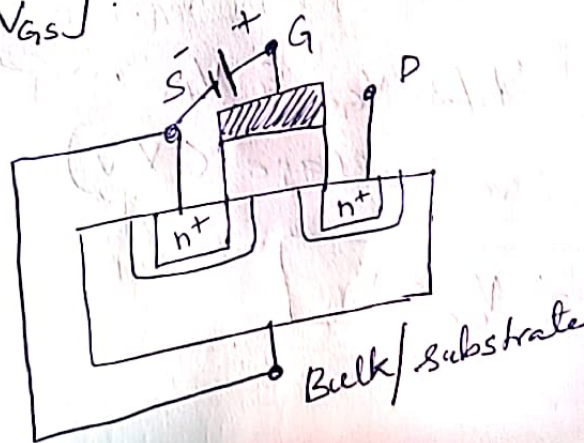
* p- is lightly doped substrate and n+ is heavily doped.

* In MOSFET, source & substrate are short-circuited.

Operation :-

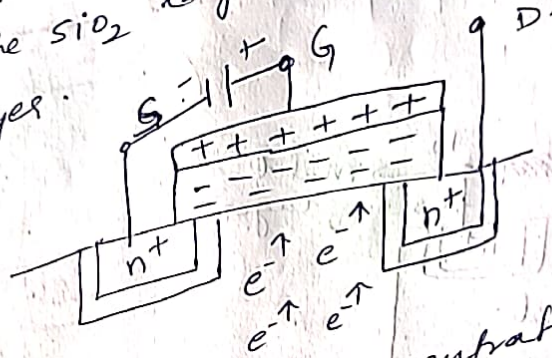
① Create a channel :-

* To form a channel we need to give some voltage b/w gate & source [V_{GS}].



1) $V_{GS} > 0$.

Gate is +ve w.r.t source & bulk. So, the metal becomes positive & polarization takes place in SiO_2 layer. Due to the SiO_2 layer the e^- get attracted below the oxide layer.



These accumulated e^- s concentration increases with $\uparrow$ of V_{GS} value.

- * At a particular value of V_{GS} that V_{GS} is called threshold voltage (V_{th}).
- * When accumulated e^- concentration = p-substrate majority carrier concentration then we call it as "channel".

$\therefore V_{GS} \geq V_{th} \rightarrow$ To operate MOSFET, we need to create a channel.

2) $V_{GS} > V_{th}$.

- * The difference b/w V_{GS} & V_{th} is called "over drive voltage (or) effective voltage (V_{ov})".

$$V_{ov} = V_{GS} - V_{th}$$

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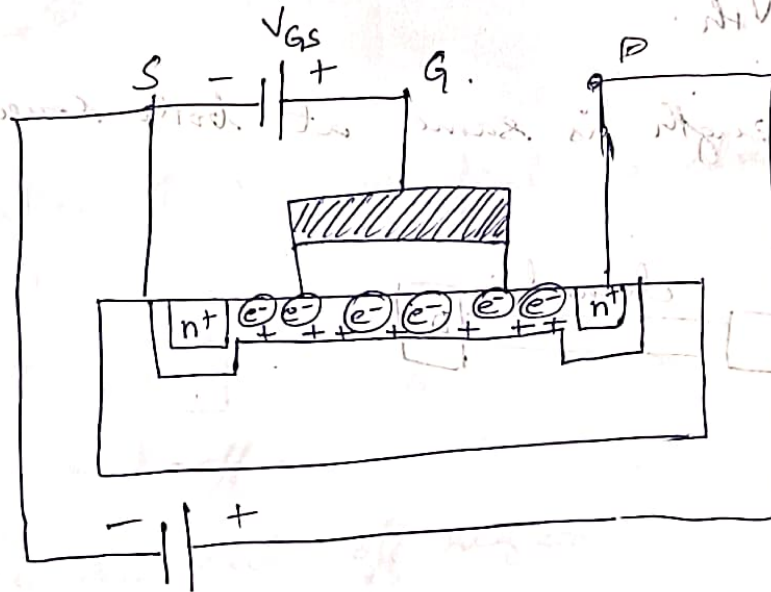
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② Applying V_{GS} & V_{DS} :

* keeping $V_{GS} \rightarrow$ constant and vary V_{DS} we get the

$V_{GS} - V_{DS}$ (net gate to channel voltage).



For creating a channel always $V_{GS} > V_{th}$.

* Drain & gate voltage both are +ve on the drain side

* Drain & source. Drain voltage is +ve & source voltage is -ve on source side.

$$\rightarrow V_{DS} = V_D - V_S$$

when $V_{GS} - V_{DS} = \text{max}$ the channel at source is more.

$V_{GS} - V_{DS} = \text{min}$ at drain side channel is less.

* When both V_{GS} & V_{DS} are applied. Net gate to channel is $(V_{GS} - V_{DS})$

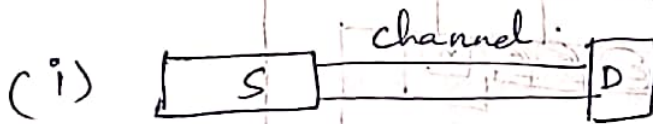
If $V_{GS} - V_{DS} = \min$ @ drain channel is less at drain.

If $V_{GS} - V_{DS} = \max$ @ source channel is more at source.

Case (1)

* If $V_{DS} = 0$
 $V_{GS} > V_{th}$

channel length is same at both source & drain side.



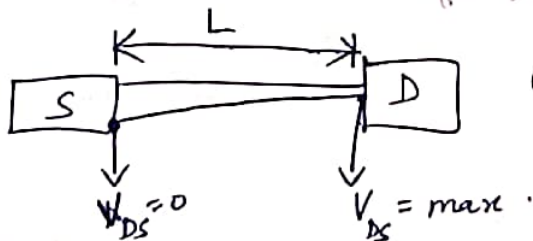
Case (2)

(2) $V_{DS} > 0$

$$V_{GS} - V_{DS} > V_{th}$$

V_{DS} value is $\uparrow$ from source to drain. At source:

$V_{DS} = 0$ & at drain $V_{DS} = \max$.



where $L \rightarrow$ length of channel.

$\therefore V_{GS} - V_{DS} = \max$ @ source end channel is max.

$V_{GS} - V_{DS} = \min$ @ drain side channel is min.

Hence channel length gets decreased from source to drain as $V_{DS} \uparrow$, I_{DS} also $\uparrow$ w.r.t V_{DS} .

$\therefore$ Drain current $I_{DS} \uparrow$ until $V_{GS} - V_{DS} = V_{th}$

~~When $V_{GS} > V_{th}$~~

* Case ③

As we further $\uparrow V_{DS}$ we find no channel @ drain side. ($I_{DS} = 0$)



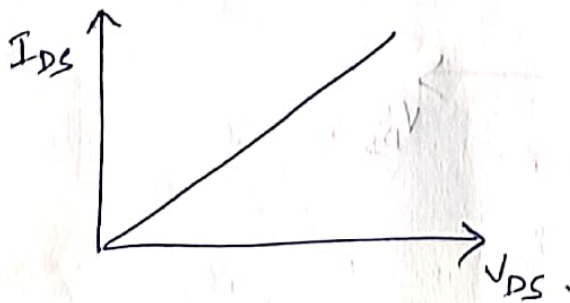
pinch-off.

$$V_{GS} - V_{DS} < V_{th}$$

When $I_{DS} = 0$ its cut-off region.

$$\left. \begin{array}{l} V_{GS} > V_{th} \text{ \& } V_{DS} > 0 \\ V_{GS} - V_{DS} > V_{th} \\ (\text{or}) \\ V_{GS} - V_{th} > V_{DS} \end{array} \right\}$$

If any of these case
satisfied
 $I_{DS} \uparrow$ w.r.t V_{DS} linearly.



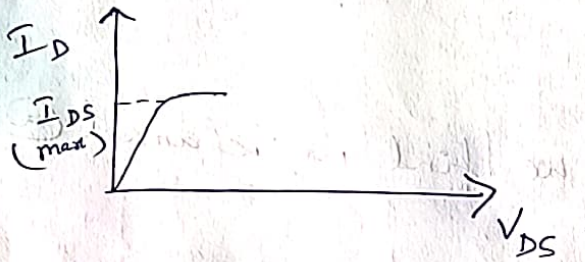
* Case (4)

$$V_{GS} > V_{th}$$

$$V_{DS} > 0$$

$$V_{GS} - V_{DS} = V_{th}$$

then I_{DS} is more & I_D just starts to enter into saturation region.



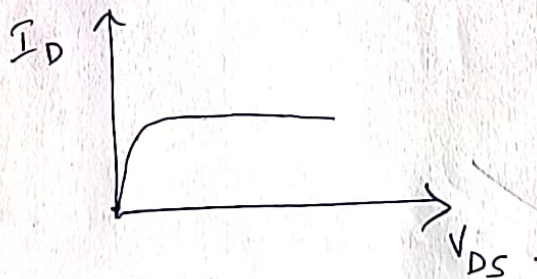
* Case (5)

$$V_{GS} > V_{th}$$

$$V_{DS} > 0$$

$$V_{GS} - V_{DS} < V_{th}$$

then I_{DS} is constant & this region is called saturation region.



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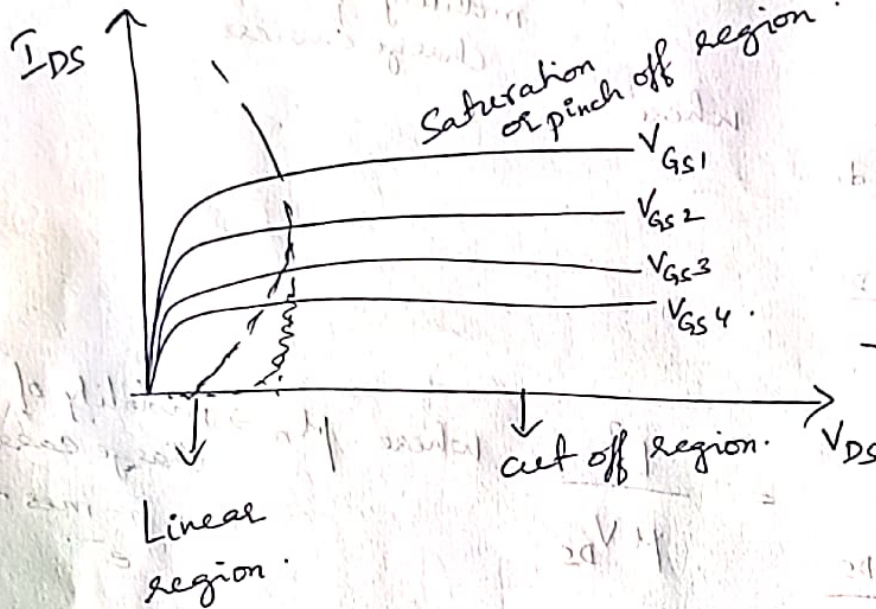
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Transfer characteristics of E-Mos n-channel.

Regions of operation



cut off.

$$V_{GS} < V_{th} \text{ \& } I_{DS} = 0.$$

Linear region.

$$V_{GS} > V_{th} \text{ \& } V_{GS} - V_{DS} = V_{th}.$$

Sat region.

$$V_{GS} > V_{th} \text{ \& } V_{DS} \geq V_{GS} - V_{th}.$$

* In linear region MOSFET is used as resistor & when MOSFET enters saturation region it is used as amplifier.

→ Relation btw I_{DS} & V_{DS} :-

I_{DS} - drain to source current / Drain current.

We know that $I = \frac{Q}{t} = \frac{\text{charge}}{\text{time}}$

$$\frac{I_{DS}}{\tau} = \frac{Q_c}{\tau}$$

where $Q_c \rightarrow$ charge induced in the channel.

$\tau \rightarrow$ transient time.

Direction of current is from drain to source so I_{DS} .

$\tau \Rightarrow$ time taken by e^- to move from source to drain in channel.

$\tau = \frac{L}{V}$ where $L \rightarrow$ Length of channel (In physics $\tau = \frac{\text{distance}}{\text{velocity}}$)
 $V \rightarrow$ Velocity.

$\tau = \frac{L}{V}$ where $V = \mu E_{ds}$ Electric field to drain source.
 $\downarrow$
 mobility of charge carriers

$\tau = \frac{L}{\mu E_{ds}}$ where

$E_{ds} = \frac{V_{ds}}{L}$

$\tau = \frac{L}{\mu V_{ds}} = \frac{L^2}{\mu V_{ds}}$ where $\mu_n \rightarrow$ mobility of charge carriers in n-mos its e^- .

Non - Sat

Charge per unit area $Q = E \cdot \epsilon$

Total charge induced in Q_c channel. $\epsilon = \epsilon_{\text{insulator}} \cdot \epsilon_0$
 $\downarrow$
 permittivity of free space.

where $A =$ Total Area.

$A = WL$

$= \epsilon_{\text{ins}} \cdot \epsilon_0 \cdot WL$

$\downarrow$
 Relative permittivity of insulator b/w gate & channel & since we are using SiO_2 .



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$$Q_c = (\epsilon_{SiO_2} \cdot \epsilon_0 \cdot WL) (V)$$

$$\therefore C = \frac{\epsilon_{ins} \cdot \epsilon_0 \cdot A}{d} \quad \text{where } C \rightarrow \text{Gate to channel capacitance.}$$

$$C = \frac{\epsilon_{SiO_2} \epsilon_0 W \cdot L}{d} \quad \frac{\epsilon_0 \cdot A}{d} = \text{Capacitance.}$$

$$V = V_G - V_C$$

$$= (V_{GS} - V_{th}) - \frac{V_{DS}}{2}$$

$$\therefore Q_c = \frac{\epsilon_0 \cdot \epsilon_{SiO_2} WL}{d} \left[(V_{GS} - V_{th}) - \frac{V_{DS}}{2} \right]$$

$$\therefore I_{DS} = \frac{Q_c}{L^2} \mu_n V_{DS}$$

$$I_{DS} = \frac{\epsilon_0 \epsilon_{SiO_2} WL}{d} \left[(V_{GS} - V_{th}) - \frac{V_{DS}}{2} \right] \cdot \frac{\mu_n V_{DS}}{L^2}$$

where $C_{ox} \rightarrow$ oxide capacitance per unit area.

$$C_{ox} = \frac{\epsilon_{SiO_2} \epsilon_0}{d}$$

$$I_{DS} = C_{ox} \frac{W}{L} \mu_n \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

→ For non-saturation region.

∴ V_{DS} is small hence $\frac{V_{DS}^2}{2}$ is very very small
hence we neglect $\frac{V_{DS}^2}{2}$.

For

$$I_{DS} = C_{ox} \mu_n \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} \right] \rightarrow \text{For Linear Region.}$$

∴ If $V_{DS} = V_{GS} - V_{th}$ in above equation ↑

$$I_{DS(sat)} = \mu_n C_{ox} \frac{W}{L} \left[\frac{(V_{GS} - V_{th})^2}{2} \right]$$

→ For saturation region.

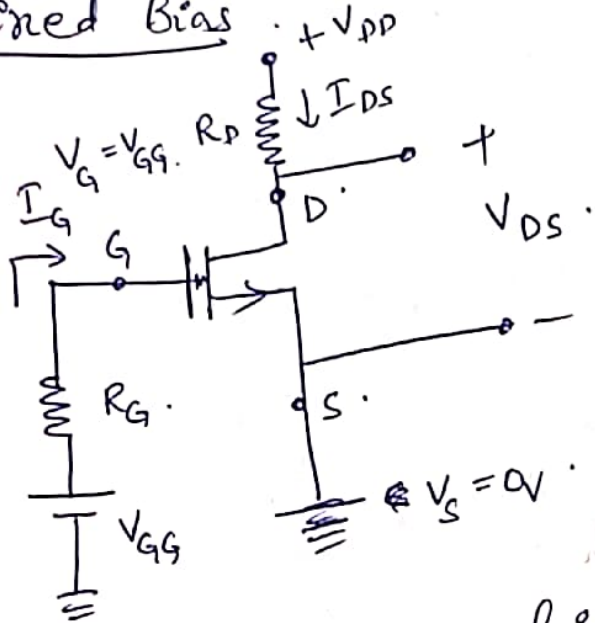
For cut off region

$I_{DS} = 0$ (hence channel is not created).

Biasing

We have different types of biasing

- 1) fixed bias
- 2) self bias
- 3) Voltage divider bias

Fixed Bias

R_G value is very high $\approx 1M\Omega$

Hence $I_G = 0$

$$\therefore I_D = I_S = I_{DS}$$

$$V_{GS} = V_G - V_S$$

$$= V_{GG} - 0$$

$$\left[\because V_G = V_{GG} \right]$$

$$V_S = 0V$$

$$\boxed{V_{GS} = V_{GG}}$$

$$I_{DS} = \beta [V_{GS} - V_{th}]^2$$

Apply KVL at o/p loop.

$$V_{DD} = I_{DS} R_D + V_{DS} + V_S$$

$$V_{DD} = I_{DS} R_D + V_{DS}$$

$$V_{DS} = V_{DD} - I_{DS} R_D$$

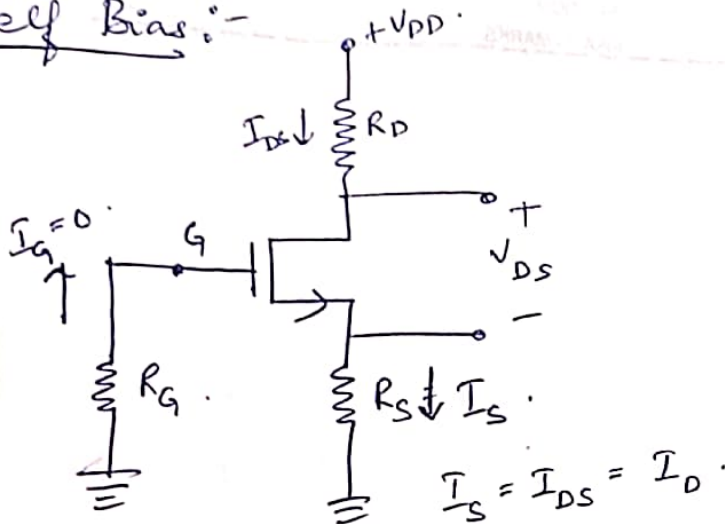
$$(\because V_S = 0V)$$

$\propto \frac{W}{L} \mu_n$ region.

Disadv/Drawback:-

Requires 2 power supplies (V_{GG} & V_{DD}) hence we go to self bias technique.

Self Bias:-



Since R_G value is very high.

$$V_{GG} = 0.$$

$V_S = I_{DS} R_S$ $\because I_G = 0$, current I_{DS} will flow from drain to source.
Hence $I_S = I_{DS}$

$$I_S = I_{DS} = I_D.$$

$$V_{GS} = V_G - V_S$$

$$V_{GS} = 0 - I_{DS} R_S.$$

$$\boxed{V_{GS} = -I_{DS} R_S}$$

$\therefore V_{GS}$ value is -ve.

Hence self bias is not used. Hence we move to voltage divider bias.



Time

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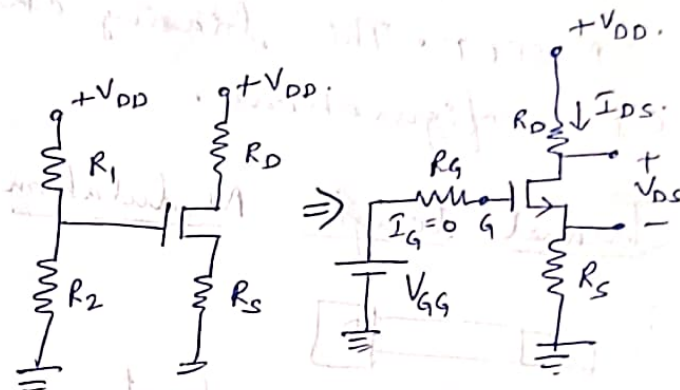
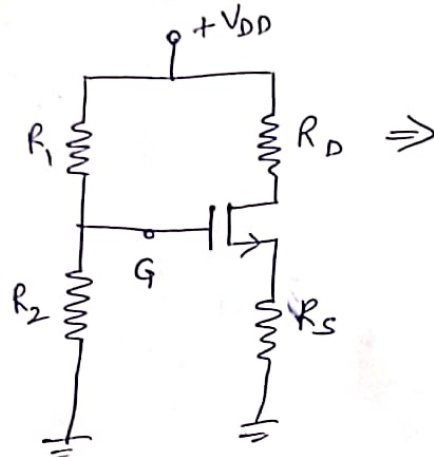
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Voltage divider Bias :-



Ckt is replaced with thevenin's equivalent ckt.

$$V_G = V_{GG}$$

$$I_G = 0$$

$$V_S = I_{DS} R_S$$

$$\therefore V_{GS} = V_G - V_S$$

$$V_{GS} = V_{GG} - I_{DS} R_S$$

V_{GS} value obtained is +ve if V_{GG} & I_{DS} value are properly selected.

$$I_{DS} = \beta [V_{GS} - V_{th}]^2$$

$$= \beta [V_{GG} - I_{DS} R_S - V_{th}]^2 \quad \left[\because V_{GS} = V_{GG} - I_{DS} R_S \right]$$

$$= \text{min}(I_D)$$

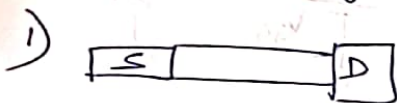
To get V_{DS} , Apply KVL at o/p loop. (1)

$$V_{DD} = I_{DS} R_D + V_{DS} + I_{DS} R_S$$

$$V_{DS} = V_{DD} - I_{DS} [R_D + R_S]$$

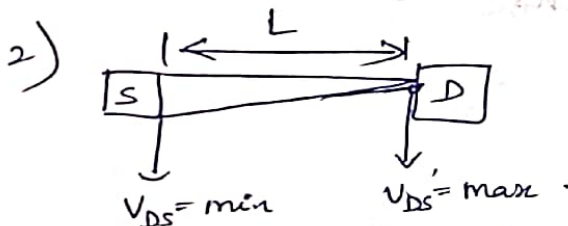
Since V_{DS} value is +ve we use it mostly in MOSFET. This biasing ckt is used for CS, CG & CD configurations.

Channel length Modulation

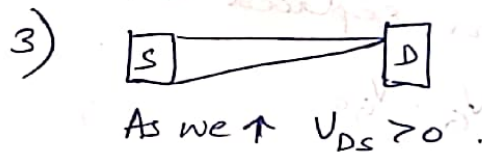


channel is constant

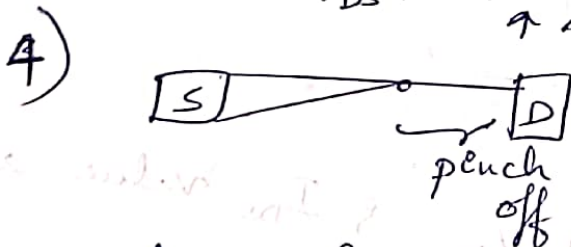
when $V_{DS} = 0$.



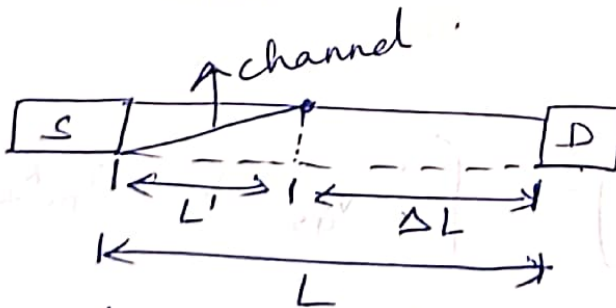
$V_{DS} > 0$ & length $\uparrow$ slowly.



As we $\uparrow V_{DS} > 0$.



As we further $\uparrow V_{DS}$ channel does not reach till the drain.



$$L = L' + \Delta L$$



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$$L' = L - \Delta L$$

$$L' = L \left(1 - \frac{\Delta L}{L} \right)$$

where L - Total length.

L' - current length

ΔL = small change in length.

$$I_{Ds(sat)} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2$$

Let us consider current is I_{DS}'

$$I_{DS}' = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2$$

$$= \frac{\mu_n C_{ox}}{2} \frac{W}{L \left(1 - \frac{\Delta L}{L} \right)} (V_{GS} - V_{th})^2$$

$$I_{DS}' = I_{Ds(sat)} \left(\frac{1}{\left(1 - \frac{\Delta L}{L} \right)} \right)$$

$$= I_{Ds(sat)} \left[1 - \frac{\Delta L}{L} \right]^{-1}$$

$$\text{For } \frac{\Delta L}{L} \ll 1 \rightarrow \left(1 - \frac{\Delta L}{L} \right)^{-1} = \left(1 + \frac{\Delta L}{L} \right)$$

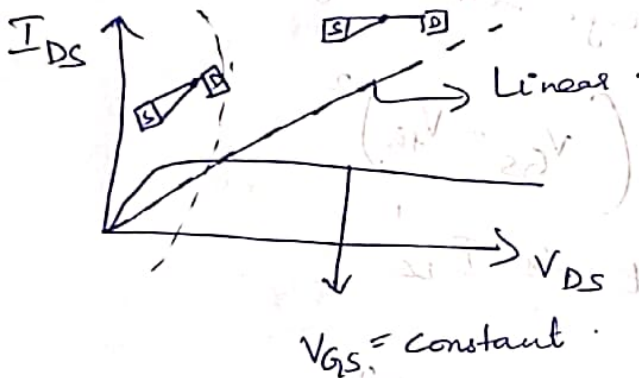
$$\therefore I_{Ds}' = I_{Ds}(\text{sat}) \left[1 + \frac{\Delta L}{L} \right]$$

$$\frac{\Delta L}{L} \propto V_{Ds}$$

As we $\uparrow \frac{\Delta L}{L}$, V_{Ds} also $\uparrow$.

$$\frac{\Delta L}{L} = \lambda V_{Ds} \text{ where } \lambda \rightarrow \text{proportionality constant.}$$

$$I_{Ds}' = I_{Ds}(\text{sat}) [1 + \lambda V_{Ds}]$$



We actually obtain a linear graph but due to channel length modulation the graph changes.

$$I_{Ds}' = I_{Ds}(\text{sat}) [1 + \lambda V_{Ds}]$$

$$I_{Ds}' = \frac{\mu_n C_{ox}}{2} \times \frac{W}{L} [V_{GS} - V_{th}]^2 [1 + \lambda V_{Ds}]$$



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Large s/g and small s/g Model :-

Large s/g Model

$$I_{DS} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Considering the I_{DS} for linear region.

$$\therefore I_{DS} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} \left[2(V_{GS} - V_{th}) V_{DS} - V_{DS}^2 \right]$$

Since V_{DS} is small we neglect it & its called deep triode region.

$$I_{DS} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} \left[(V_{GS} - V_{th})^2 \right] (1 + \lambda V_{DS})$$

↳ in saturation region

If $\frac{V_{DS}^2}{2}$ is negligible.

$$I_{DS} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} \left[2(V_{GS} - V_{th}) V_{DS} \right]$$

↳ In

In this deep triode region MOSFET acts as resistor.

$$R_{on} = \frac{V_{DS}}{I_{DS}} = \frac{V_{DS}}{\frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} \left[2(V_{GS} - V_{th}) V_{DS} \right]}$$

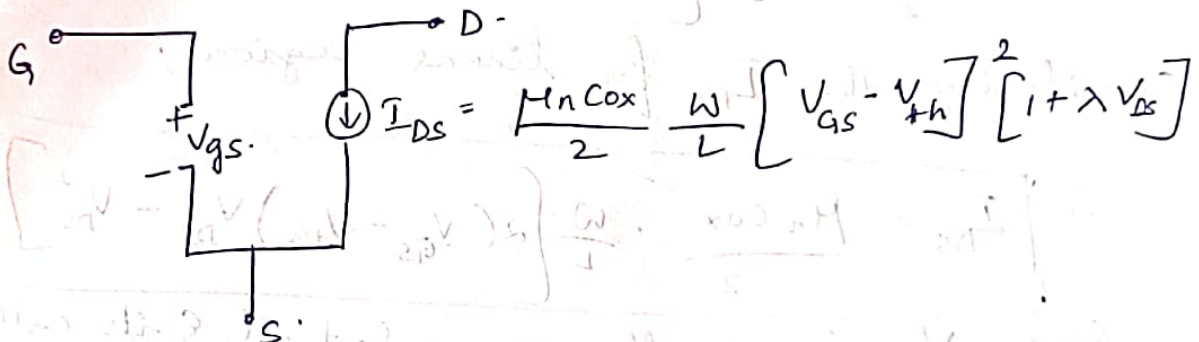
$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L} [V_{GS} - V_{th}]}$$

In saturation region :-

$$V_{GS} > V_{th}$$

$$V_{DS} > V_{GS} - V_{th}$$

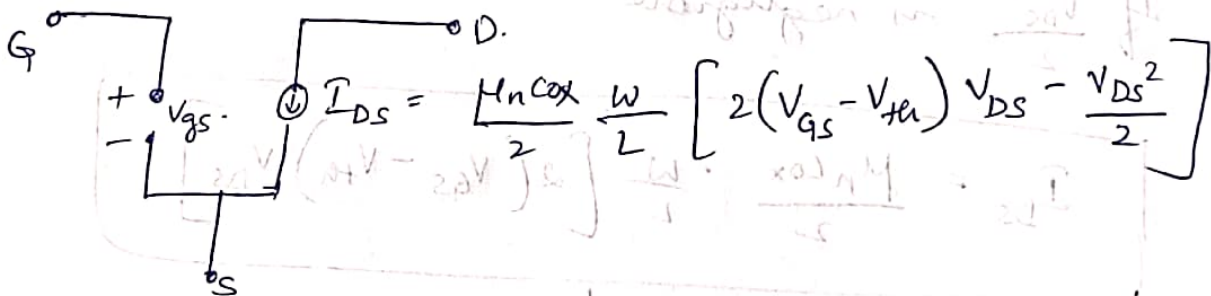
Then MOSFET is in large s/g model.



In Triode region

$$V_{GS} > V_{th}$$

$$V_{DS} < V_{GS} - V_{th}$$



In deep triode region

$$V_{GS} < V_{th}$$

$$V_{DS} \ll 2(V_{GS} - V_{th})$$



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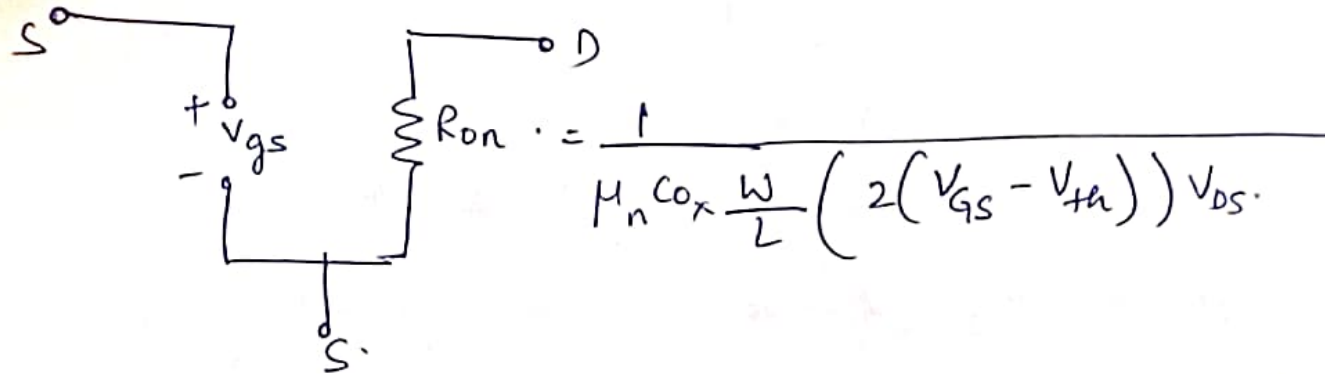
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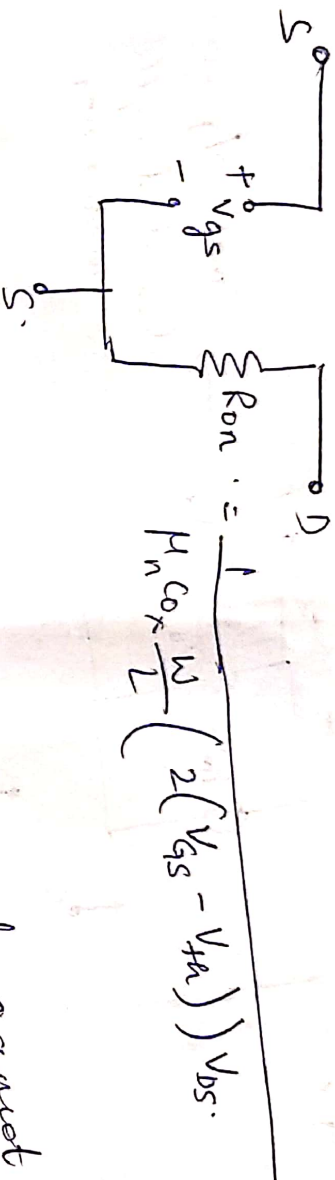
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Since V_{DS} value is very small channel cannot be created hence MOSFET acts as resistor.

All DC values are high so we are using large s/g model.

Small s/g Model



Since V_{DS} value is very small channel cannot be created hence MOSFET acts as resistor.

All DC values are high so we are using large g_m model.

Small g_m Model

From I-V characteristics

$$I_{DS} = f(V_{GS}, V_{DS})$$

By using Taylor's Series.

$$\Delta I_{DS} = \frac{\partial I_{DS}}{\partial V_{GS}} \cdot \Delta V_{GS} + \frac{\partial I_{DS}}{\partial V_{DS}} \cdot \Delta V_{DS}$$

where, ΔI_{DS} - small change in $I_{DS} = i_d$.

ΔV_{GS} - small change in $V_{GS} = V_{GS}$.

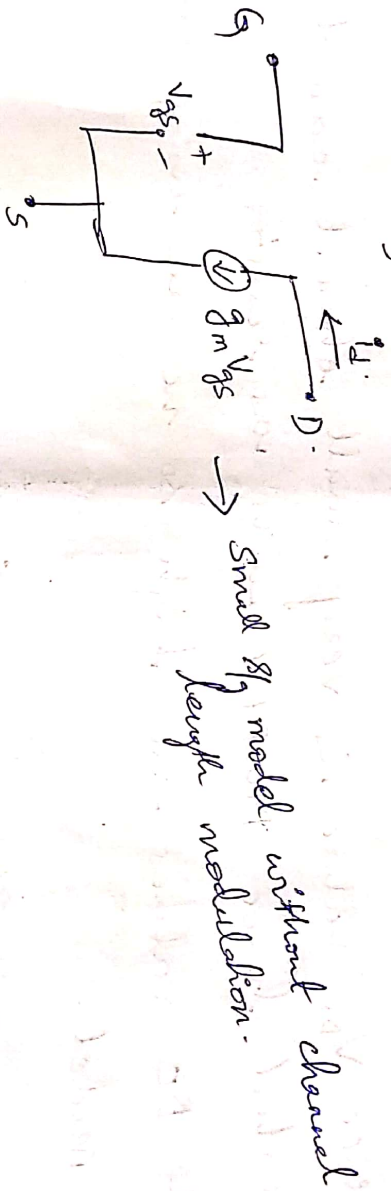
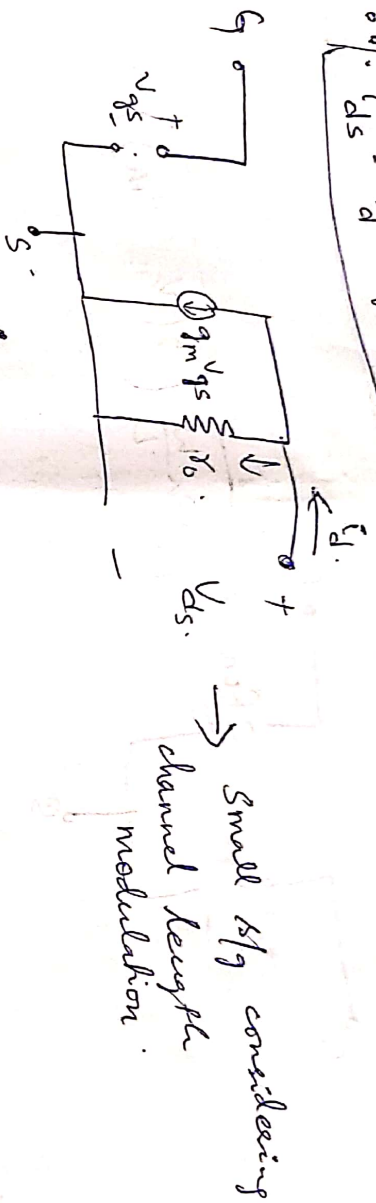
ΔV_{DS} - small change in $V_{DS} = V_{DS}$.

$$\left[\frac{\partial I_{DS}}{\partial V_{GS}} = g_m \right] = \text{Transconductance} \quad \left[g_m = \frac{1}{r} \right]$$

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$$\frac{\partial I_{DS}}{\partial V_{DS}} \left(\frac{\partial I_{DS}}{\partial V_{DS}} \right) = \frac{1}{r_o} = \frac{1}{r_d} = \text{of conductance}$$

$$i_{ds} = i_d = g_m V_{gs} + \frac{1}{r_o} \cdot V_{ds}$$



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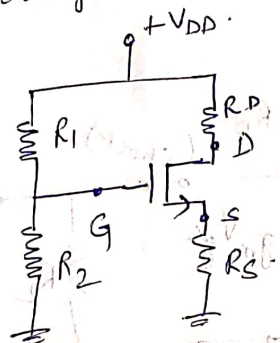
Amplifiers :-

* amplifies the weak $i/s/g$ (A_c) without changing the characteristics except its magnitude / amplitude.

* In any amplifier, we need to calculate 4 parameters.

- They are
- 1) current gain (A_i).
 - 2) i/p impedance (R_i).
 - 3) o/p impedance (R_o).
 - 4) voltage gain (A_v).

* We use voltage divider bias circuit.



Common Source Amplifiers :-

Procedure to draw the ckt diagram

* step ① - Add capacitors to 3 terminals (C_D, C_S, C_G)

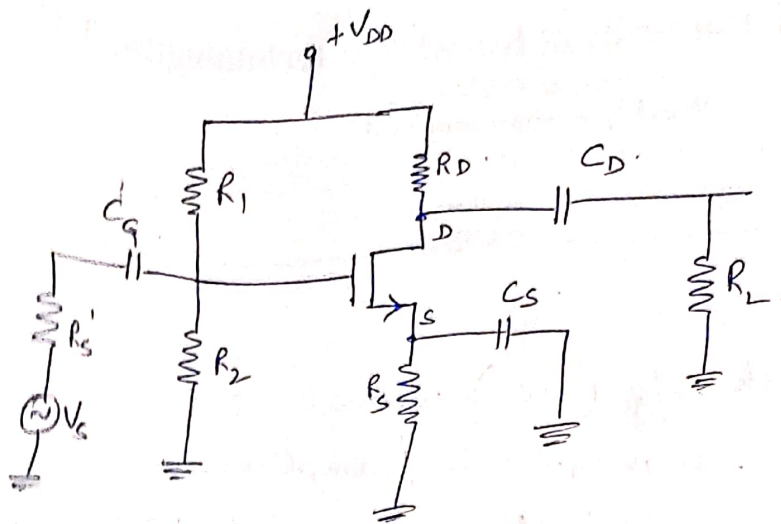
$C_D \rightarrow$ drain

C_S to source

C_G to gate.

step ② - Connect C_S to ground.

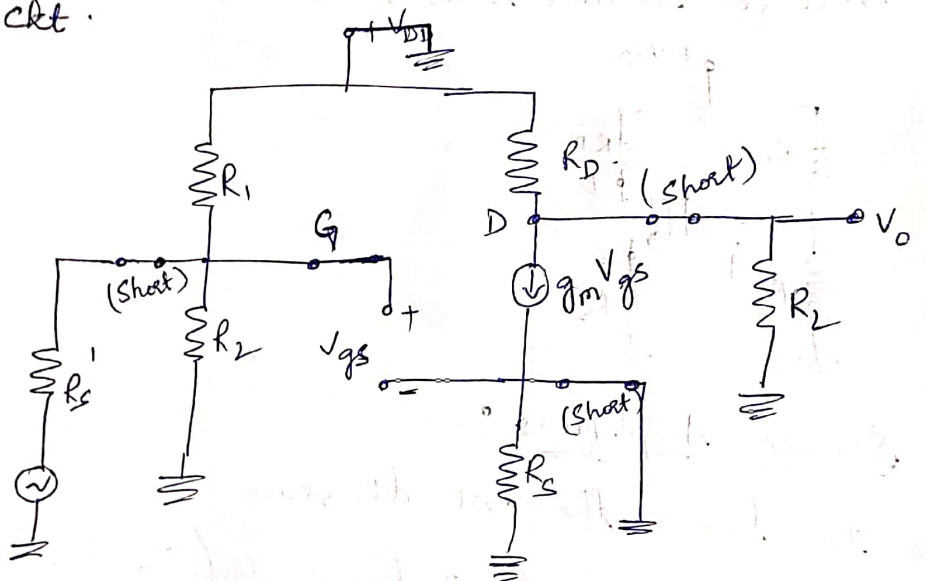
step ③ - Source at i/p & load at o/p .



Analysis:-

AC analysis

- Step ① - short ckt all external capacitors (C_S, C_g, C_D)
- Step ② - DC sources grounded.
- Step ③ - Replace MOSFET with its small s/g equivalent ckt.



Replace MOSFET with small s/g model.



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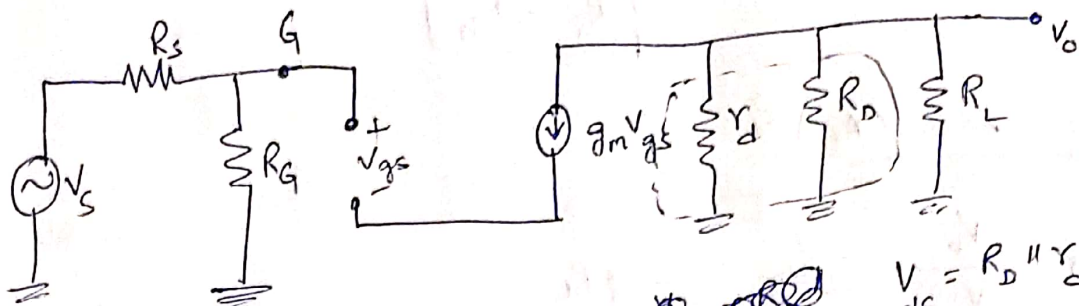
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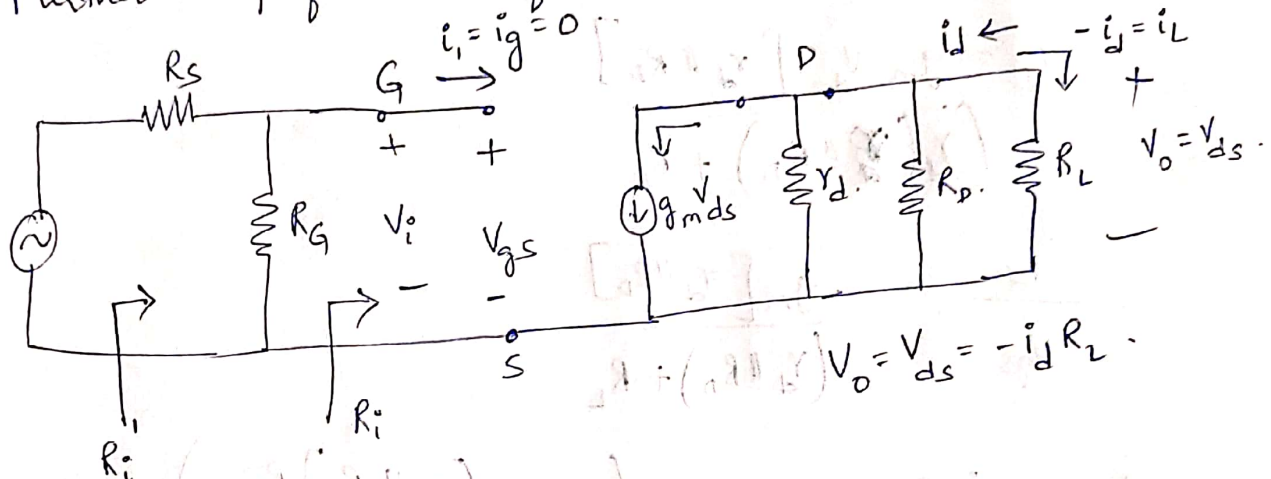
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Further simplification of the ckt.



* Current gain (A_i)

$$A_i = \frac{i_L}{i_i} = \frac{i_L}{i_g} = -\frac{i_d}{0} = \infty$$

Since $i_g = 0$ as R_G (Gate resistance is very high)

$$\therefore \boxed{A_i = \infty}$$

Input impedance (R_i)

$$R_i = \frac{V_i}{i_i} = \frac{V_i}{i_g} = \frac{V_i}{0} = \infty$$

$$R_i = \infty$$

But ideally i/p impedance is ∞ .

Effective input impedance $R_i' = R_i \parallel R_G$
 $= \infty \parallel R_G$

$$R_i' = R_G$$

Voltage gain (A_v):-

$$A_v = \frac{V_o}{V_i} = \frac{V_{ds}}{V_{gs}} = \frac{-i_d R_L}{V_{gs}}$$

From current division rule,

$$i_d = \frac{g_m V_{ds} [r_d \parallel R_D]}{(r_d \parallel R_D) + R_L}$$

$$\frac{i_d}{V_{gs}} = \frac{g_m [r_d \parallel R_D]}{(r_d \parallel R_D) + R_L}$$

$$A_v = \frac{-i_d R_L}{V_{gs}} = - \left(\frac{+ g_m [r_d \parallel R_D] R_L}{(r_d \parallel R_D) + R_L} \right)$$

$$\therefore \left(\frac{R_1 R_2}{R_1 + R_2} \text{ since } R_1 \parallel R_2 \right)$$

$$= - g_m [R_D \parallel r_d \parallel R_L]$$

$$\therefore A_v = - g_m [R_D \parallel R_L] \quad (\because r_d \gg R_L)$$



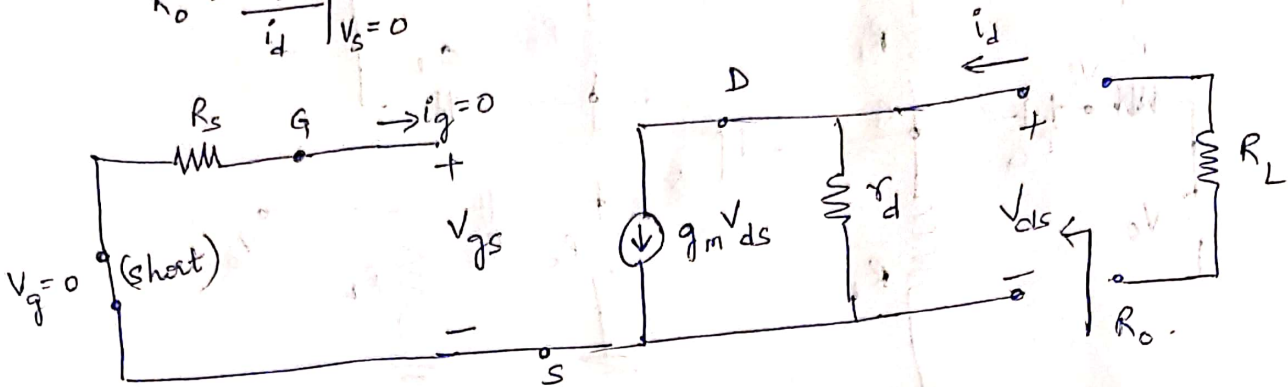
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output impedance (R_o)

$$R_o = \frac{V_o}{i_d} \bigg|_{V_s=0}$$



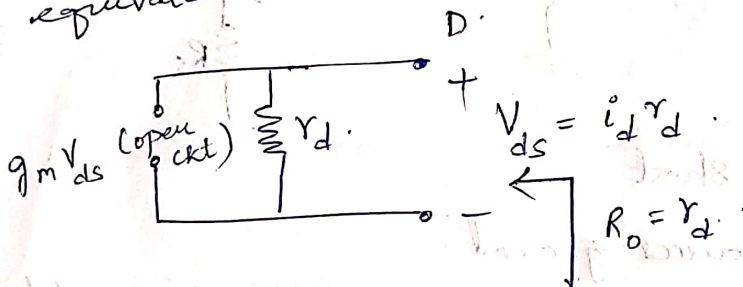
$$V_s = 0$$

$$V_{gs} = -i_g [R_g \parallel R_s]$$

$$= 0 [R_g \parallel R_s]$$

$$\therefore V_{gs} = 0$$

Then, the equivalent ckt is



$\therefore V_{gs} = 0$ then current $g_m V_{ds}$ is also zero meaning open ckt.

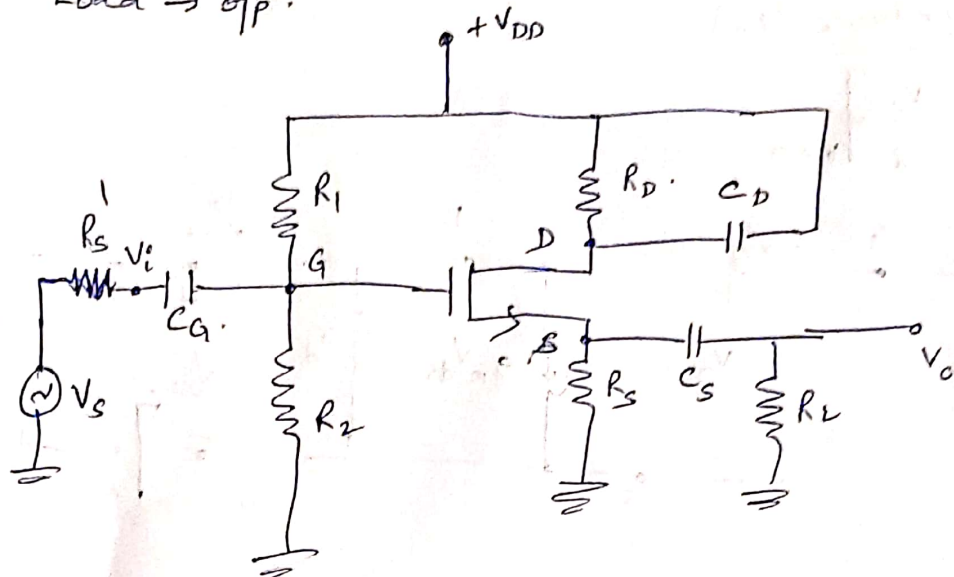
$$\text{Hence } R_D = \frac{V_o}{i_d} \bigg|_{V_s=0} = r_d$$

Effective output resistance.

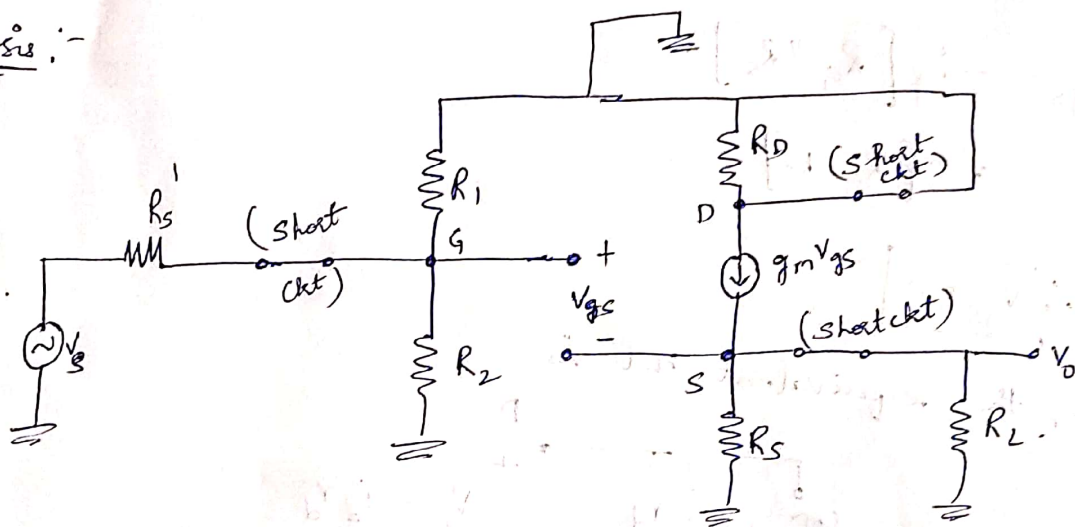
$$R_D' = R_D \parallel R_L = r_d \parallel R_L \approx R_L$$

Common Drain:-

- Step ① - Add 3 capacitors. (C_S, C_D, C_G).
Step ② - $C_D \rightarrow$ connected to supply voltage.
Step ③ - source at i/p.
Load $\rightarrow$ o/p.



Analysis:-



A

- Step ① $\rightarrow$ Capacitors short.
Step ② $\rightarrow$ Voltage sources ground.
Step ③ $\rightarrow$ Replace MOSFET with its equivalent ckt.

AC equivalent ckt:-

- Step ① $\rightarrow$ Connect drain to ground.
Step ② $\rightarrow$ Connect the source resistance to source & gate resistance to gate.
Step ③ $\rightarrow$ Add i/p source to the gate.



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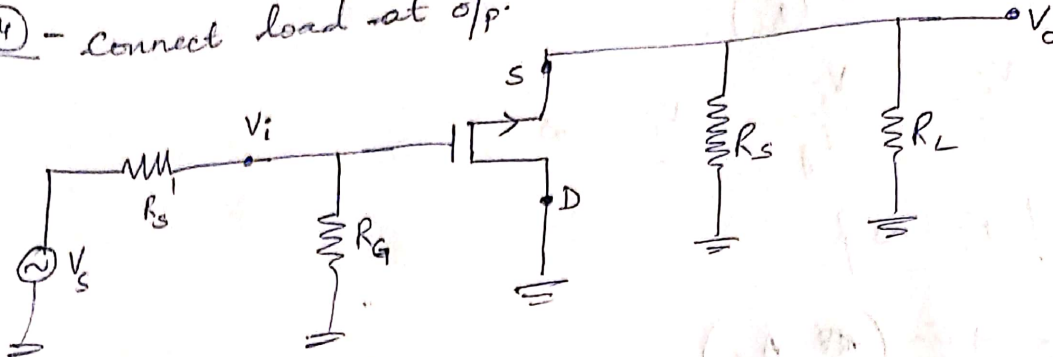
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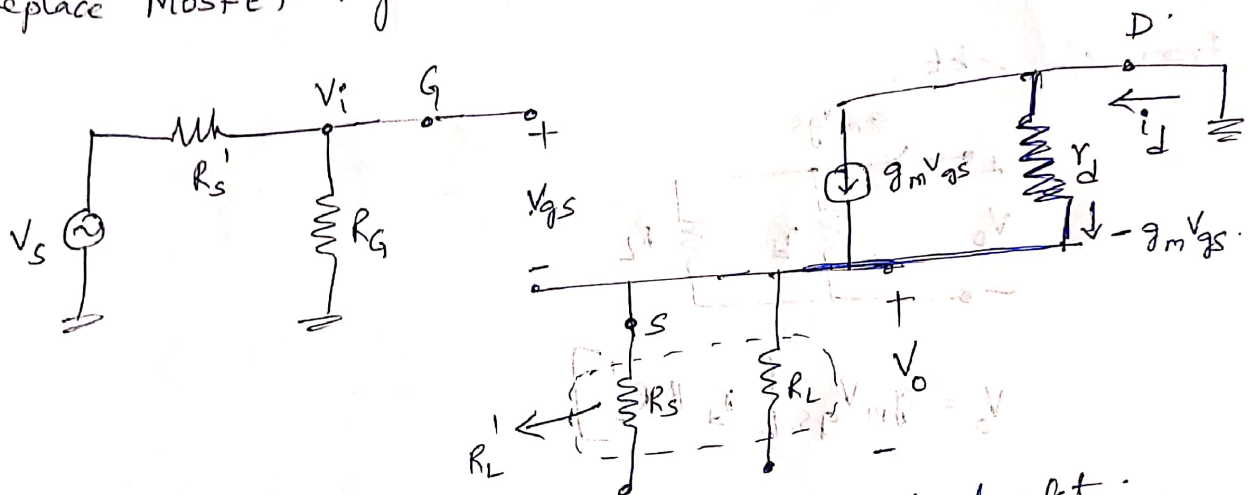
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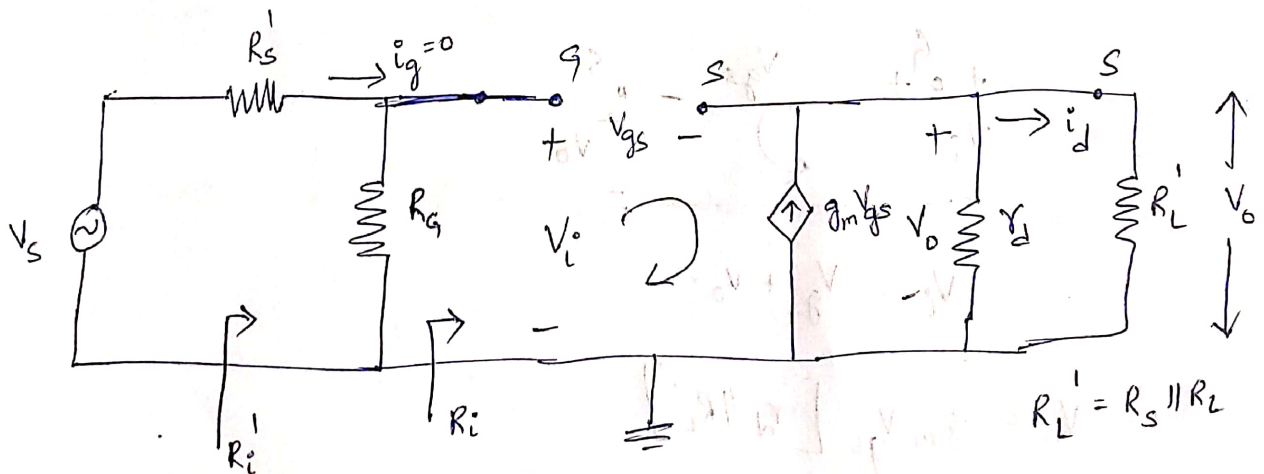
Step (4) - Connect load at o/p.



Step (5) -
Replace MOSFET by its small signal equivalent ckt.



For easy calculations modify the equivalent ckt.



Current gain (A_i) :-

$$A_i = \frac{i_L}{i_i} = \frac{i_d}{i_g} = \frac{i_d}{0} = \infty$$

$$\boxed{A_i = \infty} \quad [\because i_g = 0]$$

Input resistance (R_i) :-

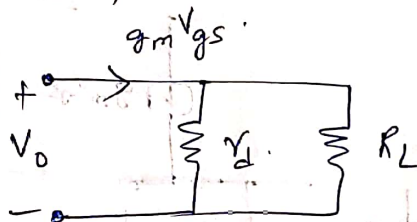
$$R_i = \frac{V_i}{i_i} = \frac{V_i}{i_g} = \frac{V_i}{0} = \infty$$

$$\boxed{R_i = \infty}$$

Voltage gain (A_v)

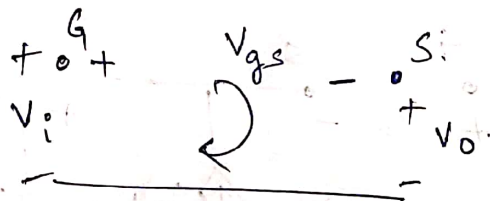
$$A_v = \frac{V_o}{V_i}$$

From o/p ckt,



$$V_o = g_m V_{gs} [r_d \parallel R_L']$$

Apply KVL at i/p side:



$$V_i = V_{gs} + V_o$$

$$\therefore V_o = g_m V_{gs} [r_d \parallel R_L']$$

$$V_i = V_{gs} + g_m V_{gs} [r_d \parallel R_L']$$



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$$V_i = V_{gs} \left[1 + g_m (r_d \parallel R_L') \right]$$

$$\therefore A_v = \frac{V_o}{V_i} = \frac{g_m V_{gs} (r_d \parallel R_L')}{V_{gs} (1 + g_m (r_d \parallel R_L'))}$$

$$A_v = \frac{g_m (r_d \parallel R_L')}{1 + g_m (r_d \parallel R_L')}$$

If $g_m (r_d \parallel R_L') \gg 1$ then 1 is ~~also~~ neglected

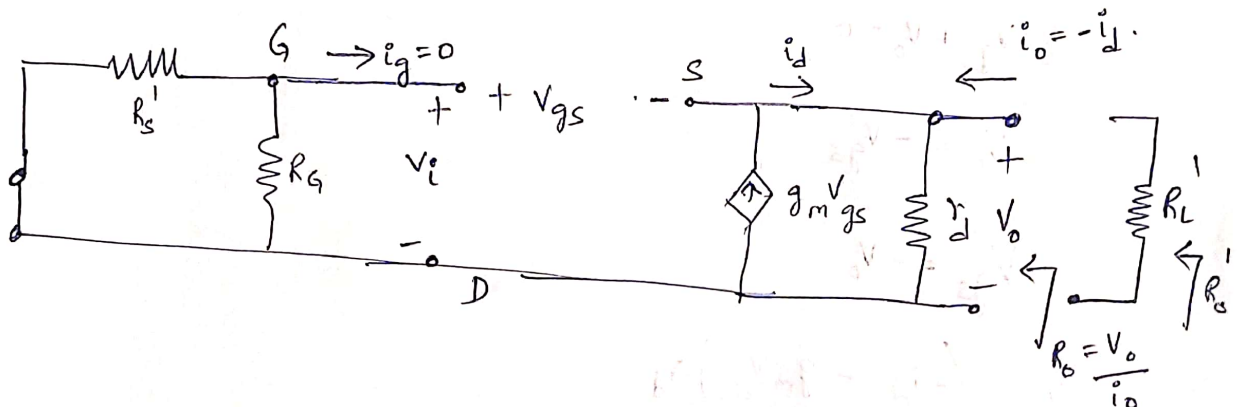
$$A_v \approx \frac{g_m (r_d \parallel R_L')}{g_m (r_d \parallel R_L')}$$

$$\therefore \boxed{A_v \approx 1}$$

Output resistance :-

$$R_o = \frac{V_o}{i_o} \Big|_{V_s=0}$$

$V_s = 0$ & Load R_L is disconnected.



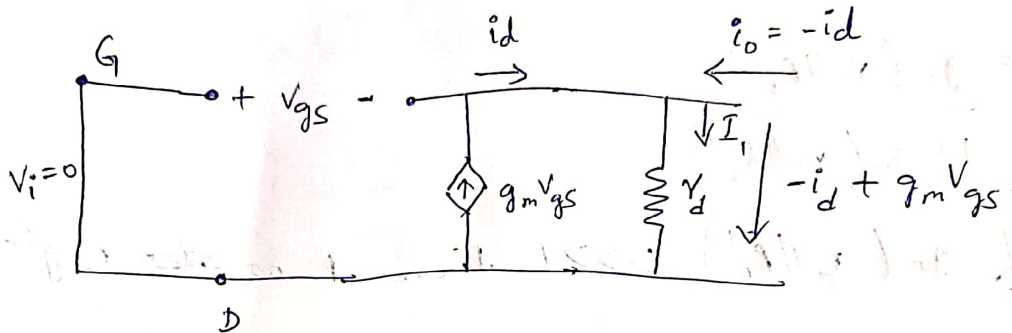
~~$$V_i = -i_g [R_s' \parallel R_G]$$~~

$$V_i = -i_g [R_s' \parallel R_G]$$

$$= 0 [R_s \parallel R_G] \quad (\because i_g = 0)$$

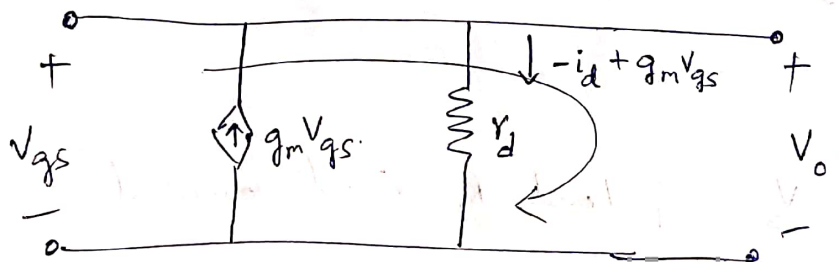
$$\boxed{V_g = 0} \quad (\text{short ckt})$$

Apply KCL.



$$g_m V_{gs} - i_d = I_1$$

Apply KVL



$$V_{gs} + V_o = 0$$

$$V_o = -V_{gs}$$

$$V_{gs} = -V_o$$

$$V_o = (-i_d + g_m V_{gs}) r_d$$



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$$V_o = -i_d r_d + g_m v_{gs} r_d$$

$$V_o = -i_d r_d + g_m (-V_o) r_d$$

$$V_o + g_m V_o r_d = -i_d r_d$$

$$V_o (1 + g_m r_d) = -i_d r_d$$

$$V_o = \frac{-i_d r_d}{(1 + g_m r_d)}$$

of p resistance $R_o = \frac{V_o}{i_o} \bigg|_{V_s=0} = \frac{V_o}{-i_d}$

$$R_o = \frac{-i_d r_d}{(1 + g_m r_d)}$$

$$= \frac{r_d}{(1 + g_m r_d)}$$

$$= r_d \times \frac{1}{g_m}$$

$$g_m \left(r_d \times \frac{1}{g_m} \right) \times \frac{1}{g_m}$$

$$= \frac{r_d \times \frac{1}{g_m}}{r_d + \frac{1}{g_m}}$$

$$\therefore R_D = r_d \parallel \frac{1}{g_m}$$

Effective o/p resistance.

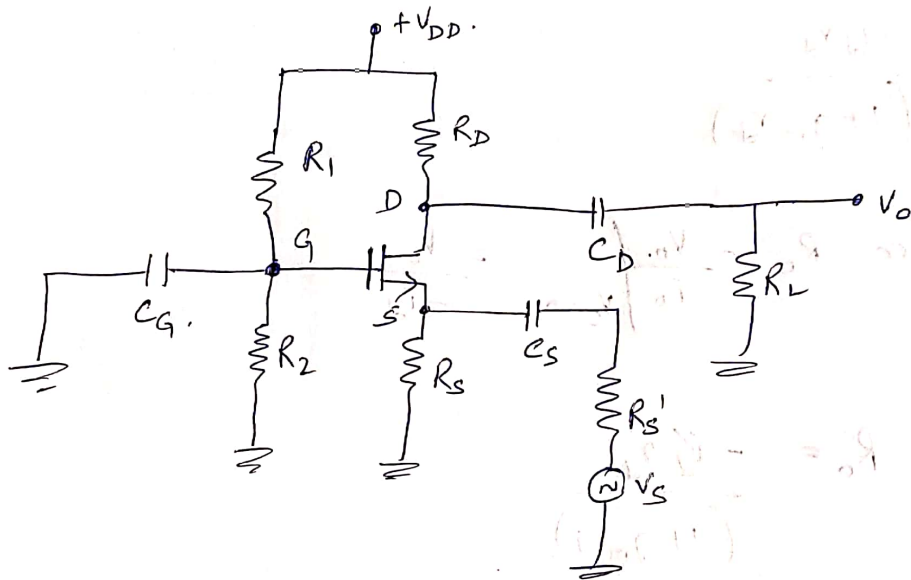
$$R_D' = \left(r_d \parallel \frac{1}{g_m} \right) \parallel R_L'$$

Common Gate :-

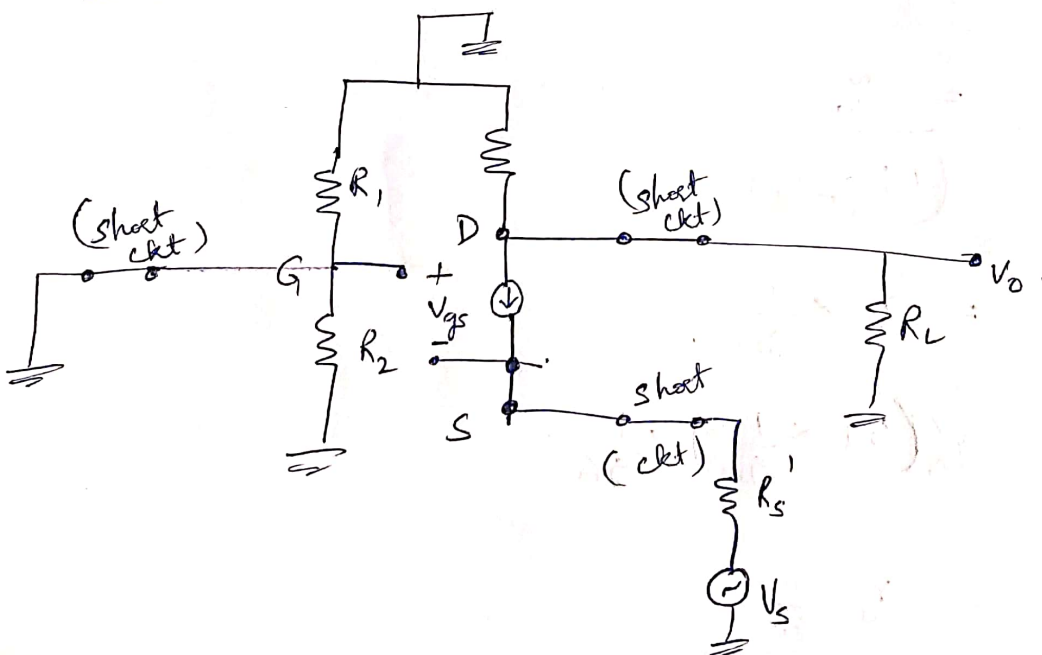
Step ① - Add 3 capacitors.

Step ② - $C_G \rightarrow$ ground.

Step ③ - source at i/p, load at o/p.



AC equivalent ckt :-





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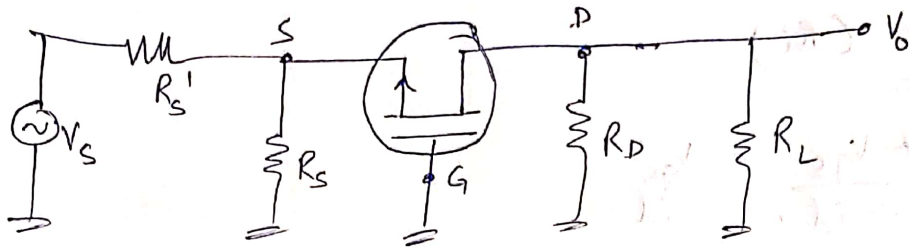
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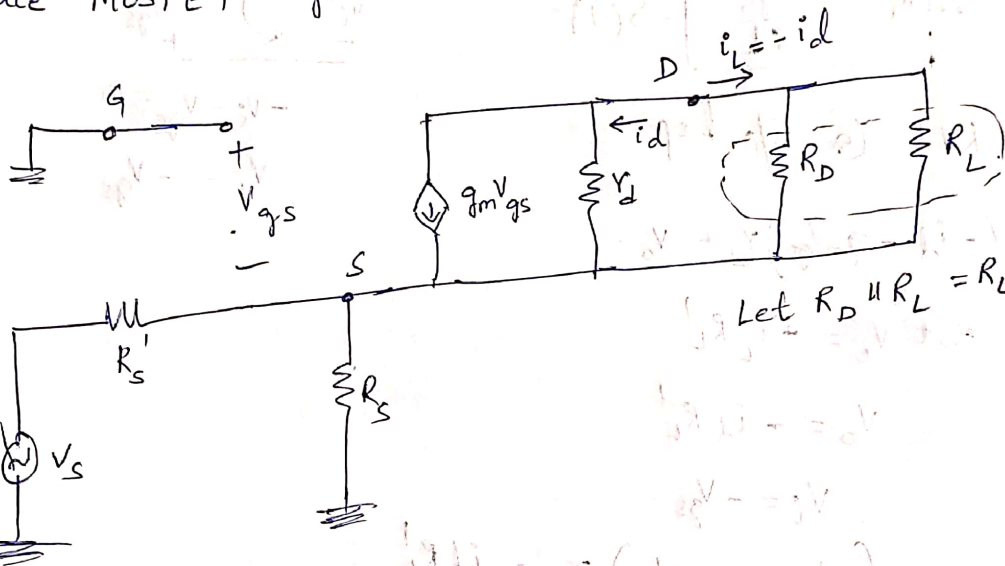
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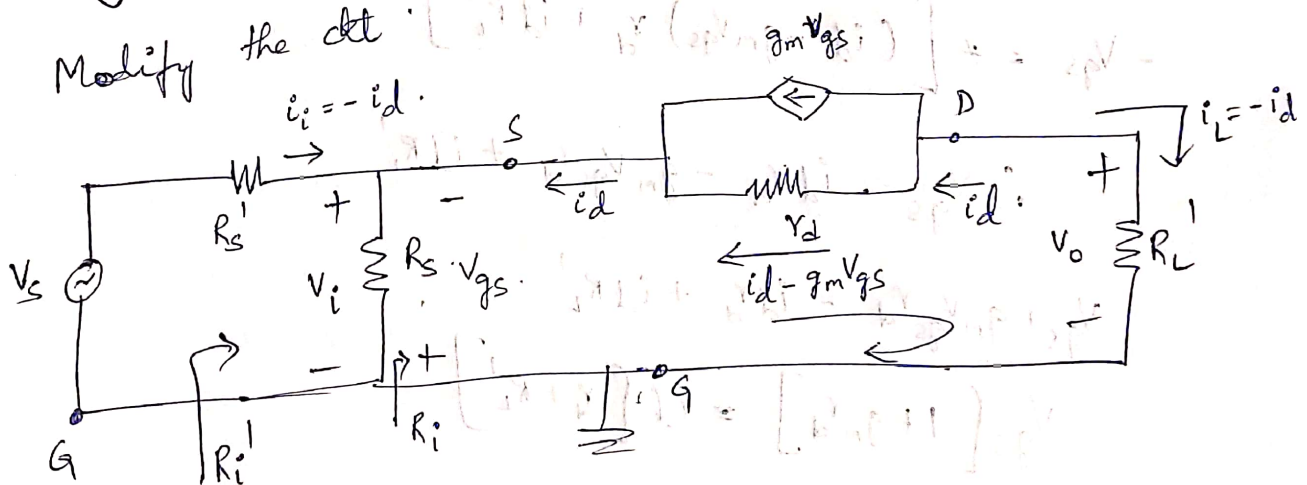
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Replace MOSFET by the small s/g equivalent ckt.



Modify the ckt.



Current gain (A_i)

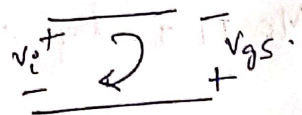
$$A_i = \frac{i_L}{i_i} = \frac{-i_d}{-i_d} = 1$$

$$\boxed{A_i = 1}$$

Input resistance (R_i)

$$R_i = \frac{V_i}{i_i} = \frac{+V_{gs}}{-i_d} = \frac{V_{gs}}{i_d}$$

$$\therefore \boxed{R_i = \frac{V_{gs}}{i_d}} \rightarrow (1)$$



$$-V_i - V_{gs} = 0$$

$$V_i = -V_{gs}$$

Apply KVL @ i/p loop

$$V_i = (-i_d - g_m V_{gs}) r_d + V_o$$

$$\text{But } V_o = +i_L R_L'$$

$$V_o = -i_d R_L'$$

$$V_i = -V_{gs}$$

$$-V_{gs} = -(i_d - g_m V_{gs}) r_d - i_d R_L'$$

$$+V_{gs} = \left[(i_d - g_m V_{gs}) r_d + i_d R_L' \right]$$

$$\therefore V_{gs} = i_d r_d - g_m V_{gs} r_d + i_d R_L'$$

$$V_{gs} + g_m V_{gs} r_d = i_d r_d + i_d R_L'$$

$$V_{gs} [1 + g_m r_d] = i_d [r_d + R_L']$$

From above

$$\frac{V_{gs}}{i_d} = R_i = \frac{(r_d + R_L')}{[1 + g_m r_d]}$$



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$$R_i = \frac{(r_d + r_L')}{(1 + g_m r_d)}$$

Voltage gain (A_v)

$$A_v = \frac{V_o}{V_i} = \infty$$

$$\frac{i_L r_L'}{-V_{gs}} = \frac{+i_d r_L'}{+V_{gs}}$$

$$A_v = \frac{i_d r_L'}{V_{gs}} \left[\because \frac{V_{gs}}{i_d} = \frac{(r_d + r_L')}{(1 + g_m r_d)} \right]$$

$$\therefore A_v = \frac{1 + g_m r_d}{(r_d + r_L')} \cdot r_L' \quad r_d > r_L' \text{ \& } g_m r_d \gg 1$$

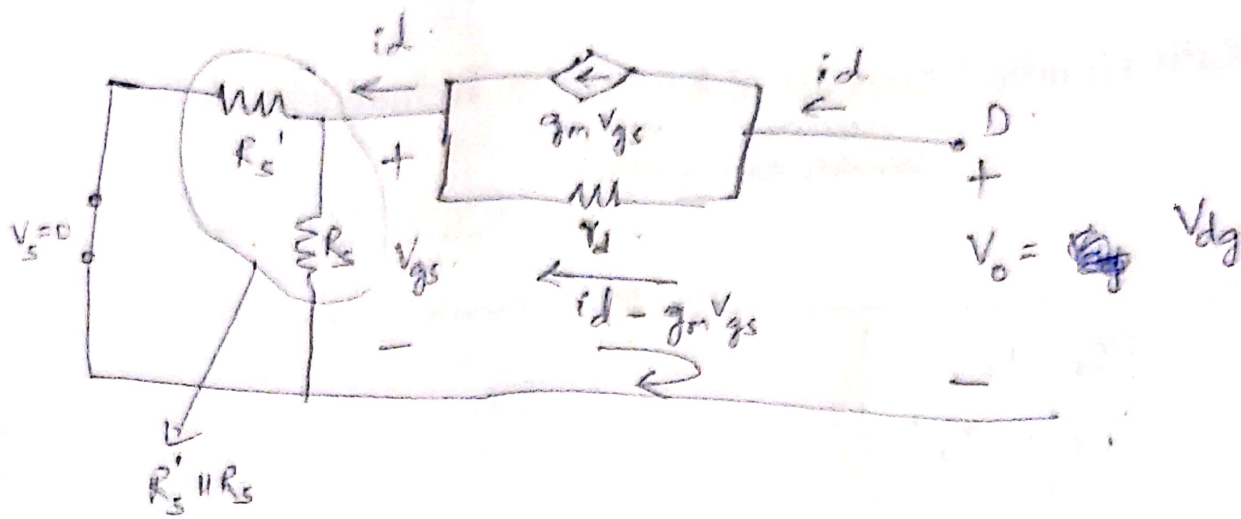
$$\approx \frac{g_m r_d \cdot r_L'}{r_d}$$

$$A_v = g_m r_L'$$

o/p resistance

$$R_o = \frac{V_o}{i_o} \Big|_{V_s = 0}$$

$\{ R_L' \text{ is disconnected.}$



$$\therefore V_o = [i_d - g_m V_{gs}] r_d + i_d (R_s' \parallel R_s)$$

From the ckt,

$$-V_{gs} = i_d [R_s' \parallel R_s]$$

$$\therefore V_o = i_d [r_d + (R_s' \parallel R_s)] + g_m (r_d i_d (R_s' \parallel R_s))$$

$$V_o = i_d [r_d + (R_s' \parallel R_s) + g_m r_d (R_s' \parallel R_s)]$$

$$\boxed{\frac{V_o}{i_d} = R_o = r_d + (R_s' \parallel R_s) + g_m r_d (R_s' \parallel R_s)}$$