Date 13/9/22

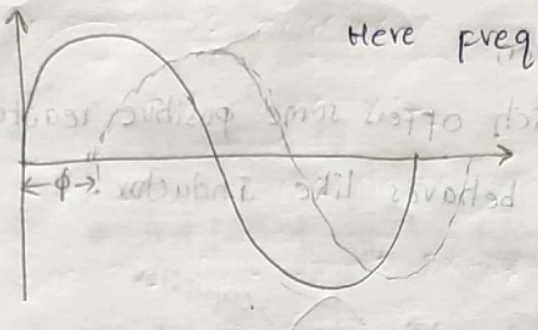
Unit 5:- Phase Locked Loop

* Introduction:-

⇒ PLL is a circuit which detects phase of two signals and reduce the phase difference and gives constant phase.

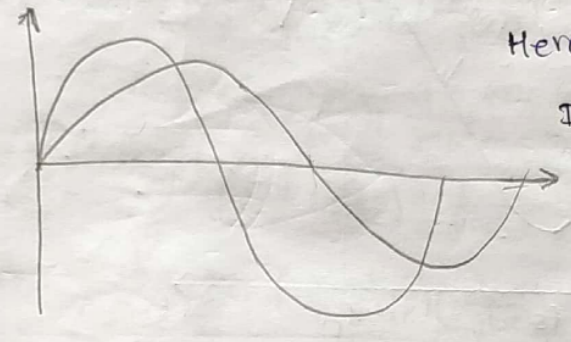
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*



Here frequency is constant for both signals. If it passes through PLL, it gives constant phase.

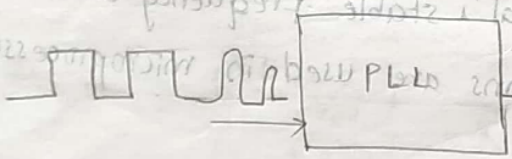
*



Here frequency is different. If it passes through PLL, it gives constant phase

⇒ Generally PLL is used in communication engineering Eg:- synchronization and demodulation like FM demodulation, FSK, AM detectors etc.

⇒ It is used for recovery of clock signals.



⇒ It is used for frequency synthesisor.

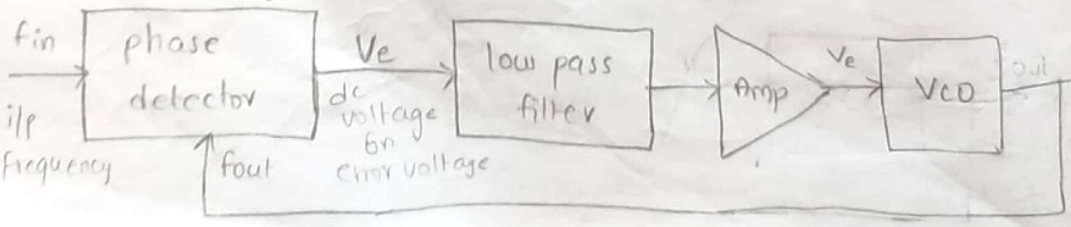
⇒ PLL consists of three major Blocks.

1) A phase detector

2) A Low pass filter

3) A Voltage controlled oscillator [VCO]

* Block diagram of PLL:-



⇒ Here phase detector has two inputs [fin & fout]. Then the output of phase dector is proportional to phase difference of inputs.

⇒ Here Olp is a dc voltage / error error voltage.

⇒ This dc voltage is given to Low pass filter [Low pass filter eliminates high frequency noise] Hence olp of Low pass filter is dc voltage.

⇒ The olp frequency change [Δf_{out}] is the function of dc i/p voltage.

$$\Delta f_{out} = f(\text{dc voltage}).$$

Here fout changes inaccordance with i/p voltage.

⇒ PLL goes through following 3 states.

1) Free running mode — without any i/p frequency [fin], PLL is operated in free running mode.
2) capture mode — The olp frequency of VCO changes in according to i/p frequency. Then PLL is operated in capture mode.
3) Lock mode — If $f_{in} = f_{out}$, Then PLL will be in Locked mode.

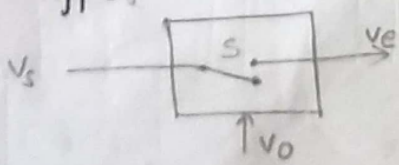
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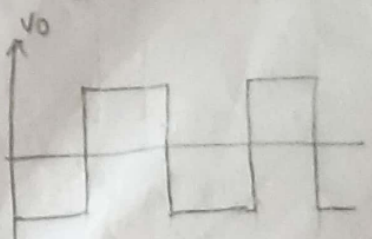
I. Phase detector:- (P.D)

⇒ phase detectors are of two types.

1) Analog phase detectors
   - switch type
   - Balance modulator.
2) Digital phase detectors
   - EX-OR
   - Edge trigger
   - monolithic P.D

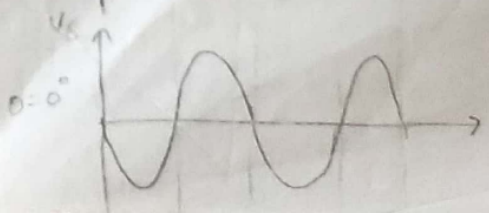
⇒ switch type:-





There are 3 cases;-

a) if $\theta = 0^\circ$, i/p & olp both are in phase

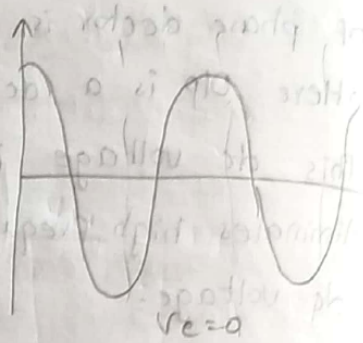


b) if $\theta = 90°$,

we have +ve portion half part and -ve portion half part.

Hence error signal is zero.

⇒ It is a perfect log condition.



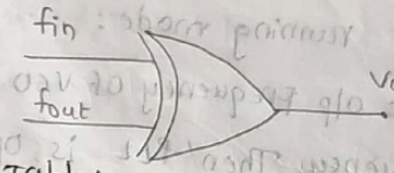
c) if $\theta = 180°$,

error signal is negative.

⇒ Digital phase detector:-

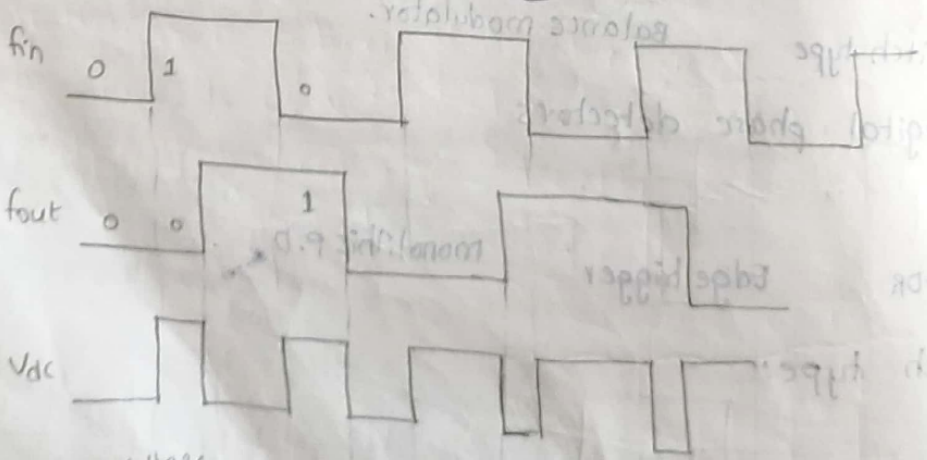
1. Exclusive-OR phase detector:-

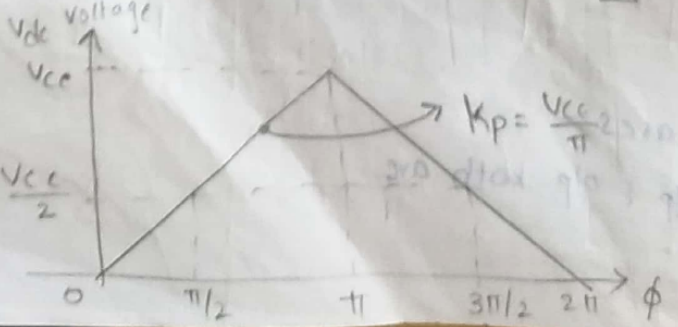
For fin and fout i/p to EX-OR gate Then produce o/p, proportional to phase(ϕ) difference of two inputs.



Truth Table:-

I/p's		o/p
fin	fout	Vdc
0	0	0
0	1	1
1	0	1
1	1	0





when $\phi = \pi$, maximum $V_{dc} = V_{cc}$

conversion
conventional gain $K_p = \frac{V_{cc}}{\pi}$, $V_{cc} = 5V$

$$\therefore \boxed{K_p = \frac{5}{\pi} = 1.6 \text{ v/rad.}}$$

⇒ It is only used for i/p having 50% duty cycle only.

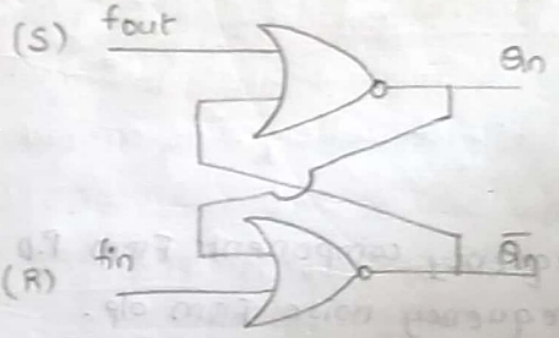
⇒ Linearity from 0 to 2π phase we are using.

⇒ For i/p having less than 50% duty cycle, go for Edge triggering.

2) Edge triggered P.D:-

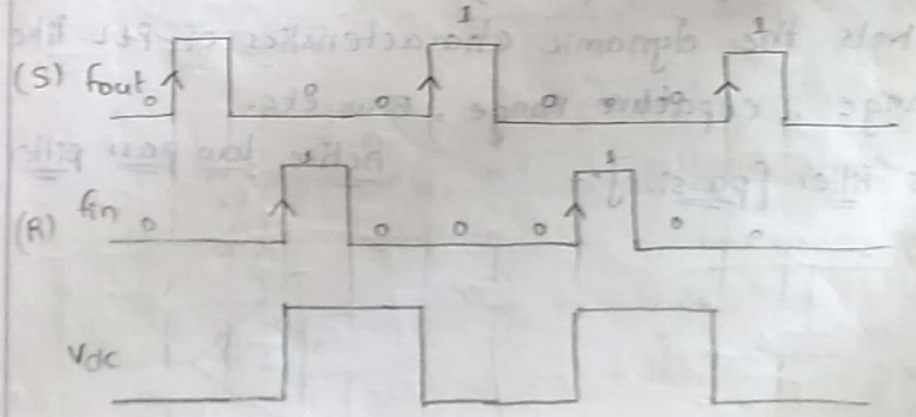
⇒ For linearity 0 to 2π. and

For i/p having less than 50% duty cycle

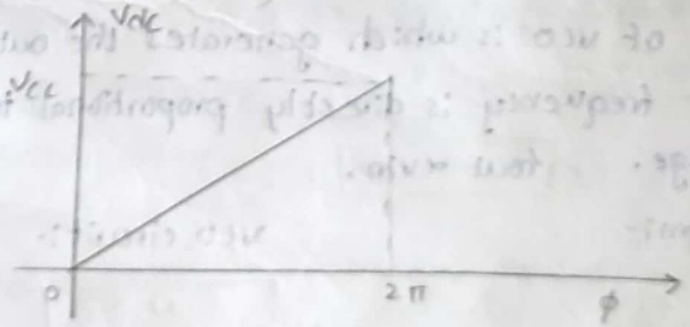


Truth Table:-

I/p's S	I/p's R	o/p's θn
0	0	θn [previous state]
0	1	1
1	0	0
1	1	X [Invalid]



Transfer characteristics:-



conversion gain $K_p = \frac{V_{cc}}{2\pi}$, $V_{cc} = 5V$

$$\therefore \boxed{K_p = \frac{5}{2\pi} = 0.8 \text{ v/rad}}$$

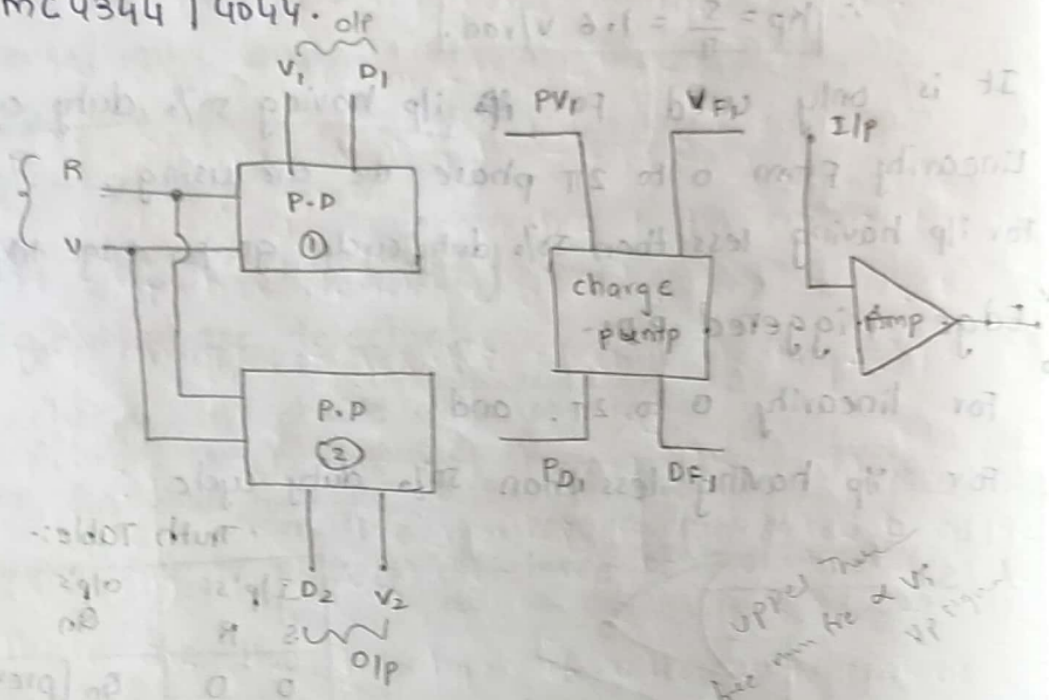
⇒ To improve the conversion gain, we go for monolithic (IC form) phase detector.

3. Monolithic (IC form) phase detector:-

⇒ Available directly in the market in the form of IC.

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MC4344 | 4044.

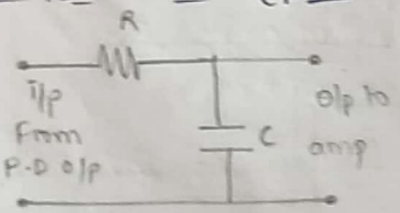


II. Low pass filter:-

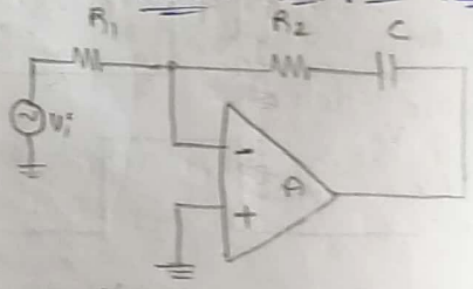
⇒ It removes high frequency components from P.D and also removes high frequency noise from olp.

⇒ It controls the dynamic characteristics of PLL like Lock Range, capature Range, B.w etc.

Low pass filter [passive]:-



Active low pass filter:-



* Voltage controlled oscillator (VCO):-

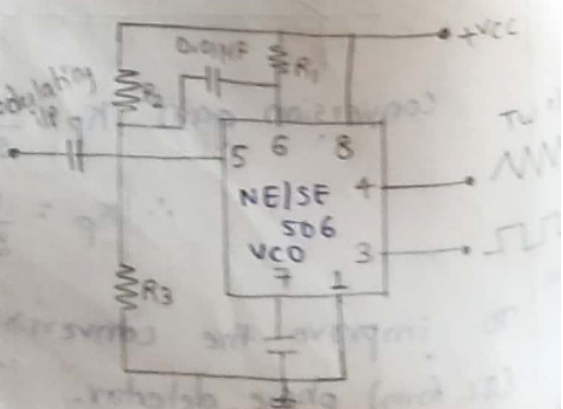
⇒ The principle of VCO is which generates the output frequency

⇒ that output frequency is directly proportional to the input signal voltage. fout ∝ vin.

⇒ Pin diagram:-



VCO circuit:-



⇒ This VCO circuit which produces two output signals.

① square wave output signal.

② Triangular wave output signal.

⇒ These two outputs are produced for the input of modulating signal.

⇒ So, This VCO which produces the frequency which is proportional to the input signal (Vin).

$f_{out} \propto V_{in}$ ***

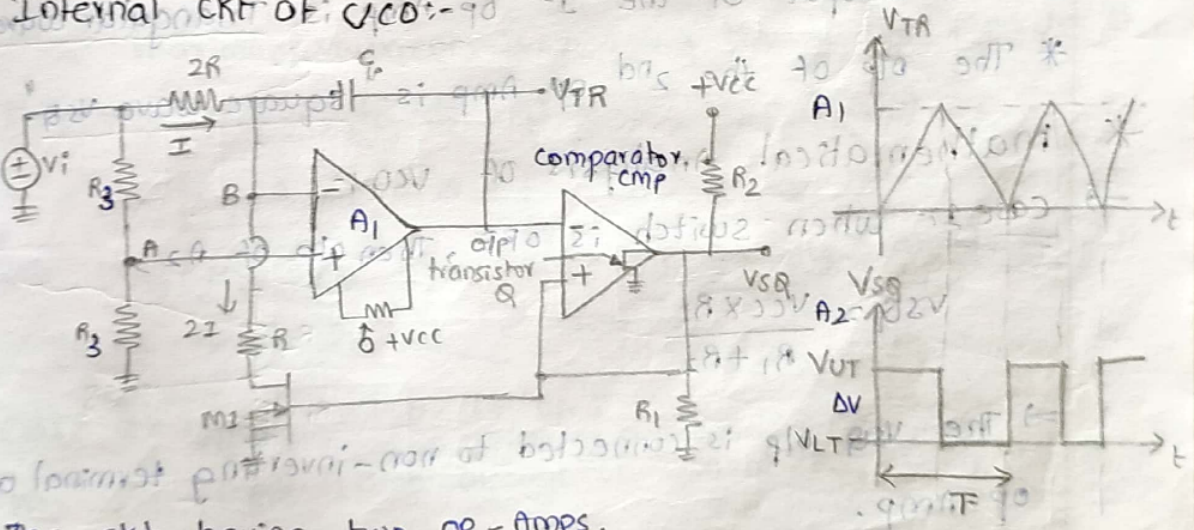
we can say clearly it is an oscillator circuit. Because it producing frequency ($f_{out} \propto V_{in}$).

⇒ This output frequency is controlled by input voltage. So, we can also called it as voltage to frequency converter.

⇒ So, the triangular wave and square wave output frequency is controlled by the input of VCO circuit. and

⇒ Triangular wave frequency (TWF) and square wave frequency of oscillation depending on the input voltage.

⇒ Internal CKT of VCO:-



⇒ The ckt having two op-Amps.

⇒ The op-Amp (A_1) acts as voltage to current converter circuit.

There are two types of voltage to current converter

1) Floating load

2) Grounded load

⇒ So, the capacitor 'c' charges which is proportional to the input voltage Vin.

⇒ To obtain the TWS and SWS, the capacitor must be charge and discharge.

⇒ So, the direction of current passing through the capacitor is controlled by MOSFET switch (M1).

⇒ The switch is driven smitttrigger comparator ckt.

⇒ The op-Amp ② is a comparator (CMP) (smitttrigger).

⇒ The schmittrigger output is always ± Vsat.

(20) If o/p is +Vsat = High - logic 1

If o/p is -Vsat = Low - logic 0

⇒ The switch 'M1' is connected to the output of 'CMP'.

If CMP has o/p - logic '0' then the switch becomes 'open' (or) OFF, so resistor 'R' will floating. ⇒ Floating load.

⇒ Suppose, if o/p of CMP - logic-1, then M1 is ON/switch is closed, Then the resistor is connected to ground.

⇒ Grounded load.

⇒ These are the two types of voltages to current converters.

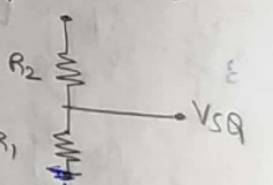
* The output of the 1st op-Amp is "Triangular wave V_{TR}"

* The o/p of the 2nd op-Amp is "square wave V_{SQ}".

* Mathematical Analysis of VCO :-

⇒ Case 1:- when switch is OFF, Then o/p of A_2,

$$V_{SQ} = \frac{V_{CC} \times R_1}{R_1 + R_2}$$



⇒ The V_{SQ} o/p is connected to non-inverting terminal of op-Amp.

⇒ This Op-Amp o/p having high and low values.

⇒ This High and low values are Threshold voltages.

∴ High - upper Threshold point

Low - Lower Threshold point

⇒ Find the voltage @ node 'A'.

$$V_A = \frac{V_{in} \cdot R_3}{R_3 + R_3} = \frac{V_{in} R_3}{2R_3}$$

$$\therefore \boxed{V_A = \frac{V_{in}}{2}}$$

But here due to virtual ground concept

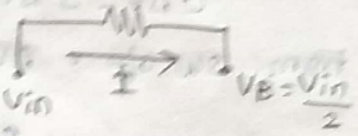
$$\therefore \boxed{V_B = V_A = \frac{V_{in}}{2}}$$

(10)

∴ The current passing through '2R',

$$I = \frac{V_i - V_B}{2R} = \frac{V_i - \frac{V_i}{2}}{2R}$$

$$= \frac{V_i\left(\frac{2-1}{2}\right)}{2R} = \frac{V_i}{4R}.$$



$$\therefore \boxed{I = \frac{V_i}{4R}} \quad ***$$

$\boxed{I \propto V_i}$ This op-Amp [A1] is voltage-current converter.

⇒ 1st op-Amp is V to C converter.

⇒ when square wave is low, Then the switch opens and Resistor (R_1) is floating, so remove the resistor.

⇒ so, the entire current, "I" is passing through capacitor because of the resistor (R_1) is removed.

Now, The o/p is 'V_{TR}' (amplitude decreases).

charging current $I = C.\frac{dv}{dt}$

⇒ The maximum current is passing through the capacitor then this V_{TR} starts to decreasing.



$\boxed{V_{TR} \text{ goes upto } 0}$

⇒ when $\boxed{V_{TR} = 0}$ *, Then comparator changes its state to High or logic -1, Then switch becomes "ON".

⇒ Case 2:- when switch is "ON".

⇒ M1 → ON, The same amount of current is passing through "R".

$$\therefore I_R = \frac{V_B}{R} = \frac{\frac{V_{in}}{2}}{R} \rightarrow I_R = \frac{V_{in}}{2R} \times \frac{2}{2}$$

$$= \frac{2V_{in}}{4R}$$

$$\therefore \boxed{I_R = 2I} \quad ** \qquad \left[\because I = \frac{V_{in}}{4R}\right].$$

⇒ now, The supply to the current 2I, The capacitor current is reversed.

so, The o/p "V_{TR} is Ramp up".



⇒ In these way, it produce TRW [Triangular wave] and SW [square wave].

* Frequency of oscillations:-

$C\Delta V = I\Delta t$

from sw o/p, $\Delta V = V_{UT} - V_{LT}$ and

$$I = \frac{V_{in}}{4R}$$

$$\rightarrow C[V_{UT} - V_{LT}] = \frac{V_{in}}{4R}[\Delta t] \qquad \Delta t = \frac{T_{o/p}}{2}\left[\begin{array}{c}\text{Half Time period}\\ \text{in square wave}\\ \text{o/p}\end{array}\right]$$

$$C[V_{UT} - V_{LT}] = \frac{V_{in}}{4R}\left[\frac{T}{2}\right]$$

$$\rightarrow T = \frac{4RCx2[V_{UT} - V_{LT}]}{V_{in}}$$

$$\therefore \boxed{f_{out} = \frac{1}{T} = \frac{V_{in}}{8Rc[V_{UT} - V_{LT}]}}$$

In VCO o/p frequency (or) free-running frequency".

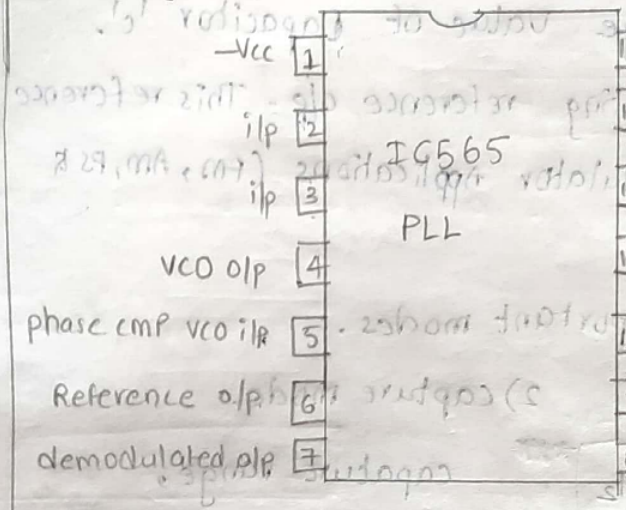
* Features of 566 VCO:-

1. Wide voltage range 10v to 24v
2. High temperature stability.
3. Excellent power supply rejection ratio.
4. Very linear modulation characteristics.
5. o/p frequency can be controlled by means of current, voltage, resistor, capacitor.

* Applications of VCO:-

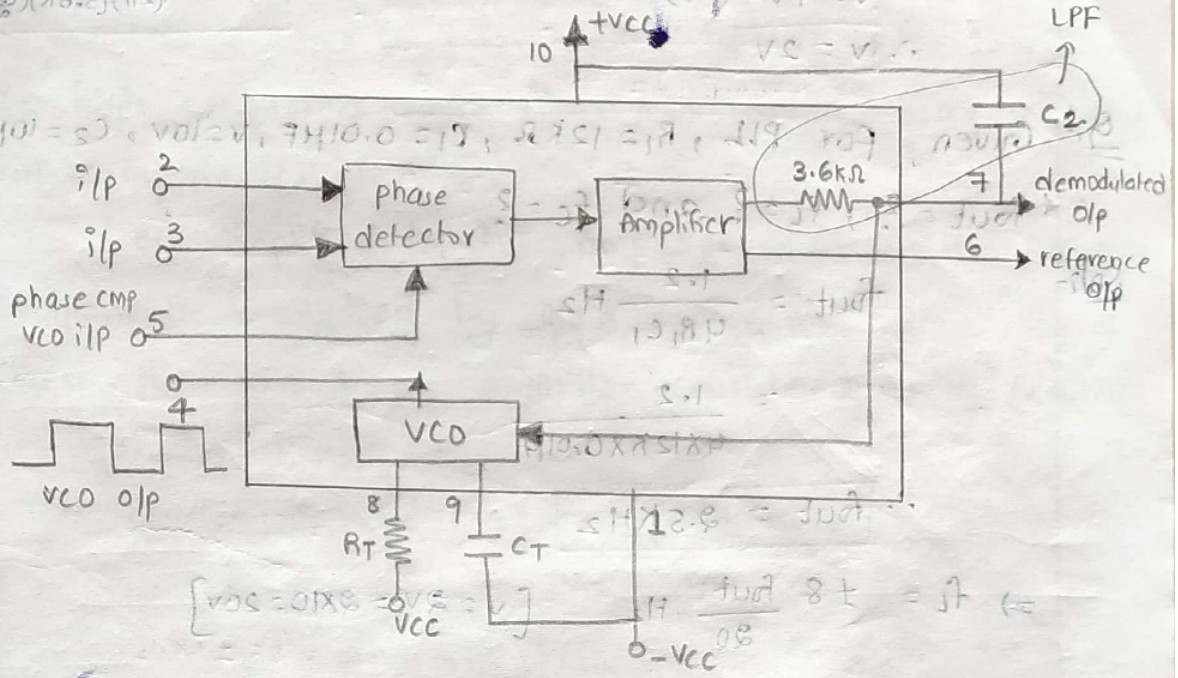
1. Fm/am modulation/demodulation
2. FSK Generation
3. Signal Generation
4. Frequency multiplier
5. Frequency translator
6. Tone generation
7. Frequency synthesizer
8. converting EEG, EKG, into Audio Frequency signals. (used in Biomedic engineering).

* pindiagram of 565 PLL:-



Generally used IC's are:-
IC 555
IC 565
IC 566
IC 7809

* Internal structure of IC565 PLL [also called monolithic PLL].



→ signetics SE/NE 560 series IC.

→ It is available in 14-pin DIP package [dual inline package].

→ The important "electrical characteristics" are:-

a) operating frequency range:- 0.001 Hz to 500 KHz [max F.R].

b) operating voltage Range:- ±6V to ±12 V.

c) Input impedance:- 10 KΩ

d) square wave output amplitude:- 5.4 volts (p-p) @ ±6V (max)

Here centre frequency of VCO $f_{out} = \frac{1.2}{4R_1C_1}$ Hz.

*** V.V.V.Imp

This fout is function of externally connected R,C.

→ In the ckt, 3.6KΩ and C forms a low pass filter and 'C' should be large enough.

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⇒ To make the VCO o/p frequency stable, Then we have to connect the large value of capacitor 'C'.

⇒ At 6 pin, is for getting reference o/p. This reference o/p is useful for demodulator applications (FM, AM, PS & demodulators).

⇒ PLL having two important modes.

*** V.V.Imp

1) Lock mode 2) capture mode.

Lock range, $f_L = \pm \frac{8 f_{out}}{V} H_z$ ***

where $V = +V - (-V)$

$\therefore V = 2V$

capature range, $f_C = \pm \sqrt{\frac{f_L}{(2\pi)(3.6K)(C_2)}} H_z$ **

Q:- Given for PLL, $R_1 = 12K\Omega$, $C_1 = 0.01\mu F$, $V = 10V$, $C_2 = 10\mu F$, $f_{out} = ?$, $f_L = ?$ and $f_C = ?$

Soln:-

$$f_{out} = \frac{1.2}{4R_1C_1} H_z$$

$$= \frac{1.2}{4 \times 12K \times 0.01\mu}$$

$\therefore f_{out} = 2.5KH_z$

$\Rightarrow f_L = \pm 8 \frac{f_{out}}{20} H_z \quad [V = 2V = 2 \times 10 = 20V]$

$= \pm 8 \frac{2.5K}{20} H_z$

$\therefore f_L = \pm 1KH_z$

$f_L = \pm 1KH_z$

High = 2.5K + 1K = 3.5K

Low = 2.5K - 1K = 1.5K

$\Rightarrow f_C = \pm \sqrt{\frac{f_L}{(2\pi)(3.6K)(C_2)}} H_z$

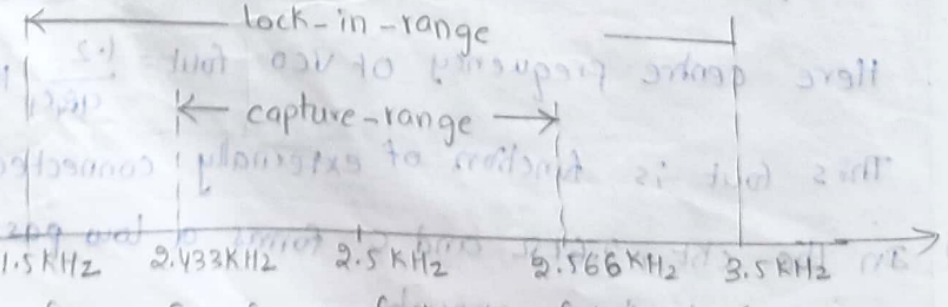
$= \pm \sqrt{\frac{\pm 1K}{(2\pi)(3.6K)(10 \times 10^{-6})}} H_z$

$\therefore f_C = \pm 66.5 H_z$

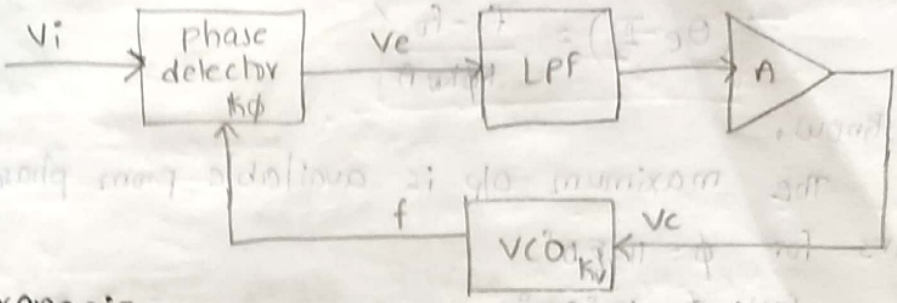
$f_C = \pm 66.5 H_z$

High = 2.5K + 66.5 = 2.566K

Low = 2.5K - 66.5 = 2.433K



* Derivation of Lock Range:-



Lock range:- It is defined as range of frequencies, PLL is lock with the incoming signals.

⇒ The output voltage of phase detector is given by "Error voltage".

$$\therefore \boxed{Ve = K\phi\left(\theta - \frac{\pi}{2}\right)} \longrightarrow (1)$$

⇒ This error voltage (Ve) is applied to 'LPF' (LPF to remove the high frequency noise signal/components). After removing H.F components,

i.e., Amplified by the Amplifier ⇒ means low frequency components multiplied by Gain factor 'A'.

⇒ Then the output of Amplifier considered as 'Vc' (control voltage).

⇒ The carrier voltage (Vc) is applied to "VCO".

$$Vc = A.Ve$$

$$\therefore \boxed{Vc = AK\phi\left(\theta - \frac{\pi}{2}\right)} \longrightarrow (2)$$

⇒ once Vc is passing through VCO, then O/p frequency is free running frequency (fout α Vc).

So, there is a shift in the VCO frequency from its centre frequency (or free-running frequency.

⇒ New/shifted frequency ⇒ fo to New frequency 'f'.

fo to f.

$$\therefore \boxed{f = fo + Vc.Kv} \longrightarrow (3)$$ where Kv = Conversion gain factor.

⇒ If PLL is locked to the input signal frequency (fi).

⇒ when VCO frequency (f) and incoming frequency (fi), both are equal, Then the PLL is locked.

$$f = fi = fo + Vc.Kv$$

$$\Rightarrow fi = f = fo + K\phi Kv A\left(\theta e - \frac{\pi}{2}\right)$$

$$\Rightarrow f_i - f_0 = K\phi K_v A\left(\theta_e - \frac{\pi}{2}\right)$$

$$\Rightarrow \boxed{\left(\theta_e - \frac{\pi}{2}\right) = \frac{f_i - f_0}{K\phi K_v A}}$$

we know,

The maximum o/p is available from phase detector occurs for $\phi = \pi$ (or) $\phi = 180° \pm 0°$.

If $\phi = 180°$, Then V_e = -ve error

If $\phi = 0°$, Then V_e = +ve error.

$$\boxed{V_e(max) = \pm K\phi\left(\frac{\pi}{2}\right)}$$

$V_e \rightarrow$ After multiplying with 'A'.

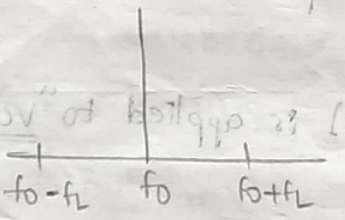
$$\boxed{V_c(max) = \pm K\phi\left(\frac{\pi}{2}\right)A}$$

Now, $f = f_i = f_0 \pm K_v K\phi\left(\frac{\pi}{2}\right)A$

$$= f_0 \pm \Delta f_L$$

$$\Rightarrow f_i - f_0 = \pm K_v K\phi\left(\frac{\pi}{2}\right)A$$

Let



For locked Range

$B.W = f_0 + f_L - f_0 + f_L$

$= 2f_L$

For lock range

$2\Delta f_L$ will be lock in Range

i.e., given by lock range $= 2\Delta f_L = K_v K\phi A\pi$

$$\boxed{\Delta f_L = K_v K\phi A \cdot \frac{\pi}{2}}$$

For PLL 565, The value of $K_v = \frac{8f_0}{V}$

where $V = +V_{CC} - (-V_{CC})$

$V = 2V_{CC}$

Similarly, for a PLL 565 $K\phi = \frac{1.4}{\pi}$ and $A = 1.4$

substitute these values in Δf_L,

$$\Rightarrow \Delta f_L = \pm 8\frac{f_0}{V} \times \frac{1.4}{\pi} \times 1.4 \times \frac{\pi}{2}$$

$$\therefore \boxed{\Delta f_L = \pm 7.84\frac{f_0}{V}}$$

This is "Lock Range".

* Derivation of capture Range:-

⇒ capture range is also range of frequencies which the PLL can acquire the lock with the input signal.

⇒ But here PLL is not initially locked to the i/p signal. Then frequency of VDC will be free running frequency 'f_0'.

So, the phase angle difference between the i/p signal and VCO o/p is

$$\theta_c = (\omega_i t + \theta_i) - (\omega_0 t + \theta_0)$$

$$\theta_c = (\omega_i - \omega_0)t + \Delta\theta \quad \text{where } \Delta\theta = \theta_i - \theta_0$$

This difference is not constant but it will changes with time.

Let $\phi = \omega t + \theta$

$$\frac{d\phi}{dt} = \omega + \theta$$

$$\Rightarrow \boxed{\frac{d\theta_c}{dt} = (\omega_i - \omega_0)}$$

The phase is converted into Fundamental Frequency. Frequency.

⇒ The phase detector [PD] o/p will be not only the dc component, it will have some AC component.

⇒ Here AC voltage with TRW of PK Amplitude is

$$\boxed{\text{Amplitude} = K_\phi\left(\frac{\pi}{2}\right)}$$

⇒ $f_i - f_0 = \Delta f$ [Δf = fundamental frequency].

⇒ The Approximate expression for the capture range for PLL. i.e., derived by using "Log filter".

⇒ $\boxed{F(j\omega) = \frac{1}{1+j\omega\tau_1}}$ transfer function of log filter.

⇒ $F(j\omega) = \frac{1}{1+j\left(\frac{\omega}{\omega_1}\right)}$ $\left[\because \tau_1 = R_1C,\ \omega_1 = \frac{1}{R_1C} = \frac{1}{\tau_1},\ f_1 = \frac{1}{2\pi R_1C}\right]$

⇒ $F(f) = \frac{1}{1+j\left(\frac{f}{f_1}\right)}$

when $\frac{f}{f_1} >> 1$, Then

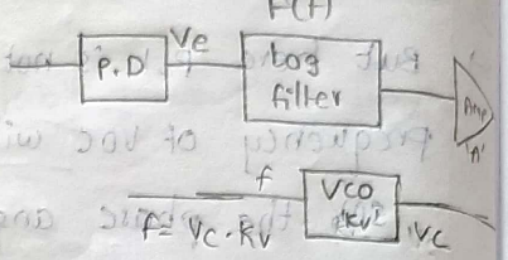
⇒ $F(f) = \frac{1}{j\left(\frac{f}{f_1}\right)} = \frac{f_1}{j(f)}$

$\therefore \boxed{F(f) = \frac{f_1}{jf}}$.

This Fundamental Frequency is applied to LPF, Then

$\Delta f = f_i - f_0$ if $\Delta f > 3f_1$, Then Transfer function of LPF will be approximately,

$$F(\Delta f) = \frac{f_1}{\Delta f} = \frac{f_i}{f_i - f_0}$$



$\Rightarrow$ voltage available at VCO,

$$V_c = V_e \cdot A \cdot F(\Delta f)$$

$$\Rightarrow V_{c(max)} = V_{e(max)} F(\Delta f) A$$

$$V_{c(max)} = \pm K_\phi \left(\frac{\pi}{2}\right) \times \frac{f_1}{\Delta f} \times A$$

$\Rightarrow$ maximum frequency shifting,

$$f_i - f_0 = K_v V_{c(max)}$$

$$\Rightarrow (f_i - f_0)_{max} = \pm K_v K_\phi \left(\frac{\pi}{2}\right) \times \frac{f_1}{\Delta f} \times A \qquad (\because \Delta f = f_i - f_0)$$

$$\Rightarrow (f_i - f_0)_{max} = \pm K_v K_\phi \left(\frac{\pi}{2}\right) A \frac{f_1}{\Delta f_{cap}}$$

Here $\Delta f_{cap} = (f_i - f_0)_{max}$

$$\Rightarrow \Delta f_{cap} = \pm K_v K_\phi \left(\frac{\pi}{2}\right) A \frac{f_1}{\Delta f_{cap}}$$

$$\Rightarrow (\Delta f_{cap})^2 = \pm \underbrace{K_v K_\phi \left(\frac{\pi}{2}\right) A}_{\Delta f_L} f_1$$

$$\Rightarrow (\Delta f_{cap})^2 = \pm \Delta f_L \cdot f_1$$

$$\Rightarrow \Delta f_{cap} = \pm \sqrt{\Delta f_L \cdot f_1}$$

$$\therefore \Delta f_{cap} = \pm \sqrt{\frac{\Delta f_L}{2\pi R_1 C}} \qquad \left(\because f_1 = \frac{1}{2\pi R_1 C}\right)$$

For 565 PLL, $R = 3.6 K\Omega$

$$\therefore \boxed{\Delta f_{cap} = \pm \left[\frac{\Delta f_L}{2\pi \times 3.6K \times C}\right]^{1/2}} \quad *** \text{ V.V. Imp}$$

This is called "capture range".