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2

OPERATIONAL AMPLIFIER

2.1 INTRODUCTION

Linear integrated circuits are being used in a number of electronic applications such as in fields like audio and radio communication, medical electronics, instrumentation control, etc. An important linear IC is operational amplifier which will be discussed in this chapter.

The operational amplifier (commonly referred to as op-amp) is a multi-terminal device which internally is quite complex. Fortunately, for the ordinary user, it is not necessary to know about the op-amp's internal make-up. The manufacturers have done their job so well that op-amp's performance can be completely described by its terminal characteristics and those of external components that are connected to it. However, for the designer's interest, the electronics of op-amp is described where the various stages of op-amp are discussed. Then some of the FET op-amps are described. The dc and ac characteristics with compensating techniques and the various applications of op-amp are taken up later.

2.2 BASIC INFORMATION OF OP-AMP

Circuit Symbol

The circuit schematic of an op-amp is a triangle as shown in Fig. 2.1. It has two input terminals and one output terminal. The terminal with a (–) sign is called inverting input terminal and the terminal with (+) sign is called the non-inverting input terminal.

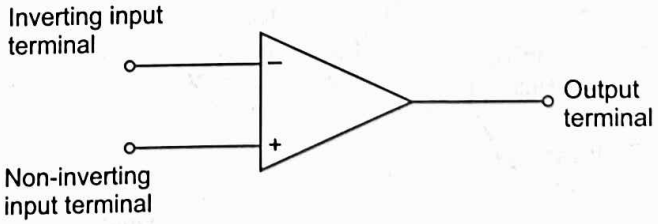


Fig. 2.1 Op-amp circuit symbol

Packages

There are three popular packages available:

1. The metal can (TO) package
2. The dual-in-line package (DIP)
3. The flat package or flat pack

Op-amp packages may contain single, two (dual) or four (quad) op-amps. Typical packages have 8 terminals (the can and the DIP or MINI DIP), 10 terminals (flatpacks and some cans) and 14 terminals (the DIP and the flat pack). The widely used very popular type, for example μA741 is a single op-amp and is available as an 8-pin can, an 8-pin DIP, a 10-pin flatpack or a 14-pin DIP. The μA747 is a dual 741 and comes in either a 10-pin can or a 14-pin DIP. Figure 2.2 shows the various IC packages along with the top view of connection diagram.

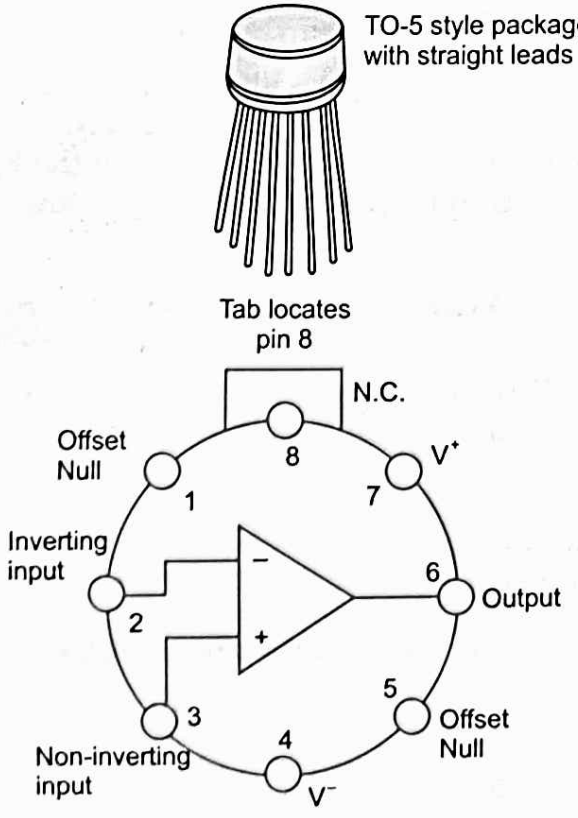
Op-Amp Terminals

Op-amps have five basic terminals, that is, two input terminals, one output terminal and two power supply terminals. The significance of other terminals varies with the type of the op-amp.

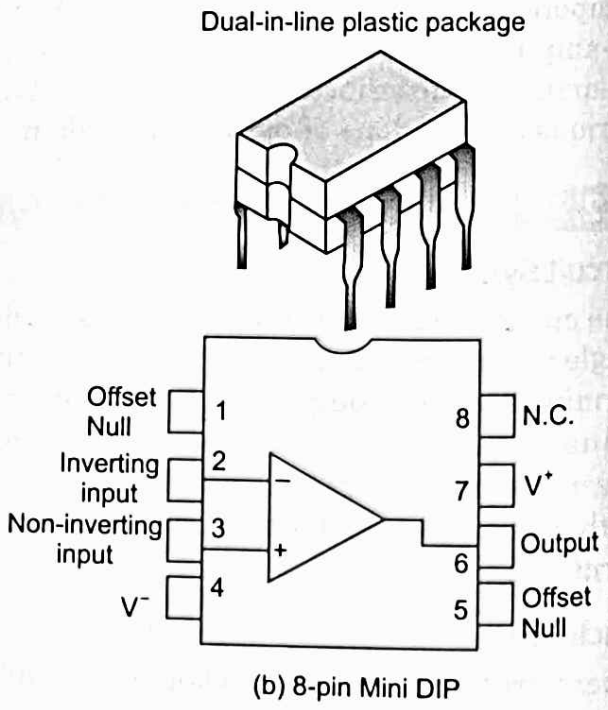
Refer to the top view of a metal can package (μA741) in Fig. 2.2 (a). The metal can has eight pins with pin number 8 identified by a tab. The other pins are numbered counter-clockwise from pin 8, beginning with pin 1. Pin 2 is called the inverting input terminal and pin 3 is the non-inverting input terminal, pin 6 is the output terminal and pins 7 and 4 are the power supply terminals labelled as V^+ and V^- respectively. Terminals 1 and 5 are used for dc offset. The pin 8 marked NC indicates 'No Connection'. In case of DIP package of 741 as in Fig. 2.2 (b, c), the top pin on the left of the notch locates pin 1, and the flat pack of Fig. 2.2 (d) has a dot on it for identification. The other pins are numbered counter-clockwise from pin 1. The pin numbers have been illustrated only for some popular op-amps and the user should consult the manufacturer's data sheet before connecting a given op-amp into a circuit.

Power Supply Connections

The V^+ and V^- power supply terminals are connected to two dc voltage sources. The V^+ pin

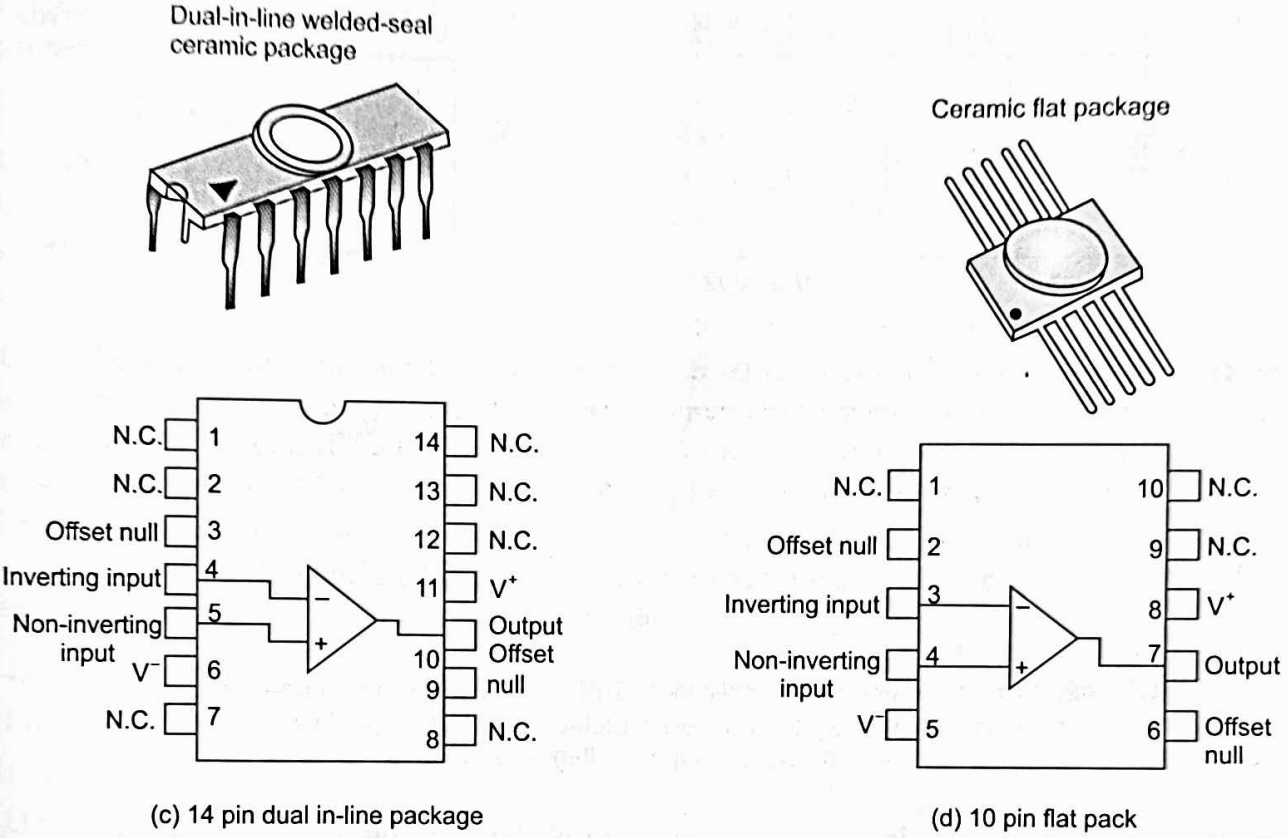


(a) 8-pin Metal can



(b) 8-pin Mini DIP

(Fig. 2.2 Contd.)

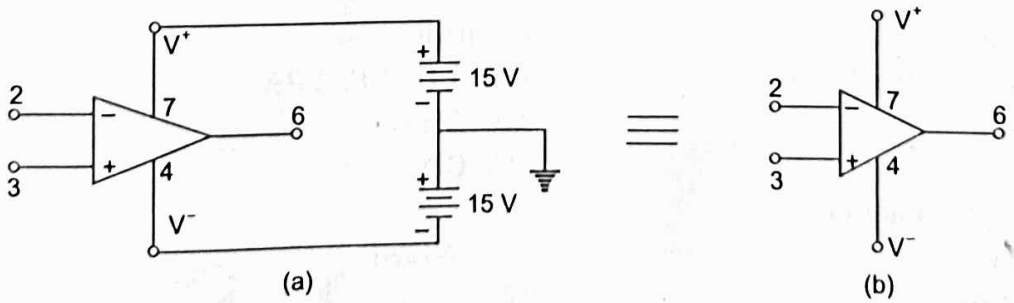


(c) 14 pin dual in-line package

(d) 10 pin flat pack

Fig. 2.2 (a, b, c, d) Various IC packages of $\mu A741$ op-amp along with connection diagrams (top view)

is connected to the positive terminal of one source and the V^- pin is connected to the negative terminal of the other source as illustrated in Fig. 2.3 (a) where the two sources are 15 V batteries each. These are typical values, but in general, the power supply voltage may range from about ±5 V to ±22 V. The common terminal of the V^+ and V^- sources is connected to a reference point or ground. Some op-amps have a ground terminal, but most do not. The ground is simply a convenient point on the circuit bread-board to which the op-amp is connected through the power supplies. The equivalent representation of Fig. 2.3 (a) is given in Fig. 2.3 (b). The common point of the two supplies must be grounded, otherwise twice the supply voltage will get applied and it may damage the op-amp. Instead of using two power



(Fig. 2.3 Contd.)

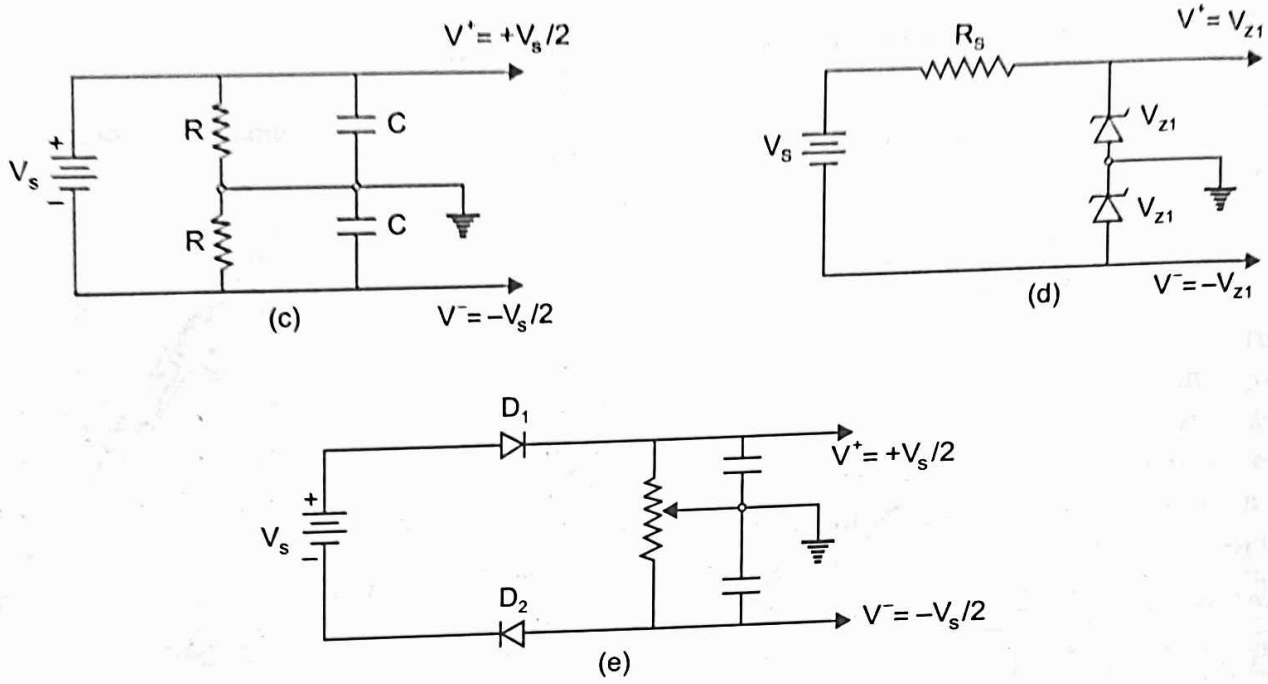


Fig. 2.3 (a) Power supply connections, (b) Circuit symbol showing power supply terminals (c, d, e) Different circuits for obtaining positive and negative supply voltages for op-amp

supplies, one can use a single power supply to obtain V^+ and V^- as shown in circuits of Fig. 2.3 (c, d, e). In Fig. 2.3 (c), resistor R should be greater than 10 kΩ so that it does not draw more current from the supply V_s. The two capacitors provide decoupling of the power supply and range in value from 0.01 to 10 μF. In the circuit of Fig. 2.3 (d), zener diodes are used to give symmetrical supply voltages. The value of the resistor R_s is chosen such that it supplies sufficient current for the zener diodes to operate in the avalanche mode. In Fig. 2.3 (e), potentiometer is used to get equal values of V^+ and V^-. Diodes D_1 and D_2 protect the IC if the positive and negative leads of the supply voltage V_s are accidentally reversed. These diodes can also be connected in the circuits of Fig. 2.3 (c) and 2.3 (d).

Manufacturer's Designation for Linear ICs

Each manufacturer uses a specific code and assigns a specific type number to the ICs produced. For example, 741 an internally compensated op-amp originally manufactured by Fairchild is sold as μA741. Here μA represents the identifying initials used by Fairchild. The codes used by some of the well-known manufacturers of linear ICs are:

1.	Fairchild	μA, μAF
2.	National Semiconductor	LM, LH, LF, TBA
3.	Motorola	MC, MFC
4.	RCA	CA, CD
5.	Texas Instruments	SN
6.	Signetics	N/S, NE/SE
7.	Burr-Brown	BB

A number of manufacturers also produce popular ICs of the other manufacturers. For easy use, they usually retain the original type number of the IC alongwith their identifying

initials. For example, Fairchild's original μA741 is also manufactured by other manufacturers as follows:

1.	National Semiconductor	LM741
3.	Motorola	MC1741
4.	RCA	CA3741
5.	Texas Instruments	SN52741
6.	Signetics	N5741

It may be noted that the last three digits in each manufacturer's designation are 741. All these op-amps have the same specifications. Since a number of manufacturers produce the same IC, one can refer to such ICs by their type number only and delete manufacturer's identifying initials. For example, μA741 or MC1741 may simple be referred as 741.

Some linear ICs are available in different classes such as A, C, E, S and SC. For example 741, 741A, 741C, 741E, 741S and 741SC are different versions of the same op-amp. The main difference of these op-amps are:

741	Military grade op-amp (Operating temperature range –55° to 125°C)	
741C	Commercial grade op-amp (Operating temperate range 0° to 70°/75°C)	
741A	Improved version of 741	Better electrical specifications
741E	Improved version of 741C	
741S	Military grade op-amp with higher slew-rate	
741SC	Commercial grade op-amp with higher slew-rate	

2.3 THE IDEAL OPERATIONAL AMPLIFIER

The schematic symbol of an op-amp is shown in Fig. 2.4 (a). It has two input terminals and one output terminal. Other terminals have not been shown for simplicity. The – and + symbols at the input refer to inverting and non-inverting input terminals respectively, i.e. if $v_1 = 0$, output v_o is 180° out of phase with input signal v_2. And, when $v_2 = 0$, output v_o will be in phase with

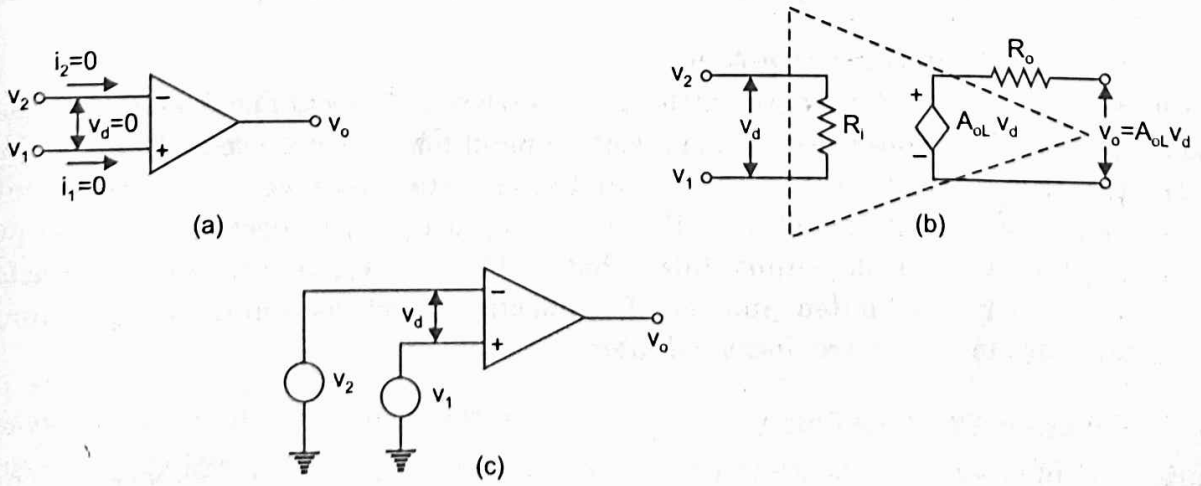


Fig. 2.4 (a) Ideal op-amp, (b) Equivalent circuit of an op-amp (c) Open loop circuit

the input signal applied at v_1. This op-amp is said to be ideal if it has the following characteristics.

Open loop voltage gain,	A_{OL}	=	∞
Input impedance,	R_i	=	∞
Output impedance	R_o	=	0
Bandwidth	BW	=	∞

Zero offset, *i.e.* $v_o = 0$ when $v_1 = v_2 = 0$.

It can be seen that

(i) an ideal op-amp draws no current at both the input terminals *i.e.*, $i_1 = i_2 = 0$. Because of infinite input impedance, any signal source can drive it and there is no loading on the preceding driver stage.

(ii) Since gain is ∞, the voltage between the inverting and non-inverting terminals, *i.e.*, differential input voltage $v_d = (v_1 - v_2)$ is essentially zero for finite output voltage v_o.

(iii) The output voltage v_o is independent of the current drawn from the output as $R_o = 0$. The output thus can drive an infinite number of other devices.

The above properties can never be realized in practice. However, the use of such an 'Ideal op-amp' model simplifies the mathematics involved in op-amp circuits. There are practical op-amps that can be made to approximate some of these characteristics.

A physical amplifier is not an ideal one. So, the equivalent circuit of an op-amp may be shown in Fig. 2.4 (b) where $A_{OL} \neq \infty$, $R_i \neq \infty$ and $R_o \neq 0$. It can be seen that op-amp is a voltage controlled voltage source and $A_{OL}\, v_d$ is an equivalent *Thevenin* voltage source and R_o is the *Thevenin* equivalent resistance looking back into the output terminal of an op-amp. The equivalent circuit is useful in analyzing the basic operating principles of op-amp. For the circuit shown in Fig. 2.4 (b), the output voltage is

$$v_o = A_{OL}\, v_d$$
$$= A_{OL}\, (v_1 - v_2) \qquad (2.1)$$

The equation shows that the op-amp amplifies the difference between the two input voltages.

2.3.1 Open Loop Operation of Op-Amp

The simplest way to use an op-amp is in the open loop mode. Refer to Fig. 2.4 (c) where signals v_1 and v_2 are applied at non-inverting and inverting input terminals respectively. Since the gain is infinite, the output voltage v_o is either at its positive saturation voltage $(+V_{sat})$ or negative saturation voltage $(-V_{sat})$ as $v_1 > v_2$ or $v_2 > v_1$ respectively. The output assumes one of the two possible output states, that is, $+V_{sat}$ or $-V_{sat}$ and the amplifier acts as a switch only. This has a limited number of applications such as voltage comparator, zero crossing detector etc. which are discussed later.

2.3.2 Feedback in Ideal Op-Amp

The utility of an op-amp can be greatly increased by providing negative feedback. The output in this case is not driven into saturation and the circuit behaves in a linear manner.

Two Important Negative Feedback Circuits

There are two basic feedback connections used. In order to understand the operation of these circuits, we make two realistic simplifying assumptions discussed earlier also:

1. The current drawn by either of the input terminals (non-inverting and inverting) is negligible.
2. The differential input voltage v_d between non-inverting and inverting input terminals is essentially zero.

2.3.3 The Inverting Amplifier

This is perhaps the most widely used of all the op-amp circuits. The circuit is shown in Fig. 2.5 (a). The output voltage v_o is fed back to the inverting input terminal through the $R_f - R_1$ network where R_f is the feedback resistor. Input signal v_i (ac or dc) is applied to the inverting input terminal through R_1 and non-inverting input terminal of op-amp is grounded.

Analysis: For simplicity, assume an ideal op-amp. As $v_d = 0$, node 'a' is at ground potential and the current i_1 through R_1 is

$$i_1 = \frac{v_i}{R_1} \tag{2.2}$$

Also since op-amp draws no current, all the current flowing through R_1 must flow through R_f. The output voltage,

$$v_o = -i_1 R_f = -v_i \frac{R_f}{R_1} \tag{2.3}$$

Hence, the gain of the inverting amplifier (also referred as closed loop gain) is,

$$A_{CL} = \frac{v_o}{v_i} = -\frac{R_f}{R_1} \tag{2.4}$$

Alternatively, the nodal equation at the node 'a' in Fig. 2.5 (a) is

$$\frac{v_a - v_i}{R_1} + \frac{v_a - v_o}{R_f} = 0$$

where v_a is the voltage at node 'a'. Since node 'a' is at virtual ground $v_a = 0$. Therefore, we get,

$$A_{CL} = \frac{v_o}{v_i} = -\frac{R_f}{R_1}$$

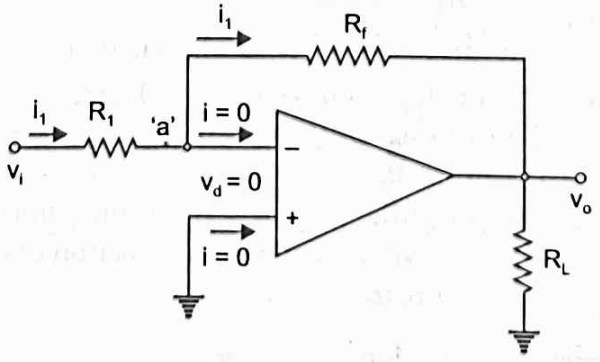


Fig. 2.5 (a) Inverting amplifier

The negative sign indicates a phase shift of 180° between v_i and v_o. Also since inverting input terminal is at virtual ground, the effective input impedance is R_1. The value of R_1 should be kept fairly large to avoid loading effect. This however, limits the gain that can be obtained from this circuit. A load resistor R_L is usually put at the output in actual practice otherwise, the

input impedance of the measuring device such as oscilloscope or DVM acts as the load. The calculation of load and output currents is shown in the Example 2.2.

If, however, resistances R_1 and R_f in Fig. 2.5 (a) are replaced by impedances Z_1 and Z_f respectively, then the voltage gain, A_{CL} will be

$$A_{CL} = -\frac{Z_f}{Z_1} \tag{2.5}$$

This expression for the voltage gain will be used in op-amp applications, such as integrator, differentiator etc.

Example 2.1

Design an amplifier with a gain of –10 and input resistance equal to 10 kΩ.

Solution

Since the gain of the amplifier is negative, an inverting amplifier has to be made.

In Fig. 2.5 (a) choose $R_1 = 10$ kΩ

Then $R_f = -A_{CL} R_1$ (from Eq. 2.4)

$= -(-10) \times 10$ kΩ $= 100$ kΩ

Example 2.2

In Fig. 2.5 (b), $R_1 = 10$ kΩ, $R_f = 100$ kΩ, $v_i = 1$ V. A load of 25 kΩ is connected to the output terminal. Calculate (i) i_1 (ii) v_o (iii) i_L and (iv) total current i_o into the output pin.

Solution

(i) $i_1 = \frac{v_i}{R_1} = \frac{1\text{ V}}{10\text{ k}\Omega} = 0.1\text{ mA}$

(ii) $v_o = -\frac{R_f}{R_1} v_i = -\frac{100\text{ k}\Omega}{10\text{ k}\Omega} 1\text{ V} = -10\text{ V}$

(iii) $i_L = \frac{v_o}{R_L} = \frac{10\text{ V}}{25\text{ k}\Omega} = 0.4\text{ mA}$

The direction of i_L is shown in Fig. 2.5 (b).

(iv) i_1 as calculated above is 0.1 mA. Therefore, total current $i_o = i_1 + i_L =$ 0.1 mA + 0.4 mA = 0.5 mA. In an inverting amplifier, for a +ive input, output will be –ive, therefore the direction of i_o is as shown in Fig. 2.5 (b).

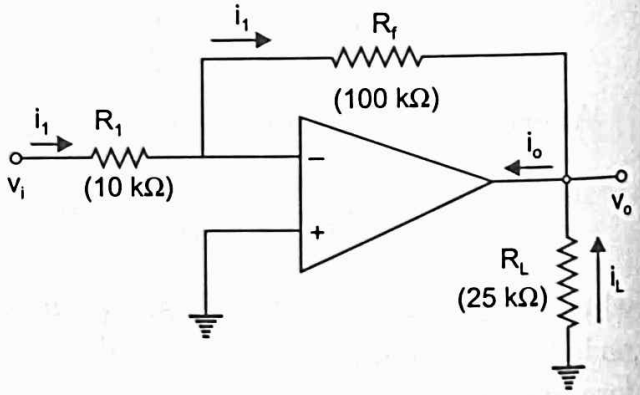


Fig. 2.5 (b) Circuit for Example 2.2

Practical Inverting Amplifier

Equation (2.4) is valid only if the op-amp is an ideal one. For a practical op-amp, the expression for the closed loop voltage gain should be calculated using the low frequency model of Fig. 2.4 (b). The equivalent circuit of a practical inverting amplifier is shown in Fig. 2.6 (a). This circuit can be simplified by replacing the signal source v_i and resistors R_1 and R_i by Thevenin's equivalent as shown in Fig. 2.6 (b) which is analysed to calculate the exact expression for closed loop gain, A_{CL} and input impedance R_{if}.

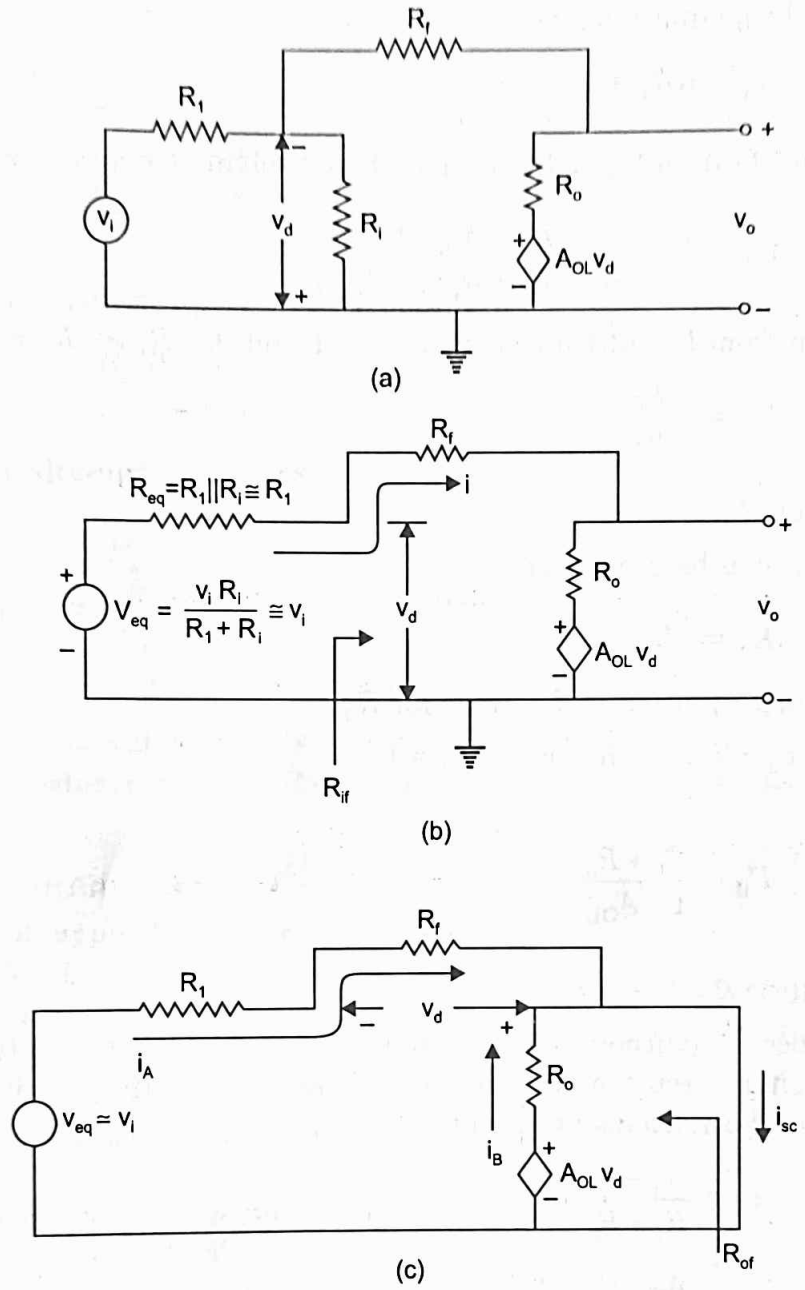


Fig. 2.6 (a) Equivalent circuit of a practical op-amp inverting amplifier, (b) Simplified circuit by using Thevenin's equivalent (c) Equivalent circuit for computing R_{of}

The input impedance R_i of an op-amp is usually much greater than R_1, so one may assume, $v_{eq} \cong v_i$ and $R_{eq} \cong R_1$.

From the output loop in Fig. 2.6 (b)

$$v_o = iR_o + A_{OL}\, v_d \tag{2.6}$$

Also

$$v_d + iR_f + v_o = 0 \tag{2.7}$$

Putting the value of v_d from Eq. (2.6) to Eq. (2.7) and simplifying,

$$v_o(1 + A_{OL}) = i(R_o - A_{OL}\, R_f) \tag{2.8}$$

Also the KVL loop equation gives

$$v_i = i(R_1 + R_f) + v_o \tag{2.9}$$

Putting the value of i from Eq. (2.8) in Eq. (2.9) and solving for closed loop gain $A_{CL} = \frac{v_o}{v_i}$, gives

$$A_{CL} = \frac{v_o}{v_i} = \frac{R_o - A_{OL} R_f}{R_o + R_f + R_1 (1 + A_{OL})} \tag{2.10}$$

It can be seen from Eq. (2.10) that if $A_{OL} >> 1$ and $A_{OL} R_1 >> R_o + R_f$, and neglecting R_o,

$$A_{CL} \cong -\frac{R_f}{R_1}.$$

Input Resistance R_{if}

In Fig. 2.6 (b), it can be seen that

$$R_{if} = \frac{v_d}{i}$$

Writing the loop equation and solving for R_{if},

$$v_d + i (R_f + R_o) + A_{OL} v_d = 0$$

We obtain

$$R_{if} = \frac{R_f + R_o}{1 + A_{OL}} \tag{2.11}$$

Output Resistance R_{of}

Output impedance R_{of} (without load resistance R_L) is calculated from the open circuit output voltage v_{oc} and short circuit output circuit i_{sc}. Now consider the circuit shown in Fig. 2.6 (c). Under short circuit conditions at output,

$$i_A = \frac{v_i - 0}{R_1 + R_f} \tag{2.12}$$

and,

$$i_B = \frac{A_{OL} v_d}{R_o} \tag{2.13}$$

Since, $v_d = - i_A R_f$

So, $i_B = -\frac{A_{OL} i_A R_f}{R_o}$

Solving for $i_{sc} = i_A + i_B$, we obtain

$$i_{sc} = i_A + i_B = v_i \frac{(R_o - A_{OL} R_f)}{R_o (R_1 + R_f)} \tag{2.14}$$

Since,

$$R_{of} = \frac{v_{oc}}{i_{sc}}$$

and $$A_{CL} = \frac{v_{oc}}{v_i}$$

Therefore, $$R_{of} = \frac{A_{CL}\, v_i}{v_i \left[(R_o - A_{OL}\, R_f) / R_o (R_1 + R_f) \right]} \tag{2.15}$$

Putting the value of A_{CL} from Eq. (2.10), we obtain

$$R_{of} = \frac{R_o (R_1 + R_f)}{R_o + R_f + R_1 (1 + A_{OL})} \tag{2.16}$$

Equation (2.16) may alternatively be written as

$$R_{of} = \frac{\dfrac{R_o (R_1 + R_f)}{R_o + R_1 + R_f}}{1 + \dfrac{R_1 A_{OL}}{R_o + R_1 + R_f}} \tag{2.17}$$

It may be seen that numerator consists of a term $R_o \parallel (R_1 + R_f)$ and is therefore smaller than R_o. The output resistance R_{of} (with feedback) is, therefore always less than R_o and for $A_{CL} \to \infty$, $R_{of} \to 0$.

2.3.4 The Non-inverting Amplifier

If a signal (ac or dc) is applied to the non-inverting input terminal and feedback is given as shown in Fig. 2.7 (a), the circuit amplifies without inverting the input signal. Such a circuit is called non-inverting amplifier. It may be noted that it is also a negative feedback system as output is being fed back to the inverting input terminal.

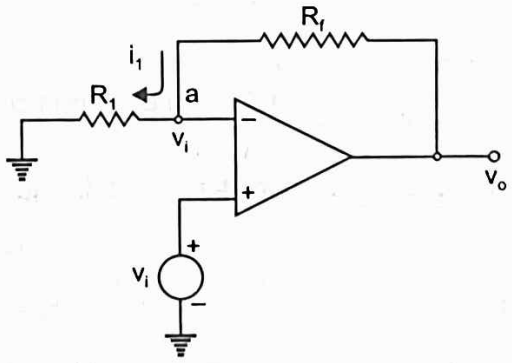


Fig. 2.7 (a) Non-inverting amplifier

As the differential voltage v_d at the input terminal of op-amp is zero, the voltage at node 'a' in Fig. 2.7 (a) 5is v_i, same as the input voltage applied to non-inverting input terminal. Now R_f and R_1 forms a potential divider. Hence

$$v_i = \frac{v_o}{R_1 + R_f} R_1 \tag{2.18}$$

as no current flows into the op-amp.

$$\frac{v_o}{v_i} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1} \tag{2.19}$$

Thus, for non-inverting amplifier the voltage gain,

$$A_{CL} = \frac{v_o}{v_i} = 1 + \frac{R_f}{R_1} \tag{2.20}$$

The gain can be adjusted to unity or more, by proper selection of resistors R_f and R_1. Compared to the inverting amplifier, the input resistance of the non-inverting amplifier is extremely large (= ∞) as the op-amp draws negligible current from the signal source.

Practical Non-inverting Amplifier

The analysis of a practical non-inverting amplifier can be performed by using the equivalent circuit shown in Fig. 2.7 (b). Writing KCL at the input node,

$$(v_i - v_d)\, Y_1 + v_d Y_i + (v_i - v_d - v_o) Y_f = 0$$

or,
$$-(Y_1 + Y_i + Y_f)\, v_d + (Y_1 + Y_f)\, v_i = Y_f v_o \tag{2.21}$$

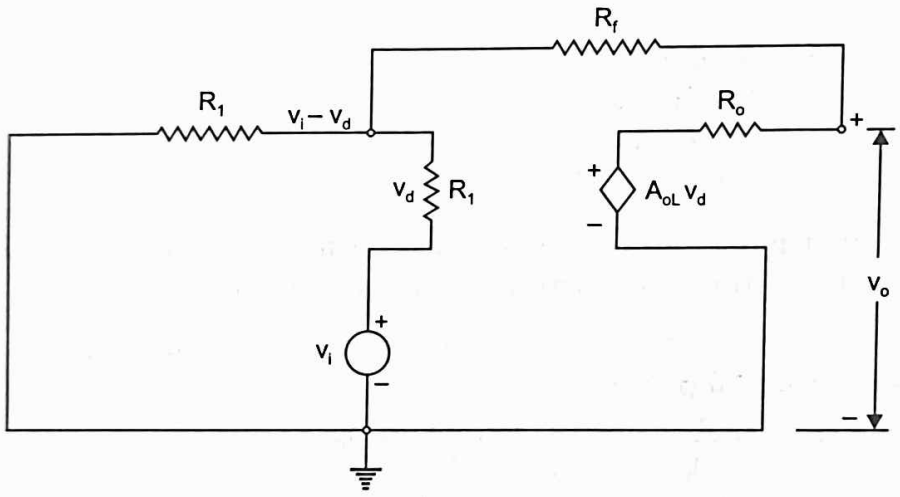


Fig. 2.7 (b) Equivalent circuit of non-inverting amplifier using low frequency model

Similarly at output node, KCL gives

$$(v_i - v_d - v_o) Y_f + (A_{OL}\, v_d - v_o) Y_o = 0$$

that is,
$$-(Y_f - A_{OL}\, Y_o)\, v_d + Y_f v_i = (Y_f + Y_o)\, v_o \tag{2.22}$$

Now solving Eqs. (2.21) and (2.22) for v_o/v_i, we get

$$A_{CL} = \frac{v_o}{v_i} = \frac{A_{OL} Y_o (Y_1 + Y_f) + Y_f Y_i}{(A_{OL} + 1) Y_o Y_f + (Y_1 + Y_i)(Y_f + Y_o)} \tag{2.23}$$

where all admittances have been taken for simplicity.

If $A_{OL} \to \infty$, Eq. (2.23) reduces to

$$A_{CL} \approx \frac{A_{OL} Y_o (Y_1 + Y_f)}{A_{OL} Y_o Y_f} = \frac{Y_1 + Y_f}{Y_f} = 1 + \frac{Y_1}{Y_f}$$

$$= 1 + \frac{R_f}{R_1}$$

which is the same expression as in Eq. (2.20).

2.3.5 Voltage Follower

In the non-inverting amplifier of Fig. 2.7 (a) if $R_f = 0$ and $R_1 = \infty$, we get the modified circuit of Fig. 2.7 (c). From Eq. (2.20) we get,

$$v_o = v_i \tag{2.24}$$

That is, the output voltage is equal to input voltage, both in magnitude and phase. In other words, we can also say that the output voltage follows the input voltage exactly. Hence, the circuit is called a voltage follower. The use of the unity gain circuit lies in the fact that its input impedance is very high (*i.e.*, MΩ order) and output impedance is zero. Therefore, it draws negligible current from the source. Thus a voltage follower may be used as buffer for impedance matching, that is, to connect a high impedance source to a low impedance load.

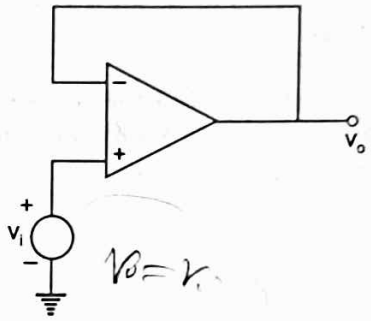


Fig. 2.7 (c) Voltage follower

Example 2.3

Design an amplifier with a gain of +5 using one op-amp.

Solution

Since the gain is positive, we have to make a non-inverting amplifier. In Fig. 2.7 (a) select R_1 = 10 kΩ. Then from Eq. (2.20)

$$A_{CL} = 1 + R_f/R_1$$

or, $$5 = 1 + R_f/10\ \text{k}\Omega$$

or, $$R_f = 4 \times 10\ \text{k}\Omega = 40\ \text{k}\Omega$$

Example 2.4

In the circuit of Fig. 2.7 (a), let R_1 = 5 kΩ, R_f = 20 kΩ and v_i = 1 V. A load resistor of 5 kΩ is connected at the output as in Fig. 2.5 (b). Calculate, (i) v_o (ii) A_{CL} (iii) the load current i_L (iv) the output current i_o indicating proper direction of flow.

Solution

(i) $$v_o = \left(1 + \frac{R_f}{R_1}\right) v_i = \left(1 + \frac{20\ \text{k}\Omega}{5\ \text{k}\Omega}\right)(1\ \text{V}) = 5\ \text{V}$$

(ii) $$A_{CL} = \frac{v_o}{v_i} = \frac{5\ \text{V}}{1\ \text{V}} = 5$$

(iii) $$i_L = \frac{v_o}{R_L} = \frac{5\ \text{V}}{5\ \text{k}\Omega} = 1\ \text{mA}$$

(iv) $$i_1 = \frac{v_i}{R_1} = \frac{v_o - v_i}{R_f} = 0.2\ \text{mA}$$

Therefore, $i_o = i_L + i_1 = 1\ \text{mA} + 0.2\ \text{mA} = 1.2\ \text{mA}$

The op-amp output current i_o flows outwards from the output junction.

Example 2.5

In the Fig. 2.7(d), calculate V_o, if $V_{in} = 1V$.

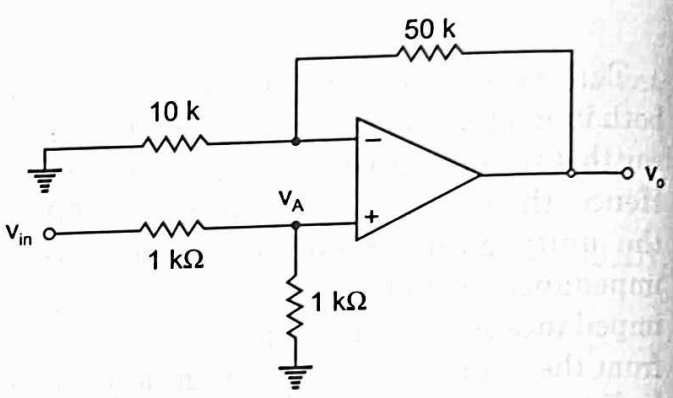


Fig. 2.7(d)

Solution

The circuit is a non-inverting amplifier. Calculating the voltage V_A at the non-inverting terminal, we get

$$V_A = \frac{1\,\text{k}\Omega}{1\,\text{k}\Omega + 1\text{k}\Omega} \times 1V$$

$$= 0.5\ V$$

Thus, output voltage V_o is

$$V_o = \left(1 + \frac{50\,\text{k}\Omega}{10\,\text{k}\Omega}\right) V_A$$

$$= 6 \times 0.5\ V$$

$$= 3.0\ V$$

2.3.6 Differential Amplifier

A circuit that amplifies the difference between two signals is called a difference or differential amplifier. This type of the amplifier is very useful in instrumentation circuits (see section 4.3). A typical circuit is shown in Fig. 2.8. Since, the differential voltage at the input terminals of the op-amp is zero, nodes 'a' and 'b' are at the same potential, designated as v_3. The nodal equation at 'a' is,

$$\frac{v_3 - v_2}{R_1} + \frac{v_3 - v_o}{R_2} = 0 \qquad (2.25)$$

and at 'b' is

$$\frac{v_3 - v_1}{R_1} + \frac{v_3}{R_2} = 0 \qquad (2.26)$$

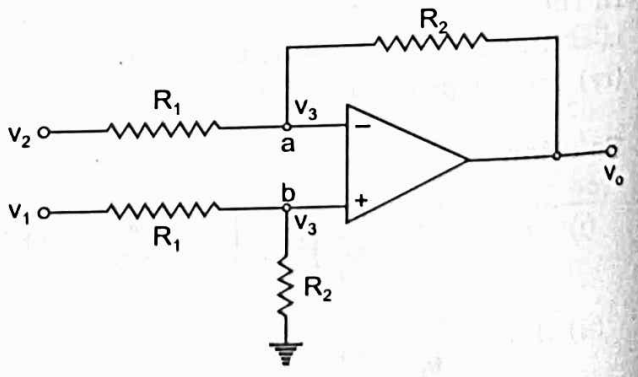


Fig. 2.8 A differential amplifier

Rearranging, we get

$$\left(\frac{1}{R_1} + \frac{1}{R_2}\right) v_3 - \frac{v_2}{R_1} = \frac{v_o}{R_2} \qquad (2.27)$$

$$\left(\frac{1}{R_1} + \frac{1}{R_2}\right) v_3 - \frac{v_1}{R_1} = 0 \qquad (2.28)$$

Subtracting Eq. (2.28) from (2.27) we get,

$$\frac{1}{R_1}(v_1 - v_2) = \frac{v_o}{R_2} \tag{2.29}$$

Therefore,

$$v_o = \frac{R_2}{R_1}(v_1 - v_2) \tag{2.30}$$

Such a circuit is very useful in detecting very small differences in signals, since the gain R_2/R_1 can be chosen to be very large. For example, if $R_2 = 100\ R_1$, then a small difference $v_1 - v_2$ is amplified 100 times.

Difference-mode and Common-mode Gains

In Eq. (2.30) if $v_1 = v_2$ then $v_o = 0$. That is, the signal common to both inputs gets cancelled and produces no output voltage. This is true for an ideal op-amp, however, a practical op-amp exhibits some small response to the common mode component of the input voltages too. For example, the output v_o will have different value for case (i) with $v_1 = 100\ \mu V$ and $v_2 = 50\ \mu V$ and case (ii) with $v_1 = 1000\ \mu V$ and $v_2 = 950\ \mu V$, even though the difference signal $v_1 - v_2 = 50\ \mu V$ in both the cases. The output voltage depends not only upon the difference signal v_d at the input, but is also effected by the average voltage of the input signals, called the common-mode signal v_{CM} defined as,

$$v_{CM} = \frac{v_1 + v_2}{2}$$

For differential amplifier, though the circuit is symmetric, but because of the mismatch, the gain at the output with respect to the positive terminal is slightly different in magnitude to that of the negative terminal. So, even with the same voltage applied to both inputs, the output is not zero. The output, therefore, must be expressed as,

$$v_o = A_1 v_1 + A_2 v_2 \tag{2.31}$$

where, A_1 (A_2) is the voltage amplification from input 1 (2) to the output with input 2(1) grounded. Since $v_{CM} = (v_1 + v_2)/2$ and $v_d = (v_1 - v_2)$,

$$v_1 = v_{CM} + \frac{1}{2}v_d \tag{2.32}$$

and

$$v_2 = v_{CM} - \frac{1}{2}v_d \tag{2.33}$$

Substituting the value of v_1 and v_2 in Eq. (2.31), we get

$$v_o = A_{DM}\, v_d + A_{CM}\, v_{CM} \tag{2.34}$$

where,

$$A_{DM} = \frac{1}{2}(A_1 - A_2) \tag{2.35}$$

and

$$A_{CM} = A_1 + A_2 \tag{2.36}$$

The voltage gain for the difference signal is A_{DM} and that for the common-mode signal is A_{CM}.

2.3.7 Common-mode Rejection Ratio

The relative sensitivity of an op-amp to a difference signal as compared to a common-mode signal is called common-mode rejection ratio (CMRR) and gives the figure of merit ρ for the differential amplifier. So, CMRR is given by:

$$\rho = \left| \frac{A_{DM}}{A_{CM}} \right| \tag{2.37}$$

and is usually expressed in decibels (dB). For example, the μA741 op-amp has a minimum CMRR of 70 dB whereas a precision op-amp such as μA725A has a minimum CMRR of 120 dB. Clearly, we should have A_{DM} large A_{CM} should be zero ideally. So, higher the value of CMRR, better is the op-amp.

Example 2.6

In Fig. 2.9 is shown a differential amplifier using ideal op-amp.

(a) Find the output voltage v_o.

(b) Show that the output corresponding to common-mode voltage

$v_{CM} = \frac{(v_1 + v_2)}{2}$ is zero if $\frac{R'}{R} = \frac{R_2}{R_1}$.

Find v_o in this case.

(c) Find CMRR of the amplifier if $\frac{R'}{R} \neq \frac{R_2}{R_1}$.

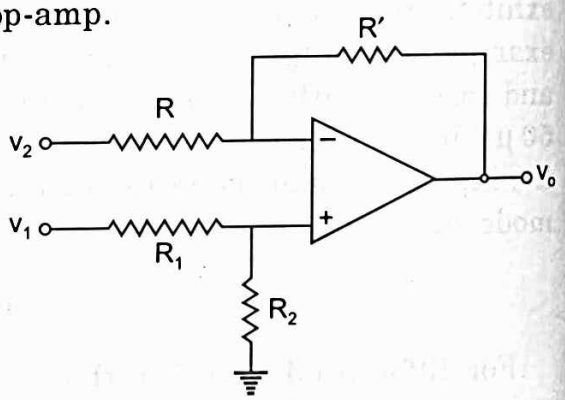


Fig. 2.9 Circuit of Example 2.6

Solution

The voltage at the non-inverting input terminal is $\frac{R_2}{R_1 + R_2} v_1$. Using principle of superposition and Eqs. (2.4) and (2.20), we have

(a) $$v_o = -\frac{R'}{R} v_2 + \left(\frac{R + R'}{R}\right)\left(\frac{R_2}{R_1 + R_2} v_1\right) \tag{2.38}$$

(b) $$v_{CM} = \frac{1}{2}(v_1 + v_2) \text{ and } v_d = (v_1 - v_2)$$

So, $$v_1 = v_{CM} + \frac{v_d}{2} \text{ and } v_2 = v_{CM} - \frac{v_d}{2}$$

v_o from Eq. (2.38) is,

$$v_o = -\frac{R'}{R}\left(v_{CM} - \frac{v_d}{2}\right) + \frac{R_2}{R}\frac{R + R'}{R_1 + R_2}\left(v_{CM} + \frac{v_d}{2}\right)$$

$$= \left(\frac{R_2}{R}\frac{R + R'}{R_1 + R_2} - \frac{R'}{R}\right) v_{CM} + \left(\frac{R'}{R} + \frac{R_2}{R}\frac{R + R'}{R_1 + R_2}\right)\frac{v_d}{2} \tag{2.39}$$

Now, if $\frac{R'}{R} = \frac{R_2}{R_1}$, we get,

$$\frac{R'}{R} + 1 = \frac{R_2}{R_1} + 1$$

or, $$\frac{R' + R}{R} = \frac{R_1 + R_2}{R_1}$$

So, from Eq. (2.39) the term corresponding to v_{CM} is zero, and

$$v_o = \left(\frac{R'}{R} + \frac{R_2}{R_1}\right)\frac{v_d}{2} = \left(\frac{R_2}{R_1}\right)v_d \tag{2.40}$$

(c) $$\text{CMRR} = \frac{A_{DM}}{A_{CM}}$$

From Eq. (2.39), find (i) $A_{DM} = v_o/v_d$ by putting $v_{CM} = 0$

and (ii) $A_{CM} = v_o/v_{CM}$ by putting $v_d = 0$

then we get

$$\text{CMRR} = \frac{R'(R_1 + R_2) + R_2(R + R')}{R'(R_1 + R_2) - R_1(R + R')} \tag{2.41}$$

2.3.8 Differential Amplifier with Two Op-Amps

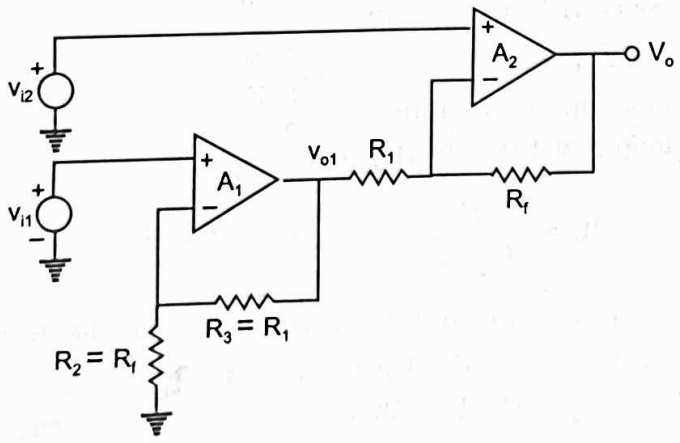


Fig 2.10 Differential amplifier with two op-amps

The circuit shown in Fig 2.10 is a differential amplifier using two op-amps. It consists of a non-inverting amplifier formed by op-amp A_1. The output V_{o1} goes to op-amp A_2 working as a differential amplifier. The advantage of this circuit is that the overall gain can be increased and the input resistance of such a circuit also increases.

The output V_{o1} of the first stage is given by

$$V_{o1} = \left(1 + \frac{R_3}{R_2}\right) V_{i1} \tag{2.42}$$

For the op-amp A_2, output V_o is given by the sum of output due to inverting input V_{o1} and non-inverting input V_{i2} as

$$V_o = -\frac{R_f}{R_1} Vo_1 + \left(1 + \frac{R_f}{R_1}\right) V_{i2}. \tag{2.43}$$

Assuming $R_3 = R_1$ and $R_2 = R_f$, we get

$$V_o = \left(1 + \frac{R_f}{R_1}\right)(V_{i2} - V_{i1}) \tag{2.44}$$

The gain of the two op-amp differential amplifier is given by

$$A_D = \frac{V_o}{V_{id}} = \left(1 + \frac{R_f}{R_1}\right) \tag{2.45}$$

where $V_{id} = V_{12} - V_{1I}$

Input Resistance

The input resistance R_i of a differential amplifier is the resistance looking into either of the two non-inverting input terminals with the other input grounded. The first stage is a non-inverting amplifier and its input resistance is

$$R_{i1} = R_i\ (1 + A\beta_1) \tag{2.46}$$

where, A $\rightarrow$ open loop gain of op-amp
R_i $\rightarrow$ open loop resistance of op-amp

$$\beta_1 = \frac{R_2}{R_2 + R_3} \tag{2.47}$$

Similarly, shorting V_{i1} input to ground, the second stage is also working as a non-inverting amplifier and its input resistance is given by

$$R_{i2} = R_i\ (1 + A\beta_2) \tag{2.48}$$

where

$$\beta_2 = \frac{R_1}{R_1 + R_f} \tag{2.49}$$

Assuming $R_1 = R_3$ and $R_1 = R_2$, we find that $R_{i1} \neq R_{i2}$. Since $R_{i1} \neq R_{i2}$ the loading of the input sources V_{i1} and V_{i2} will take place and the output signal may be less amplified.

Example 2.7

In Fig 2.10, given that $R_1 = R_3 = 560\ \Omega$, $R_f = R_2 = 5.6\ \text{k}\ \Omega$, $V_{01} = 2\text{V}$ (peak to peak), $V_{02} = 1\text{V}$ (peak to peak) $R_i = 2\ \text{M}\ \Omega$ and open loop gain $A_{0L} = 2 \times 10^5$. Determine (i) Voltage gain, (ii) input resistance, and (iii) output voltage of the differential amplifier.

Solution

Using Eq (2.45), the differential voltage gain, A_D is given by

(i) $$A_D = 1 + \frac{R_f}{R_1}$$

$$= 1 + \frac{5.6 \times 10^3}{560} = 11$$

(ii) Since $R_1 = R_3$ and $R_f = R_2$, the value of input resistance $R_{i1} = R_{i2}$ and is calculated as

$$R_{i1} = R_i \left[1 + \frac{A_{oL} R_2}{R_2 + R_3}\right]$$

$$= 2 \times 10^6 \left[1 + \frac{2 \times 10^5 \times 560}{560 + 5.6 \times 10^3}\right]$$

$$= 36.37\ \text{G}\Omega$$

So, $$R_{i1} = R_{i2} = 36.37\ \text{G}\Omega$$

(iii) The output voltage is calculated using Eq (2.45) as

$$V_o = A_D\, V_{id}$$

$$= \left(1 + \frac{R_f}{R_1}\right)(V_{o2} - V_{o1})$$

$$= 11\ (2 - 1)$$

$$= 11\ \text{V (peak to peak)}$$

Example 2.8

For the circuit shown in Fig 2.11, show that the input resistance is given by

$$R_i = \frac{R_1 R_3}{R_3 - R_1}$$

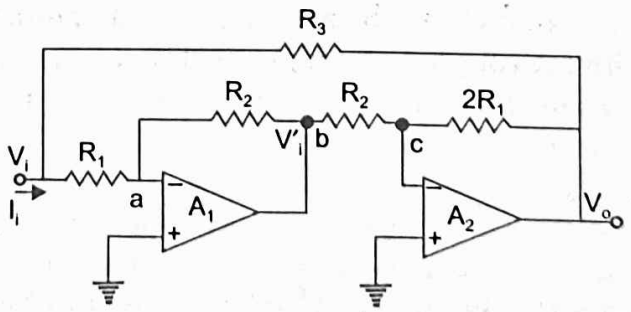


Fig. 2.11

Solution

At node 'a' of op-amp A_1, the current I_i is given by

$$\frac{V_i - 0}{R_1} = \frac{V_L' - 0}{R_2} \qquad (2.50)$$

For op-amp A_2 with input V_i' at node 'b' the current entering at node 'c' is given by

$$\frac{V_o - 0}{2R_1} = \frac{V_i' - 0}{R_2} \tag{2.51}$$

From the above equations, we get

$$\frac{V_i'}{R_2} = \frac{V_o}{2R_1}$$

or $$V_o = 2\ V_i$$

The current I_i from source V_i is given by the sum of currents through R_1 and R_3 as

$$I_i = \frac{V_i - 0}{R_1} + \frac{V_i - V_o}{R_3} \tag{2.52}$$

Substituting $V_o = 2V_i$, we get

$$I_i = \frac{V_i - 2V_i}{R_3} + \frac{V_i}{R_1}$$

$$= \frac{V_i (R_3 - R_1)}{R_1 R_3}$$

Hence, the input impedance $R_i = \dfrac{V_i}{I_i} = \dfrac{R_1 R_3}{R_3 - R_1}$

2.4 OPERATIONAL AMPLIFIER INTERNAL CIRCUIT

Commercial IC op-amps usually consists of four cascaded blocks as shown in Fig. 2.12. The first two stages are cascaded differential amplifiers and are designed to provide high gain and high input resistance. The third stage acts as a buffer as well as a level shifter. The buffer is usually an emitter follower whose input impedance is very high so that it prevents loading of the high gain stage. The level shifter adjusts the d.c. voltages so that output voltage is zero for zero inputs. The adjustment of d.c. level is required as the gain stages are direct coupled. As it is not possible to fabricate large value of capacitors, all IC's are direct coupled usually. The output stage is designed to provide a low output impedance as demanded by the ideal op-amp characteristics. The output voltage should swing symmetrically with respect to ground. To allow such symmetrical swing, the amplifier is provided with both positive and negative supply voltages. Power supply voltages of ±15 V are common. Additionally, an op-amp generally incorporates circuitry to provide drift compensation and frequency compensation which are discussed in Sec. 3.3.3.

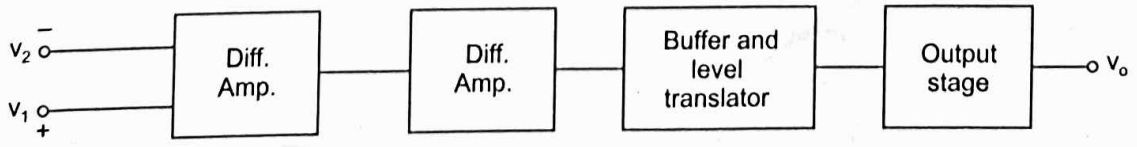


Fig. 2.12 Block schematic of an op-amp

Before describing the detailed IC circuit, we shall discuss each of the blocks in detail.

2.4.1 Differential Amplifier

The main purpose of the differential amplifier stage is to provide high gain to the difference-mode signal and cancel the common-mode signal. Thus, it is able to suppress any undesired noise which is common to both of the input terminals. The relative sensitivity of an op-amp to a difference signal as compared to common-mode signal is called common-mode rejection ratio (CMRR) and gives the figure of merit of the differential amplifier. The higher the value of CMRR, better is the op-amp. Another requisite of a good op-amp is that it should have high input impedance. In this section, we discuss in detail, the various circuits and then modifications to achieve these characteristics of a good op-amp.

A cascaded direct coupled amplifier can provide high gain down to zero frequency as it has no coupling capacitor. However, such an amplifier suffers from the major problem of drift of the operating point due to temperature dependency of I_{CO}, V_{BE} and h_{FE} of the transistor. This problem can be eliminated by using a balanced or differential amplifier as shown in Fig. 2.13 (a). It may be seen that it is essentially an emitter-coupled differential amplifier. This circuit has low drift on account of symmetrical construction. It can be designed to give high input resistance. It has two input terminals and it may be seen easily that terminal B_2 is the inverting input terminal since transistor Q_2 provides a phase shift of 180° for the output taken at the collector of Q_2. Obviously, B_1 is the non-inverting input terminal. So, a differential amplifier is well suited to obtain the ideal characteristics of an op-amp as discussed in Sec. 2.3.

A differential amplifier of the type shown in Fig. 2.13 (a) can be used in four different configurations depending upon the number of input signals used and the way output is taken. These four configurations are:

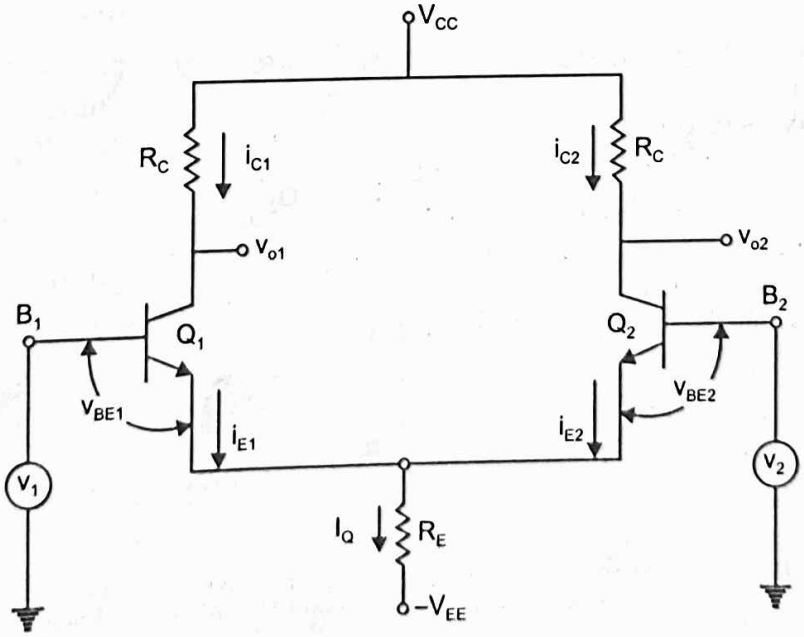


Fig. 2.13 (a) The basic differential amplifier

(i) Differential-input, differential-output or Dual-input balanced-output (ii) Differential-input, single ended-output (iii) Single-input, differential-output (iv) Single-input, single ended-output.

If signal is applied to both the inputs, then it is differential input or Dual input and the difference of signals applied to the two inputs gets amplified. In many applications a single input is only used as we shall see later. Similarly, if output voltage is measured between two collectors then it is a differential output. This is also referred to as a balanced output, as both collectors are at the same d.c. potential w.r.t. ground. We will come across these various configuration as we proceed further.

To understand the working of a differential amplifier first consider the case when both the bases B_1 and B_2 are joined together and connected to a voltage v_{CM} called the common-mode voltage. Thus in Fig. 2.13 (b), $v_1 = v_2 = v_{CM}$. As both the transistors Q_1 and Q_2 are forward-biased and matched, due to symmetry of the circuit, the current I_Q divides equally through transistors Q_1 and Q_2, that is, $i_{E1} = i_{E2} = I_Q/2$. The collector currents i_{C1} and i_{C2} through the resistors R_C is $\alpha_F I_Q/2$. The voltage at each of the collectors will be $V_{CC} - \alpha_F \frac{I_Q}{2} R_C$ and, therefore the difference of the voltage between the two collectors $(v_{o1} - v_{o2})$ will be zero. Now, even if the value of v_{CM} is changed, the voltage across the collectors will not change. Thus, the differential pair does not respond to (or rejects) the common-mode input signals. Now, consider the case when the voltage v_2 is made zero and voltage $v_1 = 1$ V (say) as shown in Fig. 2.13 (c). It can be seen that the transistor Q_1 will conduct and transistor Q_2 will be **off**. The entire current I_Q will now flow through Q_1. Since Q_1 is **on**, the voltage at its emitter will be 0.3 V. This will make emitter-base junction of Q_2 reverse-biased and thus Q_2 will be **off.** The collector voltages will be $v_{o1} = V_{CC} - \alpha_F I_Q R_C$ and $v_{o2} = V_{CC}$.

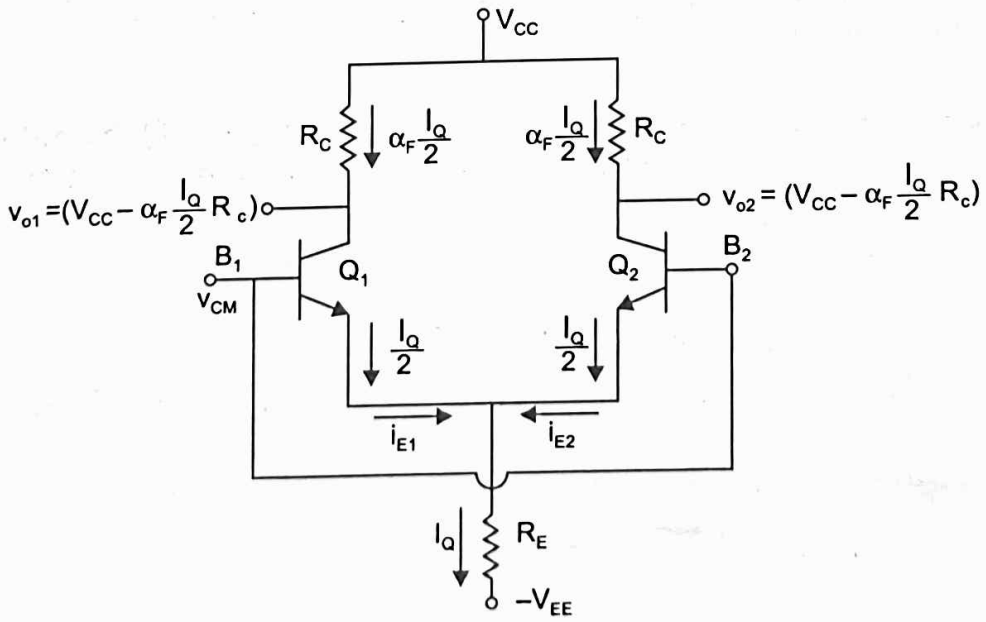


Fig. 2.13 (b) The differential pair with a common-mode input signal v_{CM}

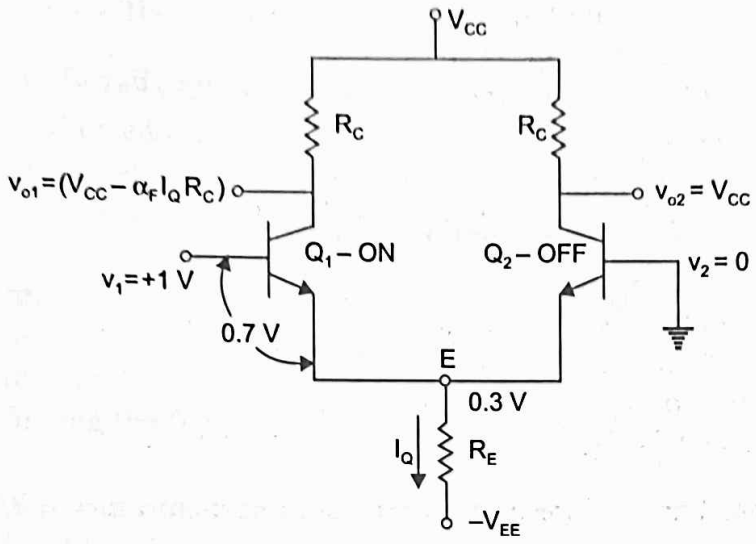


Fig. 2.13 (c) The differential pair with 'large' differential input signal

If, however, $v_1 = -1$ V and $v_2 = 0$ V, it can be seen that Q_1 will be **off** and the entire current I_Q will flow through Q_2. The voltage at the common emitter point 'E' will now be – 0.7 V which makes Q_1 **off** and Q_2 **on**. The collector voltages will be $v_{o1} = V_{CC}$ and $v_{o2} = V_{CC} - \alpha_F I_Q R_C$.

Thus, we see that the differential pair responds only to the difference mode signals and rejects common-mode signals. In the next section, we discuss the transfer characteristics of the circuit to show that a differential pair can be used either as a switch or a linear amplifier.

2.4.2 Transfer Characteristics

In Fig. 2.13 (a) collector currents i_{C1} and i_{C2} for transistors Q_1 and Q_2 biased in the forward-active mode may be given by (neglecting reverse saturation currents of the collector base junction)

$$i_{C1} = \alpha_F I_{ES}\, e^{v_{BE1}/V_T} \tag{2.53}$$

$$i_{C2} = \alpha_F I_{ES}\, e^{v_{BE2}/V_T} \tag{2.54}$$

Here, I_{ES} is the reverse saturation current of emitter-base junction and V_T is volts equivalent of temperature.

From Eqs. (2.53) and (2.54), we may write

$$\frac{i_{C1}}{i_{C2}} = e^{(v_{BE1} - v_{BE2})/V_T} \tag{2.55}$$

We may also write KVL for the loop containing two emitter-base junctions as

$$v_1 - v_{BE1} + v_{BE2} - v_2 = 0$$

or

$$v_{BE1} - v_{BE2} = v_1 - v_2 = v_d$$

where, v_d is the difference of two input voltages.

Also in Fig. 2.11 (a)

$$I_Q = i_{E1} + i_{E2} = \frac{i_{C1}}{\alpha_F} + \frac{i_{C2}}{\alpha_F}$$

$$= \frac{i_{C1}}{\alpha_F}\left(1 + \frac{i_{C2}}{i_{C1}}\right) \tag{2.56}$$

Using Eqs. (2.55) and (2.56) and solving for i_{C1} and i_{C2}, gives

$$i_{C1} = \frac{\alpha_F I_Q}{1 + e^{-v_d/V_T}} \tag{2.57}$$

$$i_{C2} = \frac{\alpha_F I_Q}{1 + e^{v_d/V_T}} \tag{2.58}$$

From Eqs. (2.57) and (2.58), the normalised transfer characteristics (i_C/I_Q vs. v_d/V_T assuming $\alpha_F = 1$) for a differential amplifier are obtained as shown in Fig. 2.14.

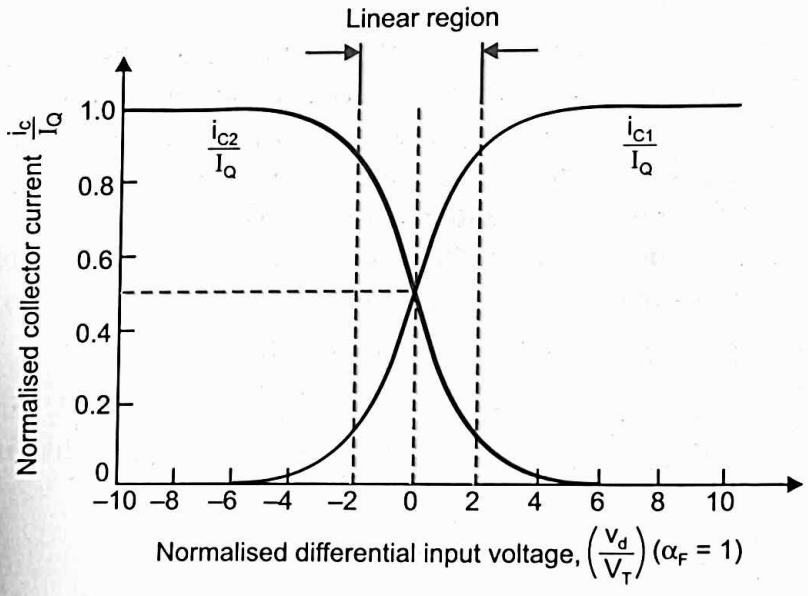


Fig. 2.14 Normalised transfer characteristics for the differential pair

The following important points are observed from the transfer characteristics:

1. For $v_d > 4\,V_T$ (~100 mV), $i_{C1} = \alpha_F I_Q$ and $i_{C2} = 0$, Hence
   $$v_{o1} = V_{CC} - \alpha_F I_Q R_C$$
   and $$v_{o2} = V_{CC}$$
   By proper choice of R_C, v_{o1} can be made very small.
2. For $v_d < -4\,V_T$, $i_{C1} = 0$ and $i_{C2} = \alpha_F I_Q$. Hence $v_{o1} = V_{CC}$ and V_{o2} is negligible. Thus, for $4V_T < v_d < -4V_T$, we can say that a differential amplifier can be made to function as a switch.
3. The differential amplifier functions as a very good limiter for $v_d > \pm 4\,V_T$.

4. DA can function as an automatic gain control (AGC) by varying I_Q.
5. Between the values $-2V_T \leq v_d \leq 2V_T$, DA functions as a linear amplifier.

2.4.3 Low Frequency Small Signal Analysis of Differential Amplifier

An ideal dual-input balanced-output differential amplifier as shown in Fig. 2.13 (a), should amplify only the differential signal at the two inputs and reject the signal common to these inputs. As transistors Q_1 and Q_2 are a matched pair of transistors, thus any unwanted signal, such as noise or hum pick up which is common to both the inputs would get rejected. However in a practical case transistors Q_1 and Q_2 are not equally matched and output does appear even when same voltage is applied to the two input terminals. In this section, we will discuss how to compute the small signal differential mode gain, A_{DM} and common-mode gain A_{CM}. These expressions help in finding the figure of merit CMRR of the differential amplifier and hence the ways to improve it.

The a.c. analysis of the differential amplifier can be performed either by using hybrid-π model or h-parameter model. Both the approaches have been dealt with.

Differential-mode Gain, A_{DM}

In Fig. 2.13 (a) for $v_1 = v_2$, the current I_Q divides equally into the two transistors Q_1 and Q_2 because of the symmetry of the circuit. However, if v_1 is now increased by an incremental voltage (small signal) $v_d/2$ and v_2 is decreased by $v_d/2$, it can be seen that the differential amplifier is being fed by differential small signal v_d. The common mode small signal is naturally zero. The collector current i_{C1} will now increase by an incremental current i_c and i_{C2} will decrease by an equal amount. The sum of total currents in transistors Q_1 and Q_2 however remains constant as constrained by the constant current I_Q. As there is no change of current through R_E, the voltage V_E at the common emitter point 'E' remains constant. Thus, for small signal analysis, the common emitter point 'E' can be considered to be at ground potential. Figure 2.15 (a) shows the small signal equivalent circuit of the differential amplifier under the differential input signal conditions described above. It may be noted that for differential amplifier to behave as a linear amplifier, the differential signal $v_d \leq 2V_T$ (that is, v_d should be smaller than about 50 mV) as discussed in the transfer characteristics (Section 2.4.2).

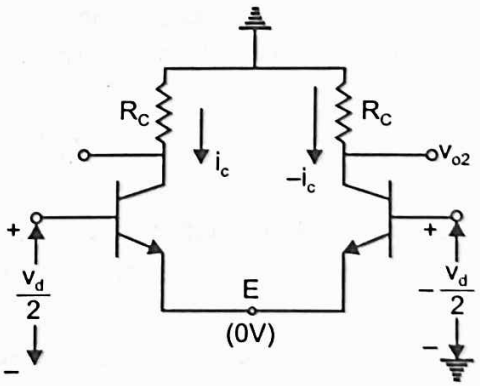


Fig. 2.15 (a) Differential amplifier with differential input signal v_d

Analysis

(i) Using Hybrid-π Model

Since the performance of two sides of the differential amplifier is identical, we need to analyze only one side of the differential amplifier called differential-half circuit. Figure 2.15 (b) shows a single stage CE transistor amplifier fed by a small signal voltage $v_d/2$ and it's a.c. equivalent circuit using hybrid-π model is shown in Fig. 2.15 (c).

From Fig. 2.15 (c),

$$\frac{v_{o1}}{v_d/2} = -g_m R_C$$

or
$$\frac{v_{o1}}{v_d} = -\frac{1}{2} g_m R_C \tag{2.59}$$

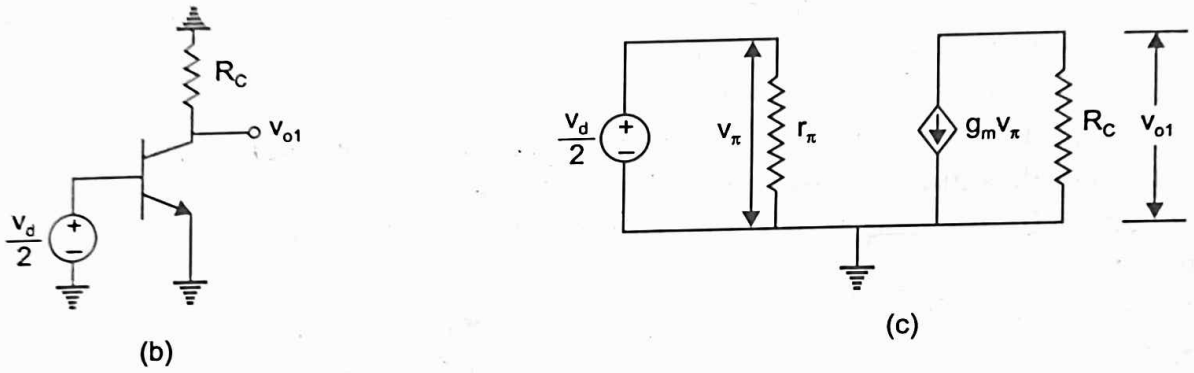


Fig. 2.15 (b) Differential mode half circuit (c) ac-equivalent circuit using hybrid-π model

Similarly, it can be seen that

$$\frac{v_{o2}}{v_d} = \frac{1}{2} g_m R_C \tag{2.60}$$

The output voltage signal of a differential amplifier can be taken either differentially (*i.e.*, between the two collectors) or single-ended (*i.e.*, between one collector and ground). If the output is taken differentially, then the differential-mode gain, A_{DM} is given by

$$A_{DM} = \frac{v_{o1} - v_{o2}}{v_d} = -g_m R_C \text{ (differential-input, differential-output)} \tag{2.61}$$

On the other hand, if output is single-ended, (say between collector of transistor Q_1 and ground), then the differential-mode gain A_{DM} is given by

$$A_{DM} = \frac{v_{o1}}{v_d} = -\frac{1}{2} g_m R_C \text{ (differential-input, single-ended output)} \tag{2.62 (a)}$$

and
$$\frac{v_{o2}}{v_d} = \frac{1}{2} g_m R_C \tag{2.62 (b)}$$

In the above analysis, we have not included the output resistance r_o of the transistor. If r_o is included, Eq. (2.61) will modify to

$$A_{DM} = -g_m \ (R_C \parallel r_o)$$

(ii) Using 'h' Parameters

The a.c. equivalent circuit for Fig. 2.15 (b) using approximate h-parameter model is shown in Fig. 2.15 (d).

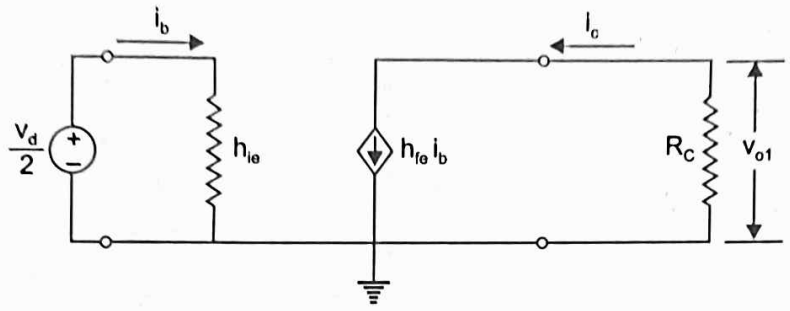


Fig. 2.15 (d) Small signal equivalent circuit of differential half circuit using *h*-parameter model

From Fig. 2.15 (d),

$$v_{o1} = -i_c R_C = -h_{fe}\, i_b\, R_C$$

and $$\frac{v_d}{2} = i_b h_{ie}$$

Therefore, differential mode gain, A_{DM} is given by

$$A_{DM} = \frac{v_{o1}}{v_d} = -\frac{1}{2}\frac{h_{fe}}{h_{ie}} R_C \text{ (Single-ended output)} \qquad (2.63\text{ (a)})$$

Similarly, we may write

$$A_{DM} = \frac{v_{o2}}{v_d} = \frac{1}{2}\frac{h_{fe} R_C}{h_{ie}} \quad \text{(Single-ended output)} \qquad (2.63\text{ (b)})$$

If the output is taken differentially between the two collectors, then

$$A_{DM} = \frac{v_{o1} - v_{o2}}{v_d} = -\frac{h_{fe} R_C}{h_{ie}} \quad \text{(differential-output)} \qquad (2.63\text{ (c)})$$

In the above analysis, the source resistance R_s has not been taken into account.

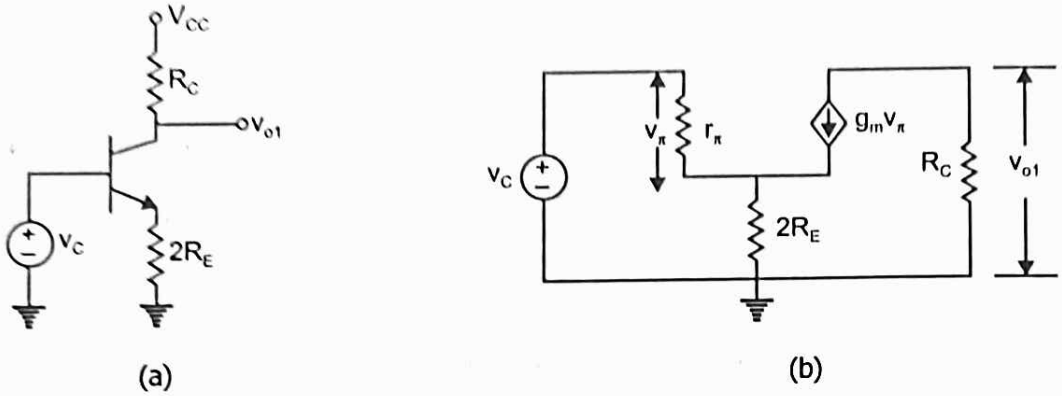
Common-mode gain, A_{CM}

Now, consider the case when v_1 and v_2 both are increased by an incremental voltage v_c. The differential signal v_d now is zero and common-mode signal is v_c. Both the collector currents i_{C1} and i_{C2} will increase by an incremental current i_c. The current through R_E now increases by $2i_c$. The voltage, V_E at emitter node is now increased by $2i_c R_E$ and no longer constant. In order to draw the common mode half circuit, replace resistance R_E by $2R_E$ as shown in Fig. 2.16 (a). The common-mode gain, A_{CM} is calculated from the small-signal hybrid-π equivalent model shown in Fig. 2.16 (b). It can be seen,

$$A_{CM} = \frac{v_{o1}}{v_c} = \frac{v_{o2}}{v_c} = \frac{-\beta_0 R_C}{r_\pi + 2(1+\beta_0)R_E} \qquad (2.64\text{ (a)})$$

For $\beta_0 >> 1$,

β_0 is the small signal CE current gain and is same as h_{fe}.



(a) (b)

Fig. 2.16 (a) Common-mode half circuit (b) a.c. equivalent circuit using hybrid-π model

$$A_{CM} = \frac{-g_m R_C}{1+2g_m R_E} \cong -\frac{R_C}{2R_E} \qquad (2.64\ (b))$$

It can be seen that, if the output is taken differentially, then the output voltage $v_{01} - v_{02}$ will be zero and the common-mode gain will be zero. In this analysis, we have assumed that the circuit is perfectly symmetrical. However, in practical circuits, it will not be so, and the differential output voltage will not be exactly zero. If the output is taken single ended, the common-mode gain will be finite and given by Eqs. (2.64 (a)) and (2.64 (b)).

The common mode gain, A_{CM}, using h-parameter model can be easily computed as

$$A_{CM} = \frac{v_{o1}}{v_c} = \frac{-h_{fe} R_C}{h_{ie} + (1+h_{fe})2R_E} \qquad (2.65)$$

The common-mode rejection ratio (CMRR) is defined as

$$\text{CMRR} = \frac{|A_{DM}|}{|A_{CM}|}$$

For differential-input, differential-output, using Eqs. (2.61) and (2.64 b), we obtain

$$\begin{aligned} \text{CMRR} &\cong \frac{g_m R_C (1+2g_m R_E)}{g_m R_C} \\ &= 1 + 2\,g_m R_E \\ &\cong 2\,g_m R_E \end{aligned} \qquad (2.66)$$

Output for Arbitrary Signals

In the previous analysis, we have assumed that either common mode signals (v_c) or a differential mode signals $\left(\frac{v_d}{2}\right)$ are applied to the two input terminals. However, in a practical situation it will not be so. If, say, any arbitrary signals v_1 and v_2 are applied at the inputs of transistors Q_1 and Q_2 in Fig. 2.11 (a), then we can represent these signals by the sum and difference of common mode component v_{CM} (= v_c) and differential mode component v_{DM} $\left(= \frac{v_d}{2}\right)$ as

$$v_1 = v_{CM} + v_{DM}$$

and $$v_2 = v_{CM} - v_{DM}$$

such that,

$$v_{DM} = \frac{v_1 - v_2}{2} \qquad (2.67\ (a))$$

$$v_{CM} = \frac{v_1 + v_2}{2} \qquad (2.67\ (b))$$

The output voltage v_{o1} and v_{o2} at the output of transistor Q_1 and Q_2 in Fig. 2.11 (a) are given by

$$v_{o1} = A_{DM}\, v_{DM} + A_{CM}\, v_{CM} \qquad (2.68\ (a))$$

and $$v_{o2} = -A_{DM}\, v_{DM} + A_{CM}\, v_{CM} \qquad (2.68\ (b))$$

Example 2.9

Differential amplifier shown in Fig. 2.11 (a) uses a transistor with $\beta = 200$ and is biased at $I_{CQ} = 100\ \mu A$. Determine the value of R_C and R_E if $|A_{DM}| = 500$ and CMRR = 80 dB.

Solution

Given $I_{CQ} = 100\ \mu A$

We know that $g_m = \frac{I_{CQ}}{V_T} = \frac{100 \times 10^{-6}}{25 \times 10^{-3}}\mho = 4\ m\mho$ [for $V_T = 25$ mV]

Using Eq. (2.50),

$$A_{DM} = -g_m R_C \qquad \text{[For differential output]}$$

$$\therefore \quad R_C = -\frac{A_{DM}}{g_m} = \frac{500}{4\,m\mho} = 125\ k\Omega \qquad \textbf{Ans.}$$

As CMRR = 80 dB,

$$\therefore \quad \text{CMRR} = \log^{-1}\left(\frac{80}{20}\right) = 10^4$$

Using Eq. (2.66),

$$\text{CMRR} = 1 + 2\, g_m\, R_E = 1 + 2 \times 4 \times R_E$$

Solving for R_E, we get

$$R_E = 1.25\ M\Omega \qquad \textbf{Ans.}$$

Example 2.10

In the basic differential amplifier of Fig. 2.11 (a), Given: $R_C = 2\ k\Omega$; $R_E = 4.3\ k\Omega$, $V_{CC} = |V_{EE}| = 5$ V; $\beta_0 = 200$, $V_{BE} = 0.7$ V.

Determine:

(i) For $V_1 = V_2 = 0$, that is for both the inputs grounded, the values of quiescent currents and voltages, I_{BQ}, I_{CQ}, V_{o1}, V_{o2}, V_{CEQ}.

(ii) A_{DM}, A_{CM} and CMRR.

Solution

(i) For $V_1 = V_2 = 0$, applying KVL for the base emitter loop, we may write,

$$V_{BE} + 2(1 + \beta_0) I_{BQ} R_E - V_{EE} = 0$$

or
$$I_{BQ} = \frac{V_{EE} - V_{BE}}{2(1+\beta_0) R_E} = \frac{5\,\text{V} - 0.7\,\text{V}}{2(1+200)\ 4.3\ \text{k}\Omega}$$

$$= .0024\ \text{mA} = 2.4\ \mu\text{A}$$

$\therefore$
$$I_{CQ} = 200 \times I_{BQ} = 0.48\ \text{mA}$$

$$V_{o1} = V_{o2} = 5\ \text{V} - 2\ \text{k}\Omega \times 0.48\ \text{mA} \qquad \text{(due to symmetry)}$$

$$= 5\ \text{V} - .96\ \text{V} = 4.04\ \text{V}$$

$$V_{CEQ} = V_C - V_E$$

$$= V_{o1} - (-V_{BE}) = V_{o1} + V_{BE}$$

$$= 4.04\ \text{V} + 0.7\ \text{V} = 4.74\ \text{V}$$

(ii)
$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.48\,\text{mA}}{25\ \text{mV}} = .0192\ \text{℧} = 19.2\ \text{m℧}$$

$$r_\pi = \frac{\beta_0}{g_m} = \frac{200}{19.2\ \text{m℧}} = 10.4\ \text{k}\Omega$$

Using Eq. (2.61),

$$A_{DM} = -g_m R_C$$

$$= -19.2\ \text{m℧} \times 2\ \text{k}\Omega = -38.4$$

From Eq. (2.64a)

$$A_{CM} = \frac{-\beta_0 R_C}{r_\pi + 2(1+\beta_0) R_E}$$

$$= \frac{-200 \times 2\ \text{k}\Omega}{10.4\ \text{k}\Omega + 2(1+200)4.3\,\text{k}\Omega} = -0.23$$

$$\text{CMRR} = \frac{A_{DM}}{A_{CM}} = \frac{-38.4}{-0.23} = 166.9 = 44.4\ \text{dB}$$

Example 2.11

In the differential amplifier designed in Example 2.6, the following inputs are applied:

$$v_1 = 15 \sin 2\pi\,(60)t + 5 \sin 2\pi\,(1000)t\ \text{mV}$$

$$v_2 = 15 \sin 2\pi\,(60)t - 5 \sin 2\pi\,(1000)t\ \text{mV}$$

Here, the signal at 60 Hz is the interference signal and the signal to be processed is at 1 kHz. Determine the output voltages v_{o1} and v_{o2}.

Chapter 2

Solution

We know from Example 2.6

$$g_m = 4 \text{ m}\mho;\ R_C = 125 \text{ k}\Omega,\ R_E = 1.25 \text{ k}\Omega$$

and

$$r_\pi = \frac{\beta_0}{g_m} = \frac{200}{4\,\text{m}\mho} = 50 \text{ k}\Omega$$

Given, $A_{DM} = -500$,

We compute A_{CM} from Eq. (2.53 (a))

$$A_{CM} = \frac{-\beta_0 \times R_C}{2(1+\beta_0)R_E + r_\pi} = \frac{-200 \times 125 \text{ k}\Omega}{2(1+200)1250 \text{ k}\Omega + 50 \text{ k}\Omega} = -0.05$$

From Eqs. (2.67 (a)) and (2.67 (b))

$$v_{DM} = \frac{v_1 - v_2}{2} = 5 \sin 2\pi\,(1000)t$$

and

$$v_{CM} = \frac{v_1 - v_2}{2} = 15 \sin 2\pi\,(60)t$$

From Eqs. (2.57 (a)) and (2.57 (b)), we get

$$v_{o1} = -500[5 \sin 2\pi\,(1000)t] - 0.05[15 \sin 2\pi\,(60)t]$$
$$= -2500 \sin 2\pi\,(1000)t - 0.75 \sin 2\pi\,(60)t \text{ mV}.$$

and

$$v_{o2} = -(-500)[5 \sin 2\pi\,(1000)t] - 0.05[15 \sin 2\pi\,(60)t]$$
$$= +2500 \sin 2\pi\,(1000)t - 0.75 \sin 2\pi\,(60)t \text{ mV}$$

Example 2.12

For the differential amplifier shown in Fig. (i) find the differential voltage gain. Given $\beta_0 = 100$

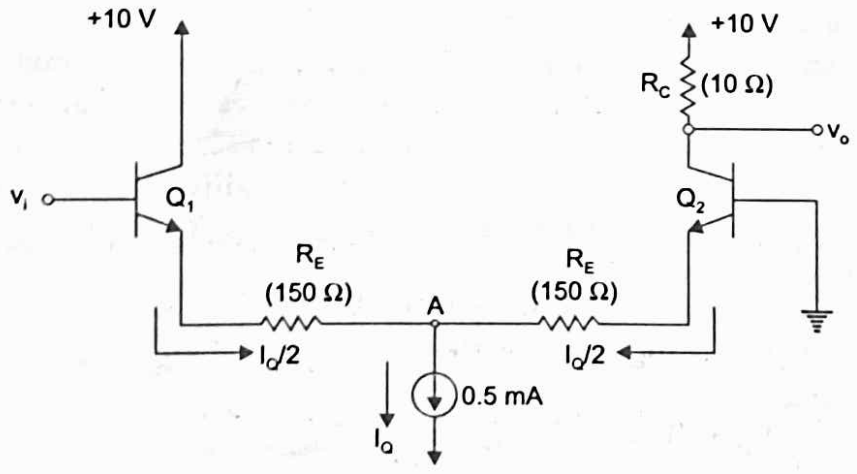


Fig. (i) Circuit for Example 2.12

Solution

Note that the circuit is a differential amplifier with single ended output taken at the collect of Q_2. Also there is a 150 Ω resistor between emitter and terminal A.

$$I_{CQ} = \frac{I_Q}{2} = \frac{0.5 \text{ mA}}{2} = 0.25 \text{ mA}$$

$$\therefore \quad g_m = \frac{I_{CQ}}{V_T} = \frac{0.25\text{mA}}{25 \text{ mV}} = \frac{1}{100}\mho$$

and $$r_\pi = \frac{\beta_0}{g_m} = \frac{100}{1/100} = 10 \text{ k}\Omega$$

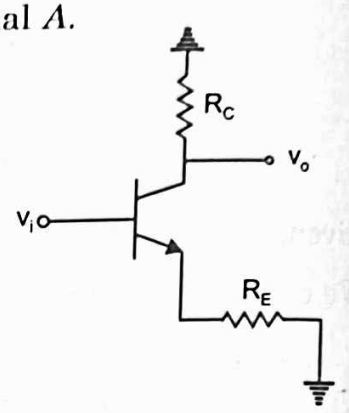


Fig. (ii) Equivalent circuit

The differential mode gain for a single stage is found from the equivalent circuit shown in Fig. (ii) and can be written as

$$A_{DM} = \frac{1}{2}\left[\frac{\beta_0 R_C}{r_\pi + (1+\beta_0)R_E}\right] \text{ [Eq. 2.51 (b) modified on account of } R_E\text{]}$$

$$= \frac{1}{2}\left[\frac{100 \times 10 \text{ k}\Omega}{10 \text{ k}\Omega + 101 \times 150\Omega}\right] = 40 \text{ V/V}$$

Note that the sign of A_{DM} is positive because the output is taken at the collector of Q_2 whereas input is applied at the base of Q_1.

2.4.4 Circuits for Improving CMRR

For CMRR to be large, A_{CM} should be as small as possible. From Eq. (2.65), it can be seen that $A_{CM} \to 0$ as $R_E \to \infty$. There are, however, practical limitations on the magnitude of R_E because of the quiescent dc voltage across it. If R_E is made large, the emitter supply V_{EE} will also have to be increased in order to maintain the proper quiescent current. And if the operating currents of the transistors are allowed to decrease, then h_{ie} will decrease, thereby decreasing h_{fe} too. This too will decrease the common mode rejection ratio.

The use of a constant current bias in place of R_E is found to be a practical solution to the problem discussed above. In Fig. 2.17, R_E is replaced by a constant current transistor circuit in which R_1, R_2 and R_3 can be adjusted to give the same quiescent conditions for the transistors Q_1 and Q_2 as in the original circuit of Fig. 2.13 (a). The modified circuit presents a very high effective emitter resistance R_E even for very small values of R_3. Typically, R_E is hundreds of kΩ even if R_3 is as small as 1 kΩ.

Let us calculate the current I_Q and verify that the emitter circuit really behaves as a constant current source. Writing KVL for the base circuit of Q_3, we get

$$V_{BE3} + I_3 R_3 = V_D + (V_{EE} - V_D)\frac{R_2}{R_1 + R_2} \tag{2.69}$$

Here V_D represents the drop across the diode D. If the base current is neglected, then

$$I_Q \simeq I_3 = \frac{1}{R_3}\left(\frac{V_{EE}R_2}{R_1+R_2} + \frac{V_D R_1}{R_1+R_2} - V_{BE3}\right) \tag{2.70}$$

By proper choice of resistors R_1 and R_2, it is possible to set,

$$\frac{V_D R_1}{R_1+R_2} = V_{BE3} \tag{2.71}$$

Then,
$$I_Q \simeq \frac{1}{R_3}\left(\frac{V_{EE}R_2}{R_1+R_2}\right) \tag{2.72}$$

So, it can be seen that the current I_Q will be essentially constant as it does not depend upon signal voltages v_1 and v_2.

What is the use of the diode D in this circuit? The diode D makes I_Q independent of temperature. We know that V_{BE3} decreases approximately by 2.5 mV/°C and the diode D also has the same temperature dependence. Hence, the two variations cancel each other and I_Q becomes independent of temperature. It is usually difficult to satisfy Eq. (2.71) with a single diode D in the circuit of Fig. 2.17 as V_D and V_{BE3} have almost the same value. Hence two diodes are normally used for V_D.

With I_Q constant, it can be shown that the common-mode gain is zero, so that the circuit provides very high CMRR. Under quiescent conditions (no ac signal) the current I_Q gets divided equally in identical transistors Q_1 and Q_2 and $I_{C1}=I_{C2}=I_{Q/2}$. Now if the same signal ($v_1 = v_2$) is applied to both the inputs, there will still be no change in the collector currents i_{C1} and i_{C2} as I_Q is constant. Thus the small signal current i_c flowing through the load resistor R_C is zero resulting in zero output voltage. Thus we can state that a diff-amp, if supplied by a constant current bias gives very high CMRR. The constant current circuit of the type shown in Fig. 2.17 is used in Motorola MC1530 (Fig. 2.23). A more commonly used IC op-amp μA 741 uses a different type of constant current source which is very simple and uses less number of components. This circuit is called current mirror and offers extremely large resistance under a.c. conditions, thereby providing a high value of CMRR.

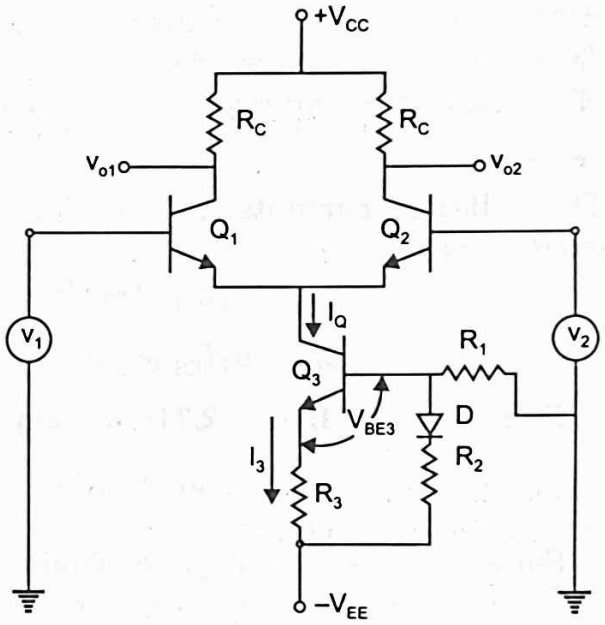


Fig. 2.17 Differential amplifier using constant current bias

Constant Current Source (Current Mirror)

A constant current source makes use of the fact that for a transistor in the active mode of operation, the collector current is relatively independent of the collector voltage. In the basic circuit shown in Fig. 2.18 transistors Q_1 and Q_2 are matched as the circuit is fabricated using IC technology. It may be noted that bases and emitter of Q_1 and Q_2 are tied together and thus have the same V_{BE}. In addition, transistor Q_1 is connected as a diode by shorting its collector to base.

The input current I_{ref} flows through the diode-connected transistor Q_1 and thus establishes a voltage across Q_1. This voltage in turn appears between the base and emitter of Q_2. Since Q_2 is identical to Q_1, the emitter current of Q_2 will be equal to emitter current of Q_1 which is approximately equal to I_{ref}. Thus, we can say that as long as Q_2 is maintained in the active region, its collector current $I_{C2} = I_o$ will be approximately equal to I_{ref}. Since the output current I_o is a reflection or mirror of the reference current I_{ref}, the circuit is often referred to as a current mirror.

This mirror effect is however, valid only for large values of β. To study the effect of β on the operation of the current mirror circuit, we analyze it further.

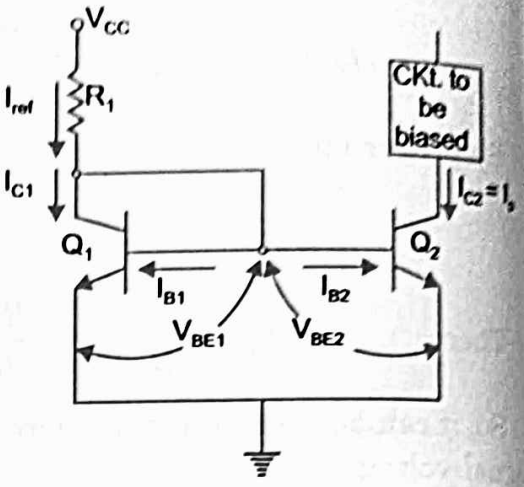


Fig. 2.18 The basic BJT current mirror

Analysis

The collector currents I_{C1} and I_{C2} for transistors Q_1 and Q_2 can be approximately expressed as

$$I_{C1} \cong \alpha_F I_{ES}\, e^{V_{BE1}/V_T} \tag{2.73}$$

$$I_{C2} \cong \alpha_F I_{ES}\, e^{V_{BE2}/V_T} \tag{2.74}$$

From Eqs. (2.73) and (2.74), we may write

$$\frac{I_{C2}}{I_{C1}} = e^{(V_{BE2} - V_{BE1})/V_T} \tag{2.75}$$

Since $V_{BE1} = V_{BE2}$, we obtain

$$I_{C2} = I_{C1} = I_C = I_o$$

Also since both the transistors are identical, $\beta_1 = \beta_2 = \beta$.

KCL at the collector of Q_1 gives

$$I_{ref} = I_{C1} + I_{B1} + I_{B2} \tag{2.76}$$

$$= I_{C1} + \frac{I_{C1}}{\beta_1} + \frac{I_{C2}}{\beta_2} = I_C\left(1 + \frac{2}{\beta}\right) \tag{2.77}$$

Solving Eq. (2.77), I_C may be expressed as

$$I_C = \frac{\beta^*}{\beta + 2} I_{ref} \tag{2.78}$$

where I_{ref} from Fig. 2.16 can be seen to be

$$I_{ref} = \frac{V_{CC} - V_{BE}}{R_1} \cong \frac{V_{CC}}{R_1} \text{ (as } V_{BE} = 0.7 \text{ V is small)} \tag{2.79}$$

From Eq. (2.78), for $\beta >> 1$, $\beta / (\beta + 2)$ is almost unity and the output current I_o is equal to the reference current, I_{ref} which for a given R_1 is constant. Typically I_o varies by about 3% for $50 \le \beta \le 200$.

---

* $\beta = \beta_F$ and is the large signal CE current gain.

It is possible to obtain current transfer ratio other than unity simply by controlling the area of the emitter-base junction (EBJ) of the transistor Q_2. For example, if the area of EBJ of Q_2 is 4 times that of Q_1, then

$$I_o = 4\ I_{ref}$$

The output resistance of the current source is the output resistance, r_o of Q_2,

$$R_o = r_{02} = \frac{V_A}{I_o} \cong \frac{V_A}{I_{ref}} \quad [V_A \text{ is the Early voltage}]$$

The circuit however operates as a constant current source as long as Q_2 remains in the active region. From the volt-ampere characteristics of Q_2 shown in Fig. 2.19, it can be seen that for $V_{CE2} < 0.3$ V, Q_2 is saturated. For $V_{CE2} > 0.3$ V, transistor operates in the active region and I_{C2} is essentially constant. The slight increase in I_{C2} is due to Early effect. The 1/slope of the curve in this region gives the output resistance r_o of the current source. For all practical purposes, early voltage may be assumed to be infinite, so that $r_o \to \infty$ and I_{C2} is constant.

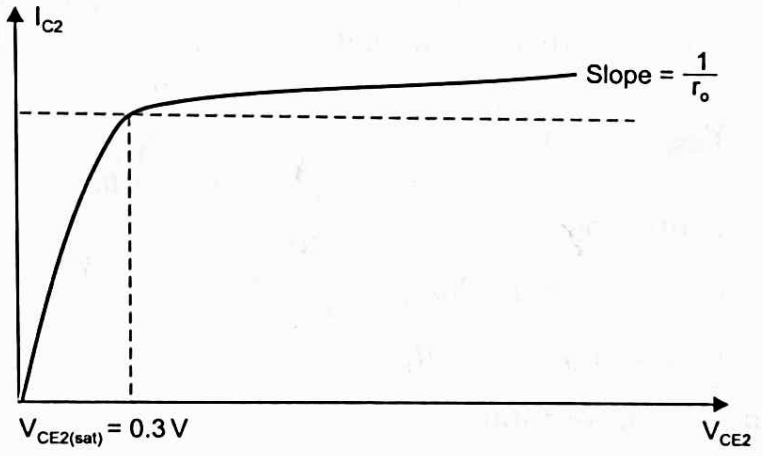


Fig. 2.19 Volt-ampere characteristics for transistor Q_2

Example 2.13

The current mirror of Fig. 2.18 is to provide a 1.0 mA current with $V_{CC} = 10$ V. Assume $\beta = 125$ and $V_{BE} = 0.7$ V. Determine (a) the value of R_1 (b) value of R_1 for $I_C = 10\ \mu A$.

Solution

(a) From Eq. (2.78), we have

$$1.0\ \text{mA} = \frac{125}{125+2} \times \frac{10\ \text{V} - 0.7\ \text{V}}{R_1}$$

$$R_1 = 9.15\ \text{k}\Omega$$

(b) Again using Eq. (2.78), the value of R_1 is found to be

$$R_1 = 915\ \text{k}\Omega$$

Widlar Current Source

The basic current mirror of Fig. 2.18 has a limitation. Whenever, we need low value current source as in Example 2.6 part (b), the value of the resistance R_1 required is sufficiently high and can not be fabricated economically in IC circuits. In Fig. 2.20 is shown a Widlar current source which is particularly suitable for low value of currents. The circuit differs from the basic current mirror only in the resistance R_E that is included in the emitter lead of Q_2. It can be seen that due to R_E, the base-emitter voltage V_{BE2} is less than V_{BE1} and consequently current I_o is smaller than I_{C1}.

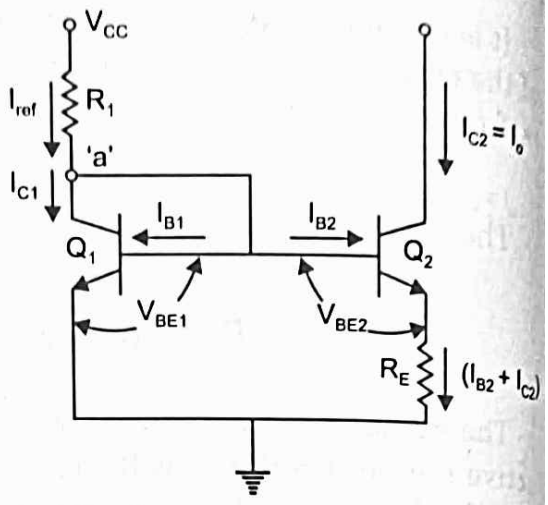


Fig. 2.20 Widlar current source

The ratio of collector currents I_{C1} and I_{C2} using Eqs. (2.73) and (2.74) is given by

$$\frac{I_{C1}}{I_{C2}} = e^{(V_{BE1} - V_{BE2})/V_T} \tag{2.80}$$

Taking natural logarithm of both sides, we get

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right) \tag{2.81}$$

Writing KVL for the emitter base loop

$$V_{BE1} = V_{BE2} + (I_{B2} + I_{C2})R_E \tag{2.82}$$

or
$$V_{BE1} - V_{BE2} = (1/\beta + 1)\, I_{C2}R_E \tag{2.83}$$

From Eqs. (2.81) and (2.83), we obtain

$$\left(\frac{1}{\beta} + 1\right) I_{C2}R_E = V_T \ln \frac{I_{C1}}{I_{C2}} \tag{2.84}$$

or
$$R_E = \frac{V_T}{\left(1 + \frac{1}{\beta}\right) I_{C2}} \ln \frac{I_{C1}}{I_{C2}} \tag{2.85}$$

A relation between I_{C1} and the reference current I_{ref} is obtained by writing KCL at the collector point of Q_1 (node 'a')

$$I_{ref} = I_{C1} + I_{B1} + I_{B2} \tag{2.86}$$

$$= I_{C1}\left(1 + \frac{1}{\beta}\right) + \frac{I_{C2}}{\beta} \tag{2.87}$$

(Assuming $\beta_2 = \beta_1 = \beta$ for identical transistors)

In the Widlar current source $I_{C2} << I_{C1}$, therefore the term I_{C2}/β may be neglected in Eq. (2.87).

Thus, $$I_{ref} \cong I_{C1}\left(1+\frac{1}{\beta}\right) \tag{2.88}$$

or $$I_{C1} = \frac{\beta}{\beta+1} I_{ref} \tag{2.89}$$

where $$I_{ref} = \frac{V_{CC} - V_{BE}}{R_1} \tag{2.90}$$

For $\beta >> 1$, $$I_{C1} \cong I_{ref} \tag{2.91}$$

The design and advantages of Widlar current source are illustrated in the following example:

Example 2.14

Design a Widlar current source for generating a constant current $I_0 = 10\ \mu A$. Assume $V_{CC} = 10$ V, $V_{BE} = 0.7$ V, $\beta = 125$. Use $V_T = 25$ mV.

Solution

For the Widlar current source of Fig. 2.20, we must first decide a suitable value for I_{ref}. If we choose $I_{ref} = 1$ mA, then, R_1 is given by

$$R_1 = \frac{10\,V - 0.7\,V}{1\,mA} = 9.3\,k\Omega$$

The value of R_E is determined from Eq. (2.85)

$$R_E = \frac{0.025}{\left(1+\frac{1}{125}\right)10\times10^{-6}} \ln\left(\frac{1\,mA}{10\,\mu A}\right) = 11.5\ k\Omega$$

It is clearly seen that Widlar circuit allows the generation of small currents using relatively small resistors.

Sometimes, it is convenient to use emitter resistances in both the transistors Q_1 and Q_2 as shown in Fig. 2.21. If $R_1 = R_2$ the currents $I_{C1} = I_{C2}$. The same circuit can also be used to provide different currents in Q1 and Q2, as we shall now see.

Analysis

Rewriting Eq. (2.75) as

$$V_{BE2} - V_{BE1} = V_T \ln \frac{I_{C2}}{I_{C1}} \tag{2.92}$$

Writing KVL in the base-emitter loop

$$V_{BE2} - V_{BE1} = I_{C1}R_1 - I_{C2}R_2$$

(Neglecting base current) (2.93)

From Eqs. (2.92) and (2.93),

$$I_{C1}R_1 - I_{C2}R_2 = V_T \ln \frac{I_{C2}}{I_{C1}} \tag{2.94}$$

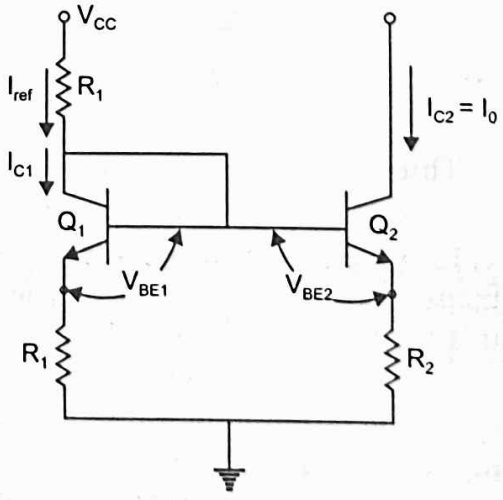


Fig. 2.21 A current mirror with magnification ($I_{C2}/I_{C1} \cong R_1/R_2$)

$$\frac{I_{C2}}{I_{C1}}\frac{R_2}{R_1} = 1 - \frac{V_T}{I_{C1}R_1}\ln\frac{I_{C2}}{I_{C1}} \tag{2.95}$$

$$\frac{I_{C2}}{I_{C1}} = \frac{R_1}{R_2}\left(1 - \frac{V_T}{I_{C1}R_1}\ln\frac{I_{C2}}{I_{C1}}\right) \tag{2.96}$$

For the range $0.1 < \frac{I_{C2}}{I_{C1}} < 10$, we can assume $\frac{I_{C2}}{I_{C1}} \cong \frac{R_1}{R_2}$. Thus even large ratios $\frac{I_{C2}}{I_{C1}}$ (say 10) is easily obtained by the modified circuit.

Current Repeaters

The basic current mirror of Fig. 2.18 can be used to source current to more than one load. Such a circuit is called current repeater and is shown in Fig. 2.22. If all the transistors are identical, then the current $I_C = I_{C1} = \ldots\ \ldots = I_{CN} \cong I_{ref}$.

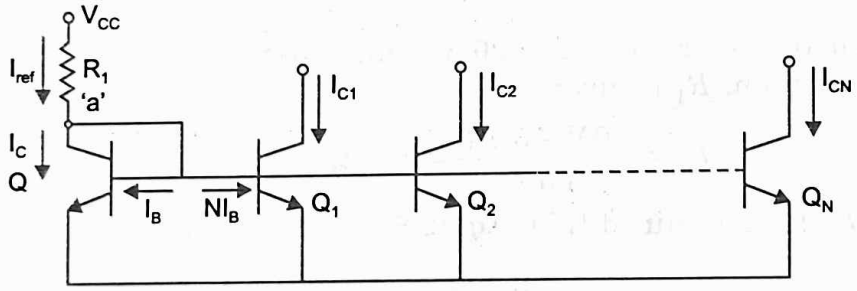


Fig. 2.22 A current repeater to source current to N transistors $Q_1, Q_2, \ldots\ \ldots\ Q_N$

It can be seen from Fig. 2.22 at node 'a'

$$I_{ref} = I_C + I_B + NI_B \text{ (Assuming identical transistors)} \tag{2.97}$$

$$= I_C + \frac{(1+N)}{\beta}I_C$$

$$= I_C\left(1 + \frac{(1+N)}{\beta}\right) \tag{2.98}$$

Thus,

$$I_C = I_{ref}\frac{\beta}{\beta+1+N} \tag{2.99}$$

It is possible to achieve different value of $I_{C1}, I_{C2}, \ldots\ \ldots\ I_{CN}$ by scaling the emitter area of transistors $Q_1, Q_2, \ldots\ \ldots\ Q_N$. The same can also be achieved by using emitter resistance as in the Widlar current source.

Example 2.15

For the circuit shown in Fig. 2.23 determine I_{C1}, I_{C2}, and I_{C3}. Assume $\beta = 125$

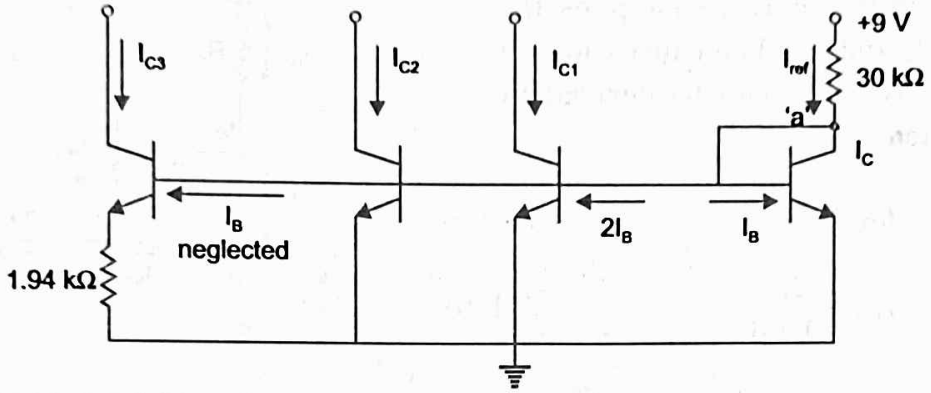


Fig. 2.23 Circuit for Example 2.15

Solution

$$I_{ref} = \frac{9\text{V} - 0.7\text{V}}{30\,\text{k}\Omega} = 0.277\ \text{mA}$$

Also at node 'a'

$$I_{ref} = I_C + 3I_B \text{ (Assume } I_{B3} \text{ of Widlar source negligible)}$$

$$= I_C\left(1 + \frac{3}{\beta}\right)$$

$$I_C = I_{ref}\left(\frac{\beta}{3+\beta}\right)$$

Putting the values and solving, we get

$$I_{C1} = I_{C2} = 0.271\ \text{mA}$$

Calculate I_{C3}, using Eq. (2.85) gives

$$1.94 = \frac{0.025}{I_{C3}\left(1 + \frac{1}{125}\right)} \ln \frac{0.271}{I_{C3}}$$

Solving the transcendental equation by trial and error, we obtain

$$I_{C3} = 0.0287\ \text{mA}$$

Improved Current Source Circuits

A good current source must meet two requirements. The first is that the output current, I_o should not be dependent upon β and secondly the output resistance of the current source should be very high. The need for high output resistance current source can be seen because the common-mode gain of the differential amplifier (used as basic building block in op-amps) the common-mode gain of the differential amplifier (used as basic building block in op-amps) can only be reduced by using high resistance current sources. Also, all differential amplifiers invariably use current source as a load. Thus to obtain high voltage gain a large output resistance load is required. Now, we discuss two circuits that exhibit reduced dependence on β or increased output resistance.

A Current Source with Gain

The circuit shown in Fig. 2.24 includes a transistor Q_3 whose emitter current supplies the base currents of Q_1 and Q_2. The expression for the source current $I_o = I_{C2}$ can be derived by writing KCL at node 'a'

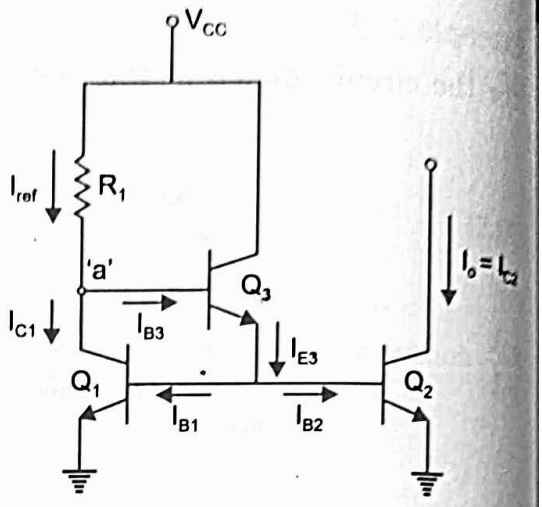


Fig. 2.24 A current source with gain

$$I_{ref} = I_{C1} + I_{B3}$$

$$= I_{C1} + \frac{I_{E3}}{1+\beta} \qquad (2.100)$$

Also $I_{E3} = I_{B1} + I_{B2} = 2I_B$ (since Q_1 and Q_2 are identical)

Thus,

$$I_{ref} = I_{C1} + \frac{2I_B}{1+\beta} \qquad (2.101)$$

$$= I_C + \frac{2I_C}{\beta(1+\beta)} = I_C\left(1 + \frac{2}{\beta(1+\beta)}\right)$$

or $$I_o = I_C = I_{ref}\frac{\beta(1+\beta)}{\beta^2+\beta+2} \qquad [I_{C1} = I_{C2} = I_o] \qquad (2.102)$$

where

$$I_{ref} = \frac{V_{CC} - 2V_{BE}}{R_1}$$

It is easily seen from Eq. (2.102) that the output current is essentially independent of β. The output resistance of the current source is only r_0. It can however be increased by using emitter resistances in Q_1 and Q_2 as is done in the modified Widlar source circuit in Fig. 2.21. The two emitter resistors can also be used to make I_o different from I_{ref}.

Wilson Current Source

The final current source shown in Fig. 2.25 provides an output current I_0, which is very nearly equal to I_{ref} and also exhibits a very high output resistance.

Analysis

Since $V_{BE1} = V_{BE2}$

$I_{C1} = I_{C2}$ and $I_{B1} = I_{B2} = I_B$

At node 'b'

$$I_{E3} = 2I_B + I_{C2} = \left(\frac{2}{\beta} + 1\right) I_{C2} \qquad (2.103)$$

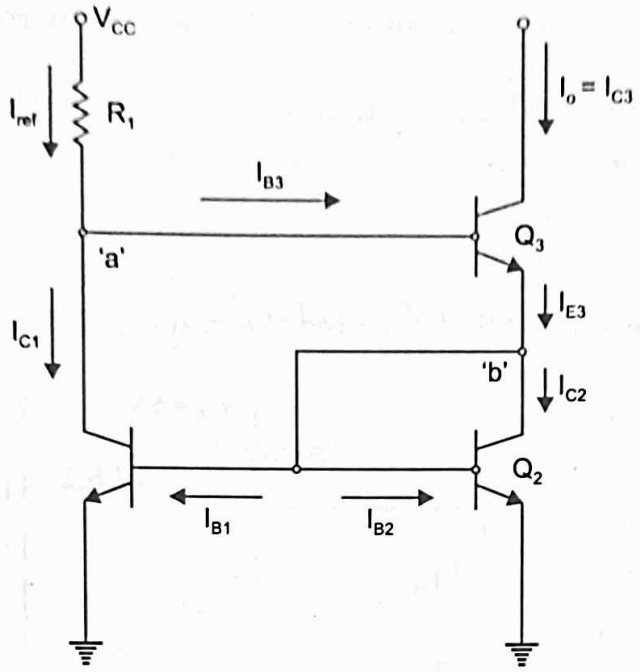


Fig. 2.25 A Wilson current source

I_{E3} is also equal to

$$I_{E3} = I_{C3} + I_{B3} = I_{C3}\left(1 + \frac{1}{\beta}\right) \tag{2.104}$$

From Eqs. (2.103) and (2.104), we obtain

$$I_{C3}\left(1 + \frac{1}{\beta}\right) = I_{C2}\left(1 + \frac{2}{\beta}\right)$$

$$I_{C3} = I_o = \left(\frac{\beta + 2}{\beta + 1}\right) I_{C2} \tag{2.105}$$

Since, $I_{C1} = I_{C2}$

$$I_o = \left(\frac{\beta + 2}{\beta + 1}\right) I_{C1} \tag{2.106}$$

At node 'a'

$$I_{ref} = I_{C1} + I_{B3} = \frac{\beta + 1}{\beta + 2} I_o + \frac{I_o}{\beta} = \frac{\beta^2 + 2\beta + 2}{\beta^2 + 2\beta} I_o$$

or $$I_o = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2} I_{ref} \tag{2.107}$$

where $$I_{ref} = \frac{V_{CC} - 2V_{BE}}{R_1} \tag{2.108}$$

The difference $$I_o - I_{ref} = \frac{2}{\beta^2 + 2\beta + 2} I_{ref} \tag{2.109}$$

is extremely small error for modest values of β. The output resistance of a Wilson curren mirror is substantially greater $\left(\cong \beta\frac{r_o}{2}\right)$ than simple current mirror or Widlar current mirro

More Solved Examples

Example 2.16

For the circuit shown in Fig. 2.26, determine the value of I_o for β = 100. Assume $V_{BE} = 0.7$

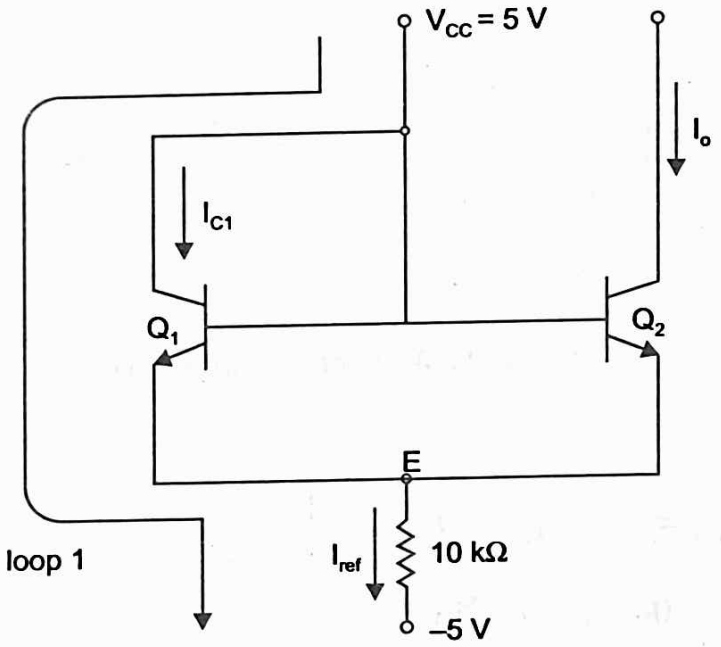


Fig. 2.26 Circuit for Example 2.16

Solution

Writing KVL for the indicated loop 1

$$5\,\text{V} - V_{BE} - 10\,\text{k}\Omega\, I_{ref} + 5\,\text{V} = 0$$

$$I_{ref} = \frac{10\,\text{V} - 0.7\,\text{V}}{10\,\text{k}\Omega} = 0.93\ \text{mA}$$

At emitter node '*E*'

$$I_{ref} = 2I_E \qquad \text{(Assuming identical transistors)}$$

$$= 2(I_C + I_B) = 2I_C\left(1 + \frac{1}{\beta}\right)$$

Then $$I_C = \frac{\beta}{2(1+\beta)} I_{ref} = 0.46\ \text{mA}$$

Due to mirror effect $$I_o = I_{C1} = I_C = 0.46\ \text{mA}$$

Example 2.17

For the circuit shown in Fig. 2.27.
(a) Determine I_{C1} and I_{C2}
(b) Find R_C so that $V_o = 6$ V. Assume $\beta = 200$.

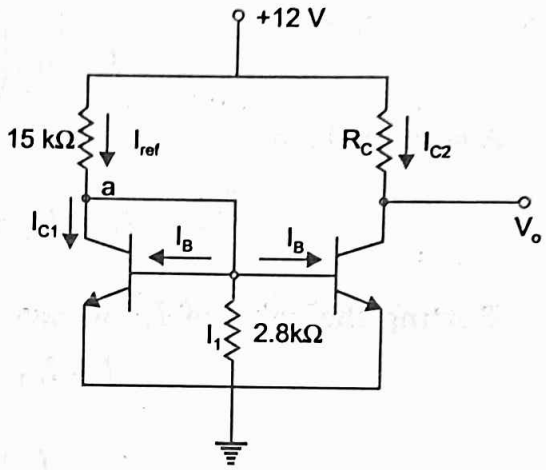


Fig. 2.27 Circuit for Example 2.17

Solution

(a)
$$I_{ref} = \frac{12\text{ V} - 0.7\text{ V}}{15\text{ k}\Omega} = 0.75\text{ mA}$$

and
$$I_1 = \frac{0.7\text{ V}}{2.8\text{ k}\Omega} = 0.25\text{ mA}$$

At node 'a'

$$I_{ref} = I_{C1} + 2I_B + I_1$$

$$= I_{C1}\left(1 + \frac{2}{\beta}\right) + I_1$$

Solving for I_{C1} gives

$$I_{C1} = 0.495\text{ mA} \cong 0.5\text{ mA}$$

$$I_{C2} = I_{C1} \qquad \text{(due to mirror effect)}$$

(b) From the outer loop

$$12\text{ V} = I_{C2}R_C + V_o$$

$$R_C = \frac{12\text{ V} - 6\text{ V}}{0.5\text{ mA}} = 12\text{ k}\Omega$$

Example 2.18

Figure 2.28 shows a modified current mirror circuit. Determine the emitter current in transistor Q_3 if $\beta = 100$ and $V_{BE} = 0.75$ V.

Solution

From Fig. 2.26 at node 'a'

$$I = I_{C1} + I_1 = I_{C1} + I_{B1} + I_1'$$

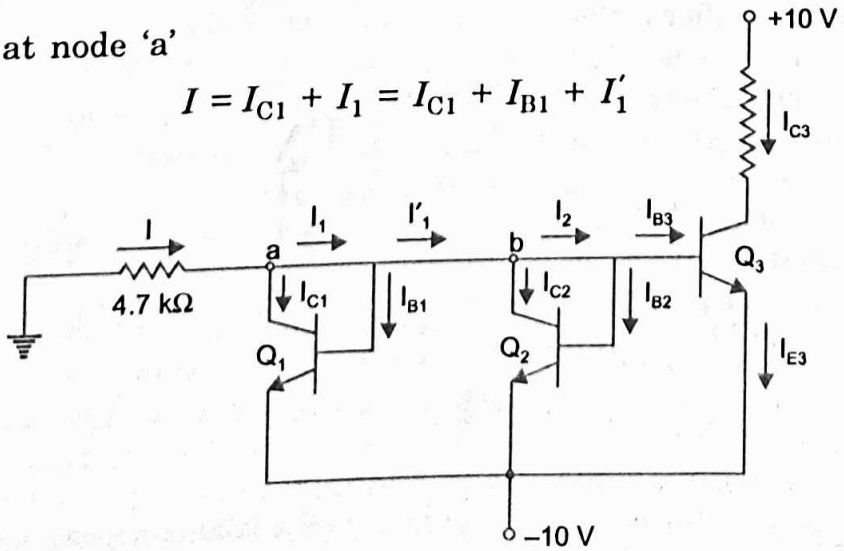


Fig. 2.28 Circuit of Example 2.18

or, $$I = I_{C1}\left(1+\frac{1}{\beta}\right) + I_1' \simeq I_{C1} + I_1' \quad (\text{as } \beta >> 1)$$

Also at node 'b'

$$I_1' = I_{C2} + I_2 = I_{C2} + I_{B2} + I_{B3} = I_{C2}\left(1+\frac{1}{\beta}\right) + I_{B3} \simeq I_{C2} + I_{B3}$$

Putting the value of I_1', we get

$$I = I_{C1} + I_{C2} + I_{B3} = 2I_C + I_{B3} \qquad [\text{as } I_{C1} = I_{C2} = I_C]$$

$$\simeq I_C\left(2+\frac{1}{\beta}\right) \simeq 2I_C$$

The current I is given by,

$$I = \frac{10 - 0.75}{4.7\ \text{k}\Omega} = \frac{9.25}{4.7\ \text{k}\Omega} = 1.97\ \text{mA}$$

The collector current of Q_3 is equal to the collector current of Q_1 and Q_2 due to mirror action. Therefore, the emitter current

$$I_{E3} \simeq I_{C3} = I_C = \frac{I}{2} = 0.98\ \text{mA}$$

2.4.5 Input Resistance

The resistance offered by the differential amplifier of Fig. 2.29 to the differential input signal $(v_1 - v_2)$ is called differential input resistance R_{id}. The emitters of Q_1 and Q_2 are floating as R_E is replaced by a constant current source, therefore $R_{id} \simeq h_{ie1} + h_{ie2} = 2\ h_{ie}$. If input 2 is grounded, then input 1 is loaded by 2 h_{ie}. The value of h_{ie} can be increased by reducing the biasing currents for Q_1 and Q_2 and input resistance of the order of 500 kΩ can be obtained.

Higher values of input resistance can be obtained by using a Darlington pair in place of transistor Q_1 and Q_2 of Fig. 2.29 as shown in Fig. 2.30. One drawback of the Darlington differential amplifier is the higher offset voltage V_{os}, (due to cascaded stages) which is about 2 times larger than the ordinary two transistor differential amplifier.

The most important feature of the Darlington pair differential amplifier is its extraordinary large current gain. For the circuit shown in Fig. 2.30, the overall current gain is

$$\beta = \frac{I_C}{I_{B1}} = \frac{I_{C1} + I_{C2}}{I_{B1}}$$

$$= \frac{I_{C1}}{I_{B1}} + \frac{I_{C2}}{I_{B1}}$$

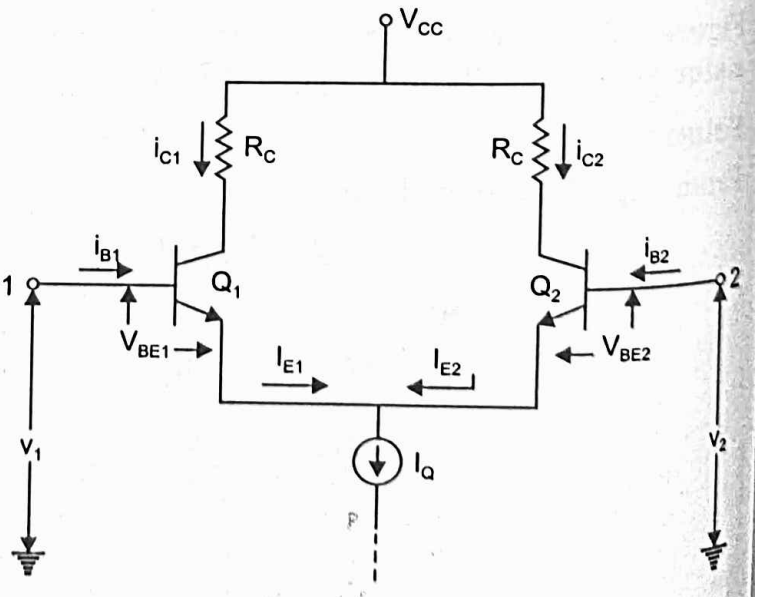


Fig. 2.29 Differential amplifier

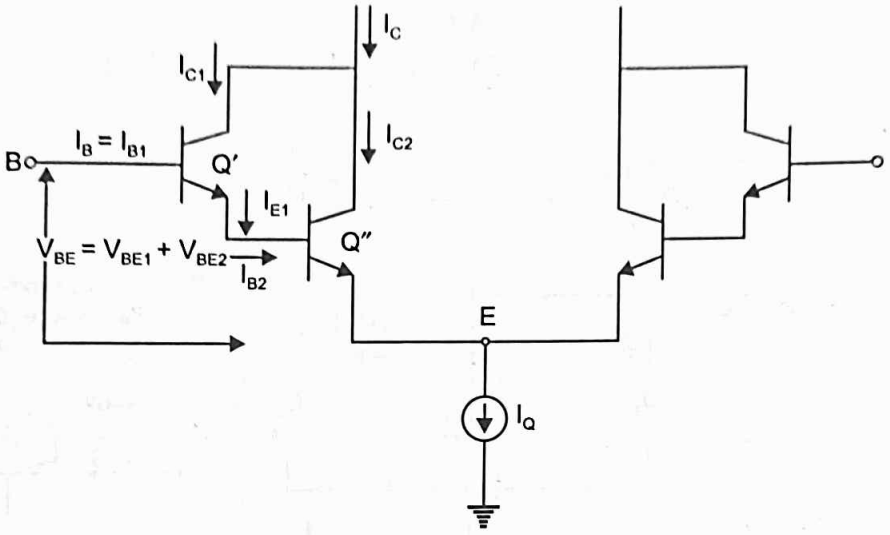


Fig. 2.30 Differential amplifier using Darlington pair

$$= \frac{I_{C1}}{I_{B1}} + \frac{I_{C2}}{I_{B2}} \times \frac{I_{B2}}{I_{B1}}$$

$$= \beta_1 + \beta_2 (\beta_1 + 1) \quad \begin{bmatrix} I_{B2} = I_{E1} \\ = I_{C1} + I_{B1} \end{bmatrix} \cong \beta_2\beta_1$$

So, the overall current gain β of the Darlington circuit will be of the order of 10,000 if the current gain of the individual transistor is about 100. Another method to get higher input resistance is to fabricate a FET differential pair as the input stage with the rest of the stages made of BJTs. Input resistance of the order of 10^{12} Ω is possible with such JFET inputs. A number of such op-amps are described in Sec. 2.6.

2.4.6 Active Load

The open circuit voltage gain of an op-amp should be as large as possible and this is achieved by cascading gain stages. However, this increases the phase shift too and amplifier becomes more susceptible to breaking out into oscillations. One can think of increasing gain by using large collector resistance values as gain is proportional to load resistor R_C. However, there are limitations to the maximum value of R_C to be used due to the following two reasons:

(i) A large value of resistance requires a large chip area.
(ii) For large R_C quiescent drop across it increases and hence a large power supply will be required to maintain a given quiescent collector current. These difficulties are circumvented by using a current source of the type shown in Fig. 2.18 as load in the place of R_C.

The current mirror discussed earlier has a dc resistance of the order of few kilohms, as the quiescent voltage across it is a fraction of the supply voltage and the current is in milliamperes. However, since it acts as a constant current source, its dynamic resistance (ac) is very high. Hence, a current mirror can also be used as an active load for an amplifier to obtain a very large voltage gain. Figure 2.31 (a) shows a diff-amp with an active load. The current mirror uses *pnp* transistors Q_3 and Q_4. The constant current I_Q may also be obtained from a current mirror. The operation of the circuit in Fig. 2.31 (a) is as follows:

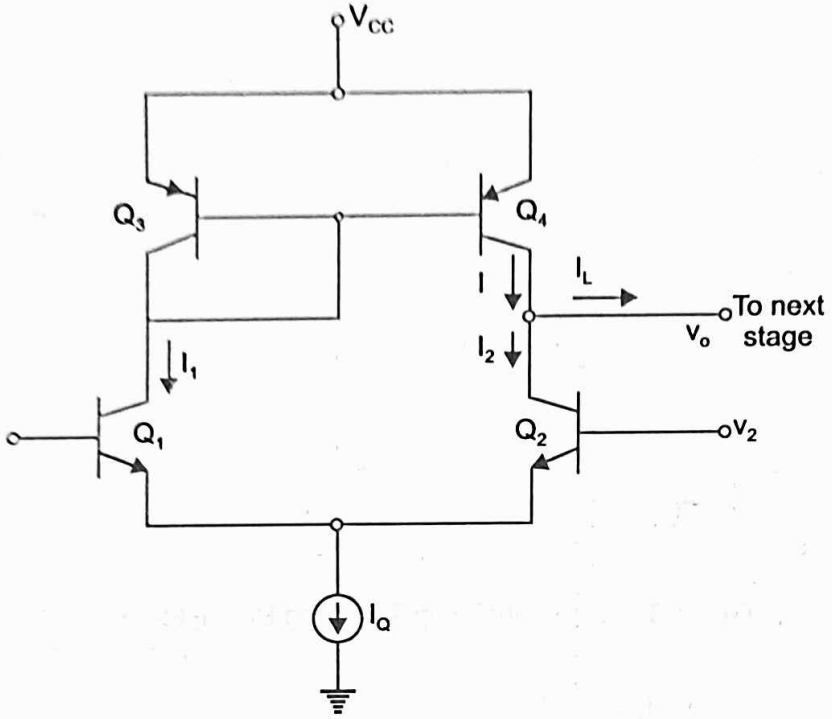


Fig. 2.31 (a) A differential amplifier with an active load Q_3–Q_4

Under the quiescent conditions, $v_1 = v_2 = 0$. From symmetry of Q_1 and Q_2, $I_1 = I_2 = I_Q/2$ where base currents are assumed to be neglected. Since Q_3 and Q_4 form a current mirror, $I = I_1 = I_2$. The load current I_L entering the next stage is

$$I_L = I - I_2 = 0 \tag{2.110}$$

However, when v_1 is increased over v_2, I_1 increases whereas I_2 decreases, since $I_1 + I_2 = I_Q$ (constant). Also the current I always remains equal to I_1 due to the current mirror. The load current is given by

$$\begin{aligned} I_L &= I - I_2 = I_1 - I_2 \\ &= g_m v_1 - g_m v_2 = g_m (v_1 - v_2) \\ &= g_m v_d \end{aligned} \tag{2.111}$$

The circuit thus behaves as a transconductance amplifier.

A popular op-amp (μA741) by Fairchild uses an alternate active load as shown in Fig. 2.31 (b). The transistors Q_1–Q_3 and Q_2–Q_4 are in cascode configuration (CE-CB) with input signal as v_1 (v_2). The transistors Q_5, Q_6 and Q_7 form the active load of the type shown in Fig. 2.24. The transistors Q_8 and Q_9 form the current mirror to provide the constant current I_Q required for high CMRR of the diff-amp. If base currents are neglected, then $I_Q \simeq I_3$. The arrangement Q_{10} and Q_{11} is another current mirror where $I_3 << I_4$ due to 5 kΩ emitter resistor. Consequently $I_Q = I_3$ is small (of the order of μA) giving a very high input resistance.

Under the quiescent conditions, $I_1 = I_2 = I_Q/2$. Since I is always equal to I_1, the load current $I_L = I_2 - I = I_2 - I_1 = 0$. Now if v_1 is increased and v_2 is decreased, I_1 rises and I_2 falls from the quiescent value of $I_Q/2$. With this excitation, $I_L = I_2 - I_1$ changes from zero to a negative value. Thus the circuit behaves as a transconductance amplifier because I_L is proportional to $v_1 - v_2$.

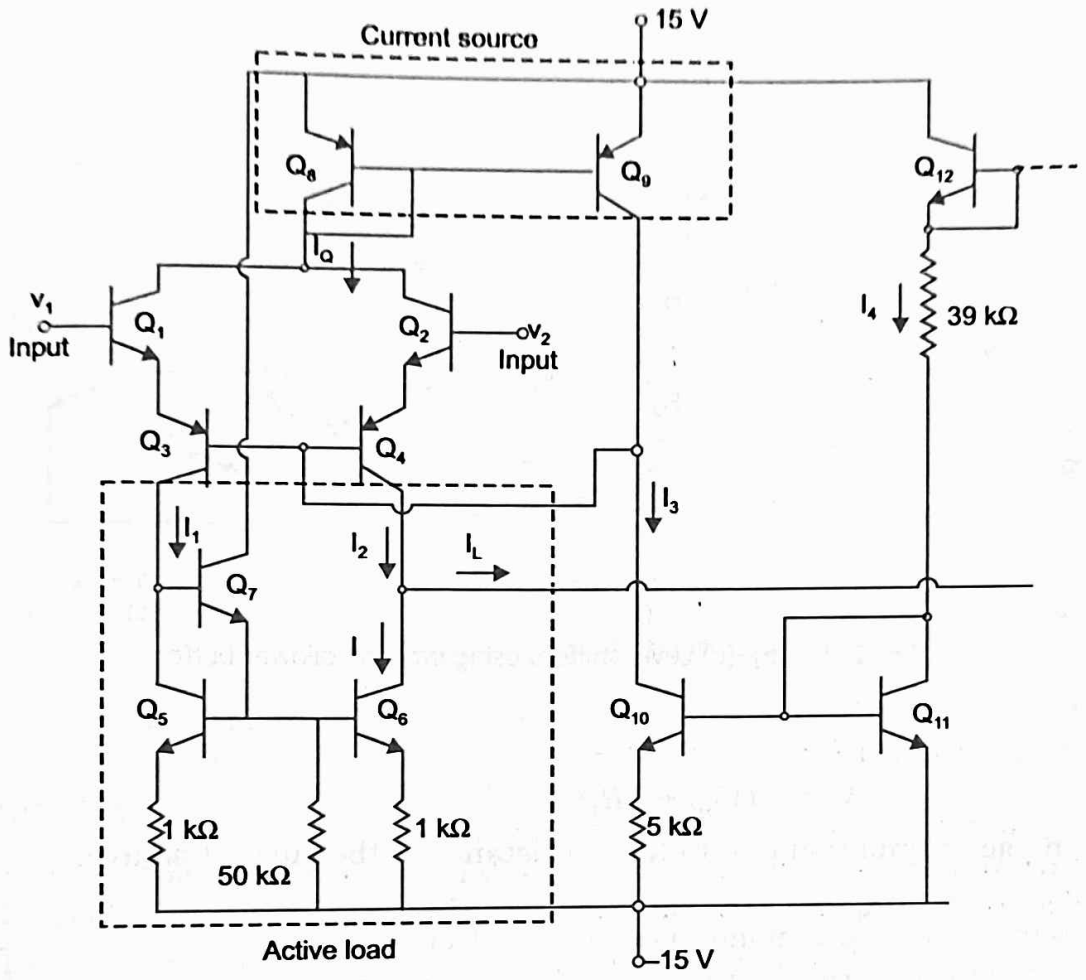


Fig. 2.31 (b) Active load (Q_5–Q_6–Q_7) of a low current differential amplifier μA741

2.4.7 Level Translator

There are two good reasons for using a level shifter in an IC op-amp. As we want an op-amp to operate down to dc, no coupling capacitor is used. Because of direct coupling, the dc level rises from stage to stage. The increase in dc level tends to shift the operating point of the next stage. This, in turn, limits the output voltage swing and may even distort the output signal. It, therefore, becomes essential that the quiescent voltage of one stage is shifted before it is applied to the next stage. Another requirement to be satisfied is that the output should have quiescent voltage level of 0 V for zero input signal.

The simplest type of a level shifter is shown in Fig. 2.32 (a). It may be noted that this is basically an emitter follower. Hence the level shifter also acts as a buffer to isolate the high gain stages from the output stage. The amount of shift obtained

$$V_o - V_i = -V_{BE} \simeq -0.7 \text{ V} \tag{2.112}$$

If this shift is insufficient, the output can be taken at the junction of two resistors R_1 and R_2, as shown in Fig. 2.32 (b). The voltage shift is now increased by the drop across R_1. However, this arrangement has the disadvantage that signal voltage also gets attenuated by $R_2/(R_1 + R_2)$. This can be easily circumvented if R_2 is replaced by a current mirror I as shown in Fig. 2.32 (c).

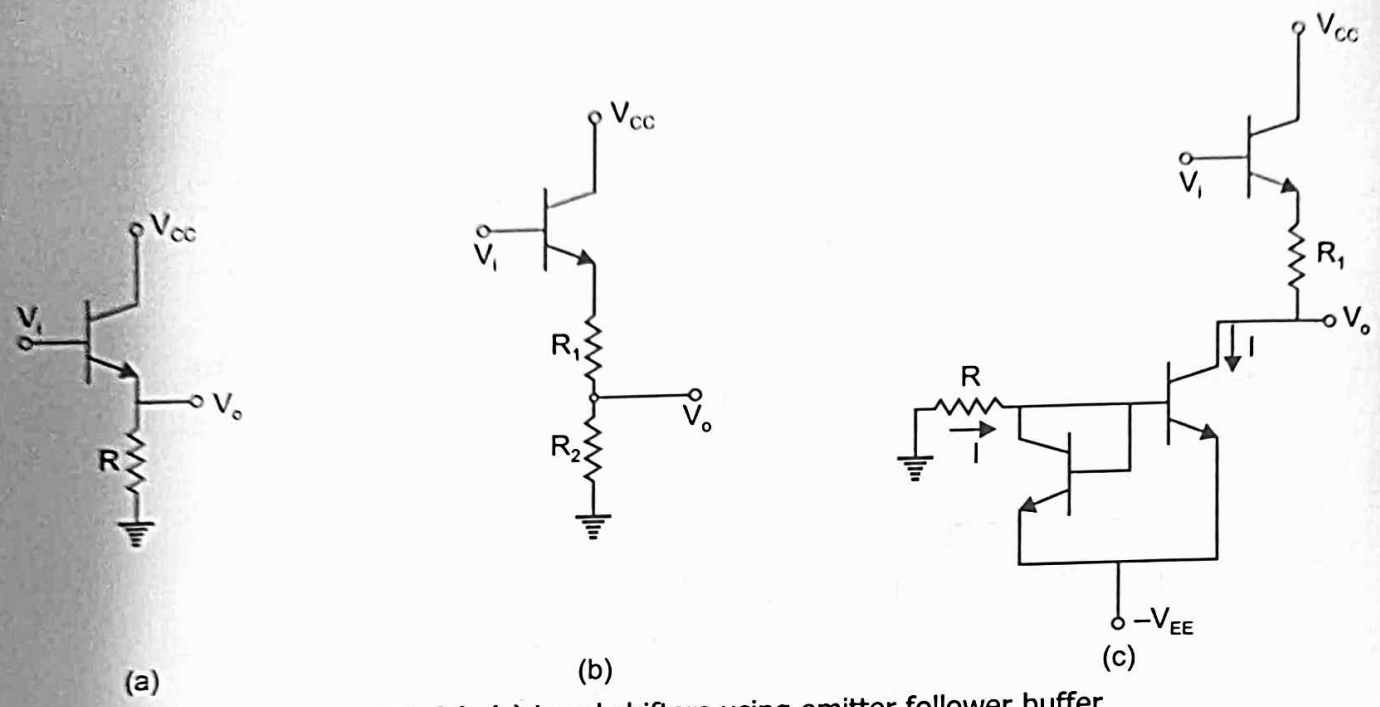


Fig. 2.32 (a)–(c) Level shifters using emitter follower buffer

The shift in level now is

$$V_o - V_i = -(V_{BE} + I R_1) \tag{2.113}$$

and there is no ac attenuation due to high resistance of the current source.

Another voltage source commonly used in μA741 op-amp is shown in Fig. 2.32 (d). It can be seen that if base current is negligible compared to the current in R_3 and R_4, then the circuit behaves as a V_{BE} multiplier as,

$$V = \frac{V_{BE}}{R_4}(R_3 + R_4) = V_{BE}\left(1 + \frac{R_3}{R_4}\right) \tag{2.114}$$

This voltage source can also be used to replace R_1 in Fig. 2.32 (b).

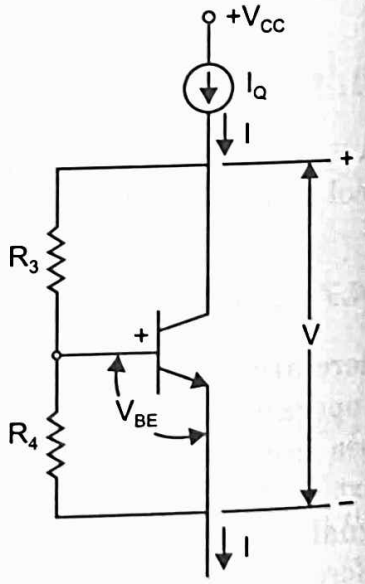


Fig. 2.32 (d) A voltage source V which is a multiple of V_{BE}

Example 2.19

Calculate $V_1 - V_2$ for the level shifter shown in Fig. 2.33. Assume identical silicon transistors with $V_{BE} = 0.7$ V and very large values of β.

Solution

Transistors Q_1 and Q_2 form a current mirror.

So, $$I_{C1} = I_{C2} = I$$

and $$I = \frac{15 - 0.7}{10\ \text{k}\Omega} = 1.43\ \text{mA}$$

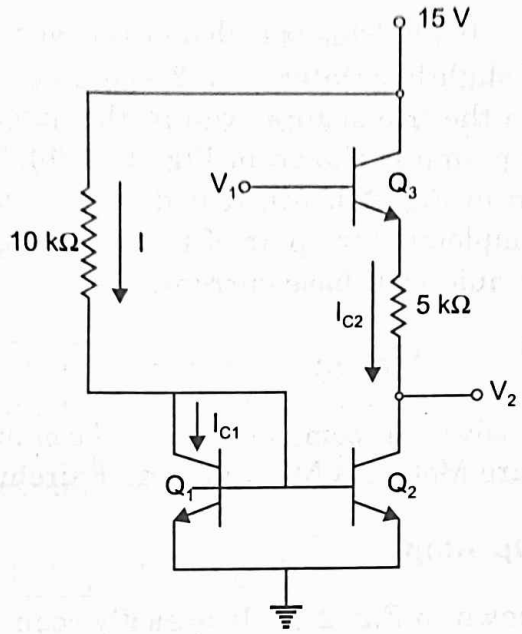


Fig. 2.33 Circuit of Example 2.19

$$V_1 - V_2 = V_{BE3} + I_{C2} \times 5\ \text{k}\Omega = 0.7\text{V} + 1.43 \times 5\ \text{k}\Omega = 7.85\ \text{V}.$$

2.4.8 Output Stage

The function of the last stage, that is, the output stage in an op-amp is to supply the load current and provide a low impedance output. It should also provide a large output voltage saving, ideally the total supply voltage *i.e.*, $V_{CC} + V_{EE}$. A simple output stage consists of two complimentary transistors Q_1 (*npn*) and Q_2 (*pnp*) connected as emitter followers as shown in Fig. 2.34 (a). It can be seen that for v_i positive, transistor Q_1 is ***on*** and supplies current to load R_L. And, if v_i is negative, Q_1 is cut off and Q_2 acts as a sink to remove current from the load R_L. There is, however, a limitation in this circuit. The output voltage v_o remains zero until the

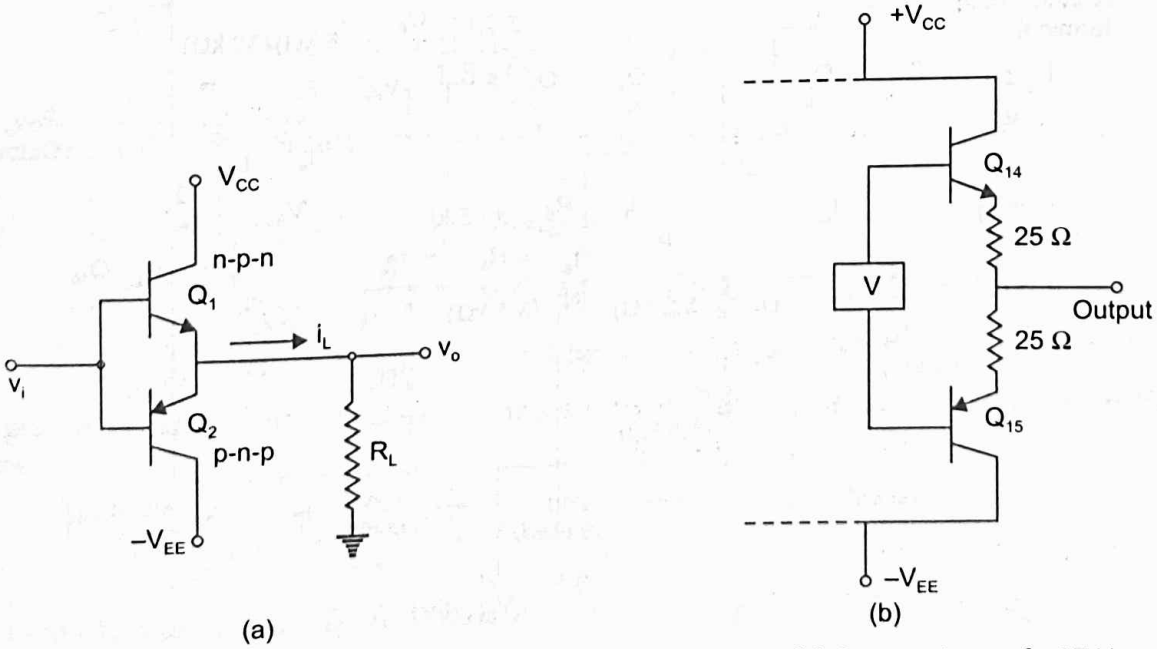


Fig. 2.34 (a) A complementary emitter follower output stage (b) Output stage of μA741

input v_i exceeds V_{BE} (cut in) = 0.5 V. This is called cross-over distortion. It can be eliminated by applying a bias voltage V slightly greater than 2 $V_{BE\,(cut\ in)}$ = 1 V between the two bases, so that a small current flows in the transistors even in the quiescent state.
The output stage of μA741 op-amp is shown in Fig. 2.34 (b). The block marked V is the V_{BE} multiplier of the type shown in Fig. 2.32 (d). It is designed to supply a voltage of about 1 V between the bases of the complementary pair of transistors Q_{14} and Q_{15}. The small emitter resistors (25 Ω) stabilize the quiescent base current.

2.5 EXAMPLES OF IC OP-AMPS

We are now in a position to analyse the complete circuit of commercially available op-amps. Two such IC op-amps discussed are Motorola MC 1530 and Fairchild μA741.

2.5.1 Motorola MC1530 Op-Amp

The circuit of MC 1530 is shown in Fig. 2.35. It is easily seen that the circuit consists of four stages. Transistors Q_2 and Q_3 form the first diff-amp stage driven by the constant current source Q_1. The output of the first diff.-amp drives the second diff.-amp formed by Q_4 and Q_5. The single ended output of the second diff-amp drives the level shifter Q_6 (emitter follower). Q_7 and diode D_3 forms another constant current source of the type shown in Fig. 2.17. The diode connected transistor Q_1 of Fig. 2.17 is shown by diode D_3 here. The output stage of MC1530 uses Q_8, Q_9 and Q_{10} where Q_9 and Q_{10} are in totem-pole configuration.

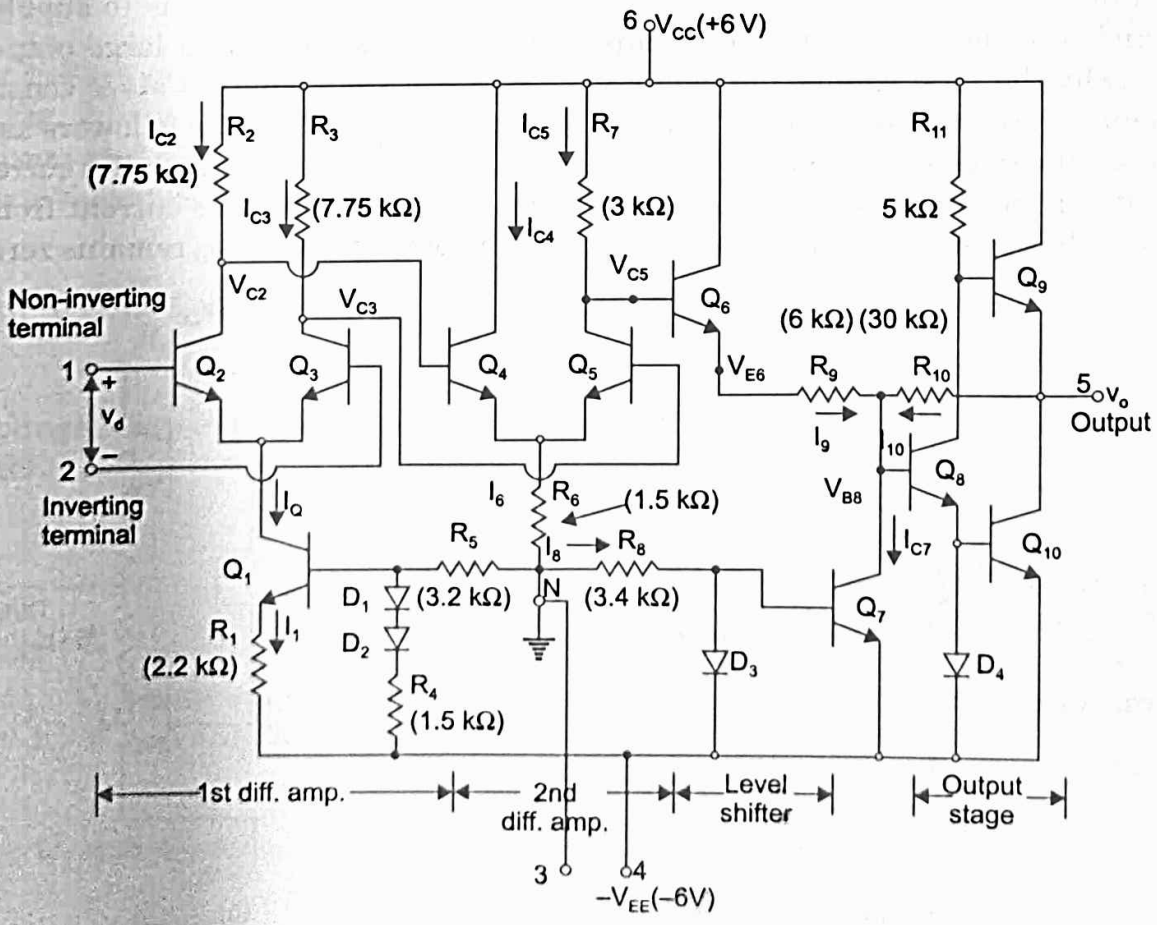


Fig. 2.35 Internal circuit of Motorola MC 1530

Example 2.20

From the circuit of Fig. 2.35 calculate:

(1) The collector current in each transistor and the output voltage under quiescent conditions.

(2) The open loop voltage gain.

Assume $h_{fe} = 100$ and $V_{BE} = V_D = 0.7$ V.

Solution

(1) The d.c. analysis is performed by assuming that both the inverting and non-inverting terminals are at ground potential. To determine the collector current in Q_2 and Q_3, first calculate the constant current I_Q. If the base current of Q_1 is neglected, then $I_Q = I_1$. The voltage V_{BN1} at the base of transistor Q_1 with respect to ground N is written using voltage divider rule as,

$$V_{BN1} = \frac{[-V_{EE} + V_D + V_D]\,R_5}{R_4 + R_5}$$

$$= \frac{(-6\text{ V} + 1.4\text{ V})\,(3.2\text{ k}\Omega)}{1.5\text{ k}\Omega + 3.2\text{ k}\Omega} = -3.13\text{ V}$$

$$I_1 = \frac{V_{EE} + V_{BN1} - V_{BE1}}{R_1} = \frac{6\text{ V} - 3.13\text{ V} - 0.7\text{ V}}{2.2\text{ k}\Omega} = 0.986\text{ mA}$$

So, $I_Q = 0.986$ mA

Under dc conditions, half of the I_Q flows through each of transistors Q_2 and Q_3. Therefore, $I_{C2} = I_{C3} = I_{Q2} = 0.493$ mA. The voltage at the collector of Q_2 and Q_3 is,

$$V_{C2} = V_{C3} = V_{CC} - R_2 I_{C2} = 6\text{ V} - (7.75\text{ k}\Omega)\,(0.493\text{ mA}) = 2.18\text{ V}$$

So the voltage at the base of Q_4 and Q_5 is 2.18 V. The dc voltage at the emitter of Q_4 is,

$$V_{E4} = V_{C2} - V_{BE4} = 2.18\text{ V} - 0.7\text{ V} = 1.48\text{ V}.$$

So,
$$I_6 = \frac{V_{E4}}{R_6} = \frac{1.48\text{ V}}{1.5\text{ k}\Omega} = 0.987\text{ mA}.$$

This current divides equally in transistors Q_4 and Q_5, so that

$$I_{C4} = I_{C5} = \frac{I_6}{2} = 0.494\text{ mA}$$

$$V_{C5} = V_{CC} - I_{C5} R_7 = 6\text{ V} - (0.494\text{ mA})\,(3\text{ k}\Omega) = 4.52\text{ V}$$

$$V_{E6} = V_{C5} - V_{BE6} = 4.52\text{ V} - 0.7\text{ V} = 3.82\text{ V}$$

Transistor Q_7 along with diode D_3 forms a current mirror of the type shown in Fig. 2.15. Hence,

$$I_{C7} = I_8 = \frac{V_{EE} - V_{D3}}{3.4} = 1.56\text{ mA}.$$

To calculate the current I_9, first calculate the voltage at the base of Q_8,

$$V_{B8} = V_{BE8} + V_{D4} - V_{EE} = 0.7\text{ V} + 0.7\text{ V} - 6\text{ V} = -4.60\text{ V}$$

$$I_9 = \frac{V_{E6} - V_{B8}}{R_9} = \frac{3.82\text{ V} + 4.6\text{ V}}{6\text{ k}\Omega} = 1.40\text{ mA}$$

$$I_{10} = I_{C7} - I_9 = 1.56\text{ mA} - 1.40\text{ mA} = 0.16\text{ mA}$$

The voltage V_o at the output terminal is,

$$V_o = I_{10}R_{10} + V_{B8} = (0.16\text{ mA})\ (30\text{ k}\Omega) - 4.60\text{ V} = 0.20\text{ V}$$
$$\simeq 0\text{ V (as expected)}$$

(2) In order to calculate the overall voltage gain, we first calculate the voltage gain of the differential amplifier stages. For this we must know the ac emitter resistance h_{ie} of the transistor used.

$$h_{ie} = \frac{h_{fe}V_T}{|I_C|}$$

where V_T is the volt equivalent of temperature = 26 mV at room temperature.

Since, $I_{C2} = I_{C3} = I_{C4} = I_{C5} \simeq 0.5$ mA

So $$h_{ie} = \frac{(100)(26\text{ mV})}{0.5\text{ mA}} = 5.2\text{ k}\Omega$$

Since emitter of Q_4–Q_5 is at ground potential under ac operation the input resistance h_{ie} of Q_4 and Q_5 is effectively in parallel to collector circuit load (R_2 and R_3) of first diff.-amp. The effective load of Q_2 and Q_3 is

$$R_{L2} = R_{L3} = 7.75\text{ k}\Omega \| 5.2\text{ k}\Omega = 3.12\text{ k}\Omega$$

The output of the first stage is double ended, its differential gain is given by Eq. (2.53) as

So, $$A_{V1} = \frac{v_{C3} - v_{C2}}{v_d} = \frac{h_{fe}R_{L2}}{h_{ie}} = \frac{100 \times 3.12\text{ k}\Omega}{5.2\text{ k}\Omega} = 60$$

For the second stage, $h_{fe} = 100$, $h_{ie} = 5.2$ kΩ and load $R_7 = 3$ kΩ (neglecting loading on Q_5 of the emitter follower Q_6). The output of the second stage is single ended, so its differential gain is,

$$A_{V2} = \frac{v_{C5}}{v_{C3}} = -\frac{1}{2}\frac{h_{fe}R_7}{h_{ie}} = -\frac{100 \times 3\text{ k}\Omega}{2 \times 5.2\text{ k}\Omega} = -28.9$$

The third stage is the emitter follower, so, $A_{V3} \simeq 1$

The last output stage uses voltage shunt feedback network R_9–R_{10},

so, $$A_{V4} \simeq \frac{R_{10}}{R_9} = -\frac{30}{6} = -5$$

Hence, the overall op-amp gain is,

$$A_V = (60)\ (-28.9)\ (-5) = 8670$$

2.5.2 741 Op-Amp

741 Op-amp has become an industry standard today. The pin configuration and the complete schematic circuit diagram for 741 op-amp is shown in Fig. 2.36 (a) and (b) respectively. Since this circuit is quite complex compared to MC1530, only the qualitative analysis is taken up.

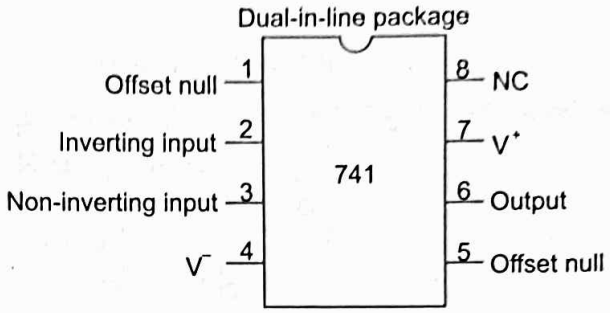


Fig. 2.36 (a) Pin configuration

In understanding an op-amp circuit as complex as this (24 transistors), first we identify the stages which provide signal gain. The input stage diff-amp consists of transistors Q_1–Q_3 and Q_2–Q_4. Transistors Q_{16} and Q_{17} provide the second stage voltage gain. Transistors Q_1Q_3 and Q_2Q_4 are in cascode (CE-CB) configuration. Two transistors in series (Q_1 feeds Q_3) provide high gain per stage needed to achieve the adequate open-loop gain in a two stage amplifier. The transistors Q_5, Q_6 and Q_7 form the active load for Q_3 and Q_4. Transistors Q_5 and Q_6 also function as a differential amplifier for the external offset nulling signal. The emitter current of transistors Q_5 and Q_6 can be controlled by varying a 10 kΩ potentiometer that is externally connected between offset null terminals as shown by dotted line in Fig. 2.36 (b). Bias currents for the input stage are provided by a complicated arrangement of current mirror pairs. Q_{12} generates a current in Q_{11}. This current is reflected over to Q_{10} (though reduced because of the emitter feedback due to R_4). This, in turn, generates a series current in Q_9 which is reflected across another mirror pair to Q_8. The bias current of Q_3 and Q_4 is effectively driven by the mirror pair Q_{10} and Q_{11}. The output of the first diff-amp is taken at the junction of Q_4 and Q_6 (point X) which acts as a complementary symmetry amplifier. The output at this point is proportional to the differential input signal. The output is now amplified by the second stage consisting of transistor Q_{16} and Q_{17} in Darlington connection.

The output of common-collector-amplifier formed by Q_{16} and R_9 drives the CE-amplifier composed of Q_{17}, R_8 and a constant current load Q_{13}. The output of CE-amplifier is a bias source for transistors Q_{18} and Q_{19}. Transistors Q_{12} and Q_{13} form a current mirror and supply current to transistors Q_{17}, Q_{18} and Q_{19}. The network consisting of transistors Q_{18}, Q_{19} and R_{10} is a fixed voltage level shifter shifting the voltage output of Q_{17} by a fixed amount on its way to the output complementary stage formed by Q_{14} and Q_{20}. The level shifter network is designed to bias the output stage in the linear region. The transistors Q_{18} and Q_{19} also separate the bases of Q_{14} and Q_{20} by two diode drops and thus temperature compensate currents in Q_{14} and Q_{20}. Transistor Q_{22} performs two functions. It serves as a buffer between Q_{17} and Q_{20} and also provides a negative feedback to Q_{16}. The final output is taken at the junction of R_6 and R_7. The output complementary pair operates so that depending upon the sign of the output, only one of the transistors Q_{14} or Q_{20} is conducting at any time. With no input signal, both devices are turned off, resulting in a low quiescent current drain in the output stage.

Transistors Q_{15}, Q_{21} and Q_{23} protect the circuit by limiting current to the output complementary stage. If the output (load) current exceeds the safe limit, the voltage drop across R_6 and R_7 increases. This turns on Q_{15} and Q_{21} which in turn makes Q_{23} on. This however shorts out, that is turns off the amplifier Q_{16}–Q_{17}. This reduces the emitter current in Q_{22} and in turn current in Q_{18} and Q_{19}. The reduction in the currents of Q_{18} and Q_{19} lowers the currents in Q_{14} and Q_{20}. The diode-connected transistor Q_{24} is a temperature compensating diode for

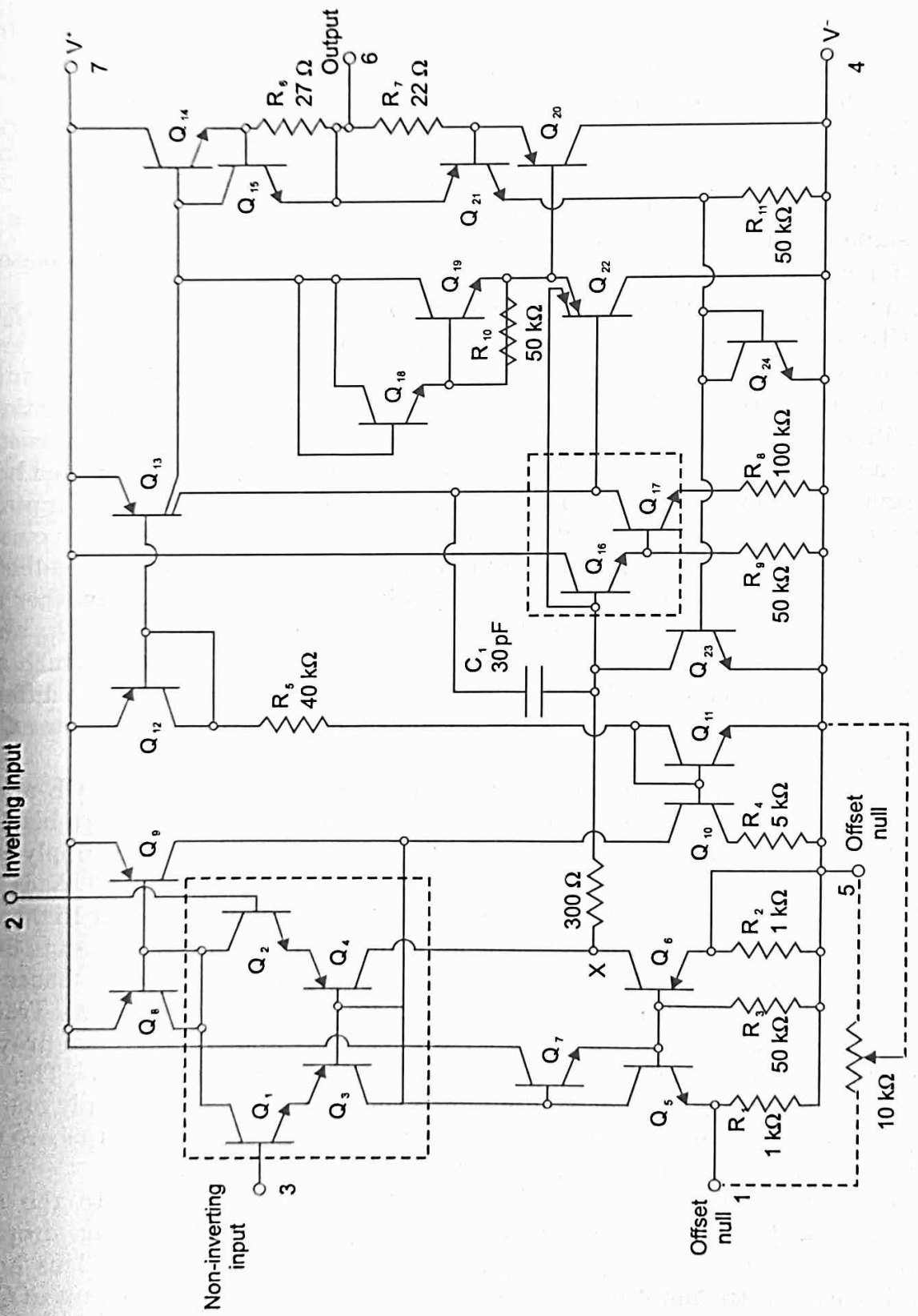


Fig. 2.36 (b) Schematic circuit diagram for 741 op-amp

transistor Q_{23}. Finally the internal 30-pF capacitor provides the high frequency roll-off to stabilize the circuit.

Example 2.21

For the op-amp circuit shown in Fig. 2.37, assume $h_{fe} = 100$, $V_{BE} = 0.7$ V.

(i) Perform the dc analysis. Note that the transistor Q_7 has four times the areas of transistors Q_3 and Q_4.

(ii) Compute the overall voltage gain.

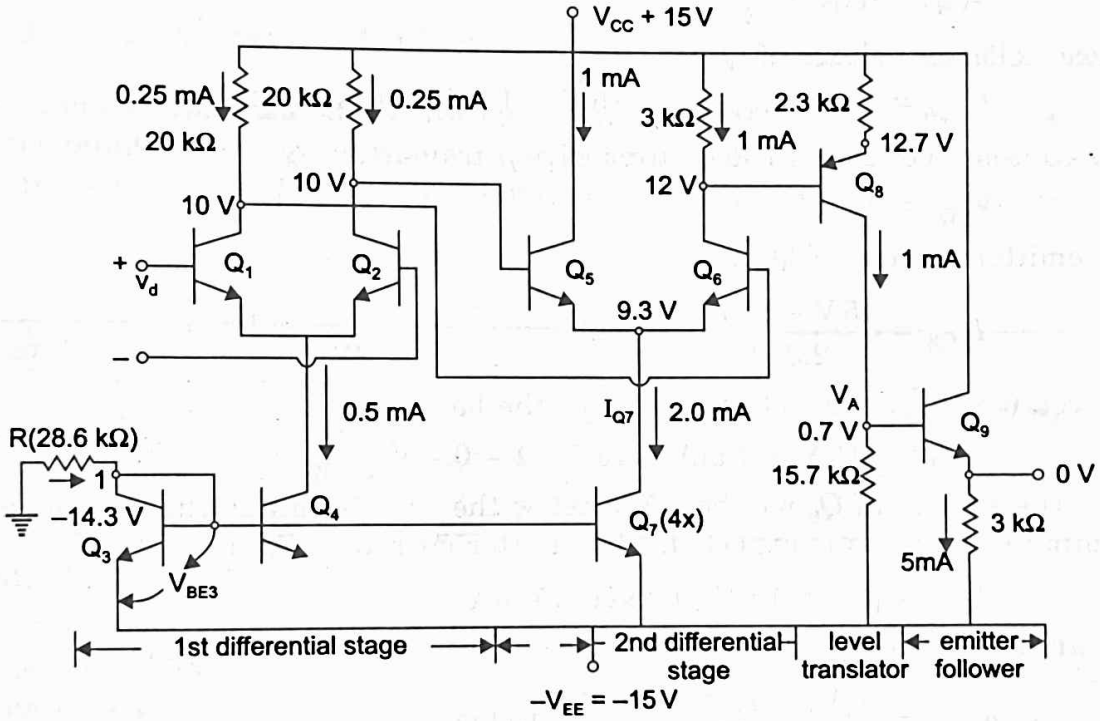


Fig. 2.37 Circuit for Example 2.21

Solution

It can be seen that the circuit has the following four stages:

(i) Dual-input, differential-output

(ii) Dual-input, single-ended output

(iii) Level translator

(iv) Emitter follower.

(i) For **dc analysis**, assume that the input terminals are shorted to ground. The reference current I of the current minor Q_3–Q_4 is obtained as

$$I = \frac{V_{EE} - V_{BE3}}{R} = \frac{15\text{V} - 0.7\text{V}}{28.6\ \text{k}\Omega} = 0.5\ \text{mA}$$

Due to current mirror action,

$$I_{CQ4} = I = 0.5\ \text{mA}$$

and $$I_{CQ1} = I_{CQ2} = I_{CQ4}/2 = 0.25\ \text{mA}$$

Thus, each of Q_1 and Q_2 are biased at 0.25 mA. The collector voltages for Q_1 and Q_2 are

$$V_{CQ1} = V_{CQ2} = V_{CC} - I_{C1}R_{C1} = 15\ \text{V} - 0.25\ \text{mA} \times 20\ \text{k}\Omega = +10\ \text{V}$$

Now, proceeding to the next differential stage, voltage at the emitter of Q_5 and Q_6 will be

$$V_{EQ5} = V_{EQ6} = 10\text{ V} - 0.7\text{ V} = 9.3\text{ V}$$

The differential pair Q_5–Q_6 is biased by the current mirror transistor Q_7. Since the area of Q_7 is 4 times that of Q_3 and Q_4, the transistor Q_7 supplies a current $4 \times 0.5 = 2$ mA.

Thus, collector currents of Q_5 and Q_6 are

$$I_{CQ5} = I_{CQ6} = \frac{I_{Q7}}{2} = 1\text{ mA}$$

Hence, collector voltage of Q_6 is

$$V_{CQ6} = V_{CC} - I_{CQ6}R_{C6} = 15\text{ V} - 1\text{ mA} \times 3\text{ k}\Omega = 12\text{ V}$$

This causes a voltage at the emitter of *pnp* transistor Q_8 at

$$V_{EQ8} = 12.7\text{ V}$$

The emitter current of Q_8 is

$$I_{EQ8} = \frac{15\text{ V} - 12.7\text{ V}}{2.3\text{ k}\Omega} = 1\text{ mA}$$

The voltage V_A at the collector of Q_8 or the base of Q_9 is

$$V_A = -15\text{ V} + 1\text{ mA} \times 15.7\text{ k}\Omega = 0.7\text{ V}$$

Since the emitter of Q_9 will be 0.7 V below the base terminal, the voltage at the output terminal 6 is 0 V as is expected. The emitter current of Q_9 is

$$I_{EQ9} = [0 - (-15\text{ V})] / 3\text{ k}\Omega = 5\text{ mA}$$

(ii) **a.c. analysis.** The ac emitter resistance of the transistor Q_1–Q_2 is

$$h_{ie_{(Q_1-Q_2)}} = \frac{h_{fe}V_T}{|I_C|} = \frac{100 \times 25\text{ mV}}{0.25\text{ mA}} = 10\text{ k}\Omega$$

The ac emitter resistance of transistor Q_5–Q_6 is

$$h_{ie_{(Q_5-Q_6)}} = \frac{100 \times 25\text{ mV}}{1\text{ mA}} = 2.5\text{ k}\Omega$$

Since emitter of (Q_5–Q_6) is at ground potential under ac conditions, the effective load for Q_1–Q_2 is

$$R_{L1} = R_{L2} = 20\text{k}\Omega\,||\,2.5\text{k}\Omega = 2.2\text{ k}\Omega$$

Voltage gain of the first differential stage is

$$A_{DM1} = \frac{h_{fe}R_{L2}}{h_{ie}} = \frac{100 \times 2.2\text{ k}\Omega}{10\text{ k}\Omega} = 22\text{ k}\Omega$$

Voltage gain of second stage which is differential input, single-ended is

$$A_{DM2} = -\frac{1}{2}\frac{h_{fe}R_{L6}}{h_{ie}}$$

Assuming no loading effect on this stage due to level translator stage,

$$A_{DM2} = -\frac{1}{2} \times \frac{100 \times 3\text{ k}\Omega}{2.5\text{ k}\Omega} = -60\text{ k}\Omega$$

The gain of the level translator stage is

$$A_3 \cong -\frac{R_L}{R_E} = -\frac{15.7\ \text{k}\Omega}{2.3\ \text{k}\Omega} = -6.82\ \text{k}\Omega$$

The last stage is emitter follower, so its voltage gain $A_{V4} \cong 1$.
So, the overall voltage gain is

$$A_V = (22)\ (-60)\ (-6.82)\ (1) = 9002$$

2.6 FET OPERATIONAL AMPLIFIER

The op-amp circuits discussed so far are bipolar op-amps. Op-amps using field transistors (FETs) in the input stage offer some very significant advantages over bipolar op-amps, especially in areas as input impedance, input bias and offset currents and slewing rate as shown in Table 2.1.

Table 2.1

Parameter	*BJT*	*JFET*	*MOSFET*
Input resistance	kΩ	10^9 Ω (giga-ohms)	10^{12} Ω (tera-ohms)
Input gate current	μA	1 nA	1 pA
Input offset current	20 nA	2 pA	0.5 pA
Slewing rate	1 V/μs	3 V/μs	10 V/μs

FET Differential Amplifier

The circuit of a basic source-coupled differential amplifier using MOSFET is shown in Fig. 2.38. The analysis for finding A_{DM} and A_{CM} is similar to what has been done for BJT differential amplifiers.

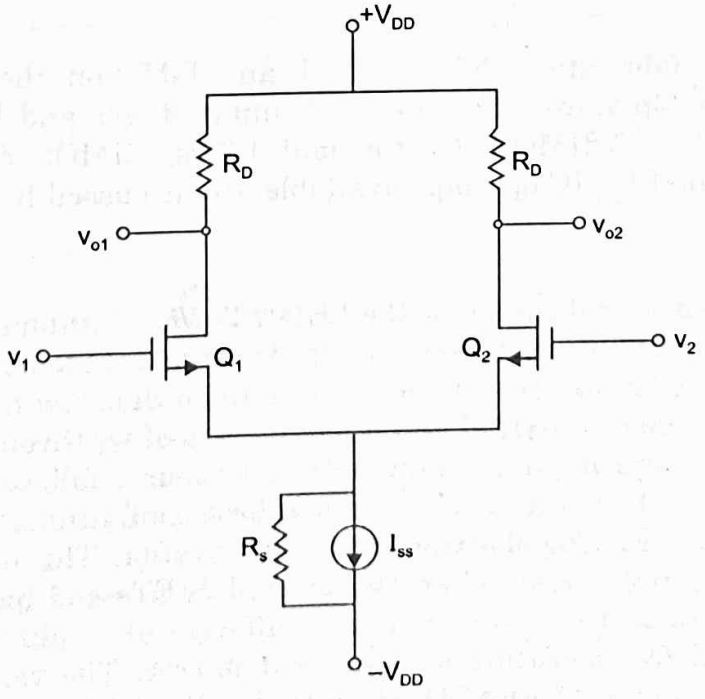


Fig. 2.38 A MOSFET differential amplifier

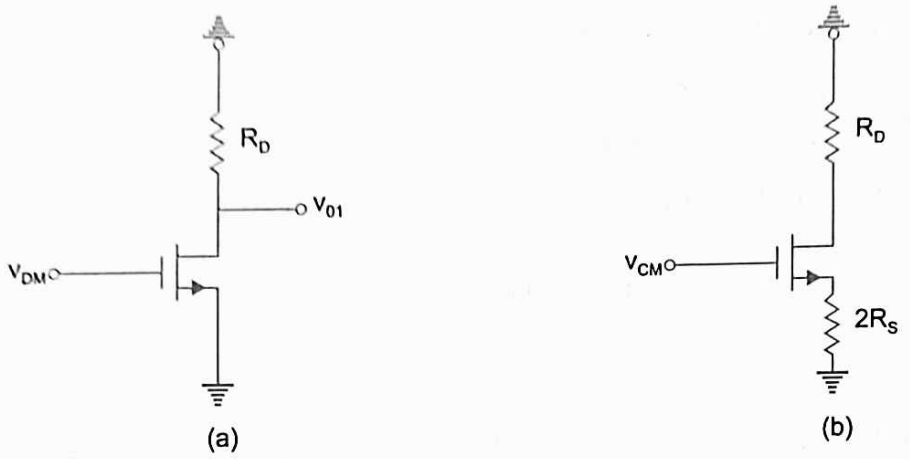


Fig. 2.39 a.c. equivalent circuit for (a) Differential-mode (b) Common-mode signals

The differential mode gain, A_{DM}, and common-mode gain, A_{CM}, can be obtained from the a.c. equivalent circuits shown in Fig. 2.39 (a) and (b) respectively as

$$A_{DM} = -\frac{\mu R_D}{r_d + R_D} \tag{2.115}$$

and

$$A_{CM} = -\frac{\mu R_D}{r_d + R_D + 2(1+\mu)R_S} \tag{2.116}$$

$$\therefore \quad \text{CMRR} = \frac{|A_{DM}|}{|A_{CM}|} = \frac{r_d + R_D + 2(1+\mu)R_S}{r_d + R_D} = 1 + \frac{2(1+\mu)R_S}{r_d + R_D} \tag{2.117}$$

For $r_d >> R_D$ and $\mu >> 1$, Equation reduces to

$$\text{CMRR} = 1 + 2\, g_m R_S \approx 2\, g_m R_S \tag{2.118}$$

It is now possible to fabricate JFET/MOSFET and BJTs on the same chip using ion implantation techniques. Op-amps which use FET input stages and BJT for the remaining stages are termed as BIFET/BIMOS. By the mid 1980s, BIMOS circuits were produced commercially. Some of the FET IC op-amps available are discussed here briefly.

JFET Op-amps

An example of a FET input hybrid op-amp is the LH0022/42/52 (National semiconductor) series. This op-amp uses a pair of JFET transistors only for the input-stage differential amplifier and the rest of the circuit uses bipolar transistors. A simplified diagram of this op-amp is shown in Fig. 2.40. The input-stage differential amplifier consists of Q_1 through Q_4 in which Q_1 and Q_2 are n-channel JFETs operating in a common-drain or source-follower configuration. These JFETs drive Q_3 and Q_4 which operate in the common-base configuration. Thus the differential amplifier uses a compound JFET/bipolar transistor configuration. This provides very high input resistance and very low input current characteristics of JFETs and high-voltage gain that is obtainable from bipolar transistors. This compound differential amplifier drives an active load consisting of Q_5 through Q_7, operating as a current mirror. The rest of this op-amp is of conventional design as discussed for μA741. Here diodes D_1 and D_2 are used to provide a pre-bias across Q_{14} and Q_{20} to minimize cross-over distortion.

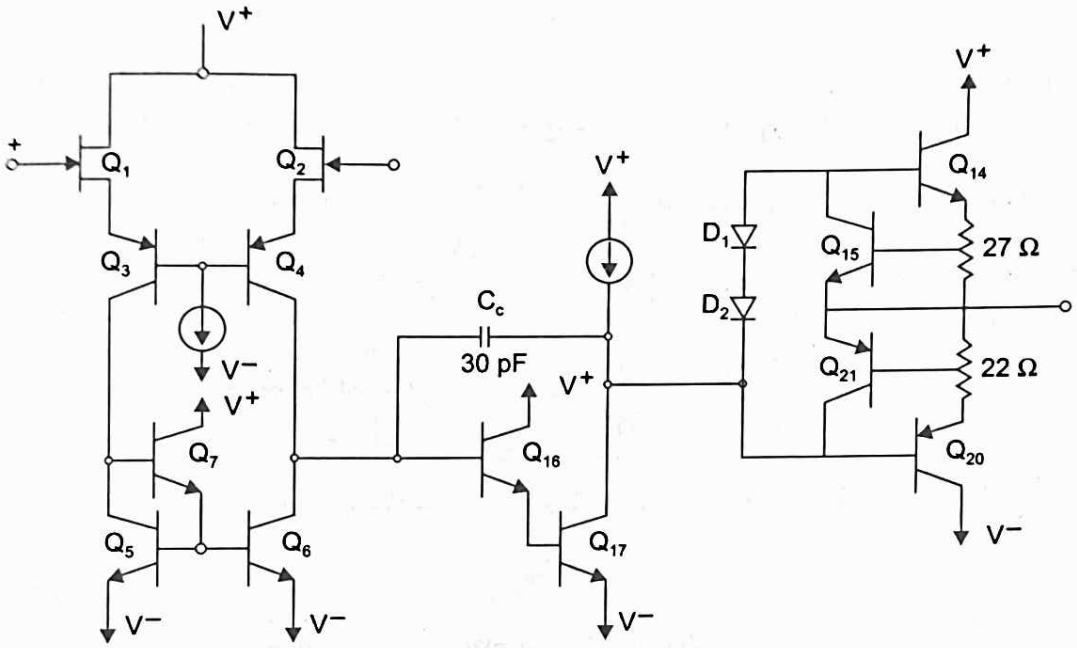


Fig. 2.40 Hybrid JFET-input op-amp LH00 22/42/52 series (National Semiconductor)

CMOS Op-amps

The bipolar op-amp IC 741 is capable of sourcing and sinking large load currents. This is facilitated by the emitter-follower output stage which achieves very low output resistance, and this characteristic was used in IC 741 for minimizing the loading effects.

On the other hand, the CMOS op-amps are normally designed for particular applications, wherein only a few picofarads of capacitive loads are required to be driven. Therefore, most of the CMOS op-amps do not require a low resistance output stage. When the op-amp input terminals are not connected directly to the IC external terminals, they do not need electrostatic input protection devices also. The folded cascade op-amp using a current mirror CMOS is discussed.

Description of the Circuit

Figure 2.41 shows a simplified circuit diagram of an all-CMOS op-amp MC14573. The PMOS transistors Q_1 and Q_2 form the input diffential pair, and the NMOS transistors Q_3 and Q_4 form the active load of the differential pair. The differential amplifier input stage is biased by the transistors Q_5 and Q_6 which form a current mirror. The reference current for the current mirror is determined by an external resistor, R_s.

The second stage acting as the output stage consists of the common-source connected transistor Q_7. The transistor Q_8 provides the bias current acting as the active load for the transistor Q_7 . An internal compensation capacitor C_1 is connected between the drain and gate of transistor Q_7 to provide stability.

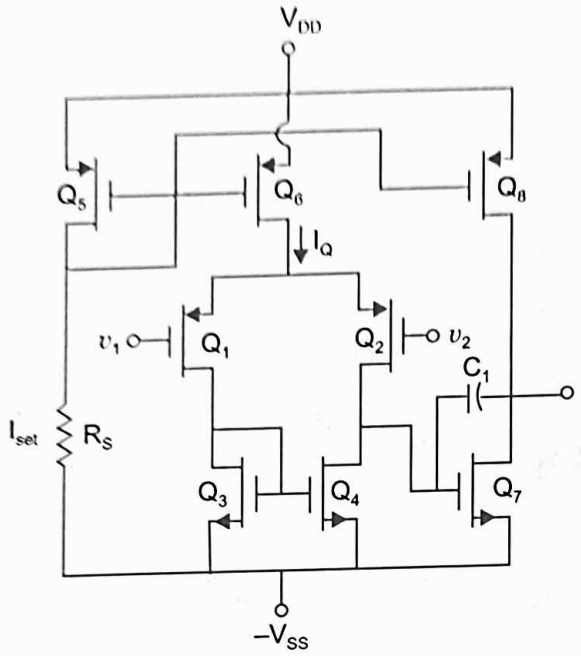


Fig. 2.41 Simplified circuit of CMOS op-amp MC 14573

The pin diagram of the quad low-power op-amp is shown in Fig 2.42.

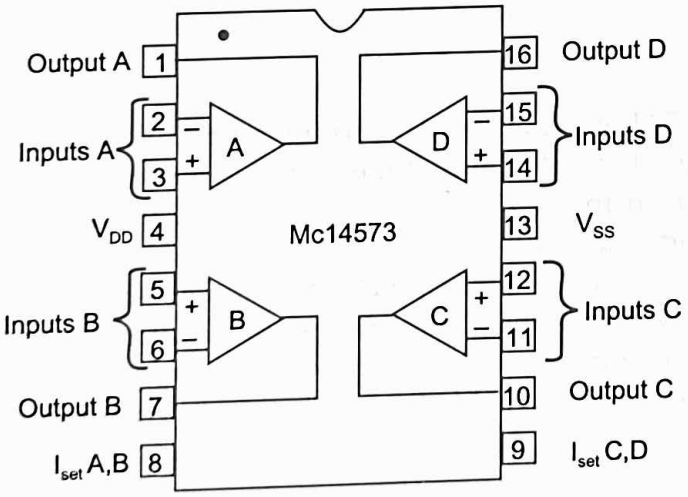


Fig. 2.42 Pin diagram of quad op-amp MC14573

It consists of four op-amps configured using CMOs devices in a monolithic structure. The operating current is programmable using the resistor connected at pin 9 and it is set by the resistor R_s connected between V_{ss} and any one or both of the I_{set} pins 8 and 9. This makes the IC versatile for making a trade-off between the power dissipation and slew rate characteristics. The op-amps are internally compensated. The set current for each op-amp pair of the comparator is given by $I_{set} = \dfrac{V_{DD} - V_{ss} - 1.5V}{R_s}$ where R_s represents the single programming resistor.

When two programming resistors are employed, the set currents are given by $I_{set} = \frac{V_{pp} - V_{ss} - 1.5V}{2R_s}$. The total device current is typically thirteen times that of I_{set} per pair when the outputs are in *low* state, whereas it is five times I_{set} per pair when the outputs are in *high* state. When the op-amps are employed in the linear region, the device current is set between the values of five and thirteen times I_{set}.

While using a single op-amp, the I_{set} terminal for the pair is normally tied to V_{DD} for achieving minimum power consumption. For minimizing the power consumption of the unused pair of comparators, it is preferable to use a high value set resistor R_S with the inputs connected to a voltage that will force the output to V_{DD}. It is to be noted that increasing the value of I_{set} for comparators will decrease the propagation delay. The normally obtainable maximum output voltage V_{OH} for a given value of load resistor R_L with respect to V_{SS} is given by

$$V_{OH} = 4 \times I_{set} \times R_L - 0.05V.$$

The typical op-amp slow rate (SR) value that can be obtained by MC14573 is given by $SR \approx 0.41\ I_{set}$.

The MC14574 and MC14575 also fall in the family of quad op-amps and comparators. These ICs are excellent building blocks for consumer, industrial, automotive and instrumentation applications. Some applications of these ICs are in active filters, voltage reference circuits, waveform generator circuits, ADCs and comparator circuits. These ICs are usable in both line and battery operated applications.

BiFET and BiMOS CIRCUITS

The fabrication technologies employing ion implantation techniques permit the fabrication of JFETs, MOSFETs and BJTs on the same substrate as a single chip. The terminologies BiFET and BiMOS normally refer to the ICs fabricated by this process. All of the BiFET and BiMOS op-amps use the FET as the input stage followed by the BJTs for the internal gain stages and output stages. Therefore, they achieve the advantages of both the bipolar and MOSFET devices for the same circuit. The main advantage of MOSFETs is their very high input impedance. Hence, when the MOSFETs form the input differential pair of an op-amp, the input bias currents achieved are extremely small. However, the equivalent noise of the input stage may be greater than that of an all-BJT op-amp.

The amplifiers with FET input stages evolved in the 1970s and by the next decade commercial ICs were commonly available in the market. This is due to the advantageous and onerous features shown by the FET differential input stages, namely, the higher differential mode input resistance, lower input current, reduced input offset currents and higher slew rates to name a few. The higher input resistance of a FET is due to the very high gate to source resistance, which is nearly an open circuit as against the r_{Π} of the bipolar transistor. It is normally four orders of magnitude larger than that of the BJTs. The input bias current of the FET is the reverse saturation current I_{ss} of the gate of channel junctions in reverse biased condition. This is normally much smaller than the base current of a BJT while assuming equal values of collector and drain currents($I_C = I_{DS}$) for the two types of transistors. Since the input current $I_{in} = I_{GSS}$ is very small, the offset current that is generated due to device mismatches is also very small than those arising in BJT based circuits. The MOSFET differential stages augment in further reducing these quantities, since the leakage current through the gate oxide is still

smaller than I_{GSS} of the JFETs. For equal values of I_C and I_{DS}, the value of g_m of a FET is smaller than that of a BJT. Hence, the smaller value of g_m results in an increased slew rate in a FET. On the other hand, the lower value of g_m makes the diffential mode gain A_{DM} of FETs less than that of BJT circuits. This limitation is overcome in the BiFET and BiMOS op-amps designs by incorporating three stage architectures as made available in AD611 type of ICs. Finally, the additional advantage of FET input stage is the lower noise effects, which makes the FETs configuring lower noise, low voltage and low power devices as compared to BJTs.

Three Stage Op-Amp

Most of the high frequency and the BiFET (BiMOS) op-amp normally constitute three gain stages, viz, a differential amplifier input stage, two gain stages incorporated with the level-shifter stages and an output stage, which is normally an emitter-follower stage. The architecture of a typical three stage op-amp is shown in Fig. 2.4.3. Since the use of the three stages facilitate higher open-loop gain, the g_m of the differential stage can be reduced, which results in improved slew rate as given by

$$SR = 8\pi V_T f_T$$

where V_T is volts equivalent of temperature

f_T is unity gain bandwidth

Moreover, the three-stage architecture with feedback can be designed to have higher values of the gain-crossover frequency f_T than are commonly obtainable in two-stage op-amps. Therefore, both the slew-rate and unity gain bandwidth performance characteristics of the op-amp are increased.

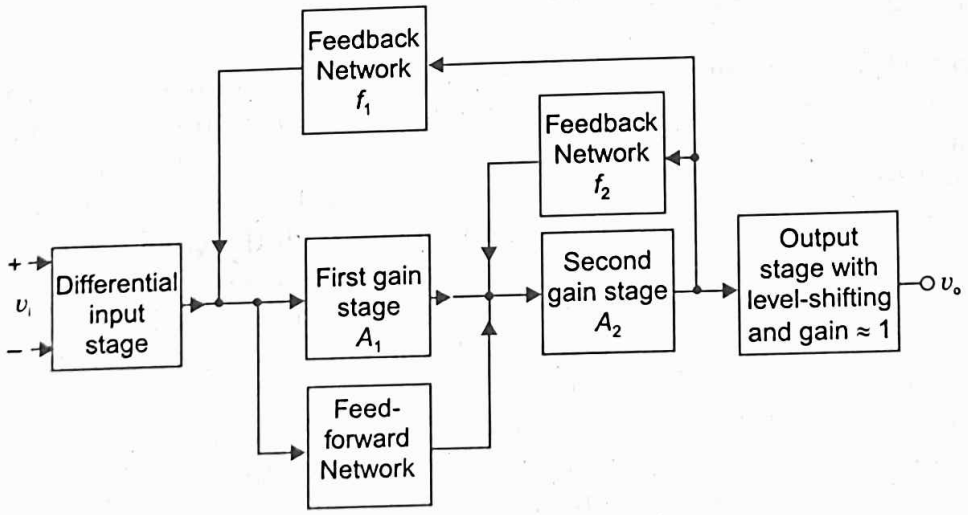


Fig 2.43 Three stage Op-amp architecture

Since each of the stages contribute for a dominant pole in the open-loop amplifier the stabilization and compensation become more difficult. Therefore, feedback network circuits are necessitated for achieving frequency compensation in the amplifier. Typically, each of these circuits is formed by RC networks rather than the single capacitor. This overall feedback loop f_1 around both the gain stages is used to obtain a dominant pole in the openloop transfer function. The inner feedback loop f_2 is designed to make the pole of second gain stage the non-dominant pole of the amplifier. A zero in the amplifier transfer function is introduced by the feed-forward network. The positive phase shift produced by this zero improves the phase margin of the stage and it also helps in stabilizing the amplifier. In addition, the positive phase

shift attempts in increasing the gain-crossover frequency f_T. The LM118 from National Semiconductor is a three-stage op-amp with a unity gain bandwidth of 15 MHz and a slew rate of 50 V/μs.

The following section discusses the CA3140 BiCMOS op-amp. Many of the features of this op-amp are similar to those of the IC 741.

Circuit Description

Figure 2.44 shows the basic equivalent circuit of the CA3140 op-amp. The op-amp consists of three basic stages, namely, the input differential stage, the gain stage and the output stage. The circuit also consists of the bias circuit that establishes the dc bias currents in the op-amp and a dynamic current sink. Typical supply voltages used for the IC are $V^+ = 15$ V and $V^- = -15$ V.

Input differential amplifier The input differential pair consists of *P*-channel MOS transistors M_9 and M_{10}, and transistors Q_{11} and Q_{12} from the active load for the diff-amp. A single-sided output at the collector of Q_{12} acts as the input to the next gain stage. Two offset null terminals are also provided for offset null facility.

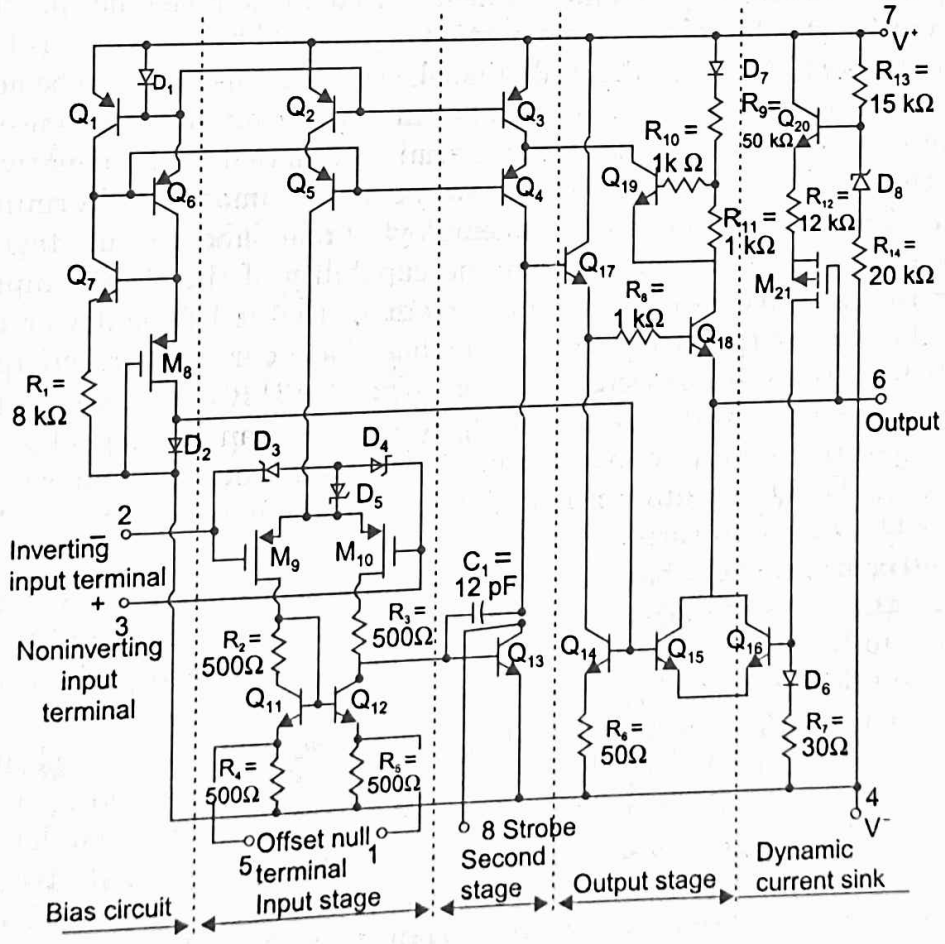


Fig. 2.44 CA3140 BiCMOS op-amp equivalent circuit

The MOS transtors are very susceptible to electrostatic charges. For example, electrostatic voltage can be accidentally induced on the gate of a MOSFET even during routine handling. These voltages may be large enough to induce breakdown in the gate oxide, thus destroying the device. Therefore, necessary protection of the input against electrostatic damage is provided by

the Zener diodes D_3,D_4 and D_5. When the gate voltage becomes sufficiently high, the diodes facilitate a discharge path for the electrostatic charge, thereby protecting the gate oxide from breakdown.

Bias circuit The dc current biasing is provided by the bias circuit and quiescent current in all stages, (except the dynamic current sink) of the CA3140 is dependent upon bias current flow in R_1. The function of the bias current is establishing and maintaining a constant current flow through D_1, Q_6, M_8 and D_2. Here D_1 and D_2 are diode connected transistors. D_1 is connected in parallel with the base-emitter junctions of Q_1,Q_2 and Q_3. D_1 may be considered as a current sampling diode that senses the emitter current of Q_6 and it automatically adjusts the base current of Q_6 (via Q_1) to maintain a constant current through Q_6, M_8 and D_2. The base currents in Q_2 and Q_3 are also determined by constant current flow through D_1. Furthermore, current in diode connected transistor Q_2 establishes the currents in transistors Q_{14} and Q_{15}. The combination of Q_6 and Q_7 pair makes the bias current independent of the power supply voltages. Diodes D_1 and D_2 are diode-connected transistors. The transistors Q_1 and diode D_1 being matched devices make the currents in the two branches of the bias circuit equal, and the value of current is set by Q_7, R_1 and M_8.

Gain stage Most of the voltage gain in the CA3140 is provided by the second amplifier stage, consisting of bipolar transistor Q_{13} and its cascade-connected load resistance provided by bipolar transistors Q_3 and Q_4. On-chip phase compensation is provided by C_1, which is found sufficient for a majority of the applications. Additional Miller-Effect compensation can be accomplished by introducing a small capacitor between Terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence condition. When Terminal 8 is tied to the negative supply point at Terminal 4, the output Terminal 6 swings low, i.e. approximately to Terminal 4 potential.

Output stage The CA3140 series circuits employ a broadband output stage that can sink loads to the negative supply to complement the capability of the PMOS input stage while operating near the negative rail. Quiescent current in the emitter-follower cascade circuit (Q_{17},Q_{18}) is established by transistors (Q_{14},Q_{15}) whose base currents are *mirrored* to current flowing through diode D_2 in the bias circuit section. When CA3140 operates such that the output terminal 6 is sourcing current, the transistor Q_{18} functions as an emitter-follower for sourcing current from the positive supply (V^+ at terminal 7) via D_7,R_9 and R_{11}. Under these conditions, the collector potential of Q_{13} is sufficiently high to permit the necessary flow of base current to emitter follower Q_{17} which, in turn drives Q_{18}.

When CA3140 operates such that the output terminal 6 is sinking current to the negative supply (V^-) bus, the transistor Q_{16} acts as the current sinking element. Transistor Q_{16} is mirror-connected to D_6, R_7 with current fed by way of M_{21},R_{12} and Q_{20}. The transistor inturn, is biased by current flow through R_{13}, zener D_8 and R_{14}. The dynamic current sink is controlled by voltage level sensing. The output terminal 6 is quiescently established at the potential midpoint between the V^+ and V^- supply rails. When output current-sinking mode operation is required, the collector potential of transistor Q_{13} is driven below its quiescent level, thus causing Q_{17},Q_{18} to decrease the output voltage of terminal 6. Therefore, the gate terminal of PMOS transistor Q_{21} is displaced towards the negative supply, thereby reducing the channel resistance of Q_{21}. As a consequence, there is rise in the current flow through Q_{20}, R_{12}, Q_{21}, D_6, R_7, and the base of Q_{16}. As a result, Q_{16} sinks current from terminal 6 in response to the incremental change in output voltage caused by Q_{18}. This sink current flows regardless of load, and any excess current is internally supplied by the emitter-follower formed by Q_{18}. Short circuit protection of the output circuit is provided by Q_{19} that is driven into conduction by the high voltage drop developed across R_{11} under output short-circuit conditions. Then, the collector of Q_{19} diverts current from Q_4 thereby reducing the base current drive from Q_{17} and limiting current flow in Q_{18} to the short circuited load terminal.

DC Analysis

The basic bias circuit of CA3140 BiCMOS op-amp is shown in Fig 2.45. The current mirror formed by the matched devices Q_1 and D_1 ensures that the two branch currents I_1 and I_2 are equal. The P-channel MOSFET M_8 is to operate in saturation region. Hence, it is necessary to satisfy the condition

$$V_{SD} > V_{SG} - |V_{Th}| \tag{2.119}$$

From Fig. 2.45, we find

$$V_{SG} = V_{SD} + |V_D|$$

i.e.
$$V_{SD} = V_{SG} - |V_D| \tag{2.120}$$

From the above two equations, we have

$$V_{SG} - V_D > V_{SG} - |V_{Th}| \tag{2.121}$$

This indicates that $|V_{Th}| > V_D$. Here, for M_8 to remain biased in the saturation region, the magnitude of the threshold voltage must be greater than the diode voltage.

From the left side of the bias current, the current is expressed by

$$I_2 \cong I_{R1} = \frac{V_{SG} - V_{BE7}}{R_1} \tag{2.122}$$

and from the right side of the circuit, we have

$$I_1 = k_p (V_{SG} - |V_{Th}|)^2 \tag{2.123}$$

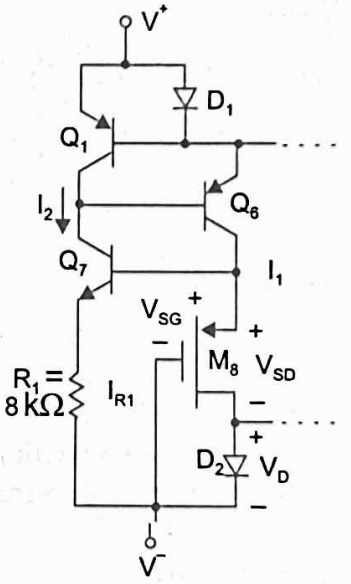


Fig. 2.45 Bias circuit of CA3140 BiCMOS op-amp

Hence Eqs.(2.122) and (2.123) develop the currents and voltages in this bias circuit.

Transistors Q_1 through Q_6 along with diode D_1 of Fig 2.45 are all matched devices. Hence, $I_{C5} = I_{C4}$. The current in D_2 sets the diode voltage, which also biased D_{14} and D_{15}.

Small-singal Analysis

The small-signal voltage gain of the CA3140 op-amp can be analyzed as follows.

Input stage The small-signal differential voltage gain for the CMOS op-amp is given by

$$A_d = \sqrt{2k_p I_{Q5}}\,(r_{o10} \,\|\, R_{act1} \,\|\, R_{i2}) \tag{2.124}$$

where I_{Q5} is the bias current supplied by Q_2 and Q_5, r_{10} is the output resistance seen looking into the drain of M_{10}, R_{act1} is the active load resistance and R_{i2} is the input resistance of the gain stage.

Gain stage The small-signal voltage gain for the second stage is given by

$$|A_{v2}| = g_{m13}(r_{o13} \,\|\, R_{o4} \,\|\, R_{i3}) \tag{2.125}$$

where R_{i3} is the input resistance of the output stage and R_{o4} is the output resistance of Q_3 and Q_4 cascode configuration. The transistor Q_{17} at the input of the output stage is connected as an emitter-follower which means that R_{i3} is typically in the range of megohms. The output resistance R_{o4} of the cascode configuration is also typically in the megohm range.

The voltage gain of the second stage is defined by

$$|A_{v2}| \cong g_{m13}\, r_{13} \tag{2.126}$$

Overall Gain The overall voltage gain of the *IC* is the product of the values of individual gain factors as given by

$$A_v = A_d A_{v2} A_{v3} \tag{2.127}$$

where A_{v3} is the voltage gain of the output stage. Assuming $A_{v3} \cong 1$ for the emitter-follower output stage, then the typical value of the gain of CA3140 op-amp is around 100,000.

Frequency response The IC CA3140 op-amp is internally compensated using Miller compensation technique by introducing a dominant pole as in the case of IC 741 op-amp. The feedback capacitor C_1 of 12pF is connected between the collector and base of Q_{13} as shown in Fig 2.45. Using Miller's theorem, the effective input capacitance of the second stage is given by

$$C_i = C_1 \left(|1 + A_{v2}|\right) \tag{2.128}$$

The low-frequency dominant pole is

$$f_{PD} = \frac{1}{2\pi R_{eq} C_i} \tag{2.129}$$

where R_{eq} is the equivalent resistance seen between the input node of second stage and ground. This resistance is dominated by the input resistance to Q_{13}, so that

$$R_{eq} \cong R_{i2} = r_{\pi 13} \tag{2.130}$$

Specifications of IC CA3140

- MOSFET input stage
- Very high input impedance-1.5TΩ (Typ)
- Very low input current-10pA (Typ) at ±15V
- Wide common mode input voltage range
- Output swing complements input common mode range
- Directly replaces industry type 741 in most applications

Applications

- Ground-referenced single supply amplifiers in automobile and portable instrumentation
- Sample-and-Hold Amplifiers
- Long duration timers/multivibrators
- Photocurrent Instrumentation
- Peak detectors
- Active filters
- Comparators
- Interface in 5V TTL Systems and other Low Voltage systems
- All standard operational amplifier applications
- Function generators
- Tone controls
- Power supplies

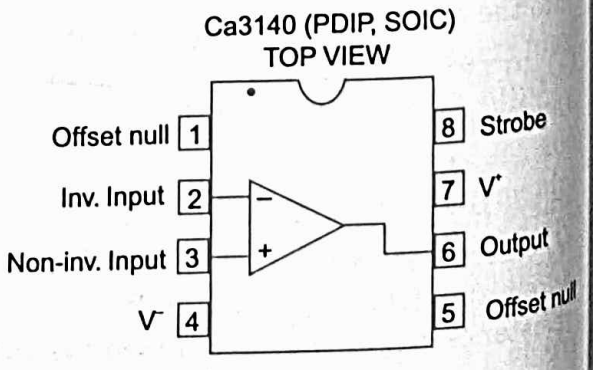


Fig. 2.46 Pin diagram of CA3140

- Portable instruments
- Intrusion alarm systems

The pin-out diagram of IC CA3140 is shown in Fig 2.46.

The important features of IC CA3140 with wide dynamic range of input and output characteristics with the most desirable high input impedance characteristics are achieved in CA3140 by the use of its unique design based on the PMOS Bipolar process. Input common mode voltage range and output swing capabilities are complementary, allowing operation with the single supply down to 4V. The wide dynamic range of these parameters also means that this device is suitable for many single supply applications, where one input is driven below the potential of terminal 4 and the phase sense of the input signal must be maintained, which is one of the most important consideration in cimparator applications.

Output circuit considerations Excellent interfacing with TTL circuitry is easily achievable with a single 6.2V Zener diode connected to terminal 8. This connection assures that the maximum output signal swing will not go more positive than the Zener voltage minus two base-to-emitter voltage drops within CA3140. These voltages are independent of the supply voltage.

Offset voltage nulling The input offset voltage can be nulled by connecting a 10 kΩ potentiometer between terminals 1 and 5 and connecting its wiper arm to terminal 4 as shown in Fig 2.47.

The specifications of BiCMOS op-amp CA3140 is shown in Table.

Table: Specifications of BiCMOS op-amp

Parameter	*Minimum*	*Typical*	*Maximum*	*Units*
Input bias current	–	10	–	pA
Open-loop gain	20000	100000	50	V/A
Unity-gain frequency	4.5	–	–	MHz

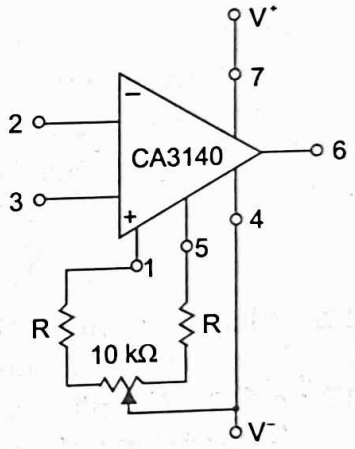


Fig. 2.47 Offset voltage nulling

SUMMARY

1. An op-amp is available in three types of IC packages: metal can, dual-in-line and flat pack.
2. There are five basic terminals: two input terminals, one output terminal and two supply terminals.
3. In open loop mode, the output of the op-amp is at positive or negative saturation level. It does not operate linearly in this mode.
4. Negative feedback stabilizes the gain. Two feedback connections used are: inverting amplifier and non-inverting amplifier.
5. A special case of non-inverting amplifier is the voltage follower.
6. A differential amplifier amplifies the difference between two input signals.
7. An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential amplifiers, followed by a level translator and an output stage.
8. For proper operation of the differential amplifier, matched components must be used. The diff amp. can be biased by using emitter bias (a combination of R_E and V_{EE}), a constant current bias or a current mirror.

9. A current mirror can be used as an active load because it has high ac resistance.
10. MOSFET op-amps offer very high input resistance ($10^{12}\ \Omega$), low input current (~1 pA) and high slewing rate (~10 V/μs).
11. CMOS op-amps are usually designed for particular on-chip applications where a capacitive load is required to be driven.
12. MC 14573 consists of four op-amps configured using CMOS devices as a monolithic IC.
13. Bi FET and BiMOS op-amps use FET as input stage to obtain very high input impedance.
14. Bi FET (Bi MOS) op-amps usually consist of three gain stages, i.e. differential amplifier input stage, two gain stages with the level shifters and an emitter follower output stage.
15. Typical value of gain for CA3140 IC is around 1,00,000.
16. Typical applications of CA 3140 are:
    (i) Sample and hold amplifier
    (ii) Long duration timers/multibrators
    (iii) Photo current instrumentation
    (iv) Peak detectors and comparators
    (v) Active-filters
    (vi) Function generators
    (vii) Intrusion alarm systems

REVIEW QUESTIONS

2.1. What is an op-amp?
2.2. What are the different linear IC packages?
2.3. A 741 op-amp is available in a 14-pins dual-in-line package. What is the terminal number for (i) inverting input (ii) non-inverting input (iii) output?
2.4. Explain with figures how two supply voltages V^+ and V^- are obtained from a single supply.
2.5. List six characteristics of an ideal op-amp.
2.6. Explain the meaning of open loop and closed loop operation of an op-amp.
2.7. Name the type of the feedback used if an external component is connected between the output terminal and the inverting input.
2.8. What is the input impedance of a non-inverting op-amp amplifier?
2.9. If the open loop gain of an op-amp is very large, does the closed loop gain depend upon the external components or the op-amp?
2.10. What is a practical op-amp? Draw its equivalent circuit.
2.11. Define common mode rejection ratio.
2.12. Explain why CMRR $\rightarrow \infty$ for an emitter coupled differential amplifier when $R_E \rightarrow \infty$.
2.13. Why is R_E replaced by a constant current bias circuit in a diff.-amp.?
2.14. List and explain the function of all the basic building blocks of an op-amp.
2.15. Explain methods for increasing the input resistance of an op-amp.
2.16. Explain the difference between constant current bias and current mirror.
2.17. Explain why active load is used?
2.18. What is a V_{BE} multiplier?

2.19. What is cross-over distortion and how it is eliminated?
2.20. Why cascade configuration is used in an op-amp?
2.21. Why are FET op-amps better than BJT op-amps?
2.22. What is meant by a BiMOS or BiFET amplifier?
2.23. What are the advantages of CMOS op-amps over BJT op-amps.
2.24. List the features of IC MC 14573.
2.25. What are the important stages of CMOS IC.
2.26. Perform the dc and ac analysis of IC MC14573.
2.27. Explain the three stage architecture of a BiMOS op-amp with neat diagram.
2.28. Explain the active load used for the input differential amplifier stages of IC CA 3140.
2.29. List some applications of IC CA 3140.

PROBLEMS

2.1. In an op-amp of Fig. 2.4 (a), $v_2 = 0$. What must be the voltage at v_1 to give an output of 5 V if $A_{OL} = 50000$?
2.2. Design an inverting amplifier with a gain of –5 and an input resistance of 10 kΩ.
2.3. Design a non-inverting amplifier with a gain of 10.
2.4. For the circuit shown in Fig. P. 2.4, calculate the range of gain and input impedance.
2.5. Calculate the exact closed loop gain of the inverting amplifier of Fig. 2.5 (b) if $A_{OL} = 200{,}000$, $R_i = 2$ MΩ and $R_o = 75\Omega$.
2.6. For the circuit shown in Fig. P. 2.6, calculate the expression of v_o/v_i.

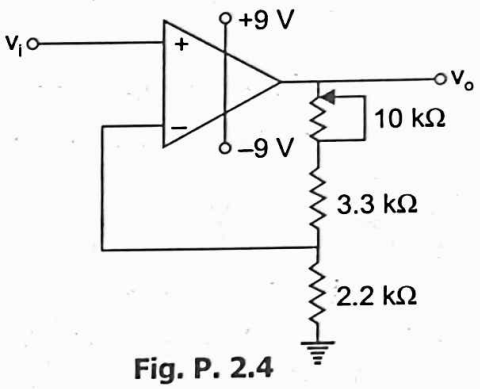


Fig. P. 2.4

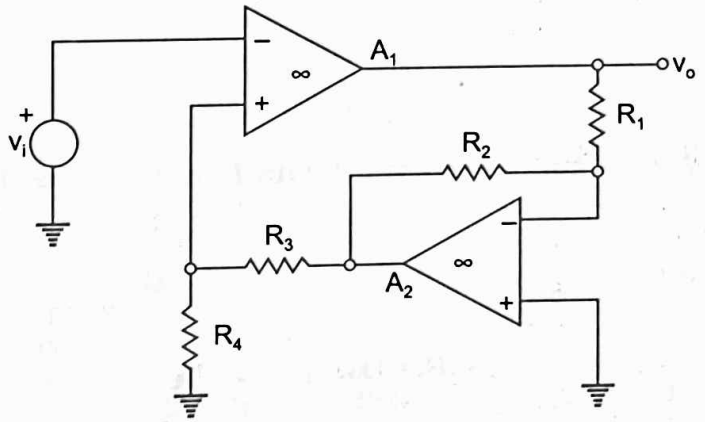


Fig. P. 2.6

2.7. In the circuit of Fig. P. 2.7 if $R_i = \infty$ show that the output admittance Y_{of} is given by

$$Y_{of} = \frac{1}{R_o}\left(1 - A_{OL}\frac{R}{R+R'}\right) + \frac{1}{R+R'}$$

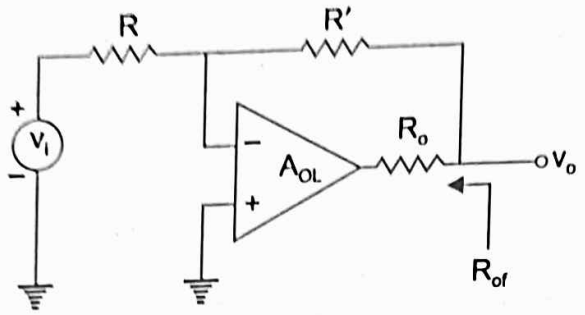


Fig. P. 2.7

2.8. Show that the input impedance for the non-inverting amplifier of Fig. P. 2.8 is

$$R_{if} = R_i \left(1 + \frac{Z_1}{Z_1 + Z_f} . A_V\right)$$

where R_i the input resistance of op-amp is large and $R_o = 0$ and A_v is the gain with feedback.

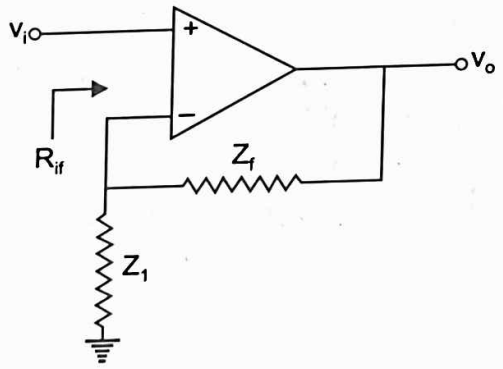


Fig. P. 2.8

2.9. Refer to Fig. P. 2.9

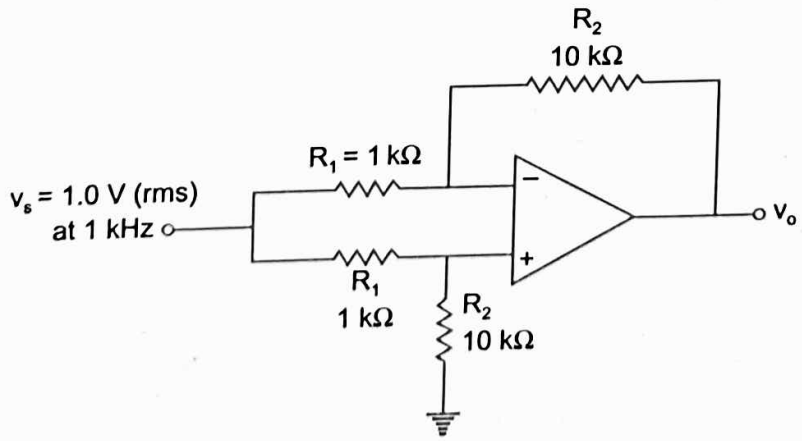


Fig. P. 2.9

(a) Find v_o if CMRR = 100 dB at 1kHz.
(b) Find v_o resulting from 1% mismatches between the two R_1 resistors.
(c) Find v_o resulting from 1% mismatch between two R_2 resistors.

2.10. Derive the expression for the output voltage v_o for the circuit shown in Fig. P. 2.10.

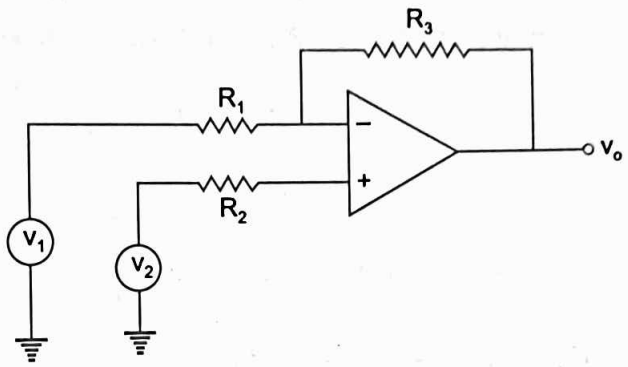


Fig. P. 2.10

2.11. Calculate the output voltage of the circuit in Fig. P. 2.11 if the input signal is a 5.5 mA current.

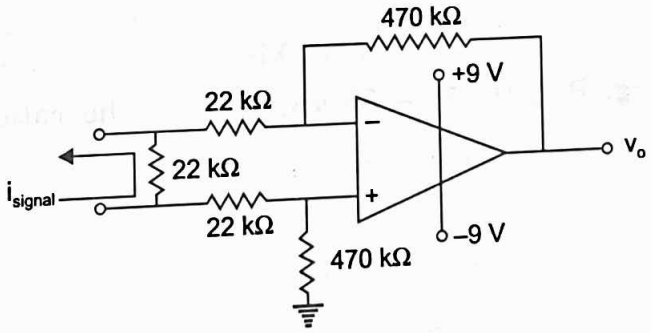


Fig. P. 2.11

2.12. What is the voltage at point A and B for the circuit shown in Fig. P. 2.12 if $v_1 = 5$ V and $v_2 = 5.1$ V?

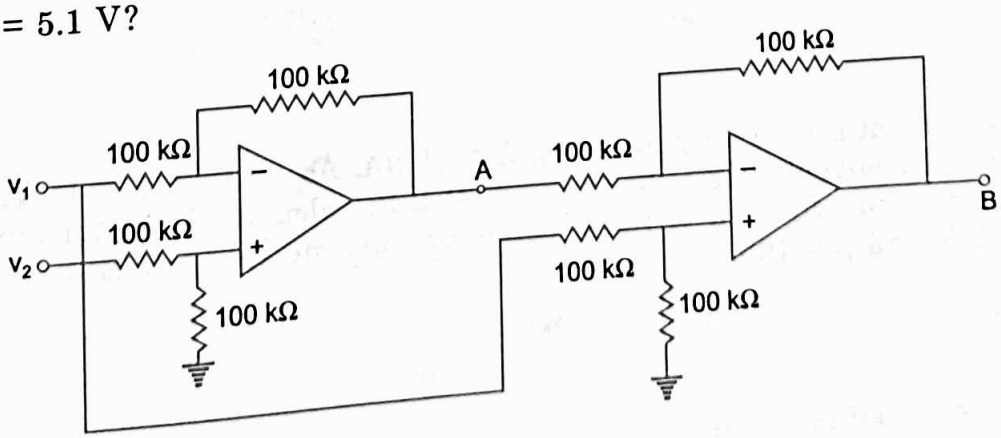


Fig. P. 2.12

2.13. For op-amp, CMRR = 10^5 and differential gain $A_{DM} = 10^6$. Calculate the common mode gain A_{CM} of the op-amp.

2.14. The CMRR of an op-amp is 10^4. Two sets of signals are applied to it. First set is V_1 = +20 μV and V_2 = –20 μV and second set is V_1 = 540 μV and V_2 = 500 μV. Calculate the per cent difference in output voltage for the two sets of signals.

2.15. For the current mirror shown in Fig. P. 2.15, determine R so that I_o = 100 μA.

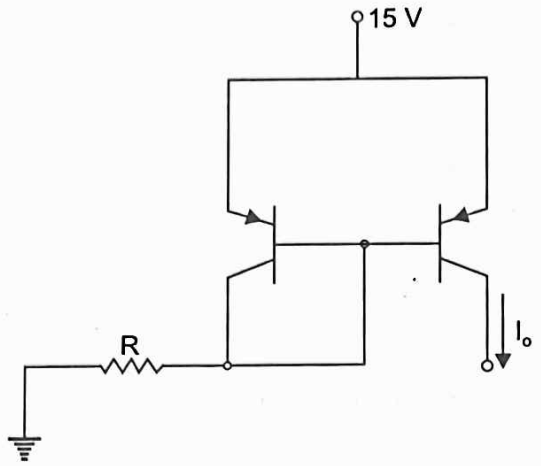


Fig. P. 2.15

2.16. In the circuit of Fig. P. 2.16, I_R = 50 μA, what is the ratio R_1/R_2 needed for I_o = 100 μA?

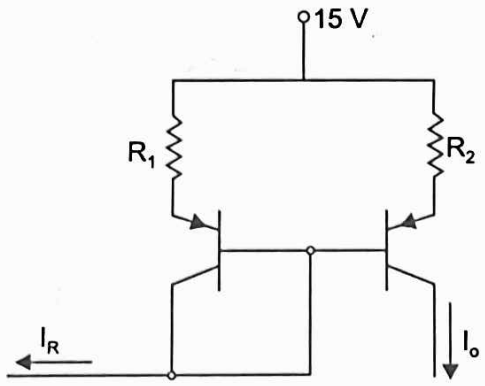


Fig. P. 2.16

2.17. Design a current source for generating I_o = 25 μA. Assume : V_{CC} = 15 V, β = 100.

2.18. For a modified current mirror shown in Fig. P. 2.18, calculate (i) the current through the collector resistor R_C and (ii) the collector current in each transistor. Assume V_{BE} = 0.7 V and β = 100.

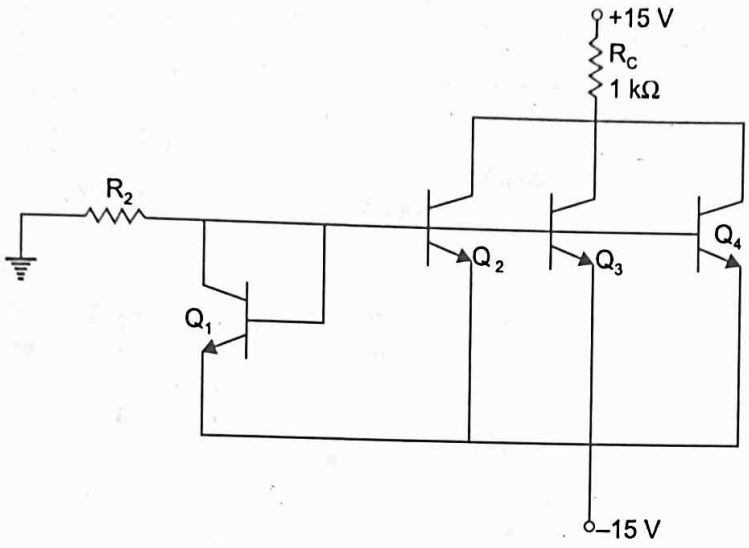


Fig. P. 2.18

2.19. For the circuit of Fig. P. 2.19, show that

$$V_o = (V_Z + V_{BE})\ (1 + R_1/R_2).$$

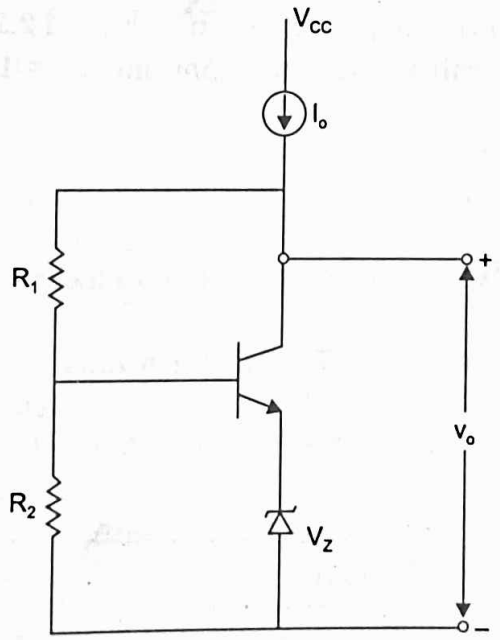


Fig. P. 2.19

2.20. For the simple op-amp shown in Fig. P. 2.20, all *npn* transistors have $\beta = 200$ and all *pnp* transistors have $\beta = 50$. Verify that $v_o = 0$ for $v_1 = v_2 = 0$. The current sources shown are realized by *pnp* current sources.

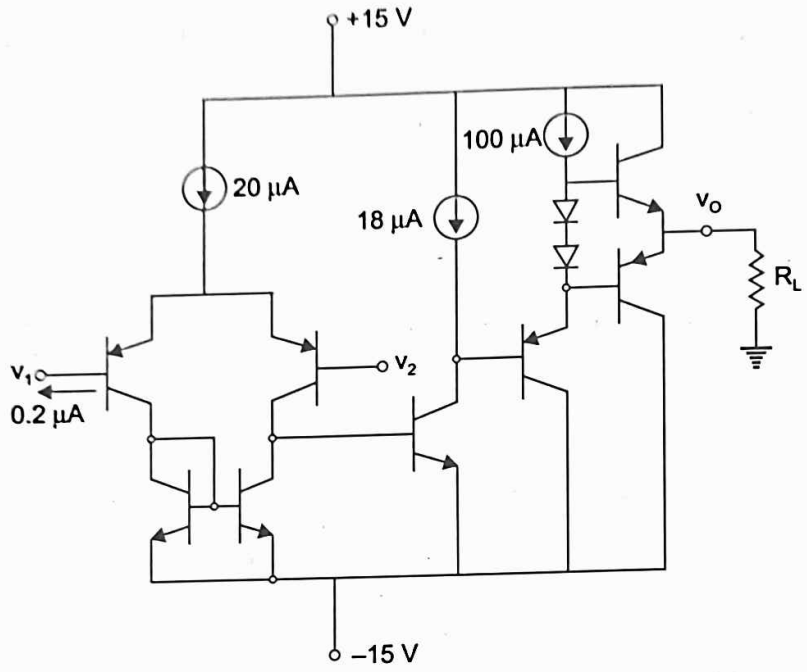


Fig. P. 2.20

2.21. For the cascaded differential amplifier shown in Fig. P. 2.21 (i) perform the dc analysis and (ii) calculate the overall voltage gain. Assume $h_{fe} = 100$ $V_{BE} = V_D = 0.7$ V.

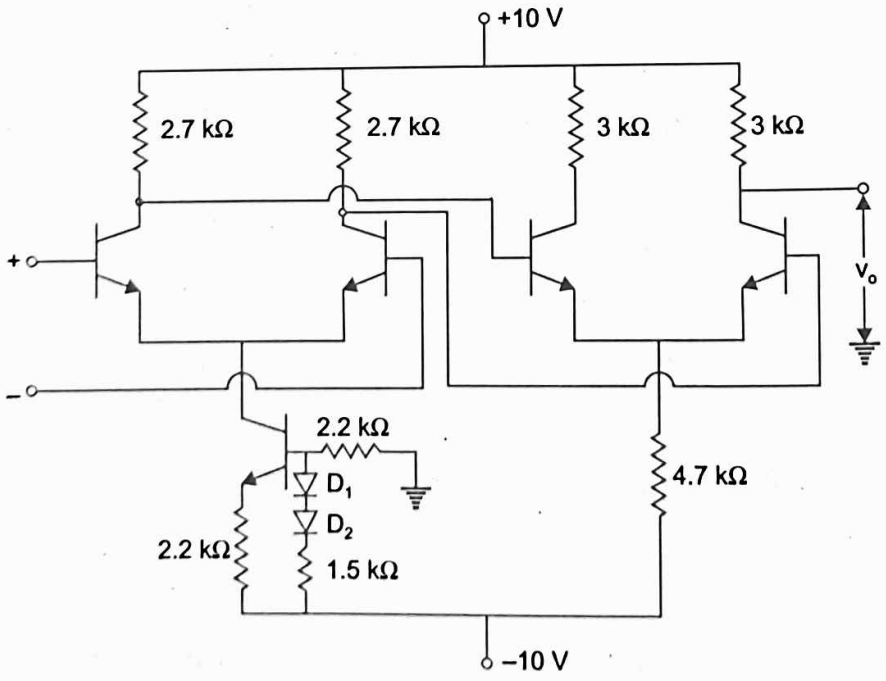


Fig. P. 2.21

EXPERIMENT

To construct and verify experimentally the theoretical closed loop voltage gain using 741 op-amp for the following:

(i) Inverting amplifier
(ii) Non-inverting amplifier
(iii) Voltage follower

PROCEDURE

1. Connect the op-amp as an inverting amplifier as shown in Fig. E. 2.1 (a).

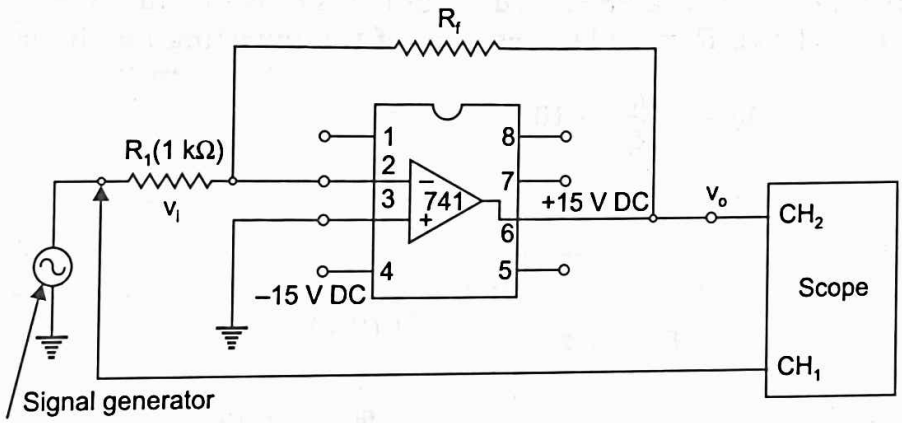


Fig. E. 2.1 (a) Inverting amplifier

2. Connect a dual channel scope to simultaneously view v_o and v_i. Adjust the signal generator to give 200 mV peak to peak sine wave at 100 Hz. Then measure and record the peak value of v_o for R_f: 1 kΩ, 10 kΩ, 33 kΩ and 100 kΩ. Note the phase of v_o with respect to v_i.
3. Calculate the theoretical closed loop gain = R_f/R_i for each value of R_f and compare it with the experimental value of v_o/v_i.
4. Now connect the op-amp as a non-inverting amplifier as shown in Fig. E. 2.1 (b).
5. Repeat step 2.
6. Calculate the theoretical gain = $1 + R_f/R_1$ for each value of R_f and compare it with the experimental value of v_o/v_i.
7. Next make a voltage follower circuit as shown in Fig. E. 2.1. (c).

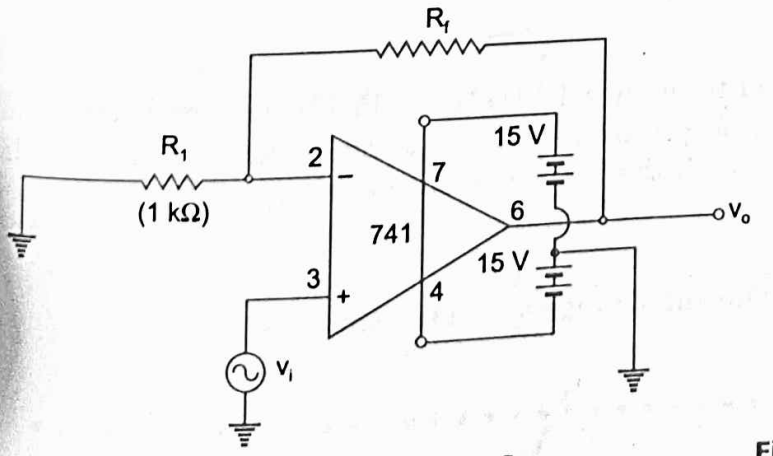


Fig. E. 2.1 (b) Non-inverting amplifier

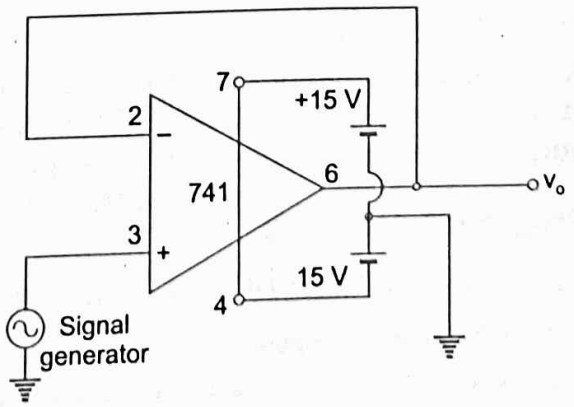


Fig. E. 2.1 (c) Voltage follower

(8) Measure and record the output voltage v_o for different input settings: 2 V peak at 100 Hz, 1 V peak at 500 Hz and 5 V peak at 1 kHz. Note the phase of v_o with respect to v_i in each case.

(9) Verify that the voltage gain of the voltage follower is always equal to 1.

COMPUTER ANALYSIS

Program 2.1

Inverting Op-amp Amplifier

Figure C. 2.1 (a) shows an inverting op-amp amplifier with various terminals numbered for writing the PSPICE program. The PSPICE description is provided in program 2.1 listing. For circuit values of R_1 = 1 kΩ, R_f = 10 kΩ, the gain of the inverting amplifier is

$$A_V = -\frac{R_f}{R_1} = -10$$

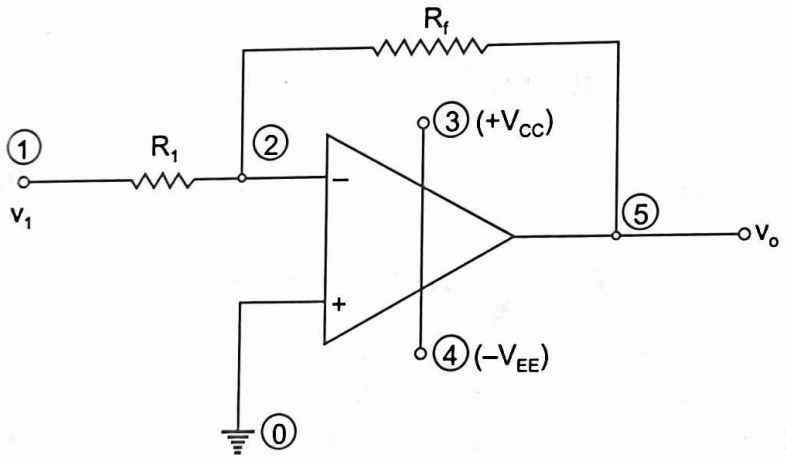


Fig. C. 2.1 (a) Circuit for program 2.1

D.C. Analysis

For input V_1 = 1 V, the output voltage V_o should V_o = –10 (1 V) = –10 V.
From the result file, it can be seen that the output V_o at node 5 is –9.998 V which gives an error or 0.02% only.

Transient Analysis

A sine wave signal of amplitude 0.1 V and frequency 1 kHz is applied at the input terminal. It can be seen from Fig. C. 2.1 (b) that the output is a sine wave of amplitude 1 V, 1 kHz. The output waveform is 180° out of the phase with the input waveform as expected.

Program 2.1: Listing

Inverting Amplifier: DC and Transient (Output Voltage vs Time) Analysis

```
**** Circuit Description
**********************************************************
```

```
* * *
    R1 1 2 IK
    RF 2 5 10K
*   Op Amp Analysis
    X1 0 2 3 4 5 µA 741
    . LIB EVAL. LIB
*   Power Supplies
    VCC 3 0 DC 12V
    VEE 0 4 DC 12V
*   Input Signal Source
    V1 1 0 DC 1V SIN(0 0.1V 1KHZ)
*   Output
    .DC V1 1 1 1
    .TRAN . 5µs 5ms 0ms .01 ms
    .PROBE
    .PRINT DC V(5) V(1)
    END
```

```
  * * * * DC Transfer Curves                    Temperature = 27.000 DEG C
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

* * *
    V1              V(5)            V(1)
    1.000E+00       -9.998E+00      1.000E+00
```

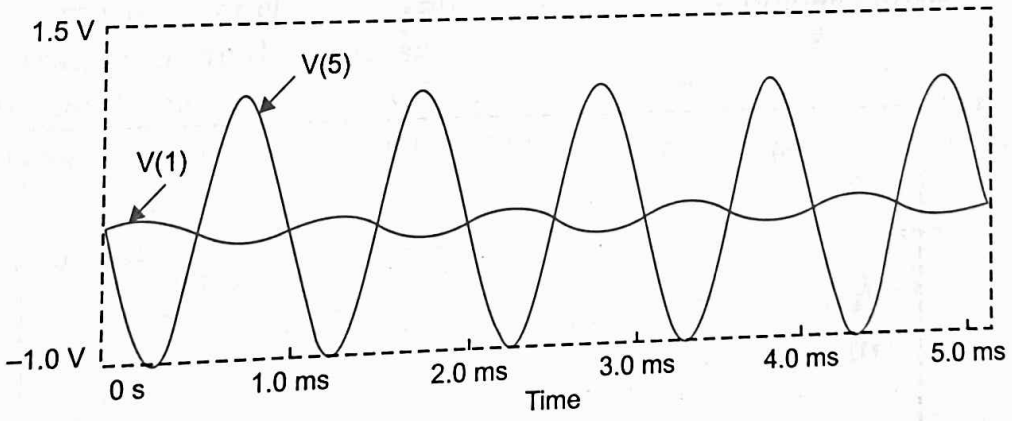


Fig. C. 2.1 (b) Inverting amplifier: Transient analysis (output voltage vs time)

Program 2.2

Non-inverting Op-amp Amplifier

The circuit of a non-inverting op-amp amplifier for writing the PSPICE program is shown in Fig. C. 2.2 (a).

For the circuit values, $R_1 = 1\ \text{k}\Omega$ and $R_f = 9\ \text{k}\Omega$, the voltage gain is

$$A_V = 1 + \frac{R_f}{R_1} = 1 + \frac{9\text{k}\Omega}{1\text{k}\Omega} = +10 = 10$$

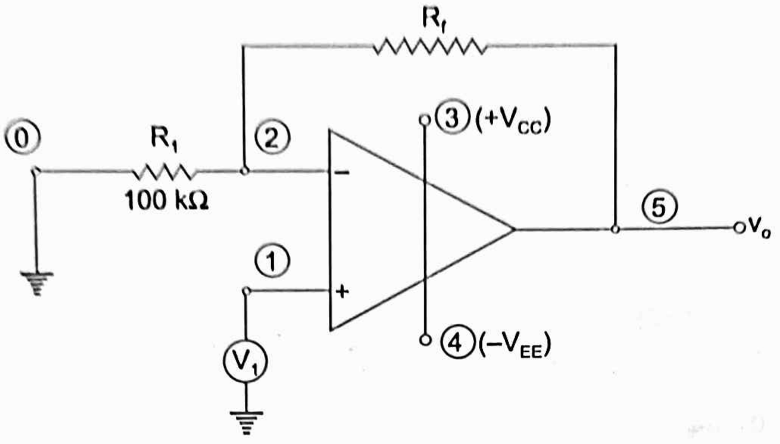


Fig. C. 2.2 (a) Circuit for program 2.2

D.C. Analysis

For input voltage $V_1 = 1$ V, the output voltage at node 5, V(5) = 10 V

Transient Analysis

For input voltage source of amplitude 0.1 V and frequency 1 kHz, the output voltage has an amplitude 1 V at 1 kHz as shown in Fig. C. 2.2 (b). It may be noted that there is no phase shift for a non-inverting amplifier.

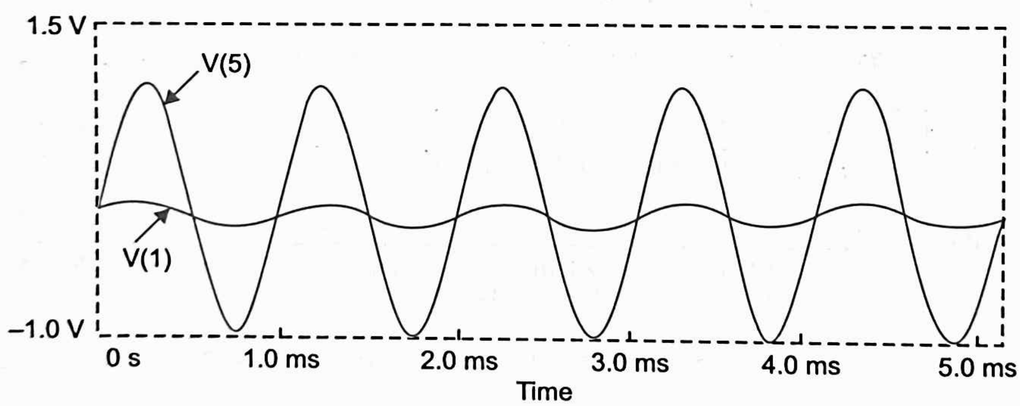


Fig. C. 2.2 (b) Non-inverting amplifier: Transient analysis (Output voltage vs time)

Program 2.2 Listing

Non-inverting Amplifier: DC and Transient (Output Voltage vs Time) Analysis

```
  * * * * Circuit Description
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
* * *
   R1  0  2  IK
   RF  2  5  9K
*  Op Amp Analysis
   X1  1  2  3  4  5  μA741
```

```
. LIB  EVAL.LIB
*  Power Supplies
   VCC  3  0  DC  12V
   VEE  0  4  DC  12V
*  Input Signal  Source
   V1  1  0  DC  1V  SIN (0  0.1V  1 KHZ)
*  Output
   .DC  V1  1  1  1
   .TRAN . 5µs 5ms 0ms 0.01 ms
   .PRINT  DC  V(5)  V(1)
   .PROBE
 * * * *     DC Transfer Curves          Temperature = 27.000 DEG C
*****************************************************

***
       V1                   V(5)                 V(1)
   1.000E+00             1.000E+01            1.000E+00
```


Program 2.3 Voltage Follower

The circuit diagram of a voltage follower and its PSPICE description are shown in Fig. C. 2.3 (a) and program 2.3 listing respectively.

The voltage gain for both d.c. and a.c. input is found to be unity and without change in phase as expected. The transient analysis is shown in Fig. C 2.3 (b). It may be noted that waveforms at node 1 and 5 overlap each other indistinguishably.

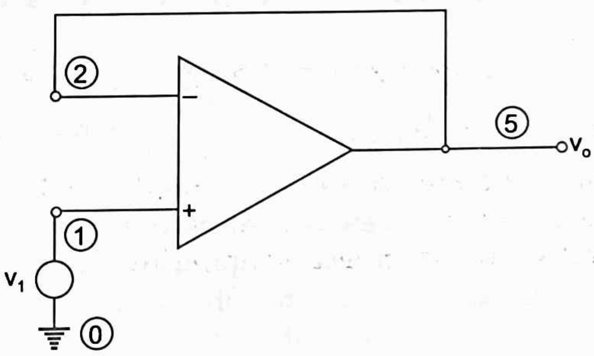


Fig. C. 2.3 (a) Circuit for program 2.3

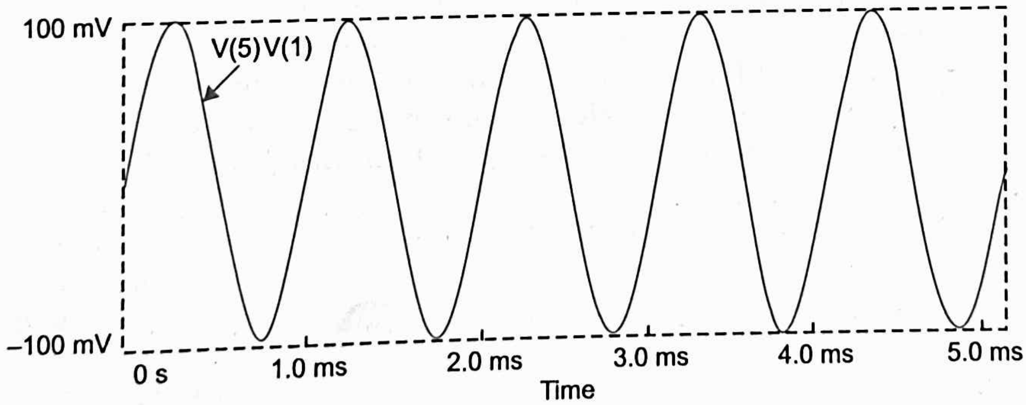


Fig. C. 2.3 (b) Transient response of voltage follower

Program 2.3 Listing

* Voltage Follower

* * * * Circuit Description

```
********************************************************************************
***
    RF  2  5  IM
*   Op Amp Analysis
    X1  1  2  3  4  5  µA741
    . LIB  EVAL.LIB
*   Power Supplies
    VCC  3  0  DC  12V
    VEE  0  4  DC  12V
*   Input Signal  Source
    V1  1  0  DC  2V  SIN(0 0.1V 1KHZ)
*   Output
    * DC  V1  2  2  2
    * TRAN 0.5µs 5ms 0ms 0.01 ms
    * PRINT  DC  V(5)  V(1)
    * PROBE
  * * * *   DC Transfer Curves            Temperature = 27.000 DEG C
********************************************************************************
***
        V1                    V(5)                   V(1)
     2.000E+00             2.000E+01              2.000E + 00
```

3

OPERATIONAL AMPLIFIER CHARACTERISTICS

3.1 INTRODUCTION

Earlier we have used an ideal op-amp, and assumed that the op-amp responds equally well to both ac and dc input voltages. However, a practical op-amp does not behave this way. A practical op-amp has some dc voltage at the output even with both the inputs grounded. The factors responsible for this and the suitable compensating techniques are discussed. Also, under ac conditions the characteristics of an op-amp are frequency dependent. The limitations of an op-amp under ac conditions and methods of compensation are discussed.

3.2 DC CHARACTERISTICS

An ideal op-amp draws no current from the source and its response is also independent of temperature. However, a real op-amp does not work this way. Current is taken from the source into the op-amp inputs. Also the two inputs respond differently to current and voltage due to mismatch in transistors. A real op-amp also shifts its operation with temperature. These non-ideal dc characteristics that add error components to the dc output voltage are:

Input bias current
Input offset current
Input offset voltage
Thermal drift.

3.2.1 Input Bias Current

The op-amp's input is a differential amplifier, which may be made of BJT or FET. In either case, the input transistors must be biased into their linear region by supplying currents into the bases by the external circuit. In an ideal op-amp, we assumed that no current is drawn from the input terminals. However, practically, input terminals do conduct a small value of dc current to bias the input transistors. The base currents entering into the inverting and non-inverting terminals are shown as I_B^- and I_B^+ respectively in Fig. 3.1 (a). Even though both the transistors are identical, I_B^- and I_B^+ are not exactly equal due to internal imbalances between the two inputs. Manufacturers specify input bias current I_B as the average value of the base currents entering into the terminals of an op-amp.

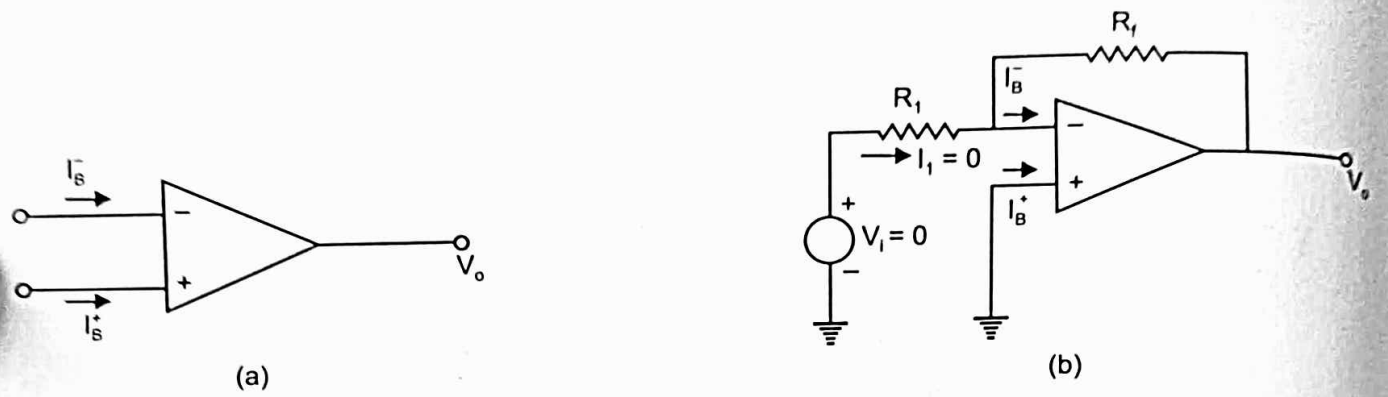


Fig. 3.1 (a) Input bias currents (b) Inverting amplifier with bias currents

So,
$$I_B = \frac{I_B^+ + I_B^-}{2} \tag{3.1}$$

For 741, a bipolar op-amp, the bias current is 500 nA or less. The FET input op-amp will have bias currents as low as 50 pA at room temperature.

Consider the basic inverting amplifier of Fig. 3.1 (b). If input voltage V_i is set to zero volt, the output voltage V_o should also be zero volt. Instead, we find that the output voltage is offset by,

$$V_o = (I_B^-)\ R_f \tag{3.2}$$

For a 741 op-amp, with a 1 MΩ feedback resistor,

$$V_o = 500 \text{ nA} \times 1 \text{ M}\Omega = 500 \text{ mV}$$

The output is driven to 500 mV with zero input because of the bias currents. In applications where signal levels are measured in millivolts, this is totally unacceptable. This effect can be compensated for as shown in Fig. 3.1 (c) where a compensation resistor R_{comp} has been added between the non-inverting input terminal and ground. Current I_B^+ flowing through the compensating resistor R_{comp} develops a voltage V_1 across it. Then, by KVL, we get,

$$-V_1 + 0 + V_2 - V_o = 0$$

or
$$V_o = V_2 - V_1 \tag{3.3}$$

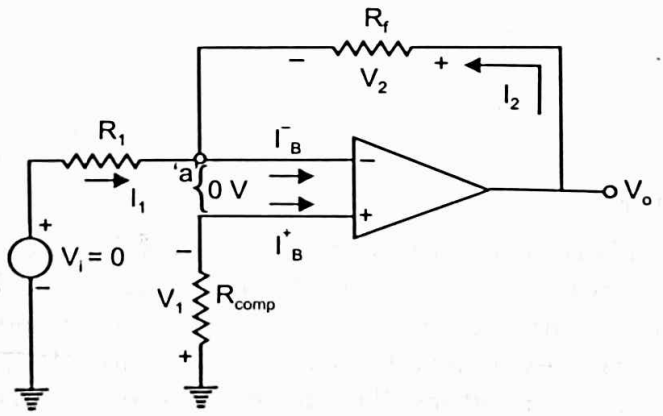


Fig. 3.1 (c) Bias current compensation in an inverting amplifier

By selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and the output V_o will be zero. The value of R_{comp} is derived as

$$V_1 = I_B^+ R_{comp}$$

or
$$I_B^+ = \frac{V_1}{R_{comp}} \tag{3.4}$$

The node 'a' is at voltage $(-V_1)$, because the voltage at the non-inverting input terminal is $(-V_1)$. So, with $V_i = 0$, we get,

$$I_1 = \frac{V_1}{R_1} \tag{3.5}$$

Also,
$$I_2 = \frac{V_2}{R_f} \tag{3.6}$$

For compensation, V_o should be zero for $V_i = 0$, that is, from Eq. (3.3) $V_2 = V_1$

So that,
$$I_2 = \frac{V_1}{R_f} \tag{3.7}$$

KCL at node 'a' gives,

$$I_B^- = I_2 + I_1 = \frac{V_1}{R_f} + \frac{V_1}{R_1} = V_1 \frac{(R_1 + R_f)}{R_1 R_f} \tag{3.8}$$

Assuming $I_B^- = I_B^+$ and using Eqs. (3.4) and (3.8) we get,

$$V_1 \frac{(R_1 + R_f)}{R_1 R_f} = \frac{V_1}{R_{comp}}$$

or,
$$R_{comp} = \frac{R_1 R_f}{R_1 + R_f} = R_1 \,||\, R_f \tag{3.9}$$

that is, to compensate for bias currents, the compensating resistor R_{comp} should be equal to the parallel combination of resistors tied to the inverting input terminal.

The effect of input bias current in a non-inverting amplifier can also be compensated by placing a compensating resistor, R_{comp} in series with the input signal V_i as shown in Fig. 3.1 (d).

The value of R_{comp} is again equal to

$$R_{comp} = R_1 \,||\, R_f$$

as the circuits for inverting amplifier and non-inverting amplifier shown in Figs. 3.1 (c) and (d) become same with input signal V_i made equal to zero.

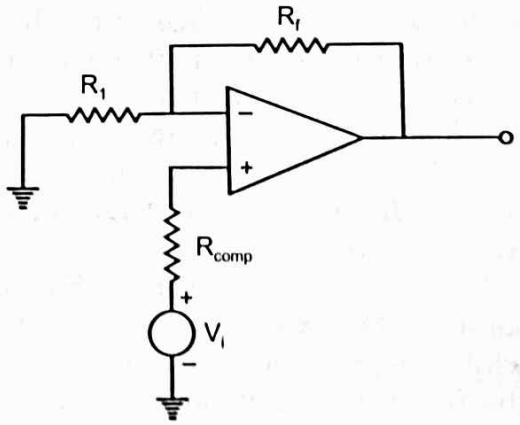


Fig. 3.1 (d) Bias current compensation in a non-inverting amplifier

3.2.2 Input Offset Current

Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal. Since the input transistors cannot be made identical, there will always be some small difference between I_B^+ and I_B^-. This difference is called the offset current I_{os} and can be written as

$$|I_{os}| = I_B^+ - I_B^- \tag{3.10}$$

The absolute value sign indicates that there is no way to predict which of the bias currents will be larger.

Offset current I_{os} for BJT op-amp is 200 nA and that for FET op-amp is 10 pA. Even with bias current compensation, offset current will produce an output voltage when the input voltage V_i is zero. Referring to Fig. 3.1 (c),

$$V_1 = I_B^+ R_{comp} \tag{3.11}$$

and

$$I_1 = \frac{V_1}{R_1} \tag{3.12}$$

KCL at node 'a' gives,

$$I_2 = (I_B^- - I_1) = I_B^- - \left(I_B^+ \frac{R_{comp}}{R_1}\right) \tag{3.13}$$

Again

$$V_o = I_2 R_f - V_1 = I_2 R_f - I_B^+ R_{comp}$$

$$= \left(I_B^- - I_B^+ \frac{R_{comp}}{R_1}\right) R_f - I_B^+ R_{comp} \tag{3.14}$$

Substituting Eq. (3.9) and after algebraic manipulation,

$$V_o = R_f [I_B^- - I_B^+] \tag{3.15}$$

So,

$$V_o = R_f I_{os} \tag{3.16}$$

So even with bias current compensation and with the feedback resistor of 1 MΩ, a 741 BJT op-amp has an output offset voltage

$$V_o = 1 \text{ M}\Omega \times 200 \text{ nA} = 200 \text{ mV}$$

with a zero input voltage. It can be seen from Eq. (3.16) that the effect of offset current can be minimized by keeping feedback resistance small. Unfortunately, to obtain high input impedance, R_1 must be kept large. With R_1 large, the feedback resistor R_f must also be high so as to obtain reasonable gain.

The T-feedback network in Fig. 3.1 (e) is a good solution. This will allow large feedback resistance, while keeping the resistance to ground (seen by the inverting input) low as shown in the dotted network. The T-network provides a feedback signal as if the network were a single feedback resistor. By T to π conversion,

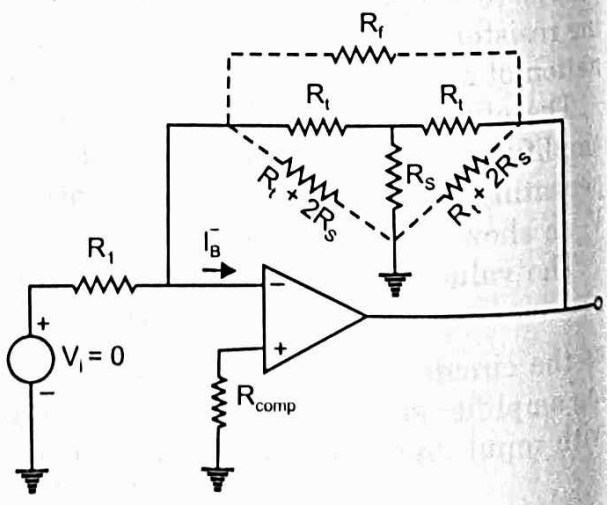


Fig. 3.1 (e) Inverting amplifier with T-feedback network

$$R_f = \frac{R_t^2 + 2R_1R_s}{R_s} \tag{3.17}$$

To design a T-network, first pick

$$R_t << \frac{R_f}{2} \tag{3.18}$$

Then calculate $$R_s = \frac{R_t^2}{R_f - 2R_t} \tag{3.19}$$

Example 3.1

Design an inverting amplifier of the type shown in Fig. 3.1 (e) using 741 op-amp to get a gain of – 10 and an input impedance of 10 MΩ. That is, calculate R_t, R_s and R_1.

Solution

In Fig. 3.1 (e), to set input impedance R_i = 10 MΩ, pick R_1 = 10 MΩ

Since, $$A_{CL} = -\frac{R_f}{R_1}$$

Therefore, $$R_f = A_{CL}R_1 = (10)\ (10\ \text{M}\,\Omega) = 100\ \text{M}\Omega$$

Choose $$R_t = 47\ \text{k}\Omega$$

$$R_s = \frac{R_t^2}{R_f - 2R_t} = \frac{(47\ \text{k}\Omega)^2}{100\ \text{M}\Omega - 2(47\ \text{k}\Omega)} = 22\ \Omega$$

3.2.3 Input Offset Voltage

Inspite of the use of the above compensating techniques, it is found that the output voltage may still not be zero with zero input voltage. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminals to make output voltage zero. This voltage is called input offset voltage V_{ios}. This is the voltage required to be applied at the input for making output voltage to zero volts as shown in Fig. 3.2. (a).

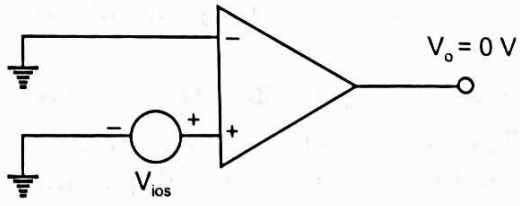


Fig. 3.2 (a) Op-amp showing input offset voltage

Let us now examine the effect of V_{ios} on the output of a non-inverting and inverting op-amp amplifier as shown in Fig. 3.2 (b, c). If V_i is set to zero, the circuits of Fig. 3.2 (b and c) become the same as in Fig. 3.2 (d). The voltage V_2 at the (–) input terminal is given by

$$V_2 = \left(\frac{R_1}{R_1 + R_f}\right)V_o \tag{3.20}$$

or $$V_o = \left(\frac{R_1 + R_f}{R_1}\right)V_2 = \left(1 + \frac{R_f}{R_1}\right)V_2 \tag{3.21}$$

Since, $V_{ios} = |V_i - V_2|$ and $V_i = 0$,

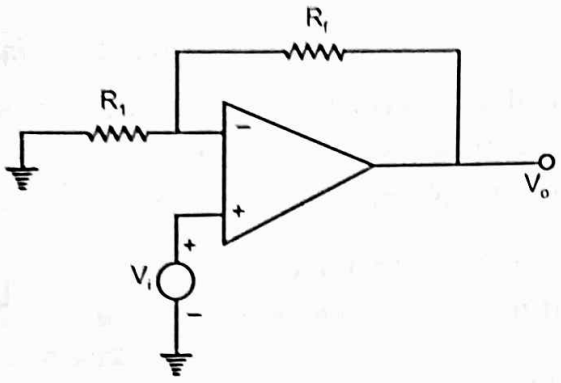


Fig. 3.2 (b) Non-inverting amplifier

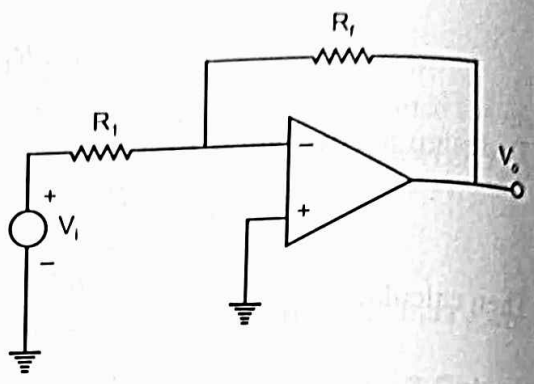


Fig. 3.2 (c) Inverting amplifier

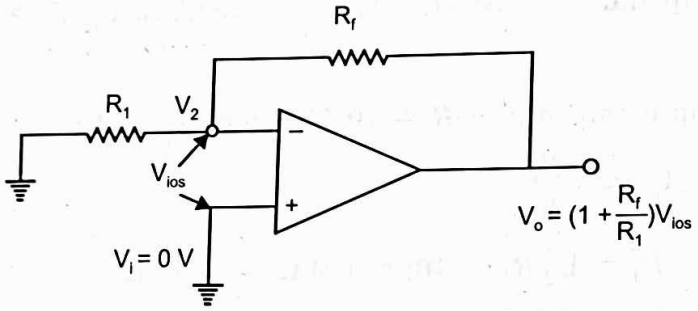


Fig. 3.2 (d) Equivalent circuit for $V_i = 0$

$$V_{ios} = |0 - V_2| = V_2 \tag{3.22}$$

or,

$$\boxed{V_o = \left(1 + \frac{R_f}{R_1}\right) V_{ios}} \tag{3.23}$$

Thus, the output offset voltage of an op-amp in closed-loop configuration (inverting or non-inverting) is given by Eq. (3.23).

3.2.4 Total Output Offset Voltage

The total output offset voltage V_{oT} could be either more or less than the offset voltage produced at the output due to input bias current or input offset voltage alone. This is because input offset voltage V_{ios} and input bias current I_B could be either positive or negative with respect to ground. Therefore, the maximum offset voltage at the output of an inverting and non-inverting amplifier of Fig. 3.2 (b, c) without any compensating technique used, is given by

$$V_{oT} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + R_f I_B \tag{3.24}$$

However, with R_{comp} in the circuit, the total output offset voltage will be given by

$$V_{oT} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + R_f I_{os} \tag{3.25}$$

Many op-amps provide offset compensation pins to nullify the offset voltage. So one must refer to the manufacturer's specifications while using the offset null connections. Figure 3.3 (a) gives the connections for the 741 op-amp. The manufacturers recommend that a 10 kΩ potentiometer be placed across offset null pins 1 and 5 and the wiper be connected to the negative supply pin 4. The position of the wiper is adjusted to nullify the output offset voltage. However, when the given op-amp does not have these offset null pins, external balancing techniques are used. Figures 3.3 (b, c) show the balancing circuits used for inverting and non-inverting operational amplifiers.

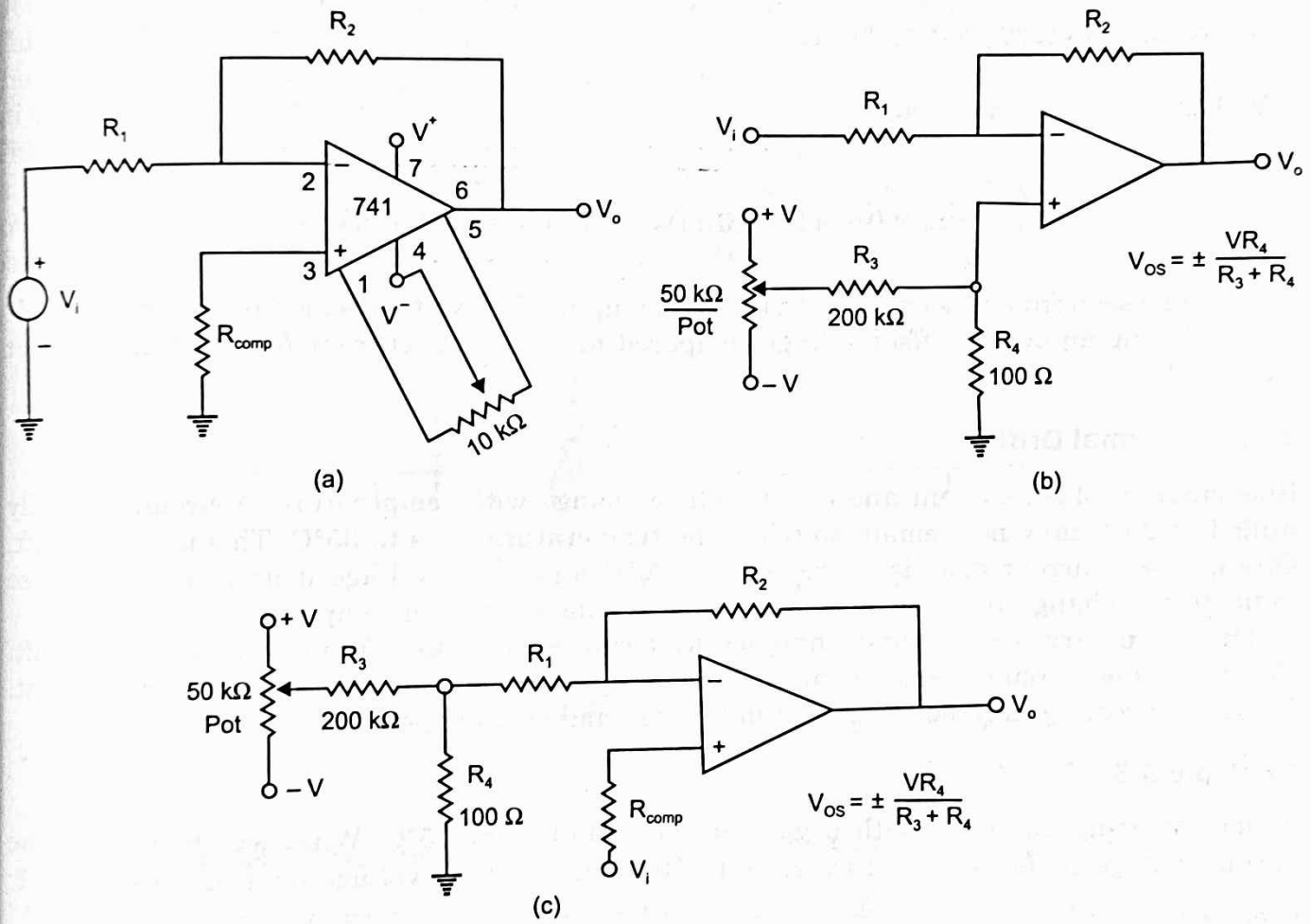


Fig. 3.3 (a) Offset null pin connection for μA741. Balancing circuit for (b) Inverting amplifier (c) Non-inverting amplifier

Example 3.2

(a) For the non-inverting amplifier of Fig. 3.2 (b), $R_1 = 1$ kΩ and $R_f = 10$ kΩ. Calculate the maximum output offset voltage due to V_{ios} and I_B. The op-amp is LM 307 with $V_{ios} = 10$ mV and $I_B = 300$ nA, $I_{os} = 50$ nA.

(b) Calculate the value of R_{comp} needed to reduce the effect of I_B.

(c) Calculate the maximum output offset voltage if R_{comp} as calculated in (b) is connected in the circuit.

Solution

(a) $$V_{oT} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + R_f I_B$$

$$= \left(1 + \frac{10\ \text{k}\Omega}{1\ \text{k}\Omega}\right) (10\ \text{mV}) + (10\ \text{k}\Omega)\ (300\ \text{nA}) = 110\ \text{mV} + 3\ \text{mV} = 113\ \text{mV}$$

(b) The value of R_{comp} needed is,

$$R_{comp} = 1\ \text{k}\Omega \| 10\ \text{k}\Omega = 990\ \Omega$$

(c) With R_{comp} in the circuit,

$$V_{oT} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + R_f I_{os} = 110\ \text{mV} + 0.5\ \text{mV} = 110.5\ \text{mV}$$

It can be seen from this example that it is the input offset voltage which is more responsible for producing an output offset voltage compared to input bias current I_B or the input offset current I_{os}.

3.2.5 Thermal Drift

Bias current, offset current and offset voltage change with temperature. A circuit carefully nulled at 25°C may not remain so when the temperature rises to 35°C. This is called drift. Often, offset current drift is expressed in nA/°C and offset voltage drift in mV/°C. These indicate the change in offset for each degree celsius change in temperature.

There are very few circuit techniques that can be used to minimize the effect of drift. Careful printed circuit board layout must be used to keep op-amps away from source of heat. Forced air cooling may be used to stabilize the ambient temperature.

Example 3.3

A non-inverting amplifier with a gain of 100 is nulled at 25°C. What will happen to the output voltage if the temperature rises to 50°C for an offset voltage drift of 0.15 mV/°C?

Solution

Input offset voltage due to temperature rise = 0.15 mV/°C × (50°C – 25°C) = 3.75 mV. Since this is an input change, the output voltage will change by

$$V_o = V_{os} \times A_{CL}$$

$$= 3.75\ \text{mV} \times 100 = 375\ \text{mV}$$

This could represent a very major shift in the output voltage.

3.3 AC CHARACTERISTICS

We have discussed so far the dc characteristics such as bias current, offset current, offset voltage and thermal drift. These will effect the steady state (dc) response of the op-amp only.

For small signal sinusoidal (ac) applications, one has to know the ac characteristics such as frequency response and slew-rate which will be discussed in this section.

3.3.1 Frequency Response

Ideally, an op-amp should have an infinite bandwidth. This means that, if its open-loop gain is 90 dB with dc signal its gain should remain the same 90 dB through audio and on to high radio frequencies. The practical op-amp gain, however, decreases (rolls-off) at higher frequencies.

What causes the gain of the op-amp to roll-off after a certain frequency is reached? Obviously, there must be a capacitive component in the equivalent circuit of the op-amp. This capacitance is due to the physical characteristics of the device (BJT or FET) used and the internal construction of op-amp. For an op-amp with only one break (corner) frequency, all the capacitor effects can be represented by a single capacitor C as shown in Fig. 3.4 (a). This figure represents the high frequency model of the op-amp with a single corner frequency. It may be observed that the high frequency model of Fig. 3.4 (a) is a modified version of the low frequency model with a capacitor C at the output. There is one pole due to R_oC and obviously one -20 dB/decade roll-off comes into effect.

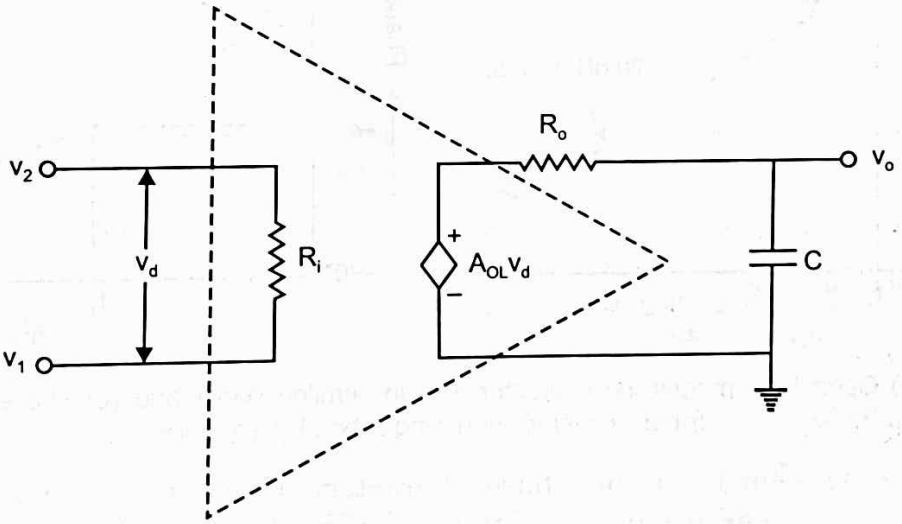


Fig. 3.4 (a) High frequency model of an op-amp with single corner frequency

The open loop voltage gain of an op-amp with only one corner frequency is obtained from Fig. 3.4 (a) as

$$v_o = \frac{-jX_c}{R_o - jX_c} A_{OL} v_d \tag{3.26}$$

or,
$$A = \frac{v_o}{v_d} = \frac{A_{OL}}{1 + j\,2\pi f R_o C}$$

or,
$$A = \frac{A_{OL}}{1 + j(f/f_1)} \tag{3.27}$$

where
$$f_1 = \frac{1}{2\pi R_o C} \tag{3.28}$$

is the corner frequency or the upper 3-dB frequency of the op-amp. The magnitude and the phase angle of the open loop voltage gain are function of frequency and can be written as

$$|A| = \frac{A_{OL}}{\sqrt{1+(f/f_1)^2}} \tag{3.29}$$

$$\phi = -\tan^{-1}(f/f_1) \tag{3.30}$$

The magnitude and phase characteristics from Eqs. (3.29) and (3.30) are shown in Fig. 3.4 (b, c). It can be seen that

(i) For frequency $f << f_1$, the magnitude of the gain is 20 log A_{OL} in dB.

(ii) At frequency $f = f_1$, the gain is 3 dB down from the dc value of A_{OL} in dB. This frequency f_1 is called corner frequency.

(iii) For $f >> f_1$, the gain rolls-off at the rate of –20 dB/decade or –6 dB/octave.

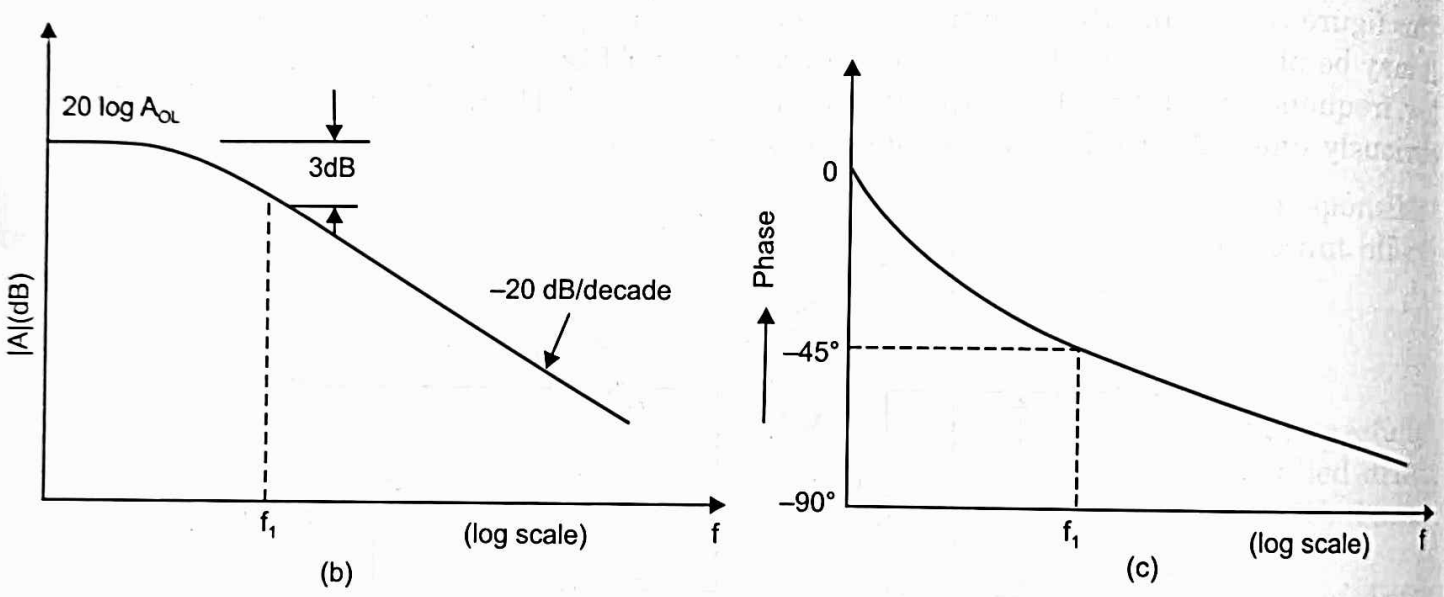


Fig. 3.4 (b) Open loop magnitude characteristics in semilog paper and (c) Phase characteristics for an op-amp with single break frequency

It can further be seen from the phase characteristics that the phase angle is zero at frequency $f = 0$. At corner frequency f_1 the phase angle is $-45°$ (lagging) and at infinite frequency the phase angle is –90°. This shows that a maximum of 90° phase change can occur in an op-amp with a single capacitor. It may be mentioned here, that zero frequency does not occur in log scale. From all practical purposes, zero frequency is taken as one decade below the corner frequency and infinite frequency is one decade above the corner frequency. The voltage transfer function is s-domain can be written as

$$A = \frac{A_{OL}}{1+j(f/f_1)} = \frac{A_{OL}}{1+j(\omega/\omega_1)}$$

$$= \frac{A_{OL}\cdot\omega_1}{j\omega+\omega_1} = \frac{A_{OL}\cdot\omega_1}{s+\omega_1}$$

A practical op-amp, however, has number of stages and each stage produces a capacitive component. Thus due to a number of RC pole pairs, there will be a number of different break frequencies. The transfer function of an op-amp with three break frequencies can be assumed as

$$A = \frac{A_{OL}}{\left(1+j\frac{f}{f_1}\right)\left(1+j\frac{f}{f_2}\right)\left(1+j\frac{f}{f_3}\right)}; 0 < f_1 < f_2 < f_3 \tag{3.31}$$

or,

$$A = \frac{A_{OL} \cdot \omega_1 \cdot \omega_2 \cdot \omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)} \tag{3.32}$$

with $0 < \omega_1 < \omega_2 < \omega_3$.

For a typical op-amp, straight line approximation of open-loop gain vs frequency in logarithmic scale is shown in Fig. 3.5. The open loop frequency response is flat (90 dB) from low frequencies (including dc) to 200 kHz, the first break frequency. From 200 kHz to 2 MHz, the gain drops from 90 dB to 70 dB which is at a –20 dB/decade or –6 dB/octave rate. At frequencies from 2 MHz to 20 MHz, the roll-off rate is –40 dB/decade or –12 dB/octave. Accordingly, as frequency is increasing, cascading effect of RC pairs (poles) come into effect and roll-off rate increases successively by –20 dB/decade at each corner frequency. Each RC pole pair also introduces a lagging phase of maximum up to –90°.

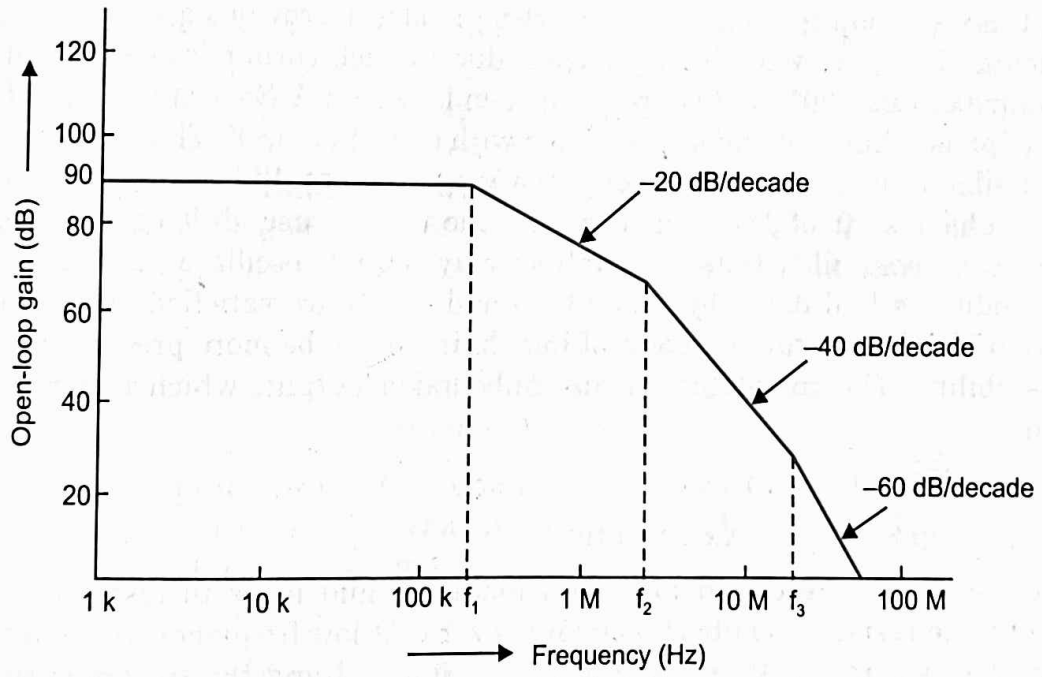


Fig. 3.5 Approximation of open loop gain vs frequency curve

3.3.2 Stability of an Op-Amp

Op-amps are rarely used in open loop configuration because of its high gain. Let us now consider the effect of feedback on op-amp frequency response. Consider an op-amp amplifier of Fig. 3.6 (a). It uses resistor feedback network and may be used as an inverting amplifier for $v_2 = 0$ and as non-inverting amplifier for $v_1 = 0$.

From the negative feedback concepts, we may write the closed loop transfer function as

$$A_{CL} = \frac{A}{1+A\beta} \tag{3.33}$$

where A is the open loop voltage gain and β is the feedback ratio. In Eq. (3.33), if characteristic equation $(1 + A\beta) = 0$, the circuit will become just unstable, that is, leads into sustained oscillation.

Rewriting the characteristic equation as, $1 - (-A\beta) = 0$ leads to

$$\text{loop gain, } -A\beta = 1 \qquad (3.34)$$

Since $A\beta$ is a complex quantity, the magnitude condition become

$$|A\beta| = 1 \qquad (3.35)$$

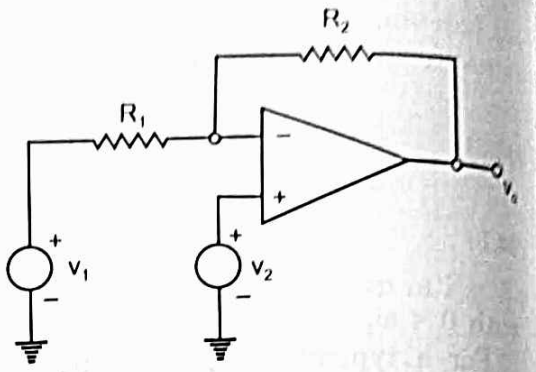


Fig. 3.6 (a) Resistive feedback provided in op-amp

and phase condition is

$$\angle -A\beta = 0 \text{ (or multiple of } 2\pi)$$

or,
$$\angle A\beta = \pi \text{ (or odd multiple of } \pi) \qquad (3.36)$$

In the given circuit, feedback network is a resistive network, so it does not provide any phase shift. Since op-amp is used in the inverting mode, it provides a phase shift of 180° at low frequencies. However, at high frequencies, due to each corner frequency, an additional phase shift of maximum –90° can take place in open loop gain A. So for two corner frequencies, a maximum of phase shift that can be associated with gain A is –180°. Thus at high frequencies, it is quite possible that for some value of β, the magnitude of $A\beta$ becomes unity when A has an additional phase shift of 180° which makes the total phase shift equal to zero. In this case, there is every possibility that the amplifier may begin to oscillate as both the magnitude and phase conditions laid down by Eqs. (3.35) and (3.36) are satisfied. This may be noted that oscillation is just the starting point of instability, or, to be more precise, it is just at the verge of instability. The instability means unbounded output; which can arise from Eq. (3.33), when

$$(1 + A\beta) < 1$$

or
$$A\beta < 0 \qquad \text{i.e. negative}$$

and then $A_{CL} > A$, i.e. the closed loop gain increases and leads to instability. The phase contribution by the resistive feedback network is zero. At low frequency, the additional phase contribution of A is zero, so $A\beta > 0$ and obviously $A_{CL} < A$ and the system is stable. But at high frequencies, the system A having three corner frequencies or three RC pole pair, there is a chance of open loop gain A to contribute a maximum of $-270°$ phase shift and for which $A\beta$ may become negative and instability occurs at high frequencies. This is further elaborated in Fig. 3.6 (b).

Let us say that a closed loop gain of 80 dB ($|A_{CL}| = 10{,}000$) is desired. The projection of 80 dB curve to the open loop frequency response curve intersects it at a –20 dB/decade rate of closure (point A) as shown in Fig. 3.6 (b). The bandwidth is approximately 600 kHz and a maximum of –90° phase shift is added to open loop gain A. The amplifier will remain stable.

Now, if the feedback resistors are so chosen that the op-amp has a closed loop gain of 1,000 or 60 dB, the bandwidth is about 3.5 MHz. However, now the 60 dB projection on the open-loop curve intersects at a –40 dB/decade rate of closure (point B). The maximum phase shift that may get added to is now (– 90° – 90°), that is –180°. This circuit is likely to be

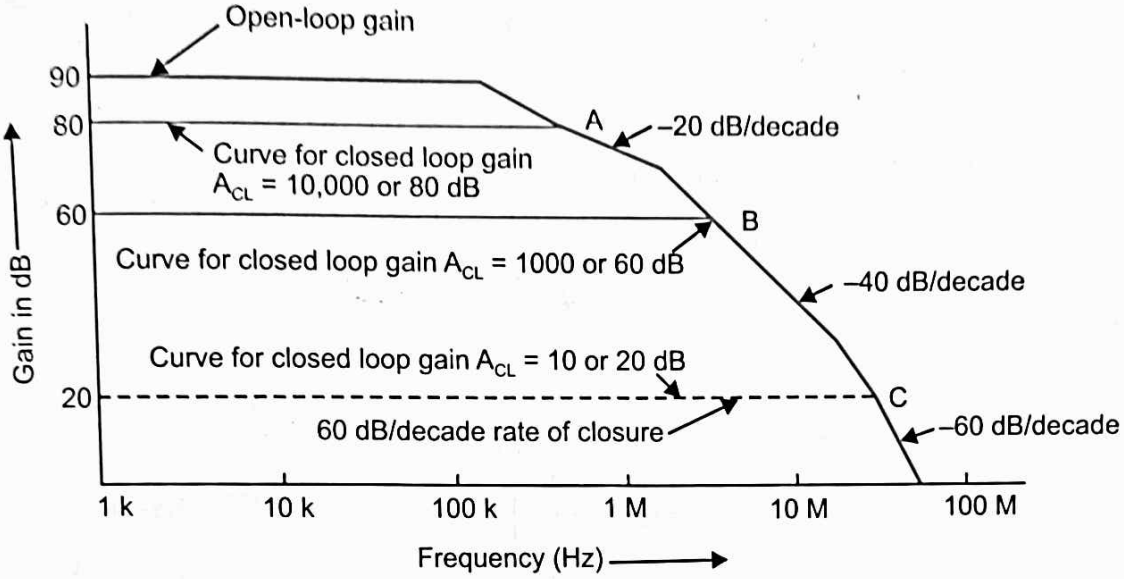


Fig. 3.6 (b) Effect of feedback on open loop gain vs frequency curve

unstable and should not be used without modification. Similarly, a closed loop gain of 20 dB causes a –60 dB/decade rate of closure (point C). A maximum –270° phase shift is added to the open loop gain A to cause unstable operation. Thus, we may conclude that for stable operation, the rate of closure between the closed loop gain projection and the open-loop curve should not exceed –20 dB/decade. At higher frequencies for lower closed loop gains, the feedback becomes significant and regenerative and may result in sustained oscillations.

So far, we have discussed stability of an op-amp qualitatively. To provide a quantitative discussion about stability, let us rewrite the transfer function of an op-amp characterized by three poles, as,

$$A = -\frac{A_{OL}\,\omega_1\,\omega_2\,\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)};\ 0 < \omega_1 < \omega_2 < \omega_3$$

Obviously the poles of the open-loop transfer function are at $-\omega_1$, $-\omega_2$ and $-\omega_3$. The closed loop poles, that is the poles of A_{CL} in Eq. (3.33) will be given by the roots of the characteristic equation

$$1 + A\beta = 0$$

Putting the value of A from Eq. (3.32), we get

$$1 + \frac{\beta A_{OL}\,\omega_1\,\omega_2\,\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)} = 0$$

or, $$(s+\omega_1)(s+\omega_2)(s+\omega_3) + \beta A_{OL}\,\omega_1\,\omega_2\,\omega_3 = 0$$

or, $$s^3 + s^2(\omega_1+\omega_2+\omega_3) + s(\omega_1\omega_2 + \omega_1\omega_3 + \omega_2\omega_3) + \omega_1\omega_2\omega_3 (1 + \beta A_{OL}) = 0 \quad (3.37)$$

The roots of the cubic equation depend upon βA_{OL}, the dc loop gain and therefore, (βA_{OL}) becomes critical parameter that determines the new pole location. Further, βA_{OL} can take any value between zero for no feedback ($\beta = 0$) and A_{OL} for maximum feedback ($\beta = 1$). For variable β in the range $0 < \beta A_{OL} < \infty$, the root loci is shown in Fig. 3.7. When $\beta A_{OL} = 0$, the roots are at $-\omega_1$, $-\omega_2$ and $-\omega_3$ and lie on the negative real axis. For small values of βA_{OL} the roots still lie on the left half of s-plane with one real root and two complex conjugate roots

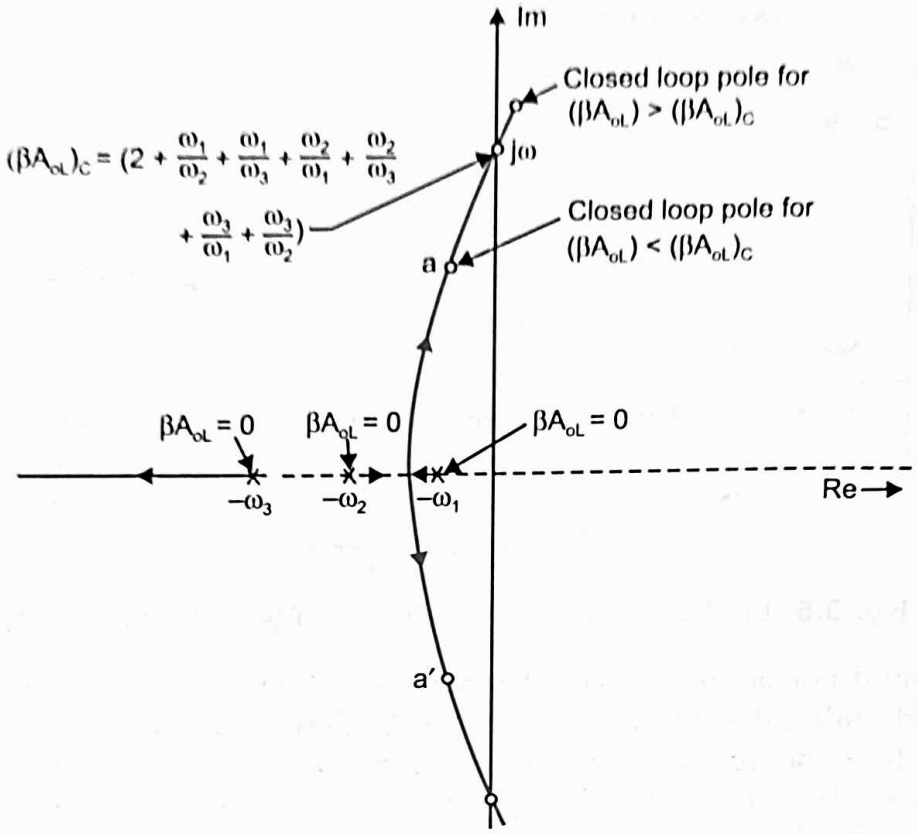


Fig. 3.7 Root loci as a function of βA_{OL}

(a, a′). If βA_{OL} is increased further beyond a critical value $(\beta A_{OL})_C$, the two roots will move to the right half of s-plane causing instability. We will find out that critical value of βA_{OL} for which the closed loop system becomes just unstable. Rewriting Eq. (3.37) as

$$a_3 s^3 + a_2 s^2 + a_1 s + a_o = 0 \tag{3.38}$$

where,

$$a_3 = 1$$
$$a_2 = \omega_1 + \omega_2 + \omega_3$$
$$a_1 = \omega_1 \omega_2 + \omega_1 \omega_3 + \omega_2 \omega_3$$
$$a_o = \omega_1 \omega_2 \omega_3 (1 + \beta A_{OL})$$

In order to find the critical value of βA_{OL}, apply ***Routh's stability criterion*** to Eq. (3.38). That is,

(i) All the coefficients a_3, a_2, a_1 and a_o should be positive.

(ii) $a_2 a_1 - a_3 a_o \leq 0$ (3.39)

Put $s = j\omega$ in Eq. (3.38)

$$a_3 (j\omega)^3 + a_2 (j\omega)^2 + a_1 (j\omega) + a_o = 0$$
$$(a_o - a_2 \omega^2) + j\omega(a_1 - a_3 \omega^2) = 0$$

Equating real and imaginary parts to zero, we get

$$a_o - a_2 \omega^2 = 0, \tag{3.40}$$
$$a_1 - a_3 \omega^2 = 0 \tag{3.41}$$

Thus, the frequency of oscillation is given by,

$$\omega_{osc} = \pm\sqrt{\frac{a_0}{a_2}} = \pm\sqrt{\frac{a_1}{a_3}} \tag{3.42}$$

Putting values of coefficients,

$$\omega_{osc} = \sqrt{\frac{a_1}{a_3}} + \sqrt{\omega_1\omega_2 + \omega_1\omega_3 + \omega_2\omega_3} \tag{3.43}$$

Also from Eq. (3.39), we get,

$$a_0 = \frac{a_2 a_1}{a_3}$$

or $\omega_1\omega_2\omega_3\{1 + (\beta A_{OL})_C\} = (\omega_1 + \omega_2 + \omega_3)(\omega_1\omega_2 + \omega_1\omega_3 + \omega_2\omega_3)$

or,
$$(\beta A_{OL})_C = 2 + \frac{\omega_1}{\omega_2} + \frac{\omega_1}{\omega_3} + \frac{\omega_2}{\omega_1} + \frac{\omega_2}{\omega_3} + \frac{\omega_3}{\omega_1} + \frac{\omega_3}{\omega_2} \tag{3.44}$$

It is obvious that $(\beta A_{OL})_C$ depends upon the ratio of open loop pole locations. The minimum value of $(\beta A_{OL})_C$ will occur when all the poles are located at the same place giving $(\beta A_{OL})_c = 8$.

As an example, if $A_{OL} = 10^5$ and $\omega_1 = \omega_2 = \omega_3 = 10^7$ rad/s, then the circuit will oscillate at a frequency of

$$\omega_{osc} = \omega_1\sqrt{3} = 10^7\sqrt{3} \text{ rad/s.}$$

On the other hand, if 10000 $\omega_1 = \omega_2 = \omega_3$, the critical loop gain is,

$$(\beta A_{OL})_C \simeq 2\frac{\omega_2}{\omega_1} \simeq 20000$$

and,
$$\beta_C < \frac{20000}{A_{OL}} = \frac{20000}{100000} = 0.2$$

In the Fig. 3.6 (a), $\beta = R_1/(R_1 + R_2)$.

For, $\beta < 0.2$,

$$\frac{R_1 + R_2}{R_1} > \frac{1}{0.2} = 5$$

or,
$$\frac{R_2}{R_1} \geq 4$$

This means that if op-amp is used as an inverting amplifier in Fig. 3.6 (a), the inverting gain magnitude should be greater than 4 and if used as non-inverting amplifier, the non-inverting gain should be greater than 5 for oscillation to sustain.

If it is desired that the amplifier should remain stable for any resistive network, that is, $0 < \beta < 1$, then A_{OL} must satisfy the most stringent condition for $\beta = 1$, that is,

$$A_{OL} < \left(2 + \frac{\omega_1}{\omega_2} + \frac{\omega_1}{\omega_3} + \frac{\omega_2}{\omega_1} + \frac{\omega_2}{\omega_3} + \frac{\omega_3}{\omega_1} + \frac{\omega_3}{\omega_2}\right) \tag{3.45}$$

3.3.3 Frequency Compensation

In applications where one desires large bandwidth and lower closed loop gain, suitable compensation techniques are used. Two types of compensating techniques are used (i) External Compensation, (ii) Internal Compensation.

External Frequency Compensation

Some types of op-amps are made to be used with externally connected compensating components specially if they are to be used for relatively low closed loop gain. The compensating network alters the open-loop gain so that the roll-off rate is –20 dB/decade over a wide range of frequency.

The common methods for accomplishing this are:

Dominant-pole compensation
Pole-zero (lag) compensation

Dominant-pole Compensation: Suppose A is the uncompensated transfer function of the op-amp in open-loop condition as given by Eq. (3.32). Introduce a dominant pole by adding RC-network in series with op-amp as in Fig. 3.8 (a) or by connecting a capacitor C from a suitable high resistance point to ground. The compensated transfer function A' becomes

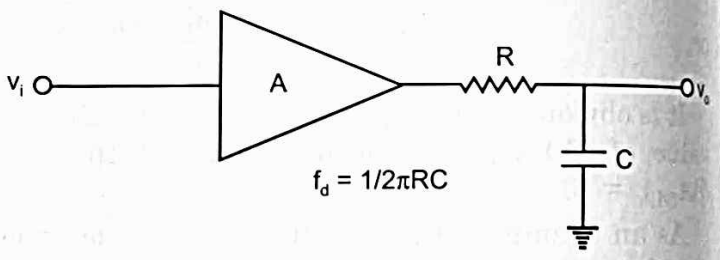


Fig. 3.8 (a) Dominant pole compensation

$$A' = \frac{v_o}{v_i}$$

$$= A \cdot \frac{\frac{-j}{\omega C}}{R - \frac{j}{\omega C}} = \frac{A}{1 + j\frac{f}{f_d}} \qquad (3.46)$$

where, $$f_d = \frac{1}{2\pi RC}$$

using Eq. (3.31) we get,

$$A' = \frac{A_{OL}}{\left(1 + j\frac{f}{f_d}\right)\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}$$

where $$f_d < f_1 < f_2 < f_3,$$

The capacitance C is chosen so that the modified loop gain drops to 0 dB with a slope of –20 dB/decade at a frequency where the poles of uncompensated transfer function A contribute negligible phase shift. Usually $f_d = \omega_d/2\pi$ is selected so that the compensated transfer function A' passes through 0 dB at the pole f_1 of the uncompensated A. The frequency can be found graphically by having A' pass through 0 dB at the frequency f_1 with a slope of –20 dB per decade as shown in the Fig. 3.8 (b). The value of capacitor C now can be calculated since $f_d = 1/2\pi RC$. There is, however, one disadvantage of this compensating technique. It

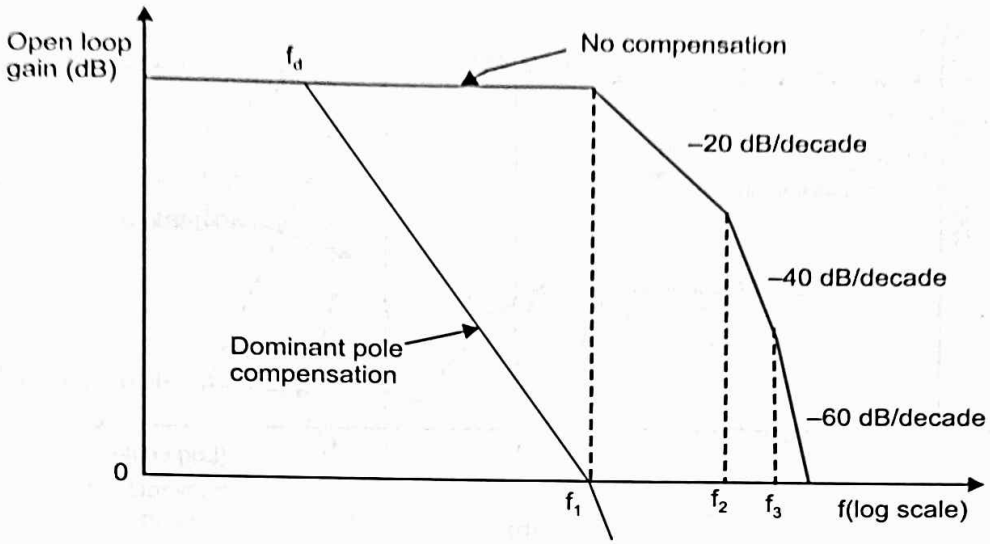


Fig. 3.8 (b) Gain vs frequency curve for dominant pole compensation

reduces the open-loop bandwidth drastically. But the noise immunity of the system is improved since the noise frequency components outside the bandwidth are eliminated.

Pole-zero Compensation: Here the uncompensated transfer function A is altered by adding both pole and a zero as shown in Fig. 3.9 (a). The zero should be at higher frequency than pole. The transfer function of the compensating network alone is,

$$\frac{v_o}{v_2} = \frac{Z_2}{Z_1 + Z_2} = \frac{R_2}{R_1 + R_2} \frac{1 + j\frac{f}{f_1}}{1 + j\frac{f}{f_o}} \tag{3.47}$$

where $Z_1 = R_1$, $Z_2 = R_2 + \frac{1}{j\omega C_2}$, $f_1 = \frac{1}{2\pi R_2 C_2}$, $f_o = \frac{1}{2\pi(R_1 + R_2)C_2}$

The compensating network is designed to produce a zero at the first corner frequency f_1 of the uncompensated transfer function A. This zero will cancel the effect of the pole at f_1. The pole of the compensating network at $f_o = \omega_o/2\pi$ is selected so that the compensated transfer function A' passes through 0 dB at the second corner frequency f_2 of the uncompensated transfer function A in Eq. (3.31). The frequency can be found graphically by having A' passes through 0 dB at the frequency f_2 with a slope of –20 dB/decade as shown in Fig. 3.9 (b). Assuming that the compensating network does not load the amplifier, *i.e.*, $R_2 >> R_1$, then the overall transfer function becomes

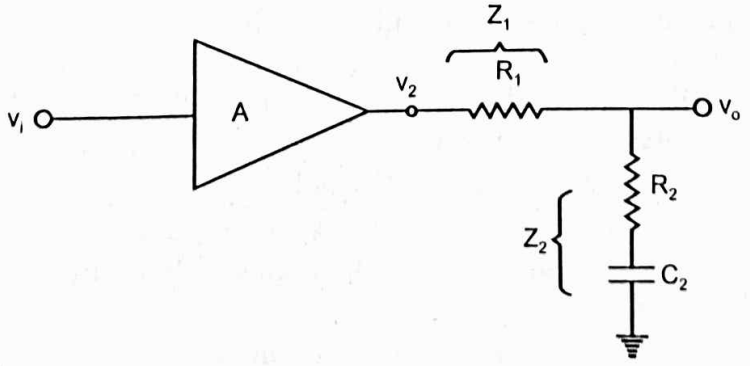
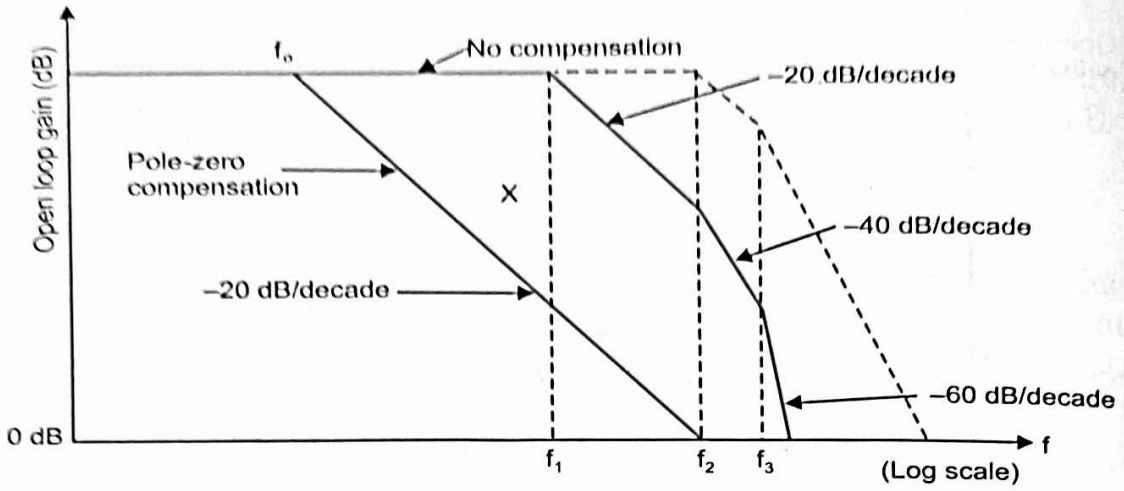


Fig. 3.9 (a) Pole-zero compensation



(b)

Fig. 3.9 (b) Open loop gain vs frequency for pole-zero compensation

$$A' = \frac{v_o}{v_i} = \frac{v_o}{v_2} \cdot \frac{v_2}{v_i} = A \cdot \frac{R_2}{R_1 + R_2} \frac{1 + j\frac{f}{f_1}}{1 + j\frac{f}{f_o}}$$

$$= \frac{A_{OL}}{\left(1 + j\frac{f}{f_1}\right)\left(1 + \frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)} \cdot \frac{R_2}{R_1 + R_2} \frac{1 + j\frac{f}{f_1}}{1 + j\frac{f}{f_o}}$$

$$= \frac{A_{OL}}{\left(1 + j\frac{f}{f_o}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)} \tag{3.48}$$

with $0 < f_o < f_1 < f_2 < f_3$

and note that $R_2 >> R_1$, so that $\frac{R_2}{R_1 + R_2} \approx 1$.

Consider again the frequency response (Bode plot) for the uncompensated op-amp having three poles at frequencies f_1, f_2 and f_3. Now select R_2 and C_2 so that the zero of the compensating network is equal to the pole at the frequency f_1 (lowest). If there had been no pole added by the compensating network, the response would have changed to that of the dotted curve. However, because of the predominance of the pole of the compensating network at f_o the rate of closure will be –20 dB/decade throughout as shown in the curve X of Fig. 3.9 (b). The pole at f_o should be selected so that the –20 dB/decade fall should meet the 0-dB line at f_2 which is the second pole of A.

A comparison of dominant pole and pole-zero compensation technique is shown in Fig. 3.10. The dominant pole is selected so that the compensated transfer function goes through 0-dB at the first pole f_1 of the uncompensated system. In pole-zero compensation, the zero is chosen at f_1 and pole is selected so that the modified transfer function goes through 0-dB at the second pole f_2 of uncompensated transfer function. The improvement in band width is clearly shown in Fig. 3.10 and is given by $(f_2 - f_1)$.

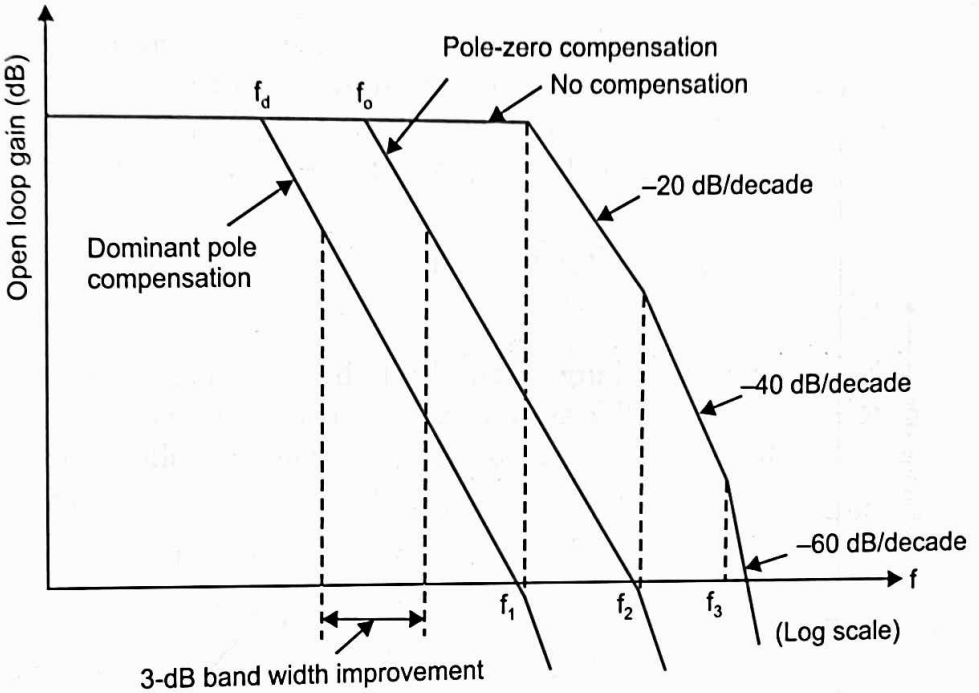


Fig. 3.10 Comparison of dominant pole and pole-zero techniques

With either type of compensation, the value of the compensating capacitance is too large to be easily built into standard integrated circuit and as a result, many IC op-amps have internal connections brought out to allow attachment of an external compensating network. However, recently, several op-amps have become available with built-in lag compensation which is accomplished by making use of Miller effect to generate large capacitance needed from fixed small capacitance which can be built into the IC.

Internally Compensated Operational Amplifier

Sometimes, the relatively broad bandwidth of the uncompensated op-amp is not needed. For example, in the instrumentation circuit, the op-amp required is to amplify relatively slow changing signals and therefore it does not require good high-frequency response. In this and similar applications, internally compensated op-amps can be used. They are sometimes called compensated op-amps. Also they are stable regardless of the value of closed-loop gain and without externally connected compensating components. The type 741 op-amp is compensated and has an open-loop gain vs frequency response as shown in Fig. 3.11. The op-amp IC 741 contains a capacitance C_1 of 30 pF (see Fig. 2.34 (b)) that internally shunts off signal current and thus reduces the available output signal at higher frequencies. This internal capacitance, which is an internal compensating component, causes the open-loop gain to roll-off at –20 dB/decade rate and thus assures for a stable circuit. The 741 op-amp has a 1 MHz gain-bandwidth product. This means that the product of the coordinates, gain and frequency of any point on the open-loop gain vs frequency curve is about 1 MHz. If 741 op-amp is wired

for a closed-loop gain of 10^4 or 80 dB, its bandwidth is 100 Hz as can be seen by projecting to the right from 10^4 in the curve of Fig. 3.11. For gain of 10^2, the bandwidth increases to 10 kHz and for gain 1, the bandwidth is 1 MHz. For 741 op-amp, unity gain-bandwidth product is specified as 1 MHz in the data sheet. This simply means that op-amp 741 has 1 MHz bandwidth with unity gain as seen in Fig. 3.11. Some internally compensated op-amps are Fairchild's μA741, National Semiconductor's LM741, LM107 and LM112 and Motorola's MC1558.

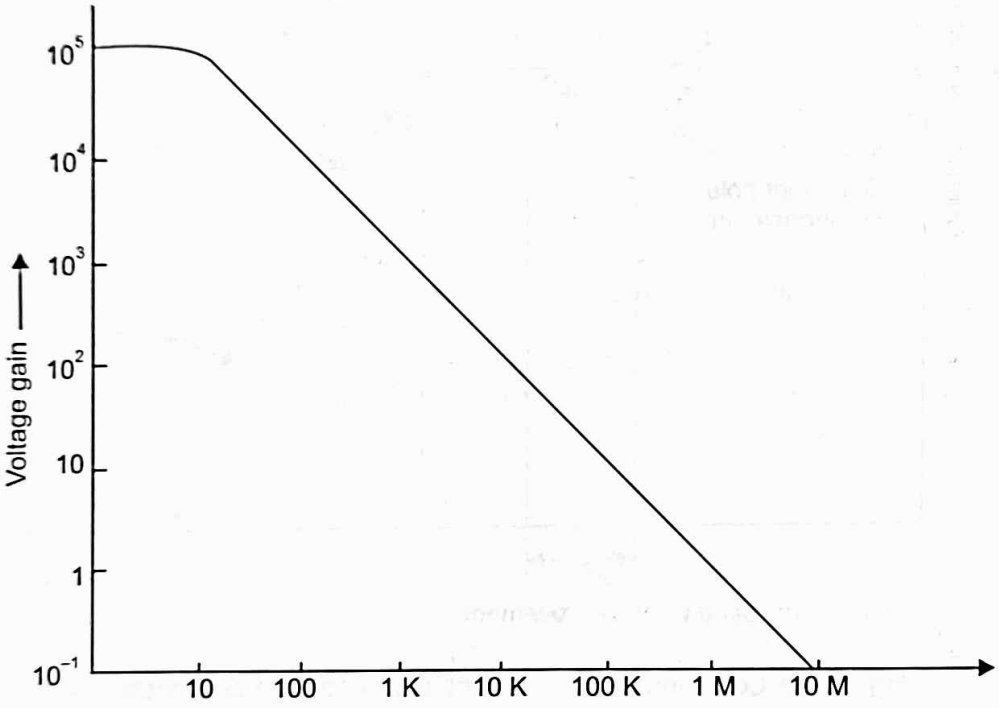


Fig. 3.11 Frequency response of μA741 op-amp

3.3.4 Slew Rate

The rise time of an amplifier is defined as the time the output takes to change from 10 to 90 per cent of the final value for a step input and is given as 0.35/BW, where BW is the bandwidth of the amplifier. Ideal response time should be zero second as BW is infinite for ideal op-amp, that is, output voltage should respond instantaneously to any change in the input. Rise time is usually specified for small signals, usually when the peak output voltage is less than one volt. However, for large signal output (i.e., $V_m > 1$ volt), the op-amp's speed is limited by slew rate, Manufacturers specify slew rate that gives the circuit designer a good idea of how quickly a given op-amp responds to changes of input voltage. An op-amp's slew rate is related to its frequency response. Usually op-amps with wide bandwidth will have higher (better) slew rates.

The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage and is usually specified in V/μs. For example, a 1V/μs slew rate means that the output rises or falls by 1 V in one microsecond. An ideal slew rate is infinite which means that op-amp's output voltage should change instantaneously in response to input step voltage. Practical IC op-amps have specified slew rates from 0.1 V/μs to well above 1000 V/μs. Slew rate listed in the data sheet is usually specified for unity gain and no load. The slew rate improves with higher closed loop gain and dc supply voltage. It is also a function to temperature and generally decreases with an increase in temperature.

What causes slew rate? There is usually a capacitor within or outside an op-amp to prevent oscillation. It is this capacitor which prevents the output voltage from responding immediately to a fast changing input. The rate at which the voltage across the capacitor v_c increases is given by,

$$\frac{dv_c}{dt} = \frac{I}{C} \tag{3.49}$$

Here, I is the maximum current furnished by op-amp to the capacitor C. This means that for obtaining faster slew rate, op-amp should have either a higher current or a small compensating capacitor. For the 741 C, the maximum internal capacitor charging current is limited to about 15 μA. So the slew rate (SR) of 741 C is,

$$SR = \left.\frac{dv_c}{dt}\right|_{max} = \frac{I_{max}}{C} = \frac{15\ \mu A}{30\ pF} = 0.5\ V/\mu s$$

Slew rate limits the response speed of all large signal waveshapes. For a sine wave input, the effect of slew rate limiting can be calculated as follows:

Consider a voltage follower shown in Fig. 3.12 (a). The input is large amplitude, high frequency sine wave.

If $v_s = V_m \sin \omega t$

Then, output $v_o = V_m \sin \omega t$

Figure 3.12 (b) shows the input-output waveform.

The rate of change of the output is given by,

$$\frac{dv_o}{dt} = V_m\ \omega \cos \omega t$$

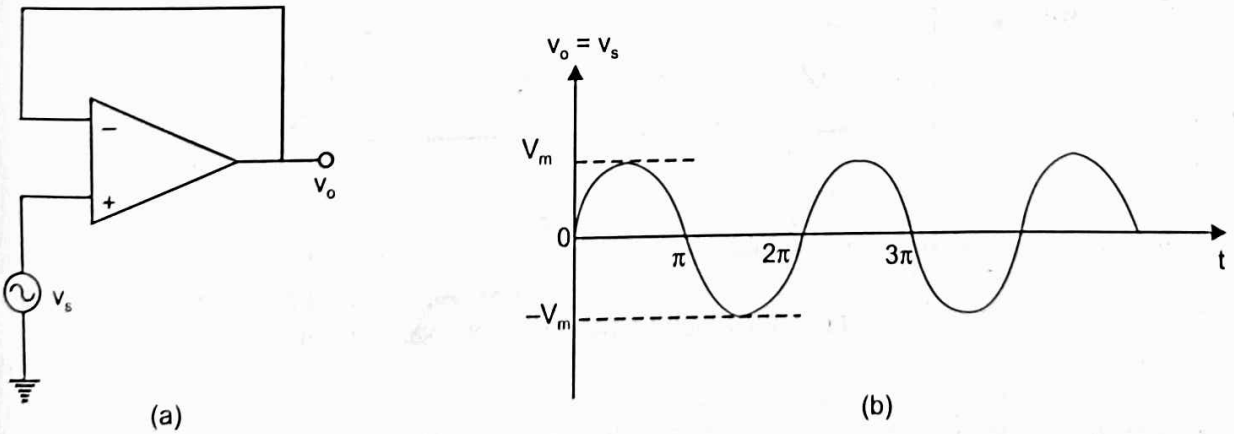


Fig. 3.12 (a) Voltage follower (b) Input/output waveform

The maximum rate of change of the output occurs when $\cos \omega t = 1$. That is,

$$SR = \left.\frac{dv_o}{dt}\right|_{max} = \omega V_m \tag{3.50}$$

Therefore, Slew Rate = $2\pi f V_m$ V/s

$$= \frac{2\pi f V_m}{10^6} \text{ V/μs} \quad (3.51)$$

Where f = input frequency (Hz),

V_m = peak output amplitude

If right hand side of Eq. (3.51) is less than the slew rate of the op-amp, then output will be undistorted. If frequency or amplitude of input signal is increased to exceed slew rate of op-amp, the output will be distorted.

Thus, the maximum input frequency f_{max} at which we can obtain an undistorted output voltage of peak value V_m is given by,

$$f_{max} \text{ (Hz)} = \frac{\text{Slew Rate}}{6.28 \times V_m} \times 10^6$$

This f_{max} is also called the full power response. It is the maximum frequency of a large amplitude sine wave with which op-amp can have without distortion.

Example 3.4

The output of an op-amp voltage follower is a triangular wave as shown in Fig. 3.13 for a square wave input of frequency 2 MHz and 8V peak to peak amplitude. What is the slew rate of the op-amp?

Solution

Since, slew rate is defined as the maximum rate of change of the output, so from Fig. 3.13, it can be seen that,

$$SR = \frac{6 \text{ V}}{(0.5/2)\mu\text{s}} = 14 \text{ V/μs}$$

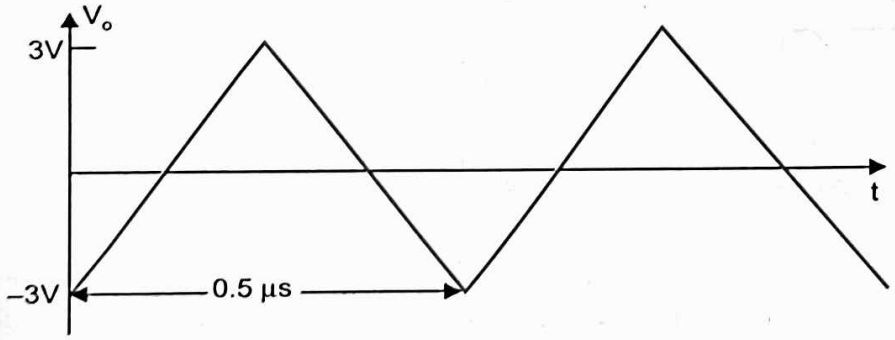


Fig. 3.13 Output waveform of Example 3.4

A less than ideal slew rate causes remarkable distortion for non-sinusoidal waveform of higher frequencies. Figure 3.14 shows typical waveforms of a voltage follower with square waves of various frequencies applied as input. The op-amp has a slew rate of 1 V/μs. The output gets worst due to limited slew rate as frequency increases. A 100 Hz square wave input produces a distortionless output as shown in Fig. 3.14 (b). And, a 10 kHz square wave gets distorted as shown in Fig. 3.14 (c). However, due to the limited slew rate, the square wave input of 1 MHz becomes distorted into sawtooth as in Fig. 3.14 (d). This has occurred because of the predominance of capacitance present in the circuit at higher frequencies, RC pairs are in cascade and the time

constants are high compared to the high frequency square wave input and the resultant output is obviously a sawtooth waveform of smaller amplitude.

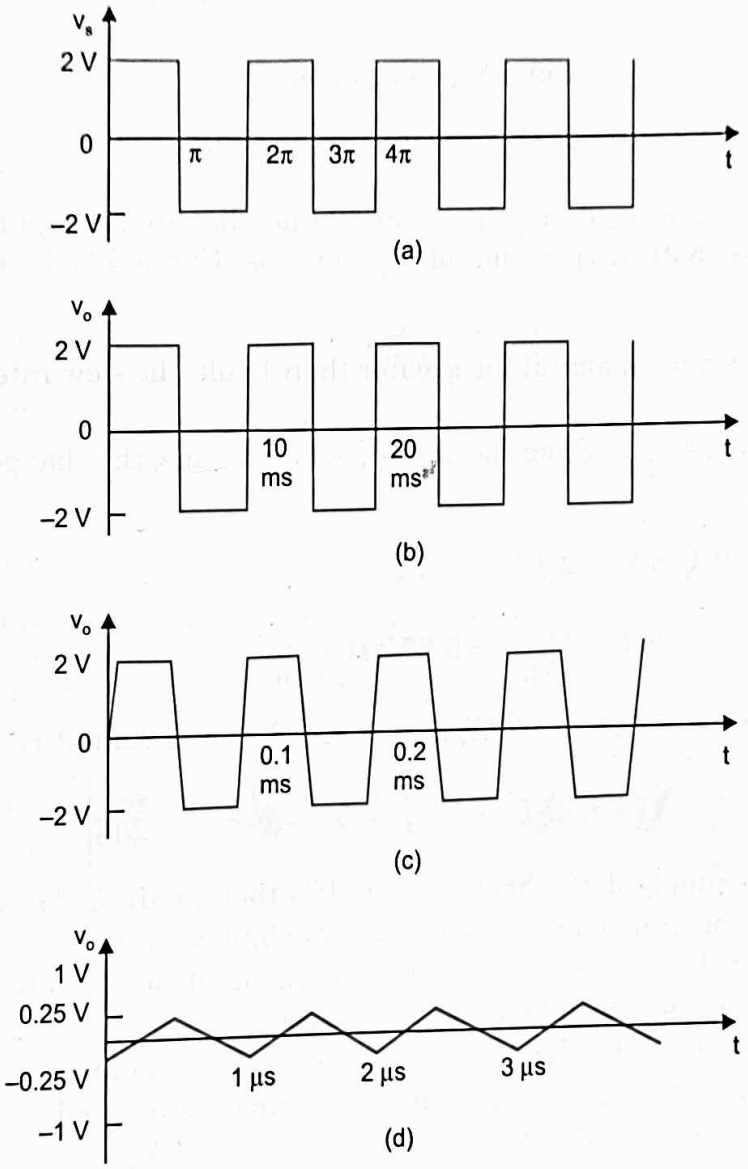


Fig. 3.14 (a) Square wave signal applied to a voltage follower using op-amp with slew rate 1 V/μs (b) Output for input frequency of 100 Hz (c) Output for input frequency of 100 kHz (d) Output for input frequency of 1 MHz

Example 3.5

A 741C op-amp is used as an inverting amplifier with a gain of 50. The voltage gain vs frequency curve of 741C is flat upto 20 kHz. What maximum peak to peak input signal can be applied without distorting the output?

Solution

The slew rate for 741C is 0.5 V/μs, so maximum output voltage at 20 kHz, is

$$0.5 = \frac{(2\pi)(20 \times 10^3)(V_m)}{10^6}$$

$$V_m = 3.98 \text{ V peak}$$

or, $V_o = 7.96$ V peak to peak.

Hence, for the output to be undistorted sine wave, the maximum input signal should be less than

$$\frac{7.96}{50} = 159 \text{ mV peak to peak.}$$

Example 3.6

A square wave of peak to peak amplitude of 500 mV has to be amplified to a peak-to-peak amplitude of 3 volts, with a rise time of 4 μs or less. Can a 741 be used?

Solution

Since, the output has a peak amplitude greater than 1 volt, the slew rate is the limiting factor.

The required slew rate = $\frac{\Delta v}{\Delta t}$. From the definition of rise time, the change in the output voltage Δv in 4 μs is equal to

$$(0.9 - 0.1)\ 3 \text{ V} = 2.4 \text{ V}$$

Therefore, $$SR = \frac{2.4 \text{ V}}{4 \text{ μs}} = 0.6 \text{ V/μs}$$

Since, the slew rate of 741 is 0.5 V/μs, it is too slow and cannot be used.

3.4 ANALYSIS OF DATA SHEETS OF AN OP-AMP

The manufacturers supply data sheets for the ICs they produce. These data sheets provide information regarding pin diagram, absolute maximum ratings, electrical characteristics, equivalent circuit of the devices etc. In this section, significance of the electrical parameters supplied in a typical op-amp data sheet is discussed.

Figure 3.15 gives the data sheet for a Fairchild μA741 op-amp. 741 series are available in models 741, 741A, 741C and 741E. The schematic diagram and electrical parameters for all these models are the same with only the values of the parameters differing from one model to another. We will consider specifications for 741C op-amp.

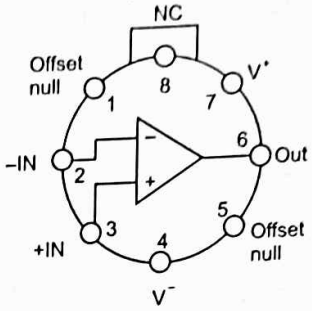
From the data sheet it can be seen that:

1. 741 is internally frequency compensated op-amp.
2. 741 is a monolithic IC fabricated using planar epitaxial process.
3. It is useful for integrator, summer, voltage follower and other feedback applications.
4. Absolute maximum ratings are specified for supply voltage, internal power dissipation, differential input voltage, input voltage, storage and operating temperature ranges, soldering pin temperature and output short circuit duration.
5. 741 is available in all three packages viz 8-pin metal can, 10-pin flat pack and 8 or 14 pin DIP. The pin diagrams for all these packages are shown in the data sheet.
6. For 741C, two sets of electrical specifications are available, one set is applicable at room temperature (25°C) and other set applies to the commercial temperature range (0° to

General Description: The μA741 is a high performance monolithic operational amplifier constructed using the planer epitaxial process. High common mode voltage range and absence of latch-up tendencies make the μA741 ideal for use as voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier and general feedback applications.

*No frequency compensation required
*Short circuit protection
*Offset voltage null capability
*Large common mode and differential voltage ranges
*Low power consumption
*No latch-up

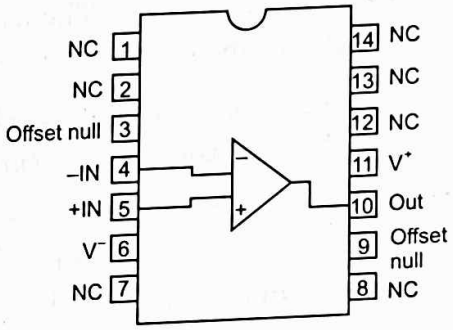
8 Pins Mini Metal Can (top view)



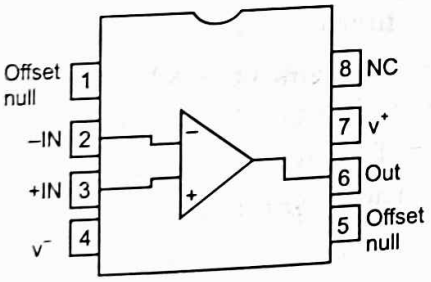
Absolute Maximum Ratings

Supply Voltage	
μA741A, μA741, μA741E	±22 V
μA741C	±18 V
Internal Power Dissipation	
Metal Can	500 m W
Molded and Hermetic DIP	670 m W
Mini DIP	310 m W
Flatpack	570 m W
Differential Input Voltage	±30 V
Input Voltage	±15 V
Operating Temperature Range	
Military (μA741A, μA741)	– 55 °C to 125 °C
Commercial (μA741E, μA741C)	0 °C to 70 °C

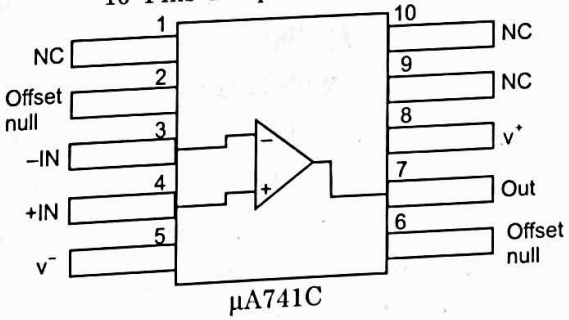
10 Pins DIP(top view)



8 Pins Mini DIP (top view)



10 Pins Flatpak (top view)



μA741C

Electrical Characteristics V_s = ±15 V, T_A = 25°C unless otherwise specified

Characteristics (see definitions)		Conditions	Min	Typ	Max	Units
Input Offset Voltage		$R_s \leq 10$ kΩ		20		mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				1.4		pF
Offset Voltage Adjustment Range				±15		mV
Input Voltage Range			±12	±13		V
Common Mode Rejection Ratio		$R_s \leq 10$ kΩ		70	90	dB
Supply Voltage Rejection Ratio		$R_s \leq 10$ kΩ			30	150	μV/V
Large Singal Voltage Gain		$R_L \geq$ kΩ			20,000	200,000	
Output Voltage Swing		V_{out} = ±10 V					V
		$R_L \geq 10$ kΩ	±12	±14			V
		$R_L \geq 2$ kΩ	±10	±13			
Output Resistance				75		Ω	
Output Short Circuit Current				25		mA	
Supply Current				1.7	2.8	mA	
Power Consumption				50	85	mW	
Transient Response (unity Gain)	Rise Time	V_{in} = 200 mV, R_L = 2 kΩ, C_L = 100 pF			0.3		μs
	Overshoot				6.0		%
Slew Rate		$R_L \geq 2$ kΩ			0.5		V/μs

Fig. 3.15 Data Sheet of μA741

+70°C). As we are interested only in showing the significance of the parameters listed, we limit the discussion to only one model, that is 741C at 25°C.

The various electrical parameters supplied in the data sheet are as follows:

Input offset voltage: It is the voltage that must be applied between the input terminals of an op-amp to nullify the output. Since this voltage could be positive or negative its absolute value is listed on the data sheet. For 741C, the maximum value is 6 mV.

Input offset current: The algebraic difference between the currents into the (–) input and (+) input is referred to as input offset current. It is 200 nA maximum for 741C.

Input bias current: The average of the currents entering into the (–) input and (+) input terminals of an op-amp is called input bias current. Its value is 500 nA for 741C.

Input resistance: This is the differential input resistance as seen at either of the input terminals with the other terminal connected to ground. For the 741C, the input resistance is 2 MΩ.

Input capacitance: It is the equivalent capacitance that can be measured at either of the input terminal with the other terminal connected to ground. A typical value of C_i is 1.4 pF.

Offset voltage adjustment range: A special feature of the 741 family op-amp is the provision of offset voltage null capability. For this refer to Sec. 3.2.4. For 741C offset voltage adjustment range is ±15 mV.

Input voltage range: This is the common-mode voltage that can be applied to both input terminals without disturbing the performance of an op-amp. For the 741C, the range of the input common-mode voltage is ±13 V. Common-mode configuration is used only for test purpose to determine the degree of matching between the inverting and non-inverting terminals.

Common-mode rejection ratio: It has been discussed in detail in Sec. 2.3.7. For 741C, CMRR is typically 90 dB. CMRR is usually measured under the test condition that the input source resistance $R_s \leq 10$ kΩ. The higher the value of CMRR, better is the matching between the two input terminals and smaller the output common-mode voltage.

Supply voltage rejection ratio: The change in an op-amp's input offset voltage due to variations in supply voltage is called the supply voltage rejection ratio (SVRR). Some manufacturers use terms like power supply rejection ratio (PSRR) or power supply sensitivity (PSS). These terms are expressed in microvolts per volt or in decibels. For 741C, SVRR = 150 μV/V. Obviously, lower the value of SVRR, better the op-amp.

Large signal voltage gain: An op-amp amplifies the difference voltage between the two input terminals and, therefore, its voltage gain is defined as,

$$\text{Voltage gain} = \frac{\text{output voltage}}{\text{differential input voltage}}$$

Since the amplitude of the output signal is much larger than the input signal, the voltage gain is commonly referred as large signal voltage gain. For 741C, typical value is, 2,00,000 under test conditions, $R_L \geq 2\,k\Omega$ and $V_o = \pm 10$ V.

Output voltage swing: The output voltage swing indicates the value of positive and negative saturation voltages of an op-amp, and never exceeds the supply voltage V^+ and V^-. For 741C, the output voltage swing is guaranteed to be between +13 V and –13 V for $R_L \geq 2\,k\Omega$.

Output resistance: Output resistance R_o is the resistance measured between the output terminal of the op-amp and the ground. It is 75 Ω for the 741C op-amp.

Output short circuit current: This is the current that may flow if an op-amp gets shorted accidentally and is generally high. The op-amp must be provided with short circuit protection. The short circuit current I_{sc} for 741C is 25 mA. This means that the built-in short circuit protection is guaranteed to withstand 25 mA of current.

Supply current: Supply current I_s is the current drawn by the op-amp from the power supply. It is 2.8 mA for 741C.

Power consumption: This gives the amount of quiescent power ($V_i = 0$ V) that must be consumed by the op-amp so as to operate properly. It is 85 mW for 741C.

Transient response: The rise time and overshoot are the two characteristics of the transient response of any circuit. These parameters are of importance whenever selecting an op-amp for ac applications. The transient response test circuit is included in the data sheet. For 741C, rise time is 0.3 μs and overshoot is 5%.

Slew rate: This is another parameter of importance whenever selecting an op-amp for high frequency applications. It has been discussed in detail in Sec. 3.3.4. Op-amp 741C has a low slew rate (0.5 V/μs) and therefore cannot be used for high frequency applications.

SUMMARY

1. A practical op-amp is not ideal and has finite values of input offset voltage, input offset current and input bias current. These produce a dc offset voltage at the output.
2. Input bias-current is the dc current necessary to flow into the inputs of op-amp to turn it *on*. The effect of input bias currents can be reduced by using compensating resistor R_{comp}.
3. Input offset current results due to non-identical transistors and is minimized by using a T-network in the feedback path.
4. Input offset voltage can be nulled by using external balancing techniques.
5. The input offset voltage and current drift with the change in temperature, thereby producing a dc error voltage in the output.
6. The gain of an op-amp decreases (rolls-off) at high frequencies because of capacitances within an op-amp.
7. The open-loop gain of the op-amp decreases at the rate of –20 dB/decade or –6 dB/octave at each break frequency.

8. An open-loop op-amp gives very small bandwidth. Feedback increases the bandwidth but may cause instability.
9. For a stable circuit, the additional phase angle provided by op-amp must be less than 180° when its magnitude reaches unity.
10. Compensating networks are used to control the phase shift and hence improve the stability.
11. External compensation is done either by pole compensation or pole-zero compensation.
12. Internally compensated op-amps are also available but give smaller bandwidth.
13. Large signal output (>1 V) is limited by the speed at which the op-amp can charge compensating capacitor. This is called slew rate and is expressed in volts per micro-second.
14. The manufacturers supply data sheets for the ICs they produce. The data sheet gives pin diagrams, equivalent circuits, absolute maximum ratings, electrical characteristics and typical applications of the device.

REVIEW QUESTIONS

3.1. List the non-ideal dc characteristics of an op-amp.
3.2. Why do we use R_{comp} resistor?
3.3. Why is R_{comp} not needed in differential amplifier?
3.4. How is input offset voltage compensated for?
3.5. What produces more offset voltage at the output: input offset current or input bias current?
3.6. Define thermal drift.
3.7. List the parameters that are important for ac applications.
3.8. What does the term roll-off mean?
3.9. What is Bode plot?
3.10. What problem can occur with an amplifier with a steep gain roll-off?
3.11. Why are low closed loop gains avoided with uncompensated op-amps?
3.12. If an op-amp is specified as being compensated, what does this mean?
3.13. If closed loop gain of an op-amp is increased, what happens to bandwidth?
3.14. If the gain-bandwidth product of an op-amp is 2 MHz, what is its bandwidth when connected as a voltage follower?
3.15. Define slew rate. What causes the slew rate?
3.16. How is the slew rate measured?
3.17. What is the effect of operation frequency on the maximum unclipped output signal capability of an op-amp?
3.18. List and explain the parameters given in manufacturer's data sheet of an op-amp.
3.19. The dc open loop gain of an op-amp is 100,000. What will be the open loop gain at its break frequency?
3.20. The transient response rise time (*unity gain*) of an op-amp is 0.07 μs. Find the small signal band width.
3.21. What is the difference between the open loop and closed loop gain of an op-amp?
3.22. Does increasing the compensating capacitor increase or decrease unity-gain band-width?

3.23. How fast can the output of an op-amp change by 10 V, if its slew rate is 1 V/μs?
3.24. Find the maximum frequency for a sine wave output voltage of 10 V peak with an op-amp whose slew rate is 1 V/μs.

PROBLEMS

3.1. A 741 op-amp is used as an inverting amplifier shown in Fig. 3.2 (c) with $R_1 = 1$ kΩ and $R_f = 100$ kΩ. What is the maximum output offset voltage caused by the input offset voltage V_{ios}? For 741, $V_{ios} = 6$ mV.
3.2. Repeat Problem 3.1, if op-amp used is LM307 with $V_{ios} = 10$ mV; $R_1 = 100$ Ω and $R_f = 4.7$ kΩ.
3.3. In an inverting amplifier of the type shown in Fig. 3.2 (c), $R_1 = 100$ kΩ, $R_f = 10$ MΩ. Calculate (i) maximum output offset voltage caused by the input offset voltage V_{ios}; (ii) maximum output offset voltage caused by the input bias current I_B. The op-amp used is 741 with $V_{ios} = 6$ mV; $I_B = 500$ nA.
3.4. In Problem 3.3, calculate the value of R_{comp} needed to eliminate the effect of input bias current.
3.5. In an inverting amplifier $R_1 = 1$ kΩ, $R_f = 100$ kΩ. The op-amp has the following specifications:

$$\frac{\Delta V_{ios}}{\Delta T} = 30\ \mu V/°C \text{ max.}$$

$$\frac{\Delta I_{os}}{\Delta T} = 0.3\ nA/°C \text{ max.}$$

Assume that the amplifier is nulled at 25°C. Calculate the value of the error voltage and the output voltage V_o at 35°C, if (i) $V_i = 1$ mV dc; (ii) $V_i = 5$ mV dc.
3.6. Repeat Problem 3.5, for a non-inverting amplifier.
3.7. The LM312 op-amp is used as an inverting amplifier with the following specifications:

$$\frac{\Delta V_{ios}}{\Delta T} = 30\ \mu V/°C;\ \frac{\Delta I_{os}}{\Delta T} = 10\ nA/°C$$

$$R_1 = 1\ k\Omega;\ R_f = 4.7\ k\Omega.$$

Assume that the amplifier is nulled at 25°C. A sine wave of 10 mV peak amplitude at 100 Hz is applied. Draw the output voltage waveform at 25°C and 45°C.
3.8. Repeat Problem 3.7 for a non-inverting amplifier.
3.9. (a) An op-amp has a slew rate of 2 V/μs. What is the maximum frequency of an output sinusoid of peak value 5 V at which distortion sets in due to the slew rate limitation?
(b) If a sinusoid of 10 V peak is specified, what is the full power bandwidth?
3.10. An op-amp has a slew rate of 2V/μs. Find the rise time for an output voltage of 10 V amplitude resulting from a rectangular pulse input if the op-amp is slew rate limited.

EXPERIMENT 3.1

To measure (a) input bias current, (b) input offset current and (c) input offset voltage of the given op-amp.

PROCEDURE

(a) Set up the circuit shown in Fig. E. 3.1 (a) to measure I_B^- (inverting input bias current) and Fig. E. 3.1 (b) to measure I_B^+ (non-inverting input bias current). Select a large resistor (in MΩ) and measure the output voltage. Calculate $I_B^- = V_o/R_f$ and $I_B^+ = V_o/R$.

(b) Offset current may be measured by the circuit shown in Fig. E. 3.1 (c). The use of the equal resistors cancel the effect of the bias current. The offset current $I_{os} = V_o/R_f$.

(c) To measure input offset voltage, set up the circuit shown in Fig. E. 3.1 (d). The effect of the bias current is compensated by R_{comp}. The output voltage is given by,

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + I_{os} R_f$$

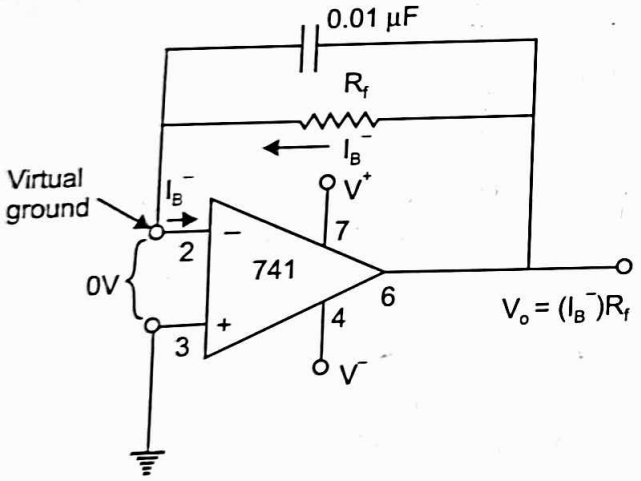


Fig. E. 3.1 (a) Measurement of inverting input bias current

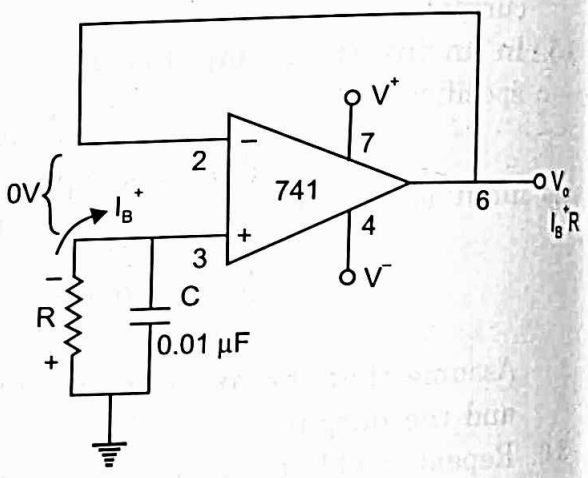


Fig. E. 3.1 (b) Measurement of non-inverting input bias current

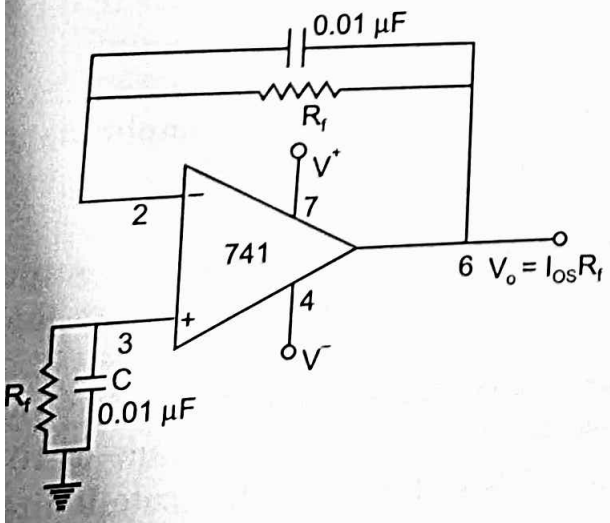


Fig. E. 3.1 (c) Offset current measurement

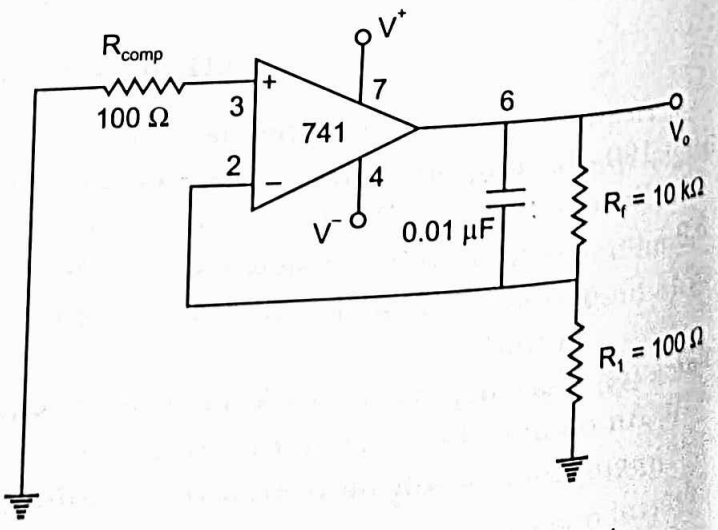


Fig. E. 3.1 (d) Offset voltage measurement

$$\simeq \left(1+\frac{R_f}{R_1}\right)V_{ios}$$

The value of V_{ios}, so obtained gives typically 98 per cent accuracy.

EXPERIMENT 3.2

To measure the slew rate of the 741C op-amp.

PROCEDURE

1. Connect the op-amp as shown in Fig. E. 3.2.
2. Adjust the input sine-wave signal generator so that the output is 1 V peak sine wave at 1 kHz.
3. Slowly increase the input signal frequency until the output gets just distorted.
4. Calculate slew rate, $SR = \frac{2\pi f V_m}{10^6}$ V/μs where V_m = peak output amplitude in volts and f = frequency in Hz.
5. Now give a square-wave input and repeat step 2.
6. Increase the input frequency slowly until the output is just barely a triangular wave. The slew rate,

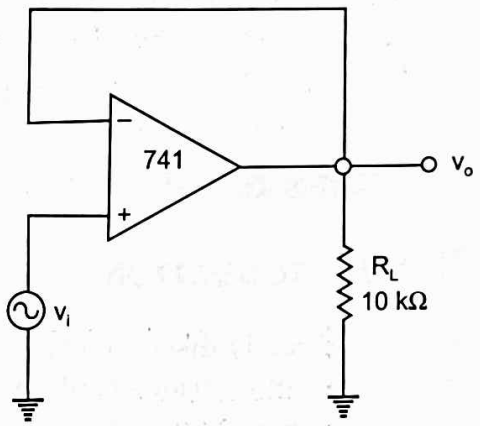


Fig. E. 3.2 Voltage follower to measure slew rate

$$SR = \frac{\Delta v_o}{\Delta t} \text{ V/μs}$$

where, Δv_o = change in the output voltage amplitude in volts.
Δt = time required for Δv_o in μs.

4

OPERATIONAL AMPLIFIER APPLICATIONS

4.1 INTRODUCTION

We have already discussed the electronics of op-amp, its dc and ac characteristics, parameter limitations and various configurations. Now we take a look at the applications of an op-amp. As we shall see, op-amp has countless applications and forms the basic building block of linear and non-linear analog systems. In linear circuits, the output signal varies with the input signal in a linear manner. Some of the linear applications discussed in this chapter are: adder, subtractor, voltage to current converter and current to voltage converter, instrumentation amplifier, analog computation, power amplifier etc.

There is another class of circuits with highly non-linear input to output characteristics. Rectifier, peak detector, clipper, clamper, sample and hold circuit, log and antilog amplifier, multiplier are the various non-linear circuits discussed. These non-linear circuits are very useful in industrial instrumentation, communication and general signal processing.

4.2 BASIC OP-AMP APPLICATIONS

Scale Changer/Inverter

In the basic inverting amplifier of Fig. 4.1, if the ratio $R_f/R_1 = K$, where K is a real constant, then the closed loop gain $A_{CL} = -K$. The circuit thus could be used to multiply by a constant factor if R_f and R_1 are selected as precision resistors. For $R_f = R_1$, $A_{CL} = -1$ and the circuit is called an inverter, *i.e.*, the output is 180° out of phase with respect to input though the magnitudes are same.

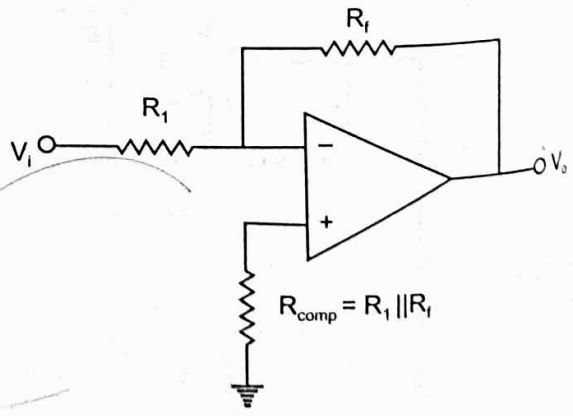


Fig. 4.1 Scale changer for $(R_f/R_1 = K)$ and phase inverter for $(R_f/R_1 = 1)$

Summing Amplifier

Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or a summer. An inverting summer or a non-inverting summer may be obtained as discussed now.

Inverting Summing Amplifier

A typical summing amplifier with three input voltages V_1, V_2 and V_3, three input resistors R_1, R_2, R_3 and a feedback resistor R_f is shown in Fig. 4.2 (a). The following analysis is carried out assuming that the op-amp is an ideal one, that is, $A_{OL} = \infty$ and $R_i = \infty$. Since the input bias current is assumed to be zero, there is no voltage drop across the resistor R_{comp} and hence the non-inverting input terminal is at ground potential.

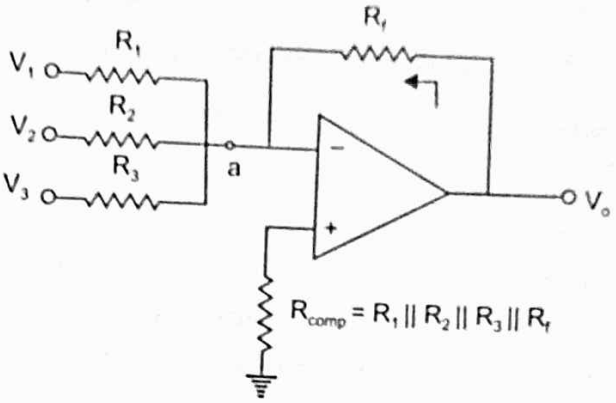


Fig. 4.2 (a) Inverting summing amplifier

The voltage at node 'a' is zero as the non-inverting input terminal is grounded. The nodal equation by KCL at node 'a' is

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_o}{R_f} = 0$$

or,

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right) \tag{4.1}$$

Thus, the output is an inverted, weighted sum of the inputs. In the special case, when $R_1 = R_2 = R_3 = R_f$, we have

$$V_o = -(V_1 + V_2 + V_3) \tag{4.2}$$

in which case the output V_o is the inverted sum of the input signals. We may also set

$$R_1 = R_2 = R_3 = 3R_f$$

in which case

$$V_o = -\left(\frac{V_1 + V_2 + V_3}{3}\right) \tag{4.3}$$

Thus, the output is the average of the input signals (inverted). In a practical circuit, input bias current compensating resistor R_{comp} should be provided as discussed in Sec. 3.2.1. To find R_{comp}, make all inputs $V_1 = V_2 = V_3 = 0$. So the effective input resistance $R_i = R_1 \| R_2 \| R_3$. Therefore, $R_{comp} = R_i \| R_f = R_1 \| R_2 \| R_3 \| R_f$.

Example 4.1

Design an adder circuit using an op-amp to get the output expression as

$$V_o = -(0.1\ V_1 + V_2 + 10\ V_3)$$

where V_1, V_2, and V_3 are the inputs.

Solution

The output in Fig. 4.2 (a) is

$$V_o = -[(R_f/R_1)\,V_1 + (R_f/R_2)V_2 + (R_f/R_3)V_3]$$

say $R_f = 10\ k\Omega,\ R_1 = 100\ k\Omega,\ R_2 = 10\ k\Omega,\ R_3 = 1\ k\Omega$

Then the desired output expression is obtained.

Non-inverting Summing Amplifier

A summer that gives a non-inverted sum is the non-inverting summing amplifier of Fig. 4.2 (b). Let the voltage at the (–) input terminal be V_a. The voltage at (+) input terminal will also be V_a. The nodal equation at node 'a' is given by

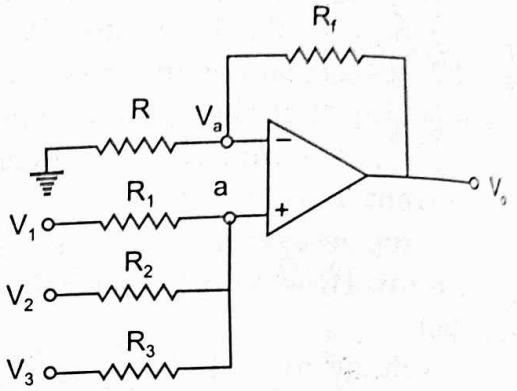


Fig. 4.2 (b) Non-inverting summing amplifier

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = 0$$

from which we have,

$$V_a = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} \tag{4.4}$$

The op-amp and two resistors R_f and R constitute a non-inverting amplifier with

$$V_o = \left(1 + \frac{R_f}{R}\right) V_a \tag{4.5}$$

Therefore, the output voltage is,

$$V_o = \left(1 + \frac{R_f}{R}\right) \frac{\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} \tag{4.6}$$

which is a non-inverted weighted sum of inputs.

Let $R_1 = R_2 = R_3 = R = R_f/2$, then $V_o = V_1 + V_2 + V_3$

Subtractor

A basic differential amplifier can be used as a subtractor as shown in Fig. 4.3 (a). If all resistors are equal in value, then the output voltage can be derived by using superposition principle. To find the output V_{o1} due to V_1 alone, make $V_2 = 0$. Then the circuit of Fig. 4.3 (a) becomes a non-inverting amplifier having input voltage $V_1/2$ at the non-inverting input terminal and the output becomes

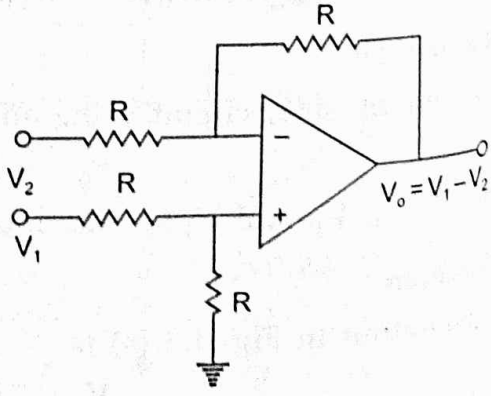


Fig. 4.3 (a) Op-amp as subtractor

$$V_{o1} = \frac{V_1}{2}\left(1 + \frac{R}{R}\right) = V_1 \tag{4.7}$$

Similarly the output V_{o2} due to V_2 alone (with V_1 grounded) can be written simply for an inverting amplifier as

$$V_{o2} = -V_2 \tag{4.8}$$

Thus the output voltage V_o due to both the inputs can be written as

$$V_o = V_{o1} + V_{o2} = V_1 - V_2 \tag{4.9}$$

Adder-Subtractor

It is possible to perform addition and subtraction simultaneously with a single op-amp using the circuit shown in Fig. 4.3 (b).

The output voltage V_o can be obtained by using superposition theorem. To find output voltage V_{o1} due to V_1 alone, make all other input voltages V_2, V_3 and V_4 equal to zero. The simplified circuit is shown in Fig. 4.3 (c). This is the circuit of an inverting amplifier and its output voltage is,

$$V_{o1} = -\frac{R}{R/2}\frac{V_1}{2} = -V_1 \tag{4.10}$$

(by Thevenin's equivalent circuit at inverting input terminal).

Similarly, the output voltage V_{o2} due to V_2 alone is,

$$V_{o2} = -V_2 \tag{4.11}$$

Now, the output voltage V_{o3} due to the input voltage signal V_3 alone applied at the (+) input terminal can be found by setting V_1, V_2 and V_4 equal to zero. The circuit now becomes a non-inverting amplifier as shown in Fig. 4.3 (d). The voltage V_a at the non-inverting terminal is

$$V_a = \frac{R/2}{R + R/2} V_3 = V_3/3 \tag{4.12}$$

So, the output voltage V_{o3} due to V_3 alone is

$$V_{o3} = \left(1 + \frac{R}{R/2}\right) V_a = 3\left(\frac{V_3}{3}\right) = V_3 \tag{4.13}$$

Similarly, it can be shown that the output voltage V_{o4} due to V_4 alone is

$$V_{o4} = V_4 \tag{4.14}$$

Thus, the output voltage V_o due to all four input voltages is given by

$$\begin{aligned} V_o &= V_{o1} + V_{o2} + V_{o3} + V_{o4} \\ &= -V_1 - V_2 + V_3 + V_4 \\ &= (V_3 + V_4) - (V_1 + V_2) \end{aligned} \tag{4.15}$$

So, the circuit is an adder-subtractor.

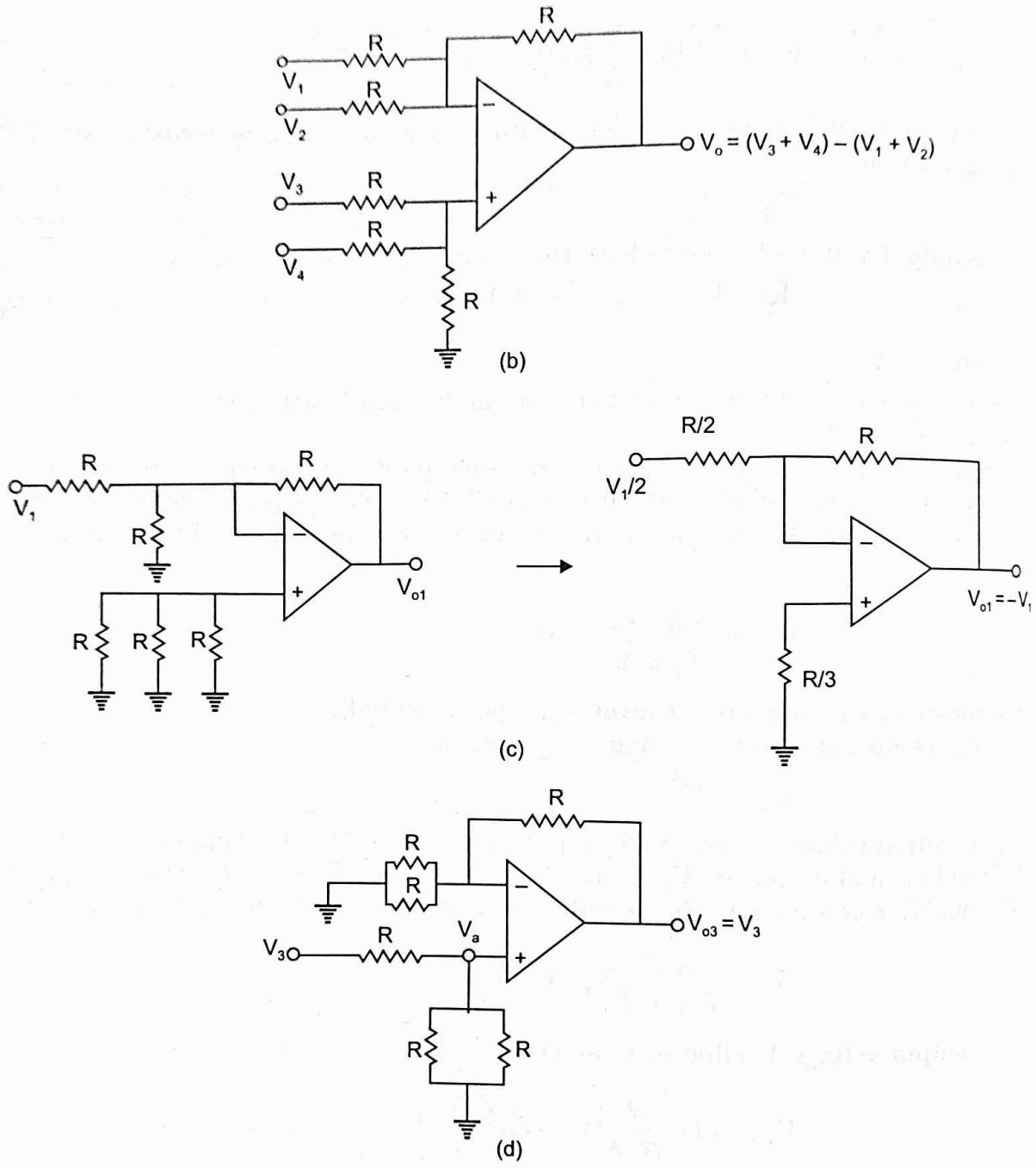


Fig. 4.3 (b) Op-amp adder-subtractor, (c) Simplifier circuit for $V_2 = V_3 = V_4 = 0$, (d) Simplified circuit for $V_1 = V_2 = V_4 = 0$

Example 4.2

Find V_o for the adder-subtractor shown in Fig. 4.4 (a).

Solution

The negative sum is obtained by setting $V_3 = V_4 = 0$. Thus,

$$V_o' = -\frac{50}{40}V_1 - \frac{50}{25}V_2$$

$$= -1.25V_1 - 2V_2$$

Now set $V_1 = V_2 = 0$ to find the output voltage due to V_3 and V_4. The voltage V_+ at the (+) input terminal due to V_3 and V_4 can be found by using superposition theorem as shown in Fig. 4.4 (b) as

$$V_+ = \frac{12}{10+12} V_3 + \frac{7.5}{20+7.5} V_4$$

or,
$$V_+ = 0.545\, V_3 + 0.273\, V_4$$

The output voltage V_o'' due to V_3 and V_4 now can be determined from the equivalent circuit of Fig. 4.4 (c) as

$$V_o'' = \left(1 + \frac{R'}{R}\right) V_+$$

Here, $R' = 50\ \text{k}\Omega$ and $R = 40 \,||\, 25 = 15.38\ \text{k}\Omega$

Therefore,
$$V_o'' = \frac{50 + 15.38}{15.38} (0.545\, V_3 + 0.273\, V_4)$$
$$= 2.32\ V_3 + 1.16\ V_4$$

The total output voltage V_o is given by

$$V_o = V_o' + V_o'' = -1.25\ V_1 - 2.0\ V_2 + 2.32\ V_3 + 1.16\ V_4$$

Putting the value of V_1, V_2, V_3 and V_4, we get

$$V_o = -1.25 \times 2 - 2.0 \times 3 + 2.32 \times 4 + 1.16 \times 5$$
$$= -2.5 - 6.0 + 9.28 + 5.80 = 6.58\ \text{V}$$

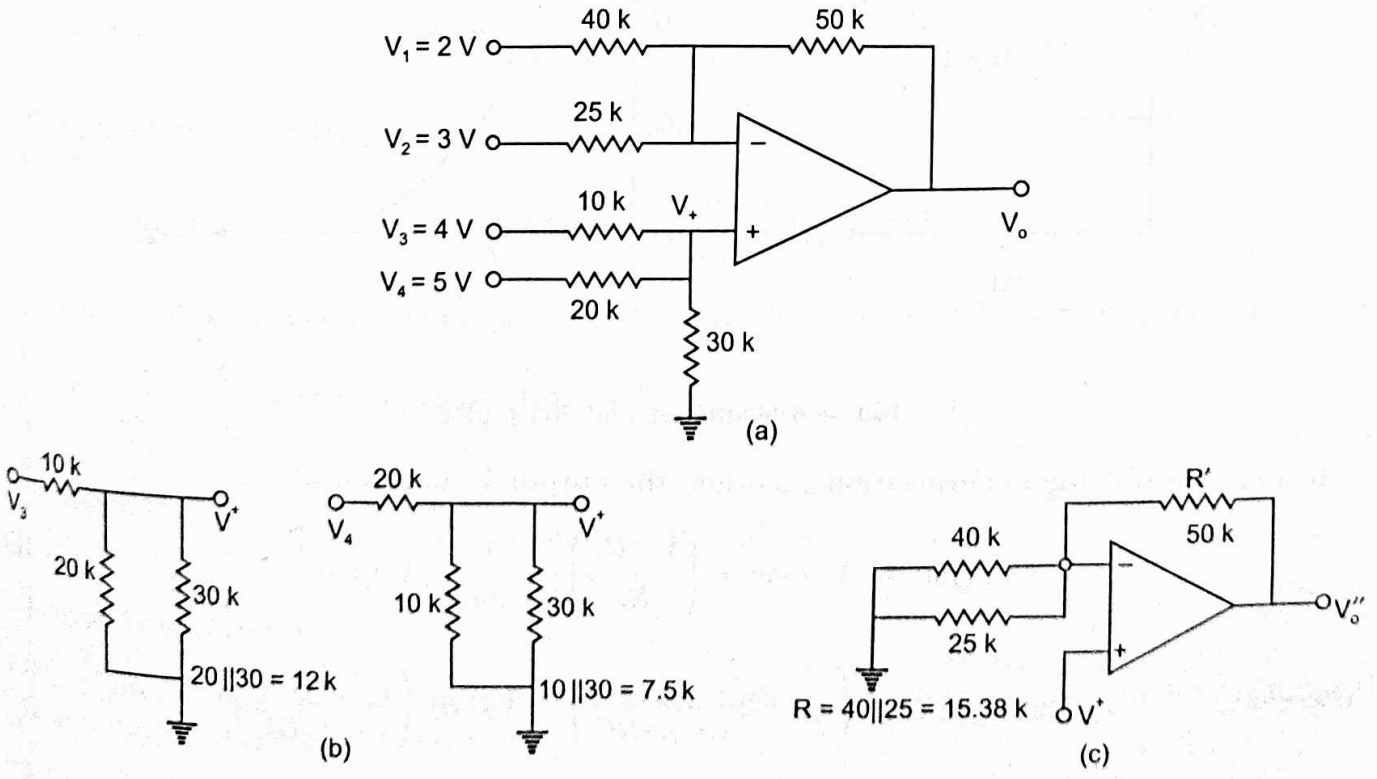


Fig. 4.4 (a) Circuit for Example 4.2 (b, c) Equivalent circuit

PHASE SHIFT CIRCUITS

The phase shift circuits produce phase shifts that depend on the frequency and maintain a constant gain. These circuits are also called *constant-delay filters* or *all-pass filters*. The constant delay refers to the fact that the time difference between input and output remains constant when frequency is changed over a range of operating frequencies. This is called all-pass because normally a constant gain is maintained for all the frequencies within the operating range. The two types of circuits, for lagging phase angles and leading phase angles are discussed below.

Phase-Lag Circuit

Fig 4.5 shows a phase-lag circuit using an op-amp. The input voltage v_i drives a simple inverting amplifier with inverting input applied at (–) terminal of op-amp and a non-inverting amplifier with a low-pass filter. The inverting gain is –1 and non-inverting gain after the low-pass circuit is $1 + \frac{R_f}{R_1} = 1 + 1 = 2$, since $R_f = R_1$.

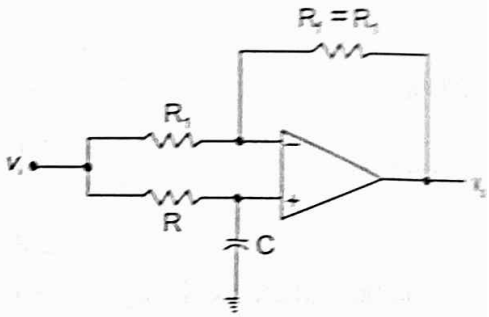


Fig. 4.5 Phase-lag circuit

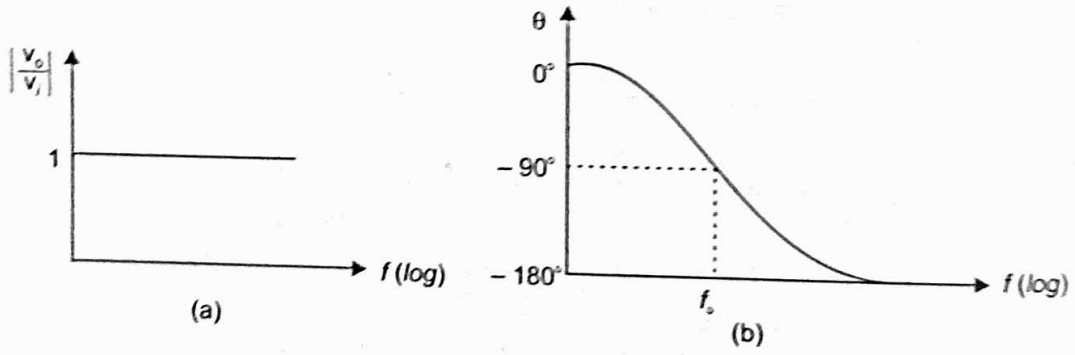


Fig. 4.6 Magnitude and Phase plot

In Fig. 4.6(a) using superposition theorem, the output V_o is given by

$$V_o(j\omega) = -V_i(j\omega) + \left(\frac{1 + R_f}{R_1}\right)\frac{1}{1 + j\omega RC}V_i(j\omega) \qquad (4.16)$$

Therefore, $$V_o(j\omega) = V_i(j\omega)\left(-1 + 2\frac{1}{1 + j\omega RC}\right) = V_i(j\omega)\left(\frac{1 - j\omega RC}{1 + j\omega RC}\right)$$

The relationship between output and input can be expressed by

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \left(\frac{1 - j\omega RC}{1 + j\omega RC}\right) \tag{4.17}$$

Since the numerator and denominator are complex conjugates, their magnitudes are identical. The phase angle is given by

$$\theta = -\tan^{-1}(\omega RC) - \tan^{-1}(\omega RC) = -2\tan^{-1}(\omega RC) \tag{4.18}$$

For $\omega = 0$, the phase angle approaches zero. When $\omega = \infty$, the phase angle approaches $-180°$. Equation (4.18) can be written as

$$\theta = -2\tan^{-1}(f/f_o) \tag{4.19}$$

where the frequency f_o is given by

$$f_o = \frac{1}{2\pi RC} \tag{4.20}$$

It can be seen that for $f = f_o$ in the phase angle $\theta = -90°$. The magnitude and phase for the phase-lag circuit is shown in Fig. 4.6(a) and (b) respectively.

Example 4.3

Determine the phase angle and the time delay for the circuit shown in Fig 4.5 for a frequency of 2kHz, assuming $R_1 = 20k\Omega$, $R = 39k\Omega$, $R_f = R_1$ and C = 1nF.

Solution

The circuit is a phase-lag network

Therefore, $$f_o = \frac{1}{2\pi RC} = \frac{1}{\left[2 \times \pi \times 39 \times 10^3 \times 1 \times 10^{-9}\right]} = 408\,\text{Hz}$$

The phase angle for frequency of 2kHz is given by

$$\theta = -2\tan^{-1}\left(\frac{2 \times 10^3}{4081}\right) = -52.2°.$$

The phase angle is directly proportional to delay, and 360° of delay corresponds to one period

i.e., $\frac{\theta}{360°} = \frac{t_d}{T}$ where, t_d is the time delay.

Therefore, $$t_d = \frac{1}{f}\frac{\theta}{360°} = \frac{1}{2 \times 10^3}\frac{-52.2}{360°} = 72.5\mu s$$

Phase-Lead Circuit

The phase-lead circuit is shown in Fig 4.7(a) in which the RC circuit forms a high-pass network. The output voltage is expressed as

$$V_o(j\omega) = -V_i(j\omega) + 2\left(\frac{j\omega RC}{1+j\omega RC}\right)V_i(j\omega)$$

Therefore, $$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-1+j\omega RC}{1+j\omega RC} \quad (4.21)$$

Equation (4.21) shows that the ratio of magnitude is constant and overall phase is given by

$$\theta = 180° - \tan^{-1}(\omega RC) - \tan^{-1}(\omega RC) = 180° - 2\tan^{-1}(\omega RC) \quad (4.22)$$

When the frequency approaches zero, the phase angle approaches 180°. As the frequency is increased, the leading phase decreases and it finally approaches zero at high frequencies. Hence, Eq. (4.22) can be written as

$$\theta = 180° - 2\tan^{-1}(f/f_o) \quad (4.23)$$

where $f_o = \dfrac{1}{2\pi RC}$. Figure 4.7(b) shows the magnitude and phase plots for the phase-lead circuit

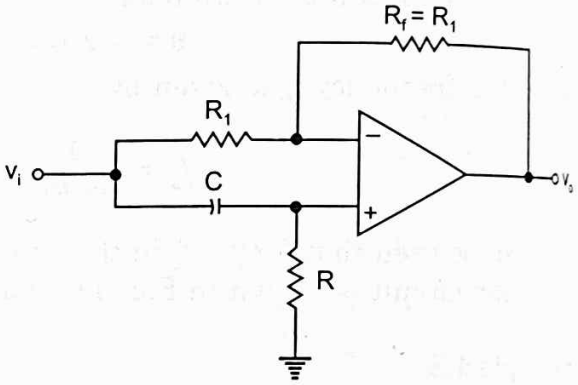
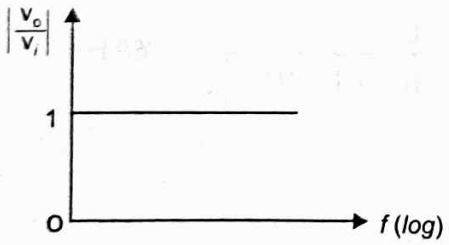


Fig. 4.7 (a) Phase-lead circuit



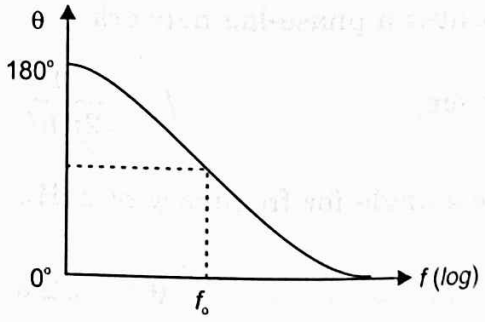


Fig. 4.7 (b) Magnitude and phase for the phase-lead circuit

4.3 INSTRUMENTATION AMPLIFIER

In a number of industrial and consumer applications, one is required to measure and control physical quantities. Some typical examples are measurement and control of temperature, humidity, light intensity, water flow etc. These physical quantities are usually measured with the help of transducers. The output of transducer has to be amplified so that it can drive the indicator or display system. This function is performed by an instrumentation amplifier. The important features of an instrumentation amplifier are:

(i) high gain accuracy
(ii) high CMRR

(iii) high gain stability with low temperature coefficient
(iv) low dc offset
(v) low output impedance

There are specially designed op-amps such as μA725 to meet the above stated requirements of a good instrumentation amplifier. Monolithic (single chip) instrumentation amplifier are also available commercially such as AD521, AD524, AD620, AD624 by Analog Devices, LM-363.XX (XX→10,100,500) by National Semiconductor and INA101,104, 3626, 3629 by Burr-Brown.

Consider the basic differential amplifier as shown in Fig. 4.8 (a). It can be easily seen that the output voltage V_o is given by,

$$V_o = -\frac{R_2}{R_1}V_2 + \frac{1}{1+\frac{R_3}{R_4}}V_1\left(1+\frac{R_2}{R_1}\right) \quad \left[V^+ = \frac{R_4}{R_3+R_4}V_1\right]$$

or,

$$V_o = -\frac{R_2}{R_1}\left[V_2 - \frac{1}{1+\frac{R_3}{R_4}}\left(\frac{R_1}{R_2}+1\right)V_1\right] \tag{4.24}$$

For $R_1/R_2 = R_3/R_4$, we obtain

$$V_o = \frac{R_2}{R_1}(V_1 - V_2) \tag{4.25}$$

In the circuit of Fig. 4.8 (a), source V_1 sees an input impedance = $R_3 + R_4$ (=101 kΩ) and the impedance seen by source V_2 is only R_1 (1 kΩ). This low impedance may load the signal source heavily. Therefore, high resistance buffer is used proceeding each input to avoid this loading effect as shown in Fig. 4.8 (b).

The op-amps A_1 and A_2 have differential input voltage as zero. For $V_1 = V_2$, that is, under common mode condition, the voltage across R will be zero. As no current flows through R and R' the non-inverting amplifier A_1 acts as voltage follower, so its output $V_2' = V_2$. Similarly op-amp A_2 acts as voltage follower having output $V_1' = V_1$. However, if $V_1 \neq V_2$, current flows in R and R', and $(V_2' - V_1') > (V_2 - V_1)$. Therefore, this circuit has differential gain and CMRR more compared to the single op-amp circuit of Fig. 4.8 (a). The output voltage V_o can be calculated as follows:

The voltage at the (+) input terminal of op-amp A_3 is $\frac{R_2 V_1'}{R_1+R_2}$. Using superposition theorem, we have,

$$V_o = -\frac{R_2}{R_1}V_2' + \left(1+\frac{R_2}{R_1}\right)\left(\frac{R_2 V_1'}{R_1+R_2}\right)$$

$$= \frac{R_2}{R_1}\left(V_1' - V_2'\right) \tag{4.26}$$

Since, no current flows into op-amp, the current I flowing (upwards) in R is $I = (V_1 - V_2)/R$ and passes through the resistor R'.

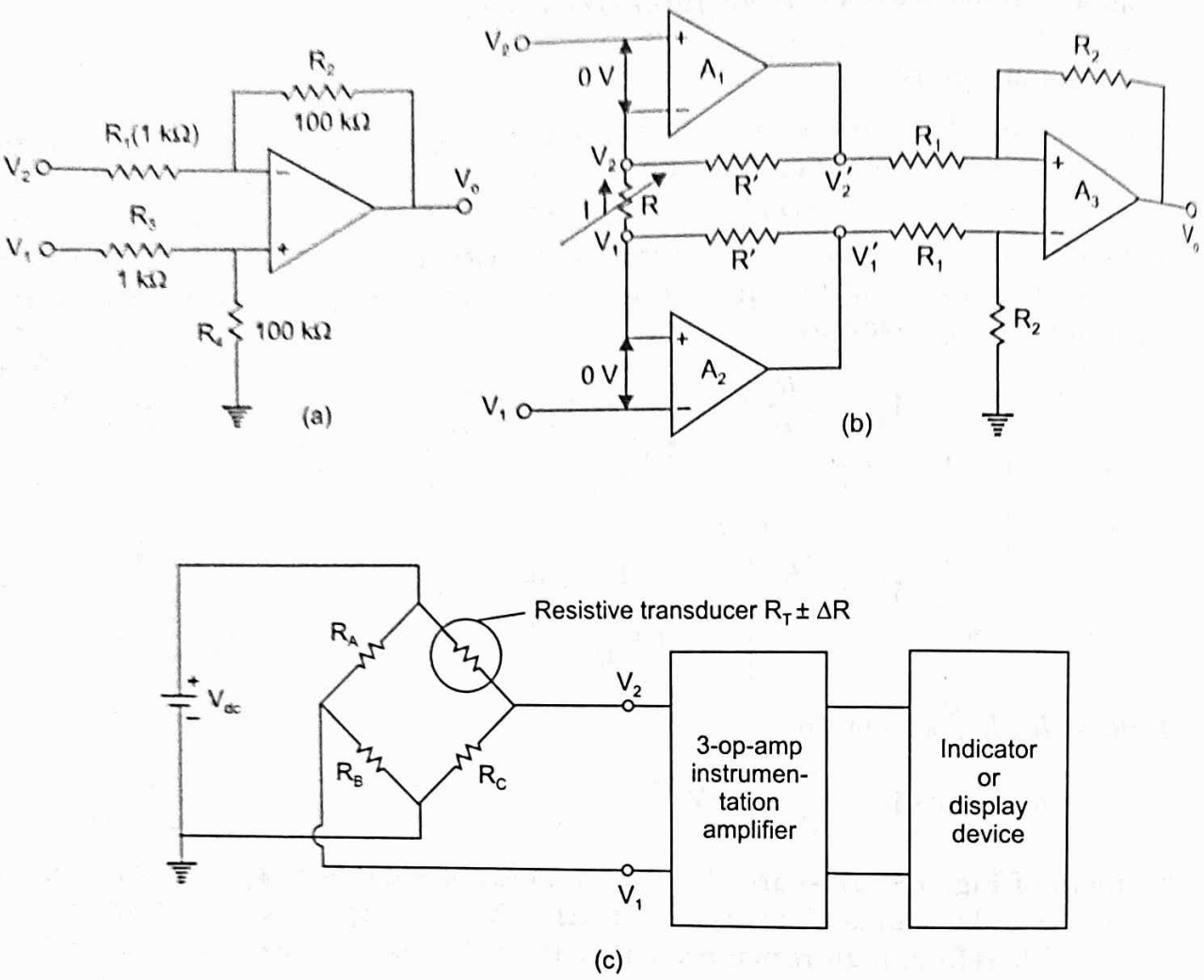


Fig. 4.8 (a) Differential amplifier using single op-amp, (b) An improved instrumentation amplifier, (c) Instrumentation amplifier using transducer bridge

$$V_1' = R'I + V_1 = \frac{R'}{R}(V_1 - V_2) + V_1 \tag{4.27}$$

and

$$V_2' = -R'I + V_2 = -\frac{R'}{R}(V_1 - V_2) + V_2 \tag{4.28}$$

Putting the values of V_1' and V_2' in Eq. (4.26), we obtain,

$$V_o = \frac{R_2}{R_1}\left[\frac{2R'}{R}(V_1 - V_2) + (V_1 - V_2)\right]$$

or,

$$V_o = \frac{R_2}{R_1}\left(1 + \frac{2R'}{R}\right)(V_1 - V_2) \tag{4.29}$$

In Eq. (4.29), if we choose $R_2 = R_1 = 25\ \text{k}\Omega$ (say) and $R' = 25\ \text{k}\Omega$; $R = 50\ \Omega$, then a gain of $\left(1+2\times\frac{25\ \text{k}\Omega}{50\ \Omega}\right) = 1001$ can be achieved. The difference gain of this instrumentation amplifier can be varied by replacing the resistance R by a potentiometer in Fig. 4.8 (b). The resistance R, however should never be made zero, as this will make the gain infinity. To avoid such a situation, in a practical circuit, a fixed resistance in series with a potentiometer is used in place of R.

Figure 4.8 (c) shows a differential instrumentation amplifier using transducer bridge. The circuit uses a resistive transducer whose resistance changes as a function of the physical quantity to be measured. The bridge is initially balanced by a dc supply voltage V_{dc} so that $V_1 = V_2$. As the physical quantity changes, the resistance R_T of the transducer also changes, causing an unbalance in the bridge ($V_1 \neq V_2$). This differential voltage now gets amplified by the three op-amp differential instrumentation amplifier.

There are a number of practical applications of instrumentation amplifier with the transducer bridge, such as temperature indicator, temperature controller, light intensity meter to name a few.

Instrumentation Amplifier IC-AD620

The pin configuration of a low cost instrumentation amplifier IC-AD620 is shown in Fig. 4.8 (d) (i). The AD620 requires only one external resistor, R_G to set gains from 1 to 1000. The relationship between gain and R_G as given by the manufacturer is

$$\text{Gain} = 1+\left(\frac{49{,}400}{R_G}\right) \tag{4.30}$$

The value of R_G required for obtaining gain values of 1, 10, 100 and 1000 are shown in Fig. 4.8 (d) (ii).

As an application of IA, consider the circuit shown in Fig. 4.8 (d) (iii), where we have to measure V_{CE} of a CE amplifier. The usual method of measuring V_{CE} will be to first measure collector voltage, V_C (w.r.t. ground), then measure emitter voltage, V_E (w.r.t. ground) and then calculate the difference. If, however, terminals C and E are connected to the input terminals of AD620 and R_G is kept open, then the gain of IA is

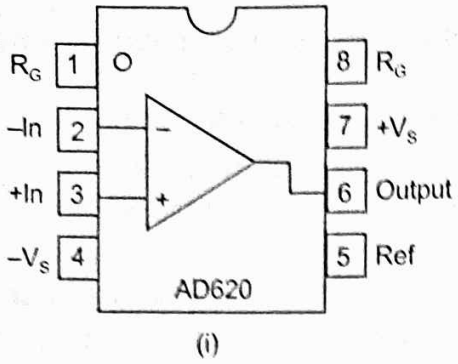
$$\text{Gain} = 1 + \frac{49{,}400}{\infty}$$

$$= 1.$$

The output voltage, V_o at pin 6 will now simply be,

$$V_o = 1(V_C - V_E)$$

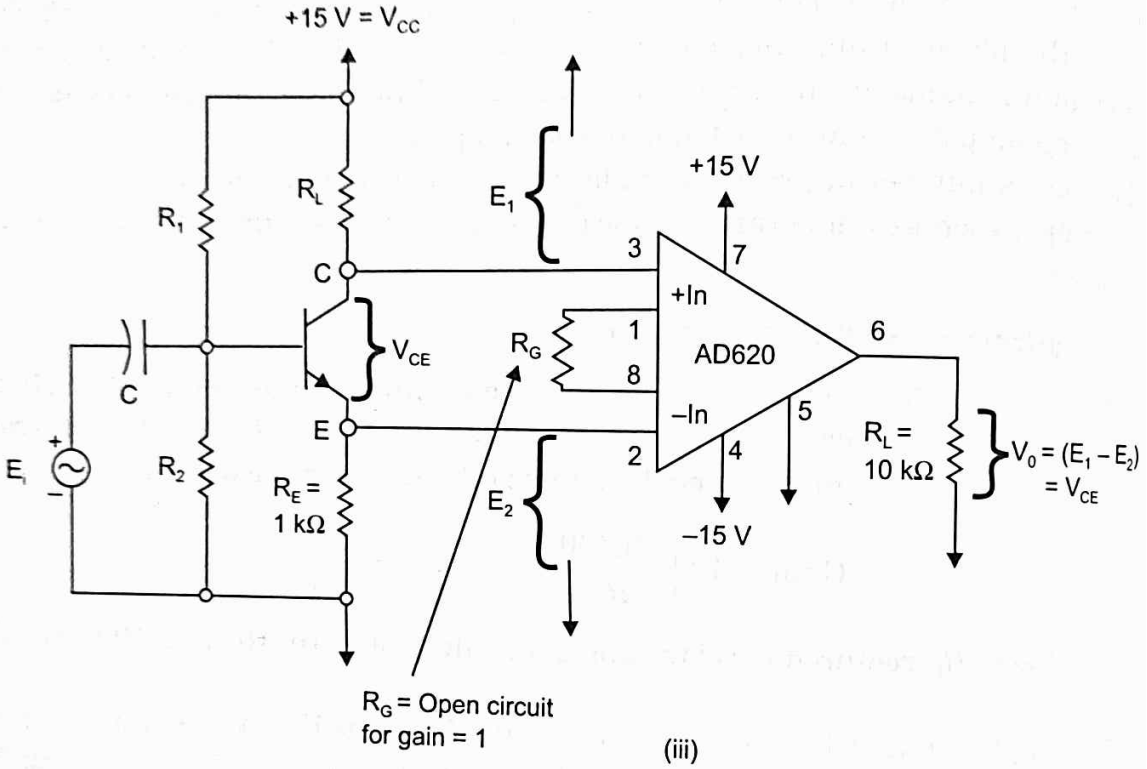
$$= V_{CE}$$



(i)

Gain	R_G
1	∞
10	5.489 kΩ
100	499 Ω
1000	49.5 Ω

(ii)



(iii)

Fig. 4.8 (d) (i) Pin configuration of AD620 (ii) Values of R_G for different gains (iii) Use of AD620 to measure a floating differential voltage

4.4 AC AMPLIFIER

The inverting and non-inverting op-amp amplifier configurations discussed earlier, respond to both ac and dc signals. However, if one wants to get the ac frequency response of an op-amp or if the ac input signal is superimposed with dc level, it becomes essential to block the dc component. This is achieved by using an AC amplifier with a coupling capacitor. AC amplifiers are of inverting and non-inverting type.

Inverting AC Amplifier

The circuit is shown in Fig. 4.9 (a). The capacitor C blocks the dc component of the input and together with the resistor R_1 sets the lower 3 dB frequency of the amplifier.

Since node 'a' is at virtual ground, the output voltage V_o (as a function of complex variables) is given by,

$$V_o = -IR_f = \frac{V_i}{R_1 + 1/sC} R_f \tag{4.31}$$

Therefore,

$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1} \frac{s}{s + 1/R_1C} \tag{4.32}$$

It is seen from Eq. (4.32) that the lower 3dB frequency is,

$$f_L = \frac{1}{2\pi R_1 C} \tag{4.33}$$

In the mid-band range of frequencies, capacitor C behaves as a short circuit and therefore, Eq. (4.32) becomes,

$$A_{CL} \approx -\frac{R_f}{R_1} \tag{4.34}$$

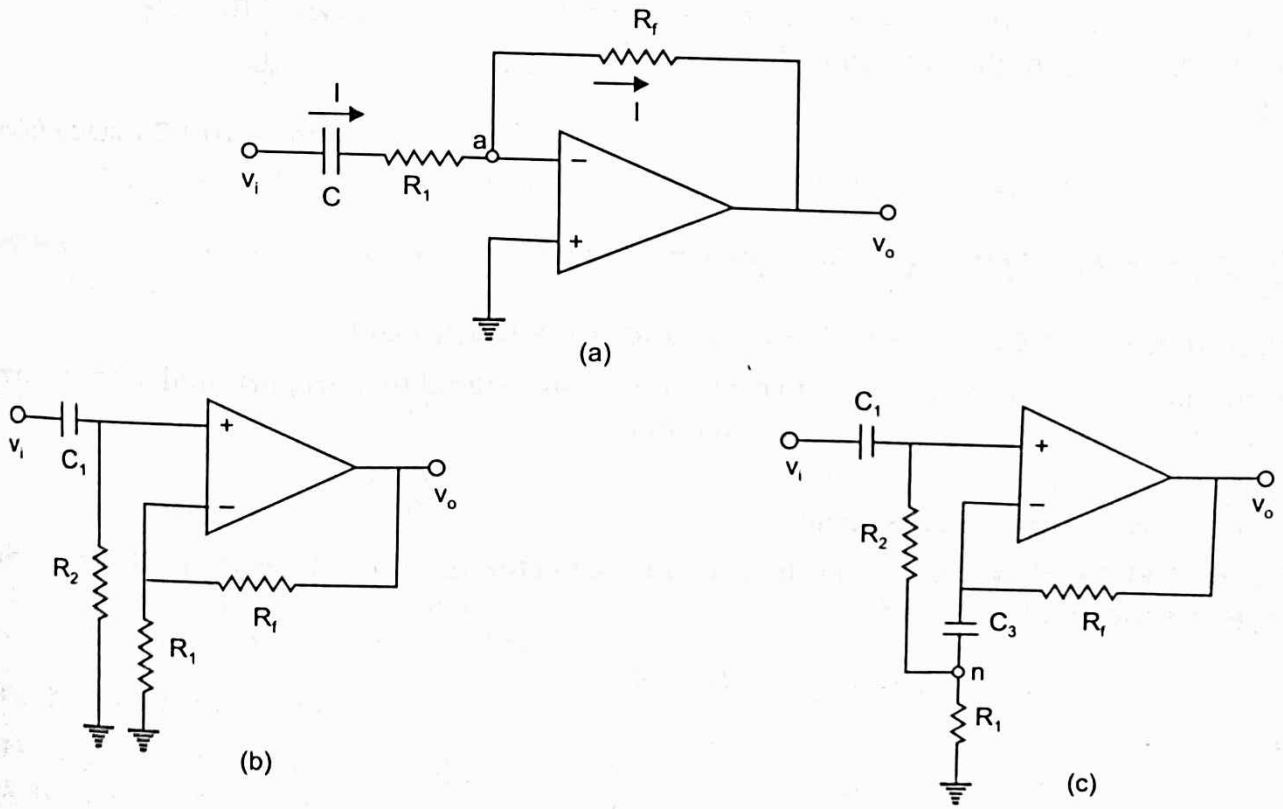


Fig. 4.9 (a) Inverting ac amplifier, (b) Non-inverting ac amplifier, (c) High input impedance non-inverting ac amplifier

Non-inverting AC Amplifier

The circuit is shown in Fig. 4.9 (b). Here a resistor R_2 is added to provide a dc return to ground. However, this reduces the overall input impedance of the amplifier, which now becomes approximately R_2. This problem of low input impedance is eliminated by connecting a capacitor C_3 as in Fig. 4.9 (c). Capacitor C_3 is large enough to act as short circuit to ac signals. The non-inverting terminal and the node 'n' will be almost at the same potential so that R_2 carries almost no current. Hence the circuit will have an extremely high input impedance.

AC Voltage Follower

The circuit of a practical ac voltage follower is shown in Fig. 4.10. The circuit is used as a buffer to connect a high impedance signal source to a low impedance load which may even be capacitive. The capacitor C_1 and C_2 are chosen high so that they are short circuit at all frequencies of operation. Resistors R_1 and R_2 provide a path for dc input current into the non-inverting terminal. C_2 acts as a bootstrapping capacitor and connects the resistance R_1 to the output terminal for ac operation. Hence the input resistance that the source sees is approximately $R_1/(1 - A_{CL})$ [from Miller's theorem], where A_{CL} is the gain of the voltage follower which is close to unity (0.9997). Thus very high input impedance can be obtained.

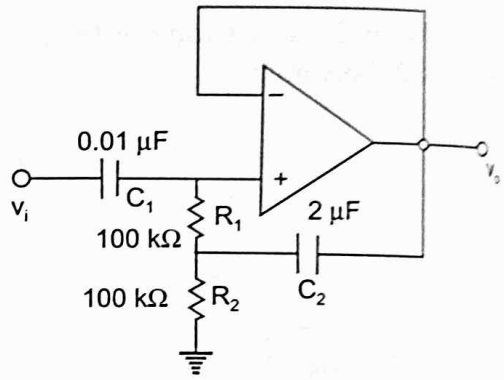


Fig. 4.10 AC voltage follower

4.5 V TO I AND I TO V CONVERTER

Voltage to Current Converter (Transconductance Amplifier)

In many applications, one may have to convert a voltage signal to a proportional output current. For this, there are two types of circuits possible:

V-I Converter with floating load
V-I Converter with grounded load

Figure 4.11 (a) shows a voltage to current converter in which load Z_L is floating. Since voltage at node 'a' is v_i, therefore,

$$v_i = i_L R_1 \text{ (as } I_B^- = 0)$$

or,
$$i_L = \frac{v_i}{R_1} \tag{4.35}$$

That is the input voltage v_i is converted into an output current of v_i/R_1. It may be seen that the same current flows through the signal source and load and, therefore, signal source should be capable of providing this load current.

A voltage-to-current converter with grounded load is shown in Fig. 4.11 (b). Let v_1 be the voltage at node 'a'. Writing KVL, we get

$$i_1 + i_2 = i_L \tag{4.36}$$

$$\frac{v_i - v_1}{R} + \frac{v_o - v_1}{R} = i_L$$

or,

$$v_i + v_o - 2v_1 = i_L R$$

or,

Therefore,

$$v_1 = \frac{v_i + v_o - i_L R}{2} \tag{4.37}$$

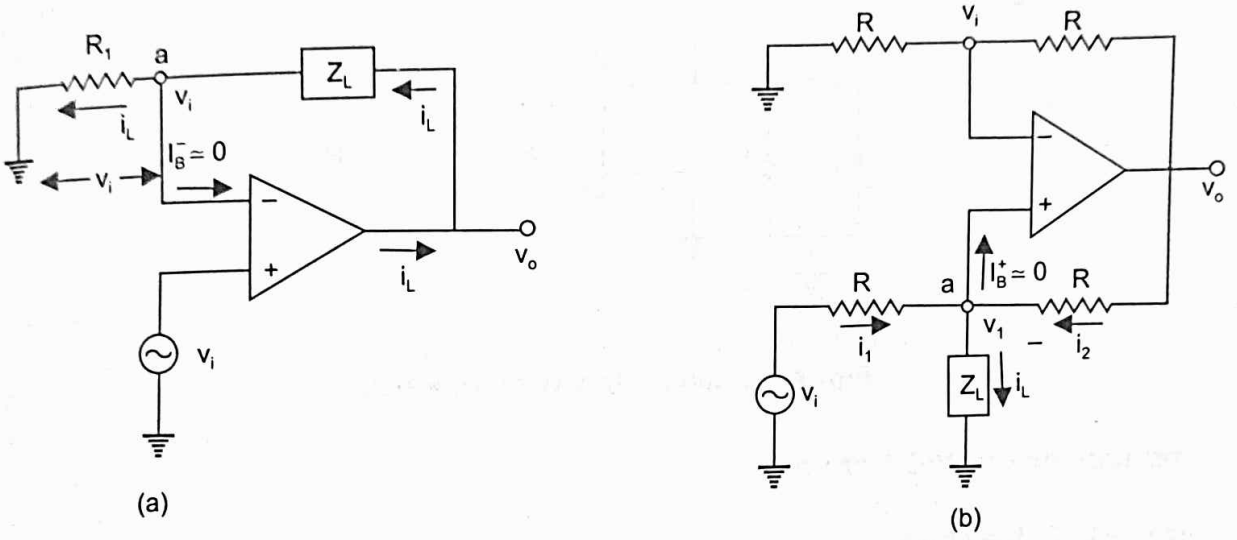


Fig. 4.11 Voltage to current converter with (a) Floating load, (b) Grounded load

Since the op-amp is used in non-inverting mode, the gain of the circuit is $1 + R/R = 2$. The output voltage is,

$$v_o = 2v_1 = v_i + v_o - i_L R$$

that is,

$$v_i = i_L R$$

or,

$$i_L = \frac{v_i}{R} \tag{4.38}$$

As the input impedance of a non-inverting amplifier is very high, this circuit has the advantage of drawing very little current from the source. A voltage to current converter is used for low voltage dc and ac voltmeter, LED and zener diode tester.

Current to Voltage Converter (Transresistance Amplifier)

Photocell, photodiode and photovoltaic cell give an output current that is proportional to an incident radiant energy or light. The current through these devices can be converted to voltage by using a current-to-voltage converter and thereby the amount of light or radiant energy incident on the photo-device can be measured.

Figure 4.9 shows an op-amp used as I to V converter. Since the (–) input terminal is at virtual ground, no current flows through R_s and current i_s flows through the feedback resistor R_f. Thus the output voltage $v_o = -i_s R_f$. It may be pointed out that the lowest current that this circuit can measure will depend upon the bias current I_B of the op-amp. This means that μA741

(I_B = 3 nA) can be used to detect lower currents. The resistor R_f is sometimes shunted with a capacitor C_f to reduce high frequency noise and the possibility of oscillations.

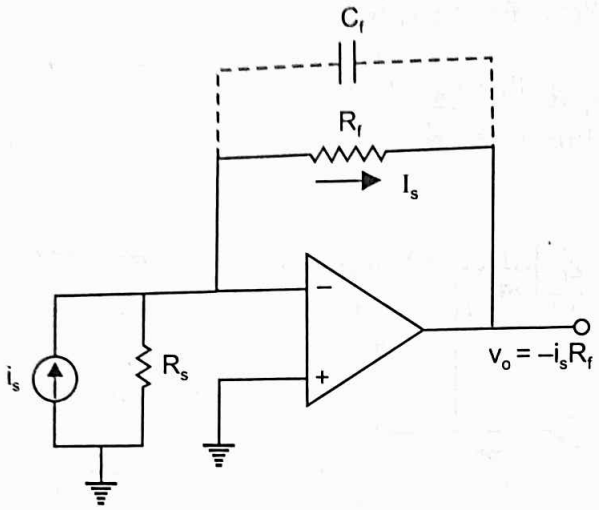


Fig. 4.12 Current to voltage converter

4.5.1 Applications of V-I Converter

Low Voltage D.C. Voltmeter

The V-I converter circuit with floating load can be modified to a low voltage d.c. voltmeter circuit. The resistance R_L is replaced by *D'*Arsonval meter as shown in Fig 4.13.

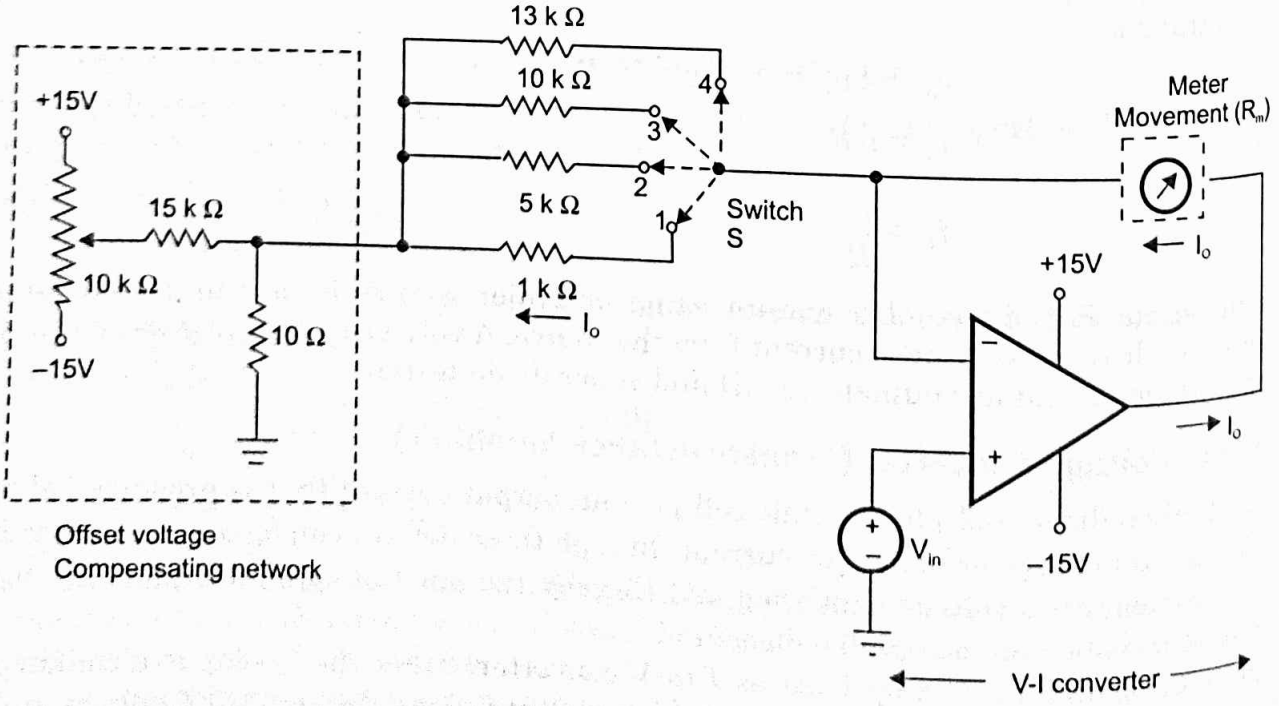


Fig. 4.13 D.C. voltmeter

For accurate readings it is necessary to make the nulling of op-amp. This is done by offset voltage compensating network. The effective Thevenin's equivalent of compensating network is 10 Ω. Hence when switch S is in position 1, the effective R_1 is 1 kΩ + 10 Ω ≈ 1 kΩ.

If $V_{in} = 1$ V then,

$$I_o = \frac{V_{in}}{R_1} \simeq \frac{1\,V}{1\,k\Omega} = 1 \text{ mA}$$

So, if meter has full scale deflection current of 1mA, then for input of IV, the current reading will be 1V.

When switch is in position 2 then $R_1 = 5$ kΩ. Thus, for full scale deflection,

$$1 \times 10^{-3} = \frac{V_{in}}{5 \times 10^3}$$

$$\therefore \quad V_{in} = 5 \text{ V}$$

Thus 5 V are required to cause full scale deflection: The range of voltmeter increases by 5. Similarly at positions 3 and 4, ranges of 10 and 13 can be obtained.

Remember that for ±15 V supply, maximum input voltage range is ±14 V, hence with ±15V supply, maximum range possible is 13.

It is important to note that meter resistance R_m does not affect the value of I_o. Thus meter can be calibrated properly to measure d.c. voltages.

Low Voltage A.C. Voltmeter

To measure a.c. voltages, the full wave bridge rectifier and D'Arsonval meter is used. The combination of mater and rectifier is used in the feedback loop of a.c. voltmeter. The circuit is shown in Fig 4.14.

The alternating current I_o is converted to d.c. During positive half cycle of V_{in} the diodes D_3 and D_4 conduct while for negative half cycle of V_{in} the diodes D_1 and D_2 conduct. The direction of current through meter is always same for both the half cycles of V_{in}. Thus meter gives the average (d.c.) value of the rectified current. If it is necessary to calibrate the meter in terms of r.m.s. values of input voltage then the factor 1.11 must be considered which relates r.m.s. and average values for purely sinusoidal waveforms. The range can be extended using the selector switch S and various resistances as shown in Fig 4.14. At position 2, X2 can be obtained. At position 3, X5 range can be obtained. At position 4, X10 range can be obtained. It must be noted that due to low slew rate of 741 op-amp, the input a.c. voltage frequency should not be greater than 4 kHz. Similarly PIV ratings of the diodes must be greater than the saturation voltages of op-amp.

Diode Tester and Match Finder

Another applications of V-I converter is a diode tester and diode match finder. The resistance R_L is replaced by a diode as shown in the Fig 4.15.

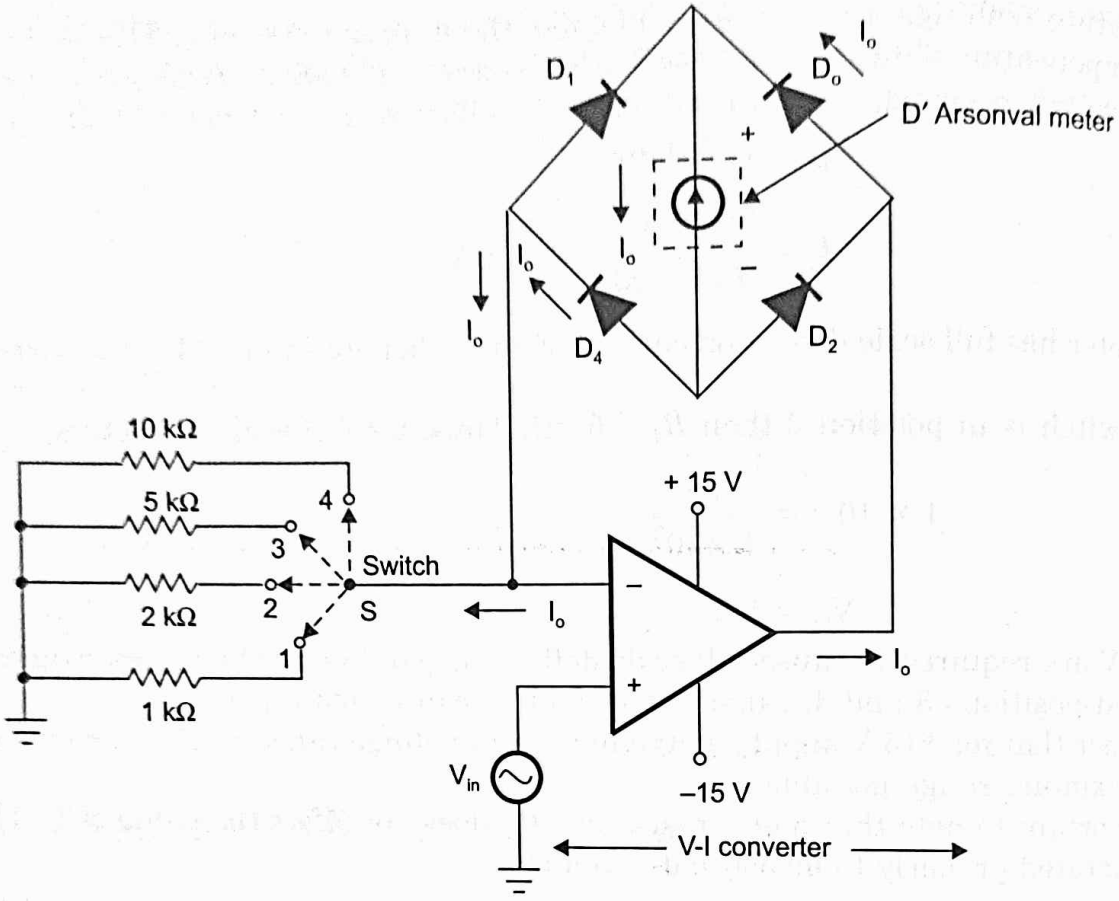


Fig. 4.14 A.C. voltmeter

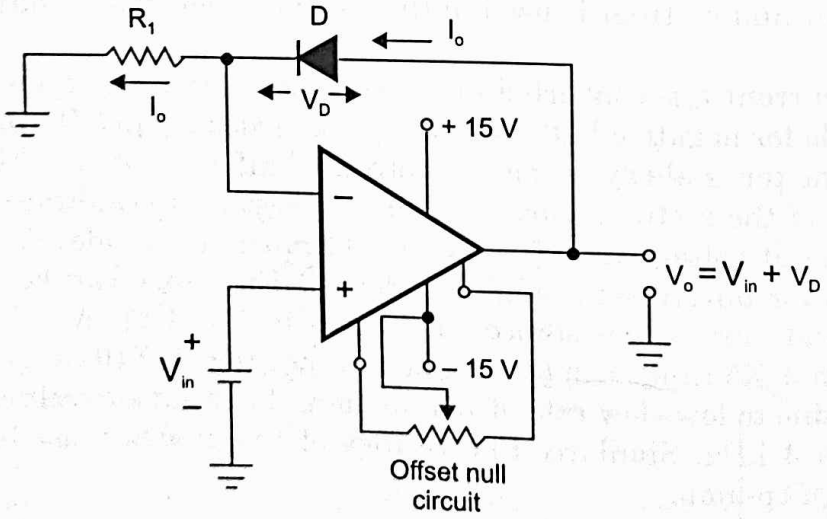


Fig. 4.15 Diode tester and match finder

The current I_o is set by V_{in} and resistnce R_1.

$$I_o = \frac{V_{in}}{R_1}$$

As long as V_{in} and R_1 are constant, the current I_o is also constant. The drop across diode can be directly measured by the voltmeter or the output voltage will be $V_o = V_{in} + V_D$. From the value of V_D, the diode can be judged for its performance. Note that to avoid error in the output voltage, op-amp should be initially nulled using offset null circuit.

Similarly replacing diodes one after the other, the perfectly matched diodes can be found out. R_1 can be selected according to V_{in} and testing current I_o required in the circuit.

Zener Diode Tester

The V-I converter circuit can also be used to test zener diode. The zener diode is connected in reverse biased condition in the feedback path as shown in Fig. 4.16.

The current I_o is set by V_{in} and R_1. If this current is more than knee current of the zener then voltage across zener is V_Z for which it is rated. Similarly matched zeners also can be obtained using same circuit.

The same circuit can be used for LED testing and match finding by replacing the feedback path by LED under test. The brightness of LEDS can be tested by setting specific current using V_{in} and R_1.

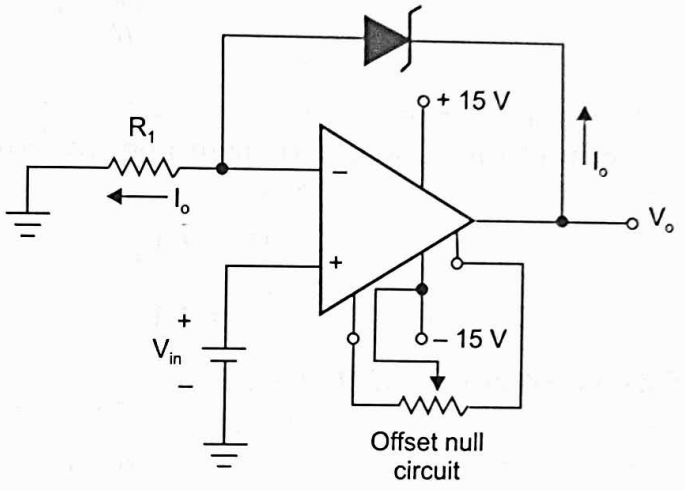


Fig. 4.16 Zener diode tester

In all the applications, as 741 is used it is necessary to note that short circuit current rating of op-amp i.e. 25 mA should not be exceeded by the current I_o.

Example 4.4

For a V-I convertor shown in Fig. 4.17 V_{in} = 5 V, R = 10 kΩ, V_1 = 1V, find the load current and output voltage V_o. Assume the op-amp is initially nulled.

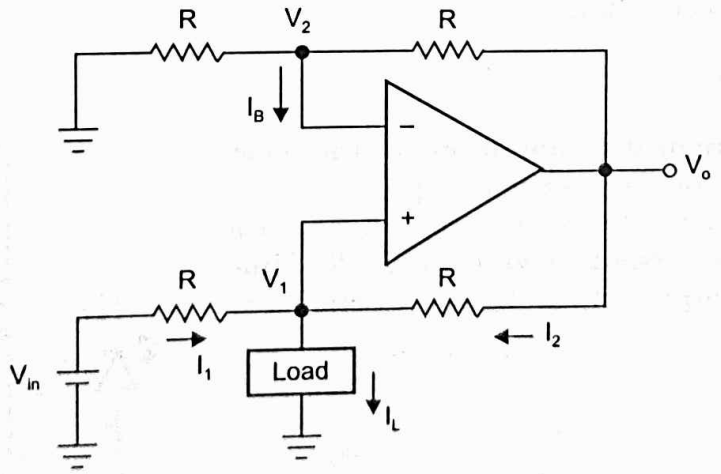


Fig. 4.17

Solution

Assume $I_R = 0A$

$$I_L = I_1 + I_2 = \frac{V_{in} - V_1}{R} + \frac{V_o - V_1}{R}$$

$$\therefore \quad \frac{V_{in} + V_o - 2V_1}{R} = I_L \qquad (4.39)$$

The gain of the op-amp circuit in non inverting mode is $A = 1 + \frac{R}{R} = 2$.

$$\therefore \quad V_o = 2\ V_1$$

$$= 2\ V$$

Further, from Eq. (4.39), we get

$$I_L = \frac{5 + 2 - 2}{10 \times 10^3}$$

$$= 0.5\ \text{mA}$$

Applications of I/V Converter

One of the most frequent applications if I/V converters is in connection with current type photodetectors such as photodiodes, photoFETs and photo multipliers. Another common application is I/V conversion of current output in a digital to analog converter. In this section we discuss two applications of I/V converters.

Photodiode Detector

Fig 4.18 shows the circuit diagram of one of the most widely used photodetectors i.e. a photodiode.

The photodiode produces electrical current in response to incident light. This current flows through R. Thus voltage across R, the output voltage V_o is proportional to the diode current.

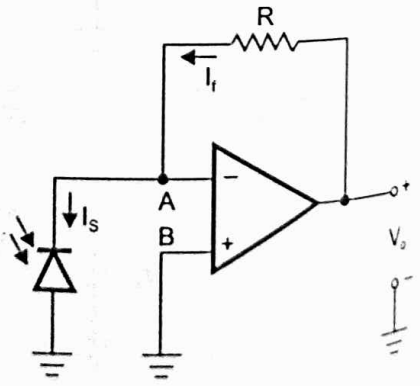


Fig. 4.18 Photodiode as a photodetector

photoFET Detector

Fig 4.19 shows another photodetector circuit with photoFET.

The PhotoFET is similar to a conventional JFET, with the exception of a lens for focusing light on the gate junction. When light falls then photons enter the gate area and excite valance electrons into the conduction band. The photon-excited current carriers cause a small current ΔI_G resulting in large current change ΔI_D. The change in I_D results in a change in the voltage drop across R and hence the output voltage. Therefore, the op-amp circuit acts as an I/V converter and gives the indication of light in terms of voltage.

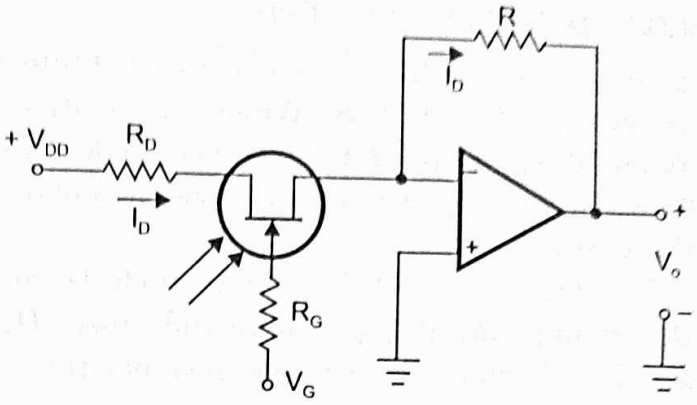


Fig. 4.19 Photodetector circuit with photoFET

4.6 OP-AMP CIRCUITS USING DIODES

The major limitation of ordinary diode is that it cannot rectify voltages below V_γ (~0.6 V), the cut-in voltage of the diode. A circuit that acts like an ideal diode can be designed by placing a diode in the feedback loop of an op-amp as in Fig. 4.20 (a). Here the cut-in voltage is divided by the open loop gain A_{OL} (~10^4) of the op-amp so that V_γ is virtually eliminated. When the input $v_i > V_\gamma/A_{OL}$ then v_{oA}, the output of the op-amp exceeds V_γ and the diode D conducts. Thus the circuit acts like a voltage follower for input $v_i > V_\gamma/A_{OL}$ (*i.e.*, $0.6/10^4 = 60\ \mu V$) and the output v_o follows the input voltage v_i during the positive half cycle as shown in Fig. 4.20 (b). When v_i is negative or less than V_γ/A_{OL}, the diode D is ***off*** and no current is delivered to the load R_L except for small bias current of the op-amp and the reverse saturation current of the diode. This circuit is called the ***precision diode*** and is capable of rectifying input signals of the order of millivolt. Some typical applications of a precision diode discussed are:

Half-wave rectifier
Full-wave rectifier
Peak-value detector
Clipper
Clamper

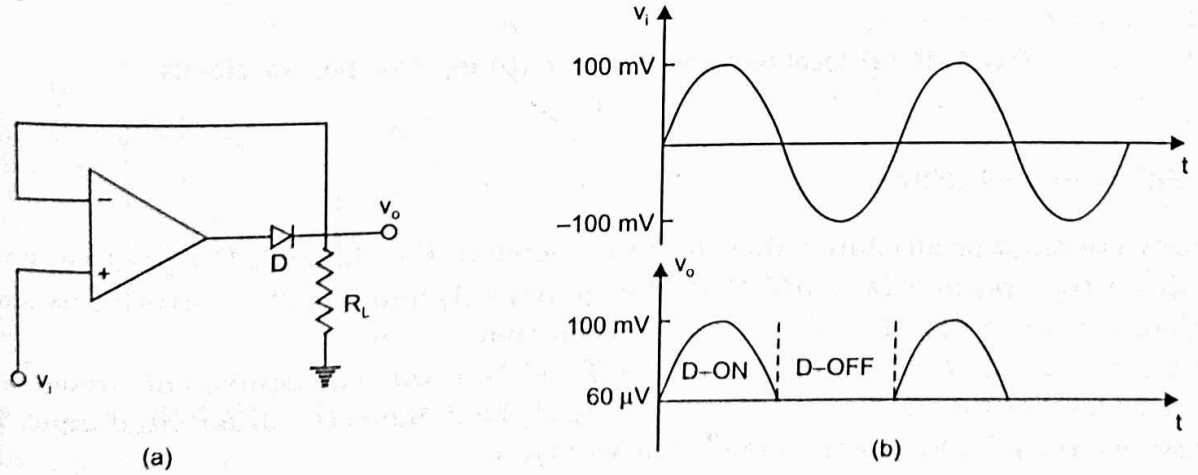


Fig. 4.20 (a) Precision diode, (b) Input and output waveforms

4.6.1 Half-Wave Rectifier

An inverting amplifier can be converted into an ideal half-wave rectifier by adding two diodes as shown in Fig. 4.21 (a). When v_i is positive, diode D_1 conducts causing v_{OA} to go to negative by one diode drop (~0.6 V). Hence diode D_2 is reverse biased. The output voltage v_o is zero, because, for all practical purposes, no current flows through R_f and the input current flows through D_1.

For negative input, *i.e.*, $v_i < 0$, diode D_2 conducts and D_1 is ***off***. The negative input v_i forces the op-amp output v_{OA} positive and causes D_2 to conduct. The circuit then acts like an inverter for $R_f = R_1$ and output v_o becomes positive.

The input, output waveforms are shown in Fig. 4.21 (b). The op-amp in the circuit of Fig. 4.21 (a) must be a high speed op-amp since it alternates between open loop and closed loop operations. The principal limitation of this circuit is the slew rate of the op-amp. As the input passes through zero, the op-amp output v_{oA} must change from 0.6 V to –0.6 V or vice-versa as quickly as possible in order to switch over the conduction from one diode to the other. The circuit of Fig. 4.21 (a) provides a positive ouput. However, if both the diodes are reversed, then only positive input signal is transmitted and gets inverted. The circuit, then provides a negative output.

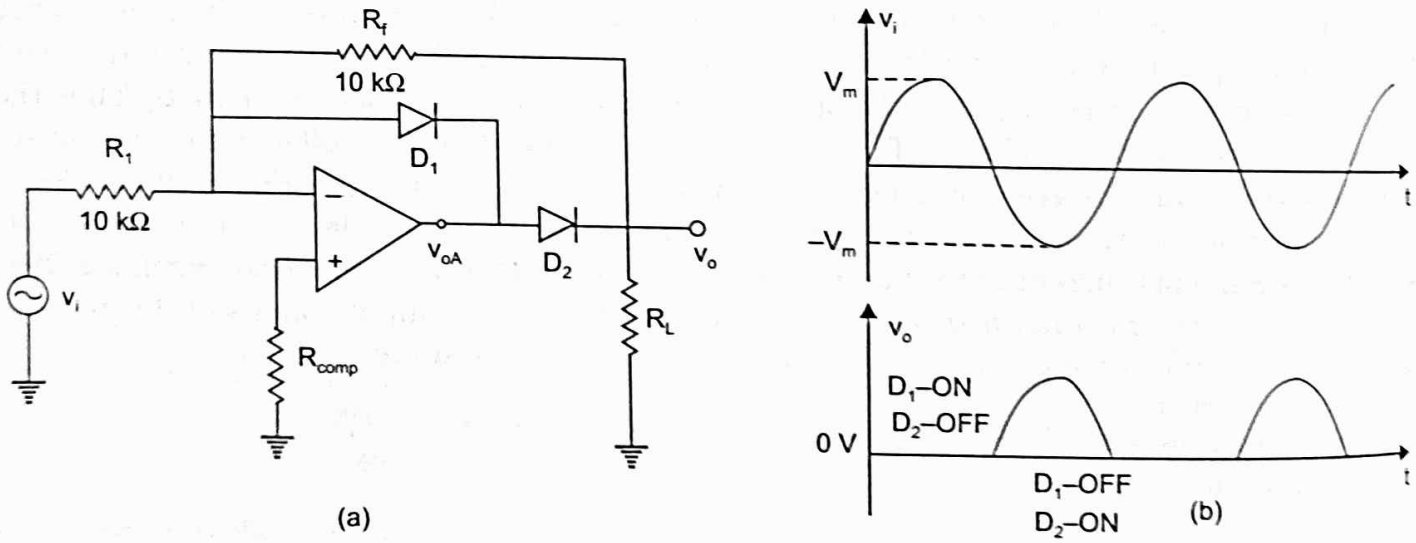


Fig. 4.21 (a) Ideal half-wave rectifier, (b) Input/output waveforms

4.6.2 Full-Wave Rectifier

A full-wave rectifier or absolute value circuit is shown in Fig. 4.22 (a). For positive input, *i.e.*, $v_i > 0$, diode D_1 is ***on*** and D_2 is ***off***. Both the op-amps A_1 and A_2 act as inverter as shown in equivalent circuit in Fig. 4.22 (b). It can be seen that $v_o = v_i$.

For negative input, *i.e.*, $v_i < 0$, diode D_1 is ***off*** and D_2 is ***on***. The equivalent circuit is shown in Fig. 4.22 (c). Let the output voltage of op-amp A_1 be v. Since the differential input to A_2 is zero, the inverting input terminal is also at voltage v.

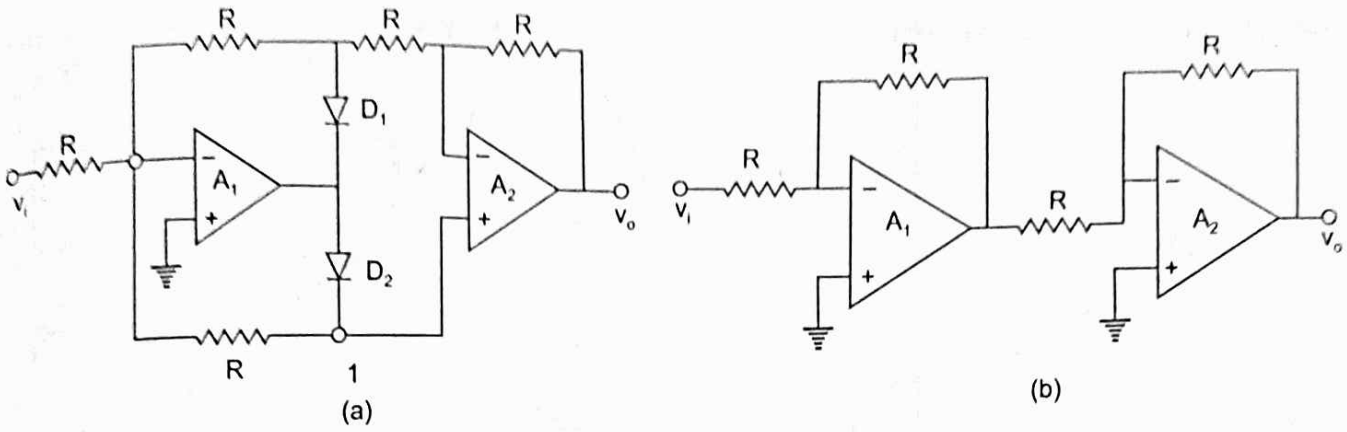


Fig. 4.22 (a) Precision full wave rectifier, (b) Equivalent circuit for $v_i > 0$; D_1 is on and D_2 is OFF; op-amp A_1 and A_2 operate as inverting amplifier

KCL at node 'a' gives

$$\frac{v_i}{R} + \frac{v}{2R} + \frac{v}{R} = 0$$

or

$$v = -\frac{2}{3} v_i \tag{4.40}$$

The equivalent circuit of Fig. 4.22 (c) is a non-inverting amplifier as shown in Fig. 4.22 (d). The output v_o is,

$$v_o = \left(1 + \frac{R}{2R}\right)\left(-\frac{2}{3} v_i\right) = v_i \tag{4.41}$$

Hence for $v_i < 0$, the output is positive. The input and output waveforms are shown in Fig. 4.22 (e). The circuit is also called an absolute value circuit as output is positive even when input is negative. For example, the absolute value of $|+2|$ and $|-2|$ is $+2$ only. It is possible to obtain negative outputs for either polarity of input simply by reversing the diodes.

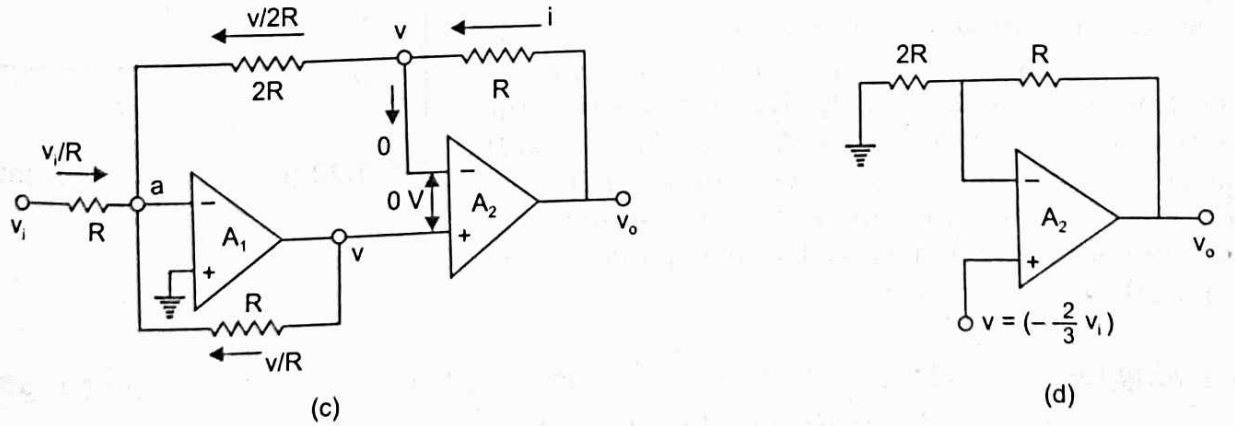


Fig. 4.22 (c) Equivalent circuit for $v_i < 0$, (d) Equivalent circuit of (c)

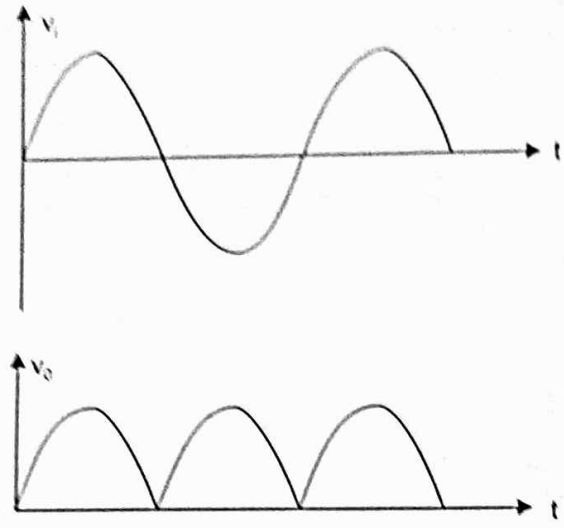


Fig. 4.22 (e) Input and output waveforms

4.6.3 Peak Detector

The function of a peak detector is to compute the peak value of the input. The circuit follows the voltage peaks of a signal and stores the highest value (almost indefinitely) on a capacitor. If a higher peak signal value comes along, this new value is stored. The highest peak value is stored until the capacitor is discharged.

Consider the circuit of Fig. 4.23 (a). When input v_i exceeds v_c, the voltage across the capacitor, the diode D is forward biased and the circuit becomes a voltage follower. Consequently, the output voltage v_o follows v_i as long as v_i exceeds v_c. When v_i drops below v_c, the diode becomes reverse-biased and the capacitor holds the charge till input voltage again attains a value greater than v_c. Figure 4.23 (b) shows the voltage waveshape for the positive peak detector. It may be noted that the peak at time t' is missed, the reason is obvious. The circuit can be reset, that is, capacitor voltage can be made zero by connecting a low leakage MOSFET switch across the capacitor. The circuit can be modified to hold the lowest or most negative voltage of a signal by reversing the diode. Peak detectors find application in test and measurement instrumentation as well as in amplitude modulation (AM) communication.

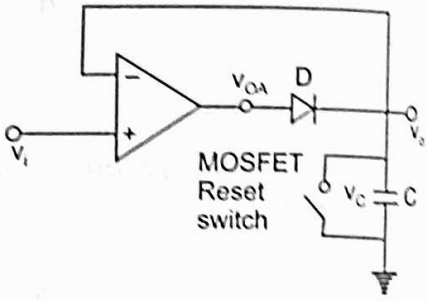


Fig. 4.23 (a) Positive peak detector

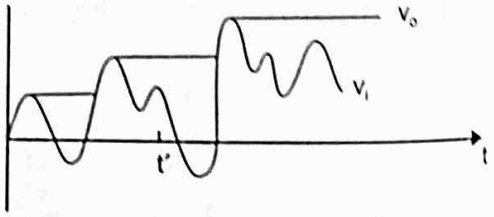


Fig. 4.23 (b) Output v_o corresponding to arbitrary input v_i

4.6.4 Clipper

A precision diode may also be used to clip-off a certain portion of the input signal to obtain a desired output waveform.

Figure 4.24 (a) shows a positive clipper. The clipping level is determined by the reference voltage V_{ref} and could be obtained from the positive supply voltage V^+. The input and output

waveforms are shown in Fig. 4.24 (b). It can be seen that the portion of the output voltage for $v_o > V_{ref}$ are clipped off.

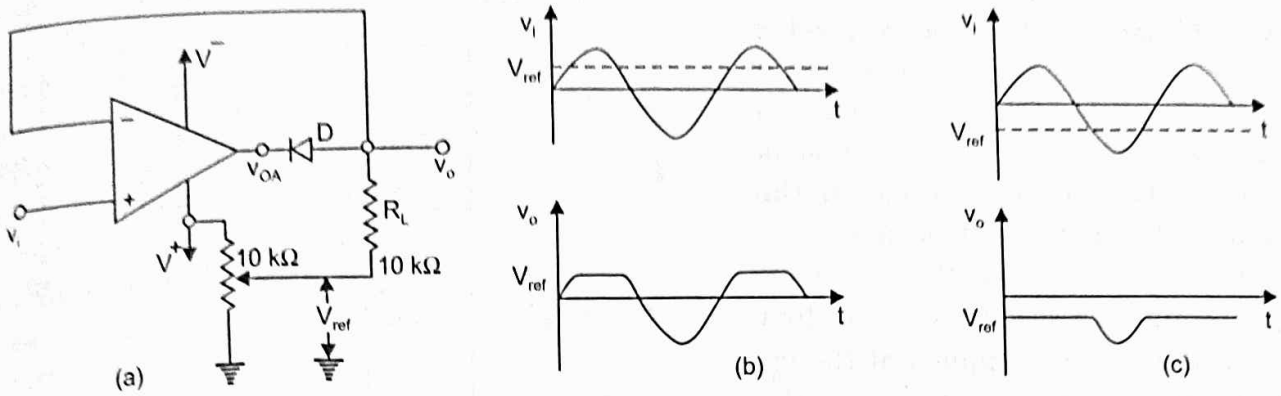


Fig. 4.24 (a) Positive clipper circuit; Input and output waveforms for (b) Positive V_{ref} (c) Negative

For input voltage $v_i < V_{ref}$, diode D conducts. The op-amp works as a voltage follower and output v_o follows input v_i till $v_i \leq V_{ref}$. When v_i is greater than V_{ref}, the output v_{oA} of the op-amp is large enough of drive D into cut-off. The op-amp operates in the open-loop and output voltage $v_o = V_{ref}$. However, if V_{ref} is made negative, then the entire output waveform above V_{ref} will get clipped off as shown in Fig. 4.24 (c).

The positive clipper of Fig. 4.24 (a) can be easily converted into a negative clipper by simply reversing diode D and changing the polarity of the reference voltage V_{ref} as shown in Fig. 4.25(a). The negative clipper clips off the negative parts of the input signal below the reference voltage. The circuit diagram of a negative clipper and the expected waveforms for negative V_{ref} and positive V_{ref} are shown in Fig. 4.25 (b and c).

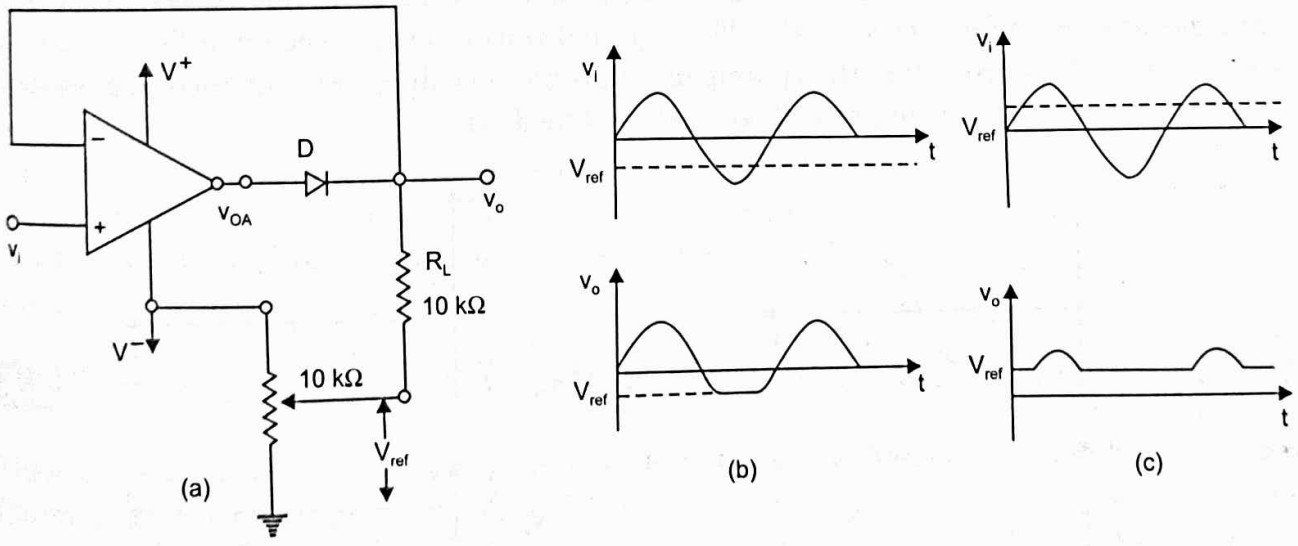


Fig. 4.25 (a) Negative clipper circuit (b, c) Input-output waveforms for negative and positive V_{ref}

4.6.5 Clamper

The clamper is also known as dc inserter or restorer. The circuit is used to add a desired dc level to the output voltage. In other words, the output is clamped to a desired dc level. If the

clamped dc level is positive, it is called positive clamper. Similarly if the clamped dc level is negative, the clamper is called negative clamper.

Figure 4.26 (a) shows a clamper with a variable positive dc voltage applied at the (+) input terminal. This circuit clamps the peaks of the input waveform and therefore is also called a peak clamper. The output voltage in the circuit is the net result of ac and dc input voltages applied to the (–) and (+) input terminals respectively. Let us first see the effect of V_{ref} applied at the (+) input terminal. For positive V_{ref}, the voltage v' is also positive, so that the diode D is forward biased. The circuit operates as a voltage follower and therefore output voltage $v_o = + V_{ref}$.

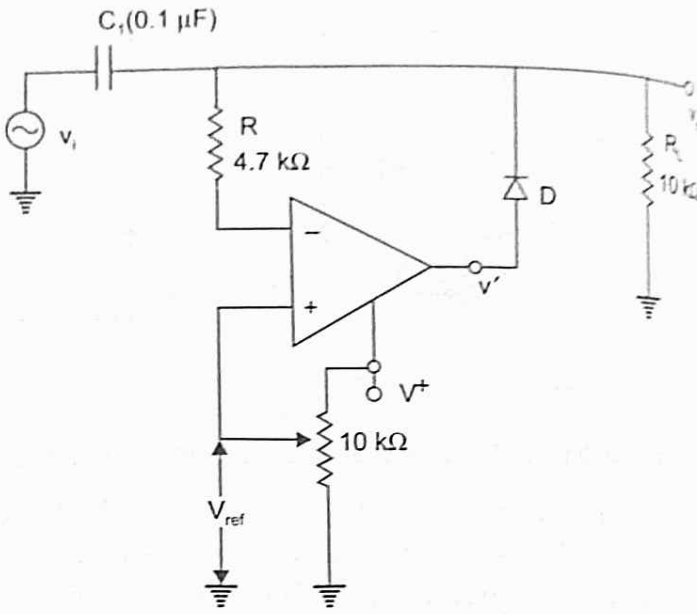


Fig. 4.26 (a) Peak clamper circuit

Now consider the ac input signal $v_i = V_m \sin \omega t$ applied at the (–) input terminal. During the negative half cycle of v_i, diode D conducts. The capacitor C_1 charges through diode D to the negative peak voltage V_m. However, during the positive half cycle of v_i, diode D is reverse biased. The capacitor retains its previous voltage V_m. Since this voltage V_m is in series with the ac input signal, the output voltage now will be $v_i + V_m$. The total output voltage is, therefore, $V_{ref} + v_i + V_m$. The input and output waveforms are shown in Fig. 4.26 (b). It is possible to obtain negative peak clamping by reversing the diode D and using a negative reference voltage $-V_{ref}$. The expected waveforms are shown in Fig. 4.26 (c). The resistor R is used for protecting the op-amp against excessive discharge currents from capacitor C_1 especially when the dc supply voltages are switched off.

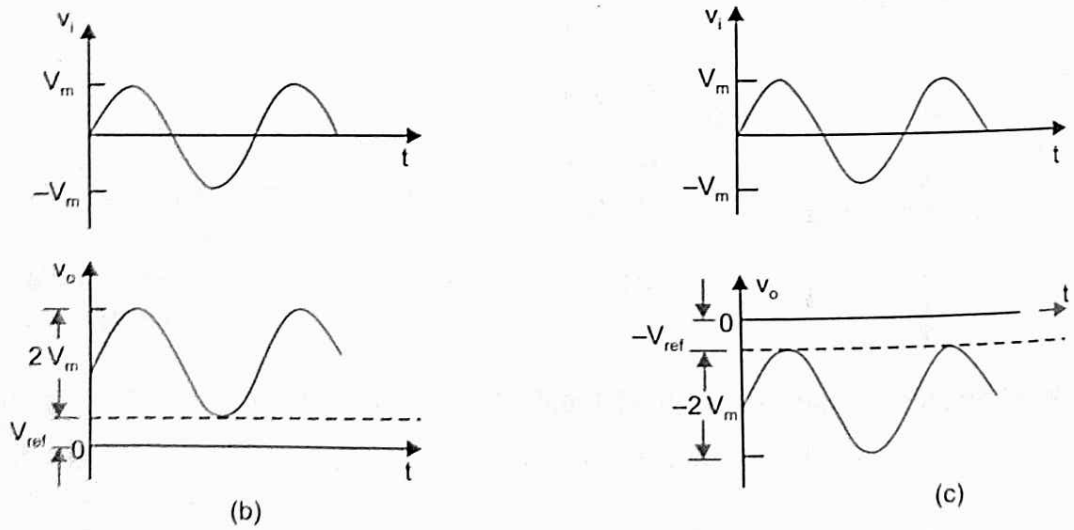


Fig. 4.26 (b) Waveforms for $+V_{ref}$, (c) Waveforms for $-V_{ref}$

4.7 SAMPLE AND HOLD CIRCUIT

A sample and hold circuit samples an input signal and holds on to its last sampled value until the input is sampled again. This type of circuit is very useful in digital interfacing and analog to digital and pulse code modulation systems. One of the simplest practical sample and hold circuit configuration is shown in Fig. 4.27 (a). The n-channel E-MOSFET works as a switch and is controlled by the control voltage v_c and the capacitor C stores the charge. The analog signal v_i to be sampled is applied to the drain of E-MOSFET and the control voltage v_c is applied to its gate. When v_c is positive, the E-MOSFET turns ***on*** and the capacitor C charges to the instantaneous value of input v_i with a time constant $[(R_o + r_{DS}\ (\textit{on})]\ C$. Here R_o is the output resistance of the voltage follower A_1 and r_{DS} (***on***) is the resistance of the MOSFET when ***on***. Thus the input voltage v_i appears across the capacitor C and then at the output through the voltage follower A_2. The waveforms are as shown in Fig. 4.27 (b).

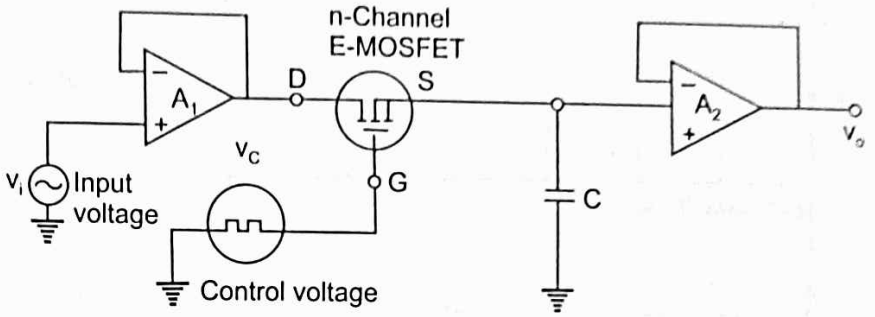


Fig. 4.27 (a) Sample and hold circuit

During the time when control voltage v_c is zero, the E-MOSFET is ***off***. The capacitor C is now facing the high input impedance of the voltage follower A_2 and hence cannot discharge. The capacitor holds the voltage across it. The time period T_S, the time during which voltage across the capacitor is equal to input voltage is called sample period. The time period T_H of v_c during which the voltage across the capacitor is held constant is called hold period. The frequency of the control voltage should be kept higher than (at least twice) the input so as to retrieve the input from output waveform. A low leakage capacitor such as Polystyrene, Mylar, or Teflon should be used to retain the stored charge.

Specially designed sample and hold ICs of make Harris semiconductor HA2420, National semiconductor such as LF198, LF398 are also available. A typical connection diagram of the LF398 is shown in Fig. 4.27 (c). It may be noted that the storage capacitor C is connected externally.

4.8 LOG AND ANTILOG AMPLIFIER

There are several applications of log and antilog amplifiers. Antilog computation may require functions such as ln x, log x or sinh x. These can be performed continuously with log-amps. One would like to have direct dB display on digital voltmeter and spectrum analyser. Log-amp can easily perform this function. Log-amp can also be used to compress the dynamic range of a signal.

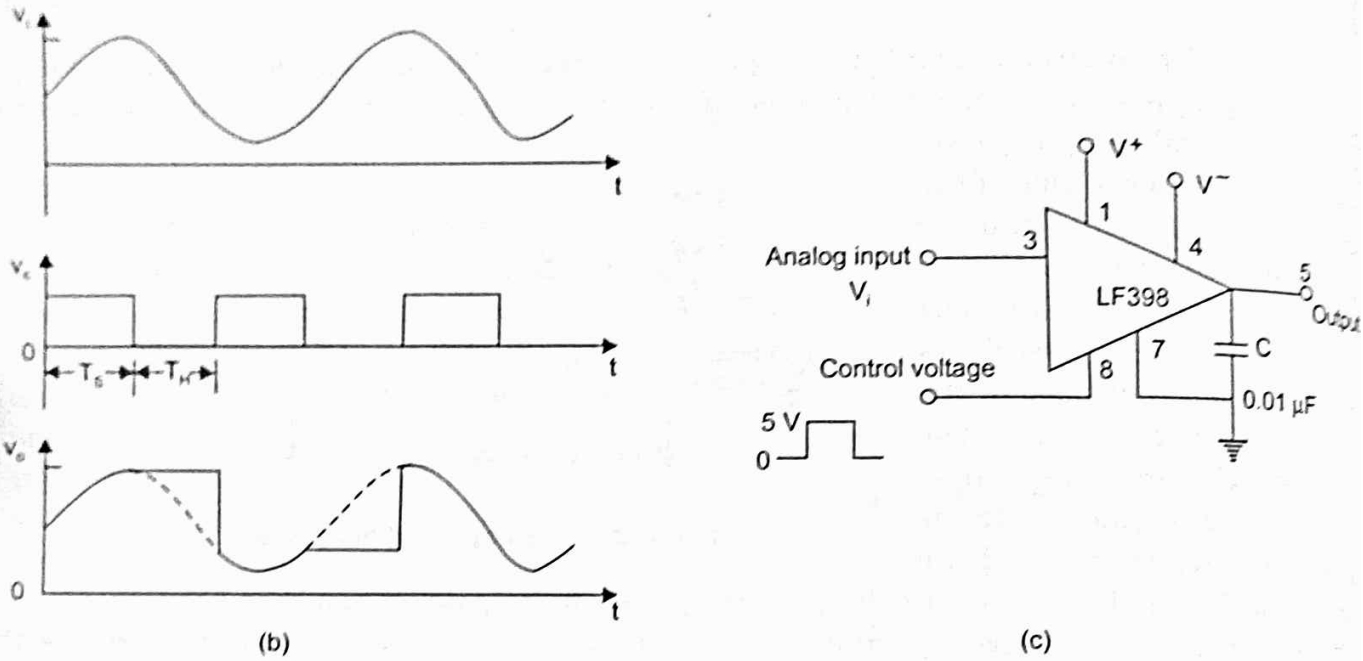


Fig. 4.27 (b) Input and output waveforms, (c) Typical connection diagram

Log Amplifier

The fundamental log-amp circuit is shown in Fig. 4.28 (a) where a grounded base transistor is placed in the feedback path. Since the collector is held at virtual ground and the base is also grounded, the transistor's voltage-current relationship becomes that of a diode and is given by,

$$I_E = I_s (e^{qV_E/kT} - 1) \qquad (4.42)$$

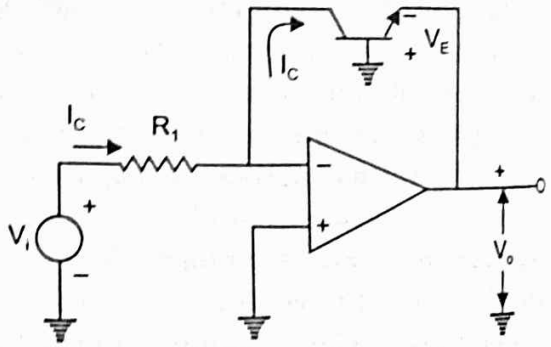


Fig. 4.28 (a) Fundamental log-amp circuit

Since, $I_C = I_E$ for a grounded base transistor,

$$I_C = I_s (e^{qV_E/kT} - 1) \qquad (4.43)$$

where I_s = emitter saturation current $\approx 10^{-13}$ A
k = Boltzmann's Constant
T = absolute temperature (in K)

$$\text{Therefore,} \quad \frac{I_C}{I_s} = (e^{qV_E/kT} - 1) \qquad (4.44)$$

or,
$$e^{qV_E/kT} = \frac{I_C}{I_s} + 1$$

$$\approx \frac{I_C}{I_s} \qquad [\text{as } I_s \approx 10^{-13} \text{ A}, I_C >> I_s]$$

Taking natural log on both sides, we get

$$V_E = \frac{kT}{q} \ln\left(\frac{I_C}{I_s}\right) \tag{4.45}$$

Also in Fig. 4.18 (a),

$$I_C = \frac{V_i}{R_1}$$

$$V_E = -V_o$$

$$V_o = -\frac{kT}{q} \ln\left(\frac{V_i}{R_1 I_s}\right) = -\frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right) \tag{4.46}$$

here $V_{ref} = R_1 I_s$

he output voltage is thus proportional to the logarithm of input voltage. Although the circuit ives natural log (ln), one can find $\log_{10}$ by proper scaling

$$\log_{10} X = 0.4343 \ln X \tag{4.47}$$

The circuit, however, has one problem. The emitter saturation current I_s varies from transistor) transistor and with temperature. Thus a stable reference voltage V_{ref} cannot be obtained. his is eliminated by the circuit given in Fig. 4.28 (b). The input is applied to one log-amp, hile a reference voltage is applied to another log-amp. The two transistors are integrated close)gether in the same silicon wafer. This provides a close match of saturation currents and nsures good thermal tracking.

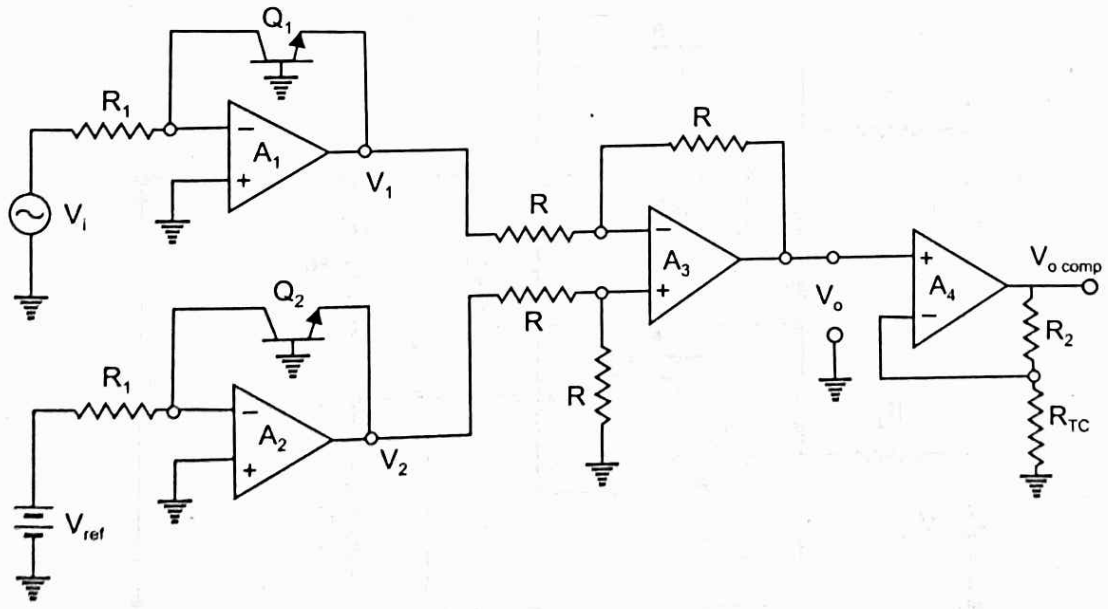


Fig. 4.28 (b) Log-amp with saturation current and temperature compensation

Assume, $$I_{s1} = I_{s2} = I_s \tag{4.48}$$

and then, $$V_1 = -\frac{kT}{q} \ln\left(\frac{V_i}{R_1 I_s}\right) \tag{4.49}$$

and $$V_2 = -\frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right) \tag{4.50}$$

Now, $$V_o = V_2 - V_1 = \frac{kT}{q}\left[\ln\left(\frac{V_i}{R_1 I_s}\right) - \ln\left(\frac{V_{ref}}{R_1 I_s}\right)\right] \tag{4.51}$$

or, $$V_o = \frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right) \tag{4.52}$$

Thus reference level is now set with a single external voltage source. Its dependence on device and temperature has been removed. The voltage V_o is still dependent upon temperature and is directly proportional to T. This is compensated by the last op-amp stage A_4 which provides a non-inverting gain of $(1 + R_2/R_{TC})$. Now, the output voltage is,

$$V_{o\ comp} = \left(1 + \frac{R_2}{R_{TC}}\right)\frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right) \tag{4.53}$$

where R_{TC} is a temperature-sensitive resistance with a positive coefficient of temperature (sensistor) so that the slope of the equation becomes constant as the temperature changes.

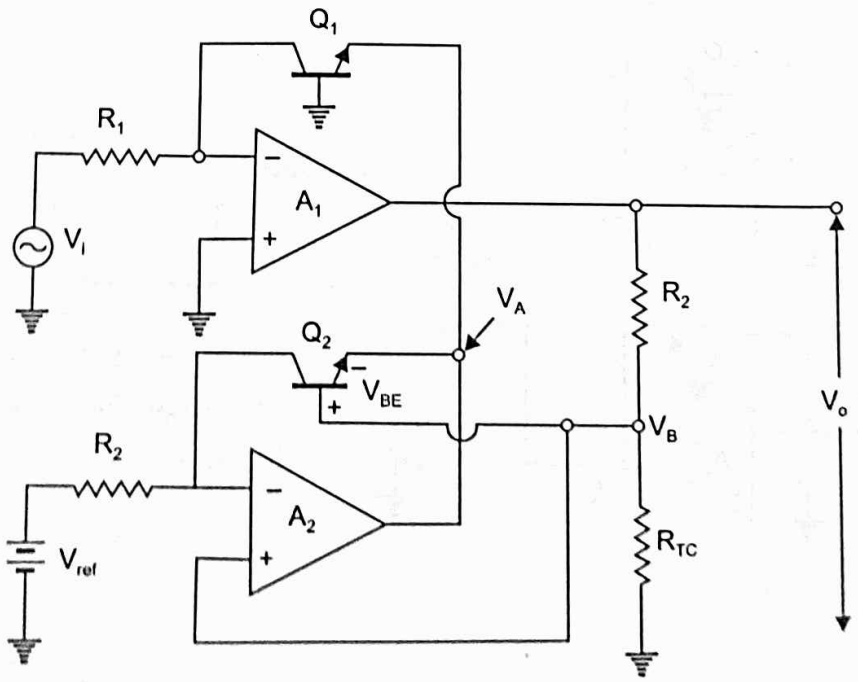


Fig. 4.28 (c) Log-amp using two op-amps only

The circuit in Fig. 4.28 (b) requires four op-amps, and becomes expensive if FET op-amps are used for precision. The same output (with an inversion) can be obtained by the circuit of Fig. 4.28 (c) using two op-amps only.

Antilog Amplifier

The circuit is shown in Fig. 4.29. The input V_i for the antilog-amp is fed into the temperature compensating voltage divider R_2 and R_{TC} and then to the base of Q_2. The output V_o of the antilog-amp is fed back to the inverting input of A_1 through the resistor R_1. The base to emitter voltage of transistors Q_1 and Q_2 can be written as

$$V_{Q1\ B\text{–}E} = \frac{kT}{q} \ln\left(\frac{V_o}{R_1 I_s}\right) \tag{4.54}$$

and

$$V_{Q2\ B\text{–}E} = \frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right) \tag{4.55}$$

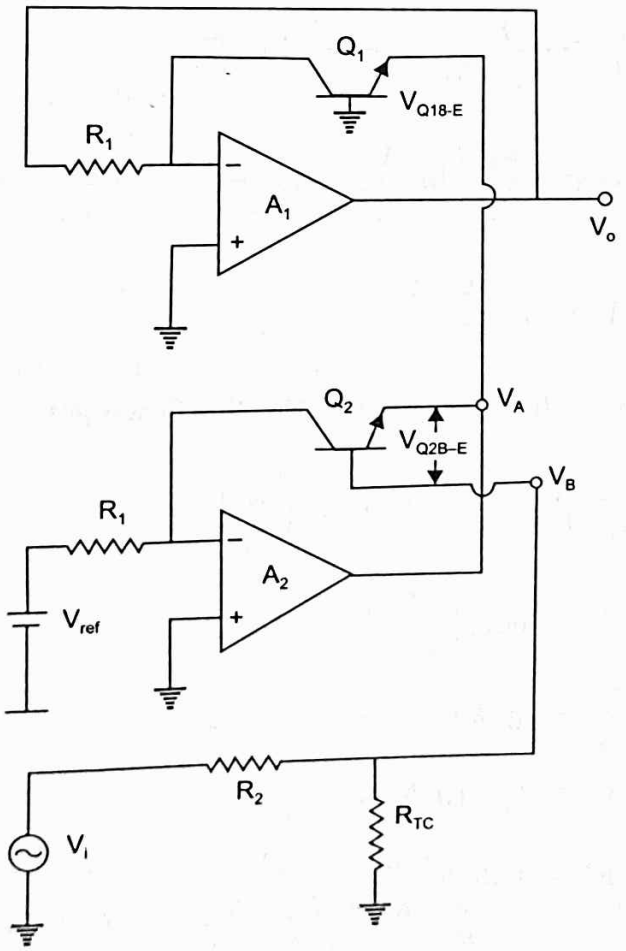


Fig. 4.29 Antilog amplifier

Since the base of Q_1 is tied to ground, we get

$$V_A = -V_{Q1\ B\text{-}E} = -\frac{kT}{q}\ln\left(\frac{V_o}{R_1 I_s}\right) \tag{4.56}$$

The base voltage V_B of Q_2 is

$$V_B = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i \tag{4.57}$$

The voltage at the emitter of Q_2 is

$$V_{Q2\ B\text{-}E} = V_B + V_{Q2\ E\text{-}B}$$

or,
$$V_{Q2\ B\text{-}E} = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i - \frac{kT}{q}\ln\left(\frac{V_{ref}}{R_1 I_s}\right) \tag{4.58}$$

But the emitter voltage of Q_2 is V_A, that is,

$$V_A = V_{Q2\ B\text{-}E}$$

or,
$$-\frac{kT}{q}\ln\frac{V_o}{R_1 I_s} = \frac{R_{TC}}{R_2 + R_{TC}}V_i - \frac{kT}{q}\ln\frac{V_{ref}}{R_1 I_s} \tag{4.59}$$

or,
$$\frac{R_{TC}}{R_2 + R_{TC}}V_i = -\frac{kT}{q}\left(\ln\frac{V_o}{R_1 I_s} - \ln\frac{V_{ref}}{R_1 I_s}\right)$$

or,
$$-\frac{q}{kT}\frac{R_{TC}}{R_2 + R_{TC}}V_i = \ln\left(\frac{V_o}{V_{ref}}\right) \tag{4.60}$$

Changing natural log, *i.e.*, ln to $\log_{10}$ using Eq. (4.47) we get

$$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i = 0.4343 \times \ln\left(\frac{V_o}{V_{ref}}\right) \tag{4.61}$$

or,
$$-K'V_i = \log_{10}\left(\frac{V_o}{V_{ref}}\right)$$

or,
$$\frac{V_o}{V_{ref}} = 10^{-K'V_i}$$

or,
$$V_o = V_{ref}\,(10^{-K'V_i}) \tag{4.62}$$

where
$$K' = 0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right) \tag{4.63}$$

Hence an increase of input by one volt causes the output to decrease by a decade. The 755 log/antilog amplifier IC chip is available as a functional module which may require some external components also to be connected to it.

4.9 MULTIPLIER AND DIVIDER

Analog Multiplier

There are a number of applications of analog multipliers such as (i) frequency doubling (ii) measurement of real power (iii) detecting phase-angle difference between two signals of equal frequency (iv) multiplying two signals (v) dividing one signal by another (vi) taking square root of a signal (vii) squaring a signal.

A basic multiplier schematic symbol is shown in Fig. 4.30 (a). Two signal inputs (v_x and v_y) are provided. The output is the product of the two inputs divided by a reference voltage V_{ref}. Thus output voltage is a scaled version of x and y inputs. The output voltage is given by

$$v_o = \frac{v_x v_y}{V_{ref}} \qquad (4.64)$$

Normally, V_{ref} is internally set to 10 volts. So,

$$v_o = \frac{v_x v_f}{10}$$

As long as

$$v_x < V_{ref}$$

and $$v_y < V_{ref}$$

the output of the multiplier will not saturate. Power supply voltage can range from ±8 V to ±18 V. Usually, multipliers are designed for the same type of power supplies as used for op-amps, namely ±15 V.

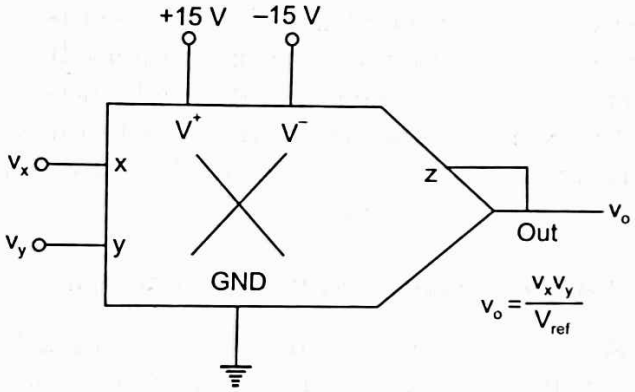


Fig. 4.30 (a) Multiplier schematic symbol

If both inputs are positive, the IC is said to be a one quadrant multiplier as shown in Fig. 4.30 (b). A two quadrant multiplier will function properly if one input is held positive and the other is allowed to swing both positive and negative Fig. 4.30 (c). If both inputs may be either positive or negative, the IC is called a four quadrant multiplier Fig. 4.30 (d).

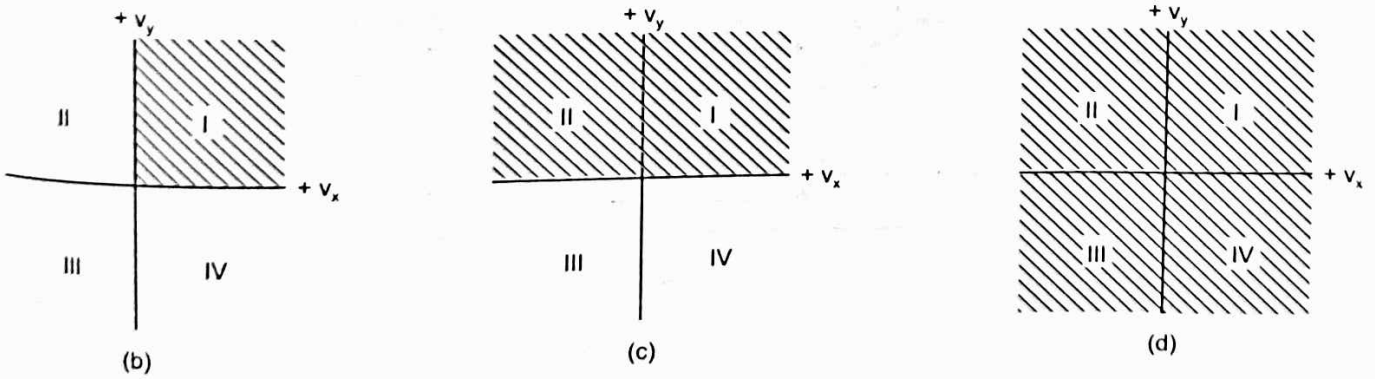


Fig. 4.30 (b) One quadrant multiplier, (c) Two quadrant multiplier (d) Four quadrant multiplier

There can be several ways to make a circuit which will multiply according to Eq. (4.64). One commonly used technique is log-antilog method. The log-antilog method relies on the mathematical relationship that the sum of the logarithm of two numbers equals the logarithm of the product of those numbers.

$$\ln v_x + \ln v_y = \ln(v_x v_y) \tag{4.65}$$

Figure 4.30 (e) is a block diagram of a log-antilog multiplier *IC*. Log-amps require the input and reference voltages to be of the same polarity. This restricts log-antilog multipliers to one quadrant operation.

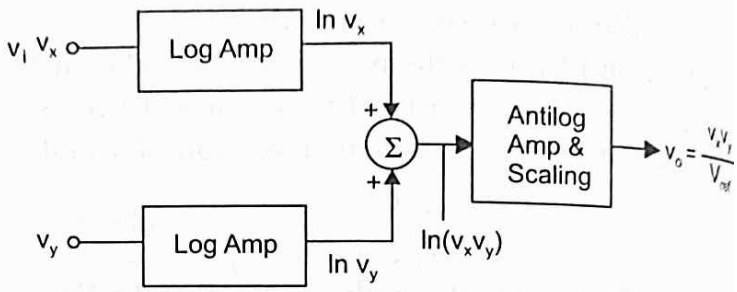


Fig. 4.30 (e) Block diagram of a log-antilog multiplier

Another very important technique suitable for monolithic *IC* realization is variable transconductance multipliers. It provides high speed operation which is 2 to 3 times more then the logarithmic method. It also redues error atleast by 10 times and provide bandwidth greater than 10 mHz. We now discuss this technique.

Variable Transconductance Multiplier

A basic emitter coupled differential amplifier discussed in chapter 2 can be used as a multiplier circuit but it has many limitations The Gilbert Multiplier cell as shown in Fig 4.31 is a modification of the basic emitter-coupled transistor pair and gives four quadrant multiplication. Two cross coupled emitter-coupled pairs in series connection with an emitter coupled pair form the structures of a Gilbert Cell

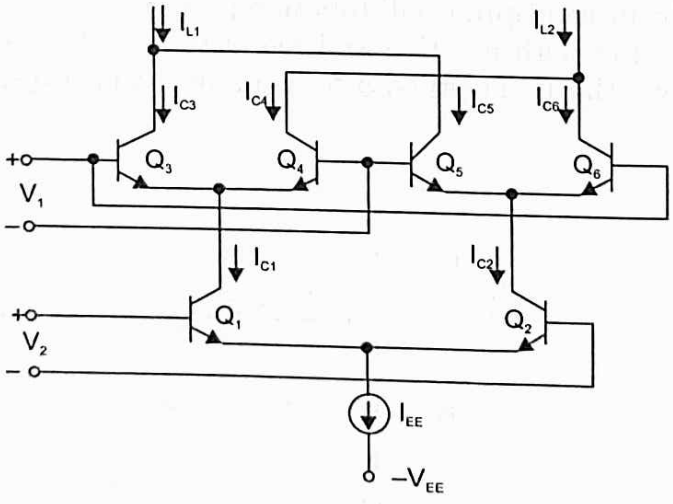


Fig. 4.31 Gilbert multiplier cell

The collector currents of Q_3 and Q_4 are given by

$$I_{C3} = \frac{I_{C1}}{1 + e^{-V_1/V_T}} \tag{4.66}$$

and
$$I_{C4} = \frac{I_{C1}}{1 + e^{V_1/V_T}} \tag{4.67}$$

Similarly the collector currents of Q_5 and Q_6 are given by

$$I_{C5} = \frac{I_{C2}}{1 + e^{V_1/V_T}} \tag{4.68}$$

and
$$I_{C6} = \frac{I_{C2}}{1 + e^{-V_1/V_T}} \tag{4.69}$$

The collector currents I_{C1} and I_{C2}, of transistors Q_1 and Q_2 can be expressed as

$$I_{C1} = \frac{I_{EE}}{1 + e^{-V_2/V_T}} \tag{4.70}$$

and
$$I_{C2} = \frac{I_{EE}}{1 + e^{V_2/V_T}} \tag{4.71}$$

Substituting Eq. (4.70) in Eqs. (4.66) and (4.67), we get

$$I_{C3} = \frac{I_{EE}}{\left[1 + e^{-V_1/V_T}\right]\left[1 + e^{-V_2/V_T}\right]} \tag{4.72}$$

and
$$I_{C4} = \frac{I_{EE}}{\left[1 + e^{V_1/V_T}\right]\left[1 + e^{-V_2/V_T}\right]} \tag{4.73}$$

Similarly, substituting Eq. (4.71) in Eqs. (4.68) and (4.69), we get

$$I_{C5} = \frac{I_{EE}}{\left[1 + e^{V_1/V_T}\right]\left[1 + e^{V_2/V_T}\right]} \tag{4.74}$$

and
$$I_{C6} = \frac{I_{EE}}{\left[1 + e^{-V_1/V_T}\right]\left[1 + e^{V_2/V_T}\right]} \tag{4.75}$$

The differential output current ΔI is given by

$$\Delta I = I_{L1} - I_{L2}$$

That is,
$$\Delta I = (I_{C3} + I_{C5}) - (I_{C4} + I_{C6})$$

or
$$\Delta I = (I_{C3} - I_{C6}) - (I_{C4} - I_{C5}) \tag{4.76}$$

Substituting Eqs (4.72) to (4.75) in (Eq 4.76) and using exponential formulae for hyperbolic functions, we get

$$\Delta I = I_{EE}\left[\tanh\left(\frac{V_1}{2V_T}\right)\tanh\left(\frac{V_2}{2V_T}\right)\right] \tag{4.77}$$

The above equation shows that when V_1 and V_2 are small, the Gilbert Cell shown in Fig 4.31 can be used as a four-quadrant analog multiplier with the use of *current-to-voltage* converters. The dc transfer characteristic of such a multiplier circuit is the product of the hyperbolic tangent of the two input voltages. The output voltage V_o can be generated from ΔI, by using two equal valued resistors connected to V_{CC} and by sending $I_{L1}(= I_{C3} + I_{C5})$ through one resistor and I_{L2} $(= I_{C4} + I_{C6})$ through the second resistor.

Complete Four-Quadrant Analog Multiplier

Fig 4.32 shows the circuit diagram of the complete four-quadrant analog multiplier using Gilbert Cell. It uses two *voltage-to-current* converters and one *current-to-voltage* converter. The currents I_9 and I_{10} passing through the emitters of Q_7 and Q_8 generate a voltage between the two emitter terminals, which is proportional to the inverse hyperbolic tangent of V_1.

Analysis of the Circuit The current through base-emitter junctions of transistors Q_7, Q_3, Q_4 and Q_8 connected in series can be expressed by

$$I_9\, I_3 = I_4\, I_{10} \tag{4.78}$$

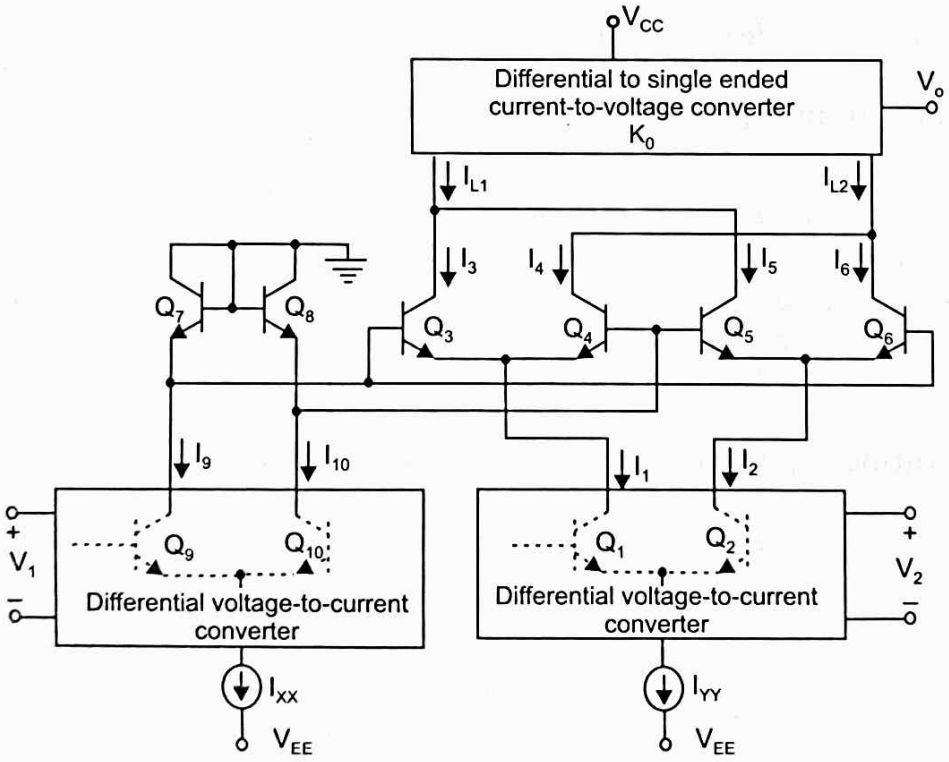


Fig. 4.32 A complete four quadrant analog multiplier using Gilbert Cell

Similarly, from the series connection of the transistors Q_7, Q_6, Q_5 and Q_8, we get

$$I_9\, I_6 = I_5\, I_{10} \tag{4.79}$$

Further, we can write

$$I_1 = I_3 + I_4 \tag{4.80(a)}$$

$$I_2 = I_5 + I_6 \tag{4.80(b)}$$

$$I_{L1} = I_3 + I_5 \tag{4.81(a)}$$

$$I_{L2} = I_4 + I_6 \tag{4.81(b)}$$

and

$$I_{XX} = I_9 + I_{10} \tag{4.82}$$

The transfer charactistics of the differential *voltage-to-current* converter is given by

$$I_9 - I_{10} = \frac{V_1}{K_1} \tag{4.83}$$

$$I_1 - I_2 = \frac{V_2}{K_2} \tag{4.84}$$

and the transfer characteristics of the *differential-to-single ended* current-to-voltage converter is given by

$$V_o = K_o(I_{L2} - I_{L1}) \tag{4.85}$$

where K_o, K_1 and K_2 are constants

Substituting for I_{L1} and I_{L2} we get,

$$V_o = K_o[(I_4 + I_6) - (I_3 + I_5]$$

Using Eqs. (4.78) and (4.79) we get

$$V_o = K_o \left[\left(I_4 + I_5 \frac{I_{10}}{I_9}\right) - \left(I_4 \frac{I_{10}}{I_9} + I_5\right)\right] \tag{4.86}$$

Simplifying the above equation, we get

$$V_o = K_o \left(\frac{I_9 - I_{10}}{I_9}\right)(I_4 - I_5) \tag{4.87}$$

Further, we see that

$$I_1 - I_2 = (I_3 + I_4) - (I_5 + I_6)$$

$$= \left(I_4 \frac{I_{10}}{I_9} + I_4\right) - \left(I_5 + I_5 \frac{I_{10}}{I_9}\right) \tag{4.88}$$

Solving for $(I_4 - I_5)$ gives

$$(I_4 - I_5) = \left(\frac{I_9}{I_9 + I_{10}}\right)(I_1 - I_2) \tag{4.89}$$

Substituting Eq. (4.89) in Eq. (4.87) and using Eq. (4.83) and Eq. (4.84) we get

$$V_o = K_o \left(\frac{I_9 - I_{10}}{I_9 + I_{10}}\right)(I_1 - I_2)$$

$$= \frac{K_o V_1 V_2}{I_{XX} K_1 K_2} = K_m V_1 V_2 \tag{4.90}$$

where $$K_m = \frac{K_o}{I_{XX} K_1 K_2}$$

Equation (4.90) uses no approximations. Hence the input signal amplitudes have no constrains.

Practical Implementation of the Four-Quadrant Analog Multiplier

A practical four-quadrant analog multiplier circuit is shown in Fig 4.33.

It can be seen that

$$I_1 - I_2 = \frac{2V_2}{R_Y} \tag{4.91}$$

$$I_9 - I_{10} = \frac{2V_1}{R_X} \tag{4.92}$$

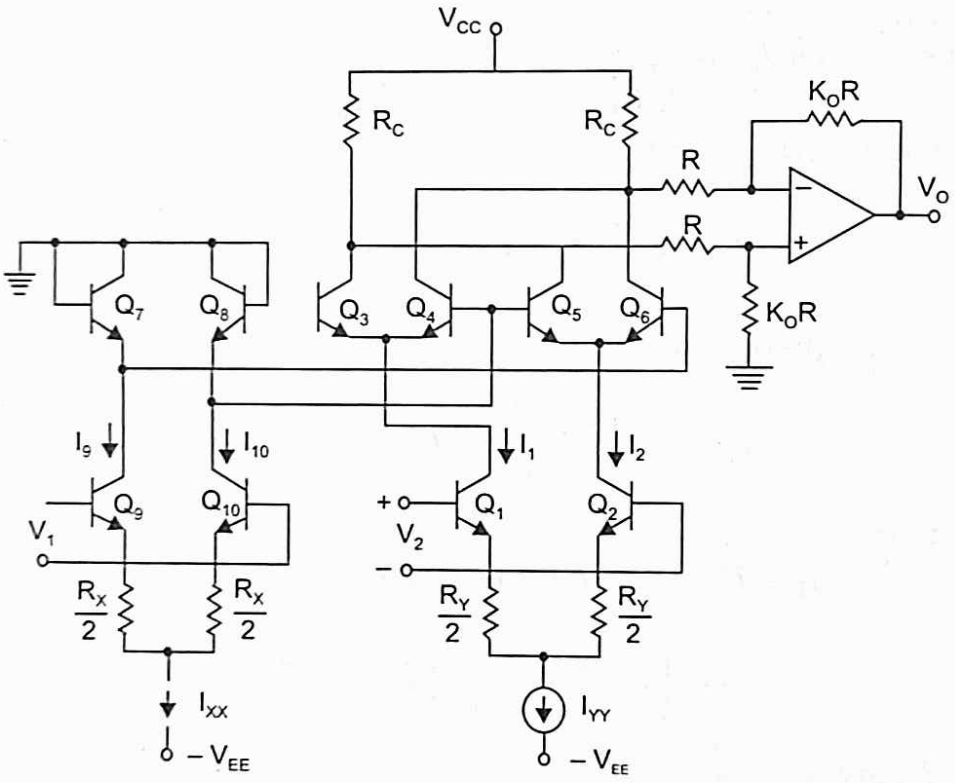


Fig. 4.33 Practical four-quadrant analog multiplier circuit

Further it is assumed that the drop across base-emitter of $Q_9 - Q_{10}$ and $Q_1 - Q_2$ pairs are small in comparison with the drop across R_X and R_Y.

Substituting Eqs. (4.91) and (4.92) in Eq. (4.93) we get

$$V_o = \frac{4K_o R_C V_1 V_2}{I_{XX} R_X R_Y}$$

$$= K_m V_1 \; V_2, \text{ where } R >> R_C$$

The circuit is capable of performing precise multiplication of a continuously varying analog signal by another signal. One of the problems though is the need to be able to trim the errors due to offsets and mismatches in the integrated circuit implementation.

ANALOG MULTIPLIER ICs

Analog multiplier is a circuit whose output voltage at any instant is proportional to the product of instantaneous value of two individual input voltages. The important applications of these multipliers are multiplication, division, squaring and square-rooting of signals, modulation and demodulation. The analog multipliers are available as integrated circuits consisting of op-amps and other circuit elements. The pin diagram of a typical analog multiplier, namely AD633 is shown in Fig 4.34.

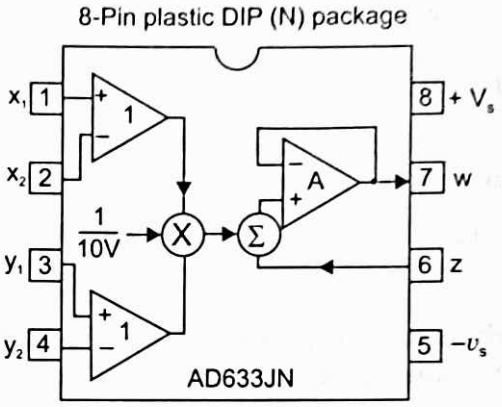


Fig 4.34 Pin diagram of AD633 multiplier IC

The AD633 multiplier is a four-quadrant analog multiplier. It possesses high input impedence, and this characteristic makes the loading effect on the signal source negligible. It can operate with supply voltages ranging from ± 8V to ± 18V. The *IC* does not require external components. The calibration by user is not necessary. The typical range of the two input signals is ± 10 V.

Multiplier Quadrants

The transfer characteristic of a typical four-quadrant multiplier is shown in Fig 4.35. Both the inputs can be positive or negative to obtain the corresponding output as shown in the transfer characteristics.

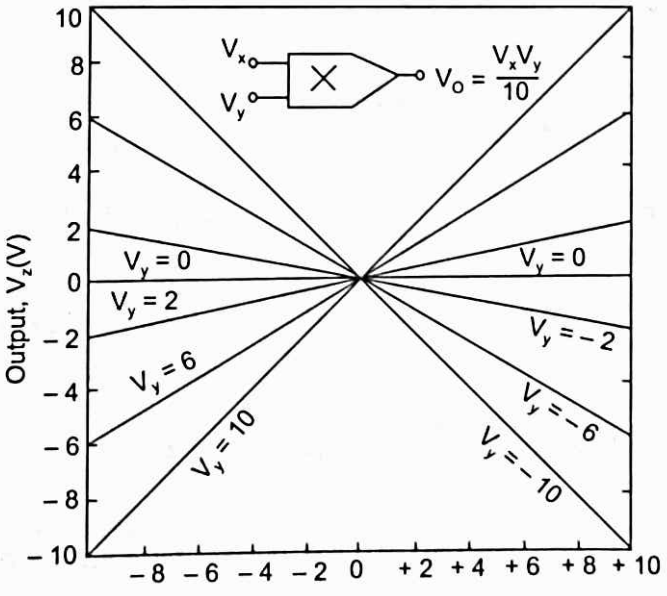


Fig 4.35 Transfer Characteristics of Four-quadrant multiplier

APPLICATIONS OF MULTIPLIER ICs

The multiplier ICs are used in the following applications:

(i) Frequency doubler
(ii) Voltage squarer

(iii) Voltage divider
(iv) Phase angle detector
(v) Square rooter

Frequency Doubler

The multiplication of two sine waves of the same frequency, but of possibly different amplitudes and phase allows to double a frequency and to directly measure *real* power.

Let, $$v_x = V_x \sin \omega t \tag{4.93}$$

$$v_y = V_y \sin (\omega t + \theta) \tag{4.94}$$

where θ is the phase difference between the two signals. Applying these two signals to the inputs of a four quadrant multiplier will yield an output as,

$$v_o = \frac{V_x \sin \omega t \, V_y \sin (\omega t + \theta)}{V_{ref}} \tag{4.95}$$

$$= \frac{V_x V_y}{V_{ref}} \sin \omega t \, (\sin \omega t \cos \theta + \sin \theta \cos \omega t)$$

$$= \frac{V_x V_y}{V_{ref}} (\sin^2 \omega t \cos \theta + \sin \theta \sin \omega t \cos \omega t)$$

As $$\sin^2 a = 1 - \cos^2 a$$

and $$\cos 2a = 2 \cos^2 a - 1$$

so, $$\cos^2 a = \frac{1}{2} + \left(\frac{1}{2}\right) \cos 2a$$

$$\sin^2 a = 1 - \frac{1}{2} - \left(\frac{1}{2}\right) \cos 2a = \frac{1}{2} - \left(\frac{1}{2}\right) \cos 2a$$

so, $$v_o = \frac{V_x V_y}{V_{ref}} \left[\cos \theta \left(\frac{1}{2} - \left(\frac{1}{2}\right) \cos 2 \omega t \right) + \sin \theta \sin \omega t \cos \omega t \right] \tag{4.96}$$

But, $$\sin a \cos a = \left(\frac{1}{2}\right) \sin 2a$$

Hence, $$v_o = \frac{V_x V_y}{2 V_{ref}} (\cos \theta - \cos \theta \cos 2 \omega t + \sin \theta \sin 2 \omega t)$$

or, $$v_o = \frac{V_x V_y}{2V_{ref}} \cos \theta + \frac{V_x V_y}{2V_{ref}} (\sin \theta \sin 2 \omega t - \cos \theta \cos 2 \omega t) \tag{4.97}$$

The first term is a DC and is set by the magnitude of the signals and their phase difference. The second term varies with time, but at twice the frequency of the inputs (2ω).

The circuit works as an ideal doubler if same frequency is applied to both the inputs. For example if

$$v_x = V_x \sin \omega t$$

and

$$v_y = V_y \sin \omega t$$

Then

$$V_o = \frac{V_x V_y}{V_{ref}} \sin^2 \omega t$$

$$= \frac{V_x V_y}{V_{ref}} \left(1 - \frac{\cos 2\ \omega t}{2}\right)$$

The output thus contains a dc term and a negative cosine wave of double frequency. The dc term can be easily removed by using a 1-μF coupling capacitor between load and the output terminal.

Voltage Squarer Circuit

The basic multiplier of Fig. 4.30 (a) can be used to square any positive or negative number provided the number can be represented by a voltage between 0 to V_{ref}. The voltage v_i representing the number is connected to both the inputs as shown in Fig. 4.36 (a).

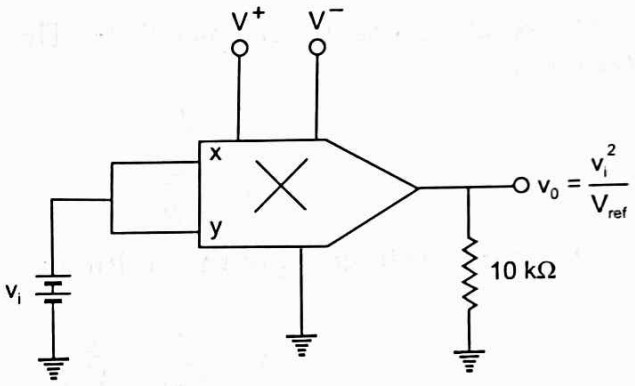


Fig. 4.36 (a) Squarer Circuit

It is possible to square a sinewave voltage too. In Fig. 4.36 (a), if a sinewave voltage $v_i = V_m \sin \omega t$ is applied to both the inputs, then the output voltage, v_o is given by

$$v_o = \frac{v_i^2}{V_{ref}}$$

For $v_i = 5 \sin 2\pi \times 10^4 t$ and $V_{ref} = 10$ V,

$$v_o = \frac{5^2}{10} (\sin 2\pi \times 10^4 t)^2$$

$$= 2.5 \left[\frac{1}{2} - \frac{1}{2}\cos 2\pi \times 2 \times 10^4 t\right] = 1.25 - 1.25 \cos 2\pi \times 2 \times 10^4 t$$

The output contains a dc term and frequency is doubled.

Phase Angle Detection

If the input signals applied to a multiplier are

$$v_x = V_{mx} \sin \omega t \quad (4.98\ (a))$$

$$v_y = V_{my} \sin (\omega t + \theta) \quad (4.98\ (b))$$

Then,

$$v_o = \frac{V_{mx} V_{my}}{V_{ref}} \sin \omega t \sin (\omega t + \theta) \quad (4.99\ (a))$$

$$= \frac{V_{mx} V_{my}}{V_{ref}} \times \frac{1}{2} [\cos \theta - \cos (2\ \omega t + \theta)] \quad (4.99\ (b))$$

The phase difference θ between the two input signals can be calculated from the dc component in the output voltage V_o. That is,

$$V_o,\text{dc} = \frac{V_{mx}V_{my}}{2V_{ref}} \times \cos\theta \qquad (4.100)$$

Thus, if the output V_o,dc = o, then the phase difference in the input signals is 90°.

Voltage Divider

Division, the complement of multiplication, can be accomplished by placing the multiplier circuit element in the op-amp's feedback loop. The output voltage from the divider in Fig. 4.36 (b) with input signals v_z and v_x as dividend and divisor respectively, is given by

$$v_o = -V_{ref}\frac{v_z}{v_x} \qquad (4.101\text{ (a)})$$

The result can be derived as follows. The op-amp's inverting terminal is at virtual ground. Therefore,

$$I_z = I_A$$

and

$$I_z = \frac{v_z}{R}$$

The output voltage V_A of the multiplier is determined by the multiplication of v_x and v_y

$$V_A = \frac{v_x v_y}{V_{ref}} = \frac{v_x v_o}{V_{ref}} \qquad (4.101\text{ (b)})$$

Again

$$V_A = -I_A R$$

so,

$$I_A = -V_A/R = -\frac{v_x v_o}{V_{ref}\,R} \qquad (4.102\text{ (a)})$$

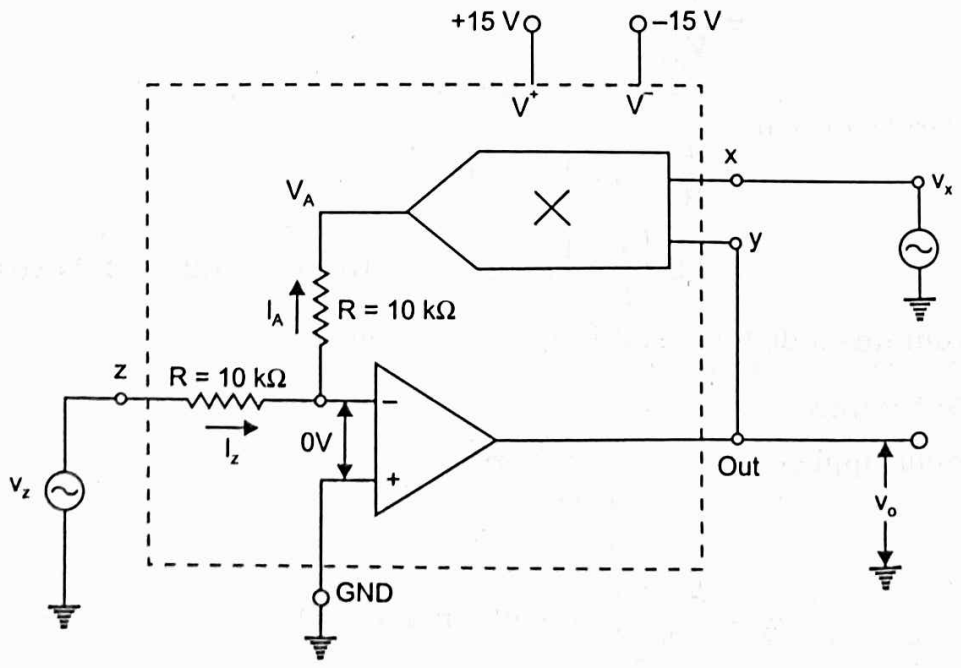


Fig. 4.36 (b) Multiplier IC configured as divider

As, $I_z = I_A$

so, $I_z = -\frac{v_x v_o}{V_{ref} R}$

and $v_z = I_z R = -\frac{v_x v_o}{V_{ref}}$

or, $v_o = -V_{ref}\frac{v_z}{v_x}$ (4.102 (b))

Division by zero is, of course, prohibited. Multiplier IC can be used for squaring a signal. Similarly, divider circuit can be used to take the square root of a signal.

Square Rooter

A divider circuit can be used to find square roots by connecting both the inputs of the multiplier to the output of an op-amp as shown in Fig. 4.36 (c).

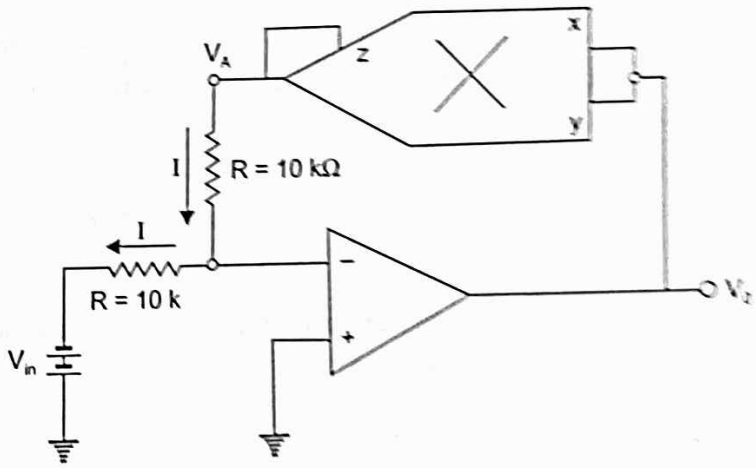


Fig. 4.36 (c) Finding square roots

In Fig. 4.36 (c)

$$V_A = \frac{V_o^2}{V_{ref}}$$

and $V_A = -V_{in}$

So, $V_o^2 = -V_{in} V_{ref}$

or $V_o = \sqrt{V_{ref}\,|V_{in}|}$ (4.103)

(taking magnitude only)

Thus, output V_o is proportional to square root of magnitude of V_{in}. Note that V_{in} must be negative or else op-amp will saturate. The range of V_{in} lies between –1 and –10 V.

4.10 DIFFERENTIATOR

One of the simplest of the op-amp circuits that contain capacitor is the differentiating amplifier, or differentiator. As the name suggests, the circuit performs the mathematical operation of differentiation, that is, the output waveform is the derivative of input waveform. A differentiator circuit is shown in Fig. 4.21 (a).

Analysis

The node N is at virtual ground potential *i.e.*, $v_N = 0$. The current i_C through the capacitor is,

$$i_C = C_1 \frac{d}{dt}(v_i - v_N) = C_1 \frac{dv_i}{dt} \quad (4.104)$$

The current i_f through the feedback resistor is v_o/R_f and there is no current into the op-amp. Therefore, the nodal equation at node N is,

$$C_1 \frac{dv_i}{dt} + \frac{v_o}{R_F} = 0$$

from which we have

$$\boxed{v_o = -R_F C_1 \frac{dv_i}{dt}} \qquad (4.105)$$

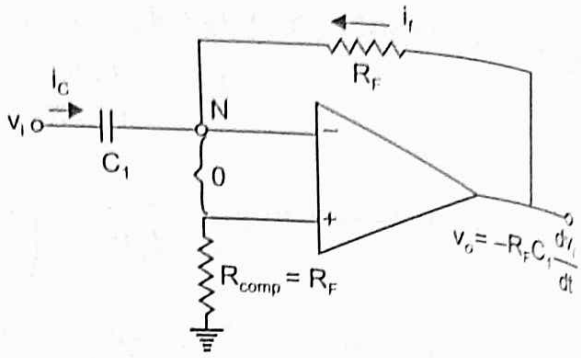


Fig. 4.37 (a) Op-amp differentiator

Thus the output voltage v_o is a constant $(-R_F C_1)$ times the derivative of the input voltage v_i and the circuit is a differentiator. The minus sign indicates a 180° phase shift of the output waveform v_o with respect to the input signal.

The phasor equivalent of Eq. (4.105) is, $V_o(s) = -R_F C_1 s V_i(s)$ where V_o and V_i is the phasor representation of v_o and v_i. In steady state, put $s = j\omega$. We may now write the magnitude of gain A of the differentiator as,

$$|A| = \left|\frac{V_o}{V_i}\right| = |-j\omega R_F C_1| = \omega R_F C_1 \qquad (4.106)$$

From Eq. (4.106), one can draw the frequency response of the op-amp differentiator. Equation (4.106) may be rewritten as

$$|A| = \frac{f}{f_a}$$

where

$$f_a = \frac{1}{2\pi R_F C_1} \qquad (4.107)$$

At $f = f_a$, $|A| = 1$, *i.e.*, 0 dB, and the gain increases at a rate of +20 dB/decade. Thus at high frequency, a differentiator may become unstable and break into oscillation. There is one more problem in the differentiator of Fig. 4.37 (a). The input impedance (*i.e.*, $1/\omega C_1$) decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise.

Practical Differentiator

A practical differentiator of the type shown in Fig. 4.37 (b) eliminates the problem of instability and high frequency noise.

The transfer function for the circuit in Fig. 4.37 (b) is given by,

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_F}{Z_1} = -\frac{sR_F C_1}{(1 + sR_F C_F)(1 + sC_1 R_1)} \qquad (4.108)$$

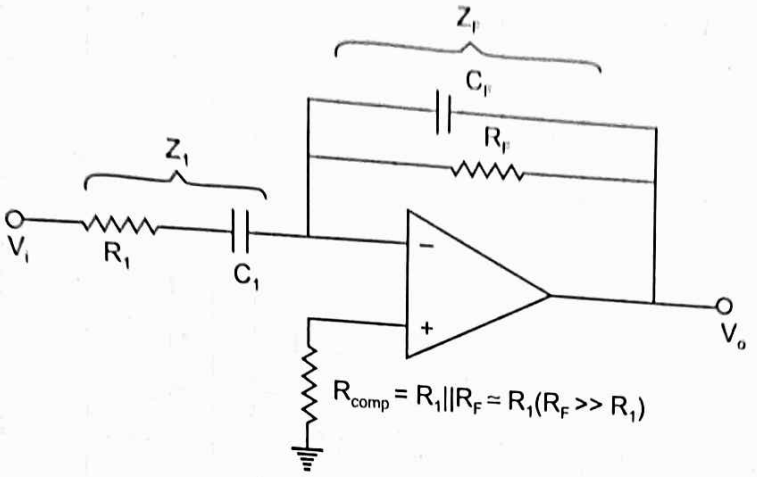


Fig. 4.37 (b) Practical differentiator

For $R_F C_F = R_1 C_1$, we get

$$\frac{V_o(s)}{V_i(s)} = -\frac{sR_F C_1}{(1 + sR_1 C_1)^2} = -\frac{sR_F C_1}{\left(1 + j\frac{f}{f_b}\right)^2} \tag{4.109}$$

where,

$$f_b = \frac{1}{2\pi R_1 C_1} \tag{4.110}$$

From Eq. (4.109), it is evident that the gain increases at +20 dB/decade for frequency $f < f_b$ and decreases at –20 dB/decade for $f > f_b$ as shown by dashed lines in Fig. 4.37 (c). This 40 dB/decade change in gain is caused by $R_1 C_1$ and $R_F C_F$ factors. For the basic differentiator of Fig. 4.37 (a), the frequency response would have increased continuously at the rate of +20 dB/decade even beyond f_b causing stability problem at high frequency. Thus the gain at high frequency is reduced significantly, thereby avoiding the high frequency noise and stability problems. The value of f_b should be selected such that,

$$f_a < f_b < f_c$$

where f_c is the unity gain-bandwidth of the op-amp in open-loop configuration.

For good differentiation, one must ensure that the time period T of the input signal is larger than or equal to $R_F C_1$, that is,

$$T \geq R_F C_1 \tag{4.111}$$

It may be noted that for $R_F C_1$ much greater than $R_1 C_1$ or $R_F C_F$, Eq. (4.108) is reduced to, $V_o/V_i = -sR_F C_1$, that is, the expression of the output voltage remains the same as in the case of an ideal differentiator as

$$v_o = -R_F C_1 \frac{dv_i}{dt} \tag{4.112}$$

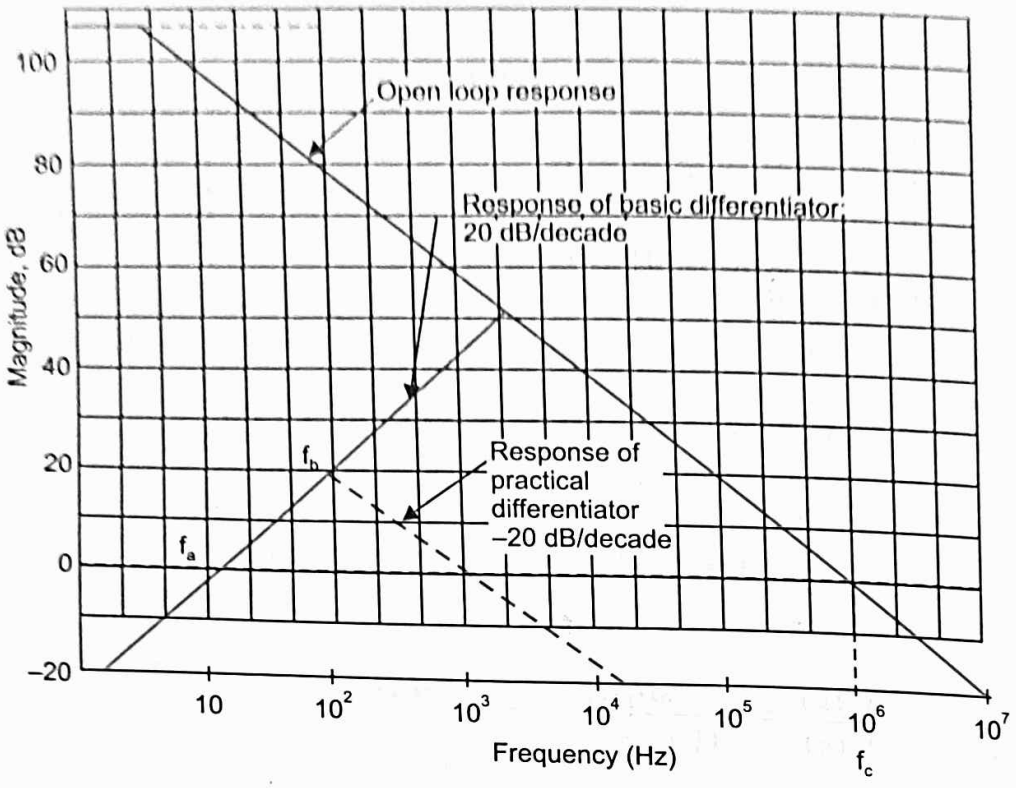


Fig. 4.37 (c) Frequency response

A resistance $R_{comp}(=R_1 \| R_F)$ is normally connected to the (+) input terminal to compensate for the input bias circuit.

A good differentiator may be designed as per the following steps:

1. Choose f_a equal to the highest frequency of the input signal. Assume a practical value of C_1 (<1 μF) and then calculate R_F.
2. Choose $f_b = 10\, f_a$ (say). Now calculate the values of R_1 and C_F so that $R_1C_1 = R_FC_F$.

Example 4.5

(a) Design an op-amp differentiator that will differentiate an input signal with f_{max} = 100 Hz.
(b) Draw the output waveform for a sine wave of 1 V peak at 100 Hz applied to the differentiator.
(c) Repeat part (b) for a square wave input.

Solution

(a) Select, $f_a = f_{max} = 100\ \text{Hz} = \dfrac{1}{2\pi R_F C_1}$ [from Eq. (4.107)]

Let $C_1 = 0.1\ \mu\text{F}$,

then $R_F = \dfrac{1}{2\pi(10^2)(10^{-7})} = 15.9\ \text{k}\Omega$

Now choose $f_b = 10\, f_a = 1\ \text{kHz} = \dfrac{1}{2\pi R_1 C_1}$ [from Eq. (4.110)]

Therefore, $$R_1 = \frac{1}{2\pi(10^3)(10^{-7})} = 1.59\ \text{k}\Omega$$

Since $$R_F C_F = R_1 C_1,$$

we get, $$C_F = \frac{1.59 \times 10^3 \times 10^{-7}}{15.9 \times 10^3} = 0.01\ \mu\text{F}$$

(b) $v_i = 1 \sin 2\pi(100)t$

From Eq. (4.69),

$$v_o = -R_f C_1 \frac{dv_i}{dt} = -(15.9\ \text{k}\Omega)\ (0.1\ \mu\text{F})\ \frac{d}{dt}[(1\,\text{V})\sin(2\pi)(10^2)t]$$

$$= -(15.9\ \text{k}\Omega)\ (0.1\ \mu\text{F})\ (2\pi)\ (10^2)\cos[(2\pi)\ (10^2)t] = -0.999\cos[2\pi\ (10^2)t]$$

$$= -1\cos[(2\pi)\ (10^2)\ t]$$

The input and output waveforms are shown in Fig. 4.38 (a).

(c) For a square wave input, say 1 V peak and 1 KHz, the output waveform will consist of positive and negative spikes of magnitude V_{sat} which is approximately 13 V for ±15 V op-amp power supply.

During the time periods for which input is constant at ±1 V, the differentiated output will be zero. However, when input transits between ±1 V levels, the slope of the input is infinite for an ideal square wave. The output, therefore, gets clipped to about ±13V for a ±15 V op-amp power supply as shown in Fig. 4.38 (b).

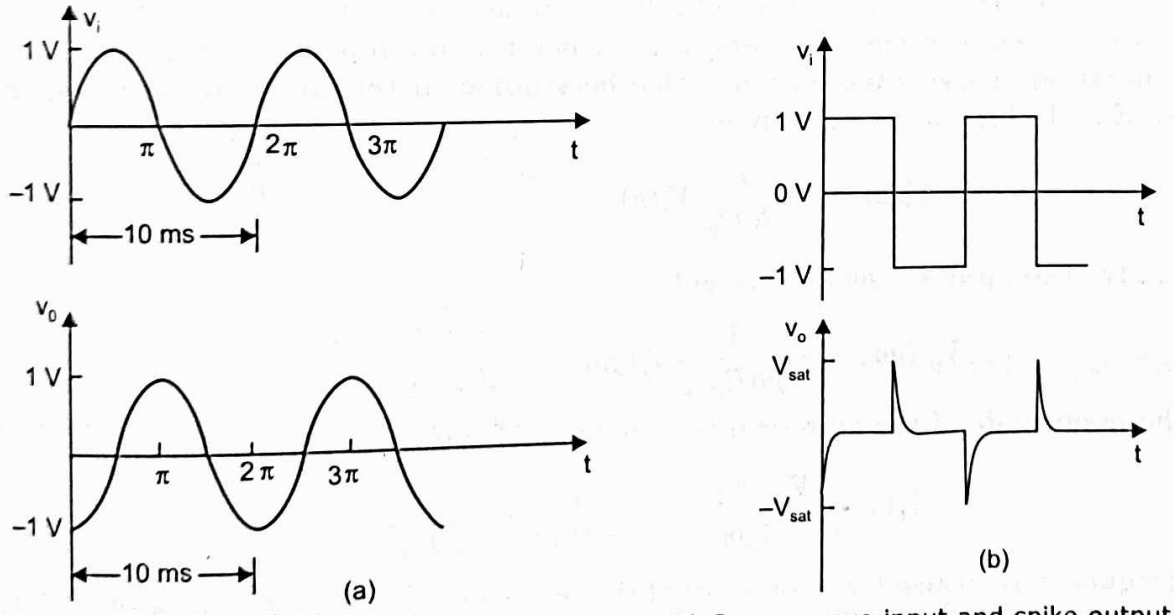


Fig. 4.38 (a) Sine-wave input and cosine output, (b) Square wave input and spike output

4.11 INTEGRATOR

If we interchange the resistor and capacitor of the differentiator of Fig. 4.37 (a), we have the circuit of Fig. 4.39 (a) which as we will see, is an integrator. The nodal equation at node N is,

$$\frac{v_i}{R_1} + C_F \frac{dv_o}{dt} = 0 \qquad (4.113)$$

or, $$\frac{dv_o}{dt} = -\frac{1}{R_1 C_F} v_i$$

Integrating both sides, we get

$$\int_0^t dv_o = -\frac{1}{R_1 C_F} \int_0^t v_i \, dt$$

$$v_o(t) = -\frac{1}{R_1 C_F} \int_0^t v_i(t)\, dt + v_o(0) \qquad (4.114)$$

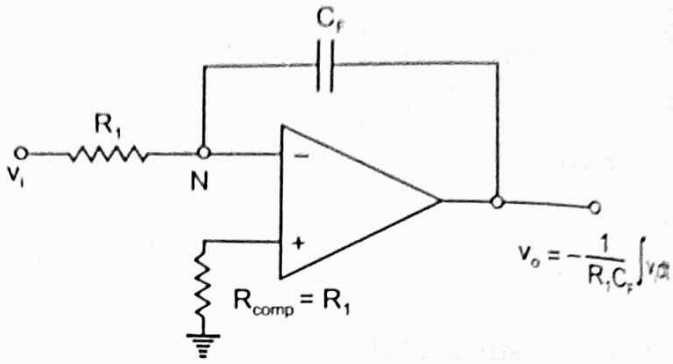


Fig. 4.39 (a) Op-amp integrator

where $v_o(0)$ is the initial output voltage.

The circuit, thus provides an output voltage which is proportional to the time integral of the input and R_1C_F is the time constant of the integrator. It may be noted that there is a negative sign in the output voltage, and therefore, this integrator is also known as an inverting integrator. A resistance, $R_{comp} = R_1$ is usually connected to the (+) input terminal to minimize the effect of input bias current.

A simple low pass RC circuit can also work as an integrator when time constant is very large. This requires very large values of R and C. The components R and C cannot be made infinitely large because of practical limitations. However, in the op-amp integrator of Fig. 4.39, by Miller's theorem, the effective input capacitance becomes $C_F(1 - A_v)$ where A_v is the gain of the op-amp. The gain A_v is infinite for an ideal op-amp, so the effective time constant of the op-amp integrator becomes very large which results in perfect integration.

The operation of the integrator can also be studied in the frequency domain. In phasor notation, Eq. (4.114) can be written as

$$V_o(s) = -\frac{1}{sR_1C_F} V_i(s) \qquad (4.115)$$

In steady state, put $s = j\omega$ and we get

$$V_o(j\omega) = -\frac{1}{j\omega R_1 C_F} V_i(j\omega) \qquad (4.116)$$

So, the magnitude of the gain or integrator transfer function is

$$|A| = \left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \left|-\frac{1}{j\omega R_1 C_F}\right| = \frac{1}{\omega R_1 C_F} \qquad (4.117)$$

The frequency response (or Bode Plot) of this basic integrator is shown in Fig. 4.39 (b). The Bode plot is a straight line of slope −6dB/octave (or equivalently −20 dB/decade). The frequency f_b in Fig. 4.39 (b) is the frequency at which the gain of the integrator is 0 dB and is given by

$$f_b = \frac{1}{2\pi R_1 C_F}$$

It can further be seen from Eq. (4.117) that at $\omega = 0$, the magnitude of the integrator transfer function is infinite. At dc, the capacitor C_F behaves as an open circuit and there is no negative

feedback. The op-amp thus operates in open loop, resulting in an infinite gain. In practice, of course, output never becomes infinite, rather the output of the amplifier saturates at a voltage close to the op-amp positive or negative power supply depending on the polarity of the input dc signal.

As the gain of the integrator decreases with increasing frequency, the integrator circuit does not have any frequency problem as faced in a differentiator. However, at low frequencies such as at dc ($\omega \cong 0$), the gain becomes infinite (or saturates). The solution to this problem is discussed in the following.

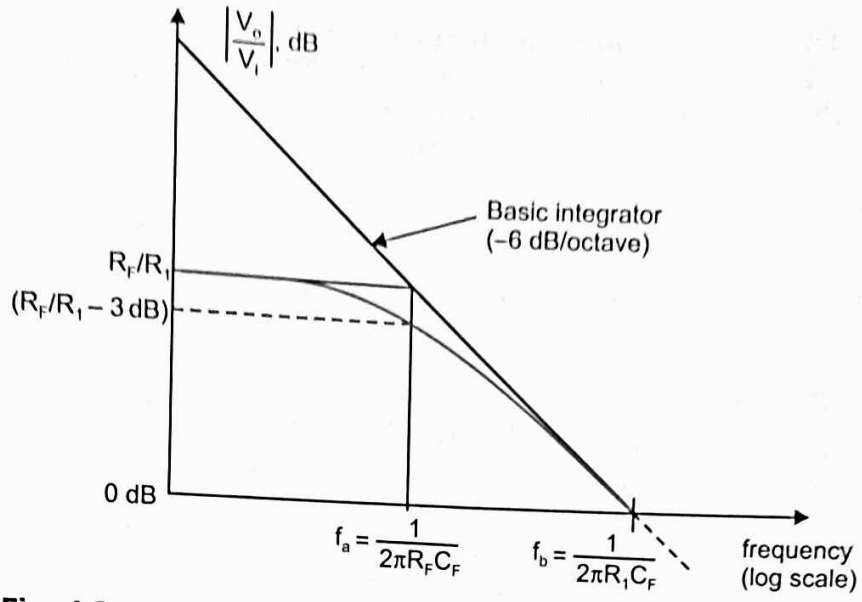


Fig. 4.39 (b) Frequency response of a basic and Lossy integrator

Practical Integrator Circuit (Lossy Integrator)

The gain of an integrator at low frequency (dc) can be limited to avoid the saturation problem if the feedback capacitor is shunted by a resistance R_F as shown in Fig. 4.39 (c). The parallel combination of R_F and C_F behaves like a practical capacitor which dissipates power unlike an ideal capacitor. For this reason, this circuit is also called a lossy integrator. The resistor R_F limits the low frequency gain to $-R_F/R_1$ (generally $R_F = 10\,R_1$) and thus provides dc stabilization.

Analysis

The nodal equation at the inverting input terminal of the op-amp of Fig. 4.39 (c) is,

$$\frac{V_i(s)}{R_1} + sC_F V_o(s) + \frac{V_o(s)}{R_F} \tag{4.118}$$

from which we have,

$$V_o(s) = -\frac{1}{sR_1C_F + R_1/R_F} V_i(s) \tag{4.119}$$

If R_F is large, the lossy integrator approximates the ideal integrator. For $s = j\omega$, magnitude of the gain of lossy integrator is given by

$$|A| = \left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{\omega^2 R_1^2 C_F^2 + R_1^2/R_F^2}} = \frac{R_F/R_1}{\sqrt{1 + (\omega R_F C_F)^2}} \tag{4.120}$$

The Bode plot of the lossy integrator is also shown in Fig. 4.39 (b). At low frequencies gain is constant at R_F/R_1. The break frequency ($f = f_a$) at which the gain is 0.707 (R_F/R_1) (or − 3 dB below its value of R_F/R_1) is calculated from Eq. (4.84) as

$$\sqrt{1 + (\omega R_F C_F)^2} = \sqrt{2}$$

Solving for $f = f_a$, we get

$$f_a = \frac{1}{2\pi R_F C_F} \tag{4.121}$$

This is a very important frequency. It tells us where the useful integration range starts. If the input frequency is lower than f_a the circuit acts like a simple inverting amplifier and no integration results. At input frequency equal to f_a, 50% accuracy results. The practical thumb rule is that if the input frequency is 10 times f_a, than 99% accuracy can result.

Initial Conditions

An integrator must also be provided with an external circuit to introduce initial conditions as shown in Fig. 4.40. When ganged switch S is in position 1, the input is zero and the capacitor is charged to the voltage V almost instantaneously* setting an initial condition of $v_o(0) = V$. When the switch S is in position 2, the amplifier is connected as in integrator and its output will be V plus a constant $-1/R_1 C_F$ times the time integral of the input voltage v_i. The capacitor C_F should have very low leakage and is usually a Teflon, Polystyrene or Mylar dielectric with typical capacitance value ranging from 0.001 to 10 μF is used.

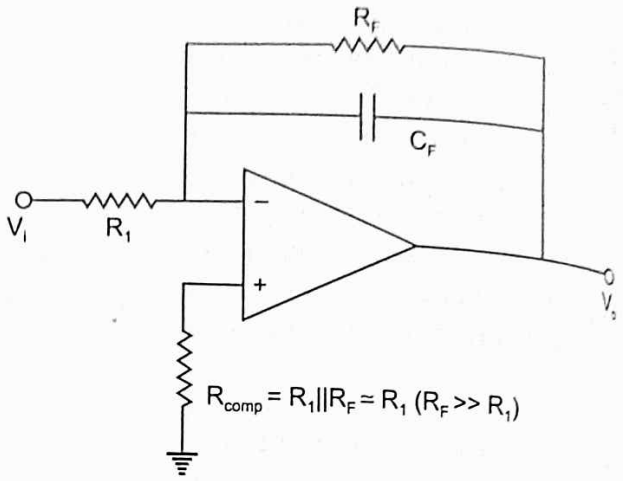


Fig. 4.39 (c) Practical or lossy integrator circuit

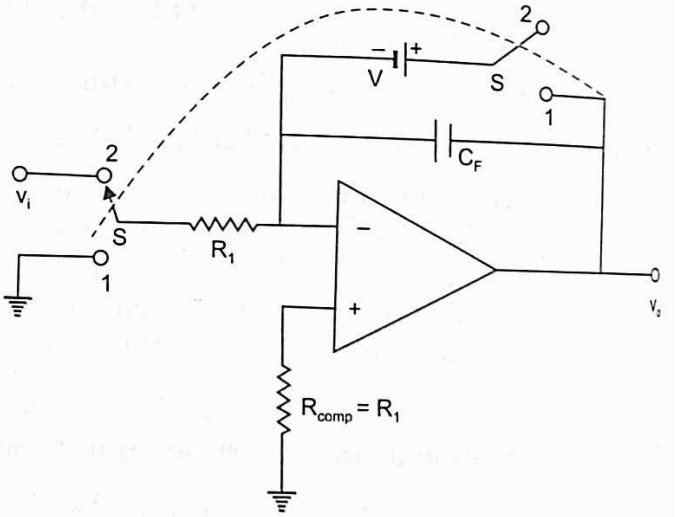


Fig. 4.40 Integrator circuit showing initial condition

Example 4.6

Consider the lossy integrator shown in Fig. 4.39 (c). For the component values. $R_1 = 10$ kΩ, $R_F = 100$ kΩ, $C_F = 10$ nF, determine the lower frequency limit of integration and study the response for the inputs (i) sine wave, (ii) step input (iii) square wave.

Solution

For the given component values, the lower frequency limit of integration f_a is

$$f_a = \frac{1}{2\pi R_F C_F} = \frac{1}{2\pi \times 100\ \text{k}\Omega \times 10\ \text{nF}} = 159\ \text{Hz}$$

For 99% accuracy, the input frequency should be at least one decade above f_a *i.e.*, 1.59 kHz. Accurate integration can be achieved beyond this frequency. However, there is an upper limit up to which circuit will integrate and it is determined by the frequency response of op-amp. However, as input frequency is increased, the output amplitude reduces as the gain of the integrator falls at a rate of 6 dB/octave.

(i) Sine wave input: For an input of 1 V peak sine wave at 5 kHz, the output v_o is

$$v_o(t) = -\frac{1}{R_1 C_F} \int v_i(t)\, dt = -\frac{1}{10\ \text{k}\Omega \times 10\ \text{nF}} \int 1 \sin (2\pi\ \ 5000\, t)\, dt$$

*In about four time constant, that is, 4 $R_o C_f$ where R_o is the small internal resistance of the voltage source V.

$$= -10^4 \int \sin(2\pi 5000 t)\, dt = -\frac{10^4}{2\pi\, 5000}\left[-\cos(2\pi 5000\, t)\right]$$

$$= 0.318 \cos(2\pi\ 5000\ t)$$

The output is a cosine wave with a peak amplitude of 0.318 V only as shown in Fig. 4.41 (a). If the frequency of the input is raised by a factor of 10 to 50 kHz, the output would be a cosine wave of frequency 50 kHz but with an amplitude of 31.8 mV only.

(ii) Step input: If input is a step voltage $v_i = 1$ V for $0 \le t \le 0.3$ ms, then the output voltage at $t = 0.3$ ms is

$$v_o = -\frac{1}{R_1 C_F}\int_0^{0.3\text{ ms}} 1.\, dt = -\frac{1}{10\ \text{k}\Omega \times 10\ \text{nF}} \times t\Big|_{t=0}^{t=0.3\text{ ms}}$$

$$= -10^4 \times 0.3 \times 10^{-3} = -3\ \text{V}$$

The output voltage is a ramp function with a slope of 10 V/ms and is shown in Fig. 4.25 (b).

(iii) Square wave input: The output waveform for an input of 5 KHz, 1 V peak square wave is shown in Fig. 4.41 (c).

It can be seen that input is of constant amplitude of 1 V from 0 to 0.1 ms and –1 V from 0.1 ms to 0.2 ms. The output for each of these half periods will be ramps as seen above for step inputs. Thus, the expected output wave form will be a triangular wave. The peak value of the output for first half cycle is

$$v_o = -\frac{1}{R_1 C_F}\int_0^{0.1\text{ ms}} 1.\, dt = -10^4 \times 0.1 \times 10^{-3} = -1\ \text{V}$$

This represents the total change in the output voltage over the first half cycle from 0 to 0.1 ms. Similarly, integration over the next half cycle produces a positive change of 1 V.

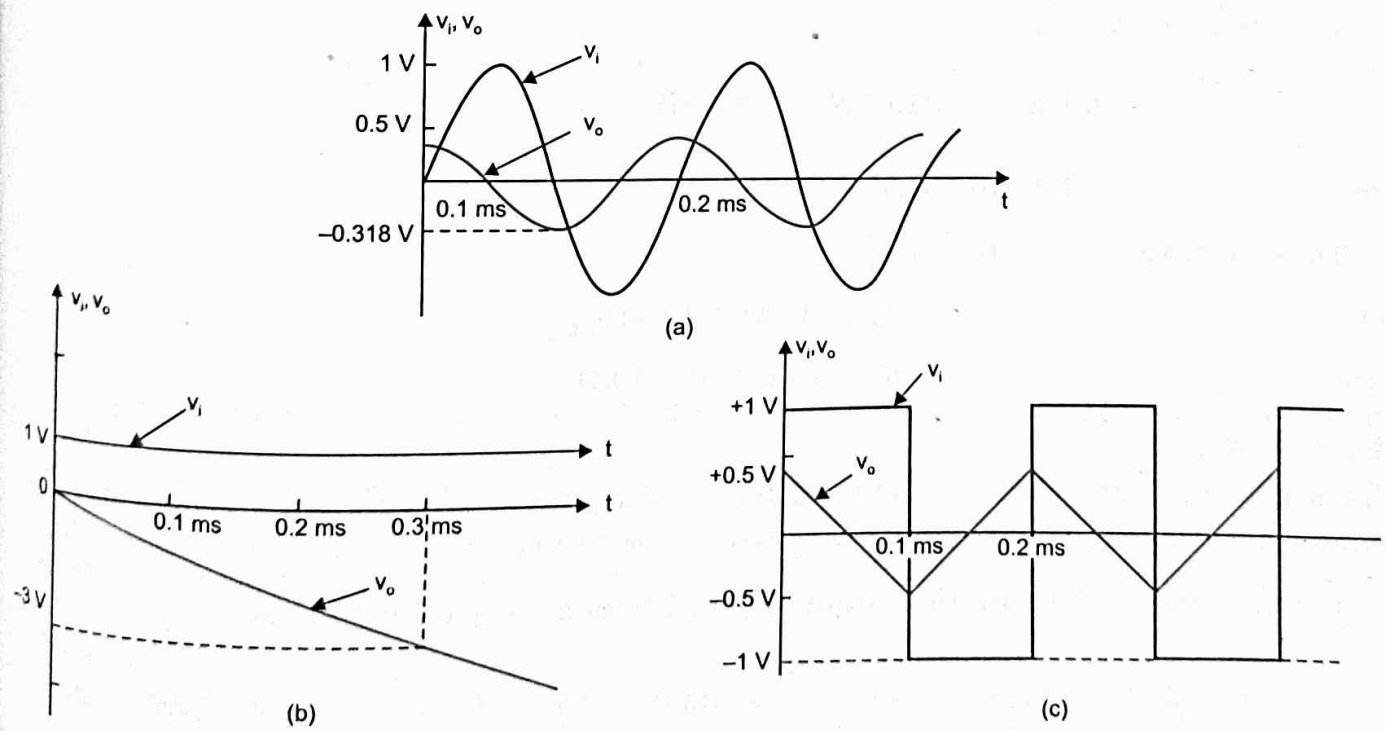


Fig. 4.41 Input and output waveforms for the integrator in Example 4.4
(a) Sine wave input, (b) Step input, (c) Square wave input

Example 4.7

Find R_1 and R_F in the lossy integrator so that the peak gain is 20 dB and the gain is 3 dB down from its peak when $\omega = 10{,}000$ rad/s. Use a capacitance of 0.01 μF.

Solution

From Eq. (4.120), we see that gain is at its peak when $\omega = 0$. The peak value in dB is therefore

$$A\,(\text{dB}) = 20 \log_{10} \frac{R_F/R_1}{\sqrt{1+0}} = 20 \qquad \text{(given)}$$

or, $$\log_{10} \frac{R_F}{R_1} = 1$$

Thus we have, $$\frac{R_F}{R_1} = 10$$

or, $$R_1 = \frac{R_F}{10}$$

At $\omega = 10^4$ rad/s, gain in dB is down by 3 dB from its peak of 20 dB, and thus is 17 dB. Therefore, converting gain to dB in Eq. (4.84) and substituting for ω, C and R_F/R, we have

$$20 \log_{10} \frac{10}{\sqrt{1+[(10^4)\,10^{-8}\,R_F]^2}} = 17 \text{ dB}$$

or, $$20 \log_{10} 10 - 20 \log_{10} \sqrt{1+(10^{-4}\,R_F)^2} = 17 \text{ dB}$$

This simplifies to

$$20 \log_{10} \left[1+(10^{-4}\,R_F)^2\right] = 3 \text{ dB}$$

or, $$1 + (10^{-4}\,R_F)^2 = 10^{3/10} = 2$$

Thus we have $$(10^{-4}\,R_F)^2 = 1$$

or, $$R_F = 10^4\ \Omega = 10\ \text{k}\Omega$$

and $$R_1 = 10\ \text{k}\Omega/10 = 1\ \text{k}\Omega$$

Example 4.8

Show that the output of an op-amp integrator to a step input of magnitude V volts is given by

$$v_o = A_v V(1 - e^{-t/R_1 C_F(1-A_V)})$$

Compare this result with the output obtained from a low pass RC circuit.

Solution

Figure 4.42 is a simple op-amp integrator where Miller's theorem is applied across the feedback capacitor C_F. The input time constant $T = R_1C_F(1 - A_v)$. Therefore,

$$v_i = V(1 - e^{-t/T}) \tag{4.122}$$

and $$v_o = A_v v_i = A_v V(1 - e^{-t/R_1C_F(1-A_v)}) \tag{4.123}$$

or, $$v_o = A_v V\left[1 - \left(1 - \frac{t}{R_1C_F(1-A_v)} - \frac{t^2}{2\left(R_1C_F(1-A_v)^2\right)} - \ldots\right)\right]$$

$$= \frac{A_v V t}{R_1C_F(1-A_v)}\left[1 - \frac{t}{2R_1C_F(1-A_v)} - \ldots.\right]$$

or, $$v_o \approx -\frac{Vt}{R_1C_F}\left[1 - \frac{t}{2R_1C_F(1-A_v)}\right];\ \text{if } A_v >> 1 \tag{4.124}$$

Also we know that for a simple low pass RC integrating network (without op-amp) the output v_o for a step input of V becomes

$$v_o = V(1 - e^{-t/RC}) \tag{4.125}$$

For large RC, $$v_o \approx \frac{Vt}{RC}\left(1 - \frac{t}{2RC}\right) \tag{4.126}$$

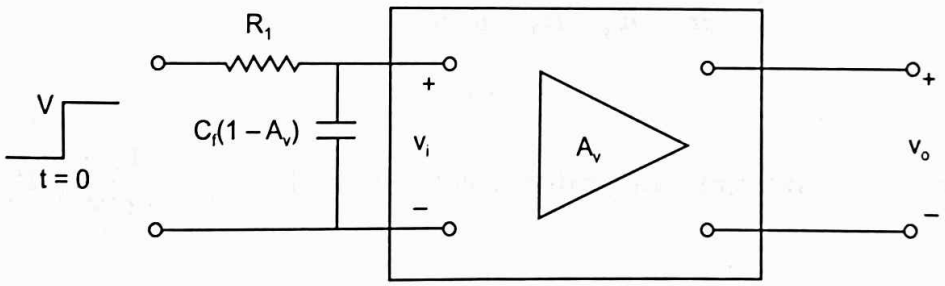


Fig. 4.42 Circuit for Example 4.6

It can be seen that the output voltage of both circuits varies approximately linearly with time (for a large RC) and for either case, $\frac{dv_o}{dt} = \frac{V}{RC}$. However, the second term in both the expressions represent deviation from the linearity. We see that op-amp integrator is more linear than the simple RC circuit by a factor of $1/(1 - A_v)$.

Example 4.9

For the circuit shown in Fig. 4.43 if the input is a constant V, show that the output $v_o(t)$ is given by a differential equation.

Solution

The transfer gain of the circuit is,

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_F}{R_1} = -\frac{R_2 + \dfrac{R_3/sC}{R_3 + 1/sC}}{R_1}$$

$$= \frac{(R_2 + R_3) + sC R_2 R_3}{R_1(1 + sC R_3)} \qquad (4.127)$$

or, $$R_1(1 + s\,C\,R_3)V_o(s) + [(R_2 + R_3) + sCR_2R_3]V_i(s) = 0 \qquad (4.128)$$

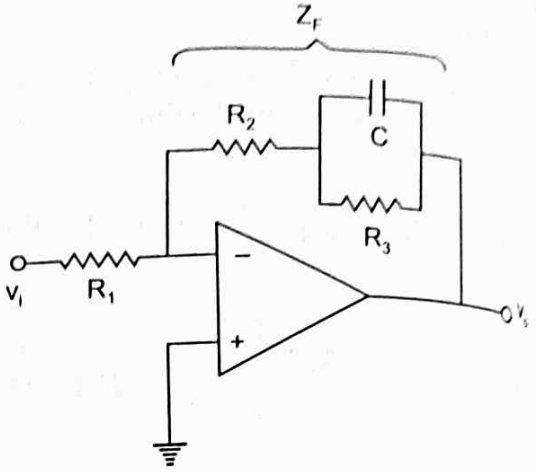


Fig. 4.43 Circuit for Example 4.7

Writing Eq. (4.128) in time domain $\left(s \to \dfrac{d}{dt}\right)$, we get

$$R_1\left(1 + CR_3\frac{d}{dt}\right)v_o(t) + \left[(R_2 + R_3) + CR_2R_3\frac{d}{dt}\right]v_i(t) \qquad (4.129)$$

Since $v_i(t) = V$

Therefore, $\dfrac{dv_i(t)}{dt} = 0.$

Hence $$CR_1R_3\frac{dv_o}{dt} + R_1v_o + (R_2 + R_3)V = 0$$

or, $$C\frac{dv_o}{dt} + \frac{v_o}{R_3} + \frac{V}{R_1} + \frac{R_2}{R_1R_3}V = 0 \qquad (4.130)$$

Example 4.10

Figure 4.44 shows a non-inverting integrator circuit. Show that $v_o = \dfrac{1}{RC}\int v_i\,dt.$

Solution

The voltage at the (+) input terminal of the op-amp due to the potential divider is,

$$V(+) = \frac{1/sC}{R + 1/sC}V_i(s) \qquad (4.131)$$

The output voltage $V_o(s)$ for the non-inverting amplifier is

$$V_o(s) = \left(1 + \frac{1/sC}{R}\right)V(+) = \frac{1}{sRC}V_i(s) \qquad (4.132)$$

Hence in time-domain, we get,

$$v_o = \frac{1}{RC}\int v_i\,dt.$$

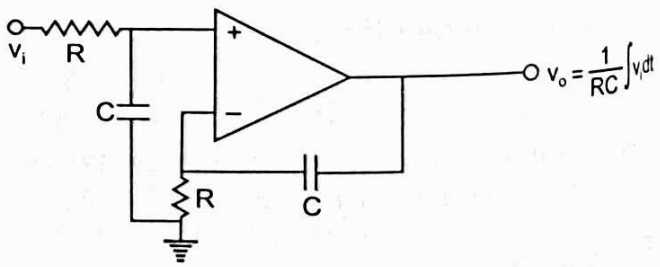


Fig. 4.44 Non-inverting integrator circuit

Note that there is no phase inversion in a non-inverting integrator.

4.12 ELECTRONIC ANALOG COMPUTATION

An analog computer performs linear operations such as multiplication by a constant, addition, subtraction and integration. Since these operations are sufficient for the solution of linear differential equation, it is possible to connect the various modules of an analog computer for obtaining the solution of differential equation.

We have already discussed the building blocks of the analog computer, that is, op-amp used as inverter, scale changer, summer, integrator, summing integrator etc. Potentiometer is widely used in analog computer to multiply voltages by a constant less than unity. The symbolic representation of a summer, potentiometer and summing integrator is shown in Fig. 4.45 (a, b, c).

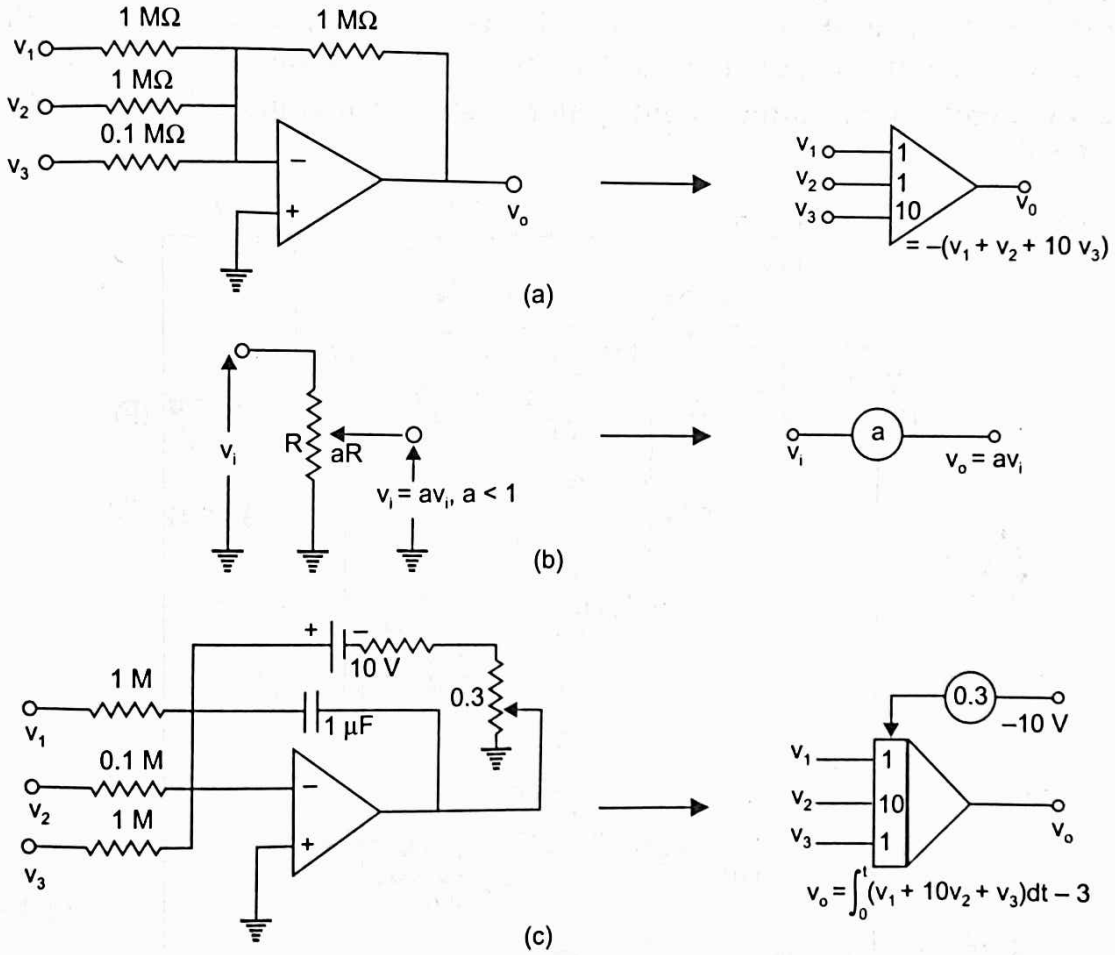


Fig. 4.45 (a) Summer and its symbolic representation, (b) Potentiometer and its symbol, (c) Summing integrator and its symbol

Let us now see how an analog computer can be used to solve a second order differential equation given as,

$$\frac{d^2y}{dt^2} + 5.4\frac{dy}{dt} + 0.58\, y = u(t) \tag{4.133}$$

with initial conditions,

$$y(0) = -4.8 \text{ and } \left.\frac{dy}{dt}\right|_{t=0} = \dot{y}(0) = 2.3$$

Rewrite Eq. (4.133) by keeping the highest order derivative on the left hand side and taking all other terms to the right side as

$$\ddot{y} = -5.4\,\dot{y} - 0.58\,y + u(t) \tag{4.134}$$

Assuming $\ddot{y}$ is available, it may be successively integrated to obtain $\dot{y}$ and y as shown in Fig. 4.46 (a). At the output of amplifier 4, *i.e.*, point B, we obtain the sum

$$-5.4\,\dot{y} - 0.58y + u(t)$$

which is precisely equal to $\ddot{y}$ with which we started in Eq. (4.134). Thus points A and B may be connected together to get the computer set-up for solving the given differential equation. The initial conditions $y(0) = -4.8$ and $\dot{y}(0) = 2.3$ have to be placed in the computer set-up with the help of the reference voltage (either $+V_{ref}$ or $-V_{ref}$ as required) and potentiometer. One has to be careful about the polarity of the reference voltage for setting up the initial condition. As in the computer set-up, the output of integrator 1 is $-\dot{y}$ which is initially set to -2.3 V to achieve $\dot{y}(0) = 2.3$ V. Similarly the output of integrator 2 is y which is initially set to -4.8 V so that $y(0) = -4.8$ V.

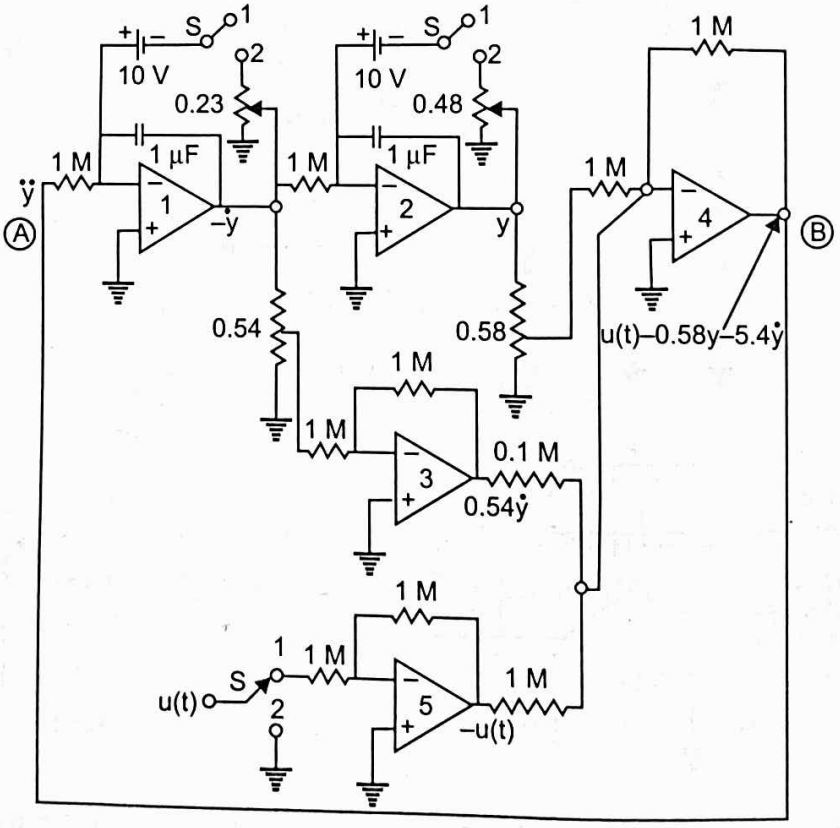


Fig. 4.46 (a) Simulation of 2nd order differential equation

The initial conditions are first established by putting the switch S in position 2. With S in position 1, the solution is obtained at the output terminal to which a CRO or plotter is connected.

Using the analog computer symbols, the set-up of Fig. 4.46 (a) is redrawn in Fig. 4.46 (b). Minimization of the components can be achieved using a summer integrator as shown in Fig. 4.46 (c).

The solution of Eq. (4.133) can also be obtained by using differentiators instead of integrators. However, the gain of a differentiator increases linearly with frequency and it tends to

amplify noise, drift which may result in spurious oscillations. Therefore, integrators are invariably preferred over differentiators.

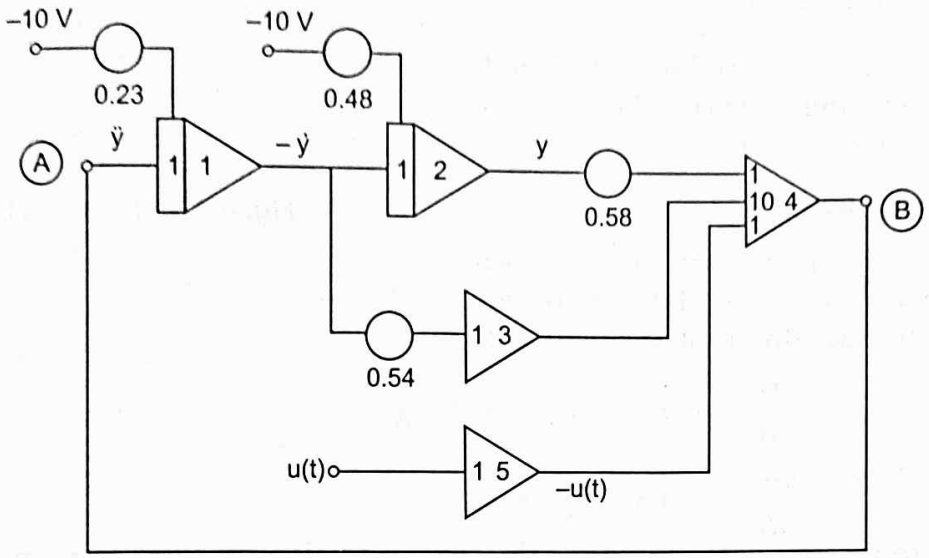


Fig. 4.46 (b) Symbolic diagram

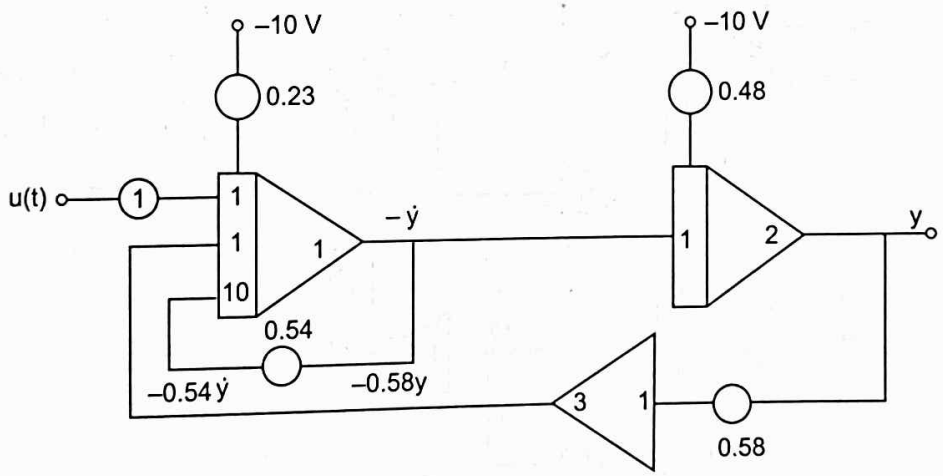


Fig. 4.46 (c) Minimum component simulation

Example 4.11

Set up an analog computer simulation to generate a sinusoidal signal 10 sin $3t$.

Solution

Let us first obtain a differential equation whose solution is 10 sin $3t$.

Let
$$x(t) = 10 \sin 3t$$
$$\dot{x}(t) = 30 \cos 3t \tag{4.135}$$
$$\ddot{x}(t) = -90 \sin 3t = -9x$$

The required differential equation is,

$$\ddot{x} + 9x = 0$$

and the initial conditions are obtained from Eq. (4.135) putting $t = 0$ as,

$$x(0) = 0,\ \dot{x}(0) = 30$$

Assuming that $\ddot{x}$ is available, $x(t)$ can be obtained by integrating x twice. The computer set up is shown in Fig. 4.47.

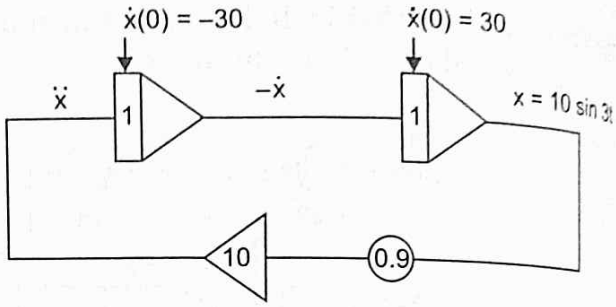


Fig. 4.47 Simulation of 10 sin 3t

Simultaneous Equations

A set of simultaneous equations in two unknowns can also be solved using analog simulation. Consider two first order differential equations:

$$\frac{dx}{dt} = -a_1 x - b_1 y + c_1 f \tag{4.136}$$

and

$$\frac{dy}{dt} = -a_2 x - b_2 y + c_2 f \tag{4.137}$$

where x and y are unknown variables, f is the input and all coefficients are known constants. Equations (4.136) and (4.137) may be simulated separately as shown in Figs. 4.48 (a) and (b). Now interconnect the two systems to get the unknown x and y as shown in Fig. 4.48 (c).

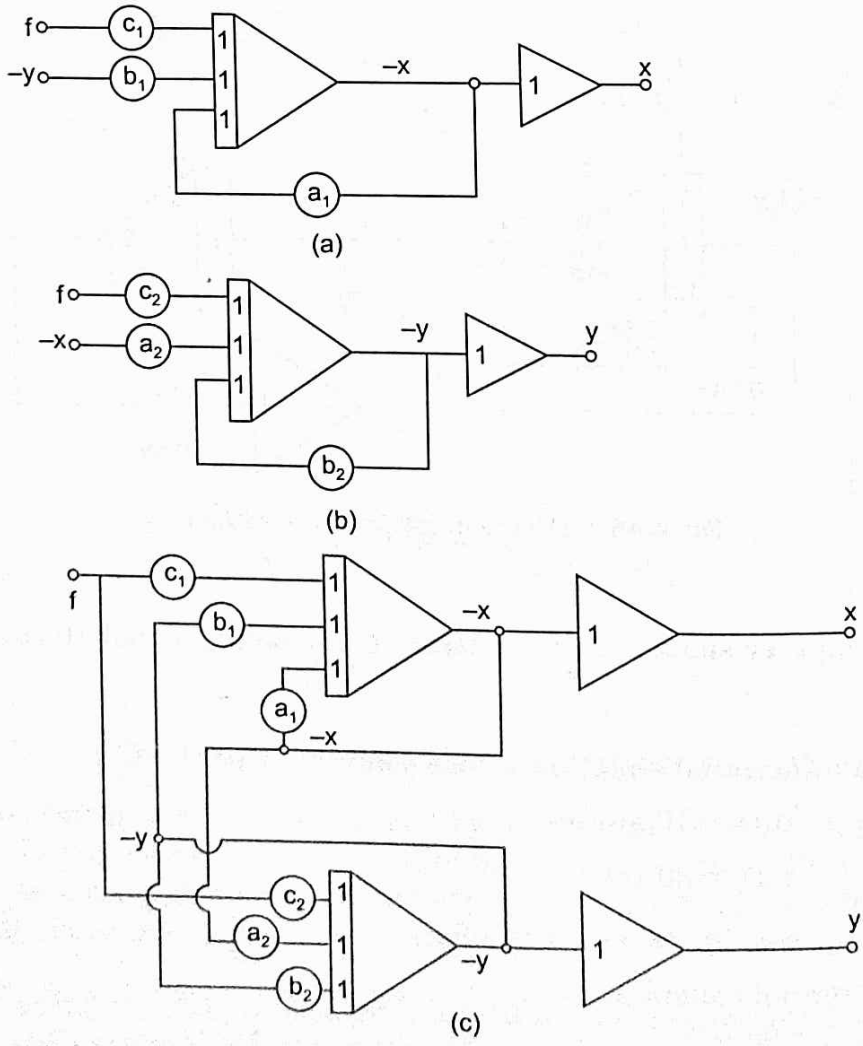


Fig. 4.48 (a) Simulation of Eq. (4.136), (b) Simulation of Eq. (4.137), (c) Final circuit

The simulation procedure can be extended to any number of simultaneous equations.

Simulation of Transfer Functions

Another important problem that one come across is to develop a circuit that has a given transfer function. As an example, in the design of an electric filter consider a first order transfer function.

$$H(s) = \frac{V_o}{V_i} = \frac{-K}{s+a} \tag{4.138}$$

so, $$V_o(s + a) = -KV_i$$

or, $$-sV_o = aV_o + KV_i \tag{4.139}$$

which may be written in time-domain as,

$$v_o = -\int (av_o + Kv_i)\,dt \tag{4.140}$$

Thus we need a summing integrator and its simulation is shown in Fig. 4.49 (a). The corresponding electric circuit is shown in Fig. 4.49 (b).

In another example, let us simulate the transfer function

$$\frac{V_o}{V_i} = \frac{K(s+a)}{s^2 + sb + c} \tag{4.141}$$

which may be written in s-domain as,

$$s^2 V_o = -sbV_o - cV_o + KsV_i + KaV_i$$

or $$-sV_o = bV_o - KV_i - \frac{1}{s}(KaV_i - cV_o) \tag{4.142}$$

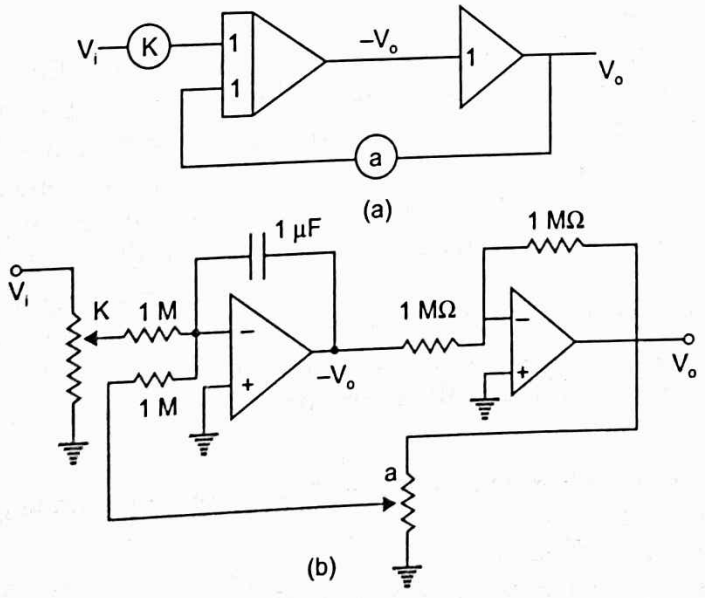


Fig. 4.49 (a) Simulation of transfer function $H(s) = -\frac{K}{s+a}$, (b) Electric circuit for (a)

Thus V_o is the output of an integrator whose input is $-sV_o$ which is the sum of the terms on the right side of Eq. (4.142). The term $-\frac{1}{s}(KaV_i - cV_o)$ is the output of an integrator

whose inputs are KaV_i and $-cV_o$ as shown in Fig. 4.50 (a). The complete circuit is shown in Fig. 4.50 (b).

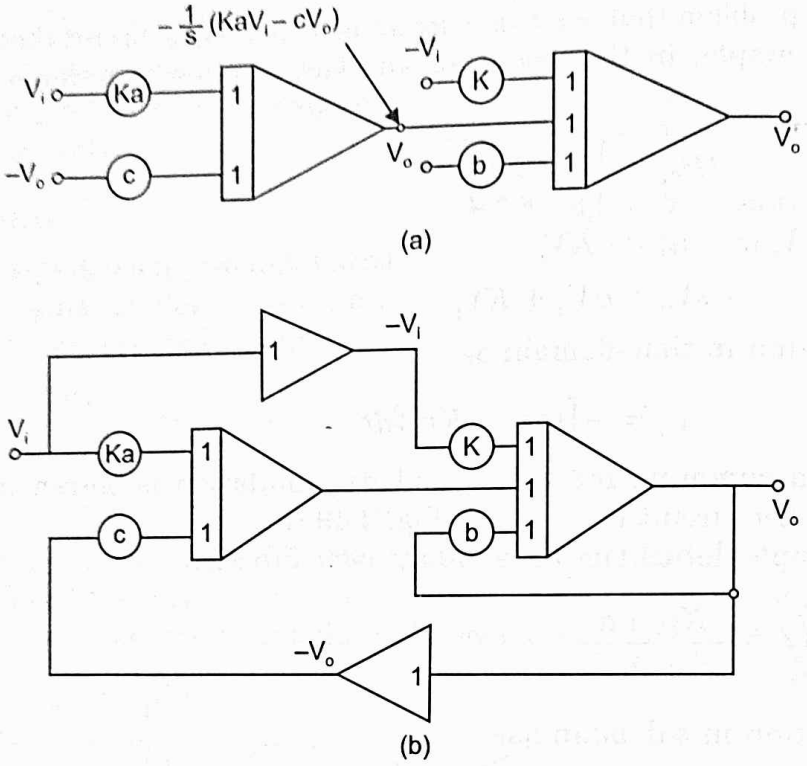


Fig. 4.50 (a) Preliminary simulation, (b) Final simulation

4.13 POWER AMPLIFIERS

Most of the practical electronic systems consist of a number of amplifying stages in cacade. The function of the input and intermediate stages is to amplify the small signals received from an input source, such as from a cassette, CD, microphone or an antenna. The signal is amplified to a large value sufficient to drive the final device which may be a speaker in a public address system or a music system or a CRT or a servomotor etc. The input amplifying stages basically operate as voltage amplifiers. Since signal voltages and currents are small, the power handling capacity and power efficiency are of little concern for the small signal amplifiers.

The last stage or the output stage of any electronic system, however has to supply large current and sufficient power to the load which may be a loudspeaker or a servomotor. Such amplifiers are called large signal amplifiers or power amplifiers. The important requirements of a power amplifier are:

1. It should have low output impedance so as to provide impedance matching for maximum power transfer.
2. High power conversion efficiency.
3. As large amount of power gets dissipated at the junction of power transistor, heat sinks have to be used.

Classification of Output Stages

One way of classifying amplifiers is based upon the position of quiescent (Q) point on the load line and the shape of the output collector current waveform when a sinusoidal input signal is

applied. The Q-point of the BJT need not necessarily be in the middle of the load line. Depending upon the position of the Q-point, amplifiers may be classified as class-A, class-B, class-AB or class-C as per the following definitions.

Class A

The operating point is chosen somewhere in the center of the load line as shown by point A in Fig. 4.51. The amplitude of the input signal is such so that the transistor conducts for the entire cycle of the input signal that is for 360°. The output collector current waveform for class-A amplifier is therefore as shown in Fig. 4.52 (a).

The input stage or intermediate stages of any electronic system are operated in class-A operation.

Class B

The Q-point is selected at the extreme end of the load line as shown by point B in Fig. 4.51. The quiescent current is, therefore, zero and the transistor conducts only for half the cycle of the input waveform. The output collector current consists of half waves only as shown in Fig. 4.52 (b). Obviously, the output is not a faithful reproduction of the input as only half cycle is present in the output. In a practical circuit, two transistors are operated in class-B in such a manner so that one transistor conducts during positive half cycle of the input waveform and the other conducts during the negative half cycle so that the output current through the load is of full cycle. This type of connection is referred to as push-pull operation and is most commonly used in power amplifiers.

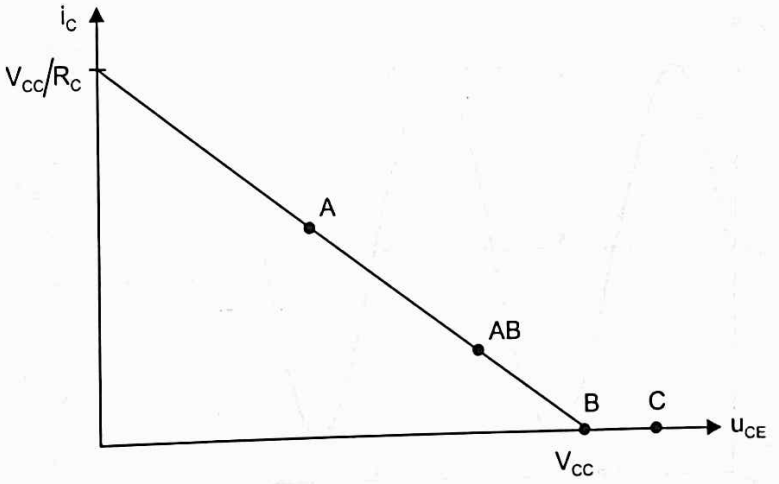


Fig. 4.51 Classification of amplifiers based on the position of Q-point

Class AB

An intermediate operation between class A and class B is class AB in which the operating point is selected between the points A and B in Fig. 4.51 as shown by point AB. As a result, the transistor conducts for an internal greater than the half cycle but less than 360°. The output collector current waveform is as shown in Fig. 4.52 (c).

Class C

The operating point is selected beyond the load line on the horizontal axis as shown by point C in Fig. 4.51. The transistor in this case conducts for an interval lesser than the half cycle resulting in pulsating current waveforms as shown in Fig. 4.52 (d). Class C amplifiers are usually employed in radio frequency (RF) power amplification (such as in mobile phones, radio and TV transmitters). These type of amplifiers have not been included in the book.

Power Conversion Efficiency (η)

An amplifier is basically converting dc power/energy supplied by the dc power supply into ac power or amplified signal at the load. The ability of an active device to connect dc power into

ac power is measured by η called the power conversion efficiency. It is usually given as a percentage, so

$$\eta = \frac{\text{ac signal power delivered to load}}{\text{dc power supplied to the circuit}} \times 100\%$$

The maximum power conversion efficiency of a class-A single stage CE amplifier is only 25%. In many practical applications, such as a radio or public address system, the load is a loudspeaker and is coupled to the amplifier through a transformer. The maximum efficiency for a transformer coupled load increases to 50%. Efficiencies up to 78.5% can be achieved by using two transistors in push-pull configuration and biasing each transistor in class-B operation. In discrete circuits, a center-tapped input transformer is used for providing signals to the two transistors. Similarly the output is obtained using a center-tapped output transformer.

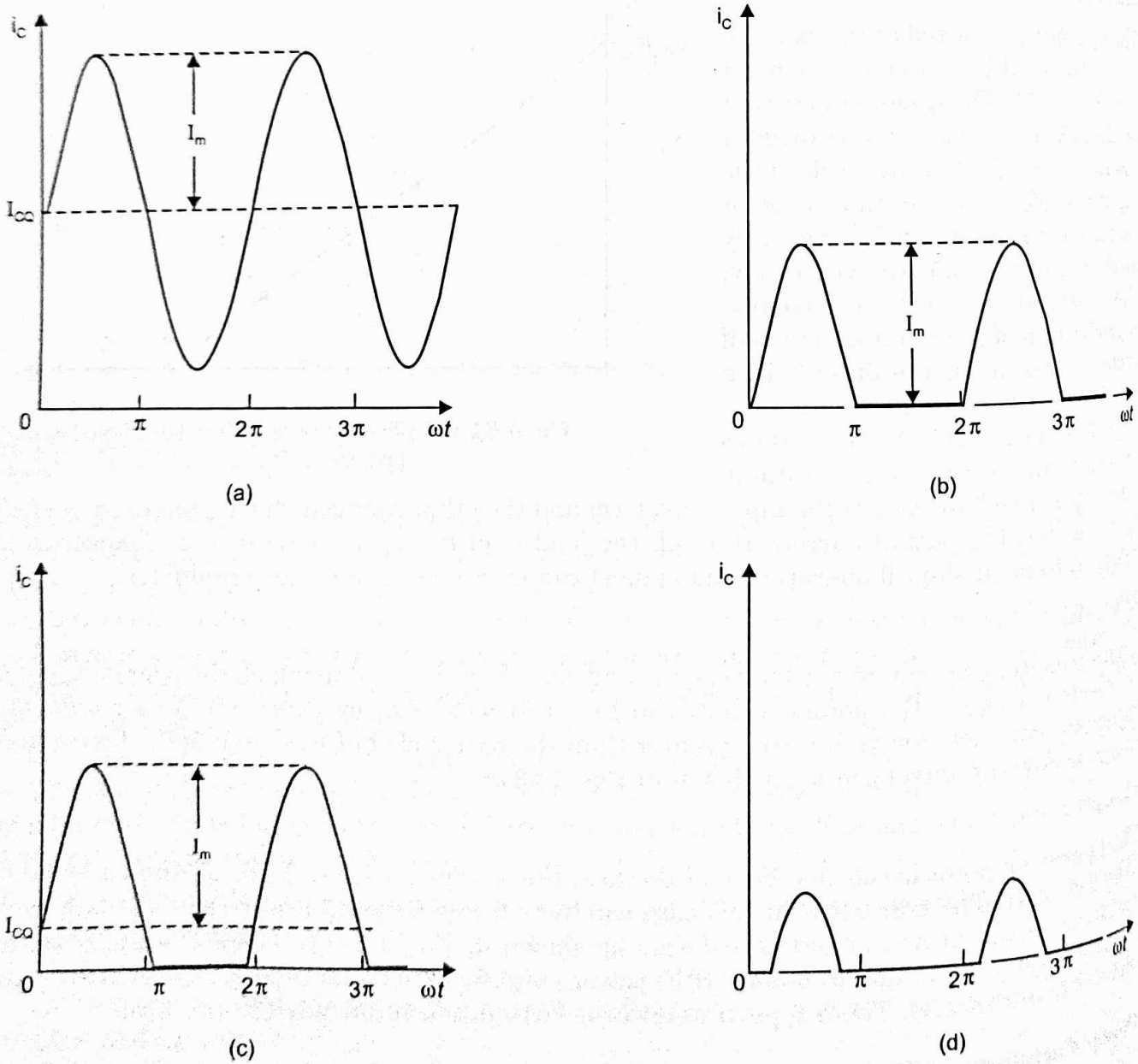


Fig. 4.52 Collector current waveforms for transistors operating in (a) Class A, (b) Class B, (c) Class AB, and (d) Class C amplifier stages

In IC amplifer circuits, use of transformers is not possible as it is difficult to fabricate these. The output stage of a commercially available 741 op-amp uses a complementary symmetry class-B. Push Pull amplifier which is discussed now.

Class-B Push Pull amplifier

Figure 4.53 shows a class-B push pull amplifier. It consists of complementary pair of transistors (an *npn* and a *pnp*) biased in class-B operation. Thus, both the transistors can not conduct simultaneously.

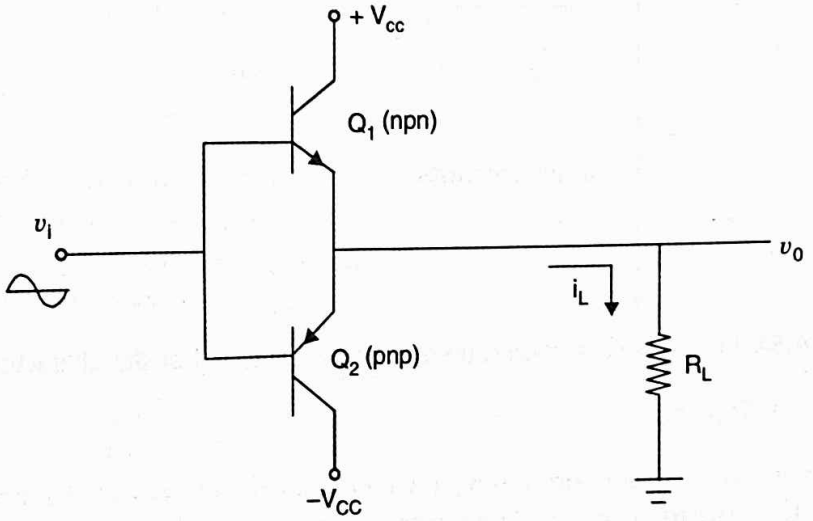


Fig. 4.53 Complementary symmetry class-B Push-Pull amplifier

When the input voltage V_i is zero, both the transistors are cut-off and the output voltage, V_0 is zero. As V_i exceeds the cut-in voltage $V_\gamma = 0.5$ V during the positive half cycle, Q_1 conducts and operates as an emitter follower. Thus V_0 follows V_i and Q_1 supplies the load current. During this time, the emitter-base junction of Q_2 will be reverse-biased and remains in cut-off state.

During the negative half cycle of input signal, V_i, Q_1 turns off and Q_2 starts conducting as soon as V_i is less than 0.5 V. Again V_0 follows V_i and now Q_2 supplies the load current.

This circuit thus operates in a push-pull fashion i.e. Q_1 pushes (sources) current into the load when V_i is positive and Q_2 pulls (sinks) current from the load when V_i is negative.

The transfer characteristics of the class-B push pull amplifier are shown in Fig. 4.38. Note that there is a range of V_i centered around zero where both transistors are cut-off and V_0 is zero. This *dead band* gives rise to *crossover distortion*. Crossover distortion is the cause of producing unpleasant sounds in audio power amplifiers.

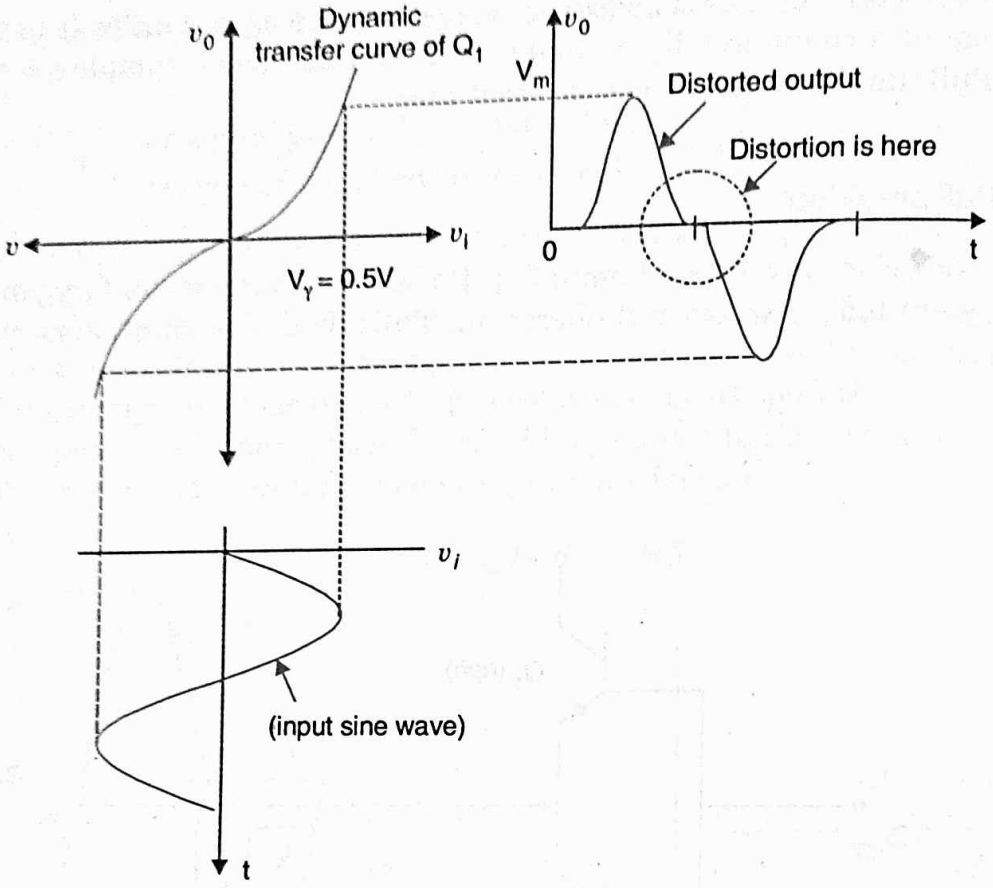


Fig. 4.54 Cross-over distortion caused by non-linearity of transfer characteristics

Power Conversion Efficiency η

To calculate the power conversion efficiency, η, we neglect the crossover distortion. Let V_m be the peak amplitude of the output sinusoid. The average power available at the load is

$$P_L = P_{ac} = \frac{1}{2}\frac{V_m^2}{R_L} \tag{4.143}$$

The current drawn from each supply will consist of half-sine waves of peak amplitude. $I_m = V_m/R_L$. Thus, the average current drawn from each of the two power supplies will be $V_m/\pi R_L$. The total dc current drawn from two power supplies will be twice this value.

Thus, the total dc power supplied is

$$P_{dc} = \frac{2}{\pi}\frac{V_m}{R_L}V_{CC} \tag{4.144}$$

The power conversion efficiency, η is given by

$$\eta = \left(\frac{1}{2}\frac{V_m^2}{R_L}\right)\Big/\left(\frac{2}{\pi}\frac{V_m}{R_L}V_{CC}\right)$$

$$= \frac{\pi}{4}\frac{V_m}{V_{CC}} \tag{4.145}$$

The maximum efficiency is obtained when V_m is at its maximum. The maximum output voltage is limited to $V_{CC} - V_{CE,\,sat} \simeq V_{CC}$

At this peak output voltage, the power conversion efficiency is obtained as

$$\eta_{max} = \frac{\pi}{4} = 78.5\% \tag{4.146}$$

Thus, the power conversion efficiency of a class-B, Push Pull amplifier is much larger than that can be obtained by class A amplifier (25%) stage. Therefore, the output stage of 741 ap-amp is always a class-B Push Pull amplifier.

There is one more parameter of interest in power amplifiers. What happens to the power which is not delivered to load as ac power output? Obviously this power is dissipated across the transistors as heat. A class-A stage dissipates maximum power under quiescent conditions (i.e. when $V_i = 0$) whereas, the quiescent power dissipation of a class B stage is zero. When an input signal is applied, the average power dissipated in the class B stage is given by

$$P_D = P_{dc} - P_{ac} \tag{4.147}$$

Substituting the values of P_{dc} and P_{ac} from (4.143) and (4.144), we get

$$P_D = \frac{2}{\pi}\frac{V_m}{R_L}V_{CC} - \frac{1}{2}\frac{V_m^2}{R_L} \tag{4.148}$$

A plot of power dissipation P_D vs amplitude of the output sinusoid V_m is shown in Fig. 4.39. It can be seen that the dissipation is zero for $V_m = 0$ and increases as V_m increases and there is a value of V_m for which dissipation is maximum. The maximum power dissipation can be computed by differentiating Eq. (4.148) w.r.t. V_m and equating it to zero, i.e.

$$\frac{dP_D}{dV_m} = \frac{2V_{CC}}{\pi R_L} - \frac{2V_m}{2R_L} = 0$$

or
$$\frac{2V_{CC}}{\pi R_L} = \frac{V_m}{R_L}$$

or
$$V_m = \frac{2V_{CC}}{\pi} \tag{4.149}$$

Putting this value of V_m in Eq. (4.148), we get the maximum power dissipation as,

$$P_{D,max} = \frac{2V_{CC}^2}{\pi^2 R_L} \tag{4.150}$$

The efficiency η, at this value of V_m is obtained as

$$\begin{aligned}\eta &= \frac{P_{ac}}{P_{dc}} \times 100 \\ &= \frac{\pi}{4}\frac{V_m}{V_{CC}} \times 100\% \\ &= \frac{\pi}{4}\frac{2V_{CC}}{\pi V_{CC}} \\ &= 50\%\end{aligned} \tag{4.151}$$

It can be seen from Fig. 4.55 that as V_m increases beyond $2V_{cc}/\pi$, the power dissipated decreases and the efficiency increases to 78.5%. However, the non-linear distortion increases as we go towards saturation which will flatten or clip the output waveform.

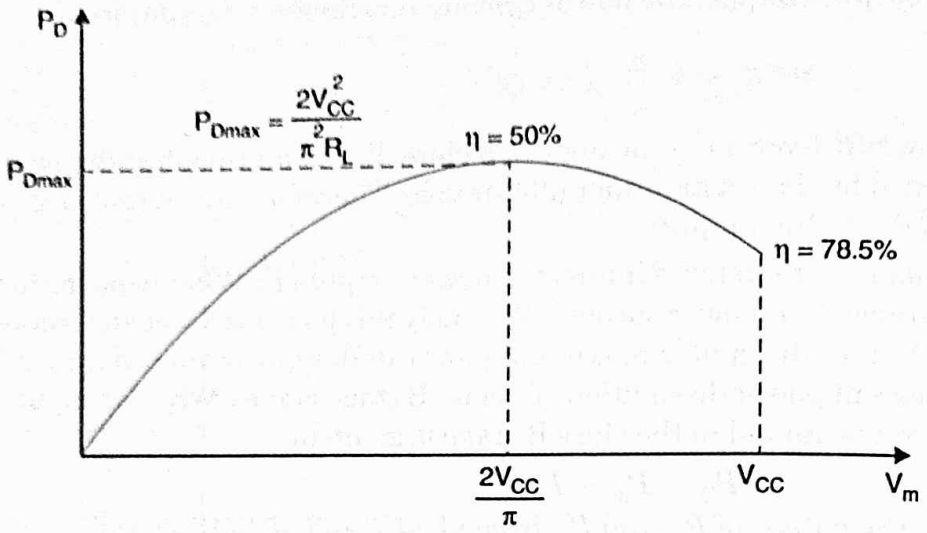


Fig. 4.55 Power dissipation of a class B output stage versus amplitude of the output sinusoid

Reducing Cross-over Distortion Using Class AB Operation

Although class-B Push Pull amplifier can provide high efficiency but the output waveform is distorted due to the non-linearity of the input characteristics. The base current starts flowing only after the base emitter junction is forward-biased by a voltage greater than the cut-in voltage V_γ. This cross-over distortion can be virtually eliminated by operating the complementary transistors Q_1 and Q_2 in class AB operation as shown in Fig. 4.56. A bias voltage V_{BB} is applied between the bases of Q_1 and Q_2. For $v_i = 0$, $V_0 = 0$ and a voltage $V_{BB/2}$ appears across the base emitter junction of each transistors Q_1 and Q_2. The value of $V_{BB}/2$ should be greater than V_γ the cut-in voltage. Another commonly used technique is to connect two diodes in series as shown in Fig. 4.56 (b).

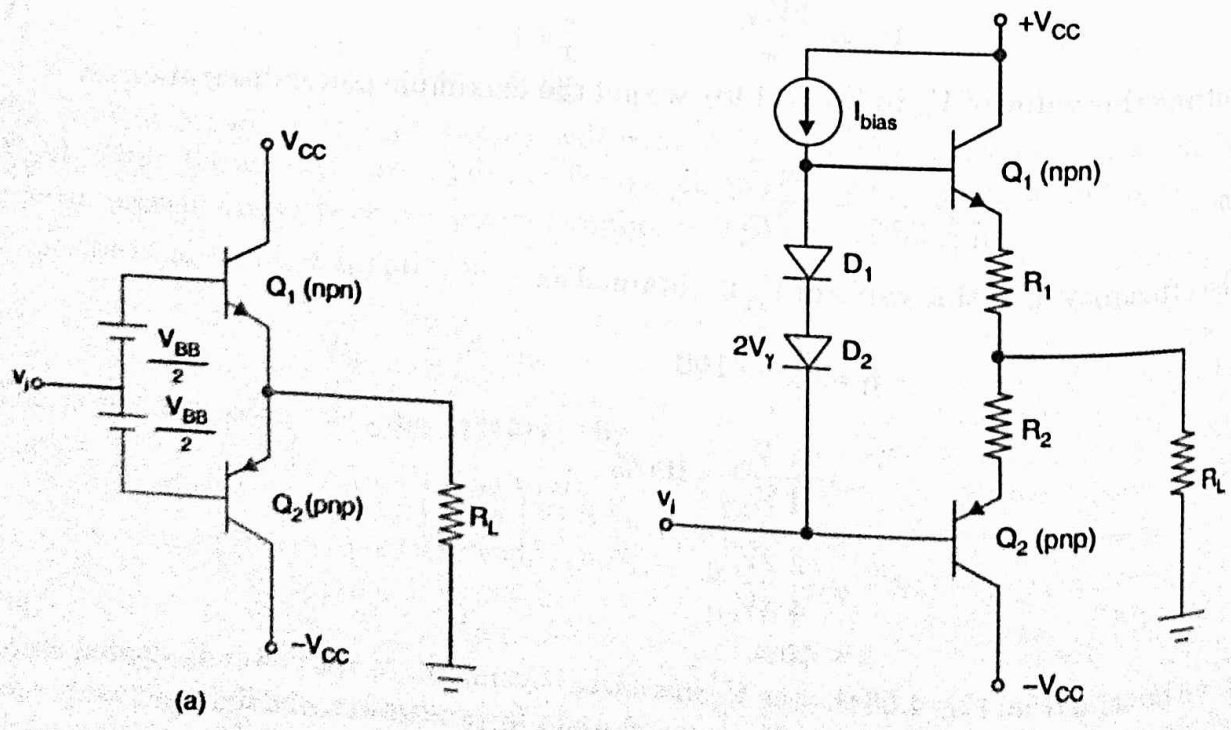


Fig. 4.56 Elimination of crossover distortion by (a) use of voltage source V_{BB} (b) use of diodes

Monolithic Power Amplifiers

The general purpose op-amp 741 can deliver about 100 mW of power which is not sufficient for most of the applications. A wide range of IC power amplifiers are now commercially available. National Semiconductors produces two popular IC power amplifiers LM380 and LM384. The pin configuration, circuit diagram and typical applications are discussed.

LM380 Power Audio Amplifiers

The LM380 power audio amplifier is designed to deliver 2.5W (r.m.s) to a capacitively coupled 8-Ω load. Figures 4.57 (a) and (b) shows the pin configuration and block diagram of LM380 respectively. It is available in a 14-pin DIP package. A copper lead frame used with the center three pins on either side (3, 4, 5 on the left and 10, 11, 12 on the right) forms a heat sink. Thus there is no need to use a separate heat sink for the audio amplifier. The internal schematic diagram of LM380 is shown in Fig. 4.57 (c).

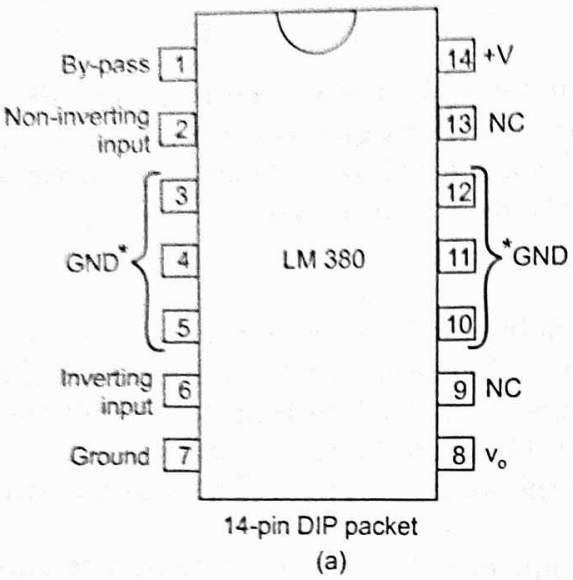
It can be seen that it has four stages: (i) PNP emitter follower; (ii) differential amplifier (iii) common emitter and (iv) quasi-complementary emitter follower.

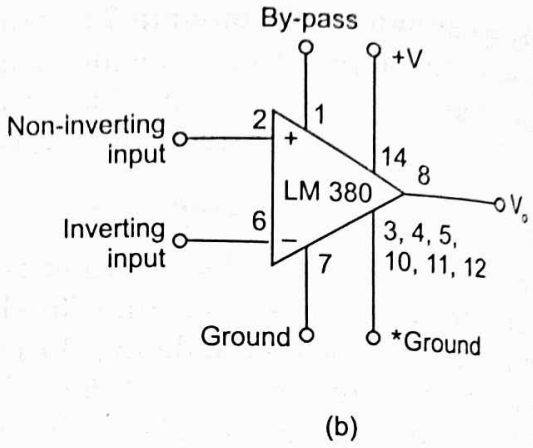
The input is coupled through inverting input terminal (pin-6) and non-inverting input terminal (pin-2) to emitter follower stages composed of PNP input transistors Q_1 and Q_2. The output from Q_1 and Q_2 drives the PNP Q_3–Q_4 differential pair. Transistors Q_5 and Q_6 constitute the collector loads for the PNP differential pair. The current in the PNP differential pair Q_3–Q_4 is established by Q_7, R_3 and V_{CC}. The transistors Q_7 and Q_8 form the current mirror and establish current in Q_9 which forms the common emitter voltage gain stage. The output of the differential pair Q_3–Q_4 is taken at the junction of Q_4 and Q_6 and is applied as input to CE voltage gain stage. The capacitor C (10 pF) between base and collector of Q_9 provides internal compensation and establishes the upper cut-off frequency of 100 kHz at 2W for 8Ω loads. As Q_7-Q_8 form a current mirror, the current through diodes D_1 and D_2 is same as that through R_3. The output stage is a quasi (false)–complementary pair emitter follower formed by transistors Q_{10} and Q_{12}. In fact, the combination of PNP transistor Q_{11} and NPN transistor Q_{12} has the power capability of an NPN transistor but the characteristics of a PNP transistor. The diodes D_1 and D_2 are used to minimize cross-over distortion. The resistors R_6 and R_7 are used for current limiting. The quiescent output voltage is established at $V_{CC}/2$ by resistors R_3 and R_5. To decouple the input stages from the supply voltage V_{CC}, a by-pass capacitor of the order of micro farads should be connected between the by-pass terminal (pin 1) and ground (pin 7).

Some of the important features of LM380 are listed below:

(i) Internally fixed gain of 50 (34 dB)
(ii) Wide supply voltage range (5 V to 22 V)
(iii) High peak current capability (1.3 A max.)
(iv) Low total harmonic distortion (0.2%)
(v) Output automatically self-centering to one-half of the supply voltage
(vi) Output short circuit proof with internal thermal limiting
(vii) High input impedance (15° kΩ)
(viii) BW of 100 kHz at an output power of 2W and a load of 8Ω.

Another commonly used audio power amplifier is LM384. The internal diagram is similar to that of LM380, except that it is designed to deliver 5W power output.





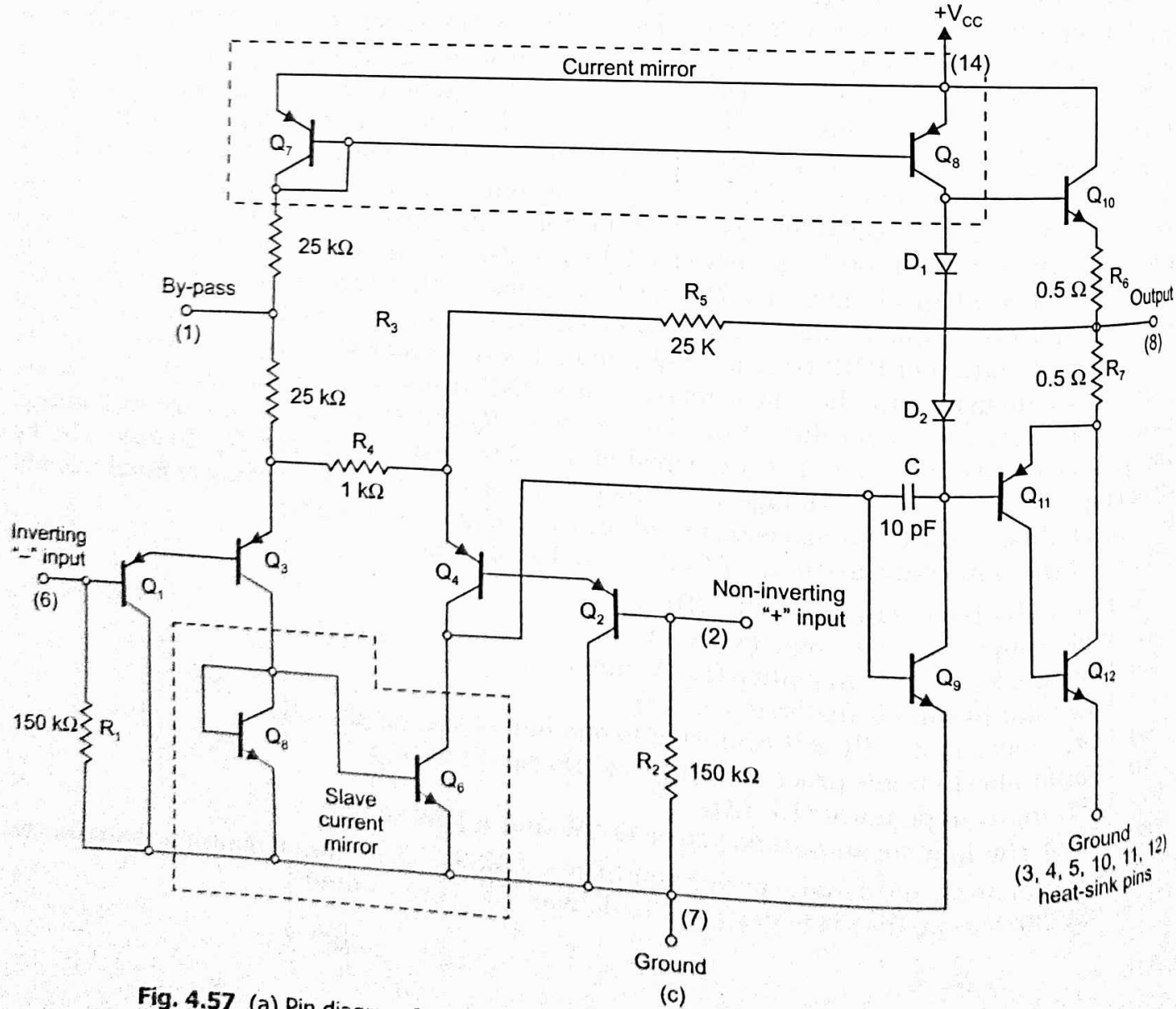


Fig. 4.57 (a) Pin diagram for LM380, (b) Block diagram, (c) Internal Schematic diagram

Applications

The most basic application of LM380 is its use as an audio power amplifier. The IC can be used both in inverting and non-inverting configuration. Figure 4.58 (a) shows its use in non-inverting mode. The inverting terminal (pin 6) can be either started to ground, left open or returned to ground through a resistor or a capacitor. The capacitor C_2 is used to cancel the effects of inductance in the power supply leads. A lag compensating RC network is usually used at the output terminal (pin 8) to eliminate 5 to 10 MHz oscillations especially in RF sensitive environment.

The gain of LM380 is internally fixed at 50 but it is possible to get the gain increased up to 300 using positive feedback. Figure 4.58 (b) shows LM380 used in the inverting configuration using positive feedback to increase the gain.

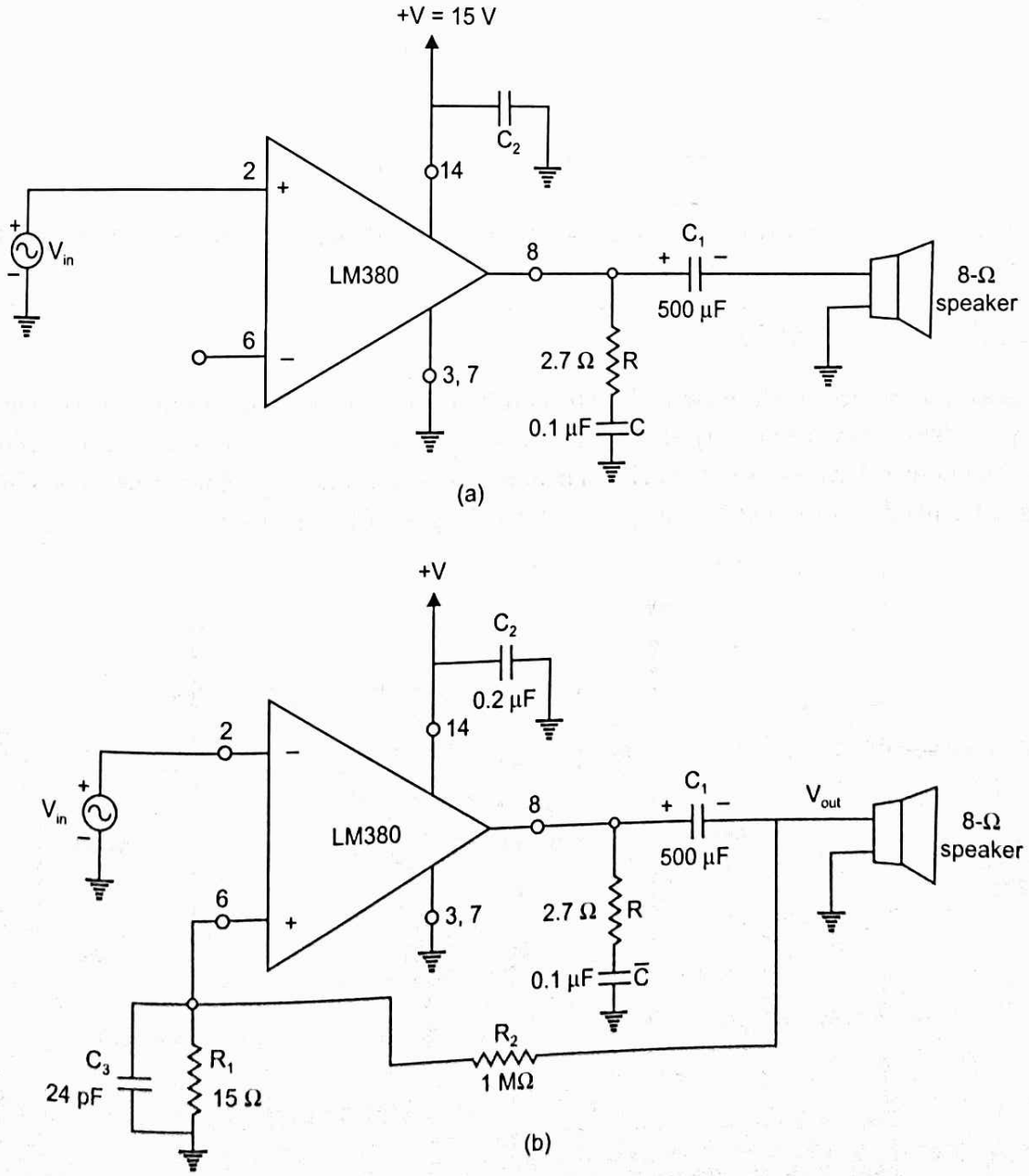


Fig. 4.58 (a) Audio power amplifier using LM380 (b) Use of positive feedback to increase gain

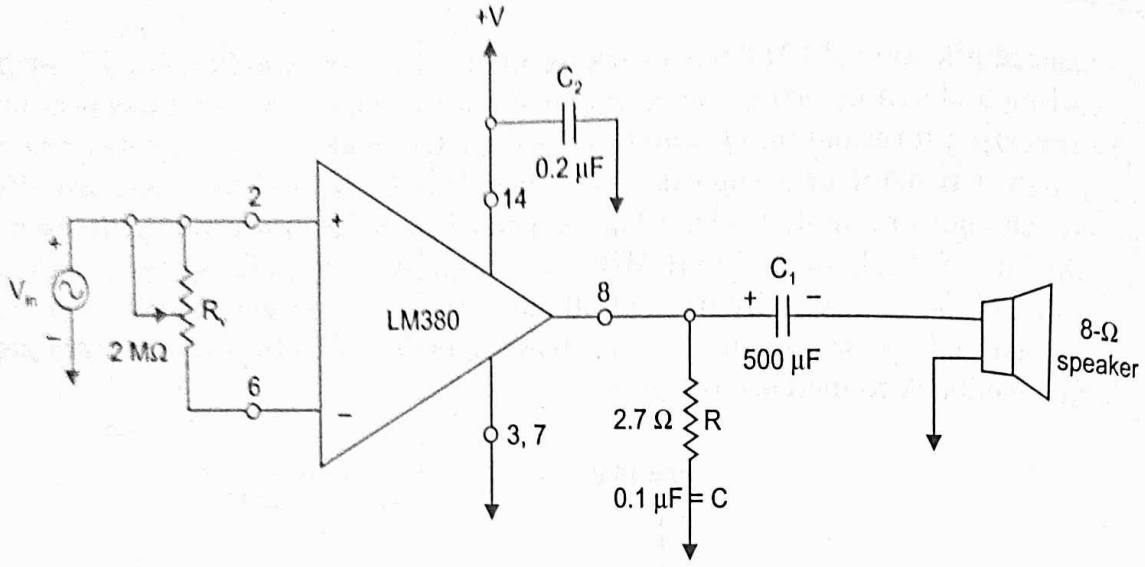


Fig. 4.59 Audio power amplifier with variable gain

It is also possible to obtain variable gains up to 50 by using a potentiometer across the two input terminals as shown in Fig. 4.59.

Bridge Power Audio Amplifier

If more power is required than two LM380s can be used in the bridge configuration as shown in Fig. 4.60. The maximum output voltage swing will be twice that of a single LM380 and therefore the power delivered to the load will be four times. For better performance, a potentiometer R_V should be used to balance the output offset voltages of the LM380s.

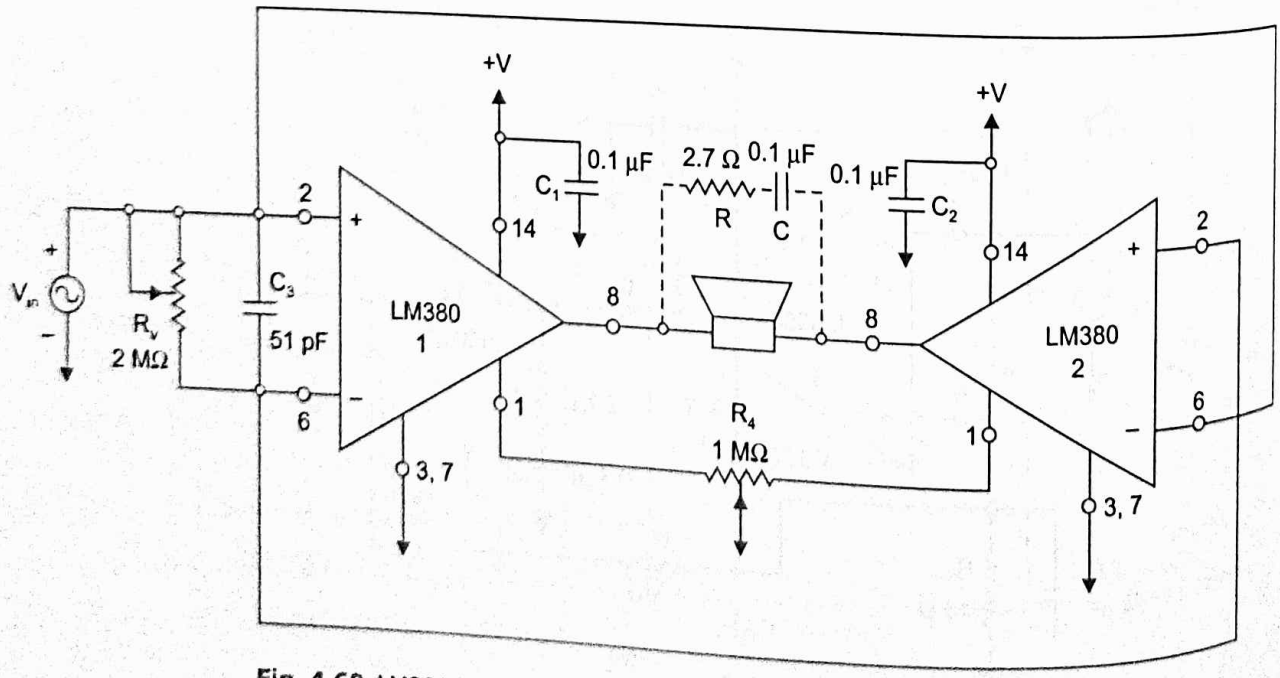


Fig. 4.60 LM380s used in bridge configuration to provide more power (*R* and *C* for stability with high-current loads.)

LM380 as Intercom System

A simple and inexpensive intercom system can be made by using the LM380 as shown in Fig. 4.61. The speakers used in this figure are permanent-magnet types and hence act as microphones as well. The talk and listen modes are defined with reference to a master station. When the switch is in the talk position, the master speaker acts as the microphone [see Figure 4.61 (a)]. On the other hand, when the switch is in the listen mode, the remote speaker acts as the microphone [Figure 4.61(b)]. In either position the overall gain of the circuit is the same and depends on the turns ratio of the transformer T as well as the internal gain of the LM380. For example, if the turns ratio $N_1/N_2 = 20$, the overall gain of the circuit will be $50 \times 20 = 1000$. However, the internal gain of the LM380 can be controlled with the use of potentiometer R_v.

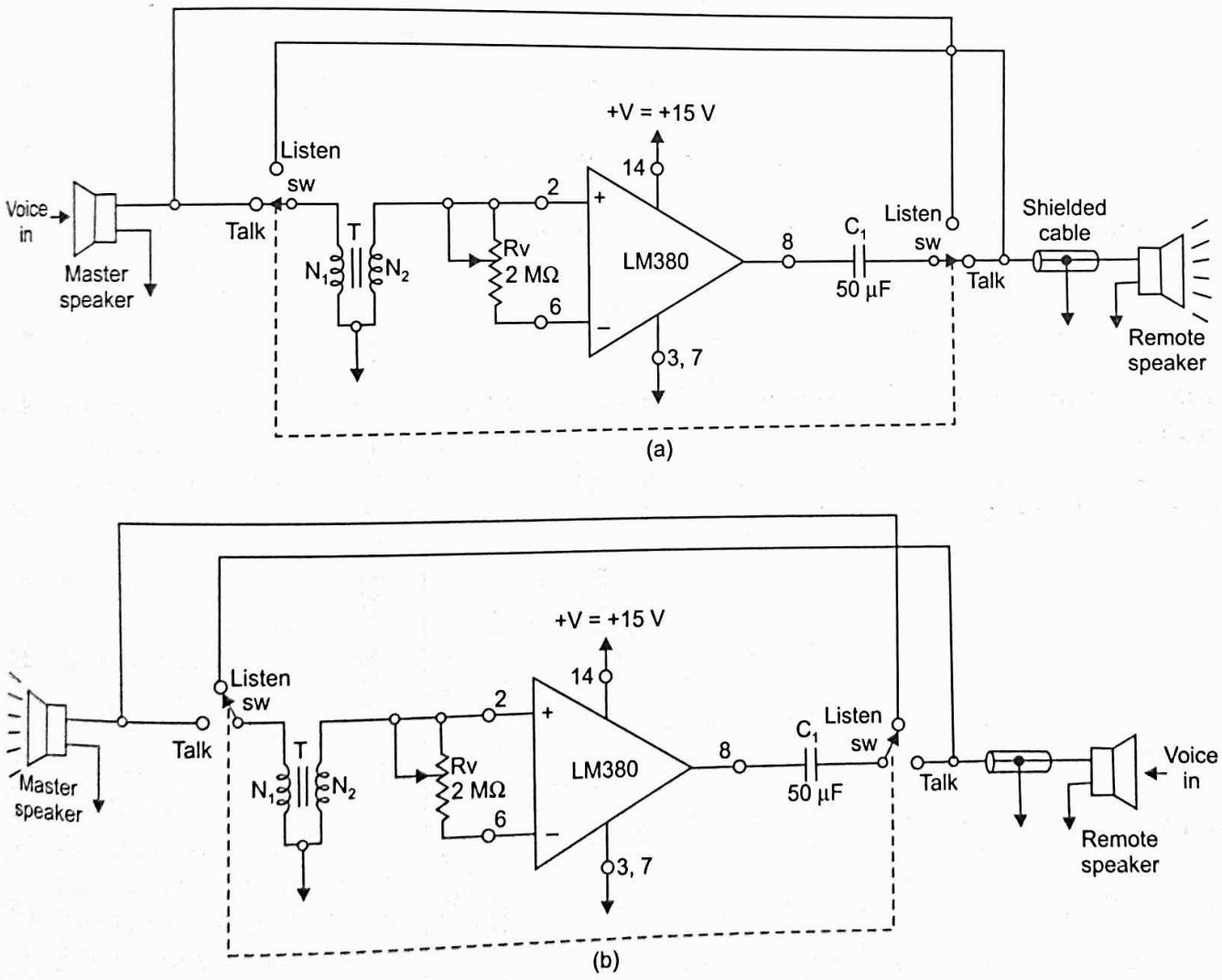


Fig. 4.61 Intercom systems using the LM380: (a) Talk mode, (b) Listen mode

Siren/Alarm using LM380 Power Amplifier

A siren/alarm system can be designed using LM380 power amplifier, as shown in Fig. 4.62. The MC1458 is a dual op-amp consisting of op-amps A_1 and A_2. The output of A_1 is square wave while the output of A_2 is a triangular or sawtooth waveform. The switch SW1 connects the outputs of A_1 and A_2 to the LM380 audio amplifier. Only one output at a time, either of A_1 or

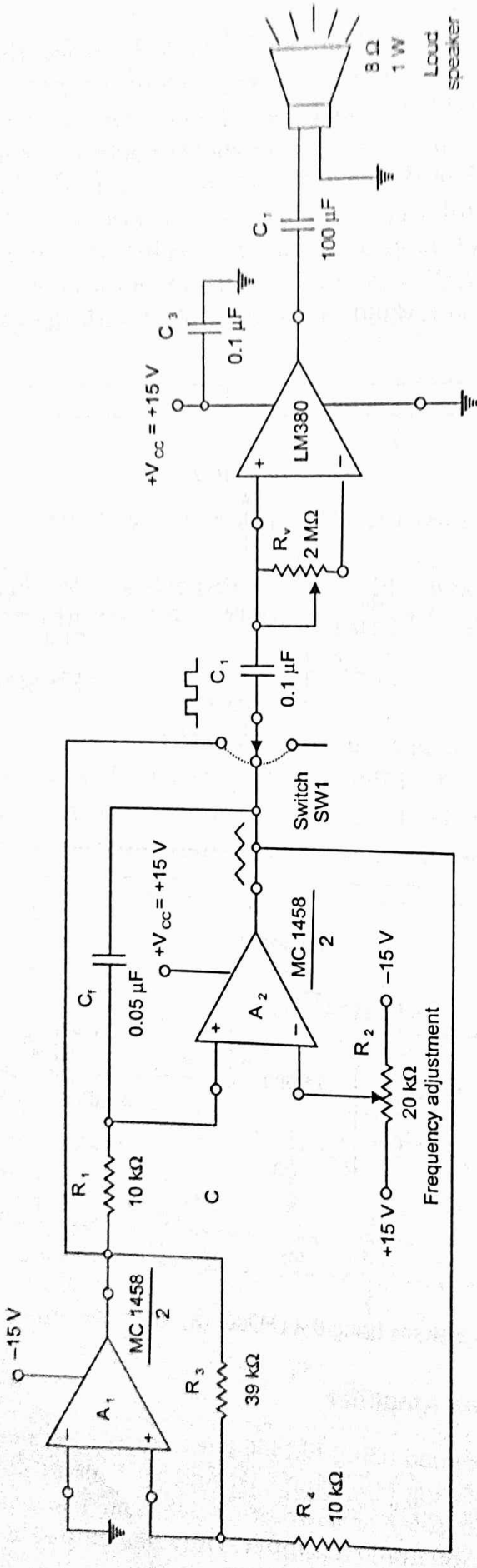


Fig. 4.62 Siren/alarm system using LM 380

A_2 gets connected to LM380 with the help of switch SW1. The LM380 drives the 8 Ω, 1 W speaker. The potentiometer R_v connected at the input terminals of LM380 controls the sound level. The sound level depends upon the switch position, R_2 and capacitor C_f. Thus varying sound intensities can be obtained.

SUMMARY

1. An op-amp can be used to perform mathematical operations such as scale changer, addition and subtraction.
2. An op-amp can be used as a phase lag or phase-lead circuit. Such a circuit is also used as constant dealy filter. The dealy is introduced without change in the gain magnitude. Therefore, these are also called All-pass circuits.
3. An instrumentation amplifier is useful for amplifying low level signals which are obtained by sensing with a transducer in the measurement of physical quantities like temperature, water flow etc.
4. Op-amps can be used for amplifying both ac and dc inputs. A capacitively coupled amplifier is used for amplifying ac signals only.
5. *V*-to-*I* converters are useful in low voltage dc and ac voltmeters, LED and zener diode testers.
6. *I*-to-*V* converters are used for testing photo devices.
7. A diode in the feedback loop of an op-amp behaves as a precision diode as its cut-in voltage gets divided by the open-loop gain of op-amp.
8. A precision diode may be used for half-wave rectification, full wave rectification, peak-value detector, clipper and clamper.
9. A sample and hold circuit samples an input signal and holds on to its last sampled value until the input is sampled again. This circuit is used in analog to digital interfacing and pulse modulating systems.
10. Op-amp may be used to perform functions such as ln, log, antilog, multiply or divide signals.
11. A typical multiplier produces an output V_0 which to proportional to two inputs V_x & V_y or $V_0 = kV_x V_y$, where K is the scaling factor usually maintained as $(1/10)V^{-1}$.
12. Qudrant is used in multiplier circuits for bipolar input signals. First quadrant device accepts only positive input signals, two quadrant device accepts one bipolar signal and one unipolar signal and the four quadrant multiplier can accept two bipolar signals.
13. A logarithmic multiplier has low accuracy and high temperature instability. This multiplier can be used only as one quadrant-device.
14. A Gilbert Multiplier cell is a modification of the basic emitter-coupled differential pair and gives four quadrant multiplication.
15. The typical analog multiplier IC is AD633 that provides four-quadrant mutliplication.
16. The op-amp integrator and differentiator are useful for signal wave shaping.
17. Integrators are preferred over differentiators for analog computers as the gain of integrator decreases with increasing frequency and hence signal to noise ratio of integrator is higher than that of differentiator.
18. A power amplifier is used as the output stage of any electronic system so as to supply large current and power to the load.
19. A power amplifier is designed to provide high power conversion efficiency.
20. A class B Push Pull amplifier provides highest conversion efficiency to a maximum of 75%.
21. Cross over distortion is due to the cut-in voltage effect and can be eliminated by operating a push pull amplifier in class AB operation.
22. IC power amplifiers, LM 380 and LM 384 with in built heat sinks are available.

REVIEW QUESTIONS

4.1. Show with the help of circuit diagram an op-amp used as (i) scale changer, (ii) phase shifter, (iii) inverting adder and (iv) non-inverting adder. Draw an op-amp circuit whose output is $V_1 + V_2 - V_3 - V_4$.

4.2. Draw and explain the working of a phase lag circuit. How to get a phase lag of 90°?

4.3. Derive the magnitude and phase response of a phase lead circuit.

4.4. What is an instrumentation amplifier? Draw a system whose gain is controlled by an adjustable resistance.

4.5. Explain the difference between the dc and ac amplifiers.

4.6. Draw and explain the operation of an ac voltage follower having very high input resistance.

4.7. Draw the circuit of a voltage to current converter if the load is (i) floating and (ii) grounded. Is there any limitation on the size of the load when grounded?

4.8. Draw and explain the operation of a current to voltage converter. If 741C is used, what is the lowest value of current that may be measured?

4.9. Discuss applications of (i) V to I converters (ii) I to V converters.

4.10. What is a precision diode?

4.11. Draw the circuit of a full-wave rectifier and explain how it gives the average value.

4.12. Name the circuit that is used to detect the peak value of the non-sinusoidal waveforms. Explain the operation.

4.13. Draw a sample and hold circuit. Explain its operation and indicate its uses.

4.14. Draw the circuit of a clipper which will clip the input signal below a reference voltage.

4.15. Draw the circuit of a log amplifier using two op-amps and explain its operation.

4.16. Indicate how two analog voltages are multiplied using log-antilog amplifiers.

4.17. Draw the circuit of a Gilbert Multiplier Cell. Explain its analysis and show that it can be used as a four-quadrant analog multiplier.

4.18. Explain a Variable Transconductance Multiplier with neat diagram.

4.19. Draw the pin diagram of IC AD633.

4.20. Explain how to get the square and square root of the given analog signal.

4.21. What are the limitations of an ordinary op-amp differentiator? Draw the circuit of a practical differentiator that will eliminate these limitations.

4.22. Draw the circuit of a lossy integrator showing initial conditions.

4.23. Explain the difference between the integrator and differentiator and give one application of each.

4.24. Show the symbolic representation of the building blocks used in analog computer.

4.25. Explain why integrators are preferred over differentiators in analog computer.

4.26. What is the difference in a voltage and power amplifier?

4.27. Classify amplifiers on the basis of position of quiescent point (Q) on the load line.

4.28. Why is class B Push Pull amplifier used as the output stage?

4.29. Explain "Cross-over distrostion" and suggest ways to climinate it.

PROBLEMS

4.1. (i) Find V_o in the circuit shown in Fig. P.4.1 if $R_f = 10$ kΩ, $R_1 = 2$ kΩ and $R_2 = 5$ kΩ.

(ii) Find R_1 and R_2 in Fig. P.4.1 if V_o is the average of V_1 and V_2 and $R_f = 10$ kΩ.

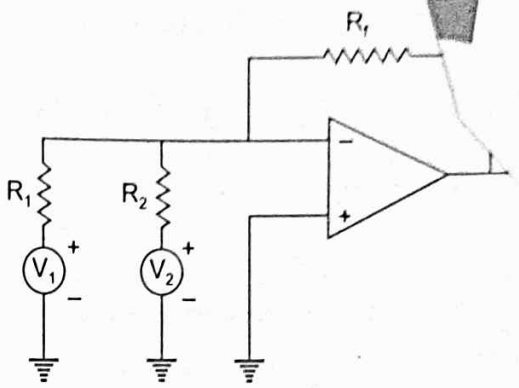


Fig. P. 4.1

4.2. Calculate V_o for the circuit of Fig. P. 4.2. for $V_1 = 5$ V, $V_2 = 2$ V.

4.3. (i) In Fig. 4.2 (a), $V_1 = 0.1$ V, $V_2 = 0.2$ V, $V_3 = -0.3$ V, $R_1 = 4$ kΩ, $R_2 = 3$ kΩ, $R_3 = 1$ kΩ, $R_f = 4.7$ kΩ. Find output voltage V_o.

(ii) The circuit of Fig. 4.2 (b) is to be used as an averaging amplifier with the following specifications: $V_1 = V_2 = 1.5$ V, $V_3 = 3$ V, $R_1 = R_2 = R_3 = R = 1.5$ kΩ, and $V_o = 5$ V. Determine the value of R_f.

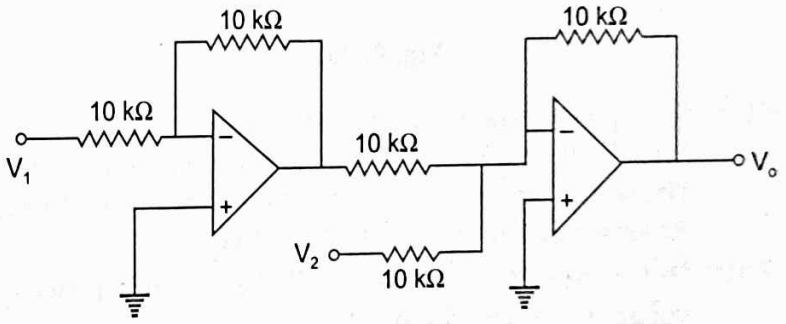


Fig. P. 4.2

4.4. Explain a variable transconductance multiplier.

4.5. Draw the pin diagram of IC AD633.

4.6. In the circuit of Fig. P. 4.4, it can be shown that

$$V_o = a_1 V_1 + a_2 V_2 + a_3 V_3$$

Find the values of a_1, a_2 and a_3. Also find the value of V_o if (i) R_4 is short circuited (ii) R_4 removed (iii) R_1 is short circuited.

4.7. Figure P. 4.5 shows a diff-amp with double ended output. Show that $V_o = \frac{R_2}{R_1}(V_1 - V_2)$ where $V_o = V_4 - V_3$.

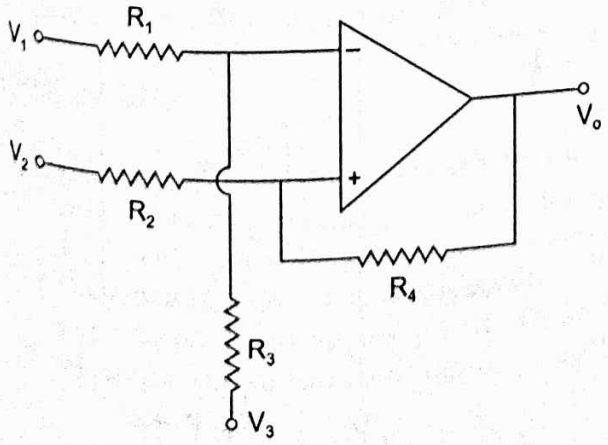


Fig. P. 4.4

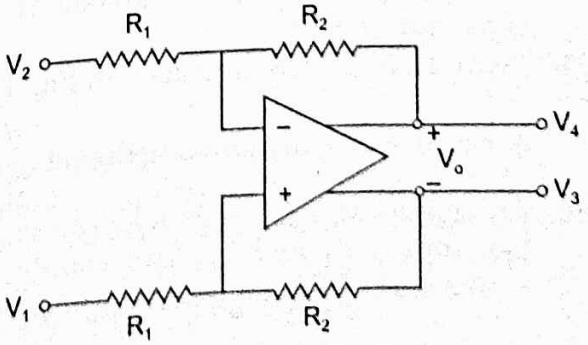


Fig. P. 4.5

4.8. For the instrumentation amplifier shown in Fig. P. 4.6 verify that,

$$V_o = \left(1 + \frac{R_2}{R_1} + \frac{2R_2}{R}\right)(V_2 - V_1)$$

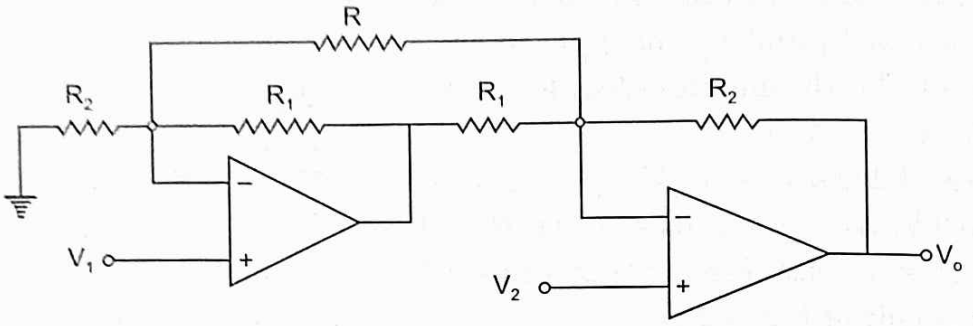


Fig. P. 4.6

4.9. In a peak detector of the type shown in Fig. 4.13 (a), $C = 0.01$ μF, $v_i = 2$ V pp square wave at 1 kHz. Draw the approximate output voltage waveform. Assume R_f for the diode = 100 Ω.

4.10. In the circuit shown in Fig. P. 4.8. input is a sweep voltage $v_i = \alpha t$. Show that the output

$$v_o = -\alpha R'C - \alpha \frac{R'}{R} t.$$

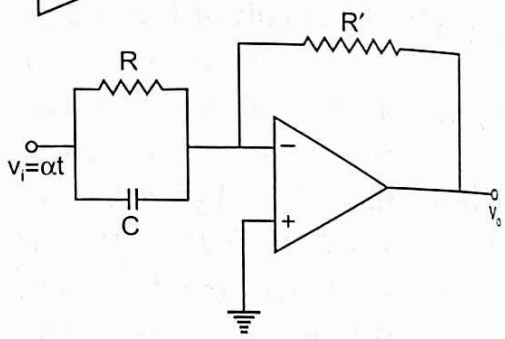


Fig. P. 4.8

4.11. The input v_i to a differentiator of Fig. 4.21 (a) is shown in Fig. P. 4.9. Find the output v_o if $R_f = 2$ kΩ and $C_1 = 0.1$ μF.

4.12. In the integrator of Fig. 4.23, find the output v_o, if $R_1 = 10$ kΩ, $C_f = 0.02$ μF, $v_o(0) = 0$, and the input voltage is,

$$v_i = 4 \cos 10^4 t + 1.$$

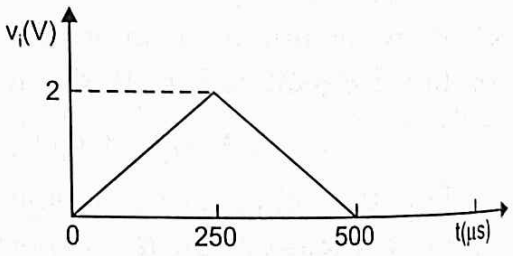


Fig. P. 4.9

4.13. Find the gain in dB of the lossy integrator of Fig. 4.25 (a) if $R_f = 10$ kΩ, $R_1 = 1$ kΩ, $C_f = 0.01$ μF, for (a) $\omega = 0$, (b) $\omega = 10{,}000$ rad/s.

4.14. Find R_f and R_1 in Fig. 4.25 (a) so that the peak gain is 20 dB and the gain is 3 dB down from its peak when $f = 10{,}000$ Hz. Use a capacitor of 1 nF.

4.15. Prove that the circuit shown in Fig. P. 4.13 is a non-inverting integrator with $v_o = \frac{2}{RC}\int v_i \, dt$.

4.16. An op-amp is used as an adder-integrator for two inputs V_1 and V_2. Two supply voltages + 10V and –10 V are available to allow for an

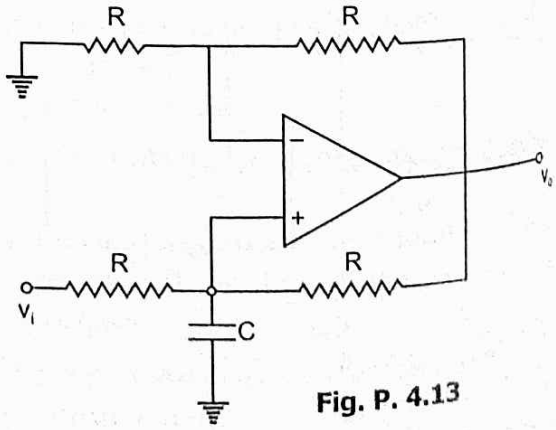


Fig. P. 4.13

initial output voltage which may be anywhere between –5 V and +5 V. Indicate the system using ganged switches so that in position 1, the initial condition is set and in position 2, the integration takes place.

4.17. Find the transfer function v_o/v_i of the circuit shown in Fig. P. 4.15.

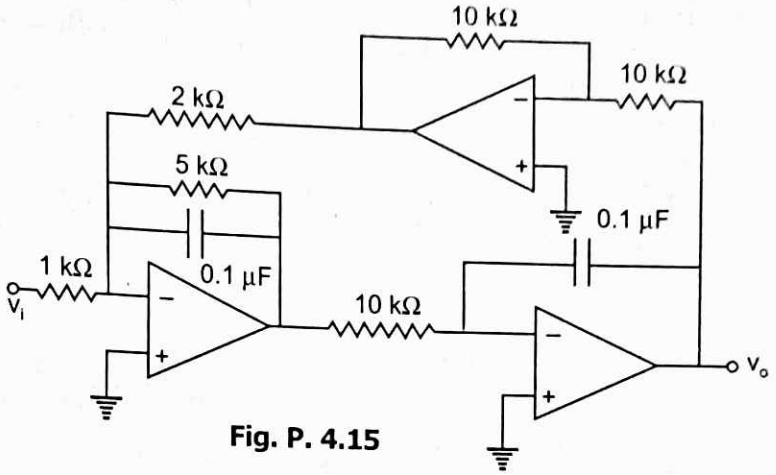
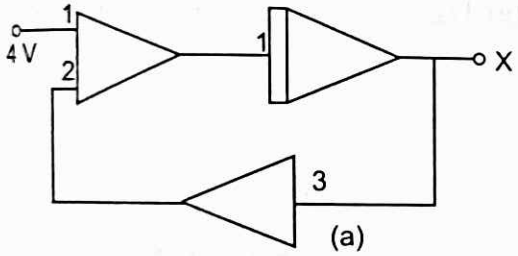


Fig. P. 4.15

4.18. Find the differential equation satisfied by the output X in the circuit of Fig. P. 4.16 (a, b).



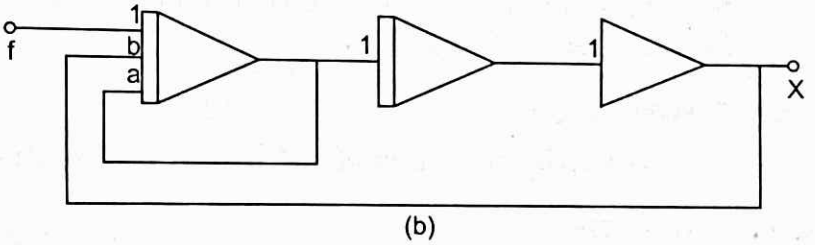


Fig. P. 4.16

4.19. Set up a computer simulation to solve the differential equation,

$$\frac{d^2v}{dt^2} + 2v - 5\sin \omega t = 0$$

where, $v(0) = -1$ and $\dot{v}(0) = 0$

Simulate also the input sinewave.

EXPERIMENT 4.1

To demonstrate the operation of an inverting summing amplifier using 741 op-amp.

PROCEDURE

1. Connect the circuit as shown in Fig. E. 4.1 (a).
2. Since it is usually not possible to have two signal generators for one experiment, op-amp 1 is used as a voltage follower to give two signals v_2 and v_1 shown in Fig. E. 4.1. (a). In this case, the two input signals v_1 and v_2 will be equal. Set the signal generator to give peak-to-peak voltage of 1 V at 100 Hz.
3. Measure the output voltage v_o using a CRO. The output should be

$$v_o = -\frac{R_f}{R_2}v_2 - \frac{R_f}{R_1}v_1$$

4. Observe the waveforms v_1, v_2 and v_0.
5. Note the phase of the output voltage v_0 with respect to input voltage.
6. If it is desired to add unequal voltages, use op-amp 1 as a non-inverting amplifier as shown in Fig. E. 4.1 (b). For the values chosen, the gain of the non-inverting amplifier will be 2.

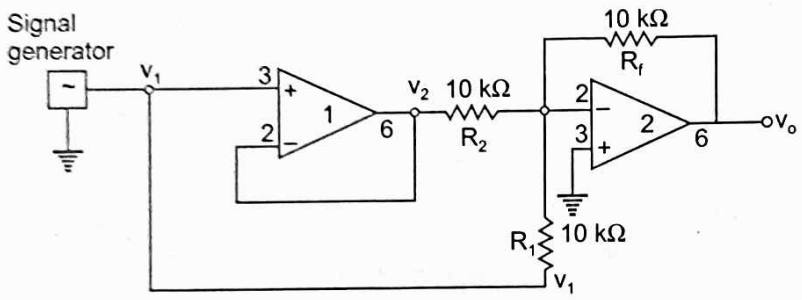


Fig. E. 4.1 (a) An inverting summing amplifier

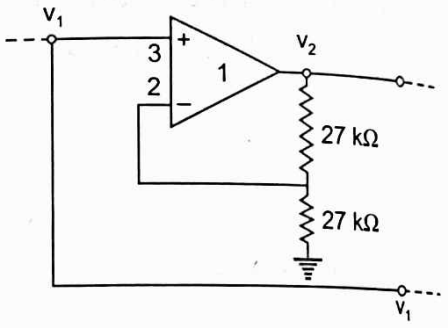


Fig. E. 4.1 (b) Op-amp '1' connected as non-inverting amplifier

7. Set the signal generator to give 1 V pp sinewave at 100 Hz.
8. Repeat step 3, 4 and 5.

EXPERIMENT 4.2

To demonstrate the operation of a Practical Differentiator.

Design Aspects

Practical Differentiator

In Fig. E. 4.2 the resistor R_1 reduces the high frequency noise and capacitor C_f helps in suppressing oscillations. The circuit will provide reasonably accurate differentiation upto a frequency f_a, where,

$$f_a = \frac{1}{2\pi R_f C_1} \text{ Hz} \qquad \text{[see Eq. (4.71)]}$$

The values of R_1 and C_f should be chosen so that $f_b = 10\, f_a$ where,

$$f_b = \frac{1}{2\pi R_1 C_1} \qquad \text{[see Eq. (4.74)]}$$

and $\quad R_1 C_1 = R_f C_f$

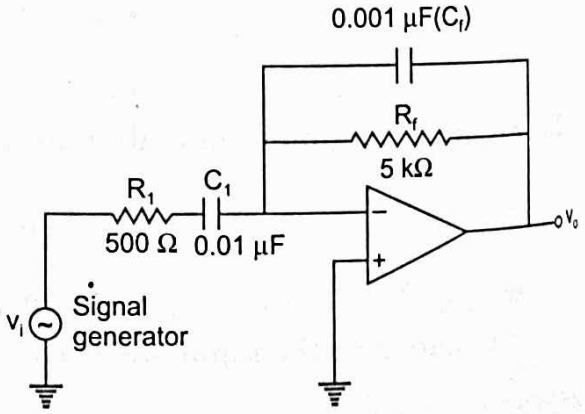


Fig. E. 4.2 A practical differentiator

For the given component values the highest frequency f_a or f_{max} up to which circuit will provide accurate differentiation is,

$$f_a = \frac{1}{2\pi R_f C_1} = \frac{1}{2\pi \times 5 \times 10^3 \times .01 \times 10^{-6}} = 3.18 \text{ kHz}$$

Thus, if we give an input signal of frequency 3 kHz, i.e.

If $\quad v_i(t) = 1 \sin 2\pi\, 3000t$

Then, $v_o = -R_f C_1 \frac{dV_i}{dt}$

$$= -5 \times 10^3 \times .01 \times 10^{-6} \frac{d(1 \sin 2\pi 3000\, t)}{dt} = -0.94 \cos 2\pi\ 3000t$$

The output waveform is also sinusoidal but it lags input by 90°. Note that the input frequency has not changed, but the amplitude has. The output amplitude of a differentiator is directly proportional to the input frequency, thus, if input frequency is changed to 1.5 kHz, the output amplitude will be half the present value.

PROCEDURE

(i) Connect the differentiator circuit shown in Fig. E. 4.2. Adjust the signal generator to produce a 5 volt peak sine wave at 100 Hz.
(ii) Observe input v_i and output v_o simultaneously on the oscilloscope. Measure and record the peak value of v_o and the phase angle of v_o with respect to v_i.
(iii) Repeat step (ii) while increasing the frequency of the input signal. Find the maximum frequency at which the circuit performs differentiation. Compare it with the calculated value of f_a.

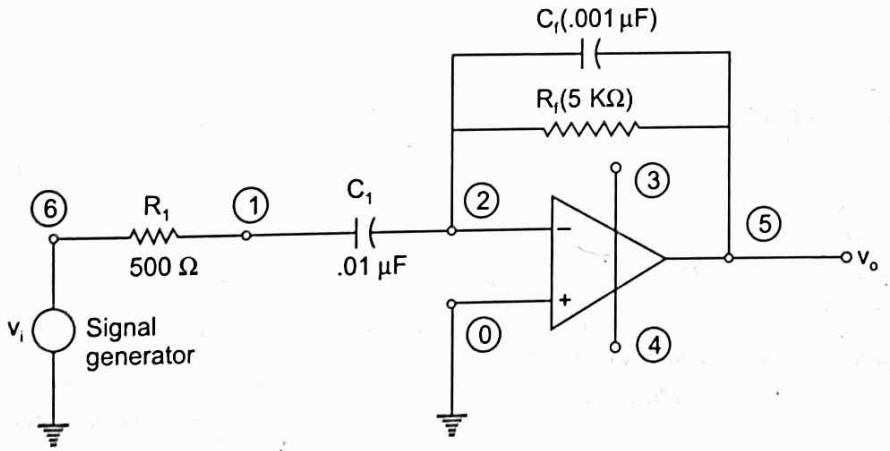


Fig. C. 4.2 (a) Practical differentiator redrawn for PSPICE program

Computer Program 4.2

The circuit of a practical differentiator shown in Fig. E. 4.2 has been redrawn in Fig. C. 4.2 (a) where various terminals have been numbered for writing the PSPICE program. The program listing is shown in Fig. C. 4.2 (b) and the output waveforms for a sinusoidal input of 3 kHz is shown in Fig. C. 4.2 (c). It may be noted that the output is plotted after several cycles of the input has passed through to achieve steady state results.

Fig. C. 4.2 (b) Program Listing

```
*Practical Differentiator-sine wave input
**** Circuit Description
**********************************************
***
```

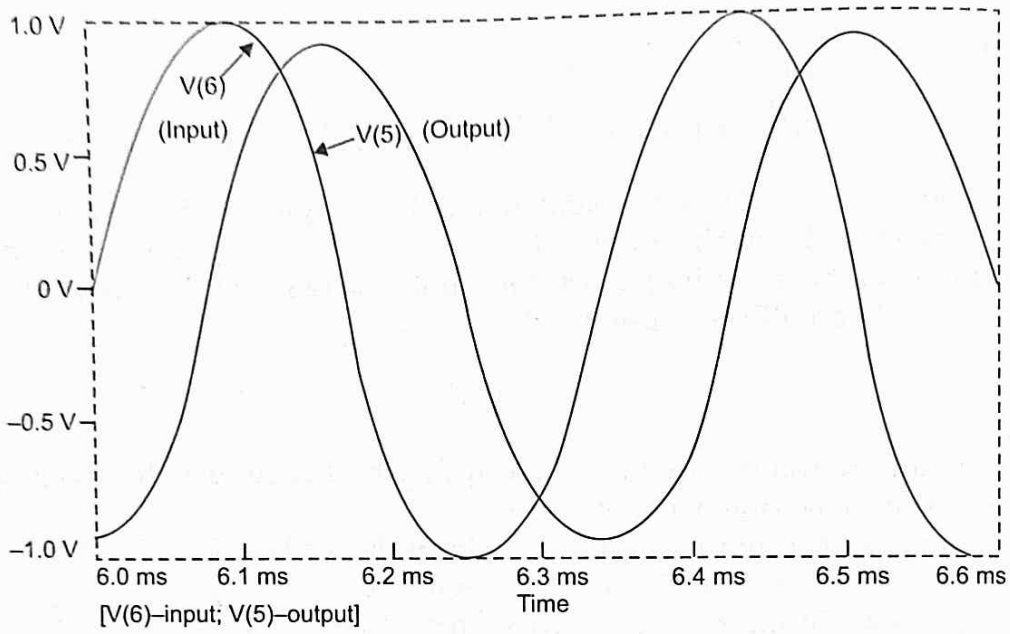


Fig. C 4.2 (c) Input and output waveforms of a practical differentiator

```
    R1  6  1  .5K
    C1  1  2  .01µF
    RF  2  5  5K
    CF  2  5  .001µF
*   Op-amp analysis
    X1  0  2  3  4  5  µA741
    . LIB  EVAL.LIB
*   Power supplies
    VCC  3  0  DC  15V
    VEE  0  4  DC  15V
*   Input signal source
    Vi  6  0  sin  (0  1V  3 kHz)
*   Output
    .TRAN  6µs  6600µs  6000µs  .001ms
    .PROBE
    .END
```

EXPERIMENT 4.3

To demonstrate the operation of a Lossy Integrator.

Design Aspects

Figure E. 4.3 (a) shows a lossy integrator designed in Example 4.4.

The resistor R_f (100 kΩ) is connected across the 0.01 µF capacitor to prevent the amplifier from saturation due to the presence of any dc offset in the input.

Choose $R_f C_f$ = period of the signal to be integrated = $1/f_a$ and $R_f = 10\ R_1$.

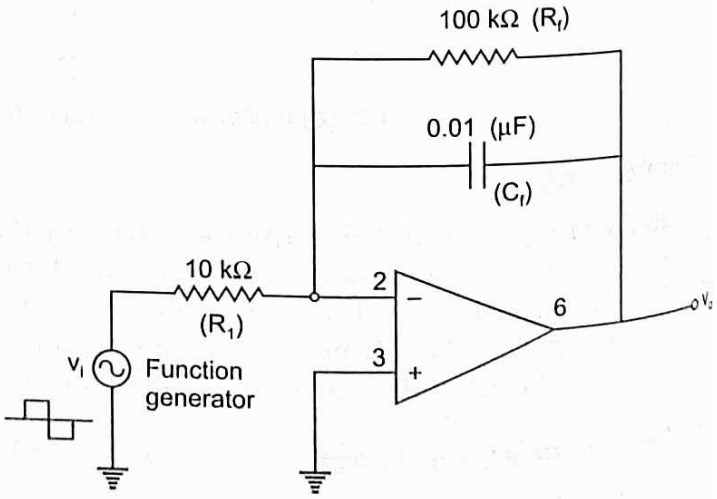


Fig. E. 4.3 (a) A Lossy integrator

For $f < f_a$, the circuit behaves as an inverting amplifier and output is given by

$$v_o = -\frac{R_f}{R_1} v_i$$

For $f > f_a$ the circuit is an integrator and output is

$$v_o = \frac{1}{R_1 C_f} \int v_i \, dt$$

PROCEDURE

(i) Connect the integrator circuit shown in Fig. E. 4.3 (a). Set the function generator to produce a square wave of 1 V peak-to-peak amplitude at 500 Hz. View simultaneously output v_o and input v_i.

(ii) Slowly adjust the input frequency until the output is a good triangular waveform. Measure the amplitude and frequency of the input and output waveforms.

(iii) Verify the following relationship between $R_1 C_f$ and input frequency f for good integration

$$f > f_a = \frac{1}{R_1 C_f}$$

(iv) Now set the function generator to a sine wave of 1 V peak-to-peak and frequency 500 Hz. Adjust the frequency of the input until the output is a negative going cosine wave. Measure the frequency and amplitude of the input and output waveforms.

Computer Program 4.3

The circuit diagram of the Lossy Integrator designed in Example 4.4 has been redrawn in Fig. C. 4.3 (a) with various nodes numbered for writing the PSPICE program. The program listing is shown in Fig. C. 4.3 (b). The response of the circuit for sine wave, step input and square wave input have been shown in Fig. C. 4.3 (c).

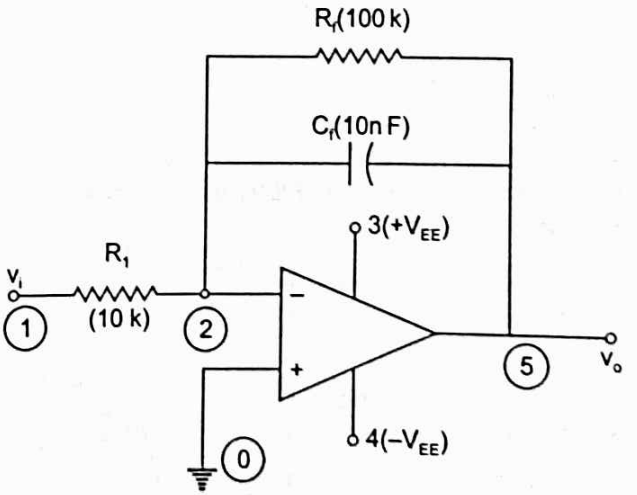


Fig. C. 4.3 (a) Circuit for Program 4.3

Fig. C. 4.3 (b): Program Listing

```
* * * * * * * * * * * * * * * * * * * * * * * * *
*
*  A Lossy Integrator
   R1  1  2  10K
   RF  2  5  100K
*  CF  2  5  10nF
*  Op-amp analysis
   X1  0  2  3  4  5  µA741
*  .LIB EVAL.LIB
*  Power supplies
   VCC  3  0  DC  15V
*  VEE  0  4  DC  15V
*  Sine wave input
*  Vi  1  0  sin  (0  1V  5Khz)
*  Output for sinewave input
*  .TRAN  .5ms  2.5ms  2ms  .001ms
*  Square Wave Input
*  Vi  1  0  PULSE (–1V  1V  0ms  0ms  0ms  .1ms  .2ms)
*  Output for square wave input
*  .TRAN  .2µs  5ms  4ms  .001ms
   Step Input
   * Vi 1 0 PULSE (0V 1V  0ms 0ms 0ms 1ms 1ms)
   * Output for step input
   * .TRAN  .2µs  .3ms  0ms  .001ms
   .PROBE
   .END
```

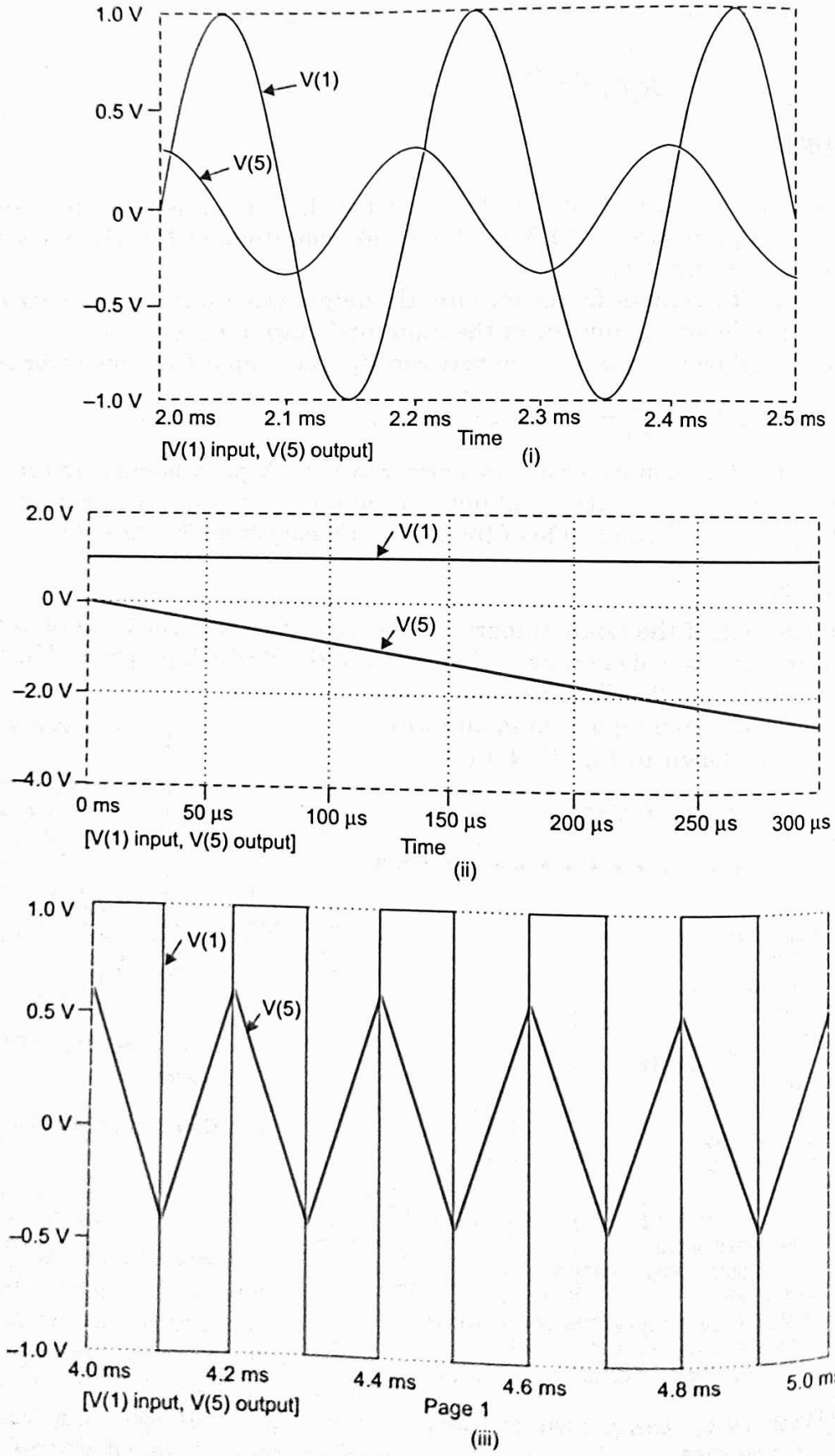


Fig. C. 4.3 (c) Response to (i) Sine wave input, (ii) Step input, (iii) Square wave input

5

COMPARATORS AND WAVEFORM GENERATORS

5.1 INTRODUCTION

An operational amplifier in the open-loop configuration operates in a non-linear manner. There are a number of applications of op-amp in this mode, such as, comparators, detectors, limiters and digital interfacing devices namely converters. In this chapter, we shall discuss comparator and its applications.

5.2 COMPARATOR

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is basically an open-loop op-amp with output $\pm V_{sat}$ (= V_{CC}) as shown in the ideal transfer characteristics of Fig. 5.1 (a). However, a commercial op-amp has the transfer characteristics of Fig. 5.1 (b).

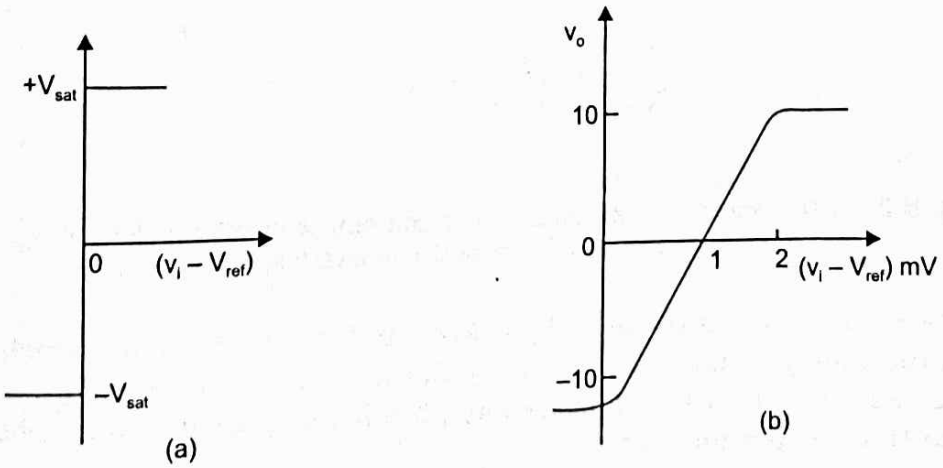


Fig. 5.1 The transfer characteristics (a) Ideal comparator (b) Practical comparator

It may be seen that the change in the output state takes place with an increment in input v_i of only 2 mV. This is the ***uncertainty region*** where output cannot be directly defined. This region is due to input off-set voltage and off-set null compensating techniques can be used to eliminate this. There are basically two types of comparators:

Non-inverting comparator
Inverting comparator.

The circuit of Fig. 5.2 (a) is called a non-inverting comparator. A fixed reference voltage V_{ref} is applied to (–) input and a time varying signal v_i is applied to (+) input. The output voltage is at $-V_{sat}$ for $v_i < V_{ref}$. And v_o goes to $+V_{sat}$ for $v_i > V_{ref}$. The output waveform for a sinusoidal input signal applied to the (+) input is shown in Figs. 5.2 (b and c) for positive and negative V_{ref} respectively.

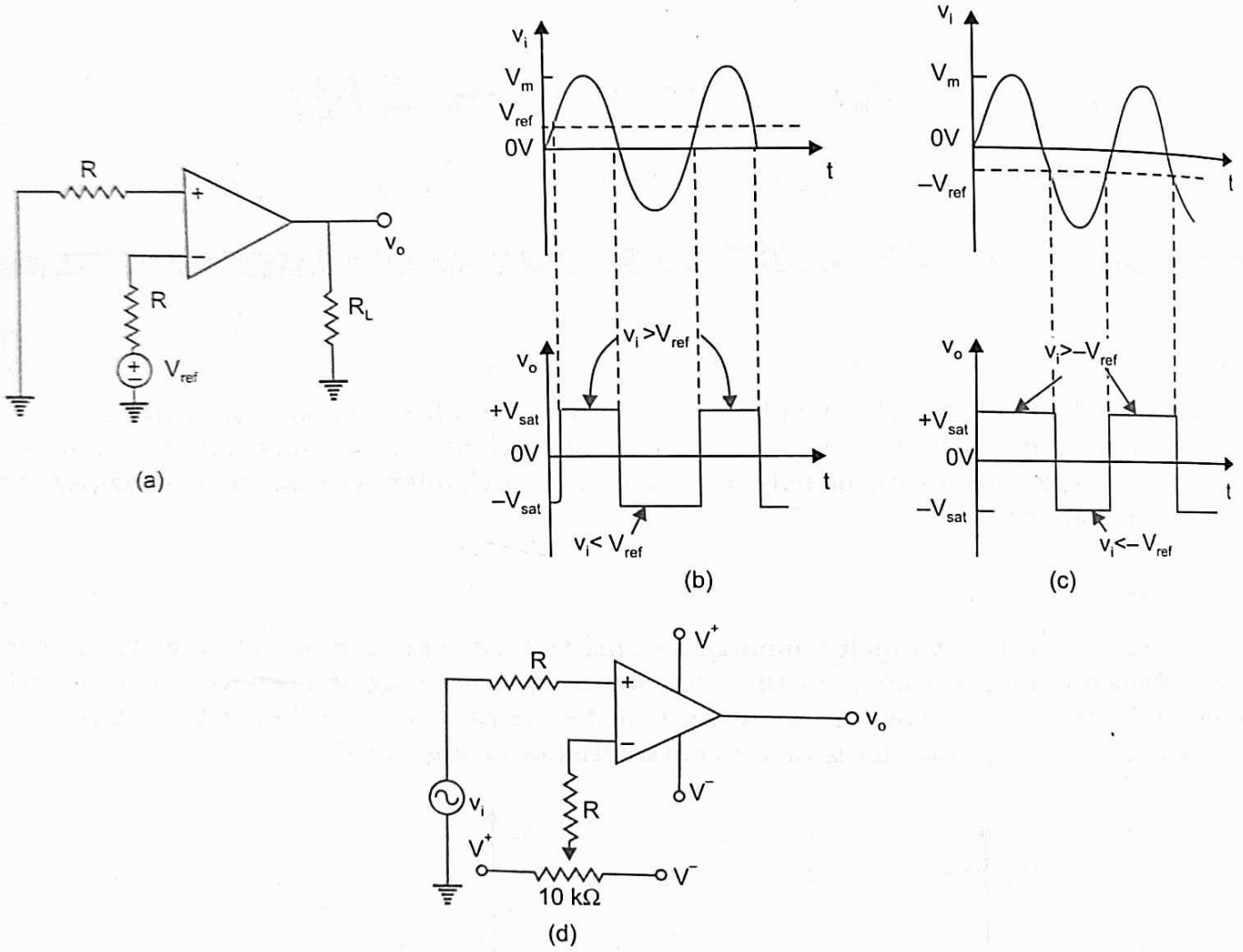


Fig. 5.2 (a) Non-inverting comparator. Input and output waveforms for (b) V_{ref} positive (c) V_{ref} negative (d) Practical non-inverting comparator

In a practical circuit V_{ref} is obtained by using a 10 kΩ potentiometer which forms a voltage divider with the supply voltages V^+ and V^- with the wiper connected to (–) input terminal as shown in Fig. 5.2 (d). Thus a V_{ref} of desired amplitude and polarity can be obtained by simply adjusting the 10 kΩ potentiometer.

Figure 5.3 (a) shows a practical inverting comparator in which the reference voltage V_{ref} is applied to the (+) input and v_i is applied to (–) input. For a sinusoidal input signal, the output waveform is shown in Fig. 5.3 (b) and (c) for V_{ref} positive and negative respectively.

Output voltage levels independent of power supply voltages can also be obtained by using a resistor R and two back to back zener diodes at the output of op-amp as shown in

Fig. 5.3 (d). The value of resistance R is chosen so that the zener diodes operate at the recommended current. It can be seen that the limiting voltages of v_o are $(V_{Z1} + V_D)$ and $-(V_{Z2} + V_D)$ where V_D (~0.7 V) is the diode forward voltage.

In the waveforms of Figs. 5.2 and 5.3, the output transitions are shown as taking place instantaneously. Practical circuits, however, take a certain amount of time to switch from one voltage level to another. The actual waveform will therefore exhibit slanted edges as well as delays at the points of input threshold crossing. These effects are more noticeable at high frequencies where the output switching times are comparable or even longer than the input period itself. Thus there is an upper limit to the operating frequency of any comparator.

If 741, the internally compensated op-amp is used as comparator, the primary limitation is the slew rate. Since 741C has slew rate equal to 0.5 V/μs, it takes $2 \times 13/0.5 \simeq 50$ μs ($V_{sat} = \pm 13$ V for 741) to swing from one saturation level to the other. In many applications, this

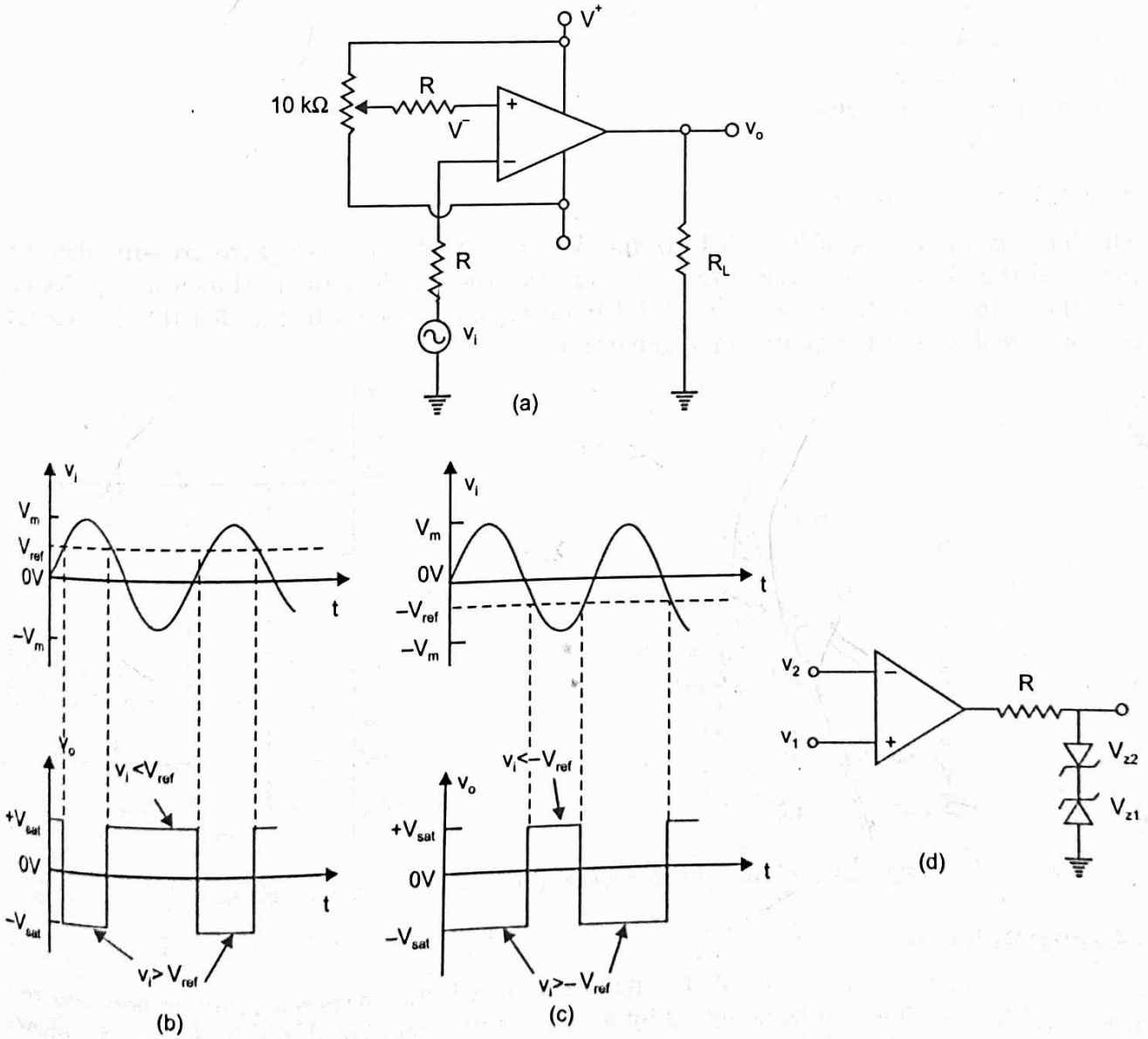


Fig. 5.3 (a) Inverting comparator. Input and output waveforms (b) $V_{ref} > 0$ (c) $V_{ref} < 0$ (d) Comparator with zener diode at the output

is too long. To decrease the response time, it is possible to use uncompensated op-amps such as 301, for comparator applications.

Although uncompensated op-amps make faster comparators than compensated op-amps, there are applications where even higher speeds are required. Also, for interfacing, it is often desired that the output logic levels be compatible with standard logic families such as TTL, CMOS, ECL. To accommodate these needs, monolithic voltage comparators are available. Some of the comparator chips available are the Fairchild μA710 and 760, the National LM 111, 160 and 311. The response time for 311 is 200 ns whereas 710 is a high speed comparator with a response time of 40 ns. CMOS comparators are also available. Some examples are TLC 372 dual, TLC 374 quad (Texas Instruments), MC 14574 quad (Motorola).

5.2.1 Applications of Comparator

Some important applications of comparator are:

Zero crossing detector
Window detector
Time marker generator
Phase meter.

Zero Crossing Detector

The basic comparators of Figs. 5.2 (a) and 5.3 (a) can be used as a zero crossing detector provided that V_{ref} is set to zero. An inverting zero-crossing detector is shown in Fig. 5.4 (a) and the output waveform for a sinusoidal input signal is shown in Fig. 5.4 (b). The circuit is also called a sine to square wave generator.

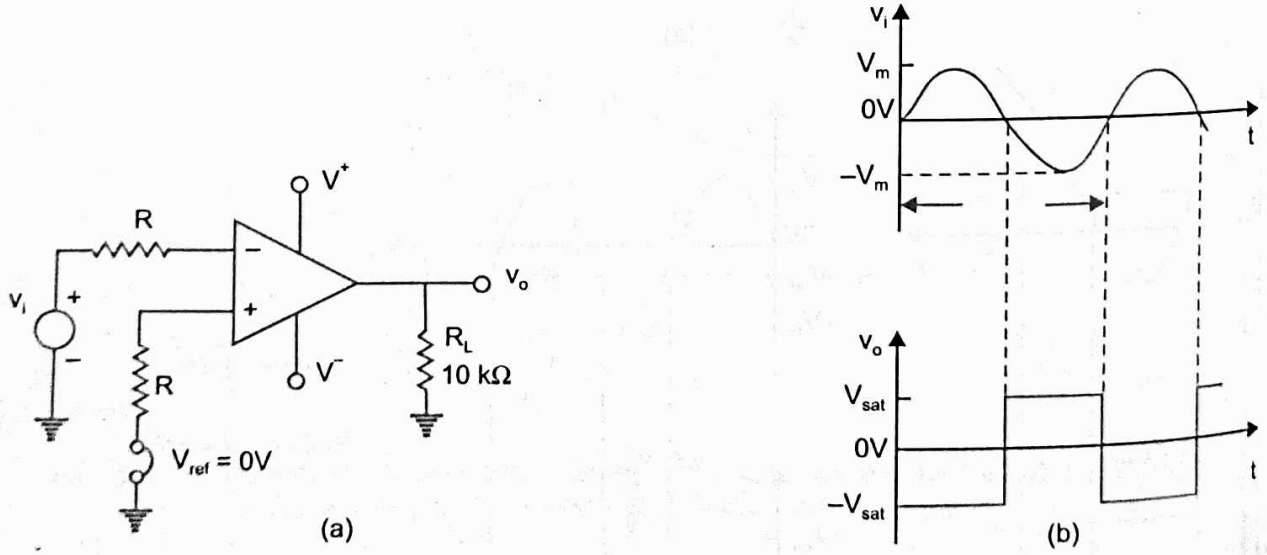


Fig. 5.4 (a) Zero crossing detector (b) Input and output waveforms

Window Detector

Sometimes one may like to mark the instant at which an unknown input is between two threshold levels. This can be achieved by a circuit called window detector. Figure 5.5 shows a three level detector with indicator circuit. There are three indicators: Yellow (LED 3) for input too low (<3 V), Green (LED 2) for safe input (3–6 V) and Red (LED 1) for high input (>6 V). They are turned ***on*** and ***off*** as indicated in Table 5.1.

Table 5.1 Three level comparator LED specifications

Input (volts)	*Yellow LED 3*	*Green LED 2*	*Red LED 1*
Less than 3 V	On	Off	Off
Between 3 V and 6 V	Off	On	Off
Greater than 6 V	Off	Off	On

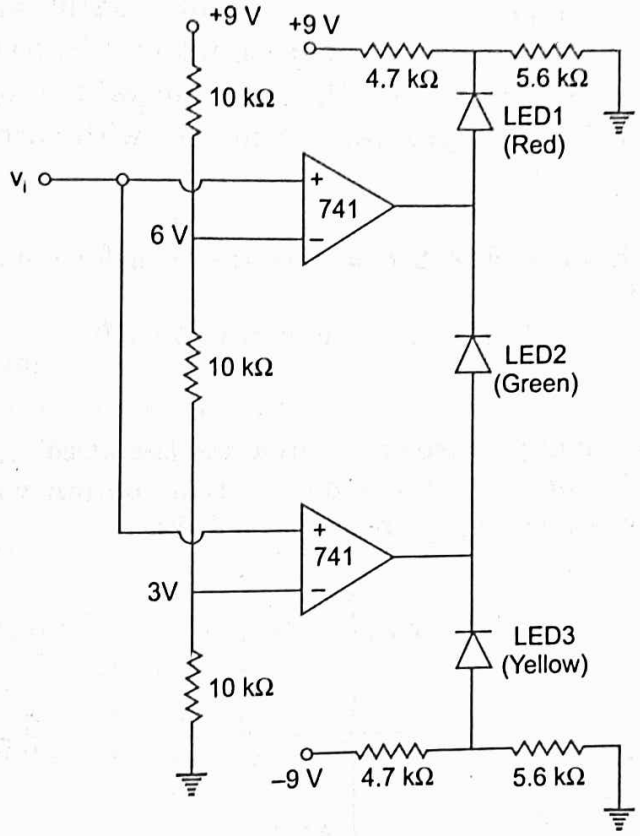


Fig. 5.5 Three level comparator with LED indicator

Time Marker Generator

The circuit is shown in Fig. 5.6 (a). The output of the zero-crossing detector is differentiated by an RC circuit ($RC << T$), so that the voltage v' is a series of positive and negative pulses

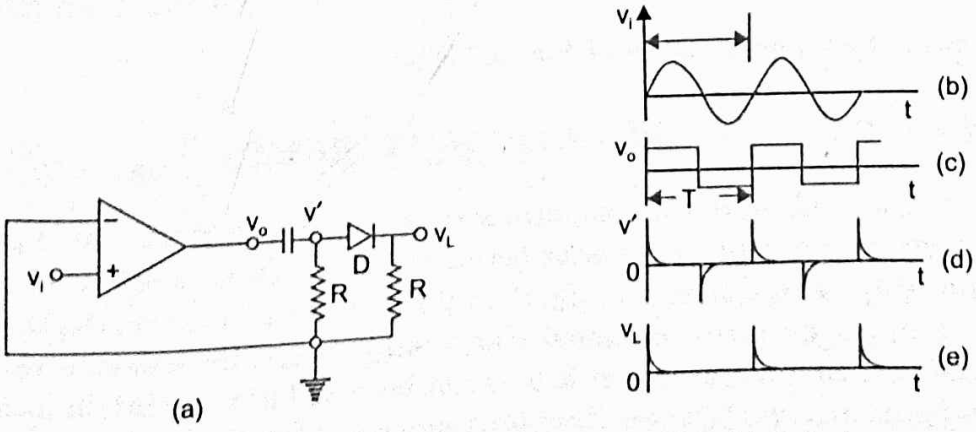


Fig. 5.6 (a) Time marker circuit (b) Input waveform (c) Output v_o (d) Differentiated output v′ (e) Output pulses

as shown in Fig. 5.6 (d). The negative portion is clipped off after passing through the diode D and the waveform v_1 is as shown in Fig. 5.6 (e). So, with the help of this circuit, the sinusoid has been converted into a train of positive pulses of spacing T and may be used for triggering the monoshots, SCR, sweep voltage of CRT etc.

Phase Detector

The phase angle between two voltages can also be measured using the circuit of Fig. 5.6 (a). Both voltages are converted into spikes and the time interval between the pulse spikes of one input and that of the other is measured. The time interval is proportional to the phase difference. One can measure phase angles from 0° to 360° with such a circuit.

Example 5.1

(a) For the comparator shown in Fig. 5.7 (a) plot the transfer curve if the op-amp is an ideal one and $V_{Z1} = V_{Z2} = 9$ V.

(b) Repeat part (a) if the open loop gain of op-amp is 50,000.

Solution

(a) Since $A_{OL} = \infty$, even a small positive or negative voltage at the input drives the output to $\pm V_{sat}$. This causes V_{Z1} or V_{Z2} to break down, giving output voltage $v_o = \pm (V_Z + V_D)$ $= \pm 9.7$ V. The transfer curve is shown in Fig. 5.7 (b).

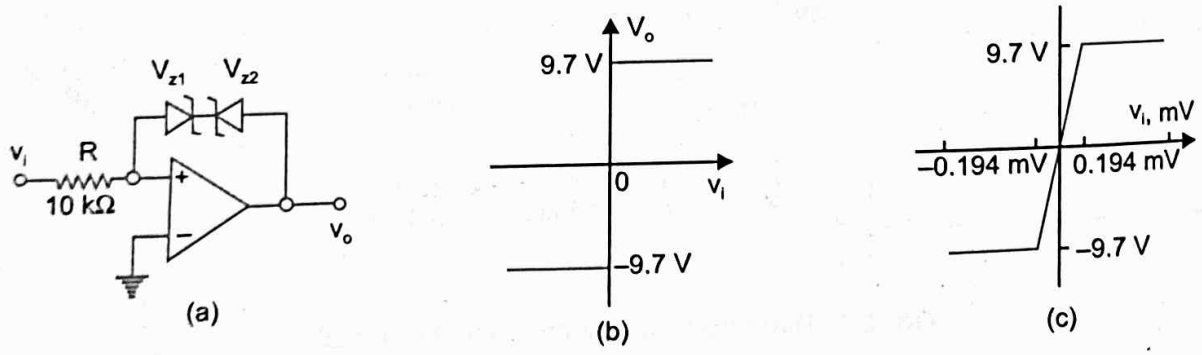


Fig. 5.7 (a) Circuit of Example 5.1 (b) Transfer curve for Example 5.1 (a). (c) Transfer curve for Example 5.1 (b)

(b) Now $A_{OL} = 50{,}000$, so $\Delta v_i \triangleq \dfrac{9.7}{A_{OL}} = 0.194$ mV. The zeners break down after ±0.194 mV as shown in the transfer curve of Fig. 5.7 (c).

5.3 REGENERATIVE COMPARATOR (SCHMITT TRIGGER)

If positive feedback is added to the comparator circuit, gain can be increased greatly. Consequently, the transfer curve of comparator becomes more close to ideal curve. Theoretically, if the loop gain $-\beta A_{OL}$ is adjusted to unity, then the gain with feedback, A_{Vf} becomes infinite. This results in an abrupt (zero rise time) transition between the extreme values of output voltage. In practical circuits, however, it may not be possible to maintain loop-gain exactly equal to unity for a long time because of supply voltage and temperature variations. So a value greater than unity is chosen. This also gives an output waveform virtually discontinuous

at the comparison voltage. This circuit, however, now exhibits a phenomenon called hysteresis or backlash.

Figure 5.8 (a) shows such a regenerative comparator. The circuit is also known as Schmitt Trigger. The input voltage is applied to the (–) input terminal and feedback voltage to the (+) input terminal. The input voltage v_i triggers the output v_o every time it exceeds certain voltage levels. These voltage levels are called upper threshold voltage (V_{UT}) and lower threshold voltage (V_{LT}). The ***hysteresis*** width is the difference between these two threshold voltages i.e. $V_{UT} - V_{LT}$. These threshold voltages are calculated as follows.

Suppose the output $v_o = + V_{sat}$. The voltage at (+) input terminal can be obtained by using superposition

$$V_{UT} = \frac{V_{ref}R_1}{R_1 + R_2} + \frac{R_2 V_{sat}}{R_1 + R_2} \tag{5.1}$$

This voltage is called upper threshold voltage V_{UT}. As long as v_i is less than V_{UT}, the output v_o remains constant at $+V_{sat}$. When v_i is just greater than V_{UT}, the output regeneratively switches to $-V_{sat}$ and remains at this level as long as $v_i > V_{UT}$ as shown in Fig. 5.8 (b).

For $v_o = -V_{sat}$, the voltage at the (+) input terminal is,

$$V_{LT} = \frac{V_{ref}R_1}{R_1 + R_2} - \frac{R_2 V_{sat}}{R_1 + R_2} \tag{5.2}$$

This voltage is referred to as lower threshold voltage V_{LT}. The input voltage v_i must become lesser than V_{LT} in order to cause v_o to switch from $-V_{sat}$ to $+V_{sat}$. A regenerative transition takes place as shown in Fig. 5.8 (c) and the output v_o returns from $-V_{sat}$ to $+V_{sat}$ almost instantaneously. The complete transfer characteristics are shown in Fig. 5.8 (d).

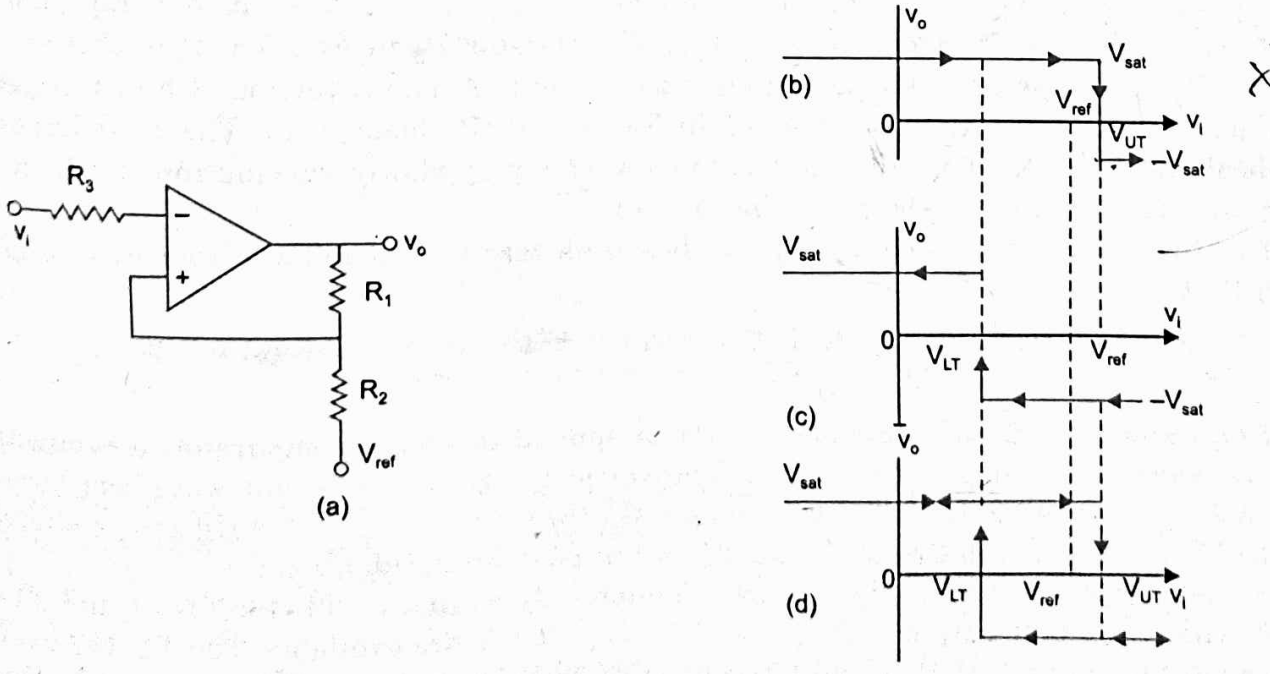


Fig. 5.8 (a) An inverting Schmitt Trigger (b, c) Transfer characteristics for v_i increasing and v_i decreasing (d) Composite input-output curve

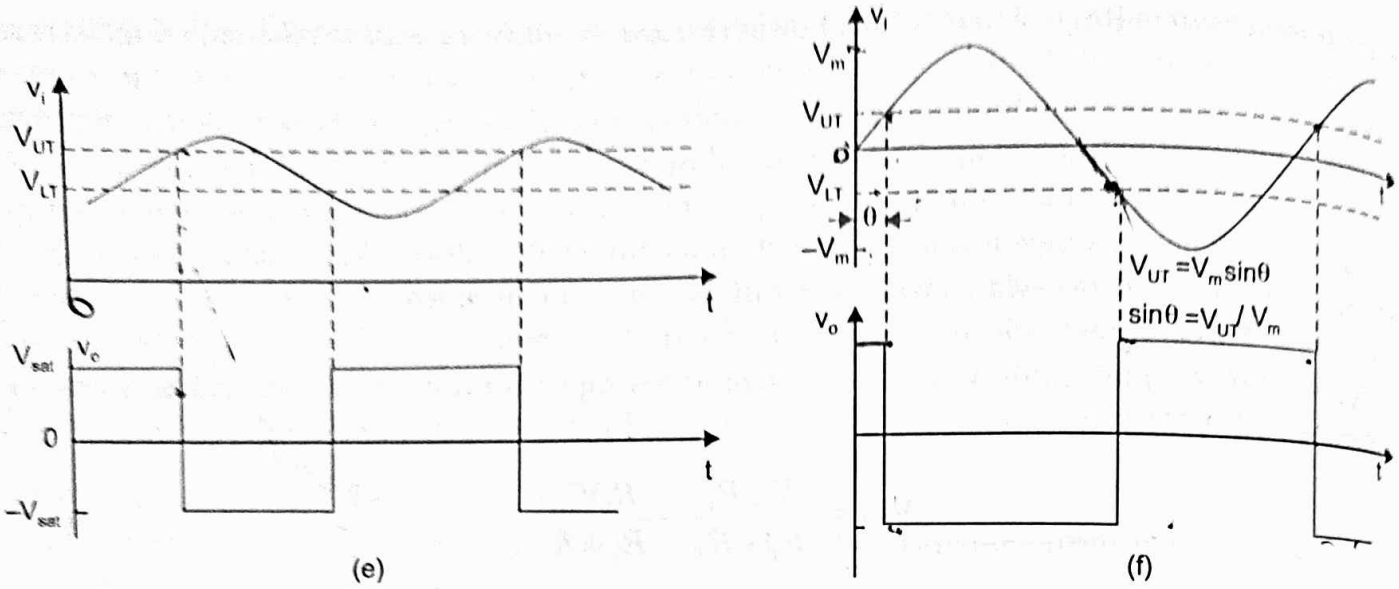


Fig. 5.8 (e) Schmitt Trigger used as a squarer (f) Shift θ in the output waveform for $V_{UT} = -V_{LT}$

Note that $V_{LT} < V_{UT}$ and the difference between these two voltages is the hysteresis width V_H and can be written as

$$V_H = V_{UT} - V_{LT} = \frac{2 R_2 V_{sat}}{R_1 + R_2} \tag{5.3}$$

Because of the hysteresis, the circuit triggers at a higher voltage for increasing signals than for decreasing ones. Further, note that if peak-to-peak input signal v_i were smaller than V_H then the Schmitt trigger circuit, having responded at a threshold voltage by a transition in one direction would never reset itself, that is, once the output has jumped to, say, $+V_{sat}$ it would remain at this level and never return to $-V_{sat}$. It may be seen from Eq. (5.3) that hysteresis width V_H is independent of V_{ref}. The resistor R_3 in Fig. 5.8 (a) is chosen equal to $R_1 \| R_2$ to compensate for the input bias current. A non-inverting Schmitt trigger is obtained if v_i and V_{ref} are interchanged in Fig. 5.8 (a) (Problem 5.10). The most important application of Schmitt trigger circuit is to convert a very slowly varying input voltage into a square wave output as shown in Fig. 5.8 (e).

If in the circuit of Fig. 5.8 (a), V_{ref} is chosen as zero volt, it follows from Eqs. (5.1) and (5.2) that

$$V_{UT} = -V_{LT} = \frac{R_2 V_{sat}}{R_1 + R_2}$$

If an input sinusoid of frequency $f = 1/T$ is applied to such a comparator, a symmetrical square wave is obtained at the output. The vertical edge of the output waveform however, will not occur at the time the sine wave passes through zero [Fig. 5.8 (f)] but is shifted in phase by θ where $\sin\theta = V_{UT}/V_m$ and V_m is the peak sinusoidal voltage.

Special purpose Schmitt triggers are commercially available. T1–13, T1–14 and T1–132 chips with totem pole output and $V_{UT} = 1.7$ V, $V_{LT} = 0.9$ V are available. The T1–132 package is a quad two-input NAND Schmitt trigger. CMOS Schmitt triggers offer the advantage of high input impedance and low power consumption. Examples of CMOS inverting Schmitt trigger are the CD40106B and 744C14.

An interesting application of hysteresis is in the detection and counting of the zero-crossings of an arbitrary waveform if it is superimposed with interference say of a frequency much higher than the signal.

Consider the Fig. 5.8(g) where the clean signal crosses the zero axis a number of times when corrupted with noise interference around each of the zero crossing points we are trying to detect. A simple comparator would change state at each of the zero crossings. If, however, we know the expected peak-to peak amplitude of the interference, the problem is solved by introducing hysteresis of appropriate width in the circuit as shown by V_{UT} and V_{LT} in Fig. 5.8 (g). The hysteresis in the comparator characteristics thus provides an effective means of rejecting interference.

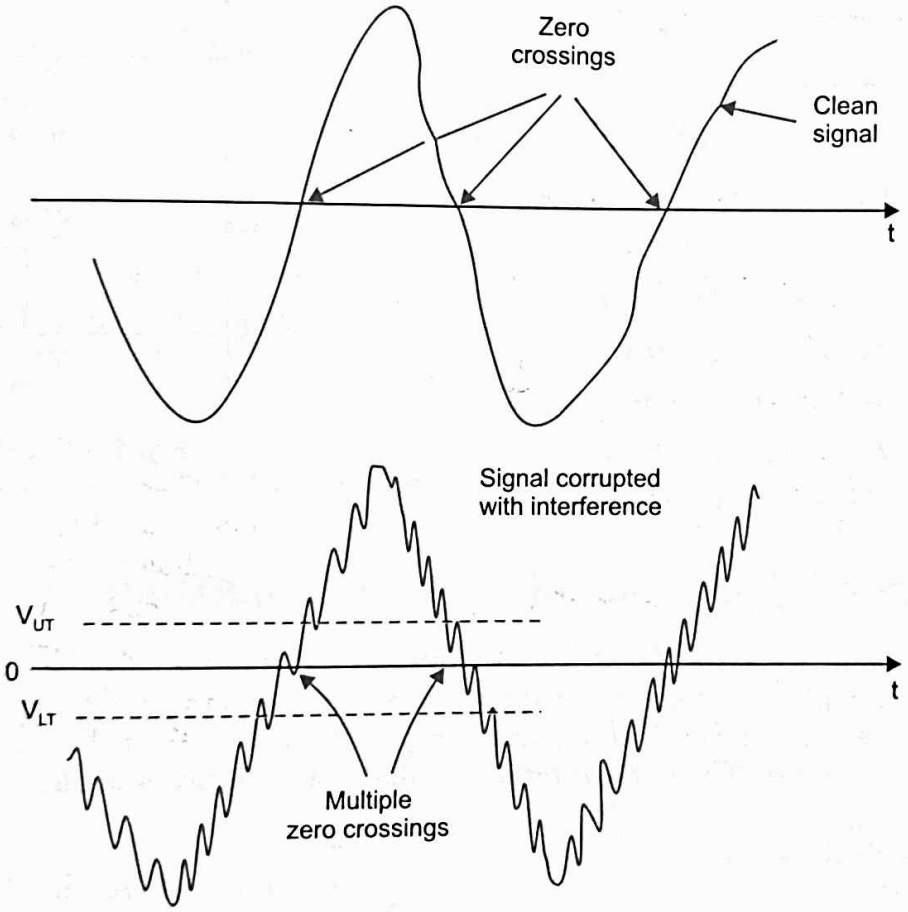


Fig. 5.8 (g) Illustrating the use of hysteresis in the comparator characteristics as a means of rejecting interference

Example 5.2

In the circuit of Schmitt trigger of Fig. 5.8 (a), $R_2 = 100\ \Omega$, $R_1 = 50\ \text{k}\Omega$, $V_{ref} = 0$ V, $\upsilon_i = 1\ V_{pp}$ (peak-to-peak) sine wave and saturation voltage = ±14 V. Determine threshold voltages V_{UT} and V_{LT}.

Solution

From Eqs. (5.1) and (5.2)

$$V_{UT} = \frac{100}{50100} \times 14 = 28\ \text{mV}$$

$$V_{LT} = \frac{100}{50100} \times (-14) = -28 \text{ mV}$$

Example 5.3

A Schmitt trigger with the upper threshold level $V_{UT} = 0$ V and hysteresis width $V_H = 0.2$ V converts a 1 kHz sine wave of amplitude $4V_{pp}$ into a square wave. Calculate the time duration of the negative and positive portion of the output waveform.

Solution

$$V_{UT} = 0$$

$$V_H = V_{UT} - V_{LT} = 0.2 \text{ V}$$

So, $V_{LT} = -0.2$ V

In Fig. 5.9, the angle θ can be calculated as

$$-0.2 = V_m \sin(\pi + \theta) = -V_m \sin\theta = -2 \sin\theta$$

$$\theta = \text{arc sin } 0.1 = 0.1 \text{ radian}$$

The period, $T = 1/f = 1/1000 = 1$ ms

$$wT_\theta = 2\pi\ (1000)\ T_\theta = 0.1$$

$$T_\theta = (0.1/2\pi) \text{ ms} = 0.016 \text{ ms}$$

So, $T_1 = T/2 + T_\theta = 0.516$ ms

and $T_2 = T/2 - T_\theta = 0.484$ ms

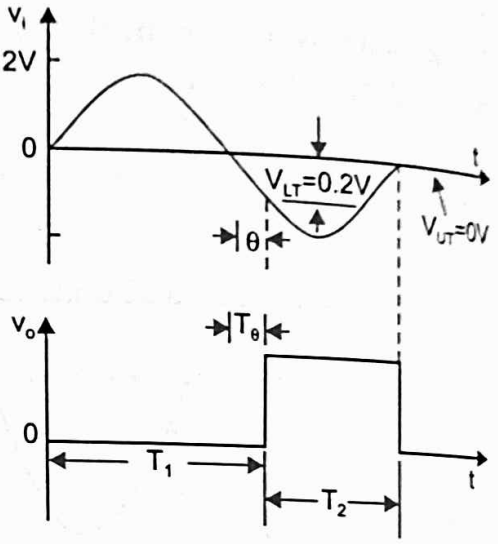
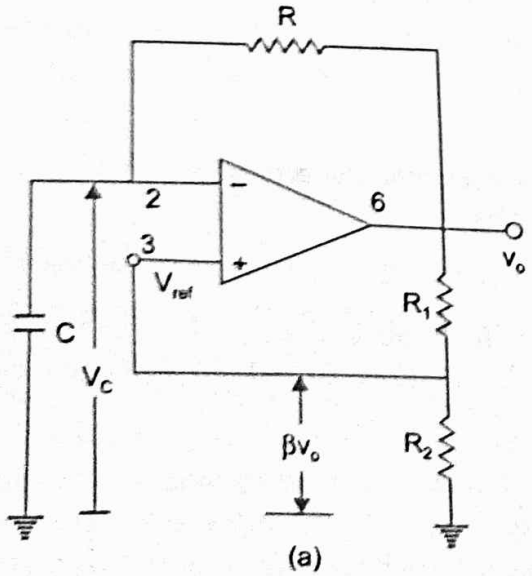


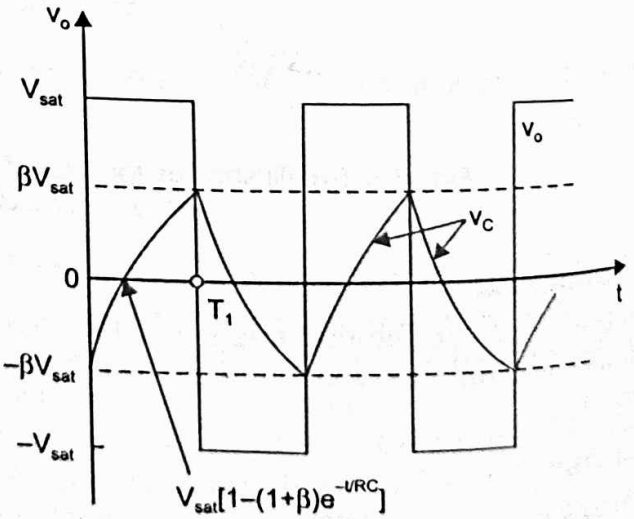
Fig. 5.9 Circuit for Example 5.3

5.4 SQUARE WAVE GENERATOR (ASTABLE MULTIVIBRATOR)

A simple op-amp square wave generator is shown in Fig. 5.10 (a). Also called a ***free running oscillator,*** the principle of generation of square wave output is to force an op-amp to operate in the saturation region. In Fig. 5.10 (a) fraction $\beta = R_2/(R_1 + R_2)$ of the output is fed back to the (+) input terminal. Thus the reference voltage V_{ref} is βv_o and may take values as



(a)



(b)

Fig. 5.10 (a) Simple op-amp square wave generator (b) Waveforms

$+\beta V_{sat}$ or $-\beta V_{sat}$. The output is also fed back to the (–) input terminal after integrating by means of a low-pass RC combination. Whenever input at the (–) input terminal just exceeds V_{ref} switching takes place resulting in a square wave output. In astable multivibrator, both the states are quasi stable.

Consider an instant of time when the output is at $+V_{sat}$. The capacitor now starts charging towards $+V_{sat}$ through resistance R, as shown in Fig. 5.10 (b). The voltage at the (+) input terminal is held at $+\beta V_{sat}$ by R_1 and R_2 combination. This condition continues as the charge on C rises, until it has just exceeded $+\beta V_{sat}$, the reference voltage. When the voltage at the (–) input terminal becomes just greater than this reference voltage, the output is driven to $-V_{sat}$. At this instant, the voltage on the capacitor is $+\beta V_{sat}$. It begins to discharge through R, that is, charges toward $-V_{sat}$. When the output voltage switches to $-V_{sat}$, the capacitor charges more and more negatively until its voltage just exceeds $-\beta V_{sat}$. The output switches back to $+V_{sat}$. The cycle repeats itself as shown in Fig. 5.10 (b).

The frequency is determined by the time it takes the capacitor to charge from $-\beta V_{sat}$ to $+\beta V_{sat}$ and vice versa. The voltage across the capacitor as a function of time is given by,

$$v_c(t) = V_f + (V_i - V_f)e^{-t/RC} \tag{5.4}$$

where, the final value, $V_f = +V_{sat}$

and the initial value, $V_i = -\beta V_{sat}$

Therefore,

$$v_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat})\, e^{-t/RC}$$

or

$$v_c(t) = V_{sat} - V_{sat}\,(1 + \beta)\, e^{-t/RC} \tag{5.5}$$

At $t = T_1$, voltage across the capacitor reaches βV_{sat} and switching takes place. Therefore,

$$v_c(T_1) = \beta V_{sat} = V_{sat} - V_{sat}\,(1+\beta)e^{-T_1/RC} \tag{5.6}$$

After algebraic manipulation, we get,

$$T_1 = RC \ln \frac{1+\beta}{1-\beta} \tag{5.7}$$

This give only one half of the period.

Total time period

$$T = 2T_1 = 2RC \ln \frac{1+\beta}{1-\beta} \tag{5.8}$$

and the output wave form is symmetrical.

If $R_1 = R_2$, then $\beta = 0.5$, and $T = 2RC \ln 3$. And for $R_1 = 1.16R_2$, it can be seen that $T = 2\ RC$

or

$$f_0 = \frac{1}{2RC}$$

The output swings from $+V_{sat}$ to $-V_{sat}$, so,

$$v_o \text{ peak-to-peak} = 2\ V_{sat} \tag{5.9}$$

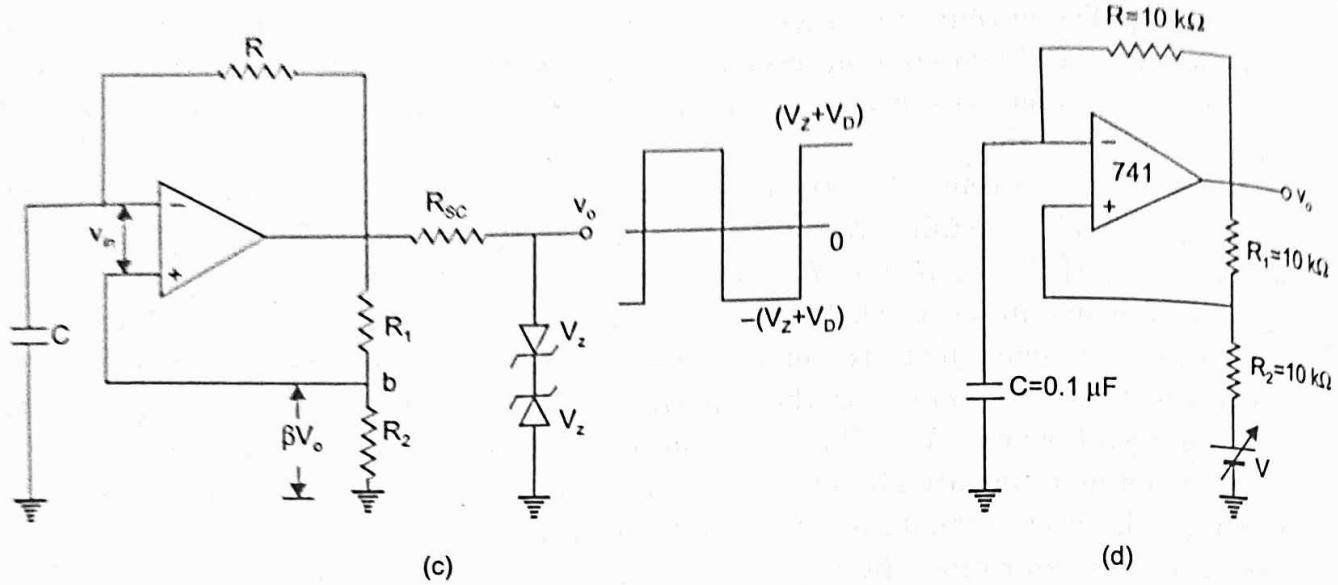


Fig. 5.10 (c) Use of back to back zener diodes. (d) Asymmetric square wave generator

The peak to peak output amplitude can be varied by varying the power supply voltage. However, a better technique is to use back to back zener diodes as shown in Fig. 5.10 (c). The output voltage is regulated to $\pm (V_Z + V_D)$ by the zener diodes.

$$v_o \text{ peak-to-peak} = 2 (V_Z + V_D) \tag{5.10}$$

Resistor R_{sc} limits the currents drawn from the op-amp to,

$$I_{sc} = \frac{V_{sat} - V_Z}{R_{sc}} \tag{5.11}$$

This circuit works reasonably well at audio frequencies. At higher frequencies, however, slew-rate of the op-amp limits the slope of the output square wave.

If an ***asymmetric square wave*** is desired, then zener diodes with different break down voltages V_{Z1} and V_{Z2} may be used. Then the output is either V_{o1} or V_{o2}, where $V_{o1} = V_{Z1} + V_D$ and $V_{o2} = V_{Z2} + V_D$. It can be easily shown that the positive section is given by,

$$T_1 = RC \ln \frac{1+\beta V_{o2}/V_{o1}}{1-\beta} \tag{5.12}$$

The duration of negative section T_2 will be the same as given by Eq. (5.12) with V_{o1} and V_{o2} interchanged.

An alternative method to get asymmetric square wave output is to add a dc voltage source V in series R_2 as shown in Fig. 5.10 (d). Now the capacitor C swings between the voltage levels $(\beta V_{sat} + V)$ and $(-\beta V_{sat} + V)$. If the voltage source V is made variable, voltage to frequency conversion can be achieved though the variation will not be linear.

5.5 MONOSTABLE MULTIVIBRATOR

Monostable multivibrator has one stable state and the other is quasi stable state. The circuit is useful for generating single output pulse of adjustable time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. The circuit shown in Fig. 5.11(a) is a modified form of the astable multivibrator.

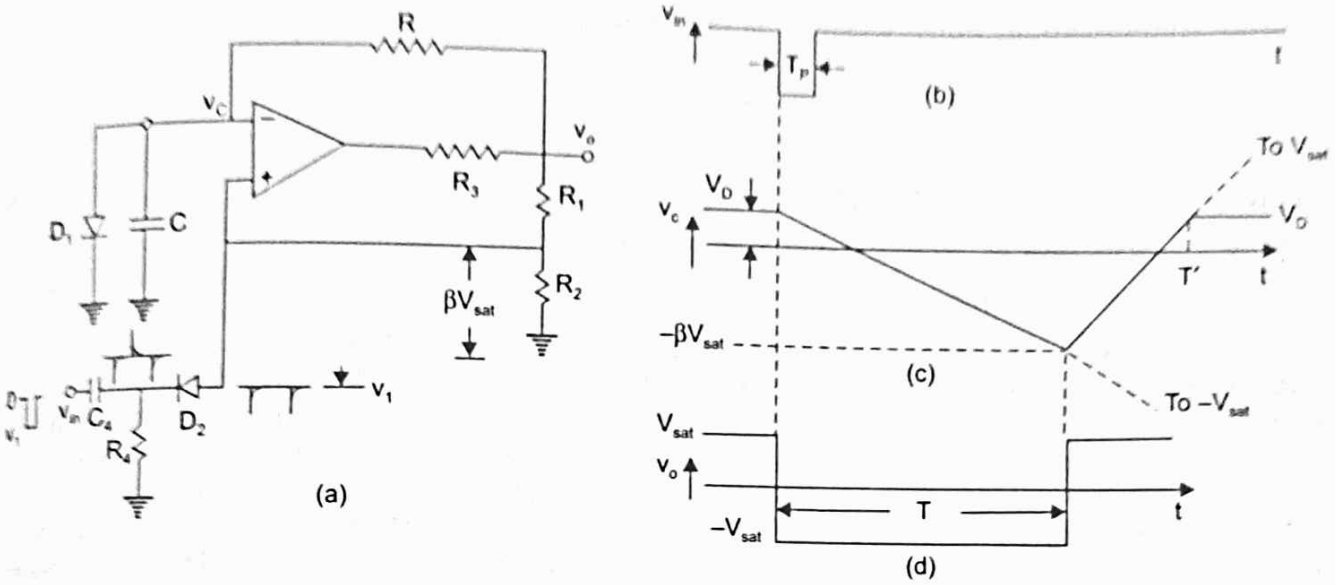


Fig. 5.11 (a) Monostable multivibrator, (b) Negative going triggering signal, (c) Capacitor waveform, (d) Output voltage waveform

A diode D_1 clamps the capacitor voltage to 0.7 V when the output is at $+V_{sat}$. A negative going pulse signal of magnitude V_1 passing through the differentiator R_4C_4 and diode D_2 produces a negative going triggering impulse and is applied to the (+) input terminal.

To analyse the circuit, let us assume that in the stable state, the output v_o is at $+V_{sat}$. The diode D_1 conducts and v_c the voltage across the capacitor C gets clamped to +0.7 V. The voltage at the (+) input terminal through R_1R_2 potentiometric divider is $+\beta V_{sat}$. Now, if a negative trigger of magnitude V_1 is applied to the (+) input terminal so that the effective signal at this terminal is less than 0.7 V, i.e. ($[\beta V_{sat} + (-V_1)] < 0.7$ V), the output of the op-amp will switch from $+V_{sat}$ to $-V_{sat}$. The diode will now get reverse biased and the capacitor starts charging exponentially to $-V_{sat}$ through the resistance R. The voltage at the (+) input terminal is now $-\beta V_{sat}$. When the capacitor voltage v_c becomes just slightly more negative than $-\beta V_{sat}$, the output of the op-amp switches back to $+V_{sat}$. The capacitor C now starts charging to $+V_{sat}$ through R until v_c is 0.7V as capacitor C gets clamped to the voltage. Various waveforms are shown in Fig. 5.11 (b, c, d).

The pulse width T of monostable multivibrator is calculated as follows:

The general solution for a single time constant low pass RC circuit with V_i and V_f as initial and final values is,

$$v_o = V_f + (V_i - V_f)e^{-t/RC} \tag{5.13}$$

For the circuit, $V_f = -V_{sat}$ and $V_i = V_D$ (diode forward voltage).

The output v_c is,

$$v_c = -V_{sat} + (V_D + V_{sat})\, e^{-t/RC} \tag{5.14}$$

at $t = T$,

$$v_c = -\beta V_{sat} \tag{5.15}$$

Therefore,

$$-\beta V_{sat} = -V_{sat} + (V_D + V_{sat})e^{-T/RC}$$

After simplification, pulse width T is obtained as

$$T = RC \ln \frac{(1 + V_D/V_{sat})}{1 - \beta} \tag{5.16}$$

where $\beta = R_2/(R_1 + R_2)$

If, $V_{sat} >> V_D$ and $R_1 = R_2$ so that $\beta = 0.5$, then

$$T = 0.69\ RC \tag{5.17}$$

For monostable operation, the trigger pulse width T_p should be much less than T, the pulse width of the monostable multivibrator. The diode D_2 is used to avoid malfunctioning by blocking the positive noise spikes that may be present at the differentiated trigger input.

It may be noted from Fig. 5.11 (b) that capacitor voltage v_c reaches its quiescent value V_D at $T' > T$. Therefore, it is essential that a recovery time $T' - T$ be allowed to elapse before the next triggering signal is applied. The circuit of Fig. 5.11 (a) can be modified to achieve voltage to time delay conversion as in the case of square wave generator. The monostable multivibrator circuit is also referred to as time delay circuit as it generates a fast transition at a predetermined time T after the application of input trigger. It is also called a gating circuit as it generates a rectangular waveform at a definite time and thus could be used to gate parts of a system.

5.6 TRIANGULAR WAVE GENERATOR

A triangular wave can be simply obtained by integrating a square wave as shown in Fig. 5.12 (a). It is obvious that the frequency of the square wave and triangular wave is the same as shown in Fig. 5.12 (b). Although the amplitude of the square wave is constant at $\pm V_{sat}$, the amplitude of the triangular wave will decrease as the frequency increases. This is because the reactance of the capacitor C_2 in the feedback circuit decreases at high frequencies. A resistance R_4 is connected across C_2 to avoid the saturation problem at low frequencies as in the case of practical integrator.

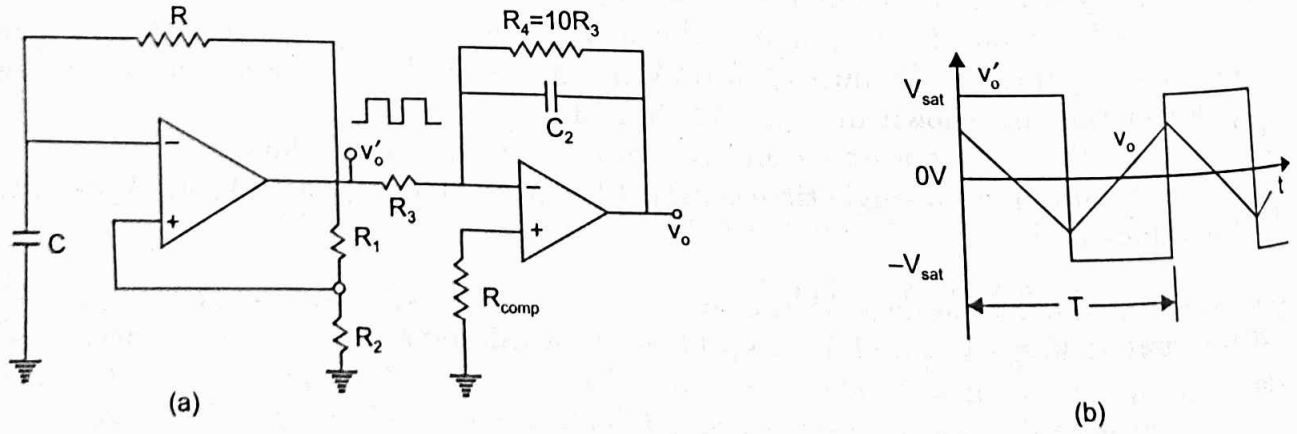


Fig. 5.12 (a) Triangular waveform generator, (b) Output waveform

Another triangular wave generator using lesser number of components is shown in Fig. 5.13 (a). It basically consists of a two level comparator followed by an integrator. The output of the comparator A_1 is a square wave of amplitude $\pm V_{sat}$ and is applied to the (–) input terminal of the integrator A_2 producing a triangular wave. This triangular wave is fed back as input to the comparator A_1 through a voltage divider R_2R_3.

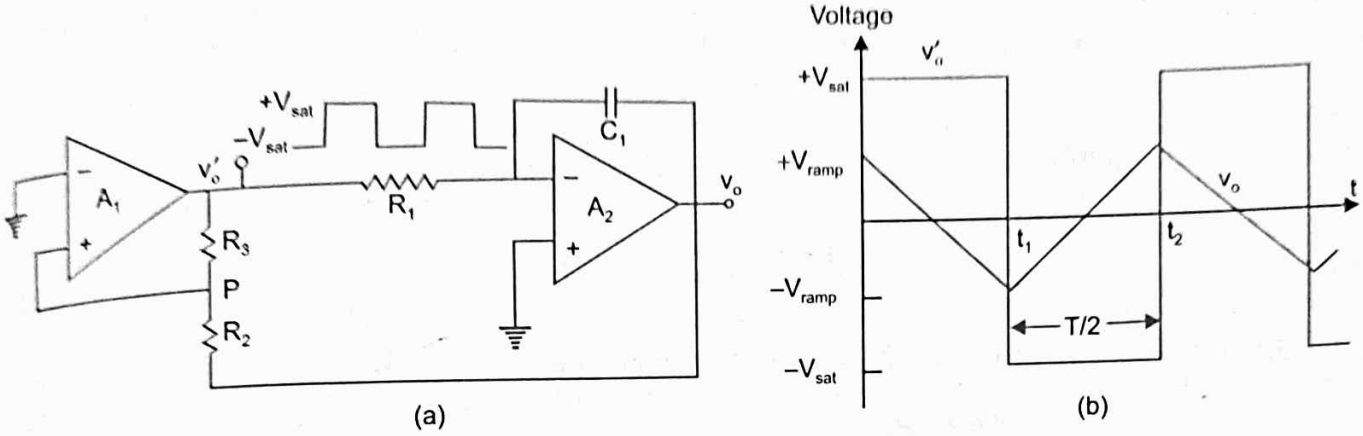


Fig. 5.13 (a) Triangular waveform generator using lesser components, (b) Waveforms

Initially, let us consider that the output of comparator A_1 is at $+V_{sat}$. The output of the integrator A_2 will be a negative going ramp as shown in Fig. 5.13 (b). Thus one end of the voltage divider R_2R_3 is at a voltage $+V_{sat}$ and the other at the negative going ramp of A_2. At a time $t = t_1$, when the negative going ramp attains a value of $-V_{ramp}$, the effective voltage at point P becomes slightly less than 0 V. This switches the output of A_1 from positive saturation to negative saturation level $-V_{sat}$. During the time when the output of A_1 is at $-V_{sat}$, the output of A_2 increases in the positive direction. And at the instant $t = t_2$, the voltage at point P becomes just above 0 V, thereby switching the output of A_1 from $-V_{sat}$ to $+V_{sat}$. The cycle repeats and generates a triangular waveform. It can be seen that the frequency of the square wave and triangular wave will be the same. However, the amplitude of the triangular wave depends upon the RC value of the integrator A_2 and the output voltage level of A_1. The output voltage of A_1 can be set to desired level by using appropriate zener diodes. The frequency of the triangular waveform can be calculated as follows:

The effective voltage at point P during the time when output of A_1 is at $+V_{sat}$ level is given by,

$$-V_{ramp} + \frac{R_2}{R_2 + R_3}\left[+V_{sat} - (-V_{ramp})\right] \tag{5.18}$$

At $t = t_1$, the voltage at point P becomes equal to zero. Therefore, from Eq. (5.18),

$$-V_{ramp} = -\frac{R_2}{R_3}(+V_{sat}) \tag{5.19}$$

Similarly, at $t = t_2$, when the output of A_1 switches from $-V_{sat}$ to $+V_{sat}$,

$$V_{ramp} = \frac{-R_2}{R_3}(-V_{sat}) = \frac{R_2}{R_3}(V_{sat}) \tag{5.20}$$

Therefore, peak to peak amplitude of the triangular wave is,

$$v_o\,(pp) = +V_{ramp} - (-V_{ramp}) = 2\frac{R_2}{R_3}V_{sat} \tag{5.21}$$

The output switches from $-V_{ramp}$ to $+V_{ramp}$ in half the time period $T/2$. Putting the values in the basic integrator equation

$$v_o = -\frac{1}{RC}\int v_i\,dt$$

$$v_o(\text{pp}) = -\frac{1}{R_1C_1}\int_0^{T/2}(-V_{sat})dt = \frac{V_{sat}}{R_1C_1}\left(\frac{T}{2}\right)$$

or,
$$T = 2\,R_1C_1\frac{v_o\,(\text{pp})}{V_{sat}} \qquad (5.22)$$

Putting the value of v_o (pp) from Eq. (5.21), we get

$$T = \frac{4R_1C_1R_2}{R_3}$$

Hence the frequency of oscillation f_o is,

$$f_o = \frac{1}{T} = \frac{R_3}{4R_1C_1R_2} \qquad (5.23)$$

Therefore, the triangular wave oscillates between + 7V and – 7V.

Sawtooth Wave Generator

The difference between the triangular and sawtooth waveforms is that the rise time of a triangular wave is always equal to its fall time. That is, the same amount of time is taken by the triangular wave to swing from $-V_{ramp}$ to $+V_{ramp}$ as from $+V_{ramp}$ to $-V_{ramp}$. On the other hand, the sawtooth waveform has unequal rise and fall times. That is, it may rise many times faster than it falls negatively, or vice versa. The triangular wave generator is as shown in Fig 5.14.

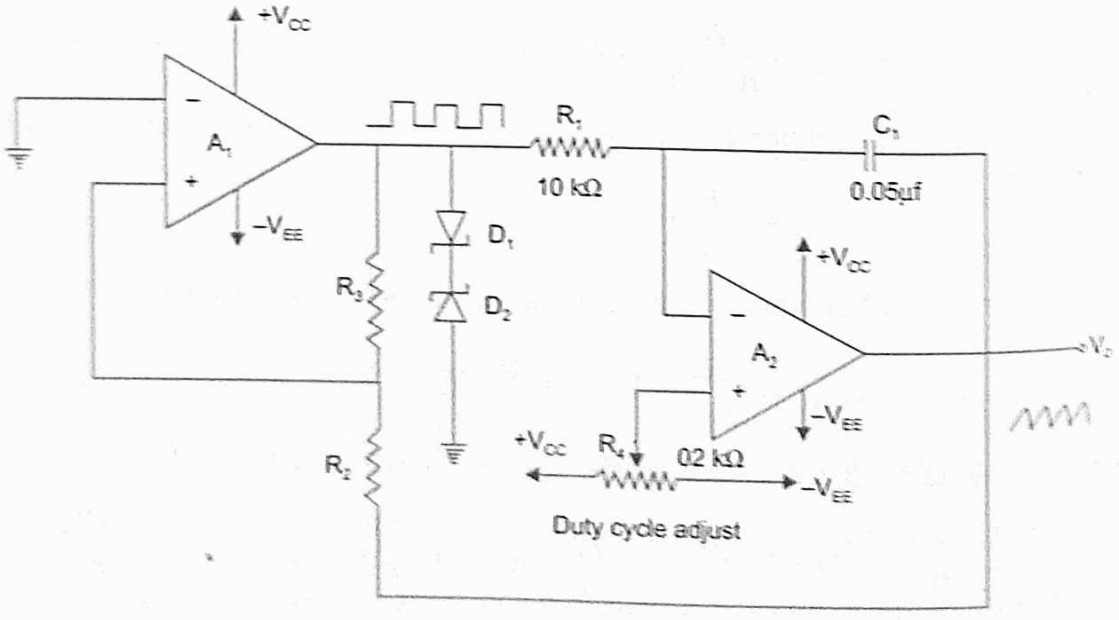


Fig. 5.14 Sawtooth Wave Generator

The triangular wave generator can be converted into a sawtooth wave generator by applying a variable dc voltage into the noninverting terminal of the integrator A_2. This can be accompalished by using the potentiometer and connecting it to the $+V_{CC}$ and $+V_{EE}$ as shown in Fig 5.14.

Depending on the R_1 setting, a certain dc level is inserted in the output of A_2. Now, suppose that the output of A_1 is a square wave and the potentiometer R_4 is adjusted for a certain dc level. This means that the output of A_2 will be a triangular wave, rising on some dc level that is a function of the R_4 setting. The duty cycle of the square wave will be determined by the polarity and amplitude of this dc level. A duty cycle less than 50% will then cause the output of A_2 to be a sawtooth. With the wiper at the center of R_4, the output of A_2 is a triangular wave. For any other position of R_4 wiper, the output is a sawtooth waveform. Specifically as the R_4 wiper is moved toward $-V_{EE}$, the rise time of the sawtooth wave becomes longer than the fall time as shown in Fig 5.15.

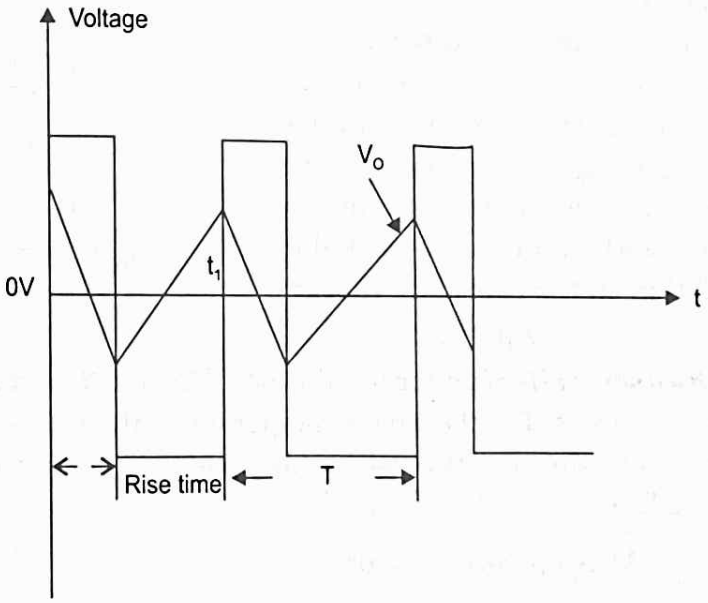


Fig. 5.15 Sawtooth waveform

On the otherhand, as the wiper is moved towards $+V_{CC}$, the fall time becomes longer than the rise time. Also, the frequency of the Sawtooth decreases as R_4 is adjusted towards $+V_{CC}$ or $-V_{EE}$

However, the amplitude of the sawtooth wave is independent of the R_4 setting.

Example 5.4

Design a sawtooth wave generator for 10V peak and frequency of 200 Hz. Assume $V_i = 2V$ and $V_{ref} = 10V$.

Solution

The ramp signal rises at a rate of 2V/ms. Therefore, choose a time constant of R_1C to produce a time period of 1.0 ms.

Let $R_1 = 10\ k\Omega$ and $C = 0.1\ \mu F$. We know that $f = \left(\frac{1}{R_1C}\right)\frac{V_i}{V_{ref}}$

Therefore $$f = \frac{1}{(10\times10^3)(0.1\times10^{-6})}\left(\frac{2}{10}\right) = 200\ Hz$$

5.7 BASIC PRINCIPLE OF SINE WAVE OSCILLATORS

The basic structure of sine wave oscillators based on the use of feedback in amplifiers is shown in Fig. 5.16. It consists of an amplifier with gain A and a frequency selective feedback network (having inductor or capacitive components) with the transfer ratio β. It may be noted that the loop is incomplete as the terminal 2 is not connected to terminal 1. To understand the operation of the circuit, consider the situation where an input signal v_i is applied at the input terminal 1 of the amplifier, so that the output $v_o = A\, v_i$. The feedback signal v_f at terminal 2, therefore is $v_f = A\beta\, v_i$. The quantity Aβ, therefore, represents the loop gain of the system. If the values of A and β are adjusted so that Aβ = 1, the feedback signal v_f will be identically equal to the externally applied signal v_i. If the terminal 2 is now connected to terminal 1 and the external signal v_i is removed, the circuit will continue to provide output as the amplifier can not distinguish whether v_i is coming from external source or from the feedback circuit. Thus, output signal can be continuously obtained without any input signal if we can satisfy the condition on the loop gain, that is,

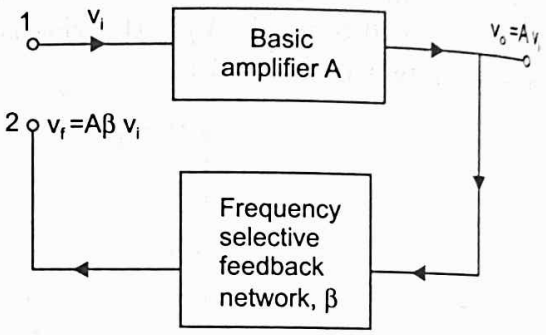


Fig. 5.16 Basic structure of a feedback oscillator

$$A\beta = 1 \tag{5.24}$$

This is called ***Barkhausen criterion*** for oscillations. The condition Aβ = 1 can be satisfied only at one specific frequency, f_o for the given component values. The circuit thus provides output at frequency, f_o where the circuit components meets the condition given by Eq. (5.24). We may rewrite Eq. (5.24) as

$$A(j\omega_o)\, \beta(j\omega_o) = 1 \angle 0° \tag{5.25}$$

There are infact two conditions in Eq. (5.25), one on phase and other on the magnitude of the loop gain which needs to be simultaneously satisfied to achieve oscillations. Thus, according to Eq. (5.25) the total phase shift of the loop gain should be zero or multiples of 2π and the magnitude of the loop gain, Aβ should be equal to unity. That is

$$|A\beta| = 1 \tag{5.26}$$

$$\angle A\beta = 0° \text{ or multiples of } 2\pi \tag{5.27}$$

The condition $|A\beta| = 1$ is usually difficult to maintain in the circuit as the values of A and β vary due to temperature variations, aging of components, change of supply voltage etc. If $|A\beta|$ becomes less than unity, the feedback signal v_f goes on reducing in each feedback cycle and the oscillations will die down eventually. In order to ensure that the circuit sustains oscillations inspite of variations, the circuit is designed so that $|A\beta|$ is slightly greater than unity. Now, the output amplitude will go on increasing with every feedback cycle. The signal, however, can not go on increasing and gets limited due to the non-linearity of the device, that is as the transistor enters into saturation. Thus it is the non-linearity of the transistor because of which the sustained oscillations can be achieved. The value of Aβ is usually kept greater by about 1 to 5% to ensure that $|A\beta|$ does not fall below unity. In explaining the principle of oscillation

in Fig. 5.14, we had assumed that we first connect a signal source to start the oscillations and later remove it. In a practical oscillator, however, it is not done so. The output waveform is obtained as soon as power is turned on. Actually, there is noise signal always present at the input (i.e. base) of the transistor due to temperature (called Johnson's noise) or variation in the carrier concentration (Schottky noise). The noise signal at the frequency at which the circuit satisfies the condition $|A\beta| = 1$ is picked up and amplified. Since $|A\beta| > 1$ in the circuit, the output signal goes on increasing until it is limited by the onset of non-linearity of the transistor (as transistor enters into saturation) as shown in Fig. 5.15.

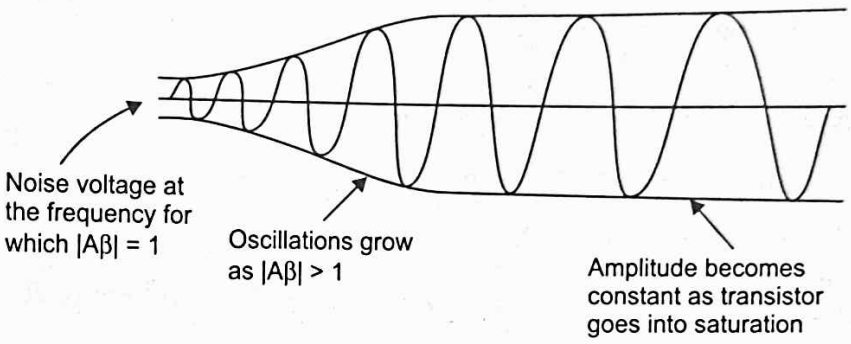


Fig. 5.17 Showing constant output amplitude as transistor goes into saturation ($|A\beta| > 1$)

There are different types of sine-wave oscillators available according to the range of frequency. The RC-phase shift oscillators can provide frequencies varying from a few hertz to several hundred kHz. LC oscillators are suitable for high frequencies up to hundreds of MHz. Here we will discuss only two types of audio frequency RC phase shift oscillators.

RC-Phase Shift Oscillator

The circuit of an RC-phase shift oscillator is shown in Fig. 5.16 (a). The op-amp is used in the inverting mode and therefore provides 180° phase shift. The additional phase of 180° is provided by the RC feedback network to obtain a total phase shift of 360°. The feedback network consists of three identical RC stages. Each of the RC stage provides a 60° phase shift so that the total phase shift due to feedback network is 180°. It is not necessary that all the three RC sections are identical so long the total phase shift is 180°. However, if we use non-identical stages, it is possible that the total phase shift is 180° for more than one frequency. This phenomenon can lead to undesirable inter-modal oscillations.

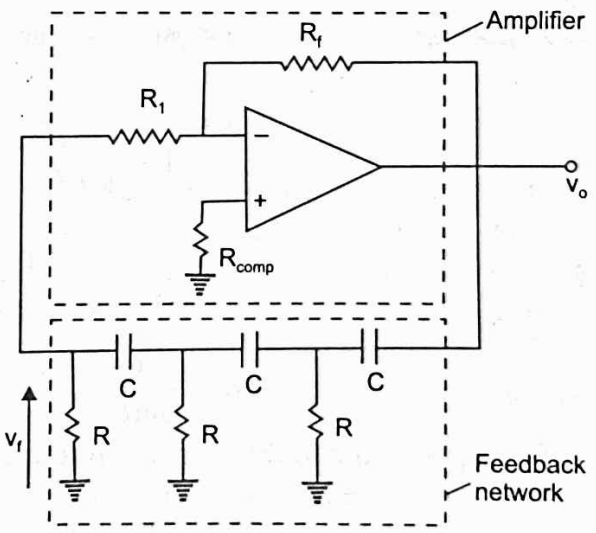


Fig. 5.18 (a) Phase shift oscillator

The feedback factor β of the RC network can be calculated by writing the KVL equations from Fig. 5.16 (b).

$$I_1\left(R+\frac{1}{sC}\right)-I_2R = V_o \qquad (5.28)$$

$$-I_1R+I_2\left(2R+\frac{1}{sC}\right)-I_3R = 0 \qquad (5.29)$$

$$0-I_2R+I_3\left(2R+\frac{1}{sC}\right) = 6 \qquad (5.30)$$

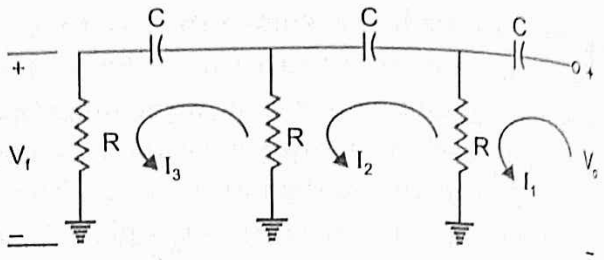


Fig. 5.18 (b) Calculating β from the phase shift network

and $$V_f = I_3R \qquad (5.31)$$

Solving Eqs. (5.28), (5.29) and (5.30) for I_3, we get

$$I_3 = \frac{V_oR^2s^3C^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3} \qquad (5.32)$$

and $$V_f = I_3R = \frac{V_oR^3s^3C^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3} \qquad (5.33)$$

$$= \frac{1}{1+\frac{6}{sRC}+\frac{5}{s^2C^2R^2}+\frac{1}{s^3C^3R^3}} \qquad (5.34)$$

Replacing $s = j\omega$, $s^2 = -\omega^2$ and $s^3 = -j\omega^3$, we get

$$\beta = \frac{1}{1-\frac{6}{j\omega RC}-\frac{5}{\omega^2R^2C^2}+\frac{1}{j\omega^3R^3C^3}} \qquad (5.35)$$

$$= \frac{1}{(1-5\alpha^2)+j\alpha(6-\alpha^2)} \qquad (5.36)$$

where $$\alpha = \frac{1}{\omega RC} \qquad (5.37)$$

For $A\beta = 1$, β should be real, that is the imaginary term in Eq. (5.36) must be zero. Thus

$$\alpha\,(6-\alpha^2) = 0 \qquad (5.38)$$

or, $$\alpha^2 = 6$$

$$\alpha = \sqrt{6}$$

That is, $$\frac{1}{\omega RC} = \sqrt{6}$$

The frequency of oscillation, f_o, is therefore given by

$$f_o = \frac{1}{2\pi RC\sqrt{6}} \qquad (5.39)$$

Putting $\alpha^2 = 6$ in Eq. (5.36), we get

$$\beta = -\frac{1}{29} \tag{5.40}$$

The negative sign indicates that the feedback network produces a phase shift of 180°.

So, $$|\beta| = \frac{1}{29}$$

Since $$|A\beta| \geq 1$$

Therefore, for sustained oscillations,

$$|A| \geq 29 \tag{5.41}$$

That is the gain of the inverting op-amp should be atleast 29, or $R_f = 29\ R_1$. The gain A_v is kept greater than 29 to ensure that variations in circuit parameters will not make $|A_v \beta| < 1$, otherwise oscillations will die out.

For low frequencies (< 1 kHz), op-amp 741 may be used, however, for high frequencies, LM 318 or LF 351 should be used.

Example 5.5

Design a phase shift oscillator of Fig. 5.17 to oscillate at 100 Hz.

Solution

Let $C = 0.1\ \mu F$. Then from Eq. (5.25)

$$R = \frac{1}{\sqrt{6}\ 2\pi (10^{-7})(100)} = 6.49\ k\Omega$$

Use $R = 6.5\ k\Omega$

To prevent loading of the amplifier by RC network, $R_1 \leq 10\ R$

Therefore, let $R_1 = 10\ R = 65\ k\Omega$

Since $R_f = 29\ R_1$

$R_f = 1885\ k\Omega$

Wien Bridge Oscillator

Another commonly used audio frequency oscillator is a Wien bridge oscillator. The circuit is shown in Fig. 5.19. It may be noted that the feedback signal in this circuit is connected to the non-inverting (+) input terminal so that the op-amp is working as a non-inverting amplifier. Therefore, the feedback network need not provide any phase shift. The circuit can be viewed as a Wien bridge with a series RC network in one arm and a parallel RC network in the adjoining arm. Resistors R_1 and R_F are connected in the remaining two arms. The condition of zero phase shift around the circuit is achieved by balancing the bridge.

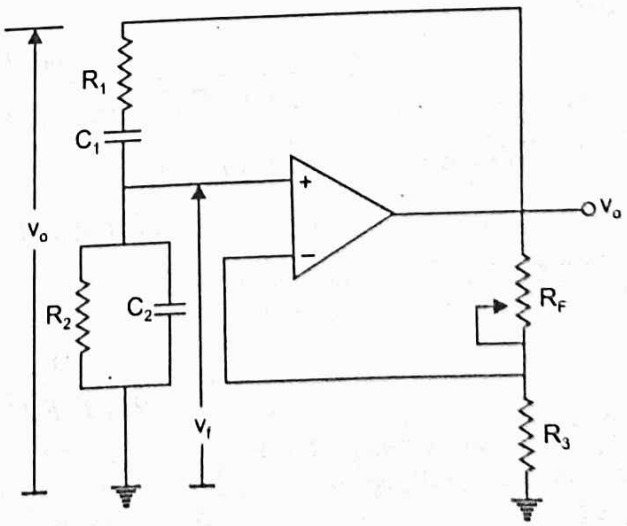


Fig. 5.19 Wien bridge oscillator

The circuit has been redrawn to show the bridge network in Fig. 5.20. The output ac signal of the op-amp amplifier is fed back to point A of the bridge. The feedback signal, V_f across the parallel combination R_2C_2 is applied to the non-inverting input terminal of the op-amp. The gain of the op-amp amplifier is

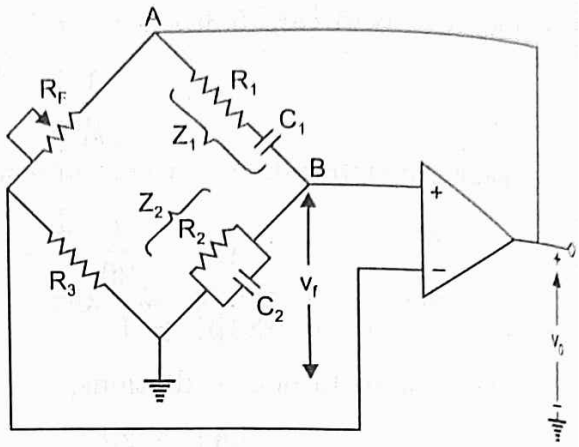


Fig. 5.20 Wien bridge oscillator showing the bridge network

$$A = 1 + \frac{R_F}{R_3} \tag{5.42}$$

and feedback factor, β from Fig. 5.18 is

$$\beta = \frac{V_f}{V_o} = \frac{Z_2}{Z_1 + Z_2} \tag{5.43}$$

where $$Z_1 = R_1 + \frac{1}{sC_1} = \frac{sR_1C_1 + 1}{sC_1} \tag{5.44}$$

$$Z_2 = \frac{R_2}{1 + sR_2C_2} \tag{5.45}$$

Putting the values of Z_1 and Z_2 in Eq.(5.43), we get

$$\beta = \frac{R_2/(1 + R_2C_2s)}{\frac{1 + sR_1C_1}{sC_1} + \frac{R_2}{1 + sR_2C_2}} \tag{5.46}$$

$$= \frac{sR_2C_1}{1 + s(R_1C_1 + R_2C_2 + R_2C_1) + s^2R_1R_2C_1C_2} \tag{5.47}$$

Putting $s = j\omega$,

$$\beta = \frac{j\omega R_2C_1}{1 + j\omega(R_1C_1 + R_2C_2 + R_2C_1) - \omega^2R_1R_2C_1C_2} \tag{5.48}$$

In order β to be a real quantity

$$1 - \omega^2R_1R_2C_1C_2 = 0$$

Thus, the frequency of oscillation,

$$f_o = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} \tag{5.49}$$

and

$$\beta = \frac{R_2C_1}{R_1C_1 + R_2C_2 + R_2C_1} \tag{5.50}$$

For $R_1 = R_2 = R$ and $C_1 = C_2 = C$,

$$f_o = \frac{1}{2\pi RC} \tag{5.51}$$

and

$$\beta = \frac{1}{3} \tag{5.52}$$

Since $|A\beta| \geq 1$ for sustained oscillations,

$|A| \geq 3$

Since

$$A = 1 + \frac{R_F}{R_3}$$

$$3 = 1 + \frac{R_F}{R_3}$$

or,

$$R_F = 2R_3 \tag{5.53}$$

If the gain $|A| > 3$, sometimes oscillations keep growing and it may clip the output sinewave. This problem is eliminated by a practical Wien bridge oscillator with adaptive negative feedback as shown in Fig. 5.21. In this circuit, resistor R_4 is initially adjusted to give a gain so that oscillations start. The output signal grows in amplitude until the voltage across R_3 approaches the cut-in voltage of the diode. As the diodes begin to turn-on (one for the positive half cycle and the other for the negative half cycle), the effective feedback resistance R_F decreases because the diode is in parallel with the resistance R_3. This will reduce the gain of the amplifier which in turn lowers the output amplitude. Hence sustained oscillations can be obtained. Further, if the output signal falls, the diodes would begin to turn-off thereby increasing R_F which in turn increases gain.

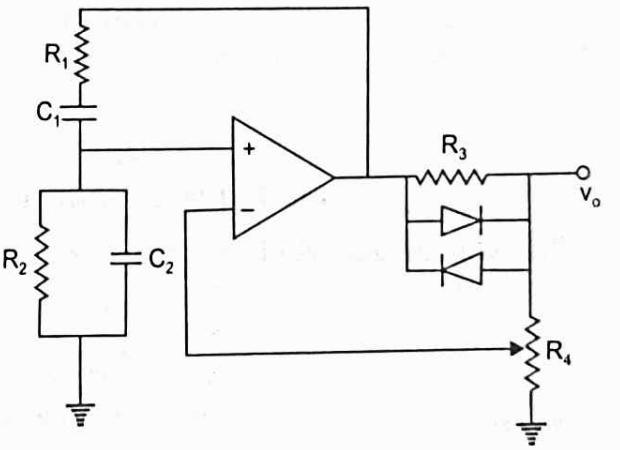


Fig. 5.21 Practical Wien bridge oscillator with adaptive negative feedback

The two op-amp RC oscillator circuits studied are suitable for the frequency range of 10 Hz to 100 kHz (maximum 1 MHz). The size of R and C components becomes very large for generating low frequencies. Thus, the low frequency limit is dictated by the size of passive components required. The upper frequency limit is governed by the frequency response and slew rate limit of the op-amp used. For generating high frequencies in the RF range, the oscillator circuits are usually designed using BJT and LC tuned circuits or crystal oscillators.

LC Oscillators

For generating high frequency sine waves in the RF range, LC tuned circuits are used. The most commonly used LC oscillators are Colpitts oscillator and Hartley oscillator which are discussed here.

Generalized oscillator circuit

A number of *LC* oscillator circuits can be analyzed by considering a generalized oscillator circuit shown in Fig. 5.22 (a). The analysis assumes that due to high input impedance of op-amp the feedback network consisting of impedances Z_1, Z_2 & Z_3 does not load the amplifier. On the ac equivalent circuit shown in Fig. 5.22 (b) op-amp is replaced with an open circuit voltage gain source A_V with output resistance R_0, and the loop broken at terminal 1.

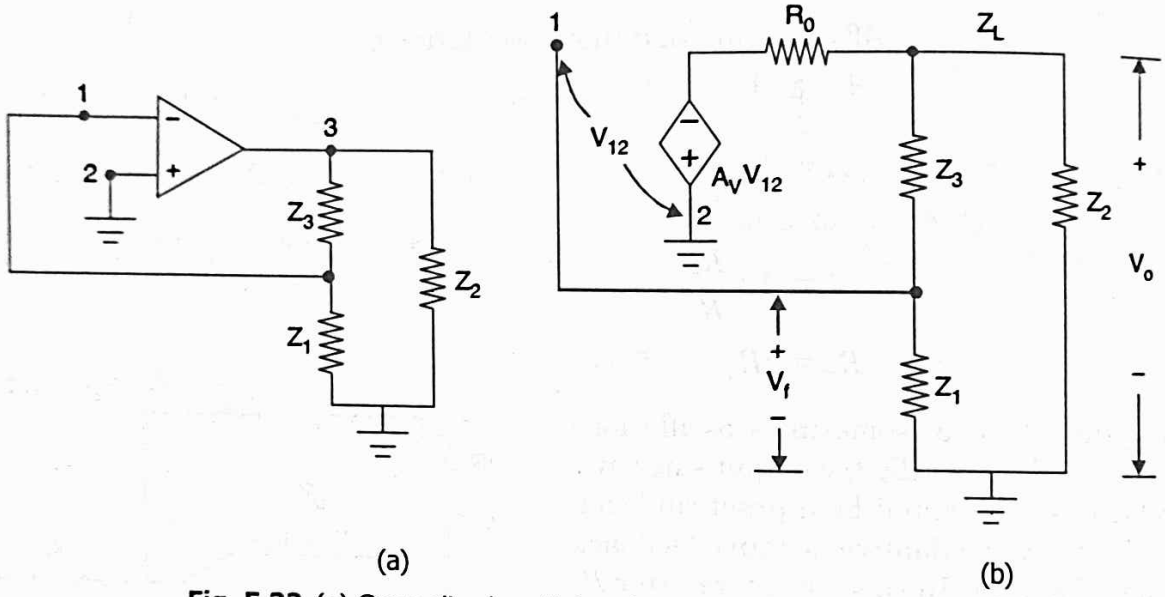


Fig. 5.22 (a) Generalized oscillator circuit, (b) ac equivalent circuit

The voltage gain A of the amplifier is given by

$$A = \frac{V_0}{V_{12}} = -\frac{A_V Z_L}{R_0 + Z_L} \tag{5.54}$$

where

$$Z_L = Z_2 \parallel (Z_1 + Z_3) \tag{5.55}$$

$$= \frac{Z_2(Z_1 + Z_3)}{Z_1 + Z_2 + Z_3} \tag{5.56}$$

Putting the value of Z_L in Eq. (5.54), we get

$$A = \frac{-A_V Z_2(Z_1 + Z_3)}{R_0(Z_1 + Z_2 + Z_3) + Z_2(Z_1 + Z_3)} \tag{5.57}$$

Feedback factor β is,

$$\beta = \frac{V_f}{V_0} = \frac{Z_1}{Z_1 + Z_3} \tag{5.58}$$

The loop gain $A\beta$ is obtained as,

$$A\beta = \frac{-A_V Z_1 Z_2}{R_0(Z_1 + Z_2 + Z_3) + Z_2(Z_1 + Z_3)} \tag{5.59}$$

In LC oscillators, impedances Z_1, Z_2 and Z_3 are pure reactances (either inductive or capacitive), so that $Z_1 = jX_1$, $Z_2 = jX_2$ and $Z_3 = jX_3$ where $X = \omega L$ (for inductance) and $X = -1/\omega C$ for (capacitance). Equation (5.59) now becomes

$$A\beta = \frac{A_V X_1 X_2}{jR_0(X_1 + X_2 + X_3) - X_2(X_1 + X_3)} \tag{5.60}$$

For sustained oscillations, loop gain $A\beta$ must be real. This is possible if in Eq. (5.60),

$$X_1 + X_2 + X_3 = 0 \tag{5.61}$$

The circuit thus oscillates at the frequency at which Eq. (5.61) is satisfied. At this frequency, Eq. (5.60) becomes,

$$A\beta = \frac{A_V X_1}{X_2} \tag{5.62}$$

In order that loop gain $A\beta$ is positive, the reactances X_1 and X_2 should be of the same sign, *i.e.*, X_1 and X_2 both should be either inductance or capacitance.

Based upon the above analysis, we can have two types of oscillator circuits. If X_1 and X_2 are capacitors and X_3 is an inductor, the circuit is called **Colpitt's oscillator**. If X_1 and X_2 are inductors and X_3 is a capacitor, the circuit is called **Hartley oscillator**. The analysis of both types of oscillators is discussed now.

Colpitt's Oscillator

In the Colpitt's oscillator shown in Fig. 5.21.

$$X_1 = -\frac{1}{\omega C_1}; \quad X_2 = -\frac{1}{\omega C_2} \ \& \ X_3 = \omega L$$

Putting the values of X_1, X_2 & X_3 in Eq. (5.61), we get

$$-\left(\frac{1}{\omega C_1} + \frac{1}{\omega C_2}\right) + \omega L = 0$$

or

$$\omega L = \frac{1}{\omega C_1} + \frac{1}{\omega C_2}$$

The angular frequency of oscillation, ω_0 is obtained as

$$\omega_0 = \frac{1}{\sqrt{L}} \sqrt{\frac{C_1 C_2}{C_1 + C_2}}$$

The condition on the voltage gain is obtained from Eq. (5.62), i.e.

$$A\beta = A_V \frac{X_1}{X_2} = \geq 1$$

i.e.

$$|A_V| \geq \frac{X_2}{X_1}$$

or $$|A_V| \geq \frac{C_1}{C_2}$$

Thus the frequency of oscillation for the Colpitt's oscillator is

$$f_0 = \frac{1}{2\pi\sqrt{LC_T}}$$

where $$C_T = C_1 \,||\, C_2 = \frac{C_1 C_2}{C_1 + C_2}$$

and $$|A_V| \geq \frac{C_1}{C_2}$$

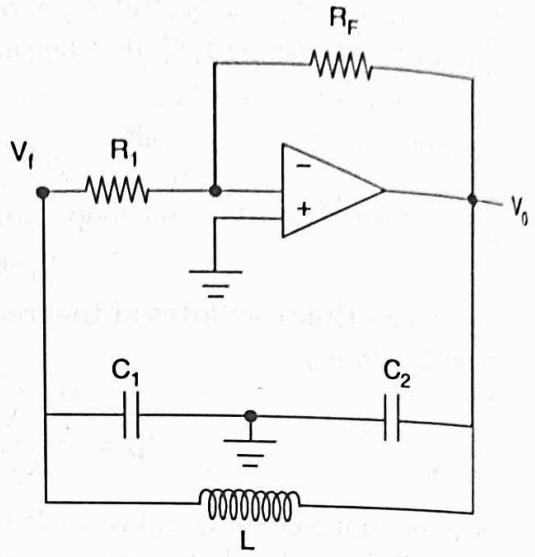


Fig. 5.23 Colpitt's Oscillator

Hartley Oscillator

The circuit diagram of Hartley oscillator is shown in Fig. 5.24.

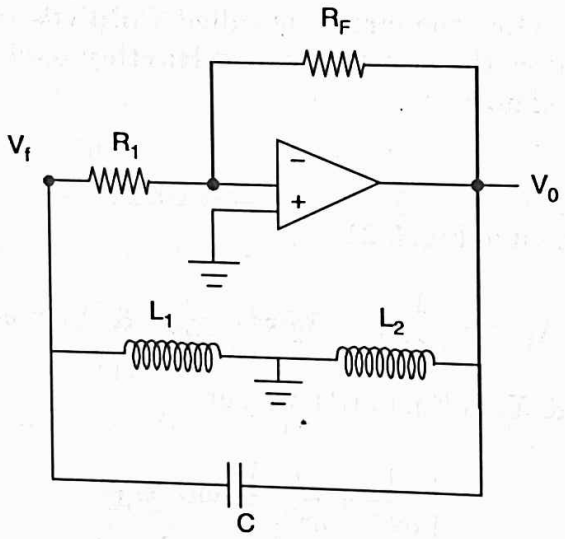


Fig. 5.24 Hartley Oscillator

In Fig. 5.24,

$$X_1 = \omega L_1; \quad X_2 = \omega L_2 \;\&\; X_3 = -\frac{1}{\omega C}$$

using Eq. (5.61) the angular frequency of oscillator is given by

$$\omega_0 = \frac{1}{\sqrt{C}}\sqrt{\frac{1}{(L_1 + L_2)}}$$

or $$f_0 = \frac{1}{2\pi\sqrt{CL_T}}$$

where $$L_T = L_1 + L_2$$

$$L_T = L_1 + L_2 + 2M$$

or

where M is the mutual conductance of inductors L_1 and L_2.

The condition on the gain for sustained oscillations is that the loop gain must be greater than unity.

Thus

$$|A_V| \geq \frac{L_2}{L_1}$$

Quadrature and Biphasic Oscillators

Signals that are of same frequency but have a phase shift of 90° with respect to each other are called quadrature signals. An example of quadrature signals is sine and cosine waves shown in Fig. 5.25 (a). It may be noted that the distinction between sine and cosine waves is meaningless unless both are present or a timing method is used to establish 'zero degrees' point.

The circuit of a quadrature oscillator that generates both sine and cosine wave is shown in Fig. 5.25 (b). It consists of two op-amps A_1 and A_2. Both the op-amps are used as Miller integrators, where A_1 is non-inverting type and A_2 is inverting integrator. The output of A_1 (i.e. V_{o1}) is assumed to be a sinewave output. In order to obtain sinewave output a total of 360° phase shift is required between the output of A_1, around the loop and back to the input of A_1. The op-amp A_2 provides 180° phase shift as A_2 is used in the inverting configuration, another 90° phase shift is obtained from A_2 as an integrator and the remaining 90° phase shift is provided by R_3C_3 network. If $R_1 = R_2 = R_3 = R$ and $C_1 = C_2 = C_3 = C$, then the frequency of oscillation is given by:

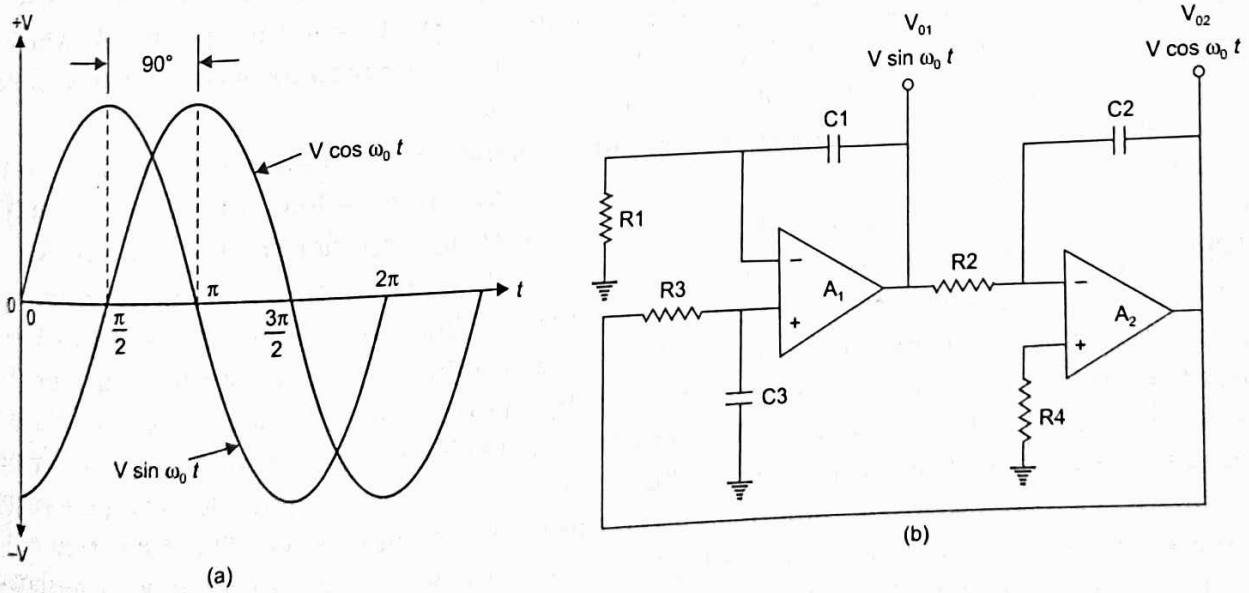


Fig. 5.25 (a) Quadrature sine cosine waves (b) Quadrature oscillator circuit

$$f = \frac{1}{2\pi RC} \tag{5.63}$$

At this frequency,

$$A = \frac{1}{\beta} = 1.414 \tag{5.64}$$

The cosine output (V_{o2}) is taken from the output of amplifier A_2. The relative amplitudes are approximately equal, but the phase is shifted by 90° between the two stages.

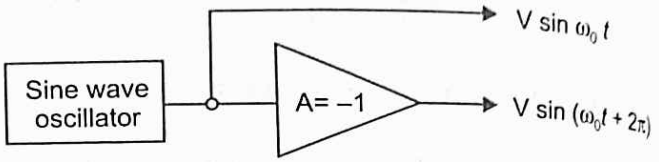


Fig. 5.26 Biphasic oscillator

A biphasic oscillator is a sine wave oscillator that outputs two identical sine wave signals that are 180° out of phase with each other. The block diagram is shown in Fig. 5.26 and consists of a sine wave oscillator followed by an inverting amplifier that has a gain of one. The output of the sine wave oscillator is $V \sin \omega_0 t$ while the output of the inverter is $V \sin (\omega_0 t + 2\pi)$.

Function Generator

We have earlier discussed circuits that generates a square wave, triangular wave or a sine wave. A function generator, however, produces all three types of waveforms simultaneously. It is possible to achieve frequencies from very low (~ 0.01 Hz) to very high (>10 MHz) without significant distortion.

The circuit of a function generator using 3 op-amps is shown in Fig. 5.27 (a). The op-amp A_2 produces a square wave as it is used as a two level comparator or a Schmitt trigger. One should use a high speed comparator such as LM 311 in place of 741 C to produce a square wave with faster rise and fall times. The square wave output from A_2 is fed to op-amp A_1 which is used as an integrator. The output of op-amp A_1 is, therefore a triangular waveform. The switch S_1 selects the capacitor and thus the operating frequency.

The op-amp A_3 is used as a sine shaper circuit. It shapes the triangle wave into a sine wave as shown in Fig. 5.27 (b). When the triangle wave's amplitude is low, all the diodes in A_3's feedback path are off. The op-amp A_3 works as an inverting amplifier with a gain $-R_f/R_4$.

The output, therefore is shown by line segment OA. When the output attains the amplitude A at time 1, a diode in the feedback path forward biases. This places a resistor is parallel with R_F thus lowering the feedback resistance. This in turn reduces the gain of the amplifier. The output, therefore, rises at a slower rate, as seen by the segment AB. Now, a second diode in the feedback path gets turned on further reducing the feedback resistance. The amplifier gain and in turn the slope of the output wave reduces once more in the segment BC. The sine shaper thus produces a sine wave by rounding off the tips of the triangle wave. The distortion of the sine wave thus produced is very high compared to the sine waves generated by RC oscillators. However, this is the only practical way to produce sine waves whose frequencies vary from very low (0.01 Hz) to very high (over 10 MHz).

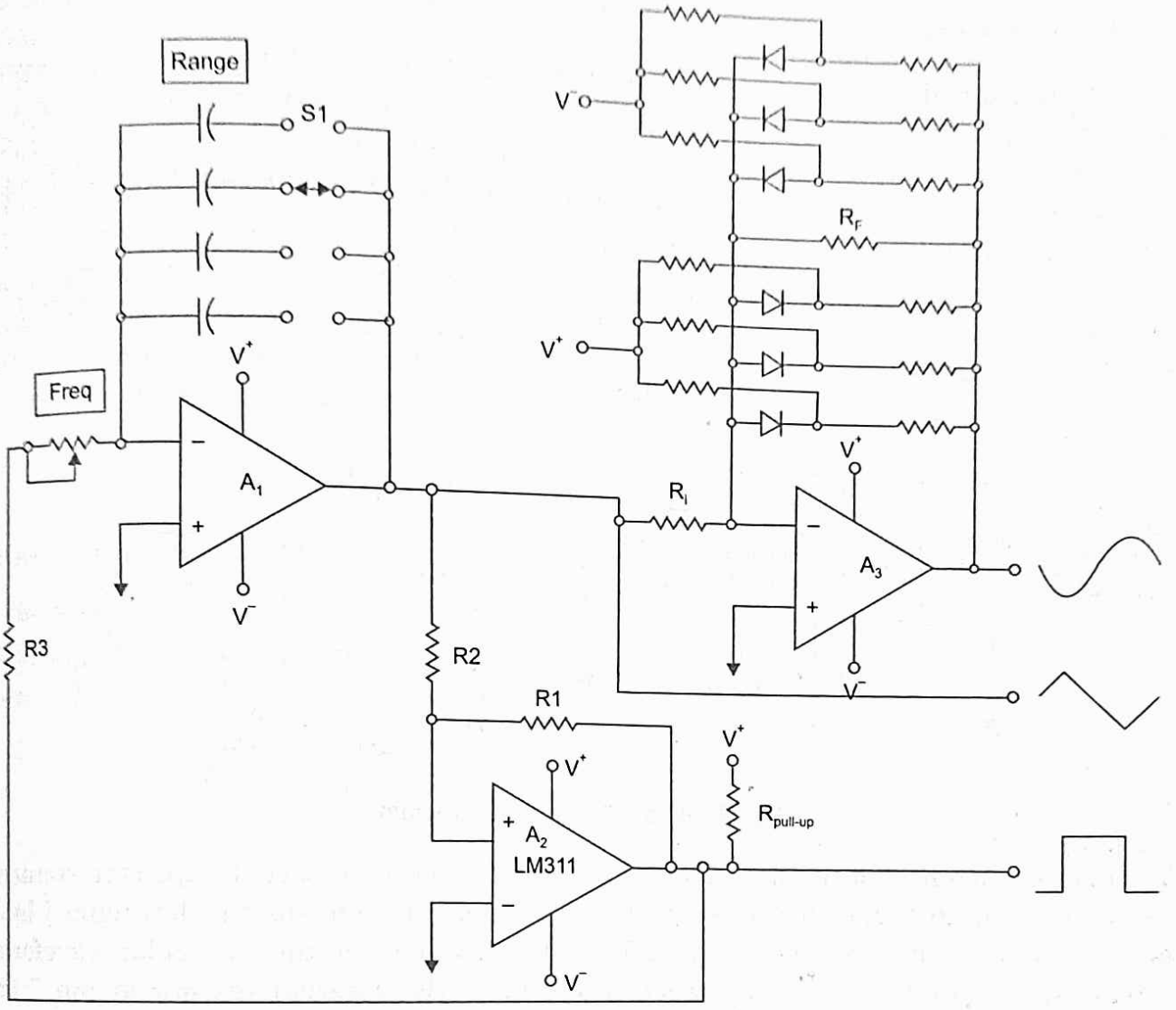


Fig. 5.27 (a) A function generator using 3 op-amps

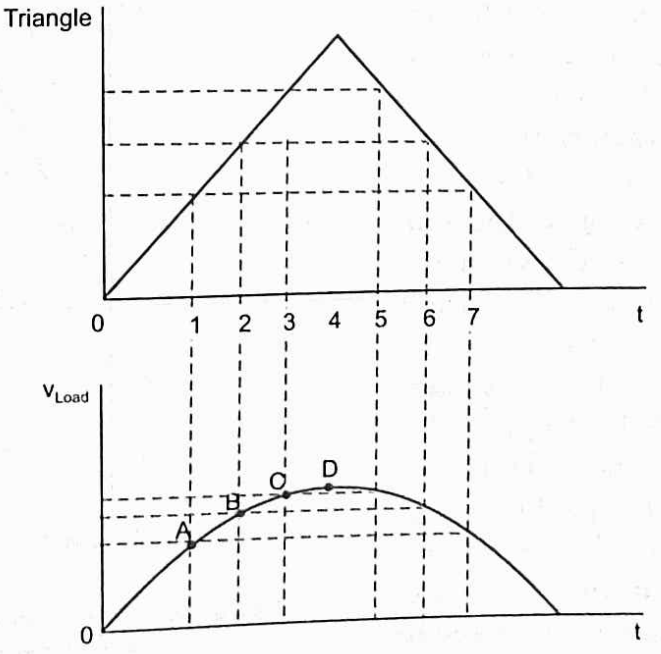


Fig. 5.27 (b) Showing operation of sine shaper

IC Function Generator

The XR-2206 is a widely used monolithic IC which can be used to build a function generator with the addition of only a few external components. It produces a triangle, square wave, sine wave and variable duty cycle pulse. It allows amplitude modulation (AM), frequency modulation (FM) and frequency shift keying (FSK) signals as well. The block diagram for the XR-2206 is shown in Fig. 5.28 (a).

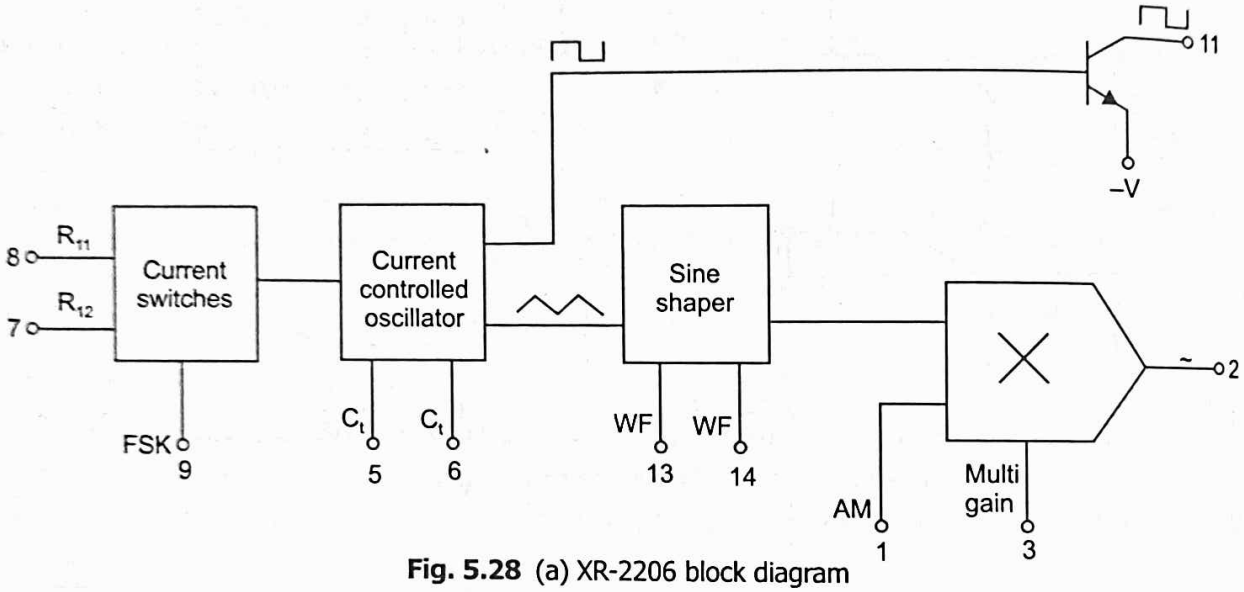


Fig. 5.28 (a) XR-2206 block diagram

A constant current I is used to charge and discharge an external capacitor connected between pin 5 and 6 of the current controlled oscillator. The current I is determined by the external resistors connected to pin 7 or 8. Thus, the frequency of the triangular waveform is controlled by external capacitor (between 5 and 6) or the external resistor at pin 7 or 8. A comparator within the current controlled oscillator produces a 50% duty cycle square wave which drives an open collector buffer. The triangular wave output from the current controlled oscillator is fed to the sine shaper circuit. The transfer characteristics of the sine shaper is shown in Fig. 5.28 (b).

When pins 13 and 14 are open, the gain of the sine shaper is linear as shown by the solid line in Fig. 5.25 (b), and the output from the sine shaper is also a triangle wave. However, if we connect a 180 Ω resistor between the pins 13 and 14, the transfer curve changes to the one shown by dotted line in Fig. 5.28 (b). The peaks of the triangle wave have got rounded to produce a sine wave. The output from the sine shaper is fed to the multiplier (discussed in

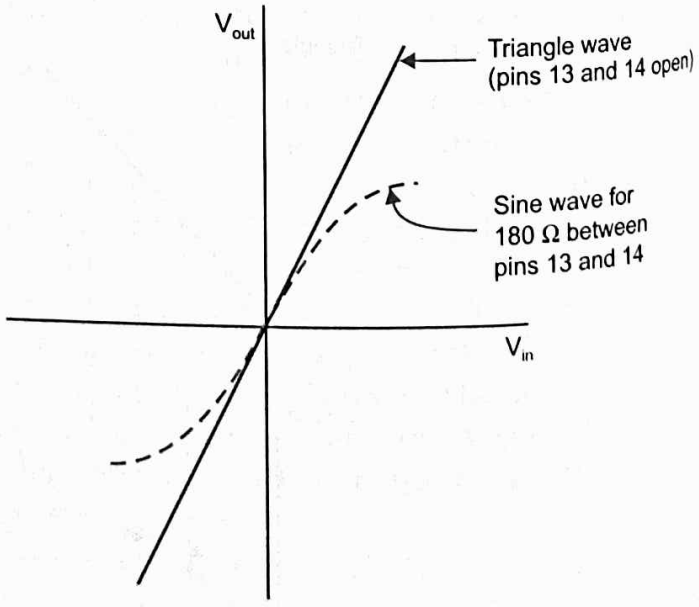


Fig. 5.28 (b) Transfer characteristics of sine shaper circuit

sec. 4.9). The output from the multiplier is the product of two inputs scaled by a multiplication gain factor. If a varying dc voltage is connected at pin 1, the amplitude of the output (sine or triangle) can be controlled. And, if we apply a low frequency sine wave to pin 1, the amplitude of the output will vary sinusoidally giving an amplitude modulated output. The output amplitude can also be controlled by changing the multiplying factor.

XR-2206 is available in a 14-pin package as shown in Fig. 5.29 (a). Power is applied between the V^+(pin 4) and V^-(pin 12) inputs. The difference of potential ($V^+ - V^-$) should be at least 10 V but less than 26 V. If a single supply is to be used, the pin 12 is grounded. Frequency can be controlled by three set of pins: Capacitor (1000 pF < C < 100 μF) between pin 5 and 6, a resistor between pin 7 and 8, a voltage at FSK (pin 9). The frequency of the output waveform is set by the current through the resistor R connected at pin 7 and is given by

$$f = \frac{0.32I}{C}$$

This current must flow out of the IC and is kept within the limits

$$1\ \mu A < I < 3\ mA$$

The voltage at pin 7 is kept 3V above V^- as shown in Fig. 5.29 (b). The current through the resistor R is given by

$$I = \frac{3V}{R}$$

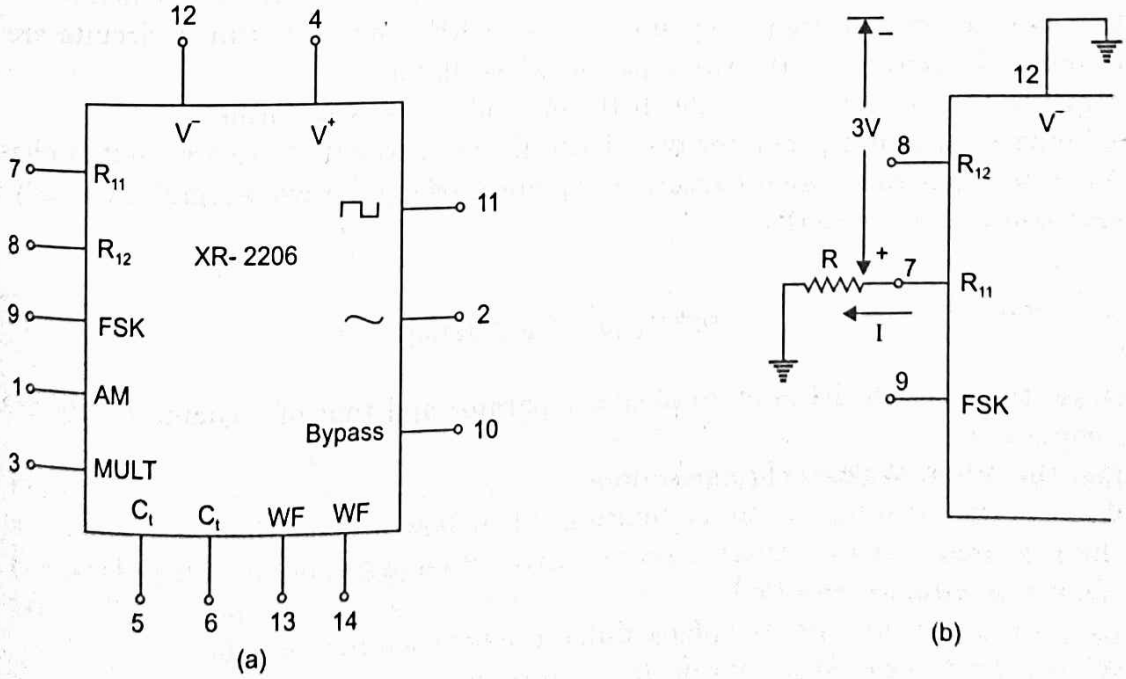


Fig. 5.29 (a) Pin configuration of XR-2206 (b) Circuit for setting the current I

SUMMARY

1. A comparator is an open loop op-amp with analog inputs and a digital output ($\pm V_{sat}$ or V_{CC}).
2. Reduced output voltage levels can be obtained by using back-to-back zener diodes at the output.
3. Zero crossing detector is a comparator with $V_{ref} = 0$.
4. A window detector determines when an unknown input is between two threshold levels.
5. Schmitt trigger is a comparator with positive feedback.
6. In Schmitt trigger, the input voltage triggers the output every time it exceeds certain voltage levels called upper threshold V_{UT} and lower threshold V_{LT}.
7. A Schmitt trigger converts slowly varying waveforms into square wave.
8. The frequency of a square wave generator depends upon the RC components and the trigger levels of the comparator.
9. A monostable multivibrator is used to generate pulses of desired duration and is also called a gating circuit.
10. A triangular wave can be generated by integrating a square wave.
11. A sawtooth waveform has unequal rise time and full time.
12. A triangular wave generator can be converted into a sawtoolh wave generator simply by applying a variable dc voltage to the non-inverting terminal of the integrator op-amp.
13. For self-sustained oscillation, two conditions must be satisfied:
    (i) The magnitude of the loop gain $A_v\beta$ must be equal to 1.
    (ii) The total phase shift of the loop gain must be 0°.
14. The phase shift and Wien bridge are the most commonly used sine wave oscillators for audio frequencies. The frequency of oscillation depends upon RC components.
15. For generating high frequency sine waves in RF range, LC tuned circuits are used. Colpitt's & Hartley are the two types of LC oscillators.
16. A quadrature oscillator generates both sine and cosine waveforms.
17. A biphasic oscillater generates two identical sine waves that are 180° out of phase.
18. A function generator can produce sine, square & triangular wave simultaneaously and is very useful in laboratories.

REVIEW QUESTIONS

5.1. Draw the characteristics of an ideal comparator and that of a commercially available comparator.
5.2. List the different types of comparators.
5.3. What is the meaning of voltage limiting? Show how it is obtained.
5.4. Draw a circuit for converting a square wave into a series of positive pulses.
5.5. What is a window detector?
5.6. Explain how to measure the phase difference between two signals.
5.7. What is hysteresis? What parameters determine the hysteresis?
5.8. Explain the operation of a square wave generator by drawing the capacitor and output voltage waveforms.

5.9. Explain how a non-symmetrical square wave can be obtained.
5.10. How would you recognize that positive feedback is being used in an op-amp circuit?
5.11. What is the other name of one shot?
5.12. Draw and explain the operation of a triangular wave generator.
5.13. What is the difference between a sawtooth wave and a triangular wave?
5.14. Draw and explain the operation of a sawtooth wave generator.
5.15. State the two conditions of oscillations.
5.16. Classify the oscillators.
5.17. In Wien bridge oscillator of Fig. 5.16, one set of circuit components determines the frequency of oscillation and another set of components determines if the circuit will oscillate at that frequency. Identify these two set of components.
5.18. Explain why RC oscillator can not generate high frequency signals?
5.19. How the frequency of oscillation is continuously varied in oscillator circuits?

PROBLEMS

5.1. Draw the input and output waveforms of the op-amp shown in Fig. P. 5.1.
5.2. Draw output of the op-amp shown in Fig. P. 5.2. (a) for given v_2 as in Fig. P. 5.2 (b) when (i) $V_1 = 0$ (ii) $V_1 = 4V$.

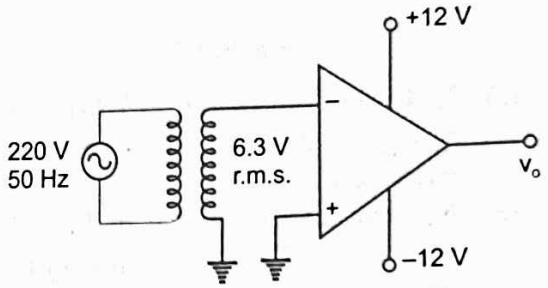


Fig. P. 5.1

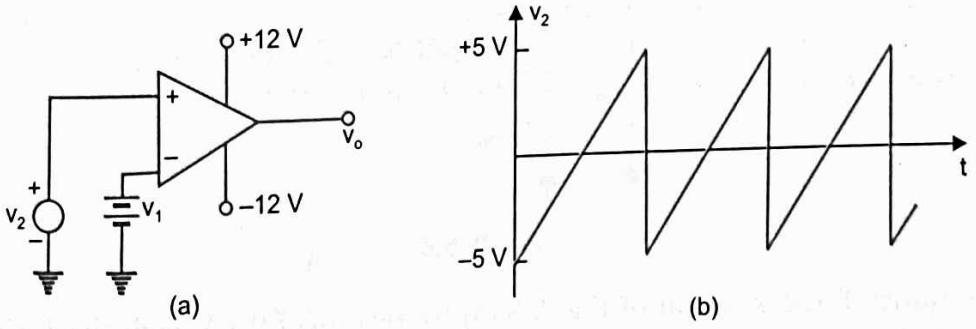


Fig. P. 5.2

5.3. For the circuit shown in Fig. P. 5.3, what is the condition of each of the LEDs for (i) v_i = 1 V (ii) v_i = 2 V.
5.4. For the circuit shown in Fig. P. 5.4, calculate the trigger points if supply voltage V = ±12 V. Plot the output voltage v_o vs t if v_i is a 100 Hz triangular wave of magnitude ±10 V.

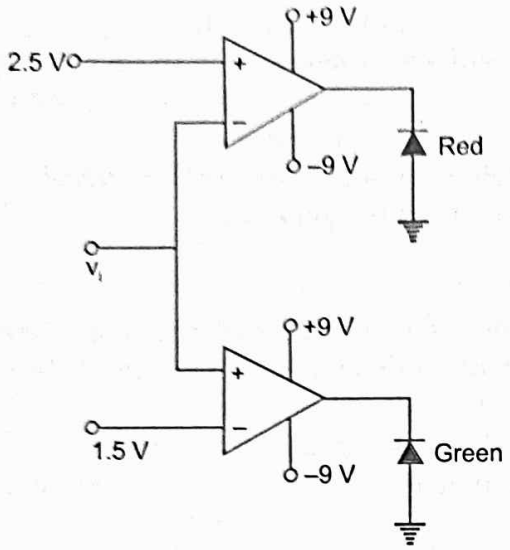


Fig. P. 5.3

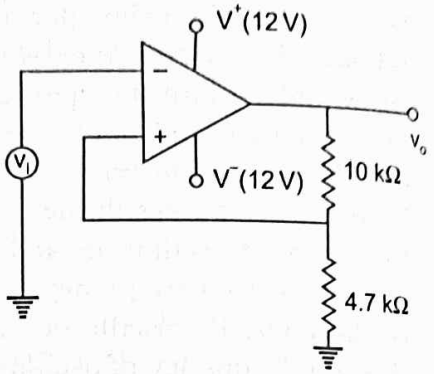


Fig. P. 5.4

5.5. In the circuit of Fig. 5.7 (a) v_i = 100 mV peak sine wave at 100 Hz, R = 1 kΩ and V_{Z1} = V_{Z2} = 6.2 V and the op-amp is a 741 with supply voltages = ±12 V. Draw the output waveform.

5.6. For the circuit shown in Fig. P. 5.6 v_i = 500 mV peak 100 Hz sine wave, R = 100 Ω, V_Z = 6.2 V, V_D = 0.7 V and supply voltages = ±15 V. Determine the output voltage swing and draw the output waveform.

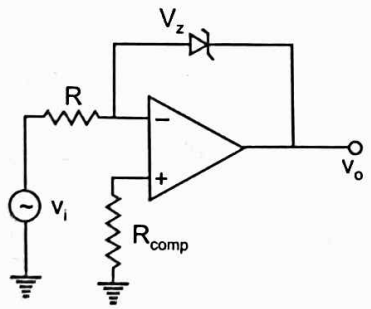


Fig. P. 5.6

5.7. In a Schmitt Trigger circuit of Fig. 5.8 (a) hysteresis of 0.1 V is desired. Calculate V_{ref}, V_{sat} and R_1 if V_{UT} = V_{ref}, A_{OL} = 100,000 and loop gain is 1000 and R_2 = 1 kΩ.

5.8. The Schmitt Trigger circuit of Fig. 5.8 (a) uses 9 V zener diodes. Calculate R_1/R_2 and V_{ref} if V_D = 0.7 V, V_{UT} = 0 and V_H = 0.2 V.

5.9. (a) In the Schmitt Trigger circuit of Fig. 5.8 (a), v_o = 8 V, V_{UT} = 4 V and V_{LT} = 3 V. Calculate R_1/R_2 and V_{ref}.

(b) Calculate the value of V_{ref} so that V_{LT} is negative.

(c) Calculate V_{ref} for V_{UT} = $-V_{LT}$.

5.10. For the non-inverting Schmitt comparator circuit shown in Fig. P. 5.10, calculate the threshold levels V_{UT} and V_{LT} and the hysteresis V_H.

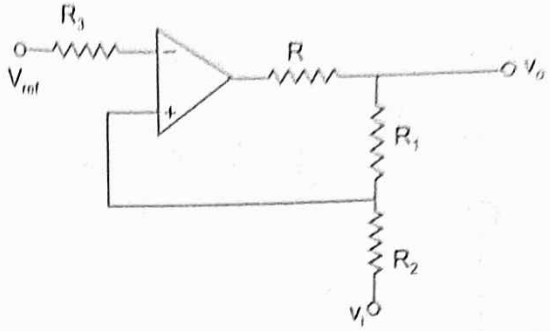


Fig. P. 5.10

5.11. In the square wave oscillator of Fig. 5.10 (a), calculate the frequency of oscillation if $R_2 = 10$ kΩ, $R_1 = 11.6$ kΩ, $R = 100$ kΩ, $C = 0.01$ μF.

5.12. Design a square wave oscillator for $f = 1$ kHz. The op-amp is a 741 with supply voltages ± 15 V.

5.13. Design a monostable multivibrator with trigger pulse shaping which will drive a LED *on* for 0.5 second each time it is pulsed.

EXPERIMENT 5.1

(a) To study the operation of 741 op-amp as a comparator.
(b) To design a Schmitt trigger for $V_{UT} = +0.5$ V and $V_{LT} = -0.5$ V and show its use for generating a square wave output.

(a) Comparator

PROCEDURE

1. Connect the circuit shown in Fig. E. 5.1 (a) and adjust the 10 kΩ potentiometer so that $V_{ref} = +0.5$ V.
2. Adjust the signal generator so that $v_i = 2$ V pp sine wave at 1 kHz.
3. Using a CRO observe the input and output waveform simultaneously. Plot the output waveform.
4. Adjust the 10 kΩ potentiometer so that $V_{ref} = -0.5$V. Repeat step 3.
5. To make a zero crossing detector, set $V_{ref} = 0$V and observe the output waveforms.

(b) Schmitt Trigger

Design: In Fig. E. 5.1 (b)

$$V_{UT} = \frac{R_2}{R_1 + R_2} V_{sat}$$

and

$$V_{LT} = \frac{R_2}{R_1 + R_2} (-V_{sat})$$

For 741, with supply voltages = ±15 V, the saturation voltage $\pm V_{sat} = \pm 14$ V.

So,

$$0.5 \text{ V} = \frac{R_2}{R_1 + R_2} (14 \text{ V})$$

Or,

$$R_1 = 27\ R_2$$

Choose,

$$R_2 = 1 \text{ kΩ}$$

So,

$$R_1 = 27 \text{ kΩ (take a 50 kΩ pot)}$$

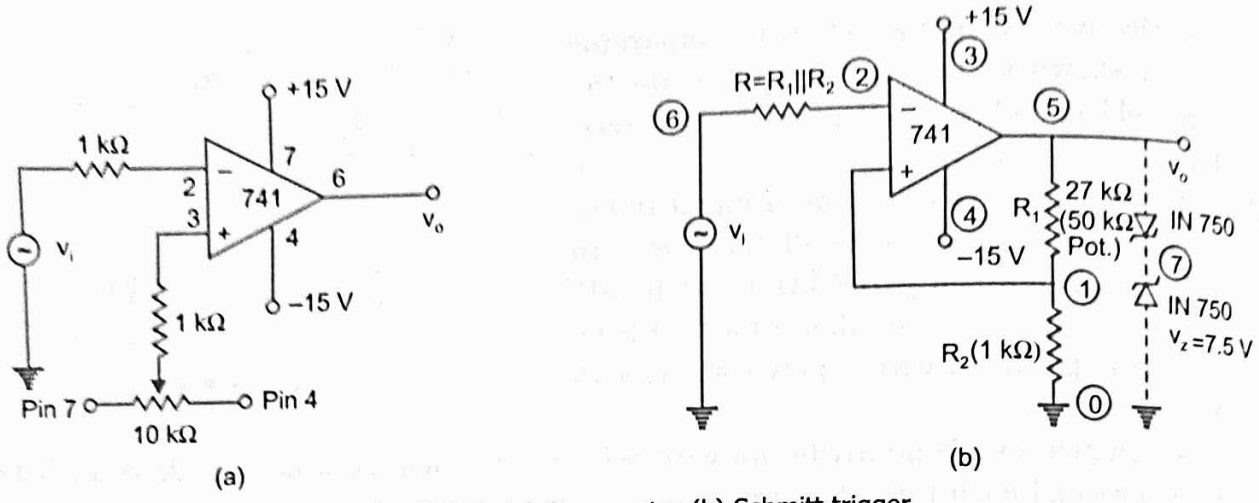


Fig. E. 5.1 (a) Comparator (b) Schmitt trigger

PROCEDURE

1. Connect the circuit of Fig. 5.1 (b) with the values obtained in the design. Please note that Fig. E. 5.1 (b) has been numbered for PSPICE simulation given in Computer program 5.1.
2. Adjust the signal generator so that v_i = 2 V pp sine wave at 1 kHz.
3. Plot the input and output waveforms.
4. Connect two zener diodes (IN 750, V_z = 7.5 V) at the output and find value of R_1 to get the same values of V_{UT} and V_{LT}.

Computer Program 5.1 (Schmitt Trigger)

Figure E. 5.1 (b) has been numbered for PSPICE simulation and its listing is shown below. The input and output waveforms have been shown in Fig. C. 5.1 (a) and (b) for (i) without zener diodes (ii) with zener diodes.

Program 5.1 Listing

```
    *Schmitt Trigger- SINE WAVE INPUT
    R   6  2  1K
    R1  5  1  27K
    R2  1  0  1K
    *Zener Diodes at the output
    *D1  5  7  DIN750
    *D2  0  7  DIN750
*   Op-amp analysis
    X1  1  2  3  4  5  UA741
    .LIB  EVAL.LIB
*   Power supplies
    VCC  3  0  DC  15V
    VEE  0  4  DC  15V
*   Input signal source
    Vi  6  0  SIN (0  2  1KHZ)
*   Output
    .TRAN  .001ms  3ms  1ms  .001ms
    .PROBE
    .END
```

* In order to study the response with zener diodes connected at the output, modify the program listing by removing stars(*) against diodes D_1 and D_2.

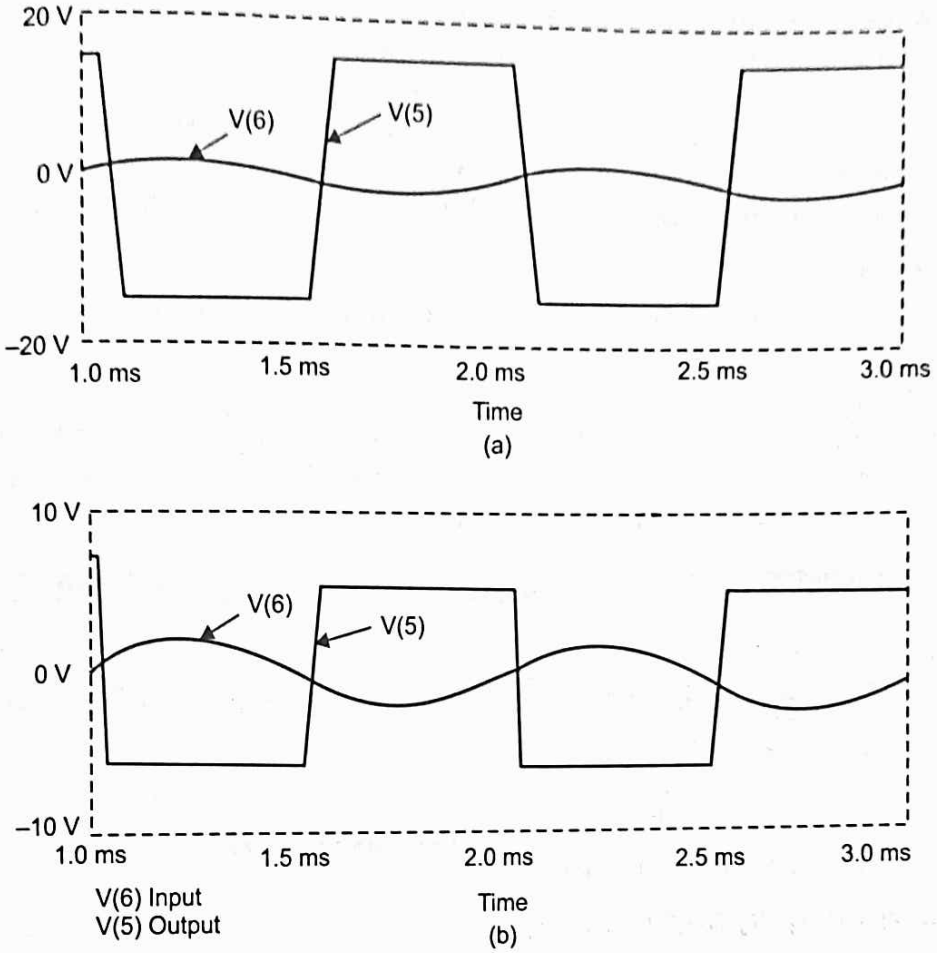


Fig. C. 5.1 Response of Schmitt trigger (a) Without zener diodes (b) With zener diodes

EXPERIMENT 5.2

Design a square wave oscillator for f_o = 1 kHz and study its performance. Use a 741 op-amp and dc supply voltage = ±12 V.

Design

In the circuit shown in Fig. 5.10 (a), use $R_1 = 1.16\ R_2$ so that the frequency of oscillation f_o is given by,

$$f_o = \frac{1}{2RC}$$

Choose $R_2 = 10\ \text{k}\Omega$,

Then $R_1 = (1.16)\ (10\ \text{k}\Omega) = 11.6\ \text{k}\Omega$

Take $$R = \frac{1}{2f_oC} = \frac{1}{2(10^3)(0.05 \times 10^{-6})}$$

$\simeq 10\ \text{k}\Omega$

So, $R_2 = 10\ \text{k}\Omega$; $R_1 = 11.6\ \text{k}\Omega$ (take 20 kΩ potentiometer)

$R = 10\ \text{k}\Omega$ and $C = 0.05\ \mu\text{F}$.

PROCEDURE

1. Make a circuit as shown in Fig. 5.10 (a) with the values of components as obtained in the design.

2. See the output waveform (pin 6) and the capacitor voltage waveform (pin 2) on the oscilloscope and measure amplitude and frequency.
3. Plot these waveforms on a linear graph paper.
4. To get reduced peak amplitude of the square wave, connect two zener diodes ($V_Z \sim 6V$) at the output terminal as shown in Fig. 5.10 (c).
5. See the output waveforms on a scope and plot the waveforms on a graph paper.

Computer Exercise

Verify the output waveforms of the square wave oscillator designed above using PSPICE.

Experiment 5.3

(a) To construct a phase shift oscillator for f_o = 500 Hz and study its operation.
(b) To construct a Wien bridge oscillator for f_o = 1000 Hz and study its operation.

Design equations and component values:

(a) Phase shift oscillator:
In Fig. 5.15,

$$f_o = \frac{1}{2\pi\sqrt{6}\,RC} \text{ and } R_f \geq 29\,R_1$$

Choose $C = 0.1\ \mu F$,

Then $$R = \frac{1}{2\pi(500)(\sqrt{6})(10^{-7})} = 1.3\ k\Omega\ (\text{use } 1.5\ k\Omega)$$

To prevent loading, $R_1 \geq 10\,R$
Therefore, take $R_1 = 10\,R = 15\ k\Omega$
$R_f = 29\ R_1 = 29 \times 15\ k\Omega$
$= 435\ k\Omega$
(Use R_f = 500 kΩ potentiometer)

(b) Wien bridge oscillator:
In Fig. 5.16 (a),

$$f_o = \frac{1}{2\pi RC} \text{ and } R_f = 2R_1$$

Choose $C = 0.05$ mF

So, $$R = \frac{1}{2\pi(1000)(0.05 \times 10^{-6})} = 3.1\ k\Omega$$

Take $R_1 = 10R = 30\ k\Omega$

and $R_f = 2R_1 = 60\ k\Omega$ (Use 100 kΩ pot)

PROCEDURE

1. Set up the Phase shift oscillator of Fig. 5.15 with the values obtained in the design.
2. See the output waveform on an oscilloscope. Adjust R_f to obtain a sine wave output.
3. Measure the frequency of oscillator and voltage amplitude.
4. Repeat steps 1, 2 and 3 for the Wien bridge oscillator.

10

PHASE-LOCKED LOOPS

10.1 INTRODUCTION

The phase-locked loop (PLL) is an important building block of linear systems. Electronic phase-locked loop (PLL) came into vogue in the 1930s when it was used for radar synchronisation and communication applications. The high cost of realizing PLL in discrete form limited its use earlier. Now with the advanced IC technology, PLLs are available as inexpensive monolithic ICs. This technique for electronic frequency control is used today in satellite communication systems, air borne navigational systems, FM communication systems, computers etc. The basic principle of PLL, different ICs and important applications are discussed.

10.2 BASIC PRINCIPLES

The basic block schematic of the PLL is shown in Fig. 10.1. This feedback system consists of:

1. Phase detector/comparator
2. A low pass filter
3. An error amplifier
4. A Voltage Controlled Oscillator (VCO).

The VCO is a free running multivibrator and operates at a set frequency f_o called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage v_c to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a "Voltage Controlled Oscillator" or, in short, VCO.

If an input signal v_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v_o of the VCO. If the two signals differ in frequency and/or phase, an error voltage v_e is generated. The phase detector is basically a multiplier and produces the sum $(f_s + f_o)$ and difference $(f_s - f_o)$ components at its output. The high frequency component $(f_s + f_o)$ is removed by the low pass filter and the difference frequency component is amplified and then applied as control voltage v_c to VCO. The signal v_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_o. Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal

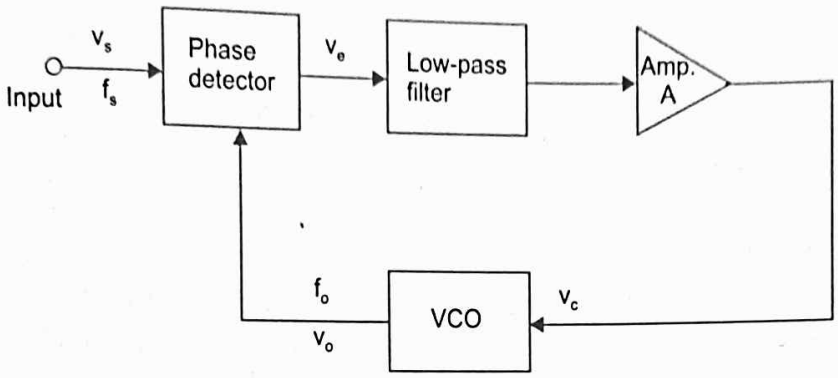


Fig. 10.1 Block schematic of the PLL

frequency. The circuit is then said to be locked. Once locked, the output frequency f_o of VCO is identical to f_s except for a finite phase difference ϕ. This phase difference ϕ generates a corrective control voltage v_c to shift the VCO frequency from f_o to f_s and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

Figure 10.2 shows the capture transient. As capture starts, a small sine wave appears. This is due to the difference frequency between the VCO and the input signal. The dc component of the beat drives the VCO towards the lock. Each successive cycle causes the VCO frequency to move closer to the input signal frequency. The difference in frequency becomes smaller and a large dc component is passed by the filter, shifting the VCO frequency further. The process continues until the VCO locks on to the signal and the difference frequency is dc.

The low pass filter controls the capture range. If VCO frequency is far away, the beat frequency will be too high to pass through the filter and the PLL will not respond. We say that the signal is out of the capture band. However, once locked, the filter no longer restricts the PLL. The VCO can track the signal well beyond the capture band. Thus tracking range is always larger than the capture range.

Some of the important definitions in relation to PLL are:

Lock-in Range: Once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. The lock range is usually expressed as a percentage of f_o, the VCO frequency.

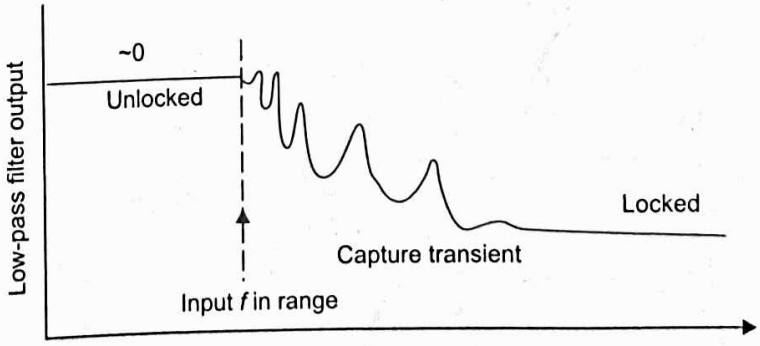


Fig. 10.2 The capture transient

Capture Range: The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_o.

Pull-in time: The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

10.3 PHASE DETECTOR/COMPARATOR

The phase detection is the most important part of the PLL system. There are two types of phase detectors used, analog and digital.

10.3.1 Analog Phase Detector

The principle of analog phase detection using switch type phase detector is shown in Fig. 10.3(a). An electronic switch S is opened and closed by signal coming from VCO (normally a square wave) as shown in Fig. 10.3 (b). The input signal is, therefore, chopped at a repetition rate determined by VCO frequency. Figure 10.3 (c) shows the input signal v_s assumed to be in phase ($\phi = 0°$) with

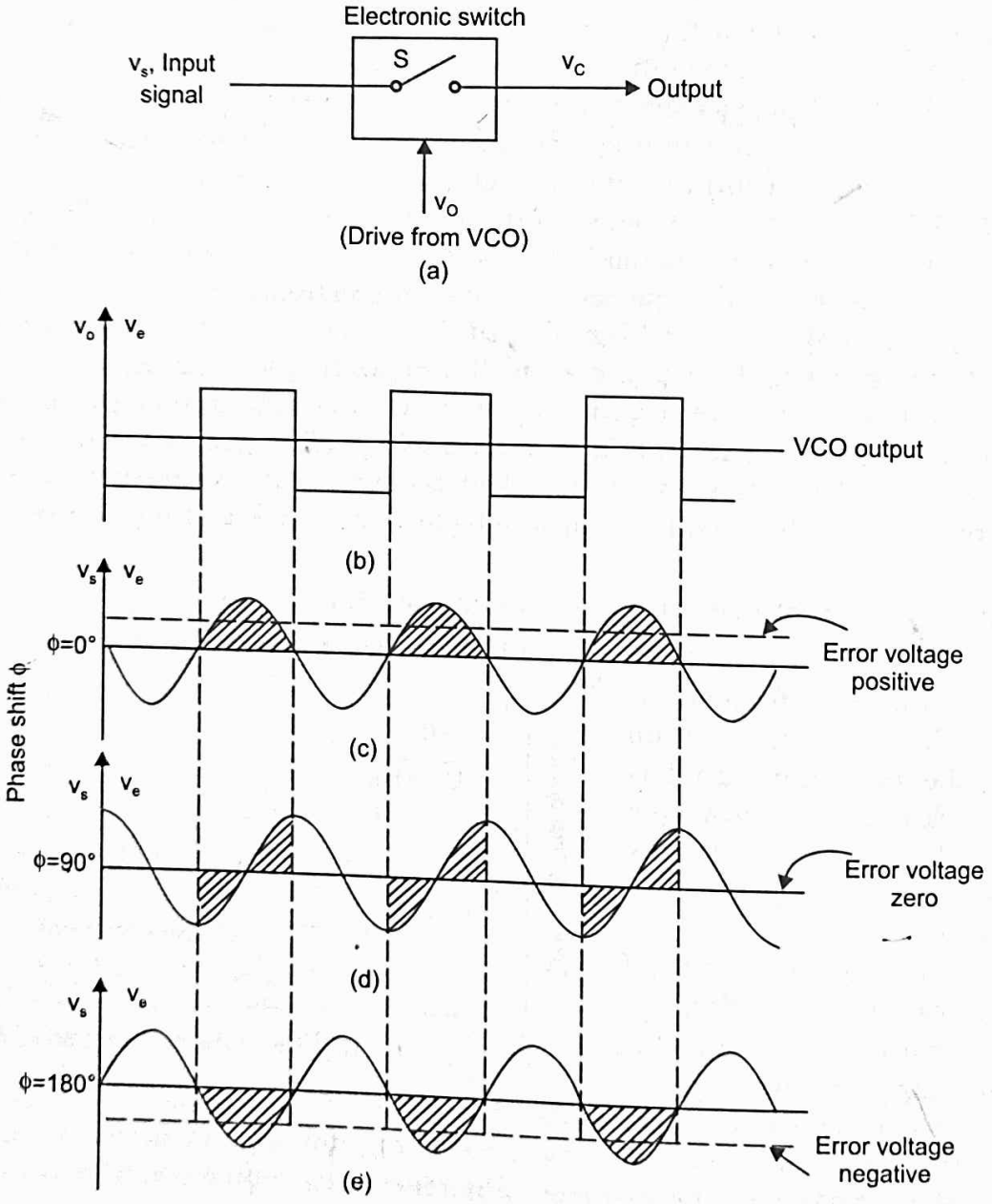


Fig. 10.3 Phase detector for PLL (a) Basic scheme (b) VCO output waveform. Input and output waveform (hatched) of phase detector for (c) $\phi = 0$ (d) $\phi = 90°$ (e) $\phi = 180°$

VCO output v_o. Since the switch S is closed only when VCO output is positive, the output waveform v_e will be half sinusoids (shown hatched). Similarly, the output waveform for $\phi = 90°$ and $\phi = 180°$ is shown in Fig. 10.3 (d, e). This type of phase detector is called a half wave detector, since the phase information for only one-half of the input waveform is detected and averaged. The output of the phase comparator when filtered through a low pass filter gives an error signal which is the average value of the output waveform shown by dotted line in Fig. 10.3 (c, d, e).

It may be seen that the error voltage is zero when the phase shift between the two inputs is 90°. So, for perfect lock, the VCO output should be 90° out of phase with respect to the input signal.

Analysis

A phase comparator is basically a multiplier which multiplies the input signal ($v_s = V_s \sin 2\pi f_s t$) by the VCO signal ($v_o = V_o \sin (2\pi f_o t + \phi)$). Thus the phase comparator output is,

$$v_e = KV_sV_o \sin (2\pi f_s t) \sin (2\pi f_o t + \phi) \tag{10.1}$$

where K is the phase comparator gain (or attenuation constant) and ϕ is the phase shift between the input signal and the VCO output. Equation 10.1 can be simplified as,

$$v_e = \frac{KV_sV_o}{2}\left[\cos(2\pi f_s t - 2\pi f_o t - \phi) - \cos(2\pi f_s t + 2\pi f_o t + \phi)\right] \tag{10.2}$$

when at lock, that is, $f_s = f_o$,

$$\text{Then } v_e = \frac{KV_sV_o}{2}\left[\cos(-\phi) - \cos(2\pi \times 2f_o t + \phi)\right] \tag{10.3}$$

This shows that the phase comparator output contains a double frequency term and a dc term $(KV_s V_o/2) \cos \phi$ which varies as a function of phase ϕ, that is, cos ϕ between the two signals. The double frequency term is eliminated by the low pass filter and the dc signal is applied to the modulating input terminal of a VCO. It can be seen that in the perfect locked state ($f_s = f_o$), the phase shift should be 90° (cos 90° = 0), in order to get zero error signal, that is, $v_e = 0$.

There are two problems associated with the switch type phase detector:

1. The output voltage v_e is proportional to the input signal amplitude V_s. This is undesirable since it makes phase detector gain and the loop gain dependent on the input signal amplitude.
2. The output is proportional to cos ϕ and not proportional to ϕ making it non-linear.

Both these problems can be eliminated by limiting the amplitude of the input signal, that is, converting the input to a constant amplitude square wave. A circuit which performs phase comparison with square wave input is shown in Fig. 10.4 (a). This is a balanced modulator used as full-wave switching phase detector. Here the input signal is applied to the differential pair Q_1Q_2. Transistors Q_3–Q_4 and Q_5–Q_6 are two sets of SPDT switches activated by the VCO output. The input signal v_s and the VCO output v_o are assumed to be high enough to switch the transistors in Fig. 10.4 (a) fully ***on*** or ***off***. In Fig. 10.4 (b) when v_s and v_o both are high during the time 0 to (π–ϕ), transistors Q_1 and Q_3 are driven ***on*** and current I_E flows through Q_1 and Q_3. This gives an output voltage

$$v_e = -I_E R_L \tag{10.4}$$

Next for the period $(\pi - \theta)$ for π, when v_s is high and v_o is low, transistors Q_1 and Q_4 are driven ***on*** resulting in an output voltage

$$v_e = I_E R_L \tag{10.5}$$

In this way, the output voltage waveform v_e in Fig. 10.4 (b) is obtained.

The average value of the phase detector output v_e can be calculated as,

$$(v_e)_{av} = \frac{1}{\pi}[(\text{area } A_1) + (\text{area } A_2)]$$

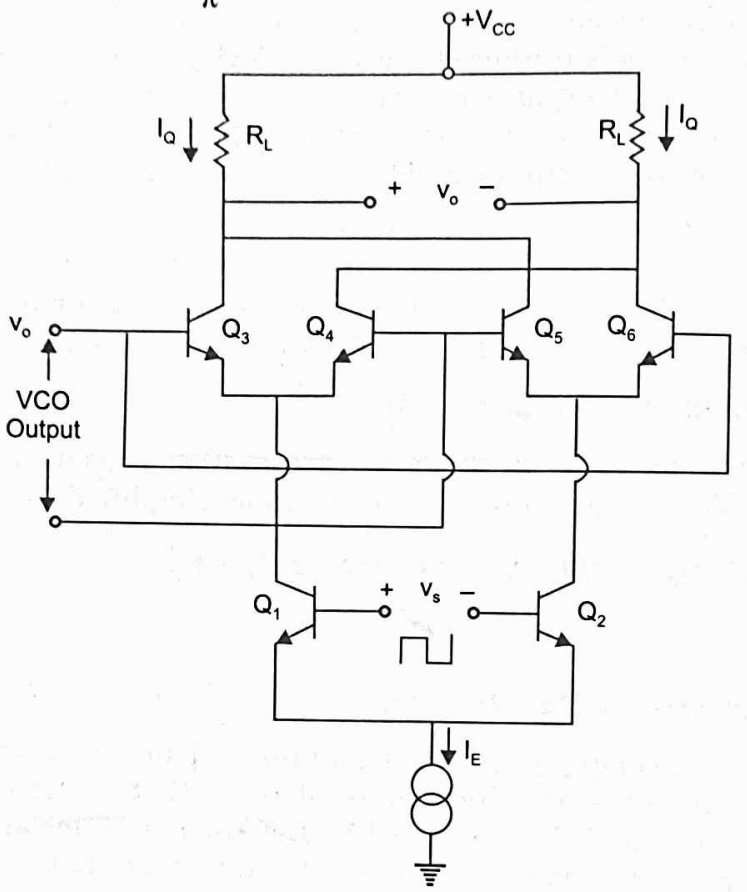


Fig. 10.4 (a) Phase detector for IC PLL

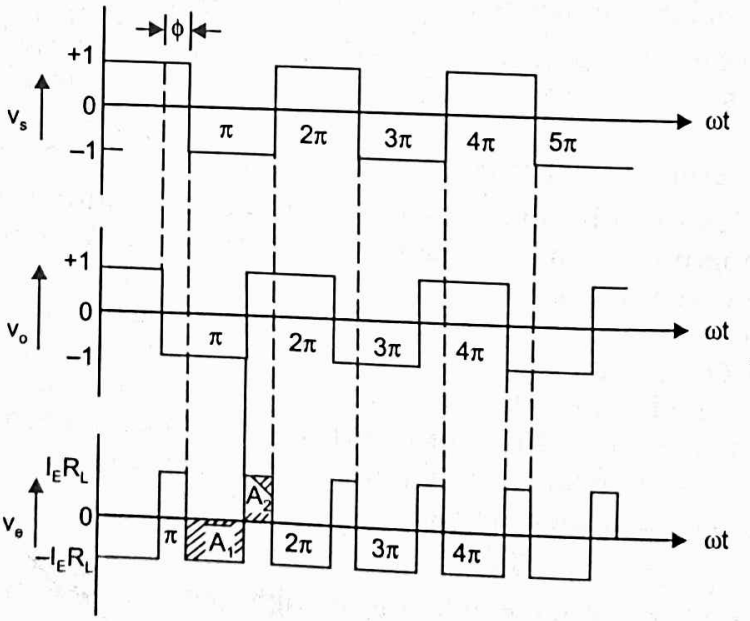


Fig. 10.4 (b) Timing diagram of input and output waveforms for balanced modulator circuit of Fig. 10.4 (a)

$$= \frac{1}{\pi}\left[I_E R_L \phi + (-I_E R_L) \times (\pi - \phi)\right] = I_E R_L \left(\frac{2\phi}{\pi} - 1\right)$$

$$= 4\frac{I_Q R_L}{\pi}\left(\phi - \frac{\pi}{2}\right) \qquad [\text{Since } I_E = 2I_Q]$$

$$= K_\phi(\phi - \pi/2) \tag{10.6}$$

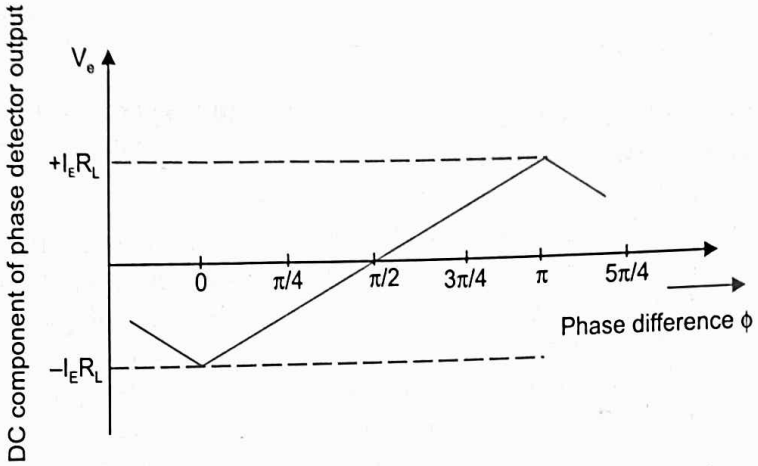


Fig. 10.4 (c) Output dc voltage versus input phase difference of balanced modulator full wave switching phase detector

where K_ϕ is the phase angle-to-voltage transfer coefficient or, the **conversion ratio of the phase detector**. This linear relationship between v_e and ϕ is depicted in Fig. 10.4 (c).

10.3.2 Digital Phase Detector

Figure 10.5 (a) shows the digital type XOR (Exclusive–OR) phase detector. It uses CMOS type 4070 Quad 2-input XOR gate. The output of the XOR gate is high when only one of the inputs signals f_s or f_o is high. This type of detector is used when both the input signals are square waves. The input and output waveforms for $f_s = f_o$ are shown in Fig. 10.5 (b). In this figure, f_s is leading f_o by ϕ degrees. The variation of dc output voltage with phase difference

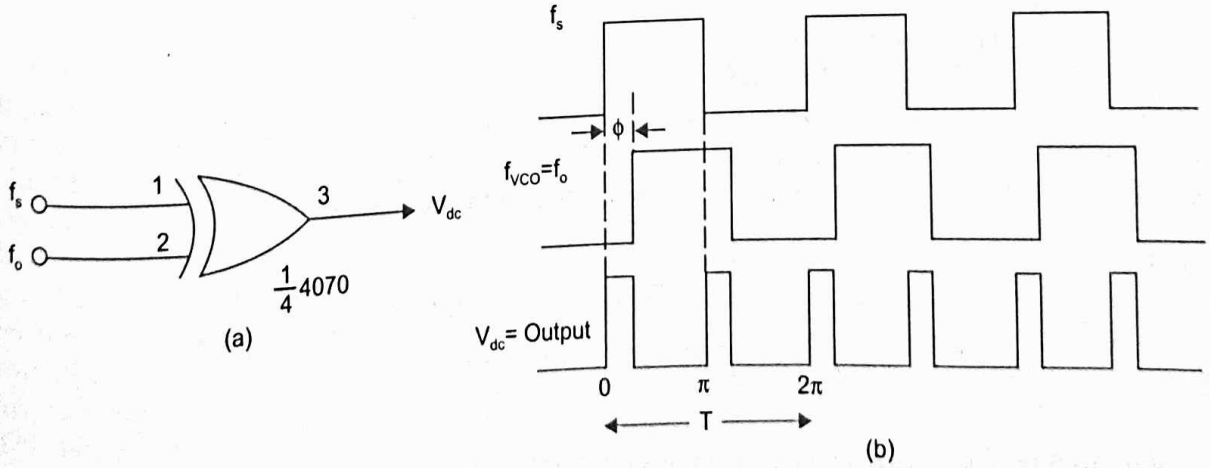


Fig. 10.5 (a) Exclusive-OR phase detector, (b) Input and output waveforms

ϕ is shown in Fig. 10.5 (c). It can be seen that the maximum dc output voltage occurs when the phase difference is π because the output of the gate remains high throughout. The slope of the curve gives the conversion ratio k_ϕ of the phase detector. So, the conversion ratio K_ϕ for a supply voltage $V_{CC} = 5$ V is,

$$K_\phi = \frac{5}{\pi} = 1.59 \text{ V/rad} \qquad (10.7)$$

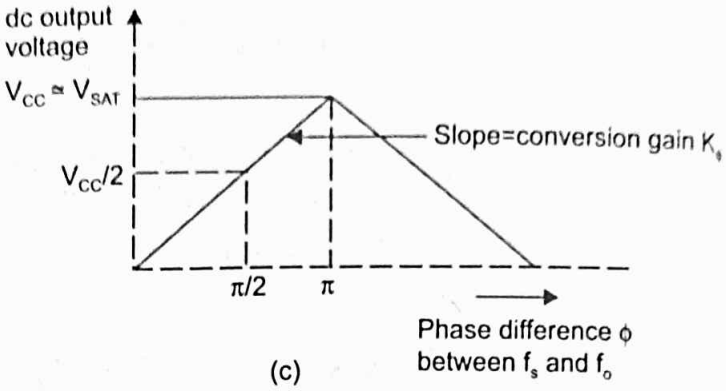


Fig. 10.5 (c) DC output voltage versus phase difference ϕ curve

Another type of digital phase detector is an ***edge-triggered phase detector*** as shown in Fig. 10.6 (a). The circuit is an R-S flip-flop made by NOR gates, such as CD 4001. This circuit is useful when f_s (incoming signal) and f_o (VCO output) are both pulse waveforms with duty cycle less than 50 per cent. The output of the R-S flip-flop changes its state on the leading edge of f_s and f_o as shown in Fig. 10.6 (b). The variation of dc output voltage vs phase difference between f_s and f_o is shown in Fig. 10.6 (c). This type of detector has better capture tracking and locking characteristics as the dc output voltage is linear upto 360° compared to 180° in the case of Exclusive-OR detector.

Digital phase detector is also available in independent monolithic IC form. A typical example is MC4344/4044. This IC gives input/output transfer characteristics which is linear upto 4π radians or 720°.

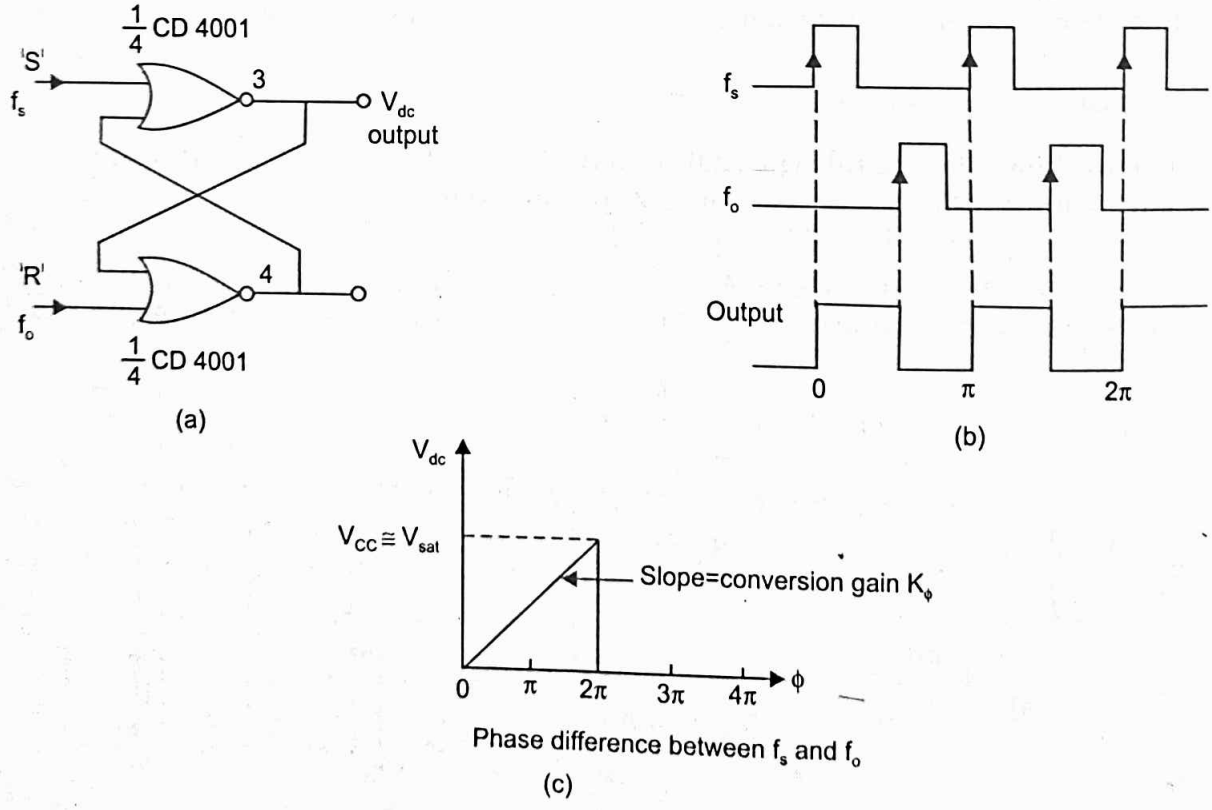


Fig. 10.6 (a) Edge-triggered phase detector using CD4001, Quad 2-input NOR gate, (b) Input and output waveforms, (c) dc output voltage vs phase difference ϕ

10.4 VOLTAGE CONTROLLED OSCILLATOR (VCO)

A common type of VCO available in IC form is Signetics NE/SE566. The pin configuration and basic block diagram of 566 VCO are shown in Fig. 10.7 (a, b). Referring to Fig. 10.7 (b), a timing capacitor C_T is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage v_c applied at the modulating input (pin 5) or by changing the timing resistor R_T external to IC chip. The voltage at pin 6 is held at the same voltage as pin 5. Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current.

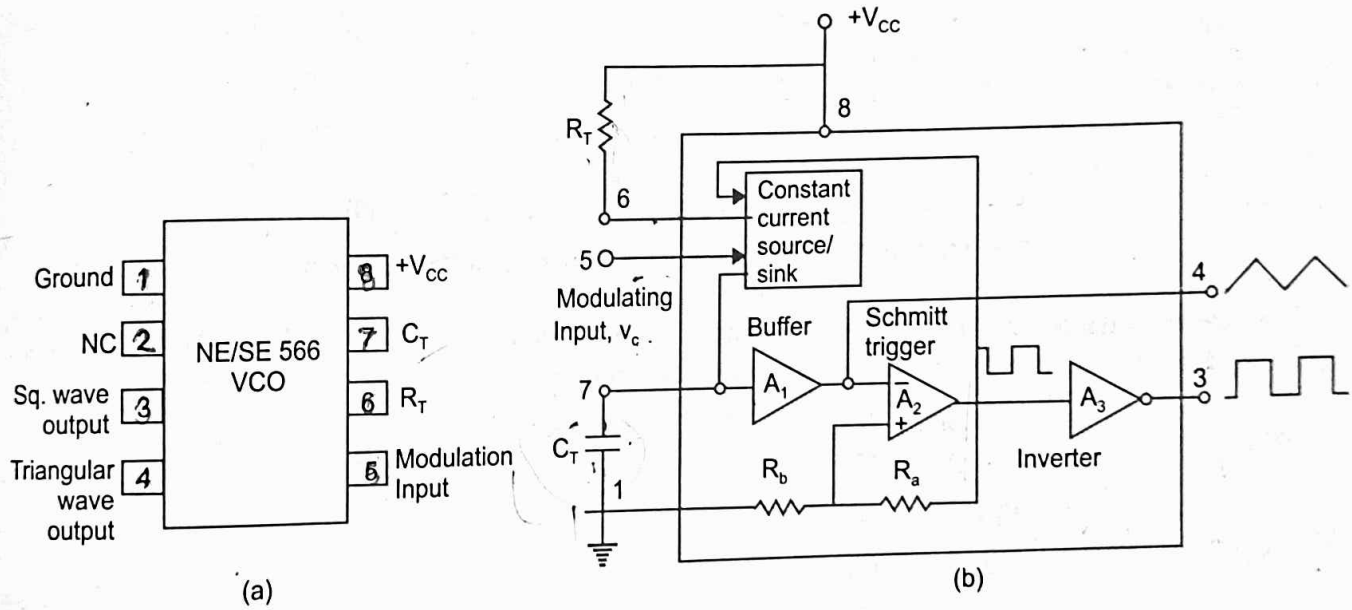


Fig. 10.7 Voltage controlled oscillator (a) Pin configuration, (b) Block diagram

A small capacitor of .001 μF should be connected between pin 5 and 6 to eliminate possible oscillations. A VCO is commonly used in converting low frequency signals such as EEGs, EKG into an audio frequency range. These audio signals can be transmitted over telephone lines or a two way radio communication systems for diagnostic purposes or can be recorded on a magnetic tape for further reference.

The voltage across the capacitor C_T is applied to the inverting input terminal of Schmitt trigger A_2 via buffer amplifier A_1. The output voltage swing of the Schmitt trigger is designed to V_{CC} and 0.5 V_{CC}. If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting input terminal of A_2 swings from 0.5 V_{CC} to 0.25 V_{CC}. In Fig. 10.7 (c), when the voltage on the capacitor C_T exceeds 0.5 V_{CC} during charging, the output of the Schmitt trigger goes LOW (0.5 V_{CC}). The capacitor now discharges and when it is at 0.25 V_{CC}, the output of Schmitt trigger goes HIGH (V_{CC}). Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across C_T which is also available at pin 4. The square wave output of the Schmitt trigger is inverted* by inverter A_3 and is available at pin 3. The inverter A_3 is basically a current amplifier used to drive the load. The output waveforms are shown in Fig. 10.7 (c).

The output frequency of the VCO can be calculated as follows:

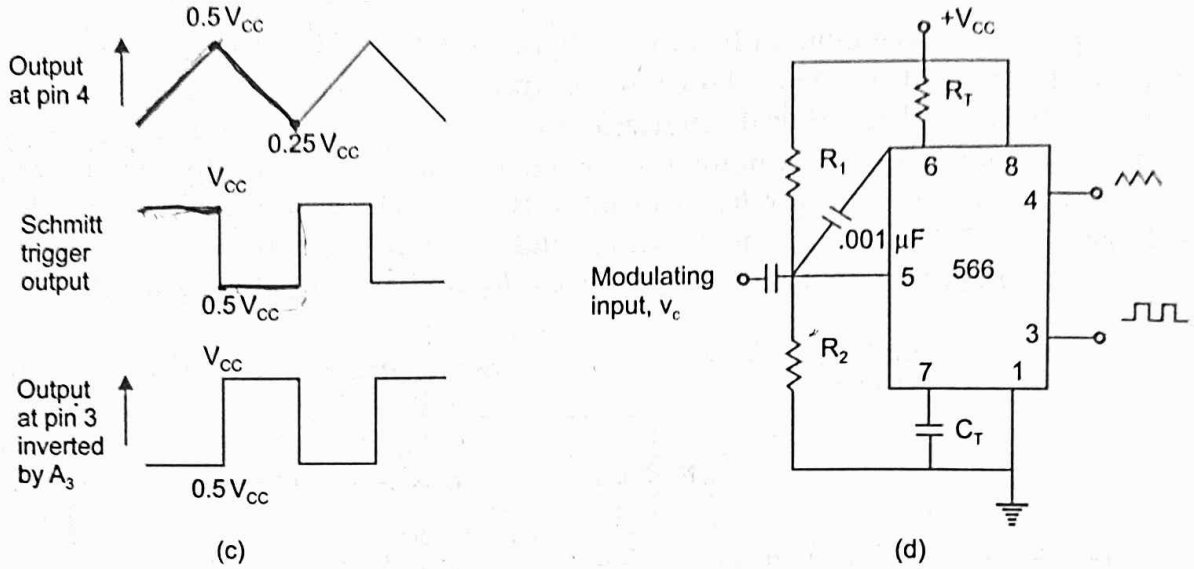


Fig. 10.7 (c) Output waveform, (d) Typical connection diagram

The total voltage on the capacitor changes from 0.25 V_{CC} to 0.5 V_{CC}. Thus $\Delta v = 0.25\ V_{CC}$. The capacitor chargers with a constant current source.

So
$$\frac{\Delta v}{\Delta t} = \frac{i}{C_T}$$

or,
$$\frac{0.25\ V_{CC}}{\Delta t} = \frac{i}{C_T}$$

or,
$$\Delta t = \frac{0.25\ V_{CC} C_T}{i} \tag{10.8}$$

The time period T of the triangular waveform = $2\Delta t$. The frequency of oscillator f_0 is,

$$f_0 = \frac{1}{T} = \frac{1}{2\,\Delta t} = \frac{i}{0.5\ V_{CC} C_T}$$

But,
$$i = \frac{V_{CC} - v_c}{R_T} \tag{10.9}$$

where, v_c is the voltage at pin 5. Therefore,

$$f_0 = \frac{2(V_{CC} - v_c)}{C_T R_T V_{CC}} \tag{10.10}$$

The output frequency of the VCO can be changed either by (i) R_T, (ii) C_T or (iii) the voltage v_c at the modulating input terminal pin 5. The voltage v_c can be varied by connecting a R_1R_2 circuit as shown in Fig. 10.7 (d). The components R_T and C_T are first selected so that VCO output frequency lies in the centre of the operating frequency range. Now the modulating input voltage is usually varied from 0.75 V_{CC} to V_{CC} which can produce a frequency variation of about 10 to 1. With no modulating input signal, if the voltage at pin 5 is biased† at (7/8) V_{CC}, Eq. (10.10) gives the VCO output frequency as,

† The expression of f_0 depends upon the initial choice of the voltage v_c. If the value of v_c is taken as 0.85 V_{CC} then f_0 comes out to be $0.3/R_TC_T$.

$$f_o = \frac{2(V_{CC} - (7/8)V_{CC})}{C_T R_T V_{CC}} = \frac{1}{4R_T C_T} = \frac{0.25}{R_T C_T} \tag{10.11}$$

Voltage to Frequency Conversion Factor

A parameter of importance for VCO is voltage to frequency conversion factor K_v and is defined as

$$K_v = \frac{\Delta f_o}{\Delta v_c}$$

Here Δv_c is the modulation voltage required to produce the frequency shift Δf_o for a VCO. If we assume that the original frequency is f_o and the new frequency is f_1, then

$$\Delta f_o = f_1 - f_o = \frac{2(V_{CC} - v_c + \Delta v_c)}{C_T R_T V_{CC}} - \frac{2(V_{CC} - v_c)}{C_T R_T V_{CC}} = \frac{2\Delta v_c}{C_T R_T V_{CC}} \tag{10.12}$$

or,
$$\Delta v_c = \frac{\Delta f_o \, C_T R_T V_{CC}}{2} \tag{10.13}$$

Putting the value of $C_T R_T$ from Eq. (10.11)

$$\Delta v_c = \Delta f_o \, V_{CC}/8f_o \tag{10.14}$$

or,
$$K_v = \frac{\Delta f_o}{\Delta v_c} = \frac{8 f_o}{V_{CC}} \tag{10.15}$$

Example 10.1

In a VCO, if input signal frequency f_s = 20 kHz, free running, frequency f_o = 21 kHz/V, voltage to frequency conversion factor K_V is 4 kHz/V, find the change in the dc control voltage V_c during lock.

Solution

The voltage to frequency conversion factor

$$K_v = \frac{\Delta f_o}{\Delta V_C}$$

So,
$$\Delta V_C = \frac{\Delta f_o}{K_v}$$

Frequency shift
$$\Delta f_o = 21 \text{ kHz} - 20 \text{ kHz}$$
$$= 1 \text{ kHz}$$

Therefore
$$\Delta V = \frac{1 \times 10^3}{4 \times 10^3} V$$
$$= 0.25 \text{ V}$$

10.5 LOW PASS FILTER

The filter used in a PLL may be either passive type as shown in Fig. 10.8 (a, b) or active type as in Fig. 10.8 (c).

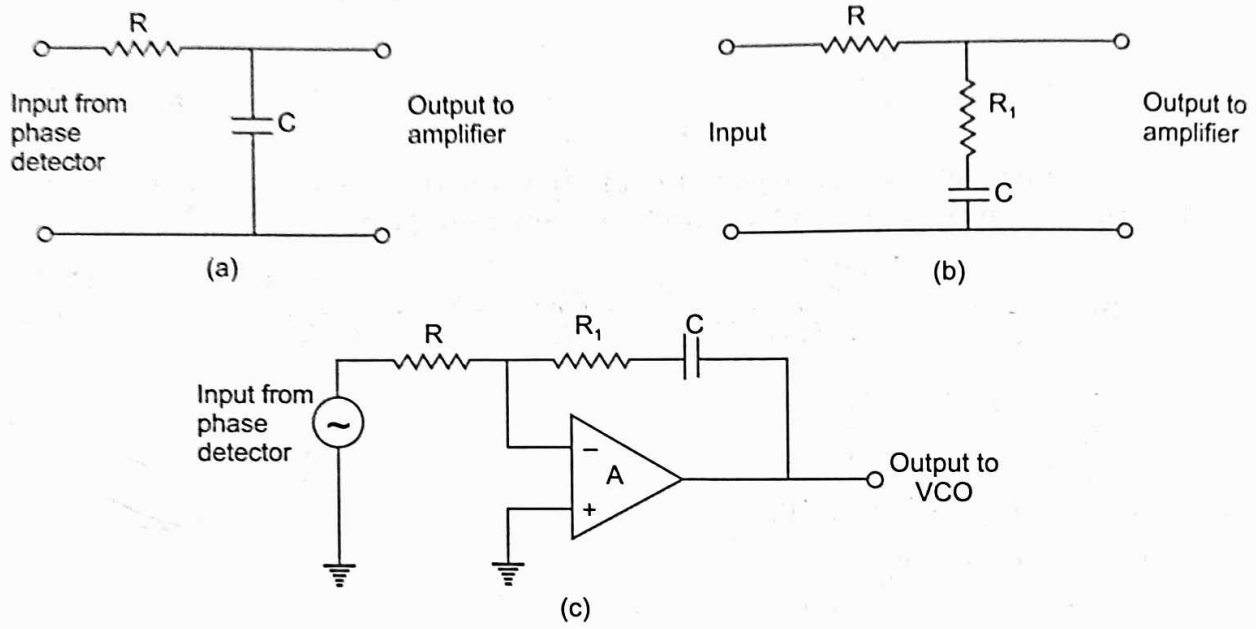


Fig. 10.8 (a) Low pass filter, (b) Passive filter, (c) Active filter

The low pass filter not only removes the high frequency components and noise, but also controls the dynamic characteristics of the PLL. These characteristics include capture and lock range, band-width and transient response. If filter band-width is reduced, the response time increases. However, reducing the band-width of the filter also reduces the capture range of the PLL. The filter serves one more important purpose. The charge on the filter capacitor gives a short time 'memory' to the PLL. Thus, even if the signal becomes less than the noise for a few cycles, the dc voltage on the capacitor continues to shift the frequency of the VCO till it picks up signal again. This produces a high noise immunity and locking stability.

Example 10.2

The free running frequency of a PLL is 300 kHz and the bandwidth of the low pass filter is 10 kHz. Will the PLL acquire lock for an input signal of 320 kHz. Also what happens if the cut-off frequency of the LPF is 25 kHz.

Solution

The phase detector outputs will be

$$f_s + f_o = 320 \text{ kHz} + 300 \text{ kHz}$$
$$= 620 \text{ kHz}$$

and $$f_s - f_o = 320 \text{ kHz} - 300 \text{ kHz}$$
$$= 20 \text{ kHz}$$

If the bandwidth of the LPF is 10 kHz, then PLL will not lock. However, for 25 kHz BW, PLL will lock.

10.6 MONOLITHIC PHASE-LOCKED LOOP

All the different building blocks of PLL are available as independent IC packages and can be externally interconnected to make a PLL. However, a number of manufacturers have introduced monolithic PLLs too. Some of the important monolithic PLLs are SE/NE560 series introduced by Signetics and LM560 series by National Semiconductor. The SE/NE 560, 561, 562, 564, 565 and 567 mainly differ in operating frequency range, power supply requirement, frequency and bandwidth adjustment ranges. Since 565 is the most commonly used PLL, we will discuss some of the important features of this IC chip.

IC PLL 565

565 is available as a 14-pin DIP package and as 10-pin metal can package. The pin configuration and the block diagram are shown in Fig. 10.9 (a, b). The output frequency of the VCO (both inputs 2, 3 grounded) as given by Eq. (10.11) can be rewritten as,

$$f_o = \frac{0.25}{R_T C_T} \text{ Hz} \qquad (10.16)$$

where R_T and C_T are the external resistor and capacitor connected to pin 8 and pin 9. A value between 2 kΩ and 20 kΩ is recommended for R_T. The VCO free running frequency is adjusted with R_T and C_T to be at the centre of the input frequency range. It may be seen that phase locked loop is internally broken between the VCO output and the phase comparator input. A short circuit between pins 4 and 5 connects the VCO output to the phase comparator so as to compare f_o with input signal f_s. A capacitor C is connected between pin 7 and pin 10 (supply terminal) to make a low pass filter with the internal resistance of 3.6 kΩ.

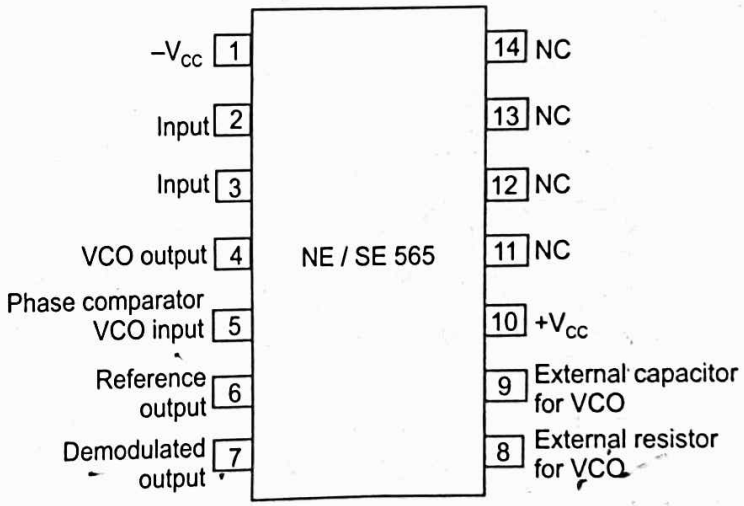


Fig. 10.9 (a) Pin diagram

Chapter 10

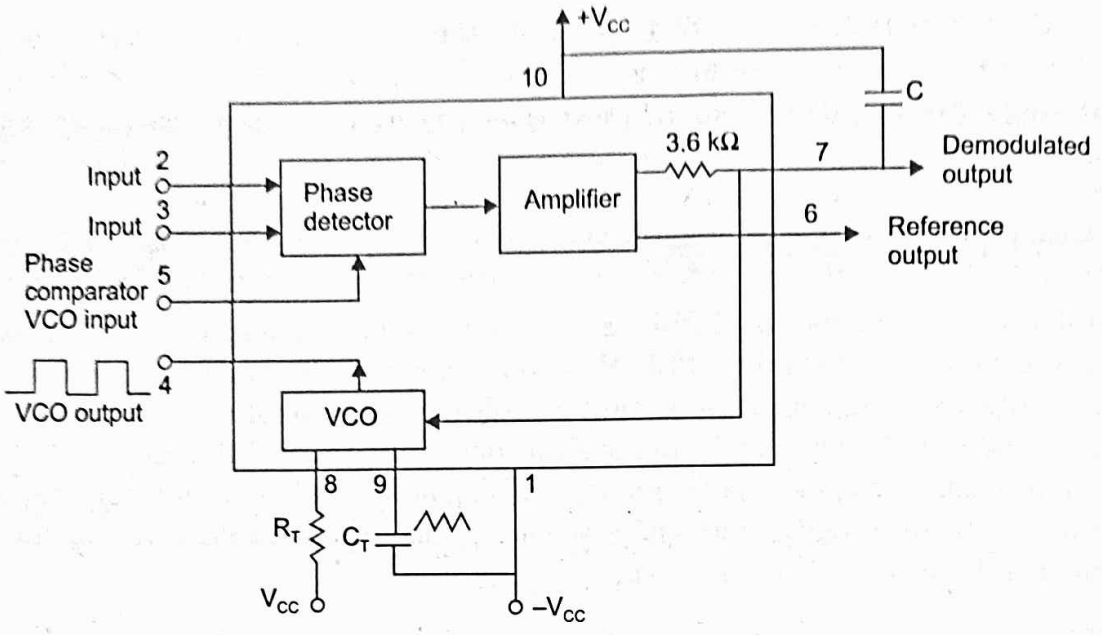


Fig. 10.9 (b) NE/SE565 PLL block diagram

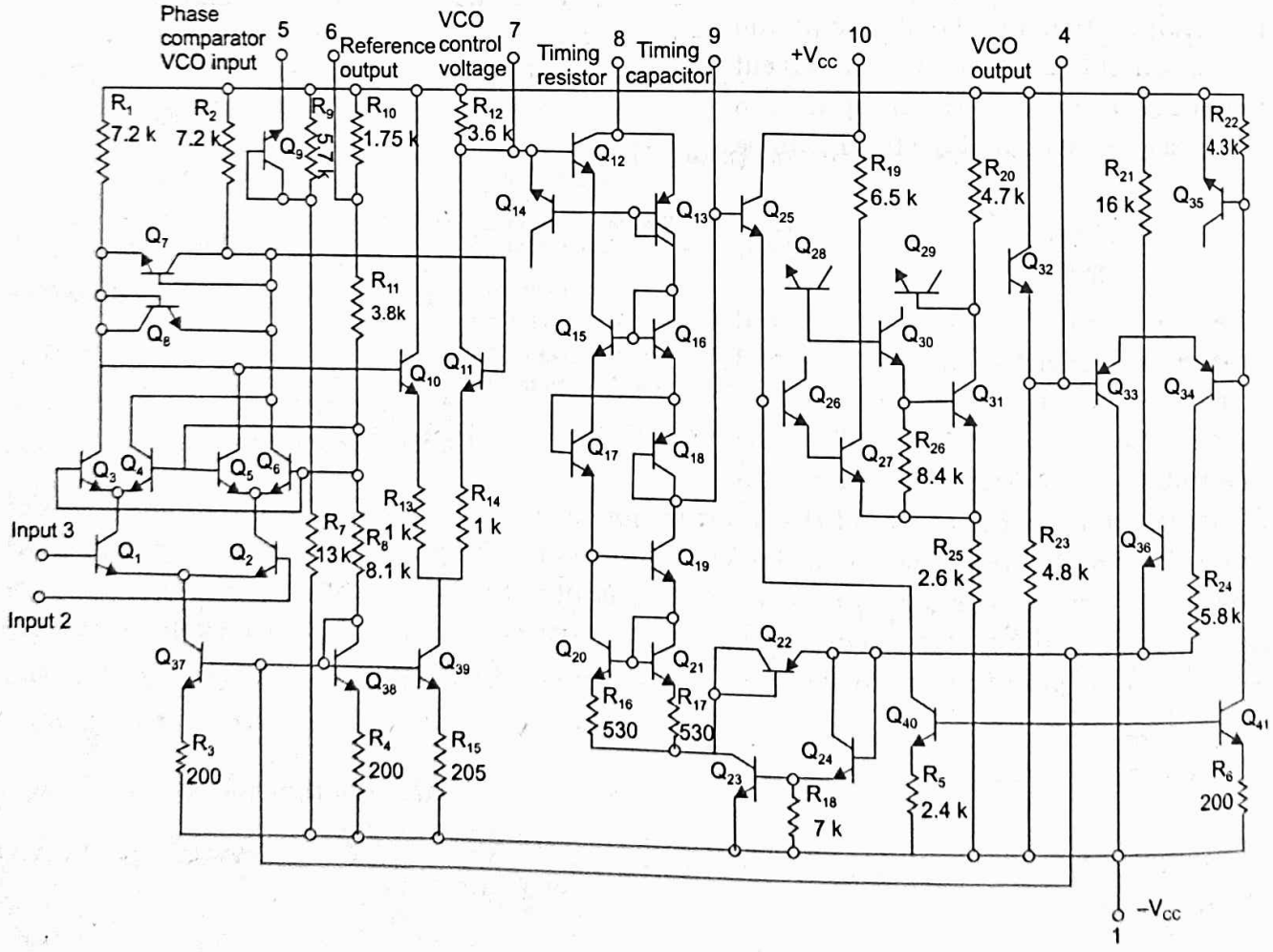


Fig. 10.10 Circuit diagram of LM565 PLL

In Fig. 10.10, a complete diagram of LM565 (National Semiconductor) IC PLL is presented. The analog phase detector is comprised of the Q_1–Q_2, Q_3–Q_4 and Q_5–Q_6 differential amplifier pairs with Q_{37} together with R_3 (200 Ω) serving as a current sink bias source. Resistors R_1 and R_2 (each 7.2 kΩ) serve as the load for the phase detector. The output voltage of the phase detector is limited by the diode-connected transistors Q_7 and Q_8 to a maximum of ±0.7 V which minimizes the effect of high amplitude noise pulses and other transient effect on the operation of the PLL. This makes the conversion ratio of the phase detector of 565 PLL as,

$$K_\phi = \frac{0.7-(-0.7)}{\pi} = \frac{1.4}{\pi} \tag{10.17}$$

A balanced output is taken from the phase detector and supplied to the Q_{10}–Q_{11} differential pair which is biased by the Q_{39} current sink. Q_{10}–Q_{11} serves as the amplifier stage (which is designed for a gain of 1.4) after phase detector. A single ended output is taken from this stage across the resistors R_{12} (3.6 kΩ). Resistor R_{12} also serves as part of the LPF when an external capacitor between pin 7 and ground of is connected.

The VCO consists of a voltage controlled current source (Q_{12} through Q_{23}). Equal charging and discharging currents are supplied to external capacitor C_T connected at pin 9. Resistor R_T is connected between pin 8 and positive supply $+V_{CC}$. The Schmitt trigger (Q_{25} through Q_{36}) with the differential amplifier output circuit (Q_{33} and Q_{34}) is part of VCO. This controls the turn-on and turn-off of Q_{23} and Q_{24} for the switching action of the current source for the charging and discharging cycles. Transistor Q_{14}, Q_{26}, Q_{30}, Q_{35} are used as diodes to obtain the desired level shift.

The important electrical parameters of 565 PLL are:

Operating frequency range	:	0.001 Hz to 500 kHz
Operating voltage range	:	±6 V to ±12 V
Input level	:	10 mV rms min. to 3 V pp max
Input impedance	:	10 kΩ typical
Output sink current	:	1 mA typical
Drift in VCO centre frequency with temperature	:	300 ppm/°C. (parts per million per degree centigrade)
Drift in VCO centre frequency with supply voltage	:	1.5 per cent/V max
Triangle wave amplitude	:	2.4 V_{pp} at ±6 V supply voltage
Square wave amplitude	:	5.4 V_{pp} at ±6 V supply voltage
Bandwidth adjustment range	:	< ±1 to ±60%

Derivation of Lock-in Range

If ϕ radians is the phase difference between the signal and the VCO voltage, then the output voltage of the analog phase detector is given by,

$$v_e = K_\phi(\phi - \pi/2) \tag{10.18}$$

where K_ϕ is the phase angle-to-voltage transfer coefficient of the phase detector. The control voltage to VCO is,

$$v_c = AK_\phi(\phi - \pi/2) \tag{10.19}$$

where A is the voltage gain of the amplifier. This v_c shifts VCO frequency from its free running frequency f_o to a frequency f given by,

$$f = f_o + K_v v_c \tag{10.20}$$

where K_v is the voltage to frequency transfer coefficient of the VCO. When PLL is locked-in to signal frequency f_s, then we have

$$f = f_s = f_o + K_v v_c \tag{10.21}$$

since, $$v_c = (f_s - f_o)/K_v = A K_\phi (\phi - \pi/2) \tag{10.22}$$

Thus, $$\phi = \pi/2 + (f_s - f_o)/K_v K_\phi A \tag{10.23}$$

The maximum output voltage magnitude available from the phase detector occurs for $\phi = \pi$ and 0 radian (see in Fig. 10.4 (c) and $v_{e(max)} = \pm K_\phi \pi/2$ from Eq. 10.6. The corresponding value of the maximum control voltage available to drive the VCO will be,

$$v_{c(max)} = \pm (\pi/2) K_\phi A \tag{10.24}$$

The maximum VCO frequency swing that can be obtained is given by,

$$(f - f_o)_{max} = K_v v_{c(max)} = K_v K_\phi A (\pi/2) \tag{10.25}$$

Therefore, the maximum range of signal frequencies over which the PLL can remain locked will be,

$$f_s = f_o \pm (f - f_o)_{max} = f_o \pm K_v K_\phi (\pi/2) A = f_o \pm \Delta f_L \tag{10.26}$$

where $2 \Delta f_L$ will be the lock-in frequency range and is given by,

lock-in range = $$2 \Delta f_L = K_v K_\phi A \pi \tag{10.27}$$

or, $$\Delta f_L = \pm K_v K_\phi A (\pi/2) \tag{10.28}$$

The lock-in range is symmetrically located with respect to VCO free running frequency f_o. For IC PLL 565,

$$K_v = \frac{8 f_o}{V} \quad \text{(from Eq. 10.15)}$$

where $$V = +V_{CC} - (-V_{CC})$$

Again, $$K_\phi = \frac{1.4}{\pi} \quad \text{(from Eq. 10.17)}$$

and $$A = 1.4$$

Hence the lock-in range from Eq. 10.28 becomes,

$$\Delta f_L = \pm 7.8 f_o/V \tag{10.29}$$

Derivation of Capture Range

Initially, when PLL is not locked to the signal, the frequency of the VCO will be free running frequency f_o. The phase angle difference between the signal and the VCO output voltage will be,

$$\phi = (\omega_s t + \theta_s) - (\omega_o t + \theta_o) = (\omega_s - \omega_o) t + \Delta\theta \tag{10.30}$$

thus the phase angle difference does not remain constant but will change with time at a rate given by

$$\frac{d\phi}{dt} = \omega_s - \omega_o \tag{10.31}$$

The phase detector output voltage will therefore not have a dc component but will produce an ac voltage with a triangular waveform of peak amplitude $K_\phi(\pi/2)$ and a fundamental frequency $(f_s - f_o) = \Delta_f$.

The low pass filter (LPF) is a simple RC network having transfer function

$$T(jf) = \frac{1}{1 + j(f/f_1)} \tag{10.32}$$

where $f_1 = 1/2\ \pi\ RC$ is the 3-dB point of LPF. In the slope portion of LPF where $(f/f_1)^2 >> 1$, then

$$T(f) \simeq \frac{f_1}{jf} \tag{10.33}$$

The fundamental frequency term supplied to the LPF by the phase detector will be the difference frequency $\Delta f = f_s - f_o$. If $\Delta f > 3f_1$, the LPF transfer function will be approximately,

$$T(\Delta f) \simeq f_1/\Delta f = f_1/(f_s - f_o) \tag{10.34}$$

The voltage v_c to drive the VCO is,

$$v_c = v_e \times T(f) \times A \tag{10.35}$$

or,
$$v_{c(max)} = v_{e(max)} \times T(f) \times A$$
$$= \pm K_\phi\,(\pi/2)A\,(f_1/\Delta f).\ \text{(from Eq. (10.24))} \tag{10.36}$$

Then the corresponding value of the maximum VCO frequency shift is,

$$(f - f_o)_{max} = K_v\, v_{c(max)} = \pm K_v K_\phi\,(\pi/2)A\,(f_1/\Delta f) \tag{10.37}$$

For the acquisition of signal frequency, we should put $f = f_s$, so that the maximum signal frequency range that can be acquired by PLL is,

$$(f_s - f_o)_{max} = \pm K_v K_\phi\,(\pi/2)A\,(f_1/\Delta f_c) \tag{10.38}$$

Now $\Delta f_c = (f_s - f_o)_{max}$

so, $(\Delta f_c)^2 = K_v K_\phi\,(\pi/2)Af_1$ (from Eq. (10.38))

since, $\Delta f_L = \pm K_v K_\phi\,(\pi/2)A$

we get, $(\Delta f_c) \simeq \pm\sqrt{f_1\,\Delta f_L}$ (10.39)

Therefore, the total capture range is,

$$2\,\Delta f_c \simeq 2\sqrt{f_1\,\Delta f_L} \tag{10.40}$$

where the lock-in range $= 2\,\Delta f_L = K_v\,K_\phi\,A\,\pi$. In case of IC PLL 565, $R = 3.6\ \text{k}\Omega$, so the capture range is

$$\pm\left[\frac{\Delta f_L}{2\pi(3.6\times10^3)C}\right]^{\frac{1}{2}} \tag{10.41}$$

where C is in farads.

The capture range is symmetrically located with respect to VCO free running frequency f_o as is shown in Fig. 10.11. The PLL cannot acquire a signal outside the capture range, but

once captured, it will hold on till the signal frequency goes beyond the lock-in range. In order to increase the ability of lock-in range, large capture range is required. However, a large capture range will make the PLL more susceptible to noise and undesirable signal. Hence a suitable compromise is often reached between these two opposing requirements of the

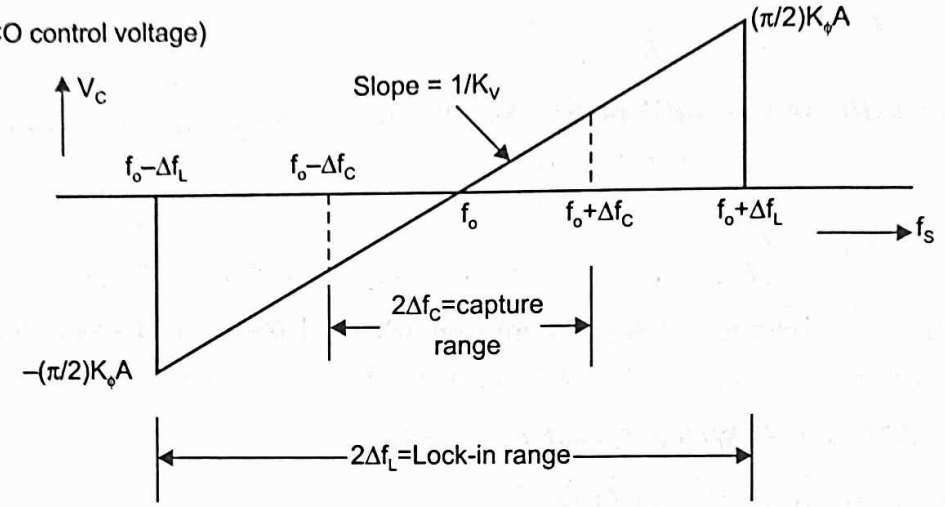


Fig. 10.11 PLL lock-in range and capture range

capture range. Many a times the LPF band-width is first set for a large value for initial acquisition of signal, then once the signal is captured, the band-width of LPF is reduced substantially. This will minimize the interference of undesirable signals and noise.

Example 10.3

The free running frequency of a 565 PLL is 100 kHz, the filter capacitar is 2μF and supply voltage is ± 6V. Compute the lock-in-range, capture range frequency and the value of external components R_T & C_T.

Solution

Given f_o = 100 kHz, C = 2μF and V_{CC} = ± 6V.

We know that the lock-in range is given by

$$\Delta f_L = \pm \frac{7.8 f_o}{V} \qquad \text{[from Eq. (10.29)]}$$

$$= \pm \frac{7.8 f_o}{V_{CC} - (-V_{CC})}$$

$$= \pm \frac{7.8 \triangle 100}{6 - (-6)V} = \pm 65 \text{ kHz}$$

Thus lock-in range = ± 65 kHz

The capture range, $2\Delta f_C$ is given by

$$2\Delta f_C = \pm \sqrt{\frac{\Delta f_L}{2\pi(\times 3.6 \times 10^3)C}} \qquad \text{[from Eq. (10.41)]}$$

Putting the values and solving, we get

$$2\Delta f_C = 2.397 \text{ kHz}$$

Further, the free running frequency, f_o is

$$f_o = \frac{0.25}{R_T C_T} \qquad \text{[from Eq. (10.16)]}$$

Assuming $R_T = 10\text{K}\Omega$, we obtain

$C_T = 250$ pF.

Example 10.4

Compute the free running frequency f_o, lock-in range and capture range of PLL 565. Assume $R_T = 20$ KΩ, $C_T = 0.01$ μF, $C = 1$ μF and supply voltage is ± 6V.

Solution

Given $R_T = 10$ KΩ, $C_T = 0.01$ μF and $C = 1$μF

The free running frequency of VCO is

$$f_o = \frac{0.25}{R_T C_T} = \frac{0.25}{10 \times 10^3 \times 0.01 \times 10^{-6}}$$

$$= 2.5 \text{ kHz}$$

The lock in range is given by

$$\Delta f_L = \pm \frac{7.8 f_o}{V} = \pm \frac{7.8 \times 2.5 \times 10^3}{12}$$

$$= 1.62 \text{ kHz}$$

The capture range is given by

$$2\Delta f_C = \sqrt{\frac{\Delta f_L}{2\pi \times (3.6 \times 10^3) C}}$$

$$= \sqrt{\frac{2 \times 1.62 \times 10^3}{2\pi \times (3.6 \times 10^3) \times 1 \times 10^{-6}}}$$

$$= 378 \text{ Hz}$$

10.7 PLL APPLICATIONS

The output from a PLL system can be obtained either as the voltage signal $v_c(t)$ corresponding to the error voltage in the feedback loop, or as a frequency signal at VCO output terminal. The voltage output is used in frequency discriminator application whereas the frequency output is used in signal conditioning, frequency synthesis or clock recovery applications.

Consider the case of voltage output. When PLL is locked to an input frequency, the error voltage $v_c(t)$ is proportional to $(f_s - f_o)$. If the input frequency is varied as in the case of FM signal, v_c will also vary in order to maintain the lock. Thus the voltage output serves as a frequency discriminator which converts the input frequency changes to voltage changes.

In the case of frequency output, if the input signal is comprised of many frequency components corrupted with noise and other disturbances, the PLL can be made to lock, selectively on one particular frequency component at the input. The output of VCO would then regenerate that particular frequency (because of LPF which gives output for beat frequency) and attenuate heavily other frequencies. VCO output thus can be used for regenerating or reconditioning a desired frequency signal (which is weak and buried in noise) out of many undesirable frequency signals.

Some of the typical applications of PLL are discussed now.

10.7.1 Frequency Multiplication/Division

Figure 10.12 gives the block diagram of a ***frequency multiplier*** using PLL. A divide by N network is inserted between the VCO output and the phase comparator input. In the locked state, the VCO output frequency f_0 is given by,

$$f_0 = N f_s \tag{10.42}$$

The multiplication factor can be obtained by selecting a proper scaling factor N of the counter.

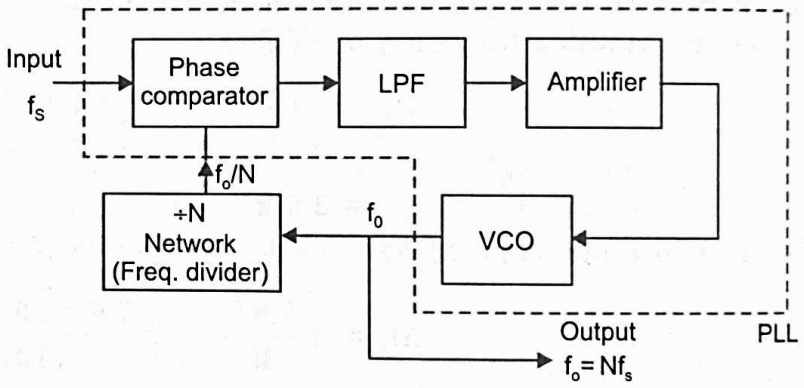


Fig. 10.12 Frequency multiplier using IC PLL

Frequency multiplication can also be obtained by using PLL in its harmonic locking mode. If the input signal is rich in harmonics e.g. square wave, pulse train etc., then VCO can be directly locked to the n-th harmonic of the input signal without connecting any frequency divider in between. However, as the amplitude of the higher order harmonics becomes less, effective locking may not take place for high values of n. Typically n is kept less than 10.

The circuit of Fig. 10.12 can also be used for frequency division. Since the VCO output (a square wave) is rich in harmonics, it is possible to lock the m-th harmonic of the VCO output with the input signal f_s. The output f_0 of VCO is now given by

$$f_0 = \frac{f_s}{m} \tag{10.43}$$

10.7.2 Frequency Translation

A schematic for shifting the frequency of an oscillator by a small factor is shown in Fig. 10.13. It can be seen that a mixer (or multiplier) and a low pass filter are connected externally to the PLL. The signal f_s which has to be shifted and the output frequency f_0 of the VCO are applied as inputs to the mixer. The output of the mixer contains the sum and difference of f_s and f_0. However, the output of LPF contains only the difference signal $(f_0 - f_s)$. The translation or offset frequency $f_1 (f_1 << f_s)$ is applied to the phase comparator. When PLL is in locked state,

$$f_0 - f_s = f_1$$

or

$$f_0 = f_s + f_1 \tag{10.44}$$

Thus, it is possible to shift the incoming frequency f_s by f_1.

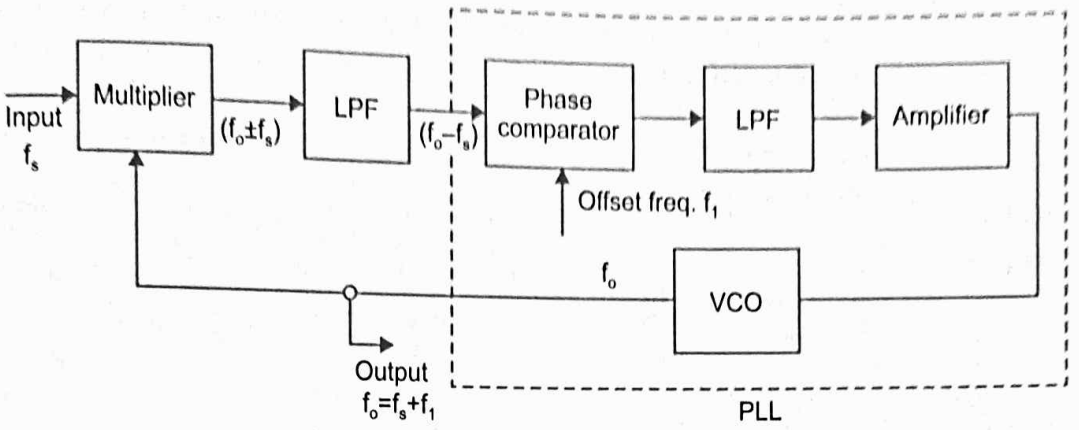


Fig. 10.13 PLL used as a frequency translator

10.7.3 AM Detection

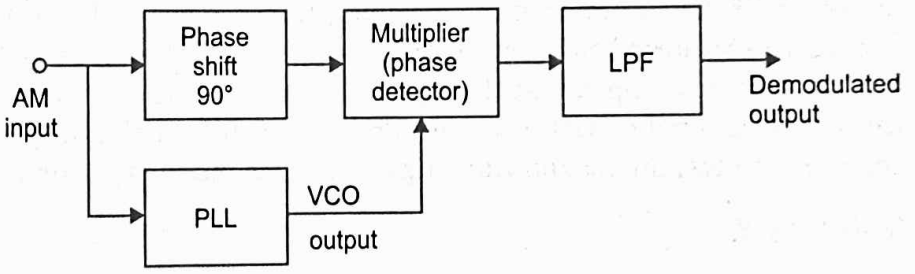


Fig. 10.14 PLL used as AM demodulator

A PLL may be used to demodulate AM signals as shown in Fig. 10.14. The PLL is locked to the carrier frequency of the incoming AM signal. The output of VCO which has the same frequency as the carrier, but unmodulated is fed to the multiplier. Since VCO output is always 90° out of phase with the incoming AM signal under the locked condition, the AM input signal is also shifted in phase by 90° before being fed to the multiplier. This makes both the signals applied to the multiplier in same phase. The output of the multiplier contains both the sum and the difference signals, the demodulated output is obtained after filtering high frequency components by the LPF. Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits a high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

10.7.4 FM Demodulation

If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output. The VCO transfer characteristics determine the linearity of the demodulated output. Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.

10.7.5 Frequency Shift Keying (FSK) Demodulator

In digital data communication and computer peripheral, binary data is transmitted by means of a carrier frequency which is shifted between two preset frequencies. This type of data transmission is called frequency shift keying (FSK) technique. The binary data can be retrieved

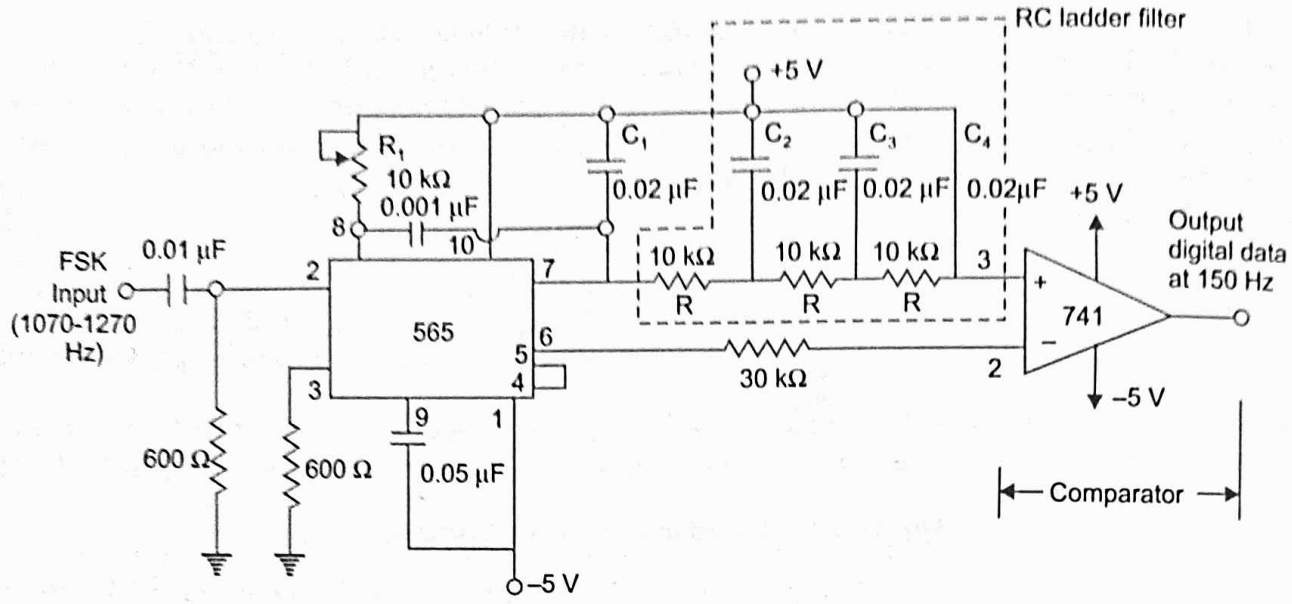


Fig. 10.15 FSK demodulator

using a FSK demodulator at the receiving end. The 565 PLL is very useful as a FSK demodulator. Figure 10.15 shows FSK demodulator using PLL for tele-typewriter signals of 1070 Hz and 1270 Hz. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output. A three stage filter removes the carrier component and the output signal is made logic compatible by a voltage comparator.

SUMMARY

1. A phase locked loop consists of a phase detector, low pass filter, amplifier and a VCO in feedback loop.
2. The important characteristics of a PLL are: lock-in range, capture range and pull-in-time.
3. The lock-in range is usually greater than the capture range. The capture range depends upon the LPF characteristics.
4. The phase detectors are of two types: analog and digital. The phase detector is basically a multiplier.
5. The frequency of VCO can be set by an external capacitor and resistor. The output frequency f_o of VCO is compared with the incoming signal f_s. When $f_o = f_s$, the PLL is said to be locked.
6. The low pass filter may be passive or active type. The LPF controls the capture range and lock range of PLL.
7. Signetics SE/NE 560 series – 560, 561, 562, 564, 565 and 567 are monolithic PLLs. All the blocks of a PLL are also available as independent ICs and can be interconnected to make a PLL.
8. The PLLs are used as frequency multiplier, divider, AM and FM demodulator, FSK demodulator etc.

REVIEW QUESTIONS

10.1. List the basic building blocks of a PLL.
10.2. Define capture range, lock-in range and pull-in-time.
10.3. Which is greater 'Capture range' or 'Lock-in range'?

10.4. What is the major difference between digital and analog PLLs?
10.5. Give the block diagram of IC 566 VCO and explain its operation.
10.6. What is the range of modulating input voltage applied to a VCO?
10.7. List the applications of PLL.
10.8. Draw the circuit of a PLL AM detector and explain its operation.

PROBLEMS

10.1. In the VCO of Fig. 10.7 calculate the change in output frequency if the supply voltage is varied between 9 V and 11 V. Assume $V_{cc} = 12$ V, $R_T = 6.8$ kΩ, $C_T = 75$ pF, $R_1 = 15$ kΩ and $R_2 = 100$ kΩ.
10.2. Determine the dc control voltage v_c at lock if signal frequency $f_s = 10$ kHz, VCO free running frequency is 10.66 kHz and the voltage to frequency transfer coefficient of VCO is 6600 Hz/V.
10.3. If $f_s = 100$ kHz, the voltage to frequency transfer coefficient of VCO, $K_v = 2$ MHz/V, f_o the VCO frequency is 5 MHz and $N = 100$ in the frequency multiplier of Fig. 10.12, what is the dc control voltage at lock?
10.4. Calculate output frequency f_o, lock range Δf_L and capture range Δf_c of a 565 PLL if $R_T = 10$ kΩ, $C_T = 0.01$ μF and $C = 10$ μF.
10.5. Repeat Problem 10.4 for $C_T = 470$ pF.

EXPERIMENT

(a) To study the operation of NE 565 PLL.
(b) To use NE 565 as a multiplier.

PROCEDURE

1. Make connections of the PLL as shown in Fig. E. 10.1 (a).
2. Measure the free running frequency of VCO at pin 4, with the input signal V_{in} set equal to zero. Compare it with the calculated value = $0.25/R_TC_T$.
3. Now apply the input signal of 1 V_{pp} square wave at a 1 kHz to pin 2. Connect one channel of the scope to pin 2 and display this signal on the scope.

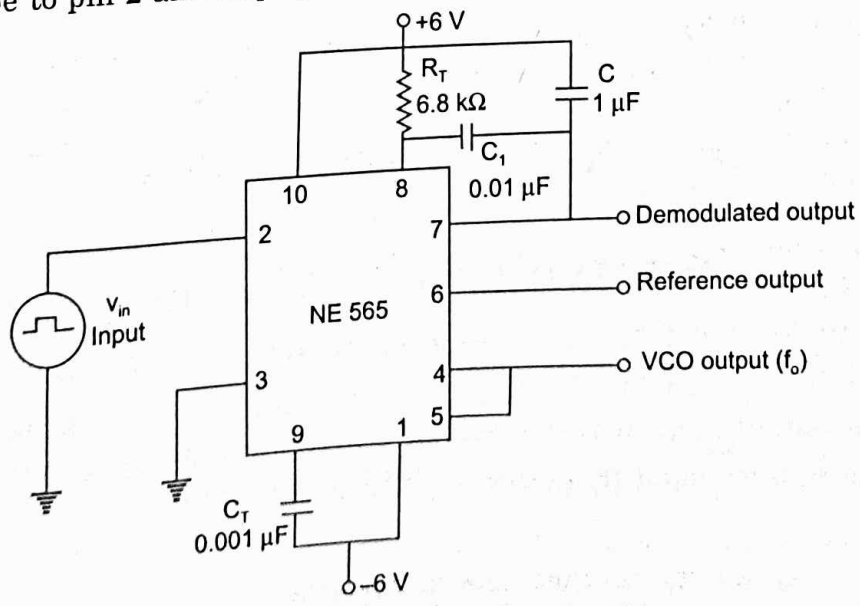


Fig. E. 10.1 (a) NE565 PLL connection diagram

4. Gradually increase the input frequency till the PLL is locked to the input frequency. This frequency f_1 gives the lower end of the capture range. Go on increasing the input frequency, till PLL tracks the input signal, say, to a frequency f_2. This frequency f_2 gives the upper end of the lock range. If input frequency is increased further, the loop will get unlocked.
5. Now gradually decrease the input frequency till the PLL is again locked. This is the frequency f_3, the upper end of the capture range. Keep on decreasing the input frequency until the loop is unlocked. This frequency f_4 gives the lower end of the lock range.
6. The lock-in range $\Delta f_L = (f_2 - f_4)$. Compare it with the calculated value of $\frac{\pm 7.8 f_o}{12}$. Also the capture range is $\Delta f_c = (f_3 - f_1)$. Compare it with the calculated value of capture range.

$$\Delta f_c = \pm \left[\frac{\Delta f_L}{(2\pi)(3.6)(10^3) \times C} \right]^{\frac{1}{2}}$$

7. To use PLL as a multiplier, make connections as shown in Fig. E. 10.1 (b). The circuit uses a 4-bit binary counter 7490 used as a divide-by-5 circuit.

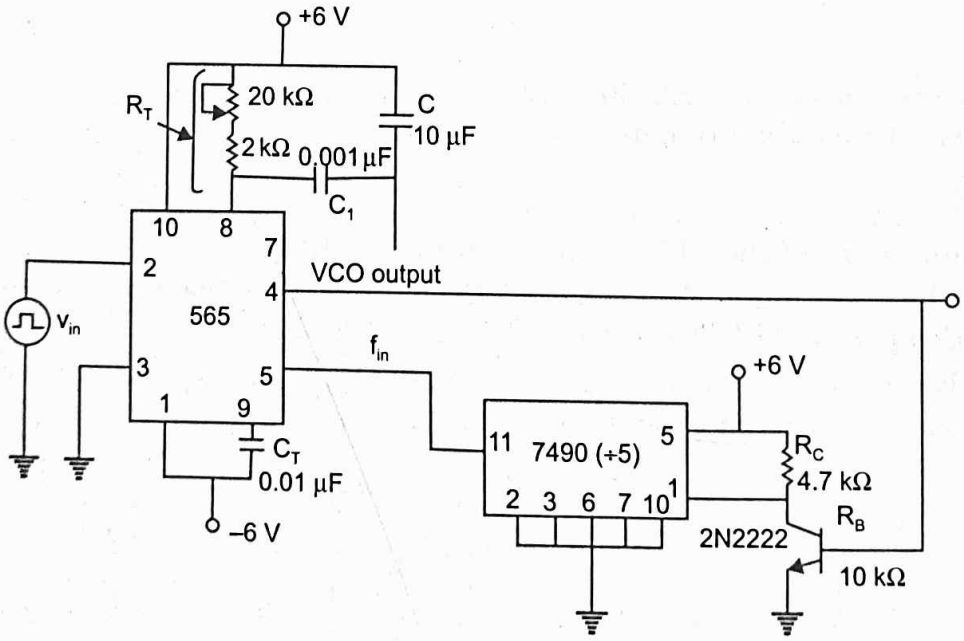


Fig. E. 10.1 (b) NE 565 as a frequency multiplier

8. Set the input signal at 1 V_{pp} square wave at 500 Hz.
9. Vary the VCO frequency by adjusting the 20 kΩ potentiometer till the PLL is locked. Measure the output frequency. It should be 5 times the input frequency.
10. Repeat steps 8, 9 for input frequency of 1 kHz and 1.5 kHz.

11

D-A AND A-D CONVERTERS

11.1 INTRODUCTION

Most of the real-world physical quantities such as voltage, current, temperature, pressure and time etc. are available in analog form. Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store or transmit the analog signal without introducing considerable error because of the superim-position of noise as in the case of amplitude modulation. Therefore, for processing, transmission and storage purposes, it is often convenient to express these variables in digital form. It gives better accuracy and reduces noise. The operation of any digital communication system is based upon analog to digital (A/D) and digital to analog (D/A) conversion.

Figure 11.1 highlights a typical application within which A/D and D/A conversion is used. The analog signal obtained from the transducer is band limited by antialiasing filter. The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal. The sampled signal has to be held constant while conversion is taking place in A/D converter. This requires that ADC should be preceded by a sample and hold (S/H) circuit. The ADC output is a sequence in binary digit. The micro-computer or digital signal processor performs the numerical calculations of the desired control algorithm. The D/A converter is to convert digital signal into analog and hence the function of DAC is exactly opposite to that of ADC. The D/A converter is usually operated at the same frequency as the ADC. The output of a D/A converter is commonly a staircase. This staircase-like digital output is passed through a smoothing filter to reduce the effect of quantization noise.

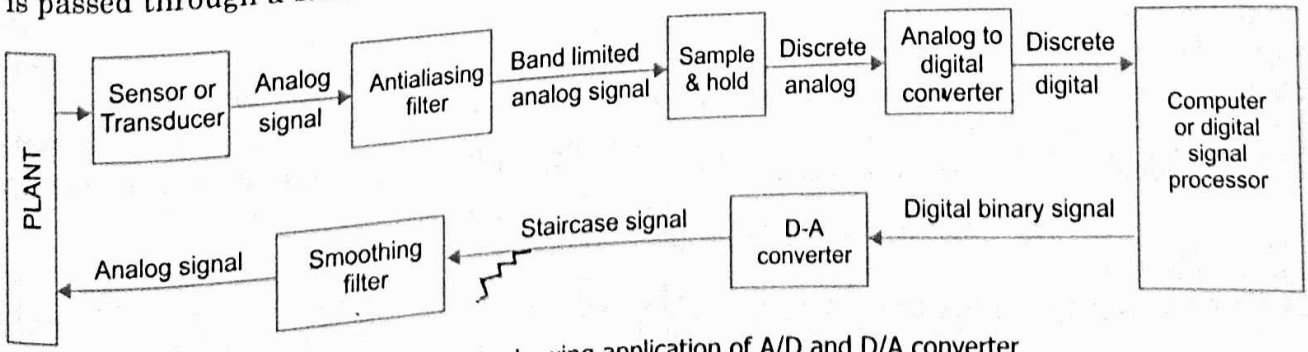


Fig. 11.1 Circuit showing application of A/D and D/A converter

The scheme given in Fig. 11.1 is used either in full or in part in applications such as digital audio recording and playback, computer, music and video synthesis, pulse code modulation transmission, data acquisition, digital multimeter, direct digital control, digital signal processing, microprocessor based instrumentation.

Both ADC and DAC are also known as data converters and are available in IC form. It may be mentioned here that for slowly varying signal, sometimes sample and hold circuit may be avoided without considerable error. The A-D conversion usually makes use of a D-A converter so we shall first discuss DAC followed by ADC.

11.2 BASIC DAC TECHNIQUES

The schematic of a DAC is shown in Fig. 11.2. The input is an n-bit binary word D and is combined with a reference voltage V_R to give an analog output signal. The output of a DAC can be either a voltage or current. For a voltage output DAC, the D/A converter is mathematically described as

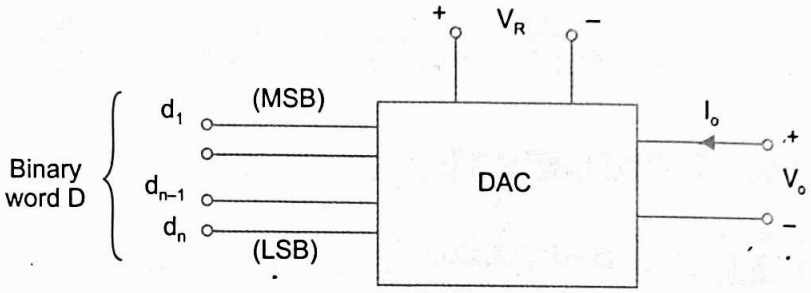


Fig. 11.2 Schematic of a DAC

$$V_o = K\, V_{FS}\, (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}) \tag{11.1}$$

where, V_o = output voltage

V_{FS} = full scale output voltage

K = scaling factor usually adjusted to unity

$d_1 d_2 \ldots d_n$ = n-bit binary fractional word with the decimal point located at the left

d_1 = most significant bit (MSB) with a weight of $V_{FS}/2$

d_n = least significant bit (LSB) with a weight of $V_{FS}/2^n$

There are various ways to implement Eq. (11.1). Here we shall discuss the following resistive techniques only:

Weighted resistor DAC

R-2R ladder

Inverted R-2R ladder

11.2.1 Weighted Resistor DAC

One of the simplest circuits shown in Fig. 11.3 (a) uses a summing amplifier with a binary weighted resistor network. It has n-electronic switches $d_1, d_2, \ldots, d_n$ controlled by binary input word. These switches are single pole double throw (SPDT) type. If the binary input to a particular switch is 1, it connects the resistance to the reference voltage ($-V_R$). And if the input bit is 0, the switch connects the resistor to the ground. From Fig. 11.3 (a), the output current I_o for an ideal op-amp can be written as

$$I_o = I_1 + I_2 + \ldots + I_n$$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \ldots + \frac{V_R}{2^n R} d_n$$

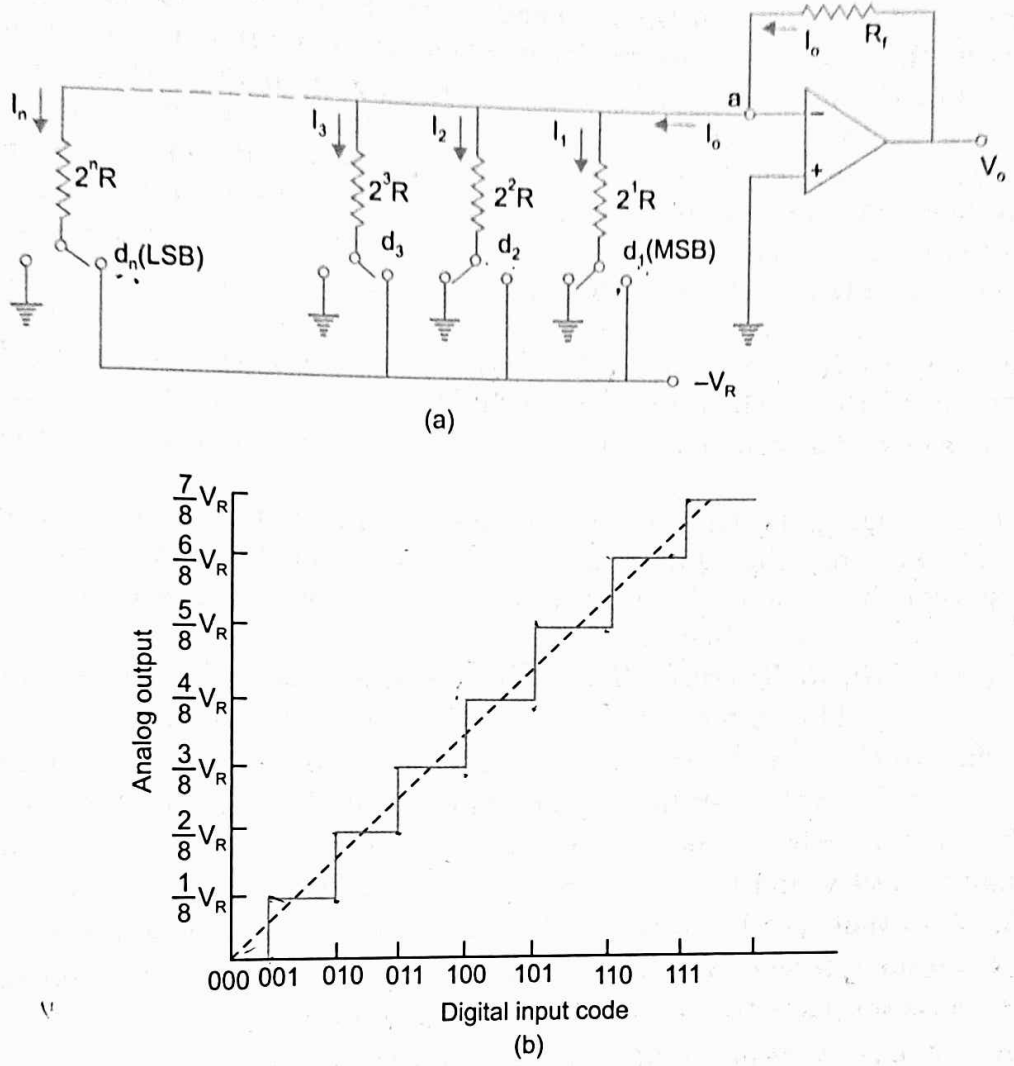


Fig. 11.3 (a) A simple weighted resistor DAC, (b) Transfer characteristics of a 3-bit DAC

$$= \frac{V_R}{R}(d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n})$$

The output voltage

$$V_o = I_o R_f = V_R \frac{R_f}{R}(d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}) \quad (11.2)$$

Comparing Eq. (11.1) with Eq. (11.2), it can be seen that if $R_f = R$ then $K = 1$ and $V_{FS} = V_R$.

The circuit shown in Fig. 11.3 (a) uses a negative reference voltage. The analog output voltage is therefore positive staircase as shown in Fig. 11.3 (b) for a 3-bit weighted resistor DAC. It may be noted that

(i) Although the op-amp in Fig. 11.3 (a) is connected in inverting mode, it can also be connected in non-inverting mode.
(ii) The op-amp is simply working as a current to voltage converter.
(iii) The polarity of the reference voltage is chosen in accordance with the type of the switch used. For example, for TTL compatible switches, the reference voltage should be +5 V and the output will be negative.

The accuracy and stability of a DAC depends upon the accuracy of the resistors and the tracking of each other with temperature. There are however a number of problems associated with this type of DAC. One of the disadvantages of binary weighted type DAC is the wide range of resistor values required. It may be observed that for better resolution, the input binary word length has to be increased. Thus, as the number of bit increases, the range of resistance value increases. For 8-bit DAC, the resistors required are 2^0R, 2^1R, 2^2R, ..., 2^7R. The largest resistor is 128 times the smallest one for only 8-bit DAC. For a 12-bit DAC, the largest resistance required is 5.12 MΩ if the smallest is 2.5 kΩ. The fabrication of such a large resistance in IC is not practical. Also the voltage drop across such a large resistor due to the bias current would also affect the accuracy. The choice of smallest resistor value as 2.5 kΩ is reasonable; otherwise loading effect will be there. The difficulty of achieving and maintaining accurate ratios over such a wide range especially in monolithic form restricts the use of weighted resistor DACs to below 8-bits.

The switches in Fig. 11.3 (a) are in series with resistors and therefore, their ***on*** resistance must be very low and they should have zero offset voltage. Bipolar transistors do not perform well as voltage switches, due to the inherent offset voltage when in saturation. However, by using MOSFET, this can be achieved.

Different types of ***digitally controlled SPDT electronic switches*** are available of which two are shown in Fig. 11.4. A totem-pole MOSFET driver in Fig. 11.4 (a) feeds each resistor connected to the inverting input terminal 'a' of Fig. 11.3 (a). The two complementary gate inputs Q and $\overline{Q}$ come from MOSFET S-R flip-flop or a binary cell of a register which holds one bit of the digital information to be converted to an analog number. Assume a negative logic, i.e. logic '1' corresponds to – 10 V and logic '0' corresponds to zero volt. If there is '1' in the bit line, $S = 1$ and $R = 0$ so that $Q = 1$ and $\overline{Q} = 0$. This drives the transistor Q_1 ***on***, thus connecting the resistor R_1 to the reference voltage $-V_R$ whereas the transistor Q_2 remains ***off***. Similarly a '0' at the bit line connects the resistor R_1 to the ground terminal.

Another SPDT switch of Fig. 11.4(b) consists of CMOS inverter feeding an op-amp voltage follower which drives R_1 from a very low output resistance. The circuit is using a positive logic with $V(1) = V_R = +5$ V and $V(0) = 0$ V. The complement $\overline{Q}$ of the bit under consideration is applied at the input. Thus $\overline{Q} = 0$ makes transistor Q_1 ***off*** and Q_2 ***on***. The output of the CMOS inverter is at logic 1, that is, 5 V is applied to resistor R_1 through the voltage follower. And if $\overline{Q} = 1$ the output of the CMOS inverter is 0 V connecting the resistance R_1 to ground.

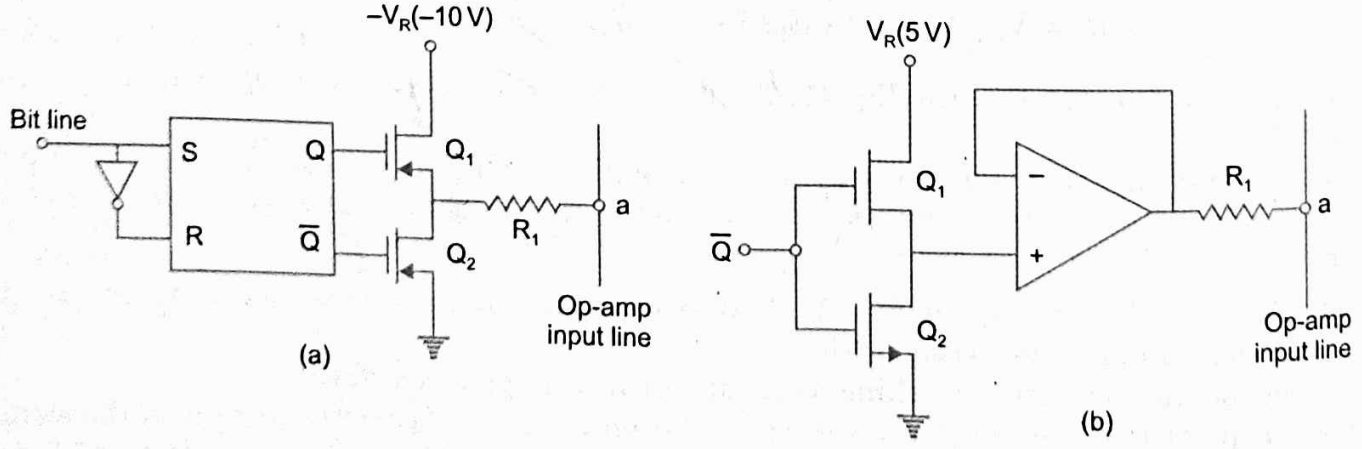


Fig. 11.4 (a) A totem pole MOSFET switch (b) CMOS inverter as switch

11.2.2 R-2R Ladder DAC

Wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required. It is well suited for integrated circuit realization. The typical value of R ranges from 2.5 kΩ to 10 kΩ.

For simplicity, consider a 3-bit DAC as shown in Fig. 11.5 (a), where the switch position $d_1\, d_2\, d_3$ corresponds to the binary word 100. The circuit can be simplified to the equivalent form of Fig. 11.5 (b) and finally to Fig. 11.5 (c). Then, voltage at node C can be easily calculated by the set procedure of network analysis as

$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R+\frac{2}{3}R} = -\frac{V_R}{4}$$

The output voltage is

$$V_o = \frac{-2R}{R}\left(-\frac{V_R}{4}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

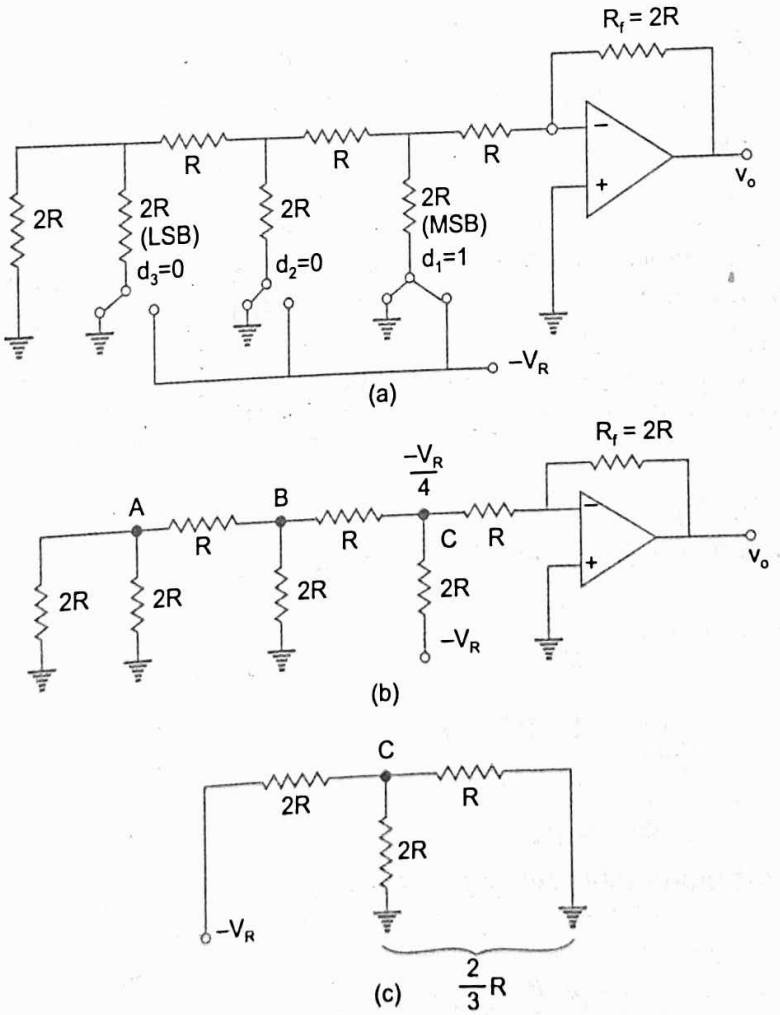


Fig. 11.5 (a) R-2R ladder DAC, (b) Equivalent circuit of (a), (c) Equivalent circuit of (b)

The switch position corresponding to the binary word 001 in 3 bit DAC is shown in Fig. 11.6 (a). The circuit can be simplified to the equivalent form of Fig. 11.6 (b). The voltages at the nodes (A, B, C) formed by resistor branches are easily calculated in a similar fashion and the output voltage becomes

$$V_o = \left(-\frac{2R}{R}\right)\left(-\frac{V_R}{16}\right) = \frac{V_R}{8} = \frac{V_{FS}}{8}$$

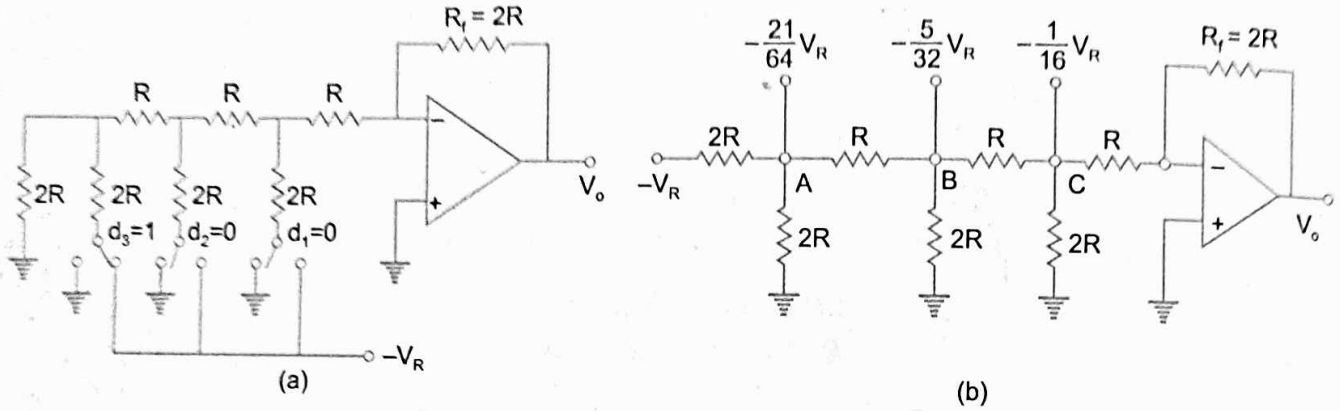


Fig. 11.6 (a) R-2R ladder DAC for switch positions 001, (b) Equivalent circuit

In a similar fashion, the output voltage for R-2R ladder type DAC corresponding to other 3-bit binary words can be calculated.

Example 11.1

Consider a 4 bit R-$2R$ ladder DAC of the type shown in Fig 11.5 (a). Given R = 10 KΩ and V_R = 10 V. Determine the value of the feedback resistance R_f for the following output conditions.

(i) value of 1 LSB at the output is 0.5V
(ii) analog output is 6V for a binary input of 1000
(iii) full scale output voltage is 10 V

Solution

(i) Given R = 10 KΩ, V_R = 10V and n = 4
The resolution of a $R - 2R$ ladder DAC is given by

$$\text{Resolution, } V = \frac{1}{2^n} \times \frac{V_R}{R} \times R_f$$

Thus
$$0.5V = \frac{1 \times 10V \times R_f}{2^4 \times 10 \times 10^3}$$

or
$$R_f = 8 \text{ KΩ}$$

(ii) For binary digital input 1000, setting $d_1 = 1$ and $d_2 = d_3 = d_4 = 0$ in Fig 11.3(a), we can write

$$V_o = V_R \frac{R_f}{R}\left(d_1 2^{-1} + d_2\, 2^{-2} + d_3 2^{-3} + d_4\, 2^{-4}\right)$$

$$6 = \frac{R_f \times 10V \times 2^{-1}}{10 \times 10^3} \left(\text{as } d_2 = d_3 = d_4 = 0\right)$$

Therefore, $R_f = 12\ \text{K}\Omega$

(iii) Now $d_1 = d_2 = d_3 = d_4 = 1$. Thus for getting the full scale voltage of 10V,

$$R_f \times \frac{10}{10 \times 10^3}\left(2^{-1} + 2^{-2} + 2^{-3} + 2^{-4}\right) = 10$$

Thus $R_f = 10.667\ \text{K}\Omega$

11.2.3 Inverted R-2R Ladder

In weighted resistor type DAC and R-2R ladder type DAC, current flowing in the resistors changes as the input data changes. More power dissipation causes heating, which in turn, creates non-linearity in DAC. This is a serious problem and can be avoided completely in 'Inverted R-2R ladder type DAC'. A 3-bit Inverted R-2R ladder type DAC is shown in Fig. 11.7 (a) where the position of MSB and LSB is interchanged. Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is also at virtual ground. Since both the terminals of switches d_i are at ground potential, current flowing in the resistances is constant and independent of switch position, i.e. independent of input binary word. In Fig. 11.7 (a), when switch d_i is at logical '0' i.e., to the left, the current through 2R resistor flows to the ground and when the switch d_i is at logical '1' i.e., to the right, the current through 2R sinks to the virtual ground. The circuit has the important property that the current divides equally at each of the nodes. This is because the equivalent resistance to the right or to the left of any node is exactly 2 R. The division of the current is shown in Fig. 11.7 (b). Consider a reference current of 2 mA. Just to the right of node *A*, the equivalent resistor is 2 R. Thus 2 mA of reference input current divides equally to value 1 mA at node *A*. Similarly to the right of node *B*, the equivalent resistor is 2 R. Thus 1 mA of current further divides to value 0.5 mA at node *B*. Similarly, current divides equally at node *C* to 0.25 mA. The equal division of current in successive nodes remains the same in the 'inverted R-2R ladder' irrespective of the input binary word. Thus the currents remain constant in each branch of the ladder. Since constant current implies constant voltage, the ladder node voltages remain constant at $V_R/2^0$, $V_R/2^1$, $V_R/2^2$. The circuit works on the principle of summing currents and is also said to operate in the current mode. The most important advantage of the current mode or inverted ladder is that since the ladder node voltages remain constant even with changing input binary words (codes), the stray capacitances are not able to produce slow-down effects on the performance of the circuit.

It may be noted that the switches used in Fig. 11.7 (a) are the SPDT switches discussed earlier. According to bit d_i, the corresponding switch gets connected either to ground for $d_i = 0$ or to $-V_R$ for $d_i = 1$. The current flows from inverting input terminal to $-V_R$ for $d_i = 1$ and from ground to $-V_R$ for $d_i = 0$. Regardless of the binary input word, the current in the resistive branches of the inverted ladder circuit remains always constant as explained in Fig. 11.7(b). However, the current through the feedback resistor R is the summing current depending upon the input binary word. It may further be mentioned that, Fig. 11.7 (b) shows only the current division for making the analysis simple, though it is a voltage driven DAC.

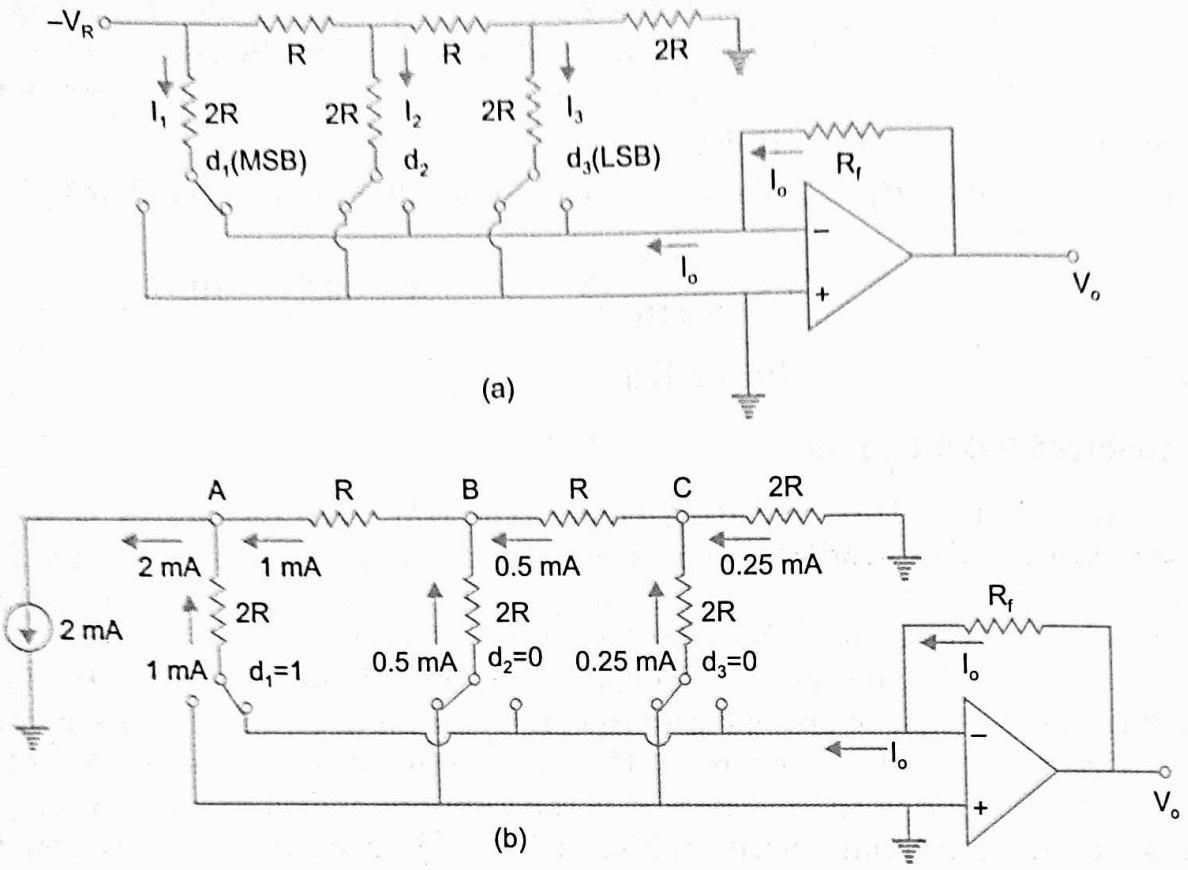


Fig. 11.7 (a) Inverted R-2R ladder DAC, (b) Inverted R-2R ladder DAC showing division of current for digital input word 001

Example 11.2

Consider the inverted $R - 2R$ ladder DAC shown in Fig 11.7 (a) Given $R = R_f = 10$ KΩ and $V_R = 10$V. Calculate the output voltage for the binary input of 1110.

Solution

In Fig 11.7 (a),

$$I_1 = \frac{V_R}{2R} = \frac{10V}{2 \times 10 \times 10^3} = 0.5 \text{ mA}$$

$$I_2 = \frac{I_1}{2} = 0.25 \text{ mA}$$

and

$$I_3 = \frac{I_2}{2} = 0.125 \text{ mA}$$

Therefore, current

$$I_o = I_1 + I_2 + I_3$$
$$= 0.5 + 0.25 + 0.125 \text{ mA}$$
$$= 0.875 \text{ mA}$$

The output voltage,

$$V_o = I_o \times R_f$$
$$= 0.875 \times 10^{-3} \times 10 \times 10^3$$
$$= 8.75 \text{ V}$$

11.2.4 Multiplying DACs

A digital to analog converter which uses a varying reference voltage V_R is called a multiplying D/A converter (MDAC). Thus if in the Eq. (11.1), the reference voltage v_R is a sine wave given by

$$v_R(t) = V_{im} \cos 2\pi ft$$

Then, $$v_o(t) = V_{om} \cos (2\pi ft + 180°)$$

where V_{om} will vary from 0V to $(1-2^{-n})\ V_{im}$ depending upon the input code. When used like this, MDAC behaves as a digitally controlled audio attenuator because the output V_o is a fraction of the voltage representing the input digital code and the attenuator setting can be controlled by digital logic. If followed by an op-amp integrator, the MDAC provides digitally programmable integration which can be used in the design of digitally programmable oscillators, filters.

11.2.5 Monolithic DAC : 1408 DAC

Monolithic DACs consisting of R-2R ladder, switches and the feedback resistor are available for 8, 10, 12, 14 and 16 bit resolution from various manufacturers. The MC 1408L is a 8-bit DAC with a current output. The SE/NE 5018 is also a 8-bit DAC but with a voltage output. There are hybrid D/A converters available in DATEL DAC-HZ series for current as well as voltage output.

A typical 8-bit DAC 1408 compatible with TTL and CMOS logic with settling time around 300 ns is shown in Fig. 11.8 (a). It has eight input data lines d_1 (MSB) through d_8 (LSB). It requires 2 mA reference current for full scale input and two power supplies V_{CC} = +5 V and V_{EE} – 5 V (V_{EE} can range from – 5 V to –15 V). The total reference current source is determined by resistor R_{14} and voltage reference V_R and is equal to V_R/R_{14} = 5 V/2.5 kΩ = 2 mA. The resistor $R_{15} = R_{14}$ match the input impedance of the reference source. The output current I_o is calculated as

$$I_o = \frac{V_R}{R_{14}} \left(\sum_{i=1}^{8} d_i\, 2^{-i} \right); d_i = 0 \text{ or } 1$$

For full scale input (i.e. d_8 through d_1 = 1)

$$I_o = \frac{5\text{ V}}{2.5\text{ k}\Omega} \left(\sum_{i=1}^{8} 1 \times 2^{-i} \right) = 2 \text{ mA } (255/256) = 1.992 \text{ mA}$$

The output is 1 LSB less than the full scale reference current of 2 mA. So, the output voltage V_o for the full scale input is

$$V_o = 2 \text{ mA } (255/256) \times 5 \text{ k}\Omega = 9.961 \text{ V}$$

In general, the output voltage V_o is given by

$$V_o = \frac{V_R}{R_{14}} R_f \left[\frac{d_1}{2} + \frac{d_2}{4} + \frac{d_3}{8} + \ldots + \frac{d_8}{256} \right]$$

The 1408 DAC can be calibrated for bipolar range from –5 V to +5 V by adding resistor R_B (5 kΩ) between V_R and output pin 4 as shown in Fig. 11.8 (b). The resistor R_B supplies 1 mA (= V_R/R_B) current to the output in the opposite direction of the current generated by the input signal. Therefore the output current for the bipolar operation I_o' is

$$I_o' = I_o - (V_R/R_B) = (V_R/R_{14}) \left(\sum_{i=1}^{8} d_i 2^{-i} \right) - (V_R/R_B)$$

For binary input word = 00000000, i.e. zero input, the output becomes,

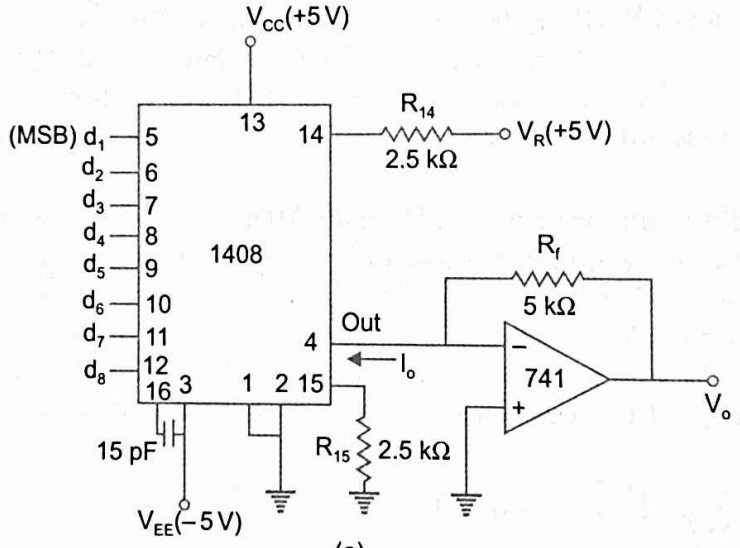
$$V_o = I_o' R_f = (I_o - V_R/R_B)R_f = (0 - 5\text{ V}/5\text{ k}\Omega) \times 5\text{ k}\Omega = -5\text{ V}$$

For binary input word = 10000000, output V_o becomes

$$V_o = (I_o - V_R/R_B)R_f = [(V_R/R_{14})\ (d_1/2) - (V_R/R_B)]R_f$$
$$= [(5\text{ V}/2.5\text{ k}\Omega)\ (1/2) - (5\text{ V}/5\text{ k}\Omega)]\ 5\text{ k}\Omega = (1\text{ mA} - 1\text{ mA}) \times 5\text{ k}\Omega = 0\text{ V}$$

For binary input word = 11111111, output V_o becomes

$$V_o = [(V_R/R_{14})\ (255/256) - (V_R/R_B)]R_f = (1.992\text{ mA} - 1\text{ mA}) \times 5\text{ k}\Omega$$
$$= 0.992\text{ mA} \times 5\text{ k}\Omega = +4.960\text{ V}$$



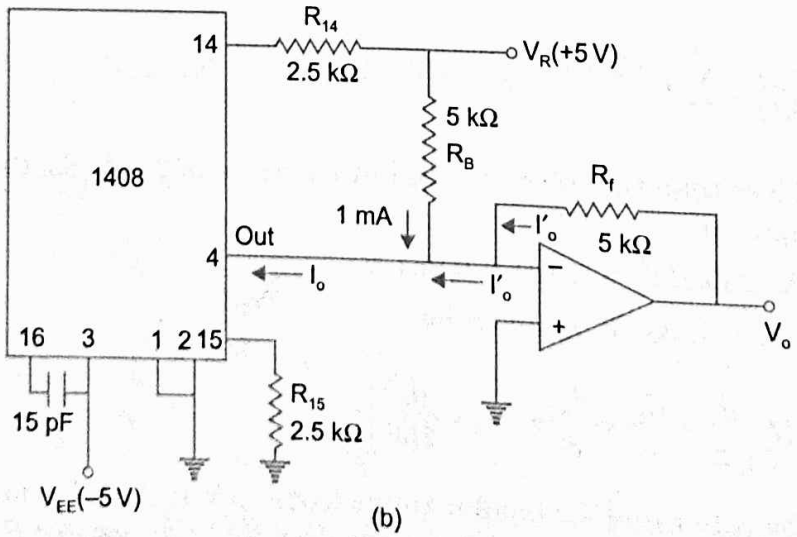


Fig. 11.8 1408 D/A converter (a) Voltage output in unipolar range (b) Modified circuit for bipolar output

Example 11.3

The basic step of a 9-bit DAC is 10.3 mV. If 000000000 represents 0 V, what output is produced if the input is 101101111?

Solution

The output voltage for input 101101111 is

$= 10.3 \text{ mV } (1 \times 2^8 + 0 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0)$

$= 10.3 \text{ mV } (367) = 3.78 \text{ V}$

Example 11.4

Calculate the values of the LSB, MSB and full scale output for an 8-bit DAC for the 0 to 10 V range.

Solution

$$\text{LSB} = \frac{1}{2^8} = \frac{1}{256}$$

For 10 V range, $$\text{LSB} = \frac{10 \text{ V}}{256} = 39 \text{ mV}$$

and $$\text{MSB} = \left(\frac{1}{2}\right) \text{ full scale} = 5 \text{ V}$$

Full scale output = (Full scale voltage – 1 LSB)

$= 10 \text{ V} - 0.039 \text{ V} = 9.961 \text{ V}$

Example 11.5

What output voltage would be produced by a D/A converter whose output range is 0 to 10 V and whose input binary number is

(i) 10 (for a 2-bit D/A converter)
(ii) 0110 (for a 4-bit DAC)
(iii) 10111100 (for a 8-bit DAC)

Solution

(i) $V_o = 10 \text{ V} \left(1 \times \frac{1}{2} + 0 \times \frac{1}{4}\right) = 5 \text{ V}$

(ii) $V_o = 10 \text{ V} \left(0 \times \frac{1}{2} + 1 \times \frac{1}{2^2} + 1 \times \frac{1}{2^3} + 0 \times \frac{1}{2^4}\right)$

$= 10\left(\frac{1}{4} + \frac{1}{8}\right) = 3.75 \text{ V}$

(iii) $V_o = 10 \text{ V } (1 \times 1/2 + 0 \times 1/2^2 + 1 \times 1/2^3 + 1 \times 1/2^4 + 1 \times 1/2^5$
$+ 1 \times 1/2^6 + 0 \times 1/2^7 + 0 \times 1/2^8)$

$= 10 \text{ V } (1/2 + 1/8 + 1/16 + 1/32 + 1/64) = 7.34 \text{ V}$

11.3 A-D CONVERTERS

The block schematic of ADC shown in Fig. 11.9 provides the function just opposite to that of a DAC. It accepts an analog input voltage V_a and produces an output binary word $d_1 d_2 ... d_n$ of

functional value D, so that

$$D = d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n} \qquad (11.3)$$

where d_1 is the most significant bit and d_n is the least significant bit. An ADC usually has two additional control lines: the START input to tell the ADC when to start the conversion and the EOC (end of conversion) output to announce when the conversion is complete. Depending upon the type of application, ADCs are designed for microprocessor interfacing or to directly drive LCD or LED displays.

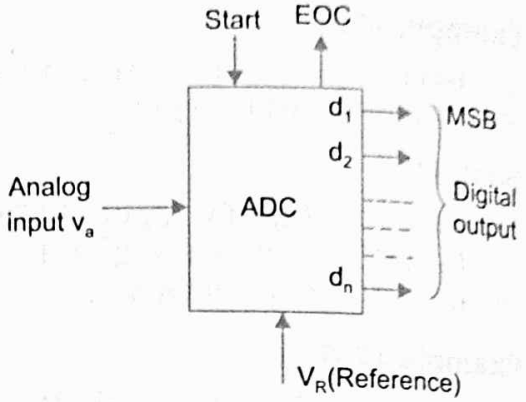


Fig. 11.9 Functional diagram of ADC

ADCs are classified broadly into two groups according to their conversion technique. Direct type ADCs and Integrating type ADCs. Direct type ADCs compare a given analog signal with the internally generated equivalent signal. This group includes

Flash (comparator) type converter
Counter type converter
Tracking or servo converter
Successive approximation type converter

Integrating type ADCs perform conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to a digital code. The two most widely used integrating type converters are:

(i) Charge balancing ADC
(ii) Dual slope ADC

The most commonly used ADCs are successive approximation and the integrator type. The successive approximation ADCs are used in applications such as data loggers and instrumentation where conversion speed is important. The successive approximation and comparator type are faster but generally less accurate than integrating type converters. The flash (comparator) type is expensive for high degree of accuracy. The integrating type converter is used in applications such as digital meter, panel meter and monitoring systems where the conversion accuracy is critical.

DIRECT TYPE ADCs

11.3.1 The Parallel Comparator (Flash) A/D Converter

This is the simplest possible A/D converter. It is at the same time, the fastest and most expensive technique. Figure 11.10 (a) shows a 3-bit A/D converter. The circuit consists of a resistive divider network, 8 op-amp comparators and a 8-line to 3-line encoder (3-bit priority encoder). The comparator and its truth table is shown in Fig. 11.10 (b). A small amount of hysteresis is built into the comparator to resolve any problems that might occur if both inputs were of equal voltage as shown in the truth table. Coming back to Fig. 11.10 (a), at each node of the resistive divider, a comparison voltage is available. Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between the reference voltage V_R and the ground. The purpose of the circuit is to compare the analog input voltage V_a with each of the node voltages. The truth table for the flash type AD converter is shown in Fig. 11.10 (c). The circuit has the advantage of high speed as the

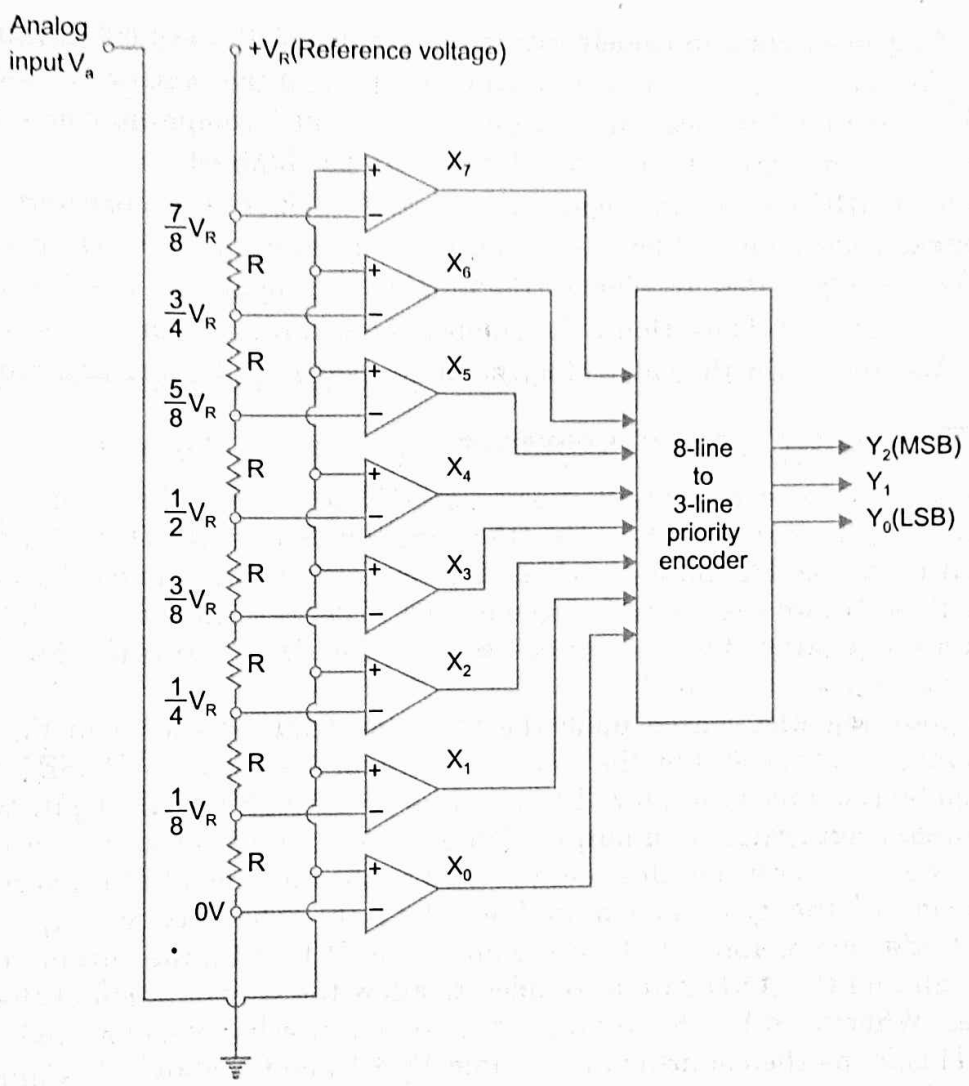


Fig. 11.10 (a) Basic circuit of a flash type A/D converter

Voltage input	*Logic output X*
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value

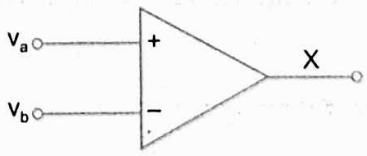


Fig. 11.10 (b) Comparator and its truth table

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$ to 3 $V_R/4$	0	0	1	1	1	1	1	1	1	0	1
3 $V_R/4$ to 7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Fig. 11.10 (c) Truth table for a flash type A/D converter

conversion take place simultaneously rather than sequentially. Typical conversion time is 100 ns or less. Conversion time is limited only by the speed of the comparator and of the priority encoder. By using an Advanced Micro Devices AMD 686A comparator and a T1147 priority encoder, conversion delays of the order of 20 ns can be obtained.

This type of ADC has the disadvantage that the number of comparators required almost doubles for each added bit. A 2-bit ADC requires 3 comparators, 3-bit ADC needs 7, whereas 4-bit requires 15 comparators. In general, the number of comparators required are $2^n - 1$ where n is the desired number of bits. Hence the number of comparators approximately doubles for each added bit. Also the larger the value of n, the more complex is the priority encoder.

11.3.2 The Counter Type A/D Converter

The D to A converter can easily be turned around to provide the inverse function A to D conversion. The principle is to adjust the DAC's input code until the DAC's output comes within ± (1/2) LSB to the analog input V_a which is to be converted to binary digital form. Thus in addition to the DAC, we need suitable logic circuitry to perform the code search and a comparator of adequate quality to announce when the DAC output has come within ± (1/2) LSB to V_a.

A 3-bit counting ADC based upon the above principle is shown in Fig. 11.11 (a). The counter is reset to zero count by the reset pulse. Upon the release of RESET, the clock pulses are counted by the binary counter. These pulses go through the AND gate which is enabled by the voltage comparator high output. The number of pulses counted increase with time. The binary word representing this count is used as the input of a D/A converter whose output is a staircase of the type shown in Fig. 11.11 (b). The analog output V_d of DAC is compared to the analog input V_a by the comparator. If $V_a > V_d$, the output of the comparator becomes high and the AND gate is enabled to allow the transmission of the clock pulses to the counter. When $V_a < V_d$, the output of the comparator becomes low and the AND gate is disabled. This stops the counting at the time $V_a \leq V_d$ and the digital output of the counter represents the analog input voltage V_a. For a new value of analog input V_a, a second reset pulse is applied to clear the counter. Upon the end of the reset, the counting begins again as shown in Fig. 11.11 (b). The counter frequency must be low enough to give sufficient time

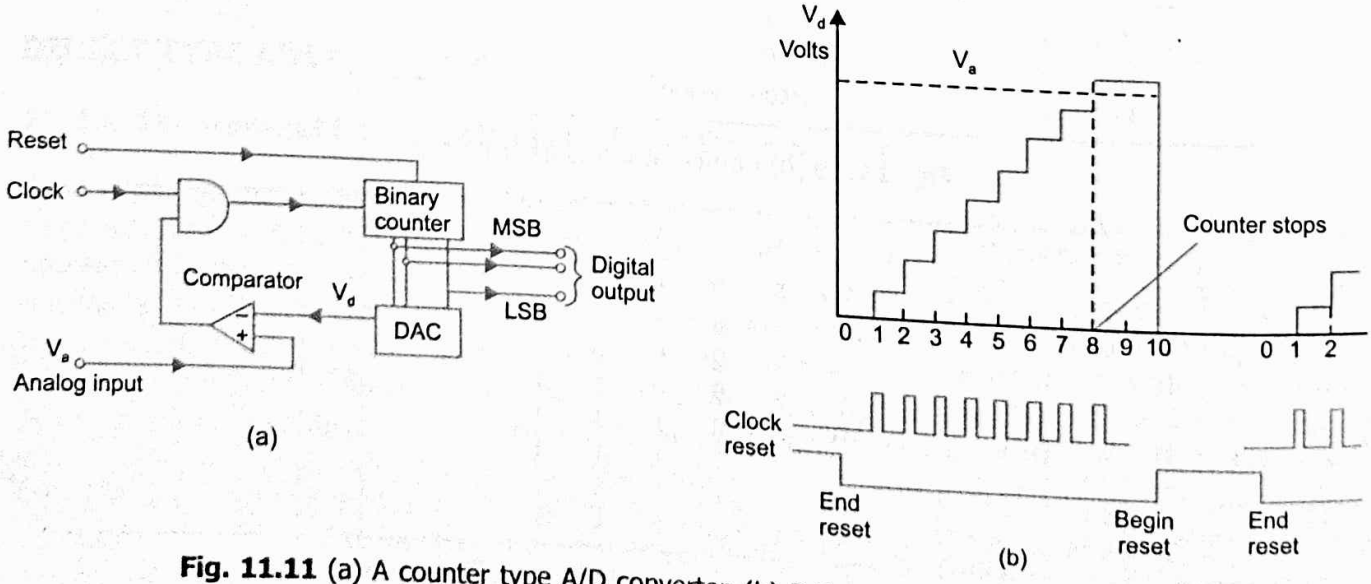


Fig. 11.11 (a) A counter type A/D converter, (b) D/A output staircase waveform

for the DAC to settle and for the comparator to respond. Low speed is the most serious drawback of this method. The conversion time can be as long as $(2^n - 1)$ clock periods depending upon the magnitude of input voltage V_a. For instance, a 12-bit system with 1 MHz clock frequency, the counter will take $(2^{12} - 1)$ μs = 4.095 ms to convert a full scale input.

If the analog input voltage varies with time, the input signal is sampled, using a sample and hold circuit before it is applied to the comparator. If the maximum value of the analog voltage is represented by n-pulses and if the clock period is T seconds, the minimum interval between samples is nT seconds.

11.3.3 Servo Tracking A/D Converter

An improved version of counting ADC is the tracking or a servo converter shown in Fig. 11.12 (a). The circuit consists of an up/down counter with the comparator controlling the direction of the count. The analog output of the DAC is V_d and is compared with the analog input V_a. If the input V_a is greater than the DAC output signal, the output of the comparator goes high and the counter is caused to count up. The DAC output increases with each incoming clock pulse and when it becomes more than V_a, the counter reverses the direction and counts down (but only by one count, LSB). This causes the control to count up and the count increases by 1 LSB. The process goes on being repeated and the digital output changes back and forth by ±1 LSB around the correct value. As long as the analog input changes slowly, the tracking A/D will be within one LSB of the correct value. However, when the analog input changes rapidly, the tracking A/D cannot keep up with the change and error occurs as shown in Fig. 11.12 (b).

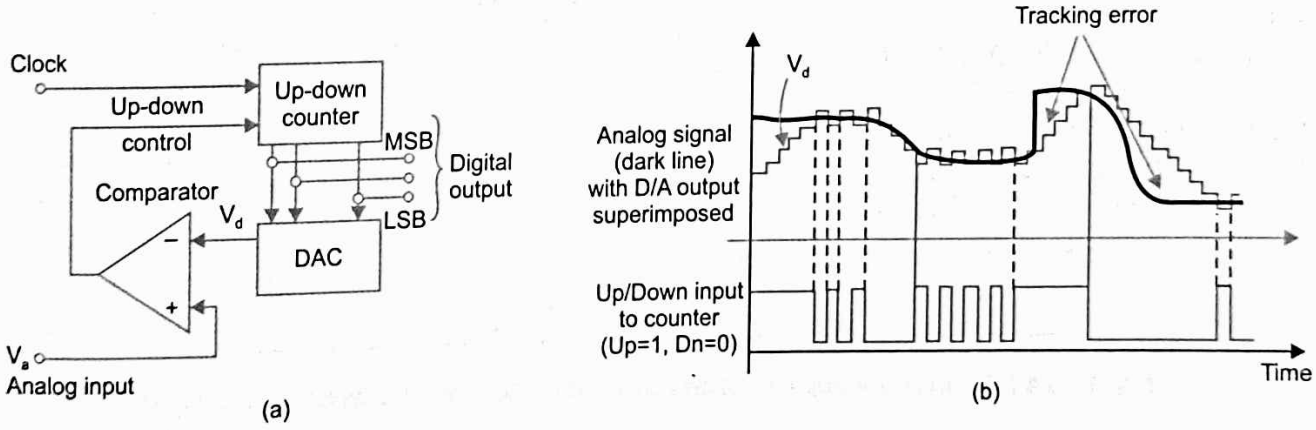


Fig. 11.12 (a) A tracking A/D converter, (b) Waveforms associated with a tracking A/D converter

The tracking ADC has the advantage of being simple. The disadvantage, however, is the time needed to stabilize as a new conversion value is directly proportional to the rate at which the analog signal changes.

11.3.4 Successive Approximation Converter

The successive approximation technique uses a very efficient code search strategy to complete n-bit conversion in just n-clock periods. An eight bit converter would require eight clock pulses to obtain a digital output. Figure 11.13 shows an eight bit converter. The circuit uses a

successive approximation register (SAR) to find the required value of each bit by trial and error. The circuit operates as follows. With the arrival of the START command, the SAR sets the MSB $d_1 = 1$ with all other bits to zero so that the trial code is 10000000. The output V_d of the DAC is now compared with analog input V_a. If V_a is greater than the DAC output V_d then 10000000 is less than the correct digital representation. The MSB is left at '1' and the next lower significant bit is made '1' and further tested.

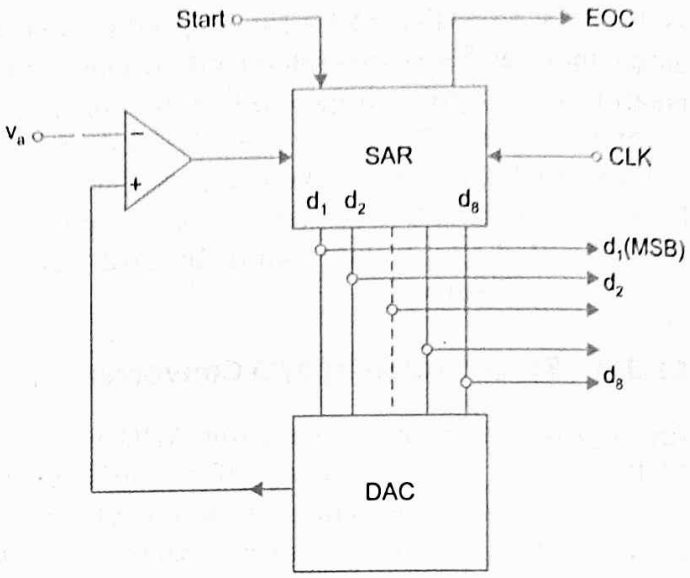


Fig. 11.13 Functional diagram of the successive approximation ADC

However, if V_a is less than the DAC output, then 10000000 is greater than the correct digital representation. So reset MSB to '0' and go on to the next lower significant bit. This procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested. Whenever the DAC output crosses V_a, the comparator changes state and this can be taken as the **end of conversion** (EOC) command. Figure 11.14 (a) shows a typical conversion sequence and Fig. 11.14 (b).

Correct digital representation	*Successive approximation register output V_d at different stages in conversion*	*Comparator output*
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

Fig. 11.14 (a) Successive approximation conversion sequence for a typical analog input

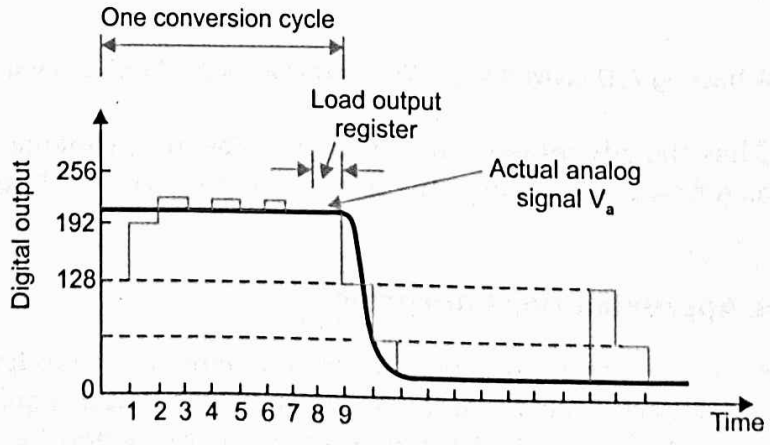


Fig. 11.14 (b) The D/A output voltage is seen to become successively closer to the actual analog input voltage

shows the associated wave forms. It can be seen that the D/A output voltage becomes successively closer to the actual analog input voltage. It requires eight pulses to establish the accurate output regardless of the value of the analog input. However, one additional clock pulse is used to load the output register and reinitialize the circuit.

A comparison of the speed of an eight bit tracking ADC and an eight bit successive approximation ADC is made in Fig. 11.15. Given the same clock frequency, we see that the tracking circuit is faster only for small changes in the input. In general, the successive approximation technique is more versatile and superior to all other circuits discussed so far.

Successive approximation ADCs are available as self contained ICs. The AD7592 (Analog Devices Co.) a 28-pin dual-in-line CMOS package is a 12-bit A/D converter using successive approximation technique.

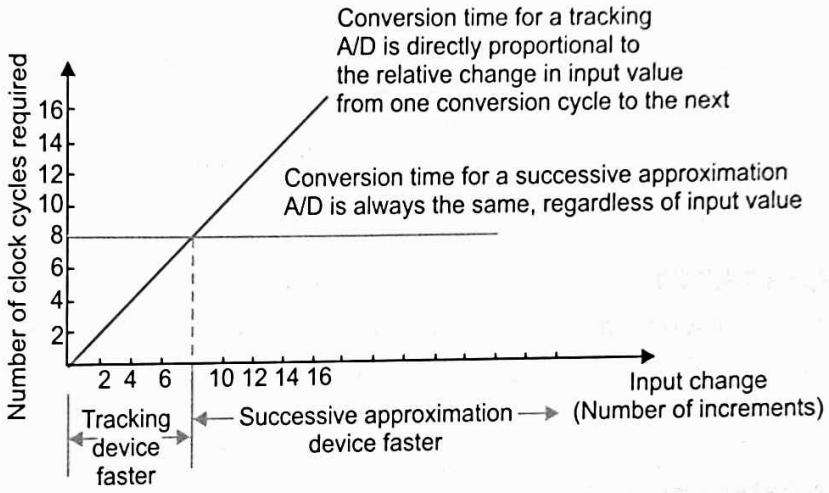


Fig. 11.15 Comparison of conversion times for tracking and successive approximation A/D devices

Example 11.6

An 8-bit A/D converter is used for converting 0 to 10V input voltage. Determine :

(i) input voltage required to change by 1 LSB
(ii) input voltage required to generate all 1's at the output
(iii) the digital output for an input voltage of 4.8V

Solution

(i) $1 \text{ LSB} = \frac{10V}{2^8} = 39.1 \text{ mV}$

(ii) Since digital output starts from 0 in a A/D converter, therefore the maximum full-scale input voltage will produce output less by 1 LSB for all digital output 1's.
Thus, $V_{iFS} = 10V - 39.1 \text{ mV} = 9.961 \text{ V}$.

(iii) The digital output for an input voltage of 4.8V is given by

$$D = \frac{4.8\,V}{39.1\,mV} = 122.76$$

$$= 123$$

Converting this to binary gives the digital output as 01111011.

Example 11.7

The conversion rate of a 8-bit ADC is 9 μs. Find the maximum frequency of the input sine wave that can be digitized.

Solution

The maximum frequency is given by

$$f_{max} = \frac{1}{2\pi(T_C)2^n}$$

$$= \frac{1}{2\pi \times 9 \times 10^{-6} \times 2^8}$$

$$= 69.07 \text{ Hz.}$$

Integrating Type of ADCs

The integrating type of ADCs do not require a S/H circuit at the input. If the input changes during conversion, the ADC output code will be proportional to the value of the input averaged over the integration period.

11.3.5 Charge Balancing ADC

The principle of charge balancing ADC is to first convert the input signal to a frequency using a voltage to frequency (V/F) converter. This frequency is then measured by a counter and converted to an output code proportional to the analog input. The main advantage of these converters is that it is possible to transmit frequency even in noisy environment or in isolated form. However, the limitation of the circuit is that the output of V/F converter depends upon an RC product whose value cannot be easily maintained with temperature and time. The drawback of the charge balancing ADC is eliminated by the dual slope conversion.

11.3.6 Dual-Slope ADC

Figure 11.16 (a) shows the functional diagram of the dual-slope or dual-ramp converter. The analog part of the circuit consists of a high input impedance buffer A_1, precision integrator A_2 and a voltage comparator. The converter first integrates the analog input signal V_a for a fixed duration of 2^n clock periods as shown in Fig. 11.16 (b). Then it integrates an internal reference voltage V_R of opposite polarity until the integrator output is zero. The number N of clock cycles required to return the integrator to zero is proportional to the value of V_a averaged over the integration period. Hence N represents the desired output code. The circuit operates as follows:

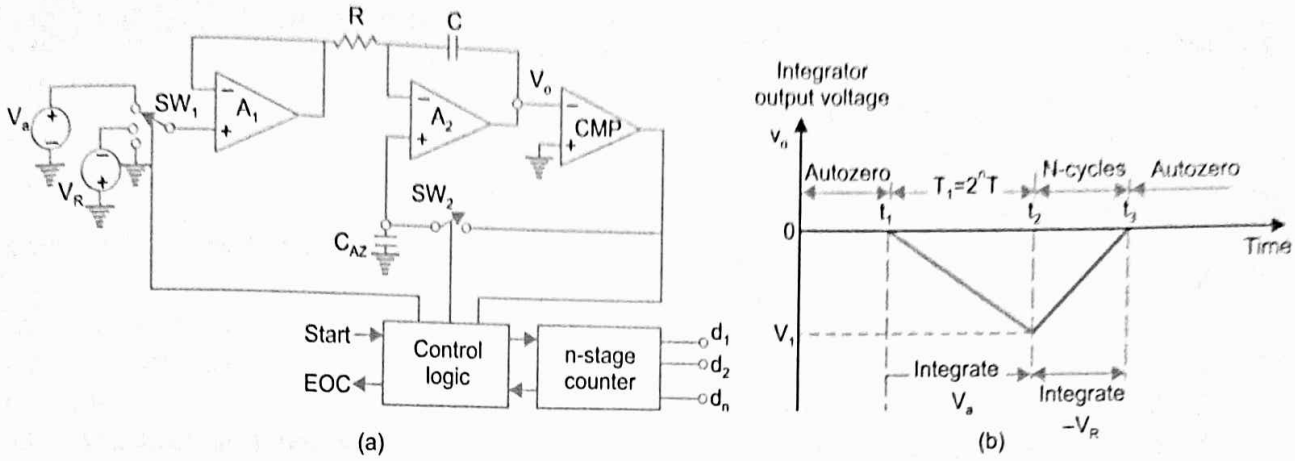


Fig. 11.16 (a) Functional diagram of the dual slope ADC (b) Integrated output waveform for the dual slope ADC

Before the START command arrives, the switch SW_1 is connected to ground and SW_2 is closed. Any offset voltage present in the A_1, A_2, comparator loop after integration, appears across the capacitor C_{AZ} till the threshold of the comparator is achieved. The capacitor C_{AZ} thus provides automatic compensation for the input-offset voltages of all the three amplifiers. Later, when SW_2 opens, C_{AZ} acts as a memory to hold the voltage required to keep the offset nulled. At the arrival of the START command at $t = t_1$, the control logic opens SW_2 and connects SW_1 to V_a and enables the counter starting from zero. The circuit uses an n-stage ripple counter and therefore the counter resets to zero after counting 2^n pulses. The analog voltage V_a is integrated for a fixed number 2^n counts of clock pulses after which the counter resets to zero. If the clock period is T, the integration takes place for a time $T_1 = 2^n \times T$ and the output is a ramp going downwards as shown in Fig. 11.16 (b).

The counter resets itself to zero at the end of the interval T_1 and the switch SW_1 is connected to the reference voltage ($-V_R$). The output voltage v_o will now have a positive slope. As long as v_o is negative, the output of the comparator is positive and the control logic allows the clock pulse to be counted. However, when v_o becomes just zero at time $t = t_3$, the control logic issues an end of conversion (EOC) command and no further clock pulses enter the counter. It can be shown that the reading of the counter at t_3 is proportional to the analog input voltage V_a.

In Fig. 11.16 (b)

$$T_1 = t_2 - t_1 = \frac{2^n \text{ counts}}{\text{clock rate}} \tag{11.4}$$

and

$$t_3 - t_2 = \frac{\text{digital count } N}{\text{clock rate}} \tag{11.5}$$

For an integrator,

$$\Delta v_o = (-1/RC)\, V(\Delta t) \tag{11.6}$$

The voltage v_o will be equal to v_1 at the instant t_2 and can be written as

$$v_1 = (-1/RC)\, V_a(t_2 - t_1)$$

The voltage v_1 is also given by

$$v_1 = (-1/RC)\, (-V_R)\, (t_2 - t_3)$$

So, $V_a(t_2 - t_1) = V_R(t_3 - t_2)$

Putting the values of $(t_2 - t_1) = 2^n$ and $(t_3 - t_2) = N$, we get

$$V_a(2^n) = (V_R)N$$

or, $$V_a = (V_R)\,(N/2^n) \tag{11.7}$$

The following important observations can be made:

1. Since V_R and n are constant, the analog voltage V_a is proportional to the count reading N and is independent of R, C and T.
2. The dual-slope ADC integrates the input signal for a fixed time, hence it provides excellent noise rejection of ac signals whose periods are integral multiples of the integration time T_1. Thus ac noise superimposed on the input signal such as 50 Hz power line pick-up will be averaged during the input integration time. So choose clock period T, so that 2^nT is an exact integral multiple of the line period (1/50) second = 20 ms.
3. The main disadvantage of the dual-slope ADC is the long conversion time. For instance, if $2^n - T = 1/50$ is used to reject line pick-up, the conversion time will be 20 ms.

Dual-slope converters are particularly suitable for accurate measurement of slowly varying signals, such as thermocouples and weighing scales. Dual-slope ADCs also form the basis of digital panel meters and multimeters.

Dual-slope converters are available in monolithic form and are available both in microprocessor compatible and in display oriented versions. The former provide the digital code in binary form whereas the display oriented versions present the output code in a format suitable for the direct drive of LED displays. The Datel Intersil ICL7109 is a monolithic 12-bit dual-slope ADC with microprocessor compatibility.

Example 11.8

A dual slope ADC uses a 16-bit counter and a 4 MHz clock rate. The maximum input voltage is +10 V. The maximum integrator output voltage should be – 8 V when the counter has cycled through 2^n counts. The capacitor used in the integrator is 0.1 μF. Find the value of the resistor R of the integrator.

Solution

Time period $(t_2 - t_1)$ in Fig. 11.16 (b) $= \dfrac{2^{16}}{4\text{ MHz}} = \dfrac{65536}{4\text{ MHz}} = 16.38$ ms

For the integrator

$$\Delta v_o = (-1/RC)\, V_a\,(t_2 - t_1)$$

So, $$RC = -(10\text{ V}/-8\text{ V})\ 16.3\text{ ms} = 20.47\text{ ms}$$

$$R = \frac{20.47\text{ ms}}{0.1\,\mu\text{F}} = 204.7\text{ k}\Omega = 205\text{ k}\Omega$$

Example 11.9

If the analog signal V_a is +4.129 V in the example 11.4, find the equivalent digital number.

Solution

Since, $V_a = V_R(N/2^n)$

So the digital count $N = 2^n\ (V_a/V_R) = 65536\ (4.129\text{ V}/8\text{ V}) = 33825$ for which the binary equivalent is 1000010000100001.

11.4 DAC/ADC SPECIFICATIONS

Both D/A and A/D converters are available with wide range of specifications. The various important specifications of converters generally specified by the manufacturers are analyzed.

Resolution: The resolution of a converter is the smallest change in voltage which may be produced at the output (or input) of the converter. For example, an 8-bit D/A converter has $2^8-1 = 255$ equal intervals. Hence the smallest change in output voltage is (1/255) of the full scale output range. In short, the resolution is the value of the LSB.

$$\text{Resolution (in volts)} = \frac{V_{FS}}{2^n - 1} = 1\,\text{LSB increment} \tag{11.8}$$

However, resolution is stated in a number of different ways. An 8-bit DAC is said to have
: 8 bit resolution
: a resolution of 0.392 of full-scale
: a resolution of 1 part in 255

Similarly, the resolution of an A/D converter is defined as the smallest change in analog input for a one bit change at the output. As an example, the input range of an 8-bit A/D converter is divided into 255 intervals. So the resolution for a 10 V input range is 39.22 mV (= 10 V/255). Table 11.1 gives the resolution for 6–16 bit DACs.

Table 11.1 Resolution for 6-16 bit DACs

Bits	*Intervals*	*LSB size (% of Full Scale)*	*LSB size (10 V Full Scale)*
6	63	1.588	158.8 mV
8	256	0.392	39.2 mV
10	1023	0.0978	9.78 mV
12	4095	0.0244	2.44 mV
14	16383	0.0061	0.61 mV
16	65535	0.0015	0.15 mV

Linearity: The linearity of an A/D or D/A converter is an important measure of its accuracy and tells us how close the converter output is to its ideal transfer characteristics. In an ideal DAC, equal increment in the digital input should produce equal increment in the analog output and the transfer curve should be linear. However, in an actual DAC, output voltages do not fall on a straight line because of gain and offset errors as shown by the solid line curve in Fig. 11.17. The static performance of a DAC is determined by fitting a straight line through the measured output points. The linearity error measures the deviation of the actual output from the fitted

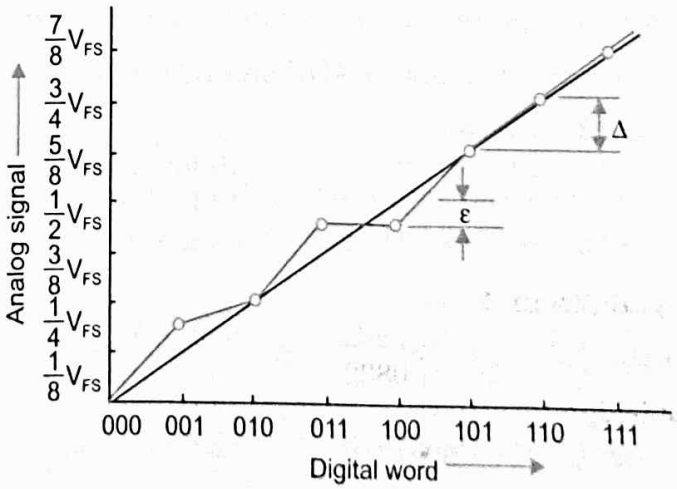


Fig. 11.17 Linearity error for 3-bit DAC

line and is given by ε/Δ as shown in Fig. 11.17. The error is usually expressed as a fraction of LSB increment or percentage of full-scale voltage. A good converter exhibits a linearity error of less than ± (1/2) LSB.

Accuracy: Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. Relative accuracy is the maximum deviation after gain and offset errors have been removed. Data sheets normally specify relative accuracy rather than absolute accuracy. The accuracy of a converter is also specified in terms of LSB increments or percentage of full scale voltage.

Monotonicity: A monotonic DAC is the one whose analog output increases for an increase in digital input. Figure 11.18 represents the transfer curve for a non-monotonic DAC, since the output decreases when input code changes from 001 to 010. A monotonic characteristic is essential in control applications, otherwise oscillations can result. In successive approximation ADCs, a non-monotonic characteristic may lead to missing codes.

If a DAC has to be monotonic, the error should be less than ±(1/2) LSB at each output level. All the commercially available DACs are monotonic because the linearity error never exceeds ±(1/2) LSB at each output level.

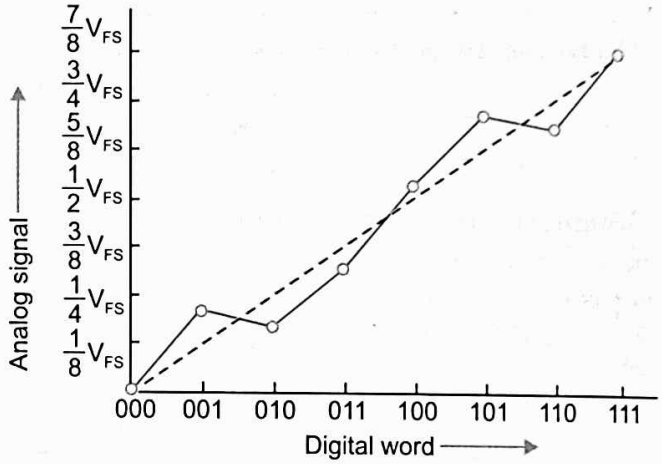


Fig. 11.18 A non-monotonic 3-bit DAC

Settling time: The most important dynamic parameter is the settling time. It represents the time it takes for the output to settle within a specified band ±(1/2) LSB of its final value following a code change at the input (usually a full scale change). It depends upon the switching time of the logic circuitry due to internal parasitic capacitances and inductances. Settling time ranges from 100 ns to 10 μs depending on word length and type of circuit used.

Stability: The performance of converter changes with temperature, age and power supply variations. So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

A brief overview of ADC and DAC selection guide is given below:

A/D converters:	
AD 7520/AD 7530	10-bit binary multiplying type
AD 7521/AD 7531	12-bit binary multiplying type
ADC 0800/0801/0802	8-bit ADC
D/A converters:	
DAC 0800/0801/0802	8-bit DAC
DAC 0830/0831/0832	microprocessor compatible 8-bit DAC
DAC 1200/1201	12-bit DAC
DAC 1208/1209/1210	12-bit microprocessor compatible DAC

Example 11.10

We are familiar with 3½ digit digital voltmeter (DVM) and 4½ digit DVM which are being used regularly in the laboratory. Obviously 3½ digit DVM is less costly as its resolution is poor compared to 4½ digit DVM which is relatively costlier and have better resolution. Let us calculate the resolution of these DVMs.

Solution

In 3½ digit DVM, the MSB can be either 0 or 1 whereas the 3 digit LSBs can be 000 to 999. Hence in 3½ digit DVM, the reading variation can be from 0000 to 1999, that is 2000. The reference voltage is 2 V. Hence the resolution is (2/2000) V = 1 mV; that is voltage variation below 1 mV is not detectable. Similarly, in 4½ digit DVM the total variation is from 0 0000 to 1 9999 and reference voltage is 2 V. Hence the resolution is (2/20000) V = 0.1 mV. Thus, the resolution of a 4½ digit DVM is ten times better than that of 3½ digit DVM.

Example 11.11

Find the resolution and dynamic range of a D/A converter, if the maximum peak to peak output voltage is 5V and the input signal is a 10 bit word.

Solution

The 10-bit word represents $2^{10} = 1024$ levels. The step size is given by

$$= \frac{5V}{1024} = 4.88 \text{ mV}$$

Thus the system can identify input changes as low as 4.88 mv.

The dynamic range is the ratio of the largest value to the smallest value that can be converted. Therefore,

$$\text{Dynamic Range} = \frac{5V}{4.88\text{mv}}$$

$$= 1024$$

The dynamic range is usually given in dBs, so $20\log_{10}^{1024} = 60$ dB.

SUMMARY

1. The output of a DAC can be either a voltage or current.
2. A multiplying DAC is the one in which the analog signal is allowed to vary.
3. Three resistive techniques for D/A conversion are: weighted resistor DAC, R-2R ladder and inverter R-2R ladder.
4. DAC essentially requires: resistors, electronics switches and an op-amp.
5. Two types of digitally controlled SPDT electronic switches are in use: a totem-pole MOSFET driver, a CMOS inverter.
6. A weighted resistor DAC requires a wide range of resistor values for better resolution whereas a R-2R ladder type DAC requires only two values of resistors.

7. In an inverted R-2R ladder, the current through the resistors remains constant, irrespective of the input data. The constant node voltages therefore eliminate stray capacitance effect and improve circuit performance.
8. Monolithic DACs for 8, 10, 12, 14 and 16 bit resolution are available.
9. A/D converters are either direct type or indirect type. Most direct type ADCs require a D/A converter.
10. The important direct ADC techniques are: Parallel comparator (Flash), Counting type, Tracking type and Successive approximation technique.
11. Integrating type ADCs perform conversion in an indirect manner. The two important converters are: Charge balancing ADC, Dual slope ADC.
12. The parallel comparator ADC is the fastest technique. But it has the disadvantage of using maximum hardware. A counting type A/D converter has low speed with conversion time as long as $(2^n - 1)$ clock periods for n-bit ADC. A tracking ADC is simple but gives error when analog signal changes rapidly.
13. Successive approximation type ADC is the most versatile. It completes n-bit conversion in just n-clock periods. Most monolithic ADCs are successive approximation type.
14. Dual slope converters are suitable for precise measurement of slowly varying signals. All digital voltmeters use dual-slope ADC. The disadvantage is of long conversion time.
15. Monolithic dual slope ADCs are available in microprocessor compatible and display-oriented versions.
16. The important converter characteristics are: Resolution, Linearity, Accuracy, Monotonicity, Settling time, Stability etc.

REVIEW QUESTIONS

11.1. Classify DACs on the basis of their output.
11.2. Name the essential parts of a DAC.
11.3. Describe the various types of electronic switches used in D/A converter.
11.4. How many resistors are required in a 12-bit weighted resistor DAC?
11.5. Why is an inverted R-2R ladder network DAC better than R-2R ladder DAC?
11.6. List the various A/D conversion techniques.
11.7. Which is the fastest ADC and why?
11.8. Give the conversion time for (i) counting ADC (ii) successive approximation ADC (iii) dual-slope ADC.
11.9. Explain the operation of Dual-slope ADC.
11.10. Explain how Dual-slope ADC provides noise rejection.
11.11. Explain the important specifications of D/A and A/D converters.

PROBLEMS

11.1. How many levels are possible in a two-bit DAC? What is its resolution if the output range is 0 to 3 V?

11.2. A 5-bit D/A converter is available. Assume that '00000' corresponds to an output of +10 V and that the D/A converter is connected for – 0.1 V per increment, what output voltage will be produced for '11111'?

11.3. If a 10-bit D/A converter spans a range of 0 to 10 V and is always within 1 mV of its ideal output. What is its linearity as a per cent of full-scale range?

11.4. Find the voltage at all nodes 0, 1, 2, ... and at the output of a 5-bit R-2R ladder DAC. The least significant bit is 1 and all other bits are equal to 0. Assume $V_R = -10$ V and $R = 10$ kΩ.

11.5. The Fig. P. 11.5 shows a binary weighted resistor D/A converter.

(i) Show that the output resistance is independent of the digital word and that

$$R_o = \frac{2^{N-1}}{2^N - 1} R$$

(ii) Show that the analog output voltage for the MSB is

$$V_o = \frac{2^{N-1}}{2^N - 1} V_R$$

(iii) Show that the analog output voltage for the LSB is

$$V_o = \frac{1}{2^N - 1} V_R$$

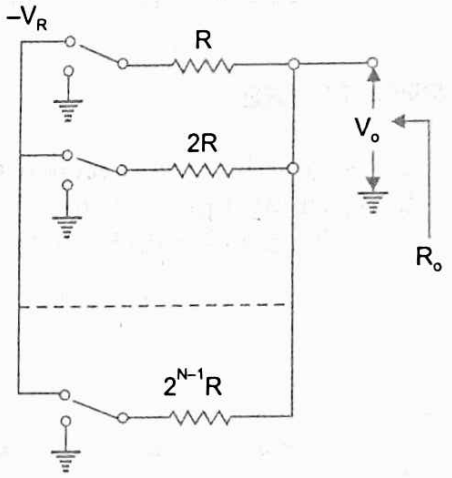


Fig. P. 11.5

10.6. (a) Draw the circuit diagram of a 6-bit inverted R-2R ladder DAC.

(b) For $V(1) = 5$ V, what is the maximum output voltage?

(c) What is the minimum voltage that can be resolved?

11.7. The analog input signal ranges for –5 to +8 V in a nine bit A/D converter.

(i) How many quantization levels are available with this A/D converter?

(ii) What is the resolution in volt per increment?

(iii) What binary number will be produced when the analog input is zero volt?

11.8. A counting A/D converter uses a 7-bit DAC. The MSB of DAC output voltage is +5 V.

(i) If the analog input voltage is +6.85 V, what will be the R-2R ladder output voltage when the clock stops?

(ii) What is the number of clock pulses that occur between the release of reset and stopping of the clock?

11.9. The ADC in problem 11.8 uses a 100 kHz clock. How long did it take to digitize 6.85 V?

11.10. What is the conversion time of a 10-bit successive approximation A/D converter if its input clock is 5 MHz?

11.11. A dual slope ADC uses a 18-bit counter with a 5 MHz clock. The maximum input voltage is +12 V and the maximum integrator output voltage at 2^N count is – 10 V. If R = 100 kΩ, find the size of the capacitor to be used for integrator.

11.12. The dual slope ADC of problem 11.11 has an input voltage of +5.237 V. Determine the digital number in binary which represents the count in the register.

EXPERIMENT 11.1

To construct a 4-bit R-2R ladder type D/A converter. Plot the transfer characteristics, that is, binary input vs output voltage. Calculate the resolution and linearity of the converter from the graph.

(i) Choose R = 10 kΩ, $2R$ = 20 kΩ of tolerance ±1% or less.

(ii) For logic '0' short to ground and logic '1' connect to a +5 V supply.

PROCEDURE

1. Set-up the circuit shown in Fig. E. 11.1.
2. With all inputs (d_0 to d_3) shorted to ground, adjust the 20 kΩ-pot until the output is 0 V. This will nullify any offset voltage at the input of the op-amp.

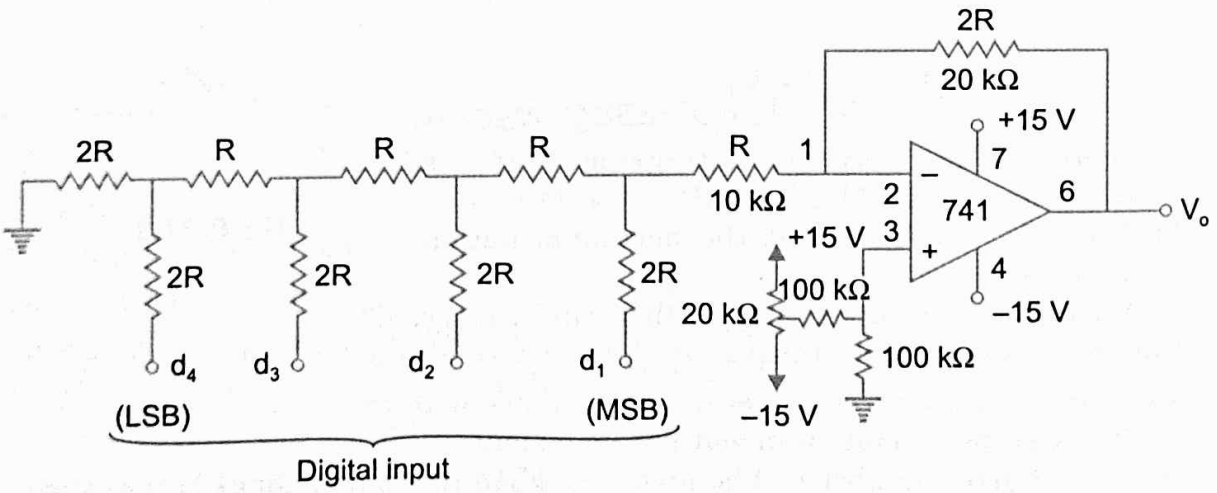


Fig. E. 11.1 A 4-bit R-2R ladder D/A converter

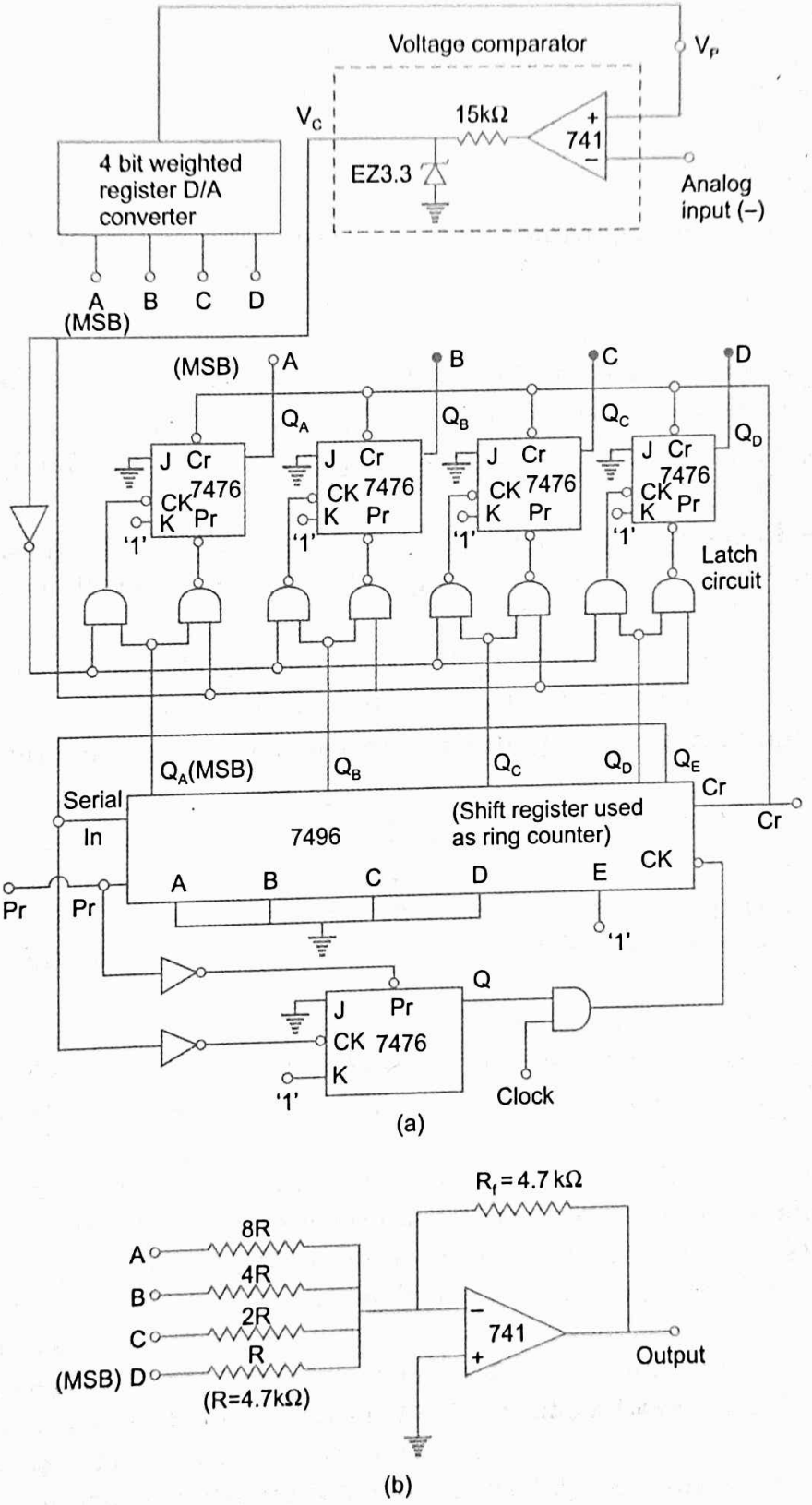


Fig. E. 11.2 (a) Successive approximation A/D converter (b) 4-bit weighted resistor D/A converter

3. Measure the output voltage for all binary inputs (0000 to 1111) states and plot a graph of binary inputs vs output voltage.
4. Measure the size of each step and hence calculate resolution.
5. Calculate linearity using the definition given in Sec. 11.4.

EXPERIMENT 11.2

To set-up a 4-bit successive approximation type A/D converter and study its performance.

PROCEDURE

(i) Set-up the circuit as shown in Fig. E. 11.2 (a). Use the circuit of Fig. E. 11.2 (b) for 4-bit weighted resistor D/A converter.

(ii) Connect the Cr terminal to ground momentarily to clear all the flip-flops and the shift resistor IC 7496.

(iii) Connect the Pr terminal momentarily to logic '1' to set the shift register (being used as ring counter) output as $Q_E = 1$, $Q_A = Q_B = Q_C = Q_D = 0$, this will also enable the AND gate for the clock to be transmitted.

(iv) Apply an analog voltage of – 10 V. Apply clock pulses, and observe the stable digital output available at the outputs Q_D, Q_C, Q_B, Q_A of the J-K flip-flops.

(v) Vary the input voltage for 0 to –10 V and repeat steps (ii), (iii) and (iv).

APPENDIX-II

ANSWER TO SELECTED PROBLEMS

Chapter-2

2.1. 100 μV
2.3. 10 kΩ, 90 kΩ
2.5. – 10
2.9. 100 μV, 0 V, 0.01 V
2.11. –2.585 V
2.12. 0.1V, 4.9 V
2.15. 137.5 kΩ
2.18. 7.5 mA, 2.5 mA

Chapter-3

3.1. 606 mV
3.2. 0.48 V
3.3. 0.606 V, 5 V

Chapter-4

4.1. $-5V_1 + 2V_2$
4.2. 3 V
4.3. 0.979 V, 2.22 kΩ
4.9. $-1.64\,(t) + 3.24(t - 250) - 1.64\,(t - 500)$
4.10. $-2 \sin 10^4 t - 5\times 10^3 t$
4.11. 20 dB, 16.989 dB
4.15. $\dfrac{0.33 \times 10^7}{s + 1.67 \times 10^6}$

Chapter-5

5.4. 3.836 V, – 3.836 V
5.5 ± 6.9 V
5.7. 5V, ± 5V, 99 kΩ
5.9. 15, 3.73 V, –2.66 V, 0 V
5.12. 11.6 kΩ, 10 kΩ, 5 kΩ, 0.01 μF

Chapter-6

6.1. 25 Ω
6.3. $R_1 = 3R_2$
6.4. $R_{sc} = 8.3\ \Omega$
6.6. $R_1 = 200\ \Omega$
$R_2 = 100\ \Omega$ for $I_L = 50$ mA

Chapter-7

7.2. 5
7.3. 1 kHz, 1.74
7.4. 9
7.6. 1.6 kΩ, for $R_f = R_i = 10$ kΩ; $C = 0.1$ μF
7.7. 2050 Hz, 1950 Hz
7.10. (a) $\frac{1}{RCs+1}$; (b) $\frac{-s}{s^2+2s+1}$

Chapter-8

8.2. 6.06 kΩ
8.3. 62.1 μs, 46.92 μs, 9.18 kHz, 43%
8.4. 0.1 μF, 108.75 kΩ, 72.5 kΩ
8.5. 0.1 μF, $R_A = R_B = 725\ \Omega$

Chapter-9

9.1. 653.6 kHz
9.2. −0.1 V
9.3. 2.5 V
9.4. 2500 Hz, ±812.5 Hz, ±59.95 Hz
9.5. ±275.6 Hz

Chapter-10

10.1. 4, 33.33% of full scale
10.2. 6.9 V
10.3. 0.102
10.4. − 3.33 V, − 1.66 V, − 0.82 V, − 0.39 V, − 0.156 V
10.7. 512, 0.0254 V
10.10. 2 μs
10.11. 0.629 μF
10.12. 101000100001100001