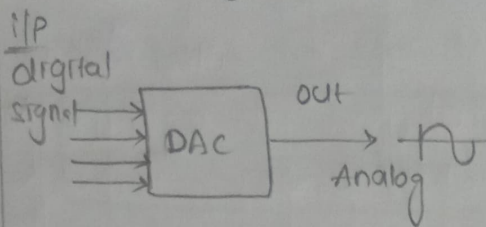


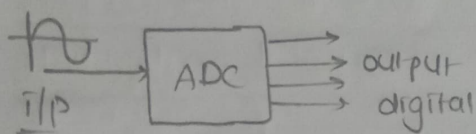
21/7/22
Thursday

CONVERTERS

DAC & ADC Conversion:-

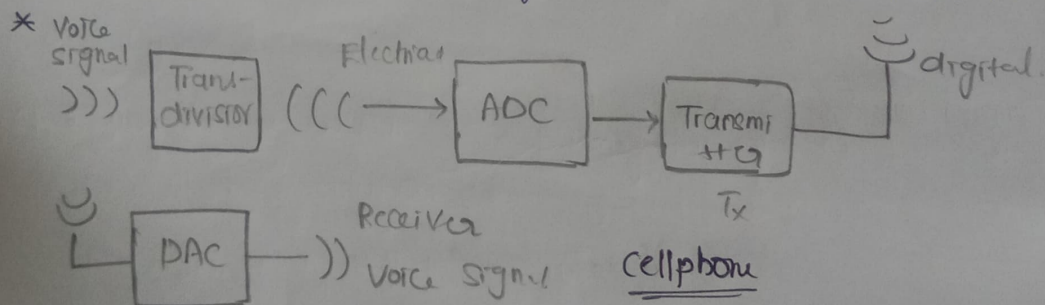


ADC
Eg- Keyboard information to system binary data requires ADC.



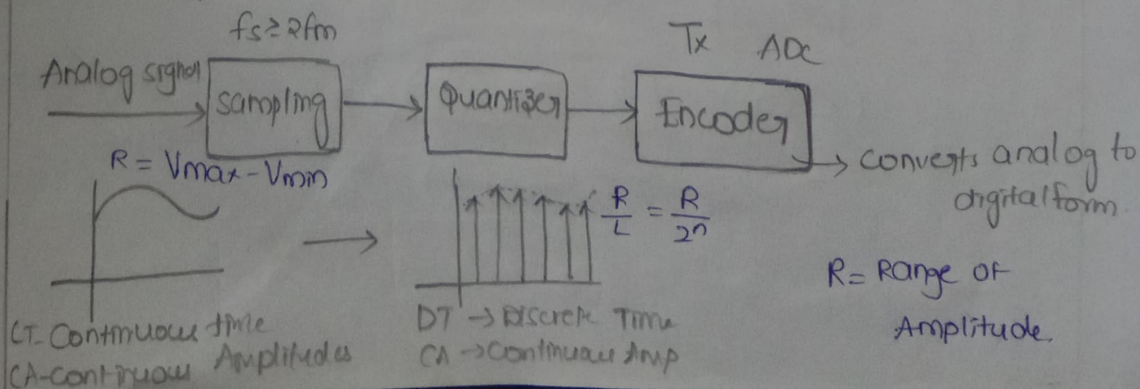
DAC
Eg- system binary data to monitor display requires DAC

- ⇒ physical parameter [Temperature, pressure, velocity, etc] to a transducer and converts into electrical.
- ⇒ These converters are also used in industries.
- ⇒ Another Application is music [ADC].
- ⇒ In Analog noise is more and it is difficult to process and it is difficult to store analog data.
Hence Analog $\xrightarrow{\text{convert}}$ to digital.
Because digital data is easily processed and the noise is less.



⇒ In digital communication.

PCM: pulse code modulation.



- * Any continuous signal converts into samples $\rightarrow$ sampling discrete time signal
- * At receiver, we can reconstruct the original signal with minimum distortion $\rightarrow$ sampling

$$\therefore f_s \geq 2f_m$$

- * $f_s = 2f_m \rightarrow$ Nyquist sampling
- * $f_s \geq 2f_m \rightarrow$ ~~excess~~ sampling (over)
- * $f_s < 2f_m \rightarrow$ under sampling, which leads to distortion called

$\Rightarrow$ Quantizer:- Quantizer which converts the infinite ^{samples with} amplitude levels to finite Amplitude levels.

Eg:-

$$\begin{array}{lcl} 0.1V & \xrightarrow{-0.1} & 0V \\ 0.9V & \xrightarrow{+0.1} & 1V \\ 1.1V & \xrightarrow{-0.1} & 1V \\ 1.7V & \xrightarrow{-0.2} & 1.5V \\ \vdots & & \end{array}$$

Approximate values of Quantizer

$$\begin{array}{lcl} & +0.25 & 2V \\ 1.75 & \xrightarrow{\quad} & \\ & -0.25 & 1.5V \end{array}$$

After Quantization

$$-\frac{0.5}{2} \text{ to } +\frac{0.5}{2}$$

Here step size is 0.5

Analog i/p by Quantization	0.5	$\rightarrow$	000
	1	$\rightarrow$	001
	1.5	$\rightarrow$	010
	2.0	$\rightarrow$	011
	2.5	$\rightarrow$	"
	3.0	$\rightarrow$	"
	3.5	$\rightarrow$	"

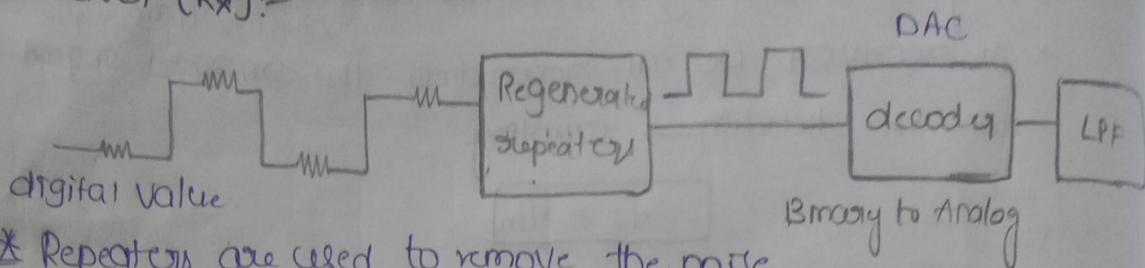
digital
form

$\Rightarrow$ Drawback of Quantizer:-

Here we get Quantization noise

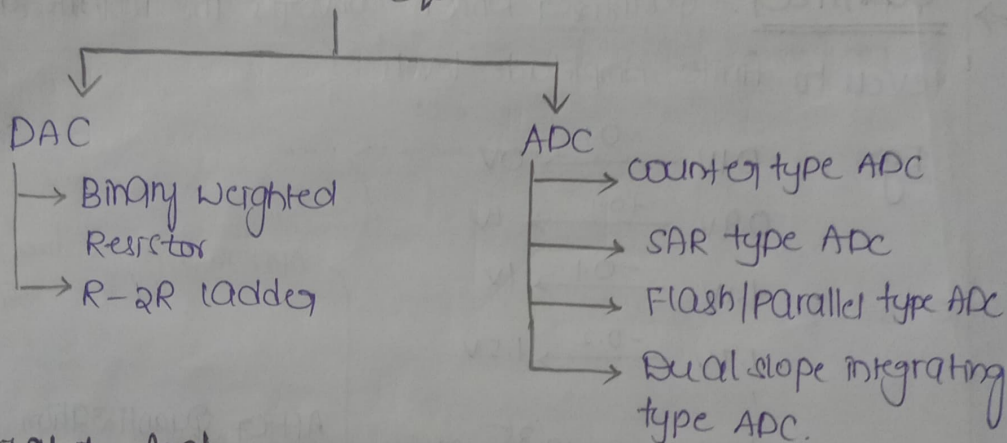
$$-\frac{\delta}{2} \text{ to } +\frac{\delta}{2} \text{ where } \delta = \text{step size}$$

2> Receiver [R_x]:-



- * Repeaters are used to remove the noise
- * Decoders are used to convert binary data to analog form.
- * LPF → with help of LPF we can get original signal with minimum distortion.

converters



⇒ Digital to Analog conversion:-

* DAC: characteristics

1> Resolution:-

changing Analog output corresponding to one (1) LSB, at the input called "Resolution", (R)

Range of Amplitude

$$R = V_{max} - V_{min}$$

Let channel in output is 4V

$$4V \Rightarrow 2^2$$

00	→ 1V	Here Resolution = 1V 1LSB increment
01	→ 2V	
10	→ 3V	
11	→ 4V	

$$R = \frac{V_{ref}}{2^n - 1}$$

⇒ Reference Voltage at logic 1 = V_{ref}
Input

n = no. of bits.

Eg:- $V_{ref} = 10V$
 $n = 4$

$$R = \frac{V_{ref}}{2^n - 1} = \frac{10}{2^4 - 1} = \frac{10}{16 - 1}$$

$$\therefore R = \frac{10}{15}$$

2) Analog output:-

⇒ Analog output resolution is multiplied with decimal equivalent of binary data.

Analog o/p = $R \times$ decimal eq. no. of binary data.

$$\text{Analog o/p} = \frac{V_{ref}}{2^n - 1} \times \sum_{i=0}^{n-1} 2^i b_i$$

↳ binary data.

Let binary data = 0101

decimal = 5

$$\therefore \text{Analog o/p} = \frac{10}{15} \times 5$$

3) Full scale Voltage:-

It is resolution is multiplied with maximum analog output.

$$V_{FS} = R \times \text{max. Analog output.}$$

$$= \frac{V_{ref}}{2^n - 1} \times 2^n - 1$$

$$\boxed{V_{FS} = V_{ref}}^{**}$$

4) Error / Accuracy:-

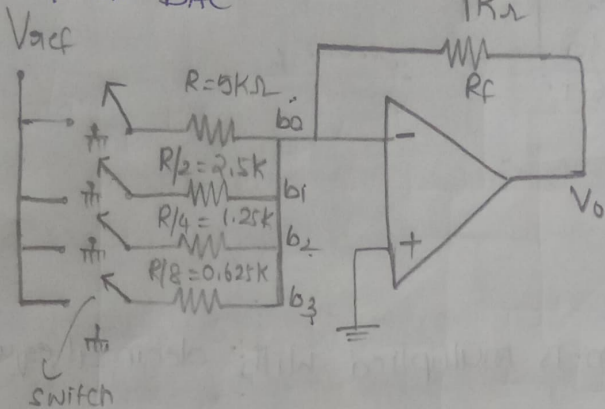
Here error must be always less than resolution.

$$\boxed{\text{Error} < R}$$

*Accuracy is nothing but maximum difference between actual output and theoretical output.

1. Binary Weighted Resistor (DAC):-

4-bit DAC

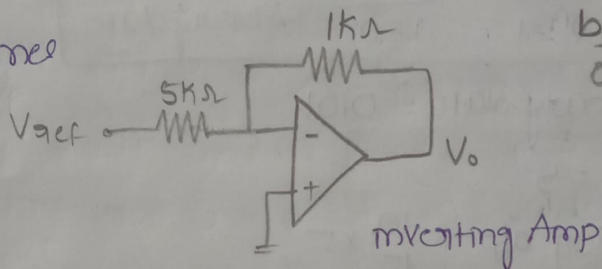


operation:-

1) When $b_0 = 1$ & $b_1 = b_2 = b_3 = 0$

i.e. b_0 is common to V_{ref} and b_1, b_2, b_3 connected to ground.

then CRT becomes



$b_3 \ b_2 \ b_1 \ b_0$
0 0 0 1 $\rightarrow -1V$

Let

$V_{ref} = 5V$,

$$\therefore V_o = -\frac{R_f}{R} V_i$$

$$= -\frac{1K}{5K} \times 5$$

$$\boxed{V_o = -1V}$$

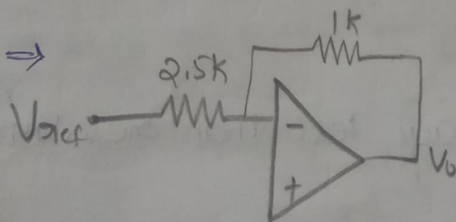
2) When $b_1 = 1$ & $b_0 = b_2 = b_3 = 0$

$b_3 \ b_2 \ b_1 \ b_0$

i.e. $b_1 = V_{ref}$ & $b_0, b_2, b_3 \rightarrow$ ground.

0 0 1 0 $\rightarrow -2V$

CRT $\Rightarrow$



$$\therefore V_o = -\frac{1K}{2.5K} \times 5 = -2V$$

$$\boxed{\therefore V_o = -2V}$$

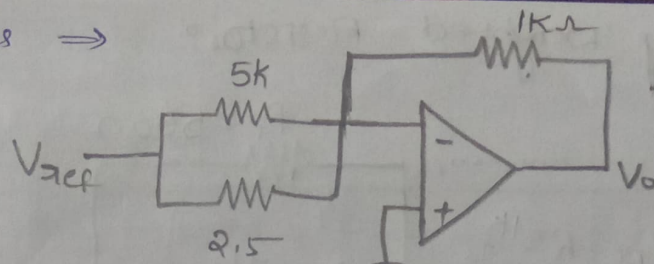
3) When $b_0 = b_1 = 1$ & $b_2 = b_3 = 0$

$b_3 \ b_2 \ b_1 \ b_0$

i.e. b_0 & $b_1 \Rightarrow V_{ref}$, & $b_2, b_3 \rightarrow$ ground.

0 0 1 1 $\rightarrow -3V$

CKI becomes $\Rightarrow$



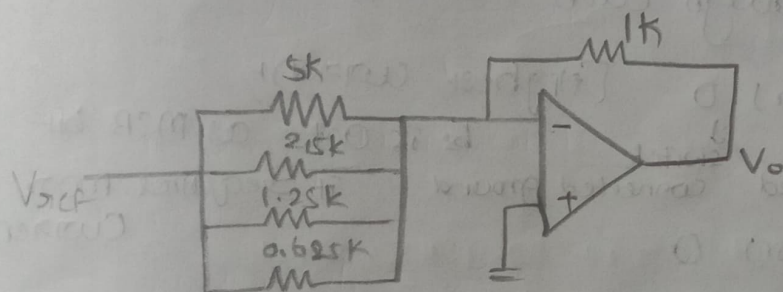
$$R_{eq} = 1.6K$$

$$V_o = -\frac{R_f}{R} \times V_i = -\frac{1K}{1.6K} \times 5$$

$$\therefore V_o = -3V$$

4) When $b_3 = b_2 = b_1 = b_0 = 1$

i.e. $b_3, b_2, b_1, b_0 \Rightarrow V_{ref}$



$$\frac{1}{R_{eq}} = \frac{1}{5K} + \frac{1}{2.5K} + \frac{1}{1.25K} + \frac{1}{0.625K} = \frac{3}{1K}$$

$$R_{eq} = 0.3K$$

$$\therefore V_o = -\frac{R_f}{R} \cdot V_{ref}$$

$$= -\frac{1K}{0.3K} \cdot 5V$$

$$\therefore V_o = -16.67V$$

b_3	b_2	b_1	b_0	
0	0	1	1	$\rightarrow -3V$
0	1	0	0	$\rightarrow -4V$
0	1	0	1	$\rightarrow -5V$
0	1	1	0	$\rightarrow -6V$
0	1	1	1	$\rightarrow -7V$
1	0	0	0	$\rightarrow -8V$
1	0	0	1	$\rightarrow -9V$
1	0	1	0	$\rightarrow -10V$
1	0	1	1	$\rightarrow -11V$
1	1	0	0	$\rightarrow -12V$
1	1	0	1	$\rightarrow -13V$
1	1	1	0	$\rightarrow -14V$
1	1	1	1	$\rightarrow -15V$

but we get
-16.67V

Hence less
Accuracy

* Drawbacks

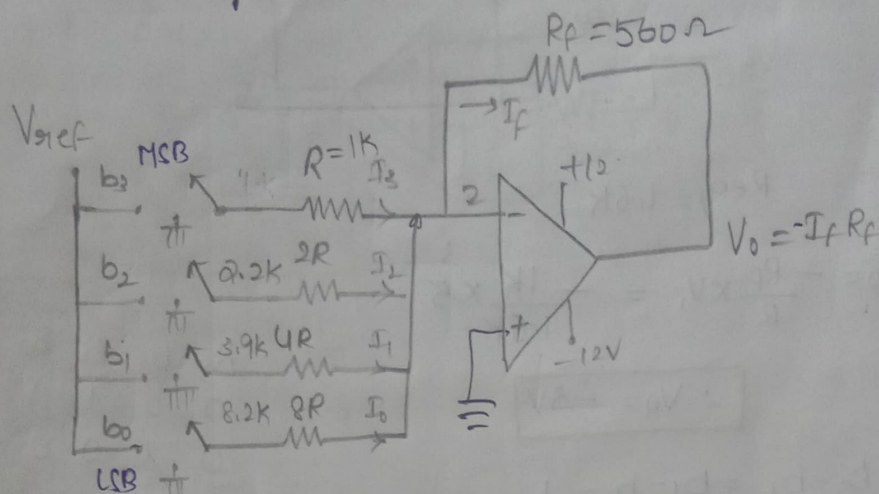
$\Rightarrow$ All the resistors are difficult to design as the no. of bits increases.

$\Rightarrow$ less Accuracy

$\Rightarrow$ To overcome this drawbacks, we go for R-2R ladder.

27/7/22
Wednes
day

4-bit Binary Weighted Resistor



V_{ref} is at logic High-1
Current passing through each terminal

$$I_3 = \frac{V_{ref}}{R} \quad (\text{or}) \quad 0 \quad \begin{array}{l} \text{[Highest current]} \\ \text{switch connected } V_{ref} \end{array} \quad \begin{array}{l} b_3 \text{ acts as MSB bit} \\ \text{it requires more current} \end{array}$$

$$I_2 = \frac{V_{ref}}{2R} \quad (\text{or}) \quad 0$$

$$I_1 = \frac{V_{ref}}{4R} \quad (\text{or}) \quad 0$$

$$I_0 = \frac{V_{ref}}{8R} \quad (\text{or}) \quad 0$$

Apply KCL @ '2' node

$$I_f = I_3 + I_2 + I_1 + I_0$$

from circuit $V_o = -I_f R_f$

$$\Rightarrow \text{LSB Resistance} = \text{MSB} \times 2^{n-1} \quad (\text{where } n = \text{no. of bits})$$

Here $n=4$

$$= R \times 2^{4-1} \quad (\because \text{MSB Resistance} = R)$$

$$\boxed{\text{LSB Resistance} = 8R}$$

$$I_f = \frac{V_{ref}}{R} + \frac{V_{ref}}{2R} + \frac{V_{ref}}{4R} + \frac{V_{ref}}{8R}$$

$$I_f = V_{ref} \left[\frac{1}{R} + \frac{1}{2R} + \frac{1}{4R} + \frac{1}{8R} \right]$$

$$= \frac{V_{ref}}{R} \left[1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8} \right]$$

$$I_f = \frac{V_{ref}}{R} \left[b_3 + \frac{b_2}{2} + \frac{b_1}{4} + \frac{b_0}{8} \right]$$

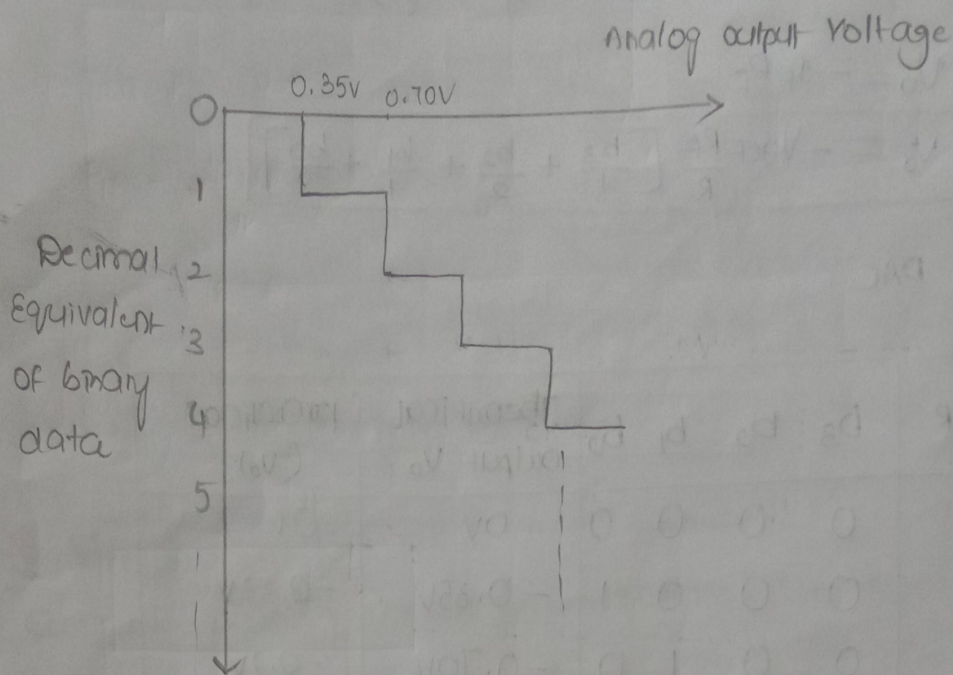
$$\Rightarrow V_o = -I_f R_f$$

$$V_o = -V_{ref} \frac{R_f}{R} \left[\frac{b_3}{1} + \frac{b_2}{2} + \frac{b_1}{4} + \frac{b_0}{8} \right]$$

4 bit DAC

S.R	b_3	b_2	b_1	b_0	Theoretical output V_o	practical (V_o)
	0	0	0	0	0V	0V
	0	0	0	1	-0.35V	-0.33V
	0	0	1	0	-0.70V	-0.7V
	0	0	1	1	-1.05V	-1.05V
	0	1	0	0	-1.40V	-1.28V
	0	1	0	1	-1.75V	-1.64V
	0	1	1	0	-2.10V	-2.0V
	0	1	1	1	-2.45V	-2.35V
	1	0	0	0	-2.8V	-2.84V
	1	0	0	1	-3.15V	-3.18V
	1	0	1	0	-3.5V	-3.55V
	1	0	1	1	-3.85V	-3.90V
	1	1	0	0	-4.2V	-4.13V
	1	1	0	1	-4.55V	-4.48V
	1	1	1	0	-4.9V	-4.8V
	1	1	1	1	-5.25V	-5.19V
	1	1	1	1		

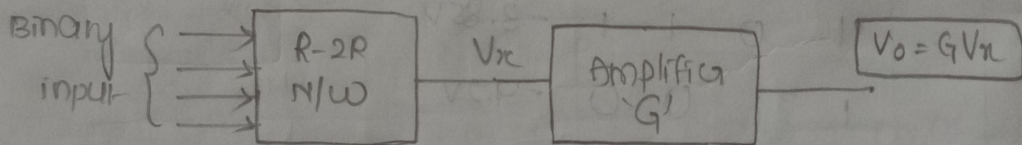
Transfer characteristics:-



Disadvantage

- 1) Less Accuracy
- 2) 'R' resistors having different tolerance values. so it is difficult to design the resistor values.
- 3) Hence to overcome this, we go for R-2R ladder [To improve accuracy].

R-2R ladder DAC:-



⇒ We know that analog voltage $V_x = R_x$ decimal eq. of binary input

$$\Rightarrow V_x = \frac{V_{ref}}{2^n} \times \left(\sum_{i=0}^{n-1} b_i 2^i \right) \text{ for } n\text{-bit}$$

⇒ This V_x is given to amplifier, then

$$\therefore V_o = GV_x \quad \text{Where } G = \text{Gain of Amp}$$

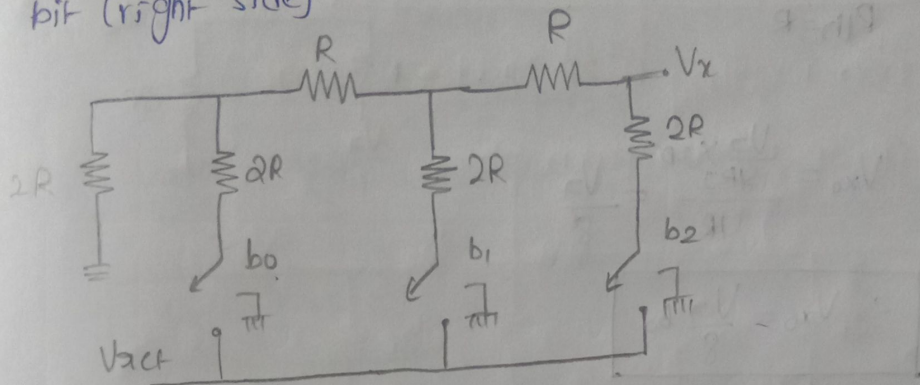
$$\therefore V_o = \left(\frac{V_{ref}}{2^n} \times \sum_{i=0}^{n-1} b_i 2^i \right) \times G$$

Eg: If inverting Amp is used, $G = -\frac{R_f}{R}$

$\Rightarrow$ for non-inverting Amp, $G = 1 + \frac{R_f}{R}$

3-bit R-2R Network

$\Rightarrow$ If 2R is connected to ground, then the adjacent bit is LSB bit (right side)



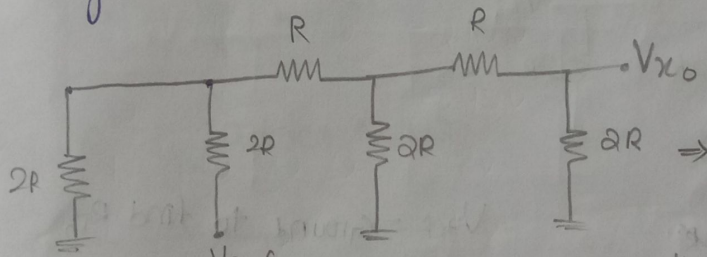
To find ' V_x ' using superposition theorem.

Case (i):

If b_0 connected to V_{ref}

$b_0 = V_{ref}$ (Activated)

similarly, $b_1 = b_2 = \text{ground}$ (deactivated)



By using Thevenin's Theorem, Thevenin's ckt is replaced in the position.

$$V_{th} = \frac{V_{ref} \cdot 2R}{2R + 2R} = \frac{V_{ref} \cdot 2R}{4R}$$

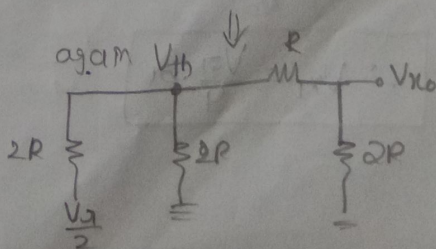
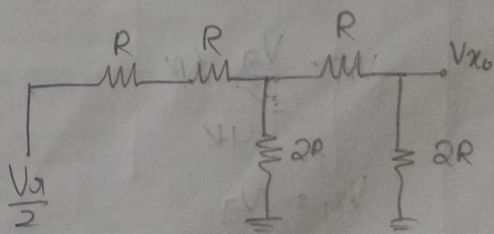
$$V_{th} = \frac{V_{ref}}{2}$$

$$R_{th} = \frac{2R \times 2R}{2R + 2R} = R$$

$$R_{th} = R$$

Again

$$V_{th} = \frac{\frac{V_{ref}}{2} \cdot 2R}{2R + 2R} = \frac{\frac{V_{ref}}{2} \cdot 2R}{4R}$$



$$V_{th} = \frac{V_0}{4}$$

To find R_{th} $\frac{V_0}{2} \rightarrow$ Ground

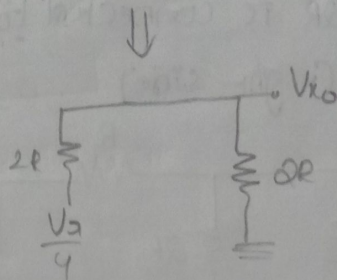
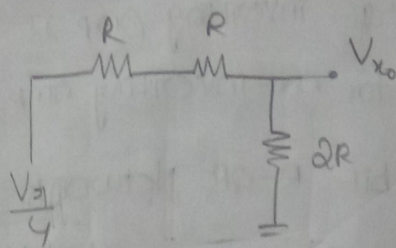
$$R_{th} = \frac{2R \times 2R}{4R} = R$$

$$R_{th} = R$$

Again,

$$V_{x0} = \frac{\frac{V_0}{4} \times 2R}{4R + 2R} = \frac{V_0}{8}$$

$$\therefore V_{x0} = \frac{V_0}{8} b_0$$



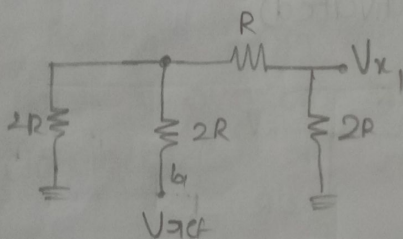
Case (ii)

If b_1 connected to V_{ref}

$b_1 = V_{ref}$, $b_2 = b_0 =$ Ground

from original circuit

(Here $2R \parallel 2R = R$
and $R + R = 2R$ series)



$$V_{th} = \frac{V_{ref} \cdot 2R}{4R + 2R}$$

$$V_{th} = \frac{V_{ref}}{2}$$

$V_{ref} =$ Ground to find R_{th}

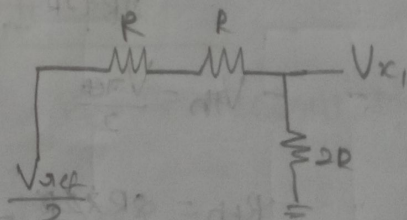
$$R_{th} = \frac{2R \times 2R}{4R} = R$$

$$R_{th} = R$$

$$V_{x1} = \frac{V_0}{2} \cdot \frac{2R}{4R}$$

$$V_{x1} = \frac{V_0}{4}$$

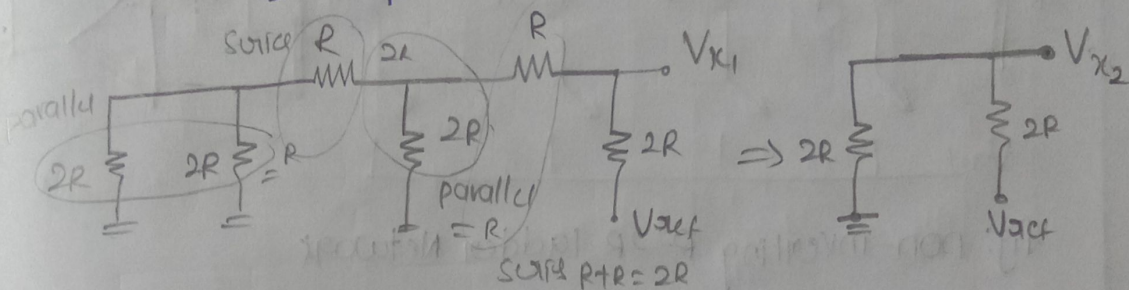
$$\therefore V_{x1} = \frac{V_0}{4} \cdot b_1$$



case-3

If b_2 connected to V_{ref}

$b_2 = V_{ref}$ $b_0 = b_1 = \text{Ground}$



$$V_{x2} = \frac{V_{ref} \cdot 2R}{4R} = \frac{V_{ref}}{2}$$

$$\therefore V_{x2} = \frac{V_{ref} \cdot b_2}{2}$$

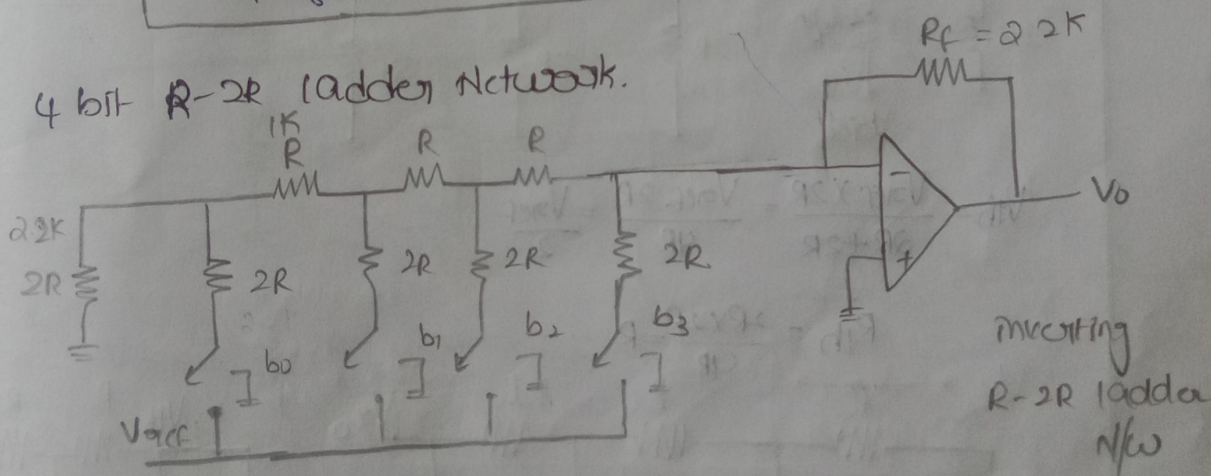
Total Response,

$$V_x = V_{x0} + V_{x1} + V_{x2}$$

$$V_x = \frac{V_g b_0}{8} + \frac{V_g b_1}{4} + \frac{V_g b_2}{2}$$

$$V_x = \frac{V_g}{8} [b_0 + 2b_1 + 4b_2]$$

* 4 bit R-2R ladder Network.



$$\therefore V_x = \frac{V_g}{2^4} [b_0 + 2b_1 + 4b_2 + 8b_3]$$

$V_{ref} = 5$

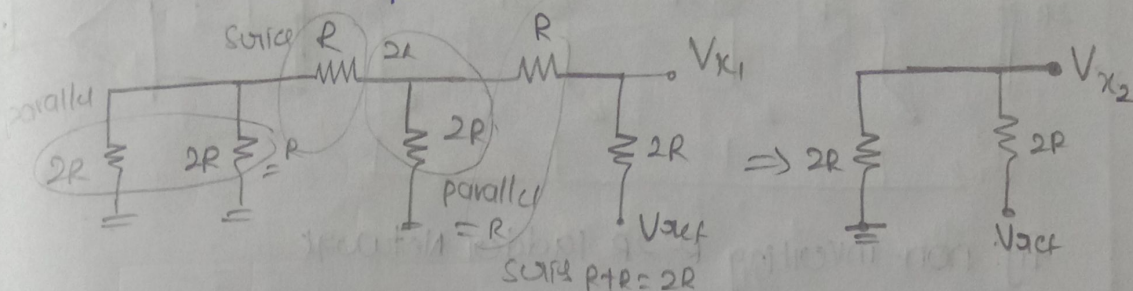
for n-bit R-2R ladder Network

$$V_x = \frac{V_g}{2^n} \left[\sum_{i=0}^{n-1} b_i 2^i \right]$$

case-3

If b_2 connected to V_{ref}

$$b_2 = V_{ref} \quad b_0 = b_1 = \text{Ground.}$$



$$V_{x2} = \frac{V_{ref} \cdot 2R}{4R} = \frac{V_{ref}}{2}$$

$$\therefore V_{x2} = \frac{V_{ref} \cdot b_2}{2}$$

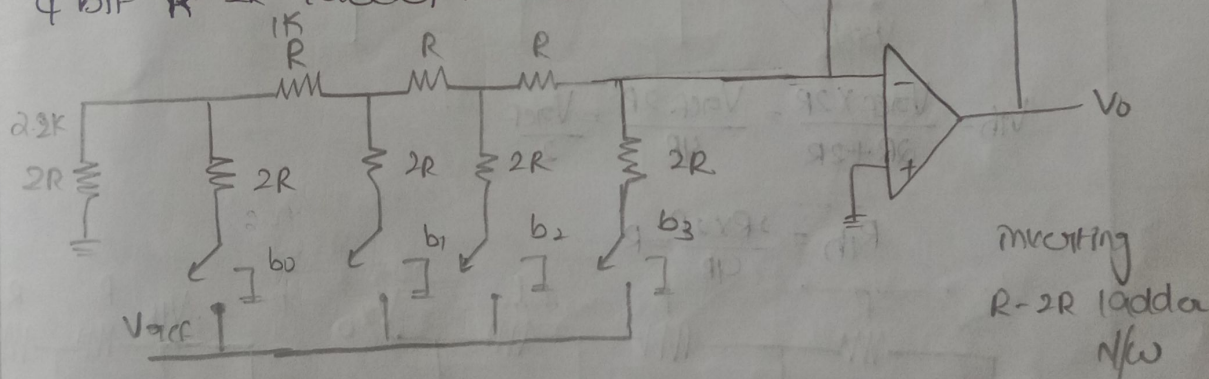
Total Response,

$$V_x = V_{x0} + V_{x1} + V_{x2}$$

$$V_x = \frac{V_{ref}}{8} b_0 + \frac{V_{ref}}{4} b_1 + \frac{V_{ref}}{2} b_2$$

$$V_x = \frac{V_{ref}}{8} [b_0 + 2b_1 + 4b_2]$$

* 4 bit R-2R ladder Network.



$$\therefore V_x = \frac{V_{ref}}{2^4} [b_0 + 2b_1 + 4b_2 + 8b_3]$$

$$V_{ref} = 5$$

for n-bit R-2R ladder Network

$$V_x = \frac{V_{ref}}{2^n} \left[\sum_{i=0}^{n-1} b_i 2^i \right]$$

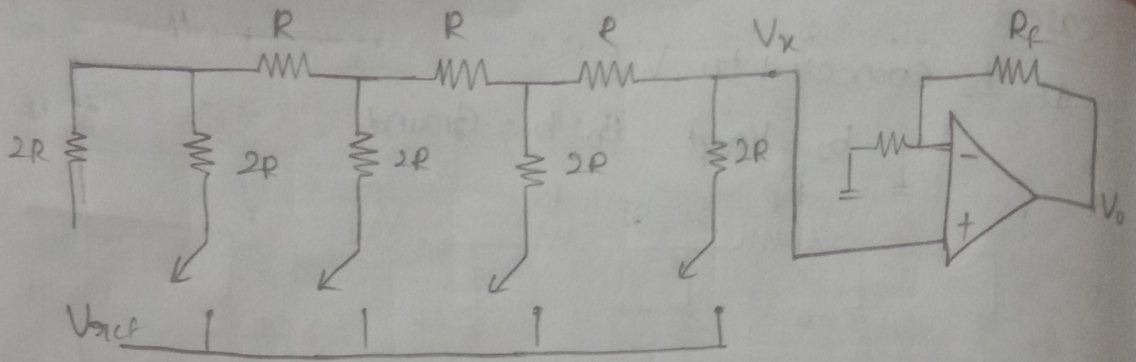
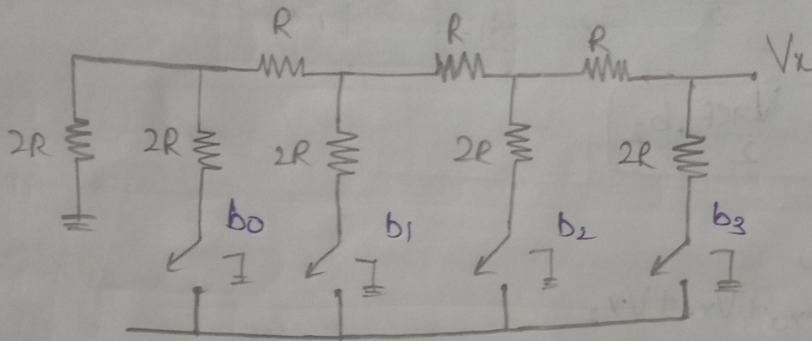
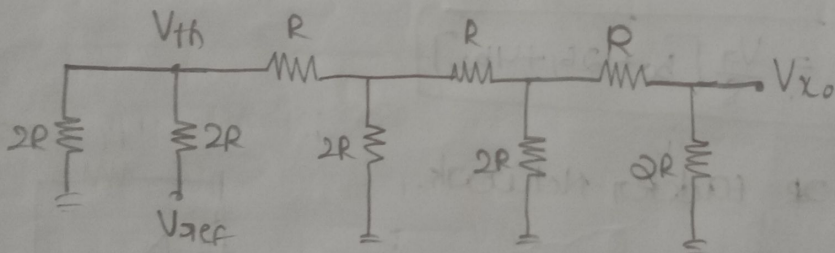


fig: non-inverting R-2R ladder Network

* 4-bit R-2R ladder network:-

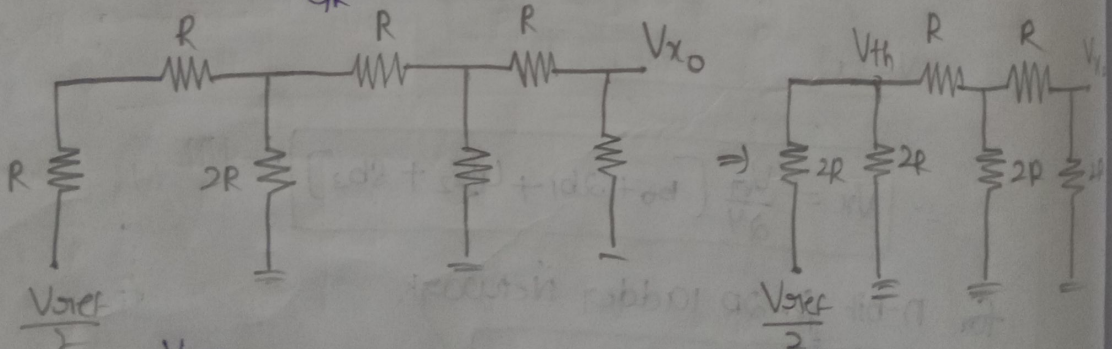


Case (i):- $b_0 = V_{ref}$ and $b_1 = b_2 = b_3 = \text{ground}$

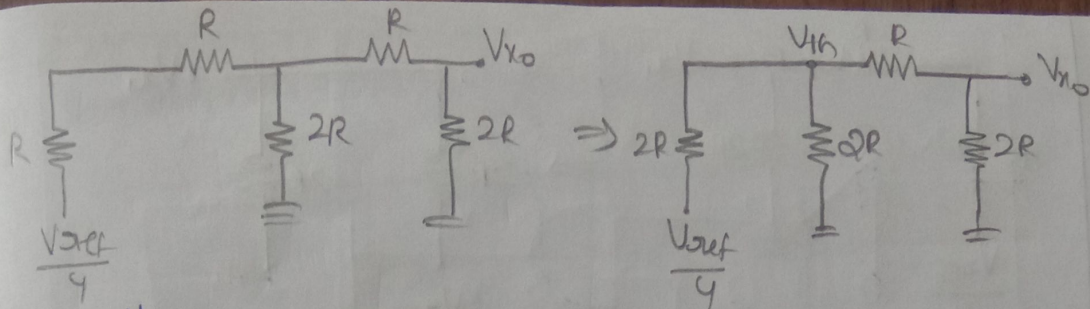


$$V_{th} = \frac{V_{ref} \times 2R}{2R + 2R} = \frac{V_{ref} \cdot 2R}{4R} = \frac{V_{ref}}{2}$$

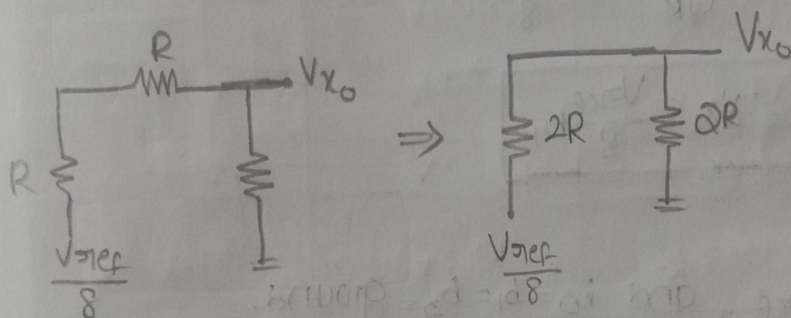
$$R_{th} = \frac{2R \times 2R}{4R} = R$$



$$V_{th} = \frac{\frac{V_{ref}}{2} \times 2R}{4R} = \frac{V_{ref}}{4}, \quad R_{th} = \frac{2R \times 2R}{4R} = R$$



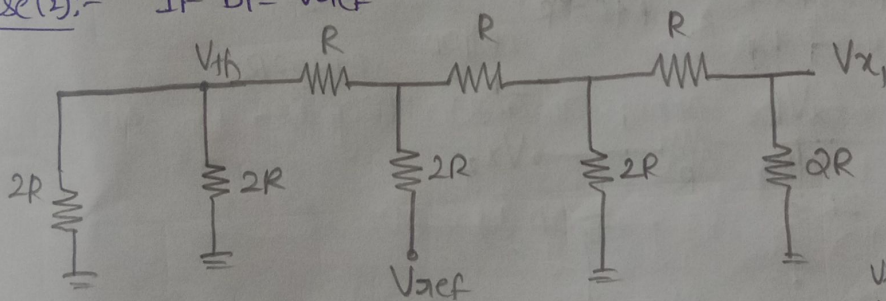
$$V_{th} = \frac{\frac{V_{ref}}{4} \times 2R}{4R} = \frac{V_{ref}}{8} ; R_{th} = \frac{2R \times 2R}{4R} = R$$



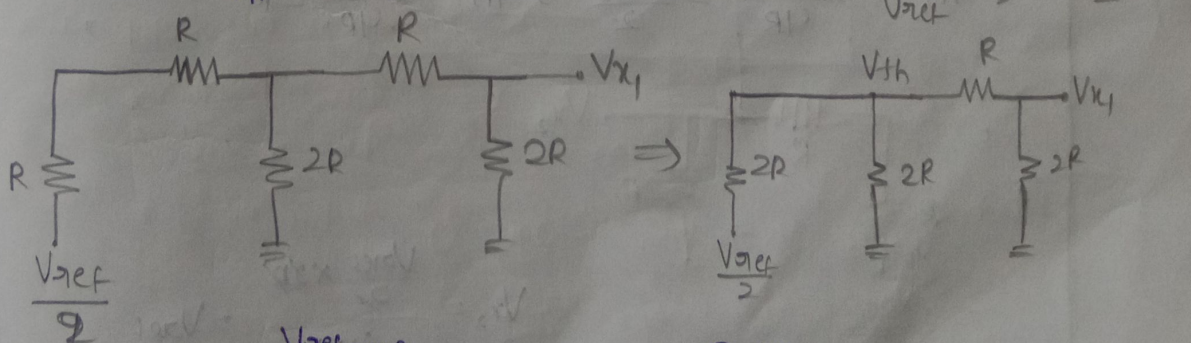
$$V_{x0} = \frac{\frac{V_{ref}}{8} \times 2R}{4R} = \frac{V_{ref}}{16}$$

$$\therefore V_{x0} = \frac{V_{ref}}{16} \quad \times$$

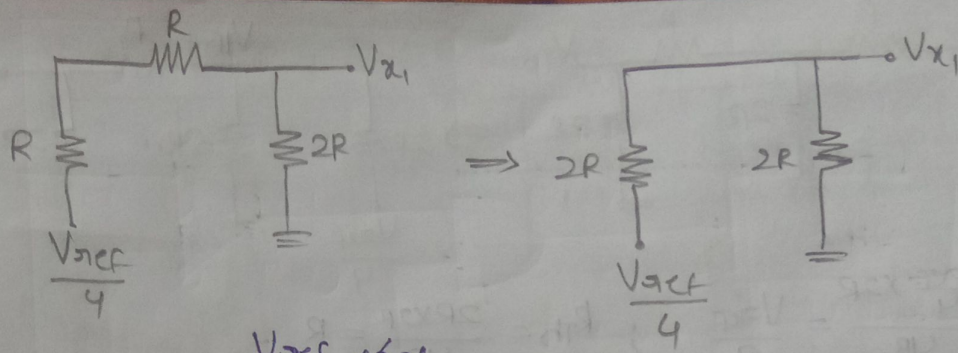
Case (2):- If $b_1 = V_{ref}$ and $b_0 = b_2 = b_3 = \text{ground}$



$$V_{th} = \frac{V_{ref} \cdot 2R}{4R} = \frac{V_{ref}}{2} , R_{th} = \frac{2R \times 2R}{4R} = R$$



$$V_{th} = \frac{\frac{V_{ref}}{2} \times 2R}{4R} = \frac{V_{ref}}{4} , R_{th} = \frac{2R \times 2R}{4R} = R$$

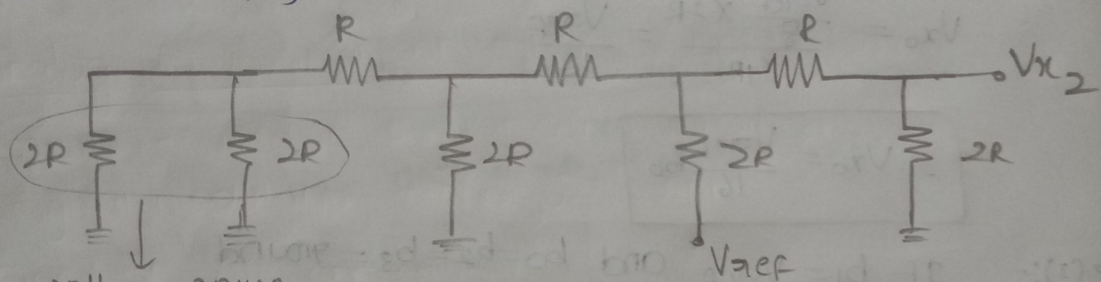


$$V_{x1} = \frac{\frac{V_{ref}}{4} \times 2R}{4R} = \frac{V_{ref}}{8}$$

$$\therefore V_{x1} = \frac{V_{ref}}{8} b_1$$

case (3):-

If $b_2 = V_{ref}$, and $b_0 = b_1 = b_3 = \text{ground}$.

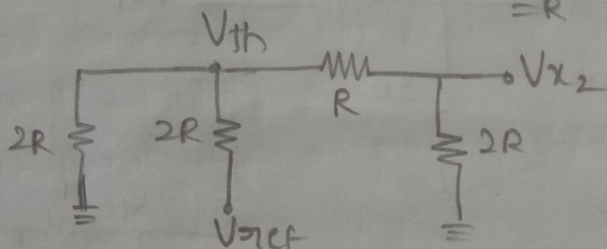


$$2R \parallel 2R = \frac{2R \times 2R}{2R + 2R} = R$$

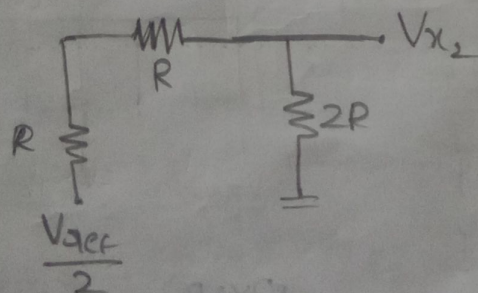
$$R + R = 2R$$

$$2R \parallel 2R = R$$

$$R + R = 2R$$



$$V_{th} = \frac{V_{ref} \cdot 2R}{4R} = \frac{V_{ref}}{2}, \quad R_{th} = \frac{2R \times 2R}{4R} = R$$

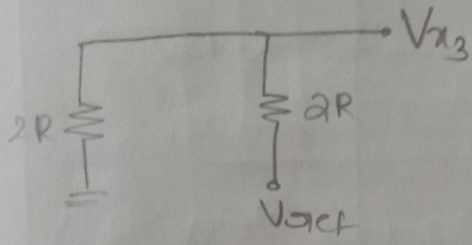
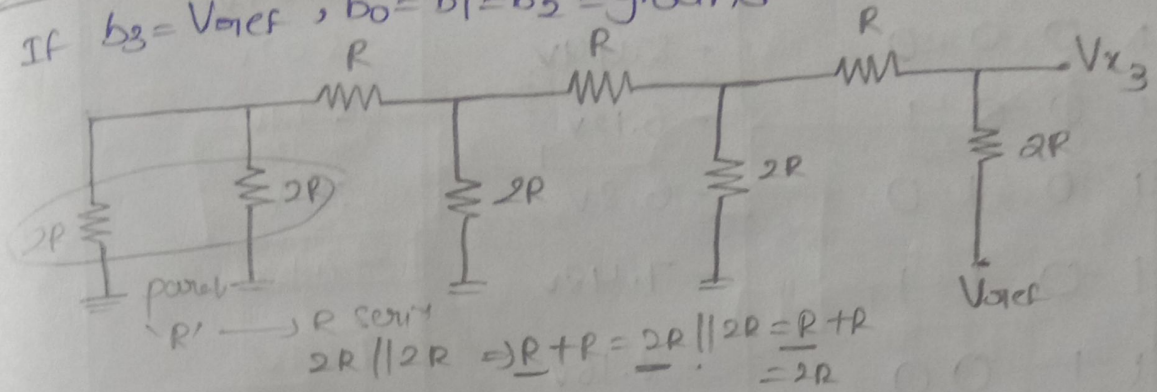


$$V_{x2} = \frac{\frac{V_{ref}}{2} \times 2R}{4R} = \frac{V_{ref}}{4}$$

$$\therefore V_{x2} = \frac{V_{ref}}{4} b_2$$

Case (4):-

If $b_3 = V_{ref}$, $b_0 = b_1 = b_2 = \text{ground}$



$$V_{x3} = \frac{V_{ref} \cdot 2R}{4R} = \frac{V_{ref}}{2}$$

$$\therefore V_{x3} = \frac{V_{ref}}{2} b_3$$

Total response, $V_x = V_{x0} + V_{x1} + V_{x2} + V_{x3}$

$$= \frac{V_{ref}}{16} b_0 + \frac{V_{ref}}{8} b_1 + \frac{V_{ref}}{4} b_2 + \frac{V_{ref}}{2} b_3$$

$$V_x = \frac{V_{ref}}{16} [b_0 + 2b_1 + 4b_2 + 8b_3]$$

$$\therefore V_0 = V_x G$$

$$\therefore V_0 = \frac{V_{ref}}{16} [b_0 + 2b_1 + 4b_2 + 8b_3] \left(-\frac{R_f}{R} \right)$$

Sl.No.	b_3	b_2	b_1	b_0	Theoretical	Practical
	0	0	0	0	0V	0V
	0	0	0	1	-0.68V	-0.7V
	0	0	1	0	-1.36V	-1.36V
	0	0	1	1	-2.04V	-2.07V
	0	1	0	0	-2.72V	-2.61V
	0	1	0	1	-3.4V	-3.32V
	0	1	1	0	-4.08V	-3.98V

0 1 1 1	-4.76V	-4.69V
1 0 0 0	-5.44V	-5.01V
1 0 0 1	-6.12V	-5.79V
1 0 1 0	-6.8V	-6.4V
1 0 1 1	-7.48V	-7.15V
1 1 0 0	-8.16V	-7.69V
1 1 0 1	-8.84V	-8.40V
1 1 1 0	-9.52V	-9.05V
1 1 1 1	-10.2V	-9.76V

28/7/22
Thursday

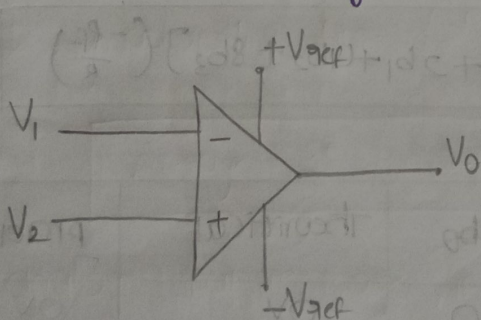
Analog to Digital converters / conversion:-

* ADC is used in Digital communication.

Digital modulation techniques, ADIM

⇒ Types of ADC conversions.

- 1> Counter type ADC
- 2> Successive Approximation Register type ADC
- 3> Flash type ADC
- 4> Dual slope integrating type ADC



comparator compares the two signals.

⇒ single bit comparators

⇒ this is header of these 4 types of ADC.

When

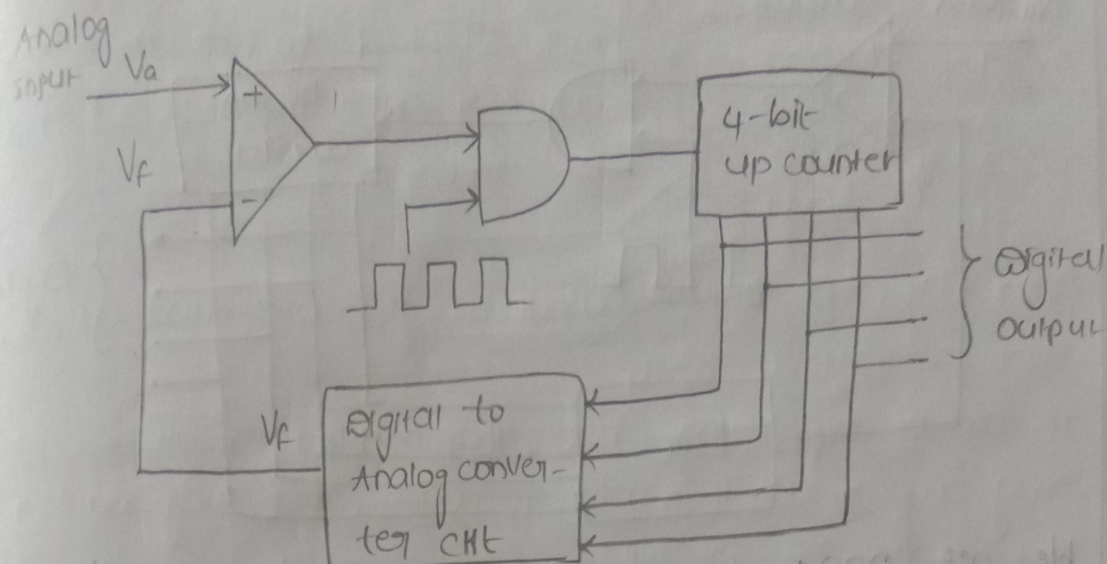
$$V_1 > V_2, V_0 = -V_{ref} = \text{logic } 0$$

$$V_1 < V_2, V_0 = +V_{ref} = \text{logic } 1$$

If $V_1 = V_2$ (decided by designer)

⇒ this is open loop ch

1. Counter type ADC:-



If $V_a > V_f$, comparator output = 1

$V_a < V_f$, comparator output = 0

$V_a = V_f$ (decided by manufacturer)

⇒ comparator compares two inputs, one is Analog input and other is feedback of DAC.

⇒ up counter always require clock with the help of AND-Gate.

⇒ If logic 1 goes to the up-counter

principle of counter:-

counts no. of clock pulse.

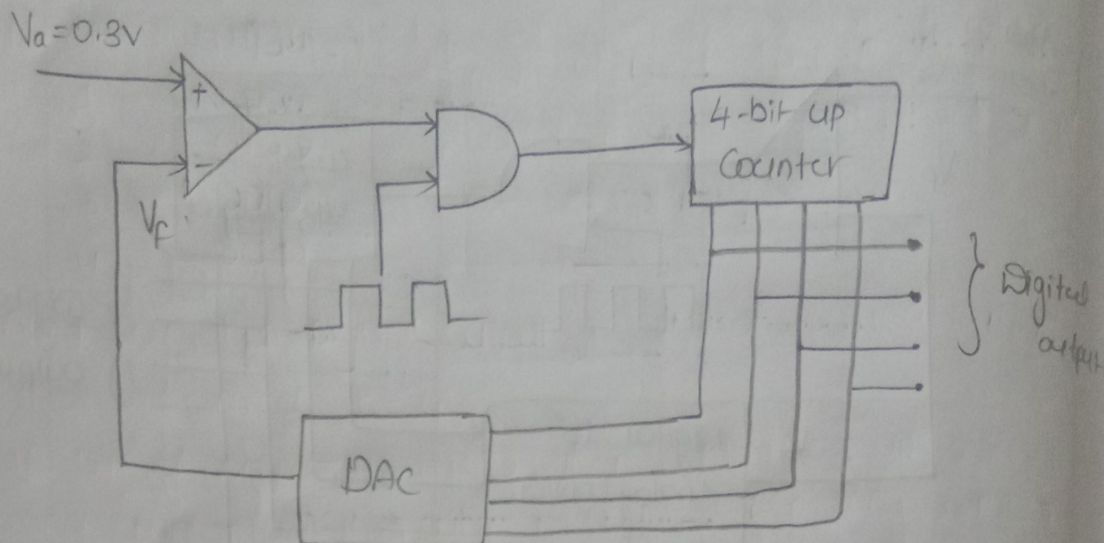
⇒ For logic 0, there is no clock.

⇒ whenever we give clock, then only the counter starts counting and logic 0 [no clock]. Then the counter stops counting.

⇒ After the counter stops counting, we consider the digital output, as final output.

⇒ For new value of Analog input, we need to reset the previous value of counter.

Eg:- Let us take $V_a = 0.3V$



We get 0001 for 0.3V, it requires one clk pulse.

upto 0.9V, it requires one clock pulse, $01p = 0001$

$\Rightarrow$ If input is 1 to 2V, it requires two clk, $01p = 0010$.

input is 2.4V, then 2 clk

input is 2.5V, then 3 clk

input is 9.5V, then 10 clk

$\Rightarrow$ Minimum = $1T_{clk}$

maximum = $(2^n - 1)T_{clk}$

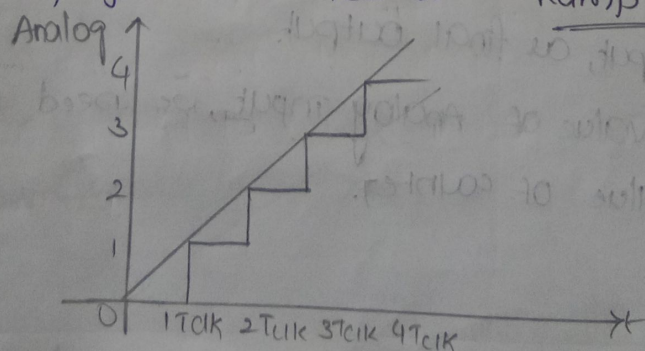
$$\Rightarrow \text{Avg} = \frac{\text{max} + \text{min}}{2} = \frac{(2^n - 1)T_{clk} + T_{clk}}{2}$$

$$* \text{ Avg conversion time} = \left(\frac{2^n - 1 + 1}{2} \right) T_{clk}$$

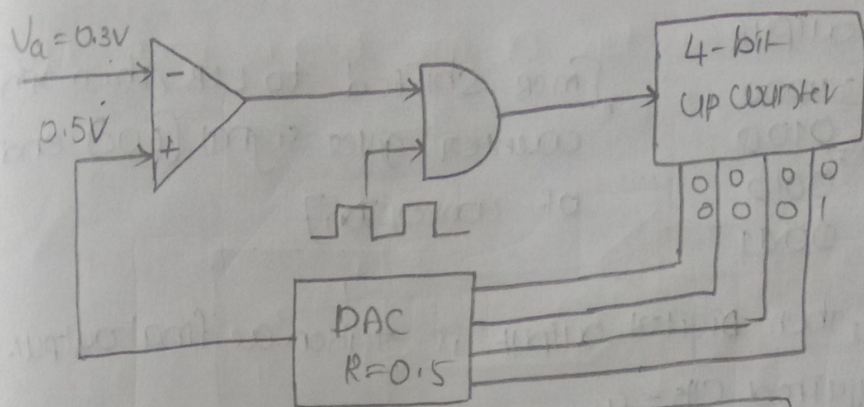
$$\therefore \text{Average} = \frac{2^n}{2} = (2^{n-1}) T_{clk}$$

$\Rightarrow$ When analog input increases, the conversion time also increases.

$\Rightarrow$ This counter type also called as "Ramp type ADC"



Let Resolution $R=0.5$ and $V_a=0.3V$



CLK
If $i/p = 0.3$, 1CLK
 $i/p = 0.8$, 2CLK

We know that $\text{Digital O/p} = \frac{\text{Analog input}}{R}$

$$\therefore \text{Digital output} = \frac{4.5}{0.5} = 9 \text{ [1001]}$$

$$\Rightarrow \text{If } V_a = 6V, \text{ then Digital output} = \frac{6}{0.5} = 12 \text{ [1100]}$$

Drawback:-

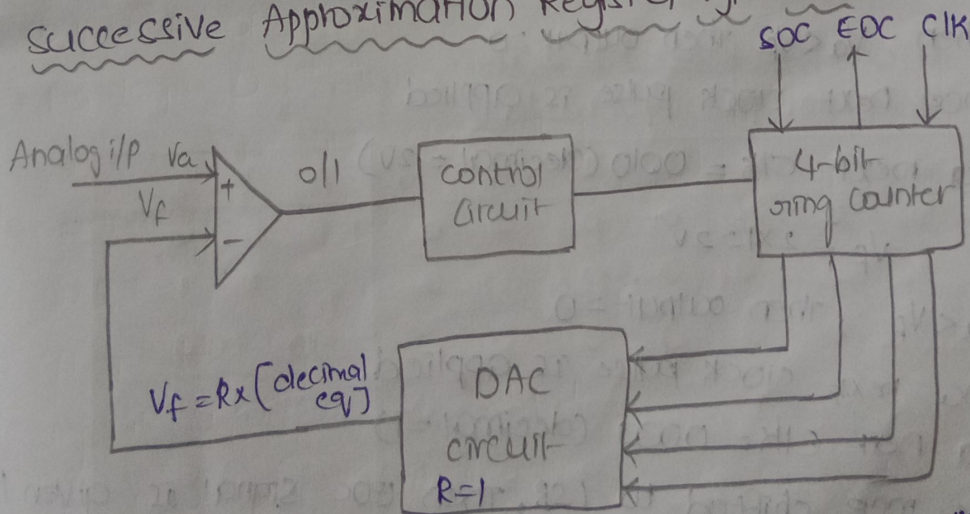
$\Rightarrow$ It is a slowest type ADC.

Because as analog input increases, the conversion time is also increases.

For 5-bit up counter $\rightarrow$ requires 3 CLK pulse.

$\Rightarrow$ For new input, reset the counter first otherwise the counter starts counting from previous count.

2. Successive Approximation Register type ADC:-



$\Rightarrow$ Ring counter is not a self starting counter. So MSB bit should be fixed (set by forcing soc (start of conversion) along with CLK.

4-bit Ring counter

clk	output
1	1000
2	0100
3	0010
4	0001

[msb shifted to LSB, then ring counter gives signal (EOC) end of conversion]

- ⇒ After EOC, then digital output is taken as final output.
- ⇒ here required clk = 4.
- ⇒ If o/p of comparator is 0, then control circuit asks the ring counter whether what it wants, then ring counter asks apply the clk pulse.

$$\begin{array}{r} * \quad 1000 \\ \quad 0100 \\ \hline \quad 0010 \end{array}$$

- ⇒ If o/p of comparator is 1, then control circuit tells ring counter to hold the previous value.

$$\text{output} = 1 \Rightarrow \underline{0011} \text{ (holds 1 as previous).}$$

⇒ operation:-

$$* \text{ Initial } = 0000$$

$$* \text{ After SOC } = 1000 \text{ (decimal } = 8)$$

$$\text{If } V_a = 0.4, V_f = 8 \times 1 = 8V$$

$$\text{Then } V_a < V_f \text{ then output } = 0$$

Hence next clock pulse is applied

$$* \text{ After next clk } = 0010 \text{ (decimal } = 2V)$$

$$V_f = 2 \times 1 = 2V$$

$$V_a < V_f, \text{ then output } = 0$$

Hence next clock pulse is applied.

$$* \text{ After next clk } = 0001 \text{ (decimal } = 1)$$

Here msb shifted to LSB, then EOC signal is given to ring counter.

$$\begin{array}{r} 0000 / x = 0 \\ \hline 1000 \\ \hline 0100 - 4 \times 1 = 4 \\ \hline 0010 - 2 \\ \hline 0001 \end{array}$$

4-bit
4-6

Hence final output = 0001.

If $V_a = 4.7V$

Initial - 0000

SOC - 1000 [8V]

0100 [4V]

Here $4.7 > 4V$ [$V_a > V_f$]

Hence output of amp = 1. Here ring counter holds previous value. - 0110 [6V]

$V_f > V_a \Rightarrow$ 0101 [5V] final output

Here for 4-bit ring counter, required CLK = 4

for n-bit, required clock pulse = n.

maximum $T_{clk} = (2^n - 1) T_{clk}$ for counter-type

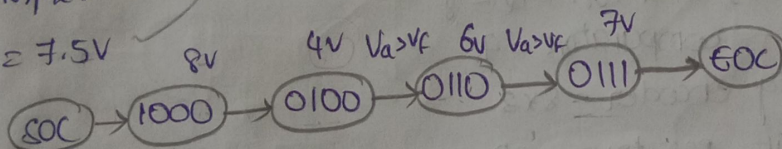
* maximum = n T_{clk}
minimum = 1 T_{clk}

$2^4 - 1 = 16 - 1 = 15$

Hence we can reduce the conversion time is reduced

* Example:-

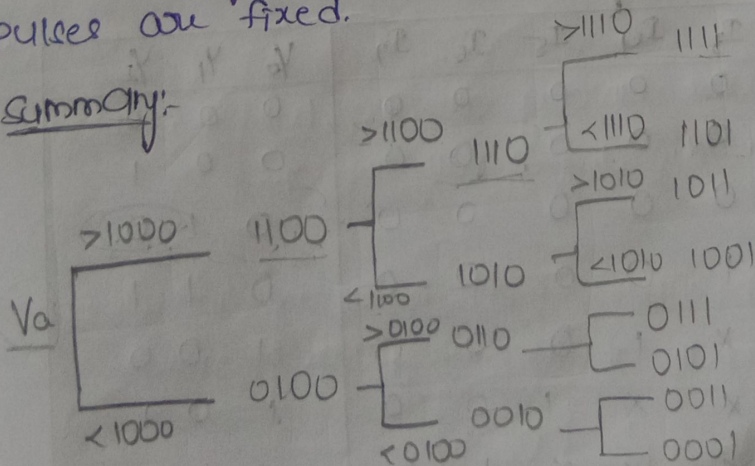
$V_a = 7.5V$



$\therefore O/P = 0111$ (7)

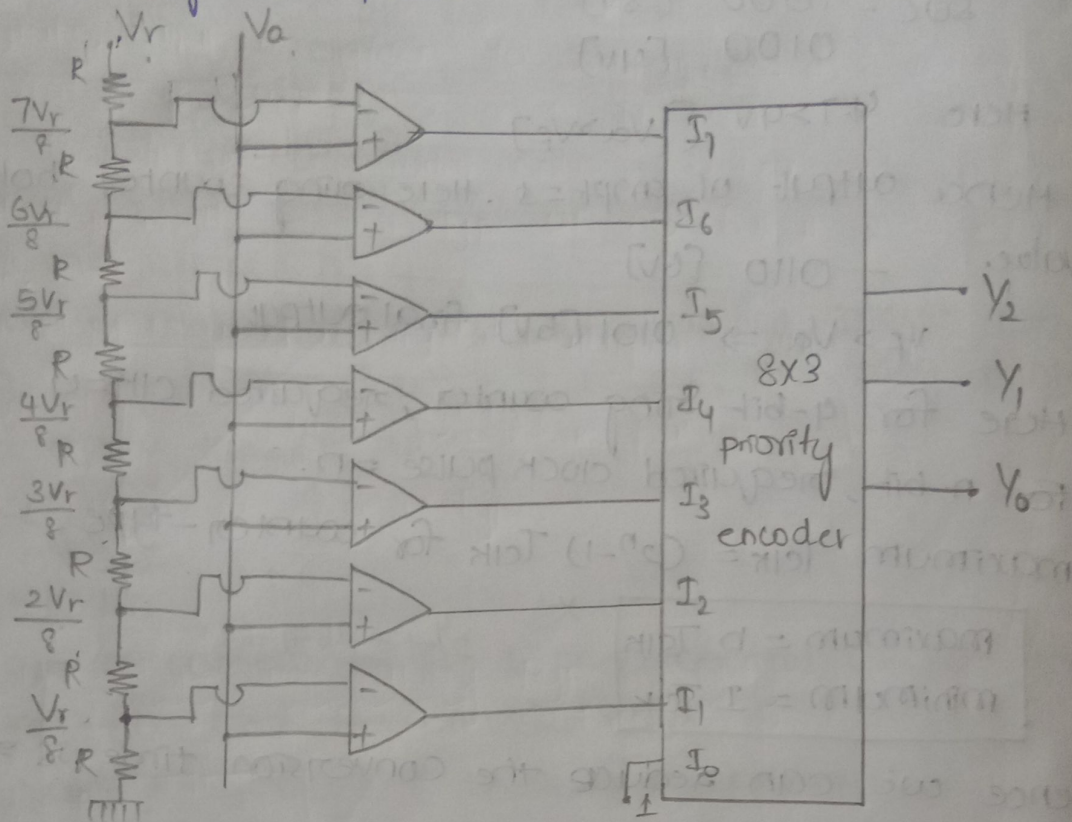
$\Rightarrow$ Here for any Analog input, the required no. of clock pulses are fixed.

* Summary:-



Flash type ADC:

It is the fastest type of ADC because no need to require any clock pulse.



⇒ For 3-bit, Resistors = $2^3 = 8$
comparators = 7

priority encoder = 8x3

⇒ for n-bit, Resistors = 2^n

comparators = $2^n - 1$

priority encoder = $2^n \times n$

Truth Table for priority encoder

I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Y_0	Y_1	Y_2
1	0	0	0	0	0	0	0	0	0	0
x	1	0	0	0	0	0	0	0	0	1
x	x	1	0	0	0	0	0	0	1	0
x	x	x	1	0	0	0	0	0	1	1
x	x	x	x	1	0	0	0	1	0	0
x	x	x	x	x	1	0	0	1	0	1
x	x	x	x	x	x	1	0	1	1	0
x	x	x	x	x	x	x	1	1	1	1

* operation:-

	Y_0	Y_1	Y_2
$V_a \leq \frac{V_r}{8}$	0	0	0
$\frac{V_r}{8} < V_a \leq \frac{2V_r}{8}$	0	0	1
$\frac{2V_r}{8} < V_a \leq \frac{3V_r}{8}$	0	1	0
$\frac{3V_r}{8} < V_a \leq \frac{4V_r}{8}$	0	1	1
$\frac{4V_r}{8} < V_a \leq \frac{5V_r}{8}$	1	0	0
$\frac{5V_r}{8} < V_a \leq \frac{6V_r}{8}$	1	0	1
$\frac{6V_r}{8} < V_a \leq \frac{7V_r}{8}$	1	1	0
$\frac{7V_r}{8} < V_a \leq V_r$	1	1	1

Let $V_a = 0.5V$ & $V_r = 8V$ $0.5 \leq \frac{8}{8} = 1$ Hence o/p is 000

$\Rightarrow$ If $V_a = 1.5V$, $1 < 1.5 \leq 2$ Hence o/p is 001

$\Rightarrow$ If $V_a = 3.5V$, $3 < 3.5 \leq 4$ Hence o/p is 011.

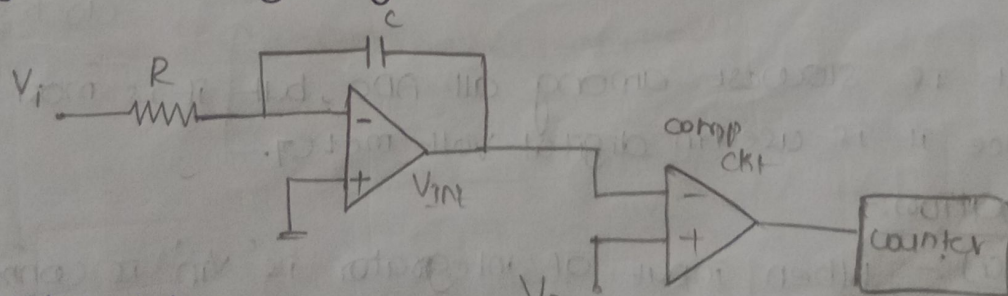
$\Rightarrow$ If $V_a = 6.2V$, $6 < 6.2 \leq 7$ Hence o/p is 110.

Here o/p depends not only on V_a but also on V_r .

* Disadvantage:- It requires more no. of comparators. It requires $(2^n - 1)$ or 2^n comparators. It requires 2^n resistors.

4) Dual slope integrating type of ADC:-

$\Rightarrow$ single slope integrating:

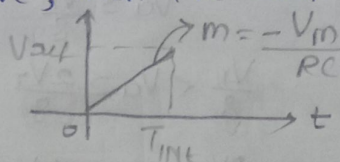


$$\begin{aligned} \text{Integrator output } V_{INT} &= -\frac{1}{RC} \int_0^{V_{INT}} V_{IN} dt \\ &= -\frac{V_{IN}}{RC} \int_0^t dt \end{aligned}$$

$$\therefore V_{INV} = -\frac{V_{IN}}{RC} t$$

Compare with $y=mx$, if $V_m = +V_e$, then $-V_e$ ramp
if $V_m = -V_e$, then $+V_e$ ramp

$$\text{Slope} = m = -\frac{V_m}{RC}$$



⇒ Integrator output is given to comparator. Then the o/p of comparator is given as 0 (or) 1. It controls the counter.
i.e., the o/p of comparator controls counter.

⇒ Dual slope is the slowest type of ADC but it gives accurate value.

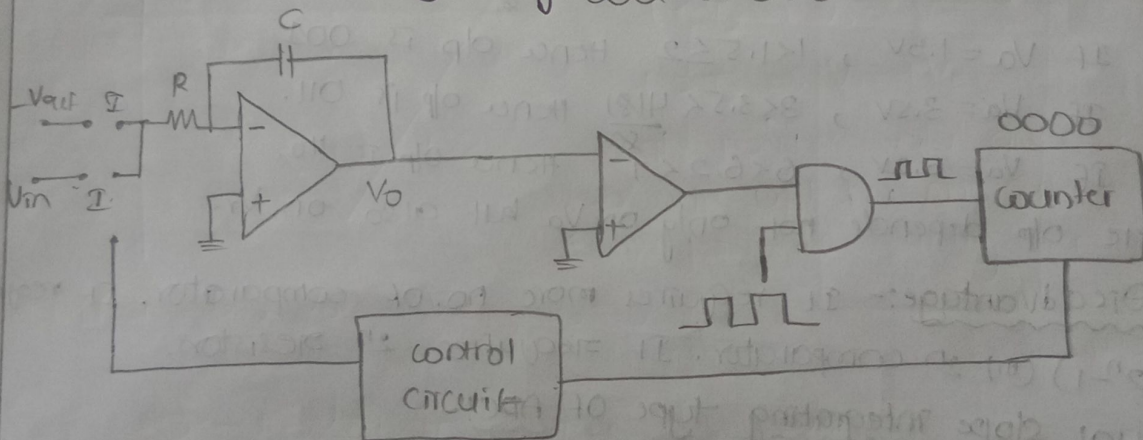
⇒ Dual Slope is used in digital multimeter.

⇒ Dual slope requires $(2^{n+1})T_{clk}$ pulses.

Hence it is a slowest type.

5/8/22
Friday

4> Dual slope Integrating type of ADC:-



Because it requires $(2^{n+1})T_{clk}$ clock pulses.

⇒ It is slowest among all ADC, but it is most accurate.
Hence it is used in digital Volt-meter.

operation:-

Case (i):- When input of integrator is ' V_{in} ' is connected, then the output of the integrator becomes

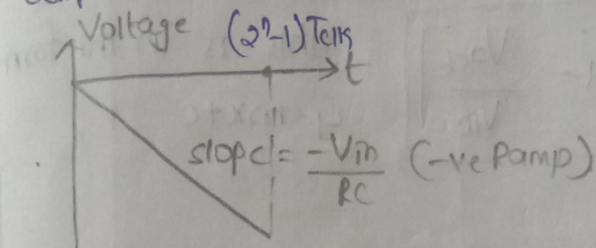
$$V_o = -\frac{1}{RC} \int_0^t V_{in} dt$$

After performing operation, $V_o = -\frac{V_{in}}{RC} t$

it is in the form of $y=mx$

$$\text{slope} = -\frac{V_{in}}{RC}$$

output waveform:



V_o is -ve. It is compared with '0' ($\because$ 2nd op-amp is Schmitt trigger) (or) comparator

if $V_o > 0$ comp $\rightarrow$ logic 0

if $V_o < 0$ comp $\rightarrow$ logic 1

(*) If V_{in} always +ve value, $\Rightarrow$ gives ' V_o ' always give '-ve' output, then comparator's output will always logic '1'!

$\Rightarrow$ Then AND Gate output is 1 and it produces in the form of clock pulse.

$\Rightarrow$ Then the counter starts counting and it will continue the state until it reaches the maximum state. Here maximum = $(2^n - 1) T_{clk}$.

$\Rightarrow$ Whenever the counter reaches maximum value, the control CK1 do two things (i) The control CK1 will reset the counter (ii) and change the position of the switch.

Case (ii)

If integrator input is ' $-V_{ref}$ ' is connected, then the output of the integrator becomes.

$$V_o = -\frac{1}{RC} \left[\int_0^{T_1} V_{in} dt + \int_{T_1}^t V_{ref} \cdot dt \right]$$

$$V_o = -\frac{1}{RC} \left[V_{in} T_1 + V_{ref} (t - T_1) \right]$$

$$V_o = -\frac{V_{in} T_1}{RC} - \frac{V_{ref}}{RC} (t - T_1)$$

$$V_o = -\frac{V_{in} T_1}{RC} - \frac{V_{ref}}{RC} t + \frac{V_{ref}}{RC} T_1$$

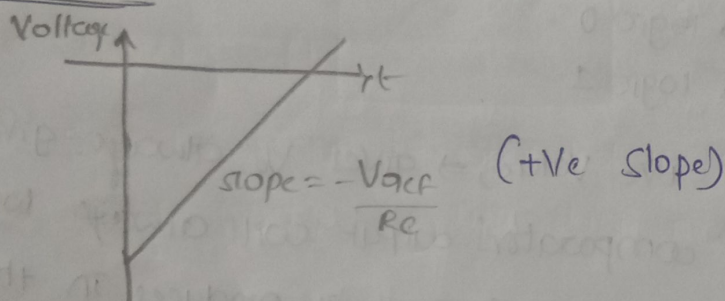
$$V_o = -\frac{T_1}{RC} (V_{in} - V_{ref}) - \frac{V_{ref}}{RC} t$$

$$V_o = -\frac{V_{ref}}{RC} t - \frac{T_1 V_{in}}{RC} \left[1 - \frac{V_{ref}}{V_{in}} \right]$$

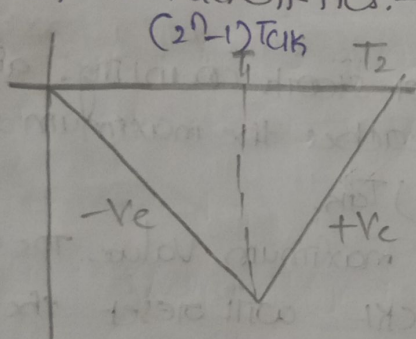
This is in the form of $y = mx + c$

Then, Slope = $-\frac{V_{ref}}{RC}$

Output wave:-



Transfer characteristics:-



$$t < T_2 \Rightarrow V_o = -V_e$$

$$t > T_2 \Rightarrow V_o = +V_e$$

$\Rightarrow$ The positive value given to cmp, $V_o > 0$, o/p = 0. Hence AND gate is disabled & counter stops counting. Hence the o/p of cmp is taken as final o/p.

After T_2 , $V_o = +V_e$, $V_o = 0$

$$\Rightarrow 0 = -\frac{V_{ref}}{RC} T_2 - \frac{T_1 V_{in}}{RC} \left[1 - \frac{V_{ref}}{V_{in}} \right]$$

$$\frac{T_1 V_{in}}{RC} \left(1 - \frac{V_{ref}}{V_{in}} \right) = -\frac{V_{ref}}{RC} T_2$$

$$T_1 V_{in} \left(1 - \frac{V_{ref}}{V_{in}} \right) = -V_{ref} T_2$$

If $V_{in} = 0$, $|V_{ref}| = |V_{in}|$ ($\because V_{ref} = -V_e$)

$$T_1 V_{in} \left(1 - \frac{-2}{2} \right) = +V_{in} T_2 \quad \left(\text{Suppose } V_{ref} = -2V, V_{in} = 2V \right)$$

$$\frac{T_1 V_{in} (2)}{V_{in}} = T_2 \Rightarrow T_2 = 2T_1$$

$$T_2 = 2 \times (2^n - 1) T_{clk}$$

$$T_2 \approx 2^{n+1} T_{clk}$$

* It is the slowest type, it requires more conversion time.
 ⇒ In counter CRT, we can also use T-Flipflop. Generally used D-Flipflop.

Lab Topic