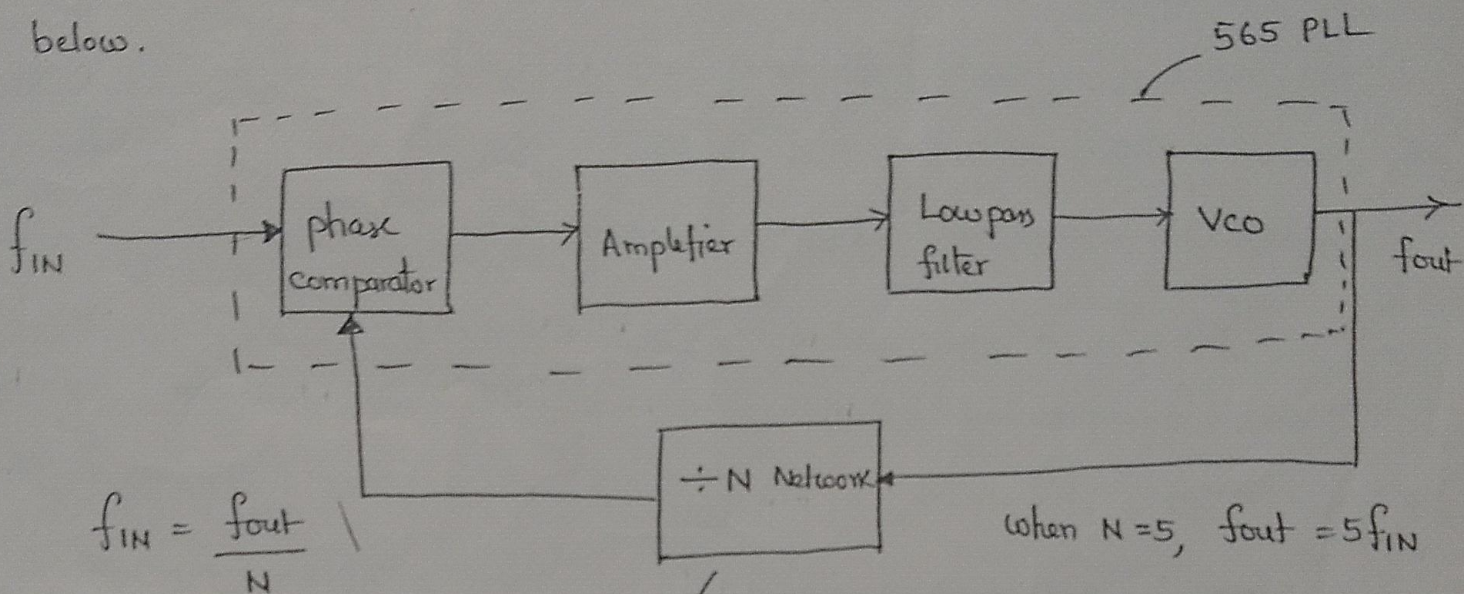


Applications of 565 PLL :-

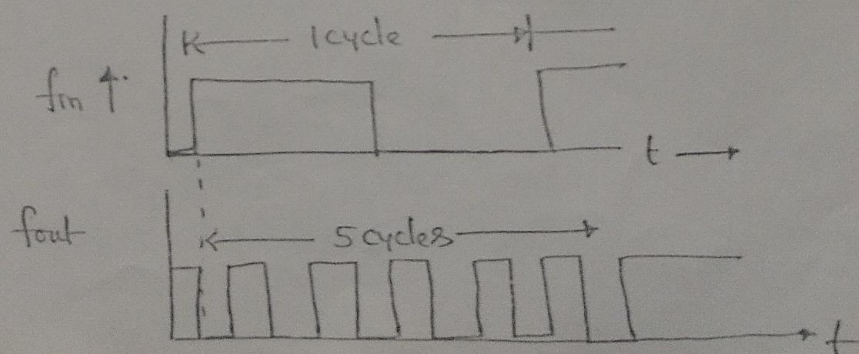
- a) Frequency Multiplier :- The block diagram of a Frequency Multiplier is given below.



In this multiplier Frequency divider network is inserted in between VCO and the phase detector. comparator. As the o/p of the divider network is locked to the input frequency f_{IN} , the VCO is actually running at the Multiples of the Input frequency. The desired multiplication can be obtained by selecting proper divide-by-N network. Here N is an integer.

For ex : If we want $f_o = 5 f_{IN}$ we have to use $\div 5$ divider Network.

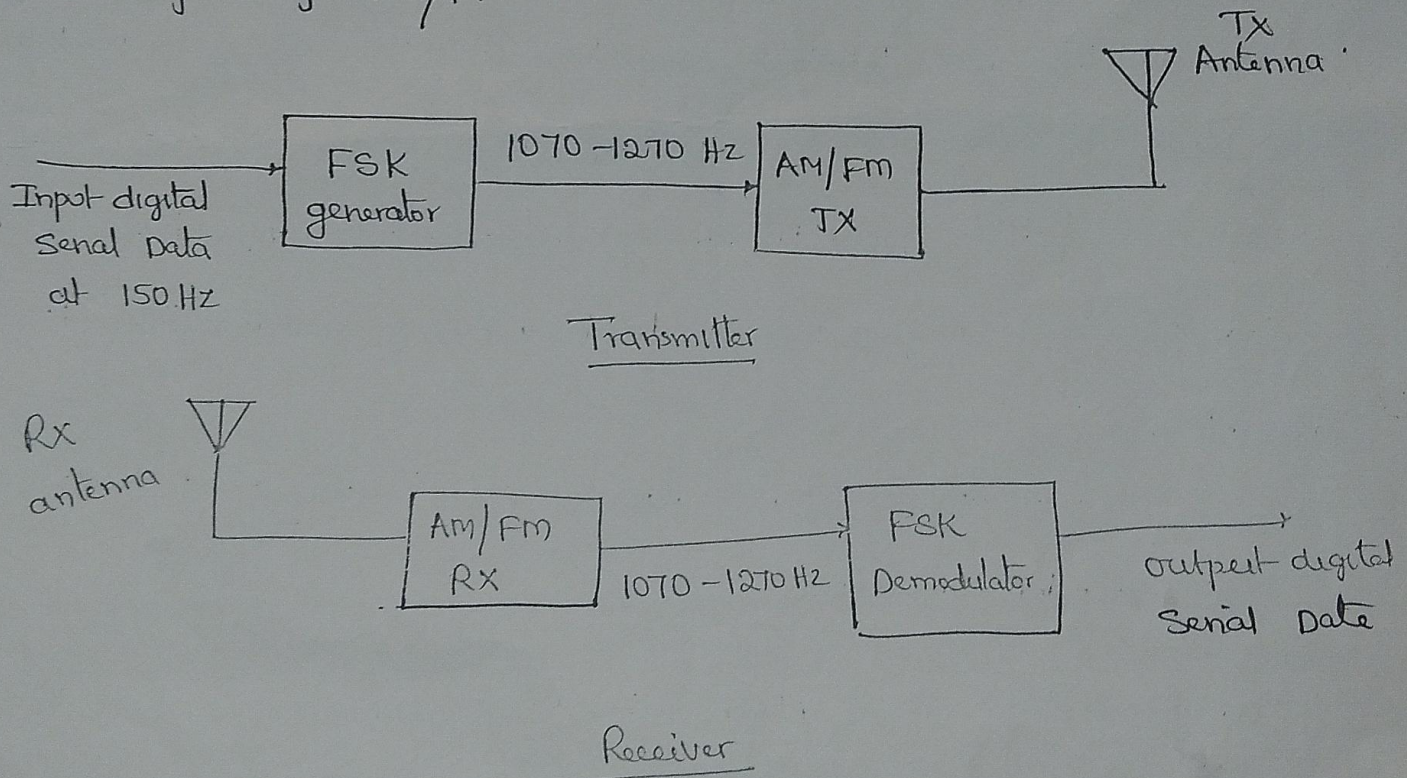
In the practical circuit Along with NE 565 PLL we have to use 7490 Frequency divider Network. The relevant input and o/p wave forms are



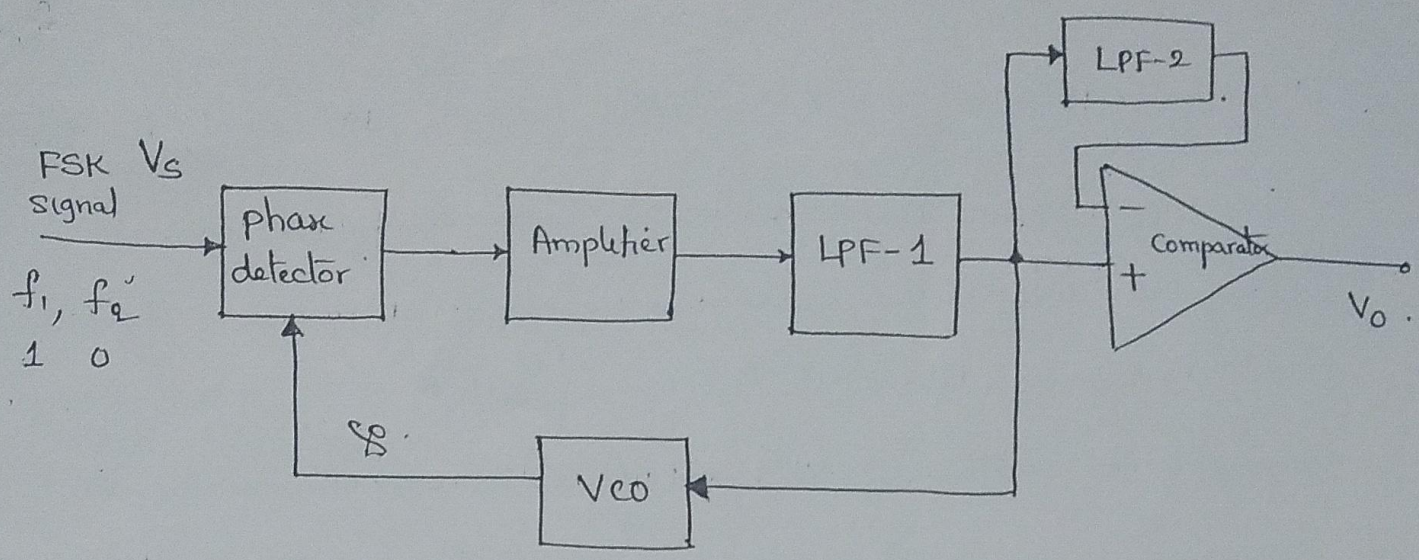
b) Frequency shift Keying (FSK) Demodulator :-

In computer and radio communications the binary coded data is transmitted by means of a carrier frequency and it is shifted between two preset frequencies. As the carrier frequency is shifted like this, the data transmission is said to use Frequency shift Keying technique (FSK).

565 PLL is also used as FSK demodulator. In 565 PLL, the frequency shift is accomplished by driving a VCO with binary data signal so that the two resulting frequencies for logic 0 and logic 1. The frequencies corresponding to logic 1 and logic 0 are called as mark & space frequencies. The block diagram of AM/FM Transmitter and Receiver is given below.



The PLL can be used as a FSK Demodulator. The block diagram is almost like FM demodulator except the addition of comparator to produce a reconstructed digital output signal.



If there are two frequencies for 1 and zero and if the PLL is remain locked into the FSK signal at both f_1 and f_2 the VCO control voltage which is also supplied to the comparator is given as

$$V_{c1} = (f_1 - f_0) / K_V$$

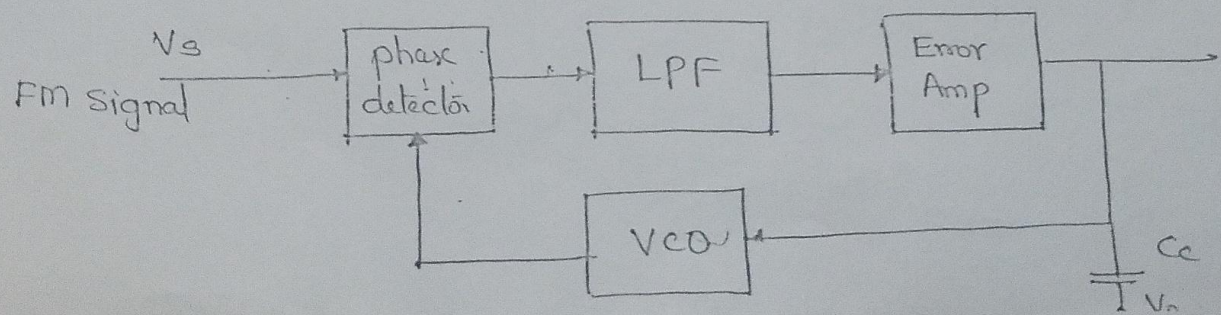
$$V_{c2} = (f_2 - f_0) / K_V$$

Here K_V is the voltage - freq transfer coefficient of VCO.

$$V_{c1} - V_{c2} = \Delta V_c = (f_2 - f_1) / K_V$$

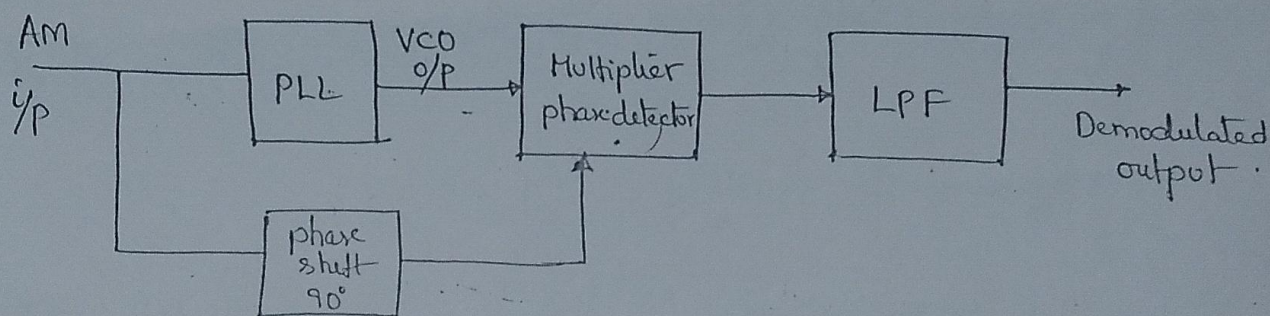
The reference voltage for the comparator is derived from the additional low pass filter which is adjusted in between V_{c1} and V_{c2} , thus comparator produces 0 and 1 respectively.

FM Demodulator :- The PLL can be used very easily as an FM detector/demodulator. The block diagram is



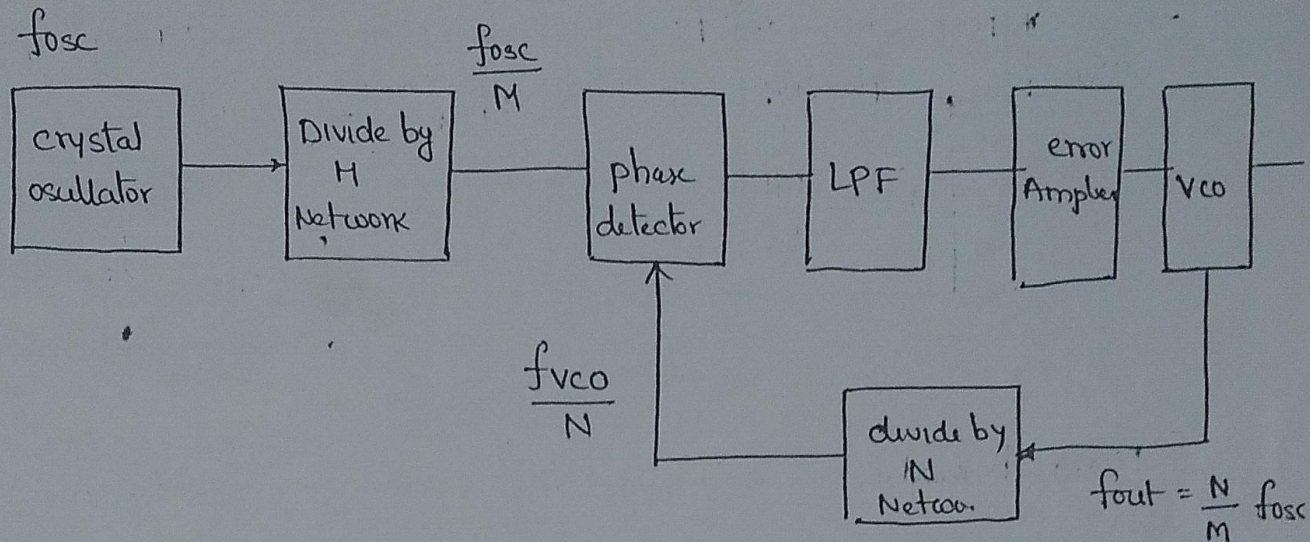
when the PLL is locked on to the incoming FM signal, the VCO frequency follows the instantaneous frequency of FM, and the error voltage is proportional to the deviation of input frequency from the centre frequency. Hence the a-c component of error voltage of VCO represent the modulating voltage of FM at the ~~receiver~~ transmitter. It is important to note that FM frequency deviation and modulating frequency should remain in the locking range of PLL for exact replica of modulating signal.

AM Detector :— The block diagram of AM demodulator is shown below



Principle : The PLL is locked into the carrier frequency of incoming signal. Once locked the o/p frequency of VCO is same as carrier frequency and it is in unmodulated form. The Modulated signal with 90° phase shift and unmodulated carrier from PLL are applied to multiplier and are in the same phase. Then the o/p of multiplier contains sum and difference signals. LPF rejects high frequency components, gives demodulated output. Because of PLL, AM detector exhibits a high degree of selectivity and noise immunity which is poor in ordinary AM demodulators.

Frequency Synthesizer :- The PLL can be used as the main component for frequency synthesizer which produces series of frequencies that are obtained from stable crystal oscillator. The block diagram is shown below.



The above circuit is similar to frequency multiplier except that divide by M network is added at the input of phase detector.

The input to the phase detector is $\frac{f_{osc}}{M}$ and the out of divide by N network is $\frac{f_{vco}}{N}$. when the PLL is in locked state we have

$$\frac{f_{osc}}{M} = \frac{f_{vco}}{N}$$

$$\therefore \text{The o/p freq or } f_{vco} = \left(\frac{N}{M}\right) f_{osc}$$

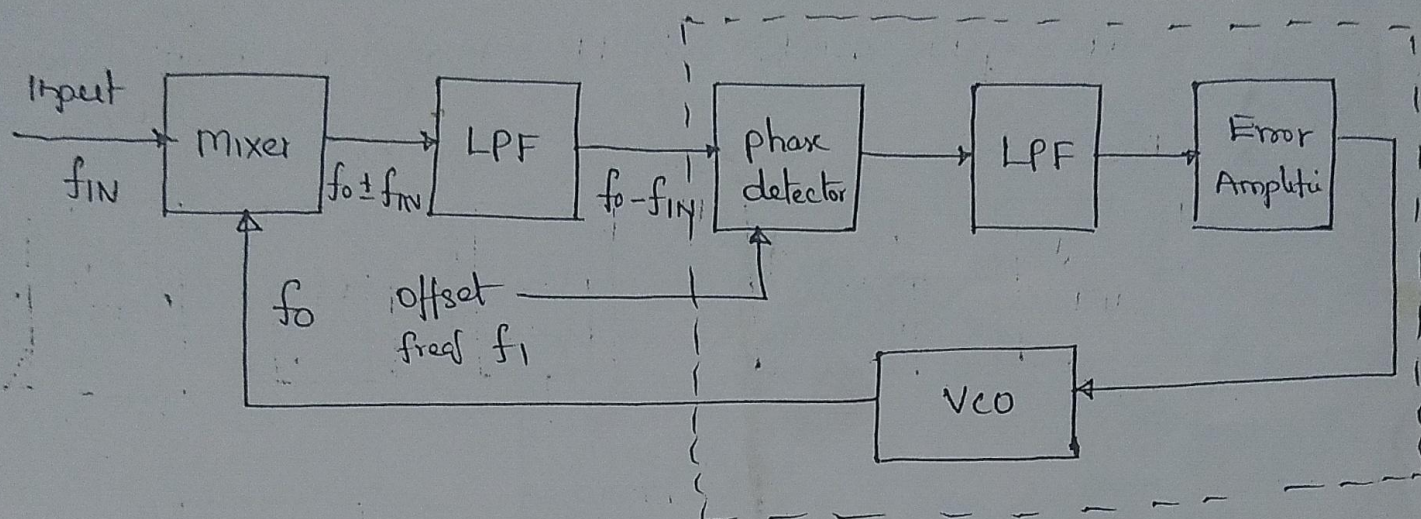
by adjusting divider counts to desired values large no of frequencies can be produced.

Frequency Translator :- Frequency Translation means shifting the frequency of an oscillator by a small factor.

The block diagram of Frequency Translator is given below. It consists of mixer, low pass filter and the PLL.

(2)

PLL



Mixer heterodynes or mixes the incoming frequency f_{IN} and VCO freq f_0 producing $f_0 \pm f_{IN}$ i.e. it produces sum and difference of frequencies. The LPF allows only $f_0 - f_{IN}$ and rejects $f_0 + f_{IN}$. Then the $f_0 + f_{IN}$ component is applied to phase detector and another input is offset freq f_1 . In the locked mode

$$f_0 - f_{IN} = f_1$$

$$f_0 = f_1 + f_{IN}$$

By adjusting the offset frequency, we can shift frequency of the oscillator to any desired value.