

UNIT-5

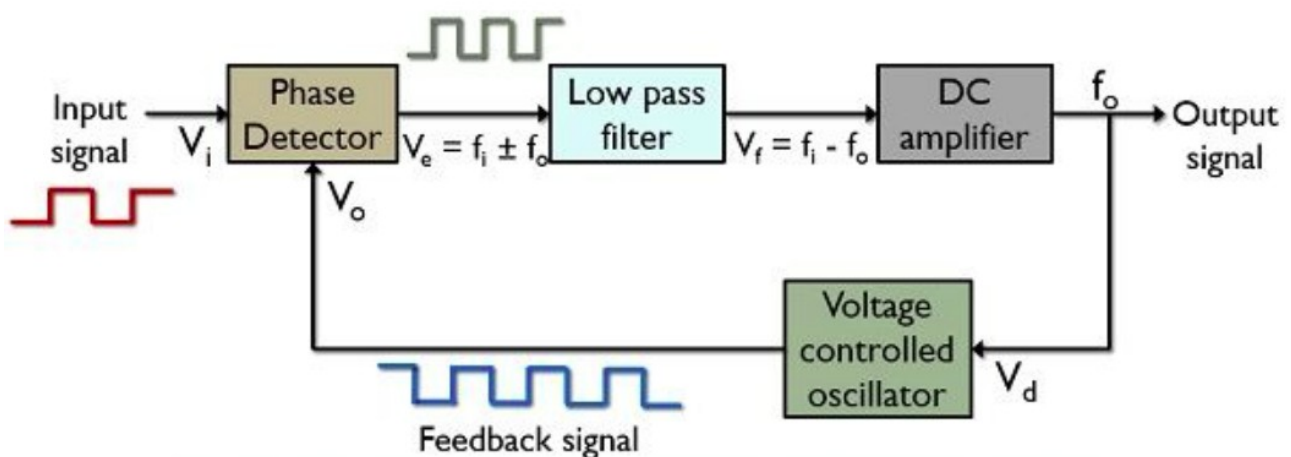
PHASE LOCKED

LOOP(PLL)

Phase-Locked Loops (PLL)

Definition: Phase-locked loops are the circuits used to maintain synchronization between input and output frequency of oscillator circuits by comparing the difference in phase of the two signals. With the evolution of IC, it has emerged as the basic building block of electronic circuits.

Block Diagram and Working of Phase-Locked Loop



Phase Detector

The phase detector performs a comparison of the frequency of actually applied digital input signal with the frequency of feedback signal. The output generated is a dc voltage (also called error voltage, V_e) whose amplitude is proportional to the phase difference of the two signals applied at the input. Here output voltage is a DC voltage and error voltage.

Low-pass filter

The output of the phase detector is provided to a low pass filter, that eliminates the high-frequency component and noise from the output of the comparator. We can use active LPF and passive LPF.

Voltage Controlled Oscillator

It generates high frequency signals. The instantaneous VCO frequency is controlled by its input frequency.

i.e, $f_0 = f + k w_m$

k=based on input voltage

The frequency of VCO is directly controlled by DC input voltage.

MODES OF OPERATION OF PLL:

PLL has three stages (or) three modes of operations

1.Free running

2.Capture rate

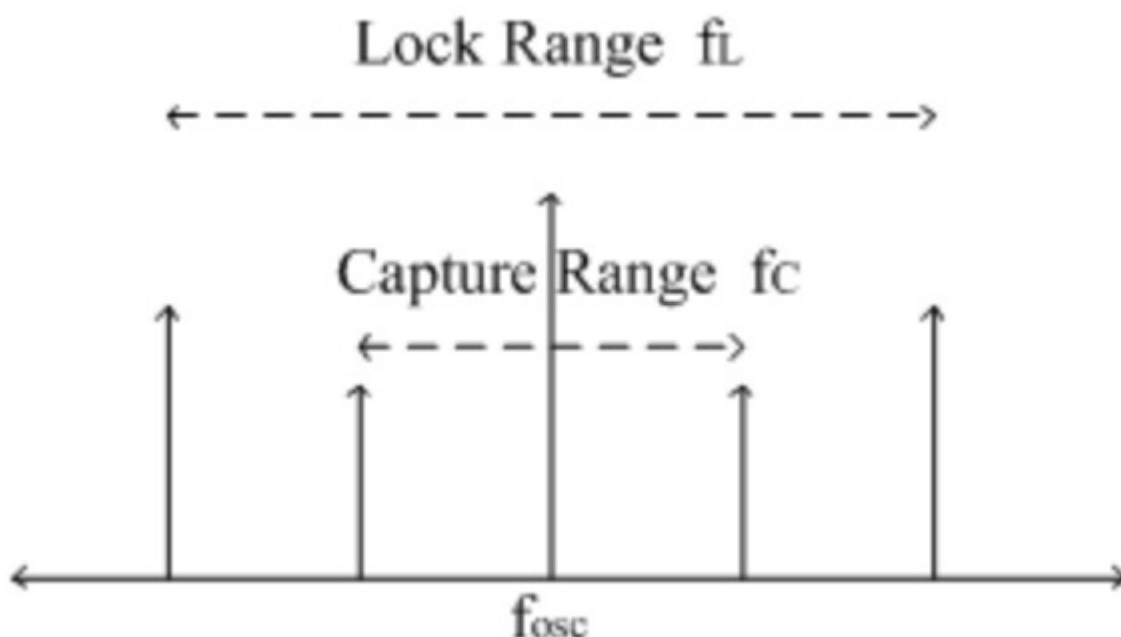
3.Phase-Locked mode

PLL operates in **free running mode** when no input is applied to it. When an input signal having some frequency is applied to PLL, then the output signal frequency of VCO will start change. At this stage, the PLL is

said to be operating in the **capture mode**. The output signal frequency of VCO will change continuously until it is equal to the input signal frequency. Now, it is said to be PLL is operating in the **lock mode**.

PLL Ranges:

PLL can acquire lock state only when input signal is within the capture range.

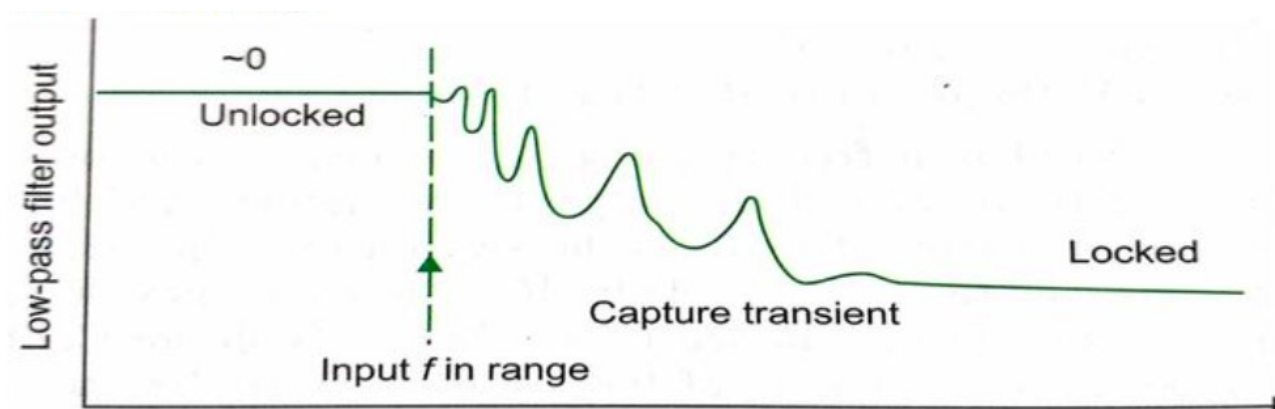


CAPTURE RANGE:

The range of input frequencies around the VCO centre frequency in which loop can lock when starting from unlock condition.

LOCK RANGE:

The range of input frequencies over which the loop remain in the lock condition once it has capture the input signal. The below figure shows the capture transient.



TYPES OF PHASE DETECTORS:

There are two types of phase detectors

1. Analog phase detector

1.1 Switch detector

1.2 Balanced modulator

2. Digital phase detector

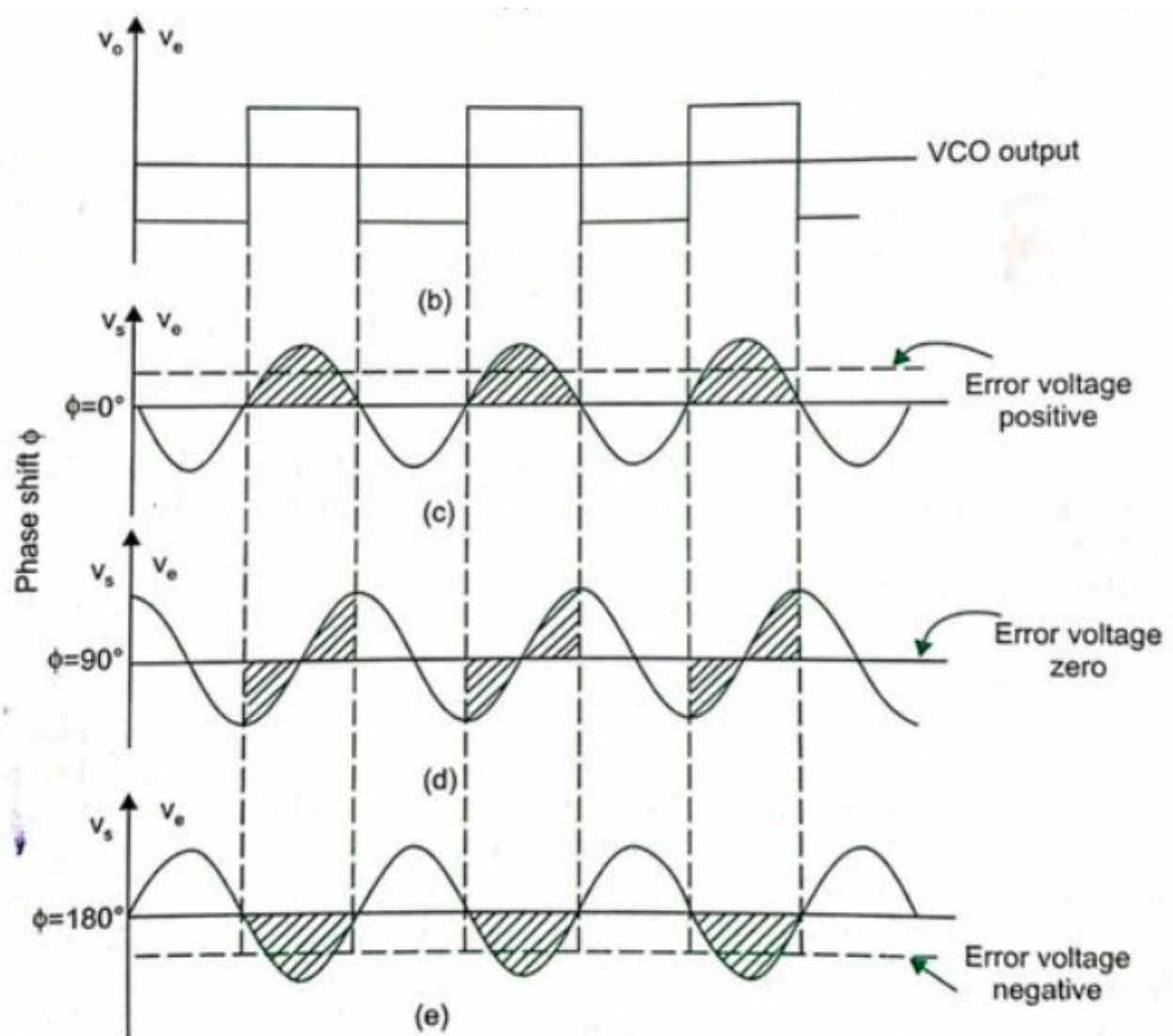
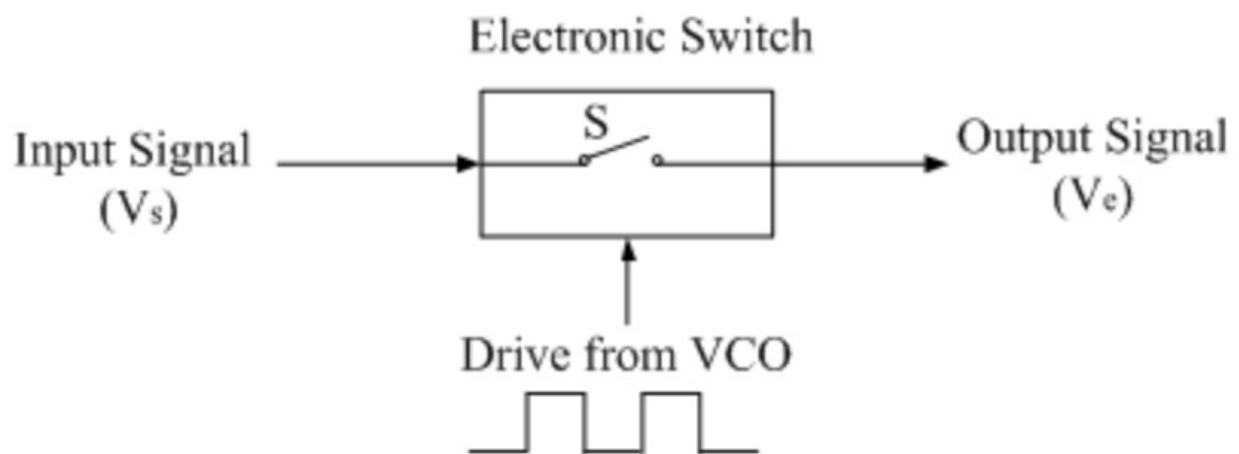
2.1 EX-OR phase detector

2.2 Edge trigger phase detector

2.3 Monolithic phase detector

1. Analog phase detector

1.1 switch type:



Mathematical Analasis for Analog phase detector:

A phase comparator is basically a multiplier which multiplies the input signal ($V_s = V_s \sin \omega t = V_s \sin \pi 2f_s t$) by the VCO signal ($V_o = V_o \sin 2\pi f_o t + \phi$) the output of phase detector is i.e,

$$V_e = k \cdot V_s \cdot V_o \sin(2\pi f_s t) \cdot \sin(2\pi f_o t + \phi)$$

where,

k = phase comparator gain

ϕ = phase shift between input signal & VCO output

Therefore, the above equation is expressed as

$$2 \sin A \sin B = \cos(A-B) - \cos(A+B)$$

$$V_e = k V_s V_o / 2 \times 2 \sin(2\pi f_s t) \cdot \sin(2\pi f_s t + \phi)$$

$$V_e = kV_s V_0 / 2 \times (\cos(2\pi f_s t - 2\pi f_s t + \emptyset)) - (\cos(2\pi f_s t + 2\pi f_s t + \emptyset))$$

The perfect lock condition is $f_s = f_o$

$$\mathbf{V_e = kV_s V_0 / 2 \times (Cos(-\emptyset) - (Cos(4\pi f_o t + \emptyset))}$$

The above error voltage is passed through the LPF.

$4\pi f_o t + \emptyset$ is high frequency (or) double frequency. This component is removed by the LPF.

The error voltage passes through the LPF and LPF can remove the high frequency component and allow the low frequency component.

$$V_e = kV_s V_0 / 2 \times (\cos(-\emptyset))$$

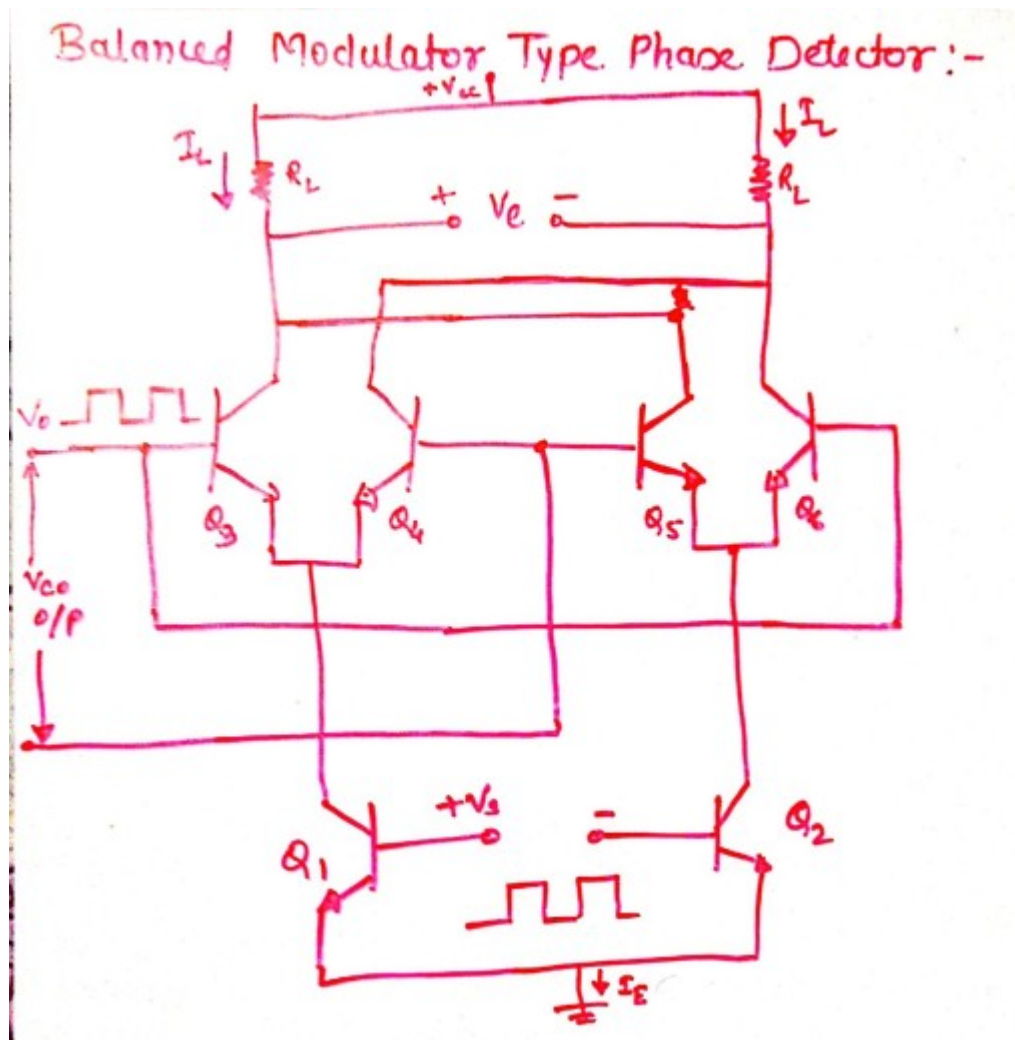
Here, $\emptyset = 90^\circ$

$$V_e = kV_s V_0 / 2 \times (\cos(-90^\circ))$$

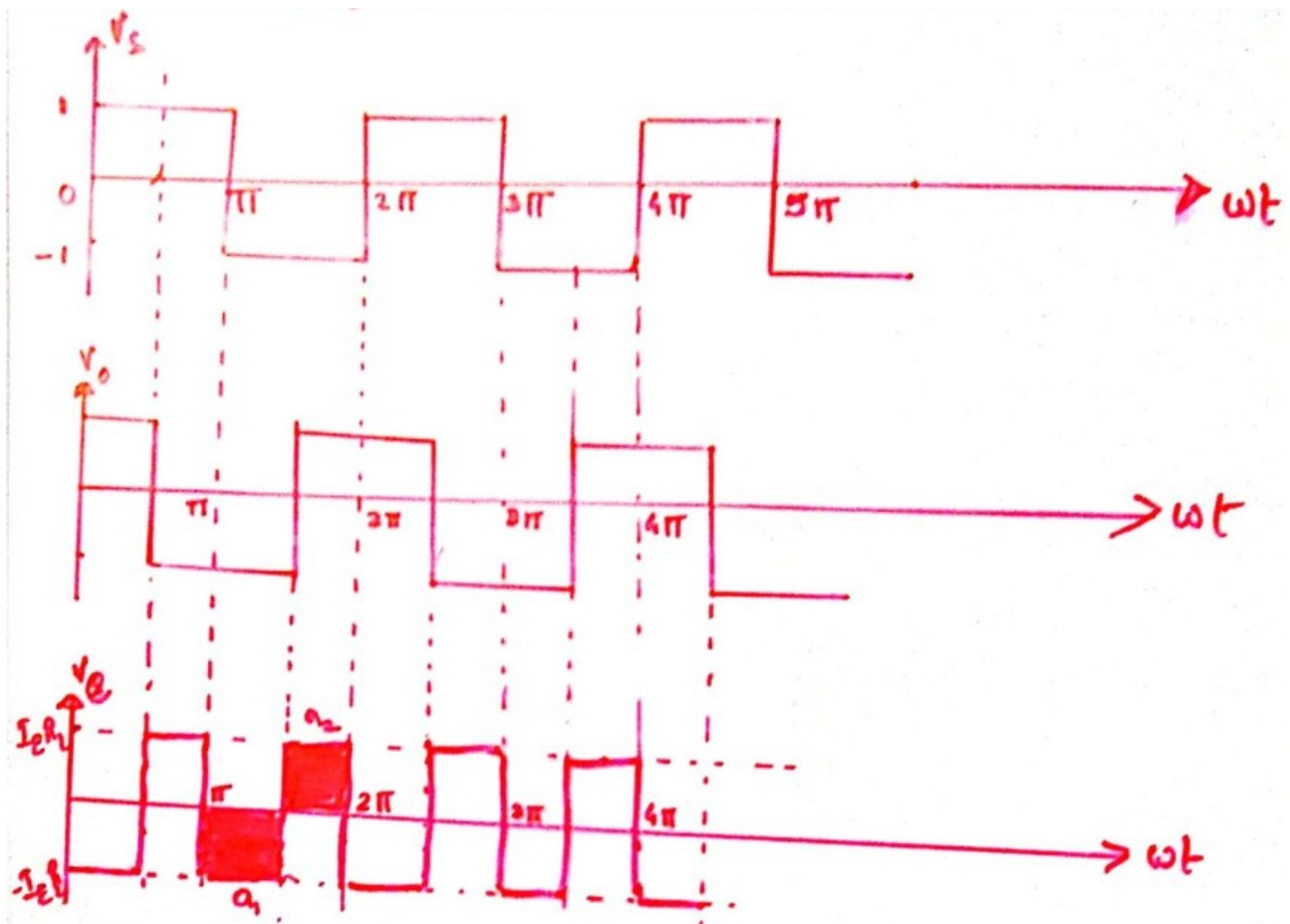
$$v_e = 0$$

Does the VCO output and input signals V_S should be 90° out of phase for a perfect lock.

1.2 BALANCED MODULATOR



figA: Balanced modulator



figB: Timing diagram of input and output of balanced modulator

V_s	V_o	Q_1	Q_2	Q_3-Q_6	Q_4-Q_5	V_e
Positive	Positive	ON	OFF	ON	OFF	Negative
Positive	Negative	ON	OFF	OFF	ON	Positive
Negative	Positive	OFF	ON	ON	OFF	Positive
Negative	Negative	OFF	ON	OFF	ON	Negative

Here input signal is applied to the differential pair Q1&Q2.

The transistors Q3&Q4 and Q5&Q6 are two set of SPDF switches activated by the VCO output. The input signal V_s the VCO output

V_0 are assume to be high enough to switch the transistors.

*figure A is fully on (or) off state and figure B is when V_s and V_0 both are high during the time 0 to $(\pi - \theta)$, the transistors Q1&Q3 are driven ON the current I_E flows through the Q1&Q3.

*This gives the output voltage.

$$*V_E = -I_E \cdot R_L \dots 1$$

And for the next period $(\pi - \theta)$ for π ,

*when V_s is high and V_0 is low the transistors Q1&Q4 are driven ON state. resulting in an output voltage

$$V_e = I_E R_L \dots 2$$

The average value of phase detector output V_e can be calculated as follows,

$$V_{e(avg)} = 1/\pi \times (\text{area } A1 + \text{area } A2)$$

$$= 1/\pi \times (I_E R_L \phi + (-I_E R_L (\pi - \phi)))$$

$$= 1/\pi \times (I_E R_L \phi - I_E R_L \pi + I_E R_L \phi)$$

$$= 1/\pi \times (2I_E R_L \phi - I_E R_L \pi)$$

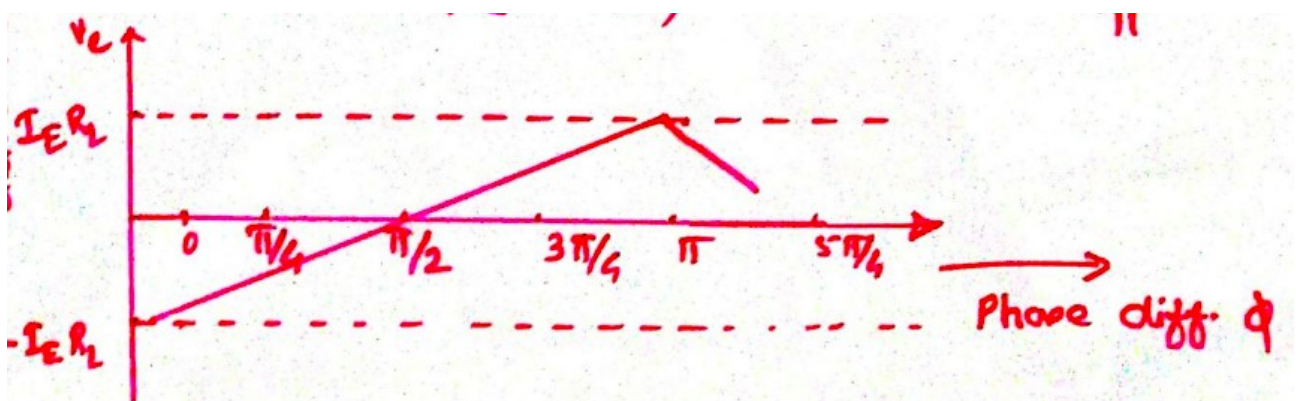
$$= I_E R_L / \pi \times (2\phi - \pi)$$

$$= I_E R_L \times (2\phi / \pi - 1) \quad (I_E = 2I_Q)$$

$$= 4I_Q R_L / \pi \times (\phi - \pi/2)$$

$$\mathbf{V_e = k\phi(\phi - \pi/2)}$$

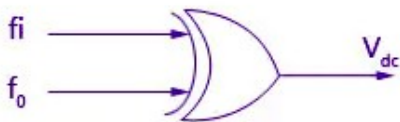
where, $k\phi =$ conversion ratio of the phase detector.



2.DIGITAL PHASE DETECTOER

2.1 EX-OR GATE PHASE DETECTOR

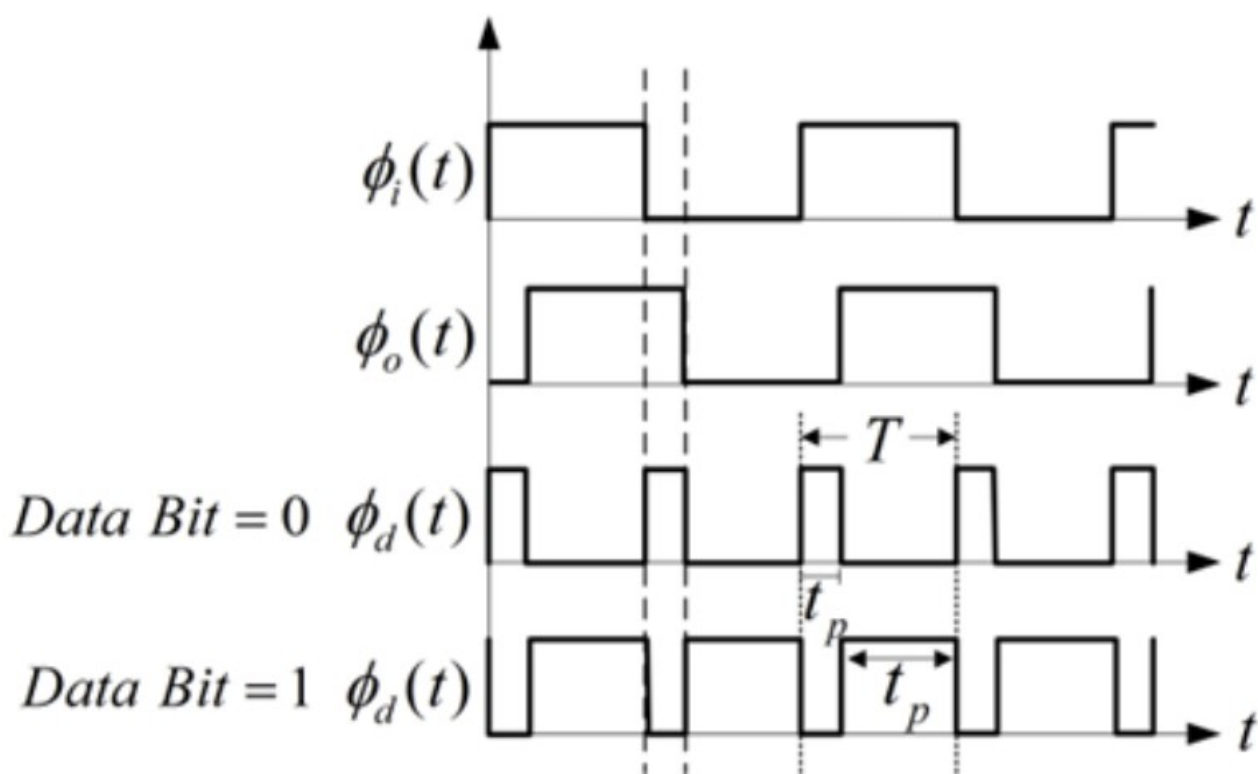
Exclusive - OR Phase Detector



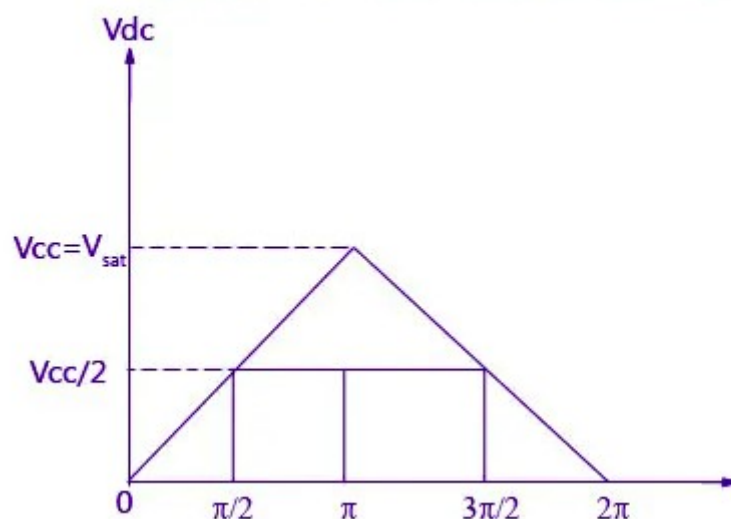
f_i	f_o	Output
Low	Low	Low
Low	High	High
High	Low	High
High	High	Low

The XOR phase detector is simply exclusive OR gate. We know the simple operation of exclusive OR gate, it compare phase difference between both signal and produce output pulses basis on the input varies. It provide dc level proportional to the phase difference between the inputs. While the XOR circuit produces error pulses

on both rising and falling edges. The operation of phase detectors is similar to that of differential amplifiers in that both sense the difference between the inputs, generating a proportional output. It doesn't contain any phase difference information.



Exclusive - OR Phase Detector - Waveform



$$K\phi = V_{cc}/\pi$$

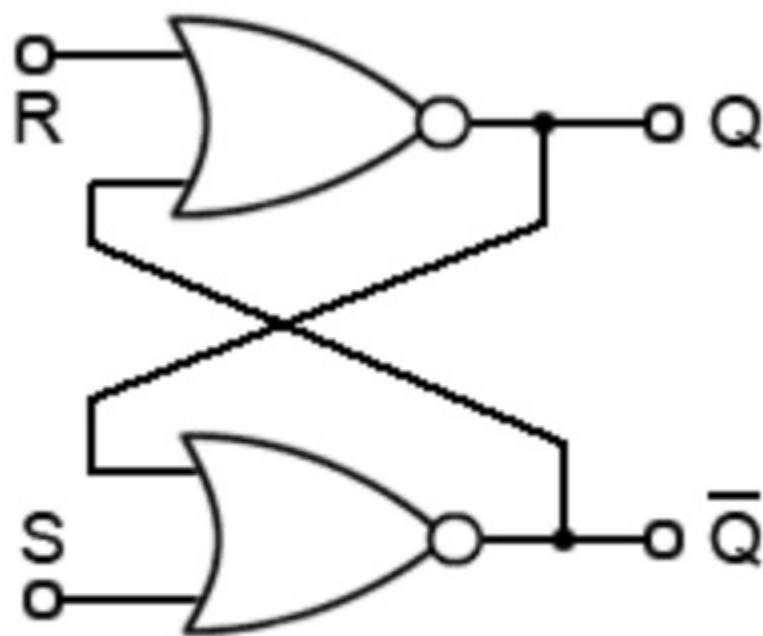
$$\text{If } V_{cc} = 5V$$

$$K\phi = 5/\pi$$

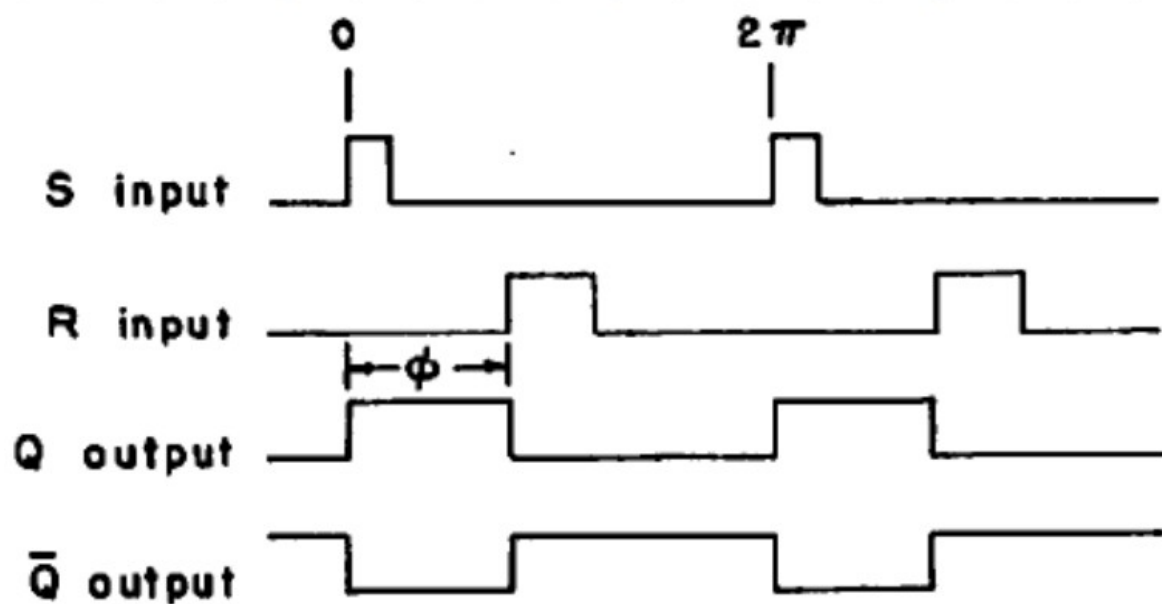
$$K\phi = 1.59V/\text{rad}$$

2.2 EDGE TRIGGER PHASE DETECTOR

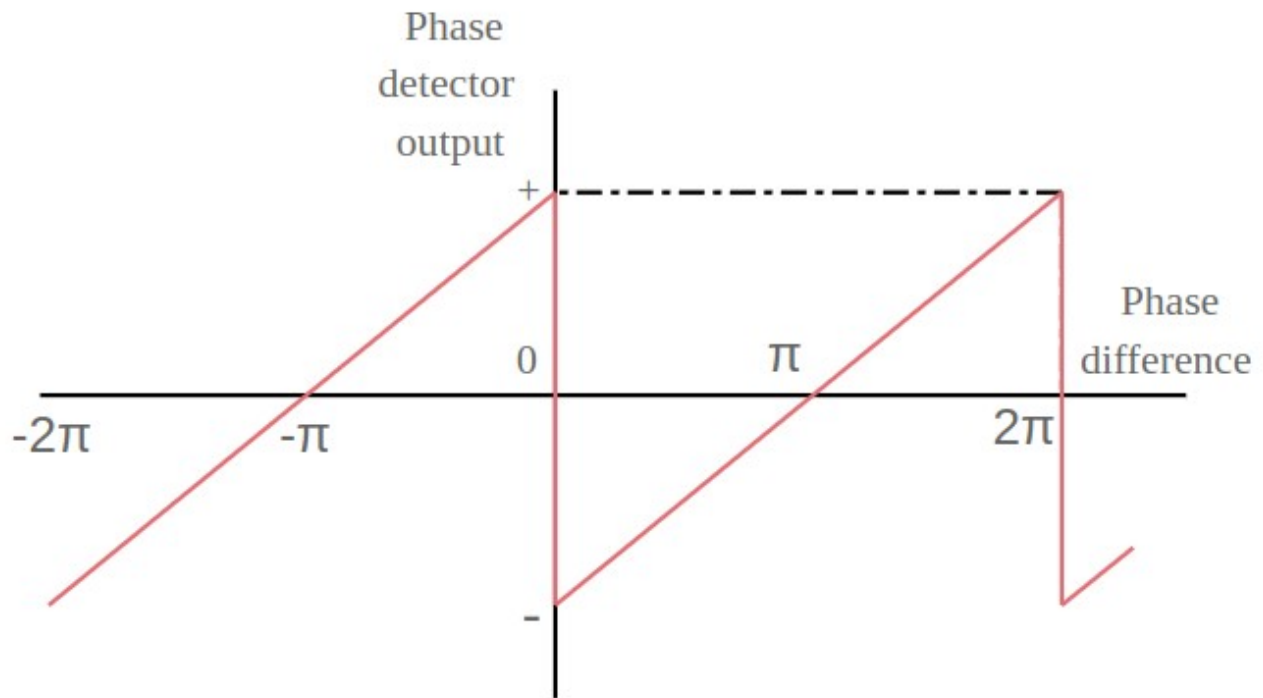
An edge trigger phase detector is used when the input and output frequencies are in pulse waveform, which is less than 50% duty cycle. The R-S flip flop is used for the phase detectors, which is shown in the below figure. To form R-S [flip flop](#), the two NOR gates are cross-coupled. The output of the phase detector can change its logic state by triggering the R-S flip flop. The positive edge of the input and output frequencies can change the output of the phase detector.



Edge Trigger Phase Detector



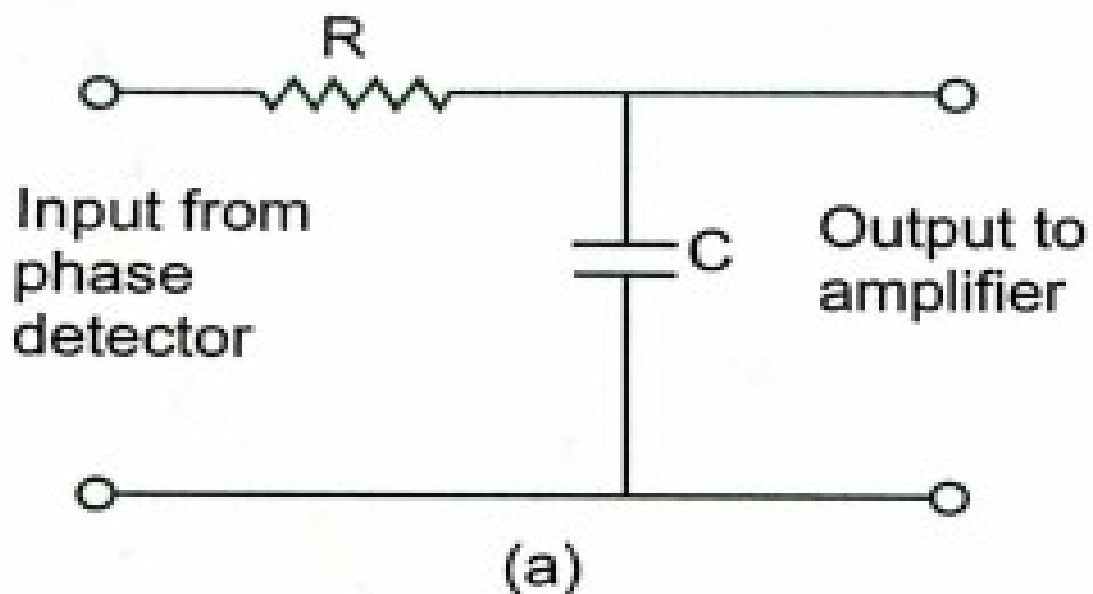
Input/output waveforms for the R-S flip-flop edge-triggered phase detector.



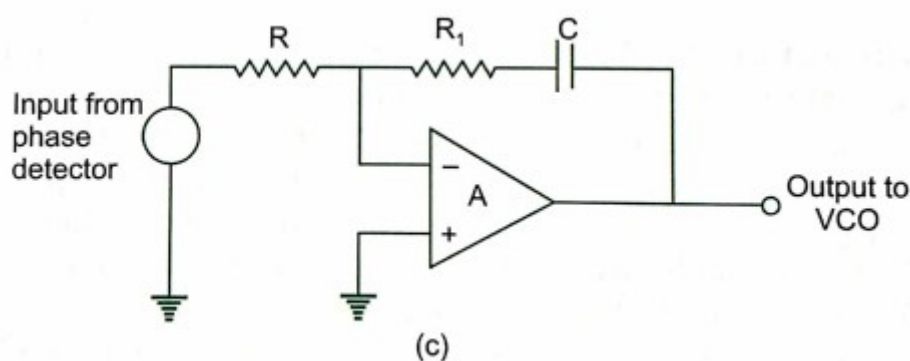
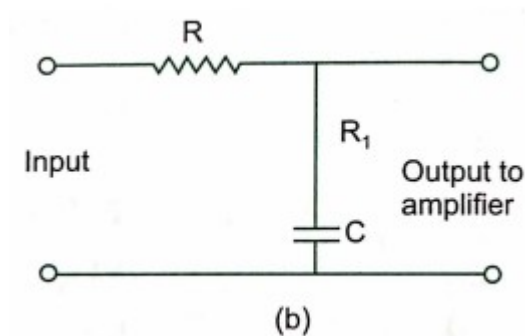
$$K\phi = V_{cc}/2\pi ; \text{If, } V_{cc} = 5V$$

$$K\phi = 5/2\pi; K\phi = 0.8V/\text{rad}$$

LOW PASS FILTER



PASSIVE FILTER

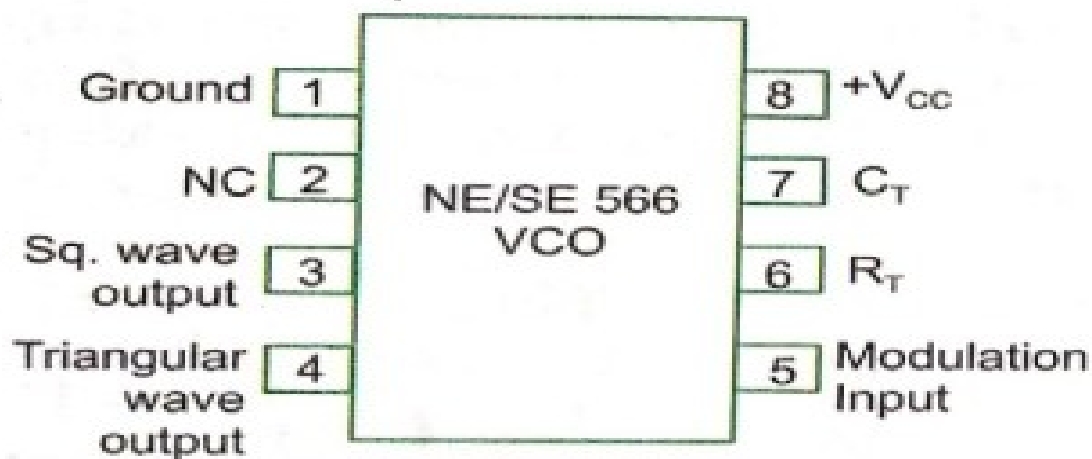


ACTIVE FILTER

The low pass filter not only removes the high frequency components and noise but also controls the dynamic characteristics of PLL. such as like capture, lock range, band width and transient response. If the filter band width is reduced the response time is increases. However reducing the

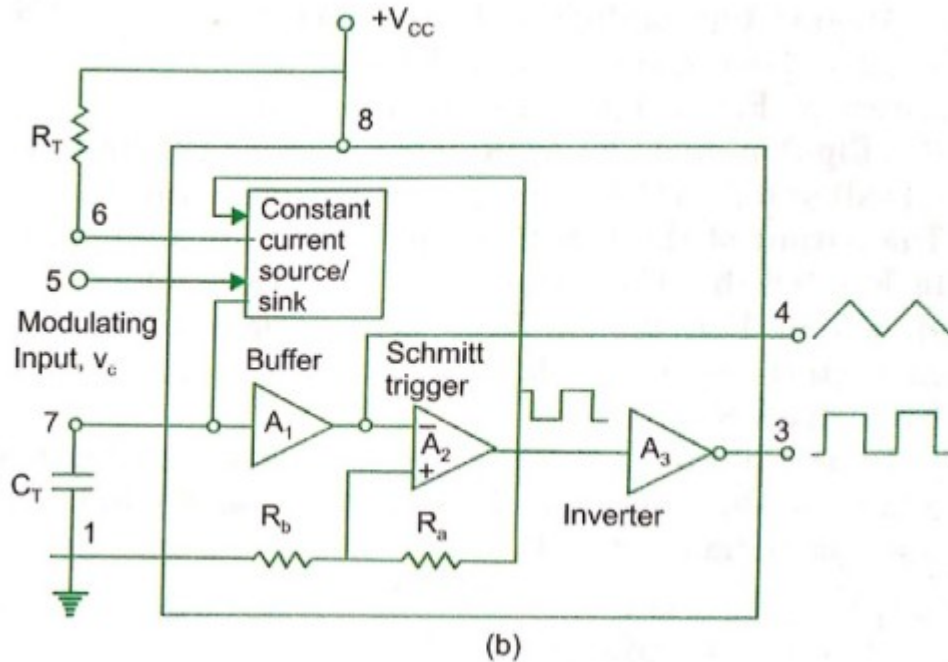
bandwidth of filter also reduces the capture range of the PLL. This produces high noise immunity and locking stability of PLL.

VOLTAGE CONTROLLED OSCILLATOR

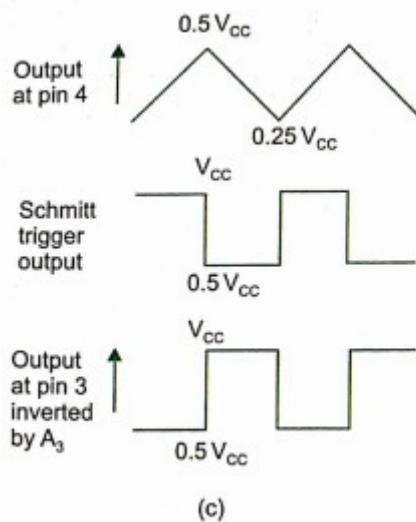


(a)

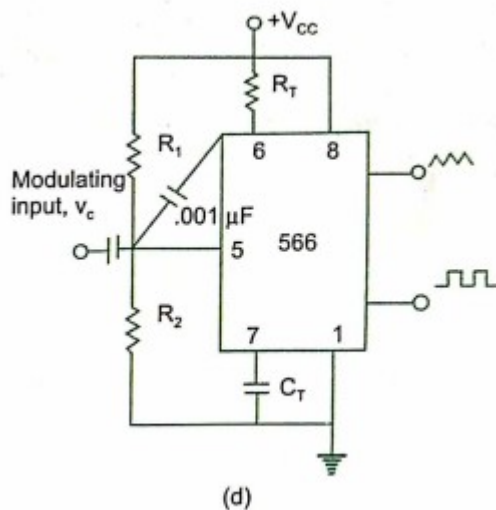
PIN CONFIGURATION OF IC NE/SE 566



BLOCK DIAGRAM OF IC566



OUTPUTWAVEFORMS



TYPICAL CONNECTION DIAGRAM

The total voltage on the capacitor changes from $0.25 V_{CC}$ to $0.5 V_{CC}$. Thus $\Delta v = 0.25 V_{CC}$. The capacitor charges with a constant current source.

So
$$\frac{\Delta v}{\Delta t} = \frac{i}{C_T}$$

or,
$$\frac{0.25 V_{CC}}{\Delta t} = \frac{i}{C_T}$$

or,
$$\Delta t = \frac{0.25 V_{CC} C_T}{i} \quad (9.8)$$

The time period T of the triangular waveform $= 2\Delta t$. The frequency of oscillator f_o is,

$$f_o = \frac{1}{T} = \frac{1}{2\Delta t} = \frac{i}{0.5 V_{CC} C_T}$$

But,
$$i = \frac{V_{CC} - v_c}{R_T} \quad (9.9)$$

where, v_c is the voltage at pin 5. Therefore,

$$f_o = \frac{2(V_{CC} - v_c)}{C_T R_T V_{CC}} \quad (9.10)$$

$$f_o = \frac{2(V_{CC} - (7/8) V_{CC})}{C_T R_T V_{CC}} = \frac{1}{4R_T C_T} = \frac{0.25}{R_T C_T} \quad (9.11)$$

Voltage to Frequency Conversion Factor

A parameter of importance for VCO is voltage to frequency conversion factor K_v and is defined as

$$K_v = \frac{\Delta f_o}{\Delta v_c}$$

Here Δv_c is the modulation voltage required to produce the frequency shift Δf_o for a VCO. If we assume that the original frequency is f_o and the new frequency is f_1 , then

$$\Delta f_o = f_1 - f_o = \frac{2(V_{CC} - v_c + \Delta v_c)}{C_T R_T V_{CC}} - \frac{2(V_{CC} - v_c)}{C_T R_T V_{CC}} = \frac{2\Delta v_c}{C_T R_T V_{CC}} \quad (9.12)$$

or,
$$\Delta v_c = \frac{\Delta f_o C_T R_T V_{CC}}{2} \quad (9.13)$$

Putting the value of $C_T R_T$ from Eq. (9.11)

$$\Delta v_c = \Delta f_o V_{CC} / 8f_o \quad (9.14)$$

or,
$$K_v = \frac{\Delta f_o}{\Delta v_c} = \frac{8f_o}{V_{CC}} \quad (9.15)$$

A Voltage-Controlled Oscillator (VCO) is a circuit that provides a varying output signal (typically of square-wave or triangular-wave form) whose frequency can be adjusted over a range controlled by an externally applied DC voltage.

The VCO provides a linear relationship between the applied voltage and the oscillation frequency. The applied voltage is called control voltage. The control of frequency with the help of control voltage is known as voltage to frequency conversion. Hence VCO is otherwise known as Voltage to frequency converter.

Practically VCO is available in IC form. IC 566 (LM566/SE566) from Signetics is a popular VCO. IC 566 contains circuitry to generate both square-wave and triangular-wave signals whose frequency is set by an external resistor and capacitor and then varied by an applied dc voltage.

With the following practical circuit value restrictions:

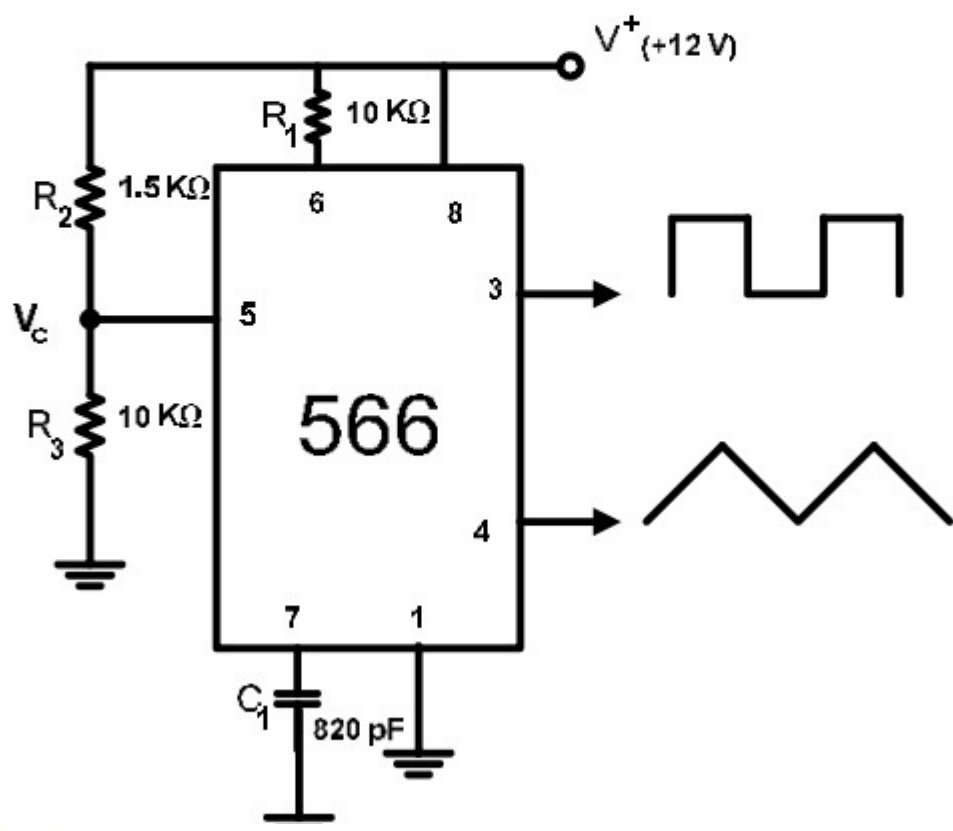
1. R_1 should be within the range ($2K\Omega \leq R_1 \leq 20K\Omega$).
2. V_c should be within range ($\frac{3}{4}V^+ \leq V_c \leq V^+$).
3. f_o should be below 1MHz.
4. V^+ should range between 10 V and 24 V.

Features:

1. Wide supply voltage range 10-24V
2. Very Linear Modulation characteristics
3. High temperature stability
4. Excellent power supply rejection
5. 10 to 1 Frequency range with fixed C1
6. The frequency can be controlled by means of current, voltage, resistor or capacitor.

For the circuit shown in Fig.(2), $R_1 = 10\text{ K}\Omega$ and $C_1 = 820\text{ pF}$, Find:

1. The control voltage V_c .
2. The free running-frequency f_o .



Solution:

$$1. \quad V_c = \frac{R_3}{R_2 + R_3} \times V^+ = \frac{10\text{ K}\Omega}{1.5\text{ K}\Omega + 10\text{ K}\Omega} \times (12\text{ V}) = 10.4\text{ V}$$

2. Using equation (1) yields:

$$f_o = \frac{2}{(10 \times 10^3)(820 \times 10^{-12})} \times \left(\frac{12 - 10.4}{12} \right) \approx 32.5\text{ KHz}$$

4.14.4 Applications of VCO

The various applications of VCO are

1. FM modulation.
2. Signal generation (Triangular or square wave)
3. Function generation.
4. Frequency shift keying i.e. FSK demodulator.
5. In frequency multipliers.
6. Converting low frequency signals such as EEG and EKG into audio frequency range signals.
7. Tone generation.

►►► **Example 4.11 :** For a 566 VCO shown in the Fig. 4.35 $+V = 10\text{ V}$, $R_2 = 1.2\text{ k}\Omega$ and $R_1 = R_3 = 10\text{ k}\Omega$ with $C_1 = 0.001\text{ }\mu\text{F}$.

a) Calculate the frequency of output.

b) Calculate the variation in f_o if V_C is varied between 7.7 V and 9.5 V .

MONOITHIC FACE LOCKED LOOP

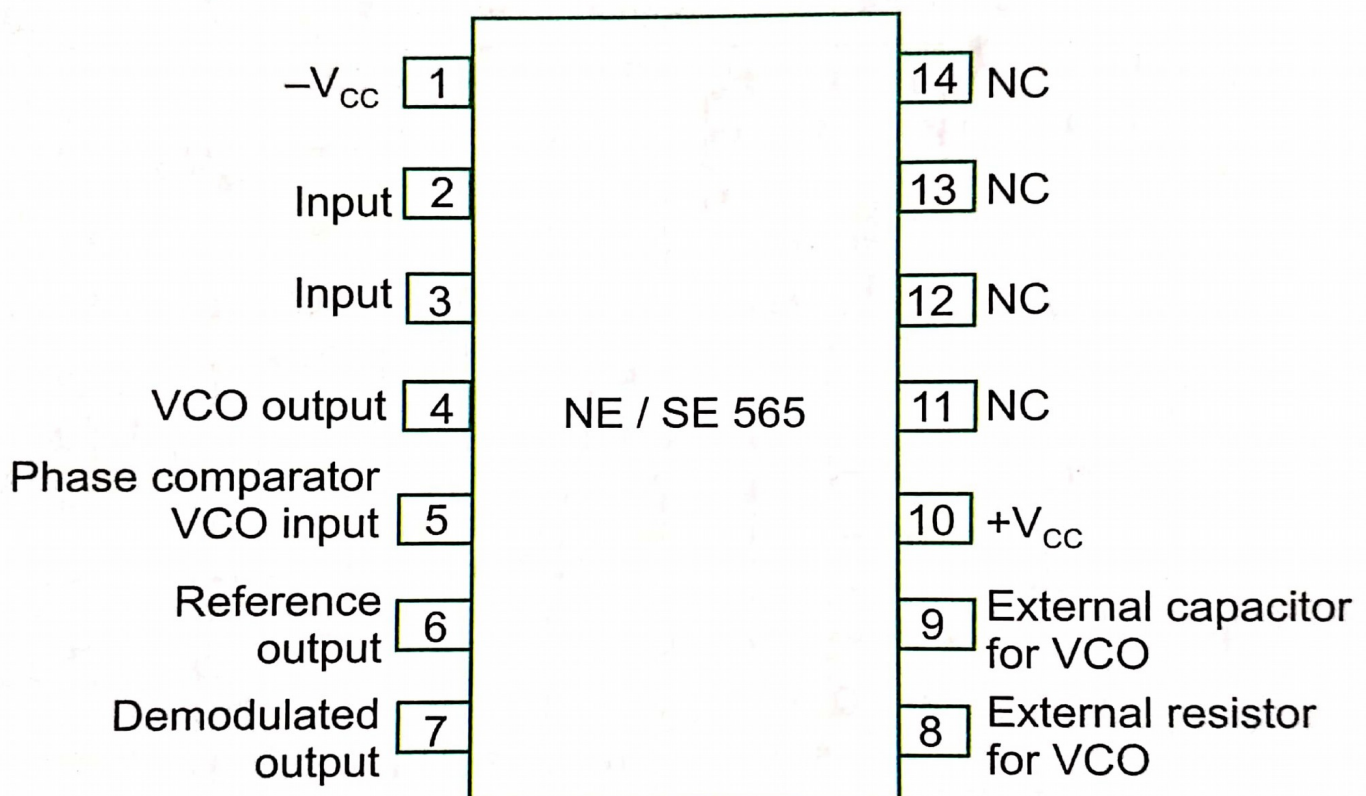


Fig. 9.9 (a) Pin diagram

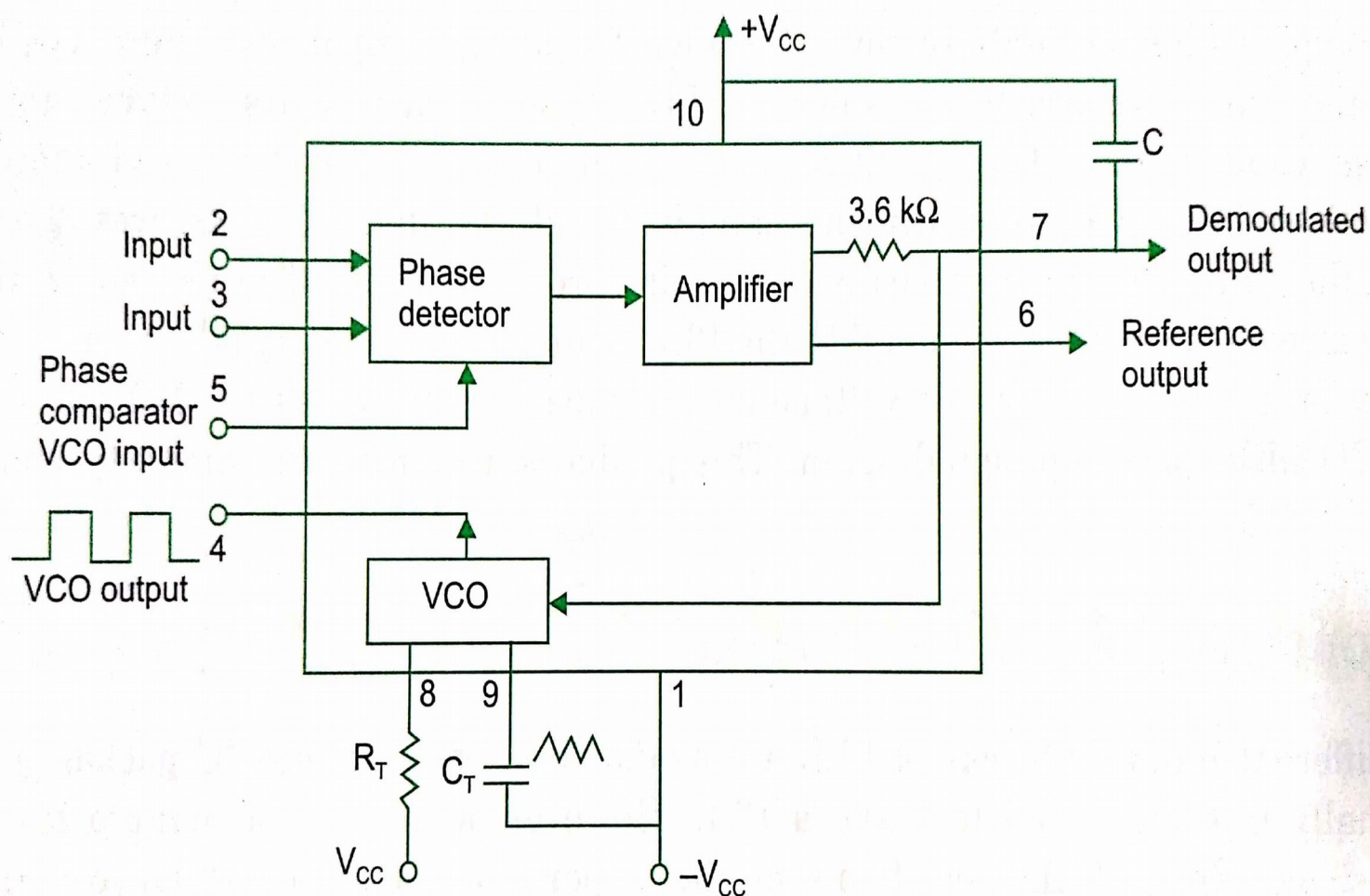
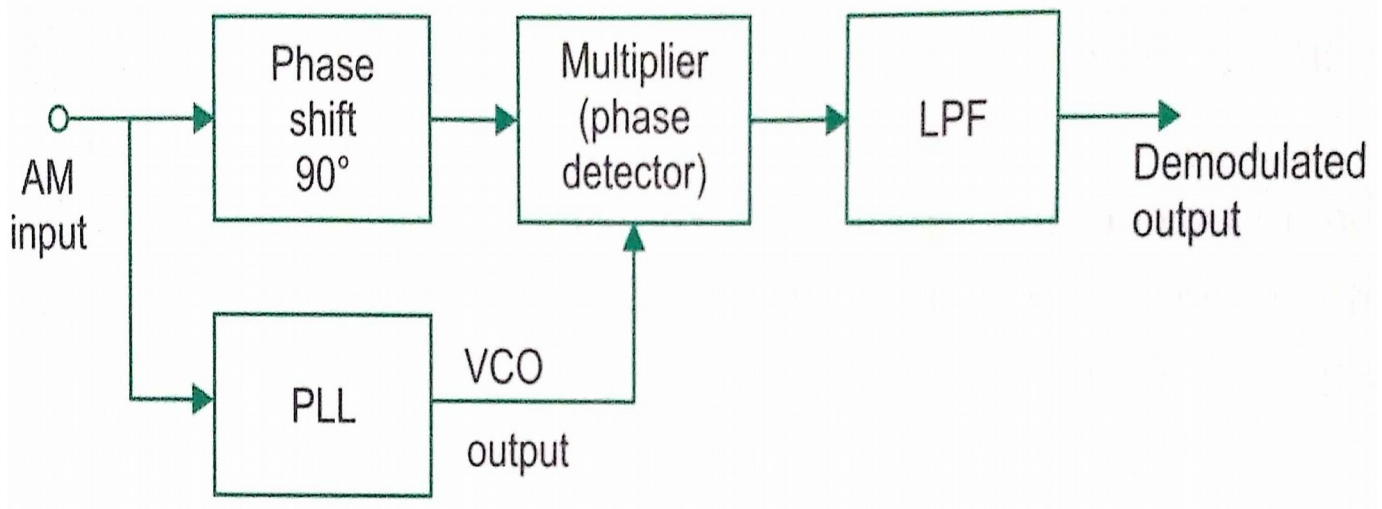


Fig. 9.9 (b) NE/SE565 PLL block diagram

The important electrical parameters of 565 PLL are:

Operating frequency range	: 0.001 Hz to 500 kHz
Operating voltage range	: ± 6 V to ± 12 V
Input level	: 10 mV rms min. to 3 V pp max
Input impedance	: 10 k Ω typical
Output sink current	: 1 mA typical
Drift in VCO centre frequency with temperature	: 300 ppm/ $^{\circ}$ C. (parts per million per degree centigrade)
Drift in VCO centre frequency with supply voltage	: 1.5 per cent/V max
Triangle wave amplitude	: $2.4 V_{pp}$ at ± 6 V supply voltage
Square wave amplitude	: $5.4 V_{pp}$ at ± 6 V supply voltage
Bandwidth adjustment range	: $< \pm 1$ to $\pm 60\%$

PLL: Application-AM Detector



The PLL may be used to demodulate AM signal as shown in fig. The PLL is locked to the Carrier frequency of the incoming AM signal. $F_o = \text{Carrier Frequency}$ (VCO output).

Since the un-modulated AM is fed to the Multiplier through 90° phase shift network as VCO output (F_o) is always 90° phase shifted with incoming AM signal under the locked condition. This makes both the signal applied to the multiplier in same phase.

The output of the multiplier contains both sum ($AM + F_o$) and difference ($AM - F_o$) signals, the demodulated output is obtained after filtering high frequency signal by LPF. Therefore,

Demodulated output = $A_M - F_o$

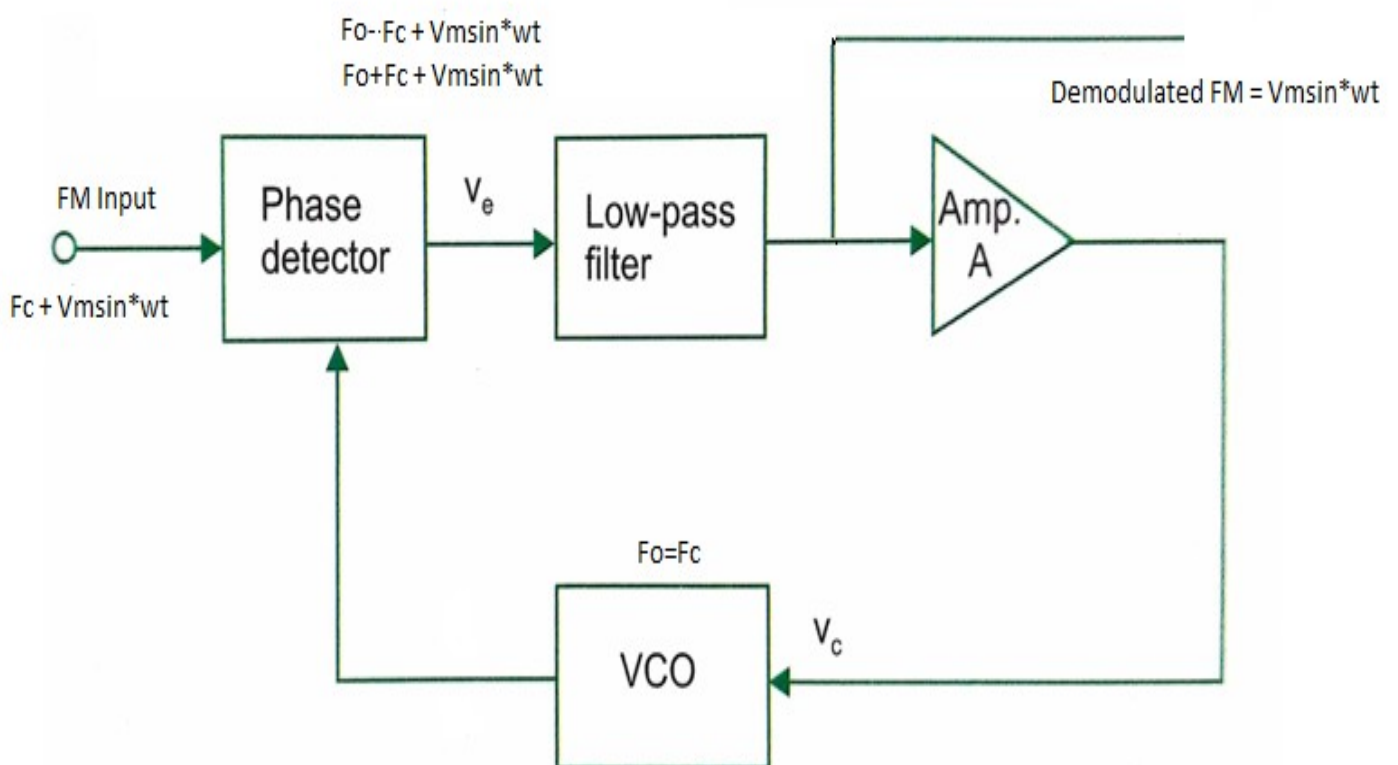
$$A_M = F_s + F_c$$

VCO locked to F_c therefore $F_o = F_c$

Therefore

$$\text{Demodulated output} = F_s + F_c - F_o = F_s$$

PLL: Application-FM Detector



The Un-modulated FM signal ($F_c + V_m \sin \omega t$) and VCO frequency (F_o) which is locked to the carrier frequency (F_c) of the Un-modulated FM signal is given to the Phase detector of PLL. The output of the Phase detector contains both sum ($F_o + F_c + V_m \sin \omega t$) and difference ($F_o - F_c + V_m \sin \omega t$) signals, the demodulated output is

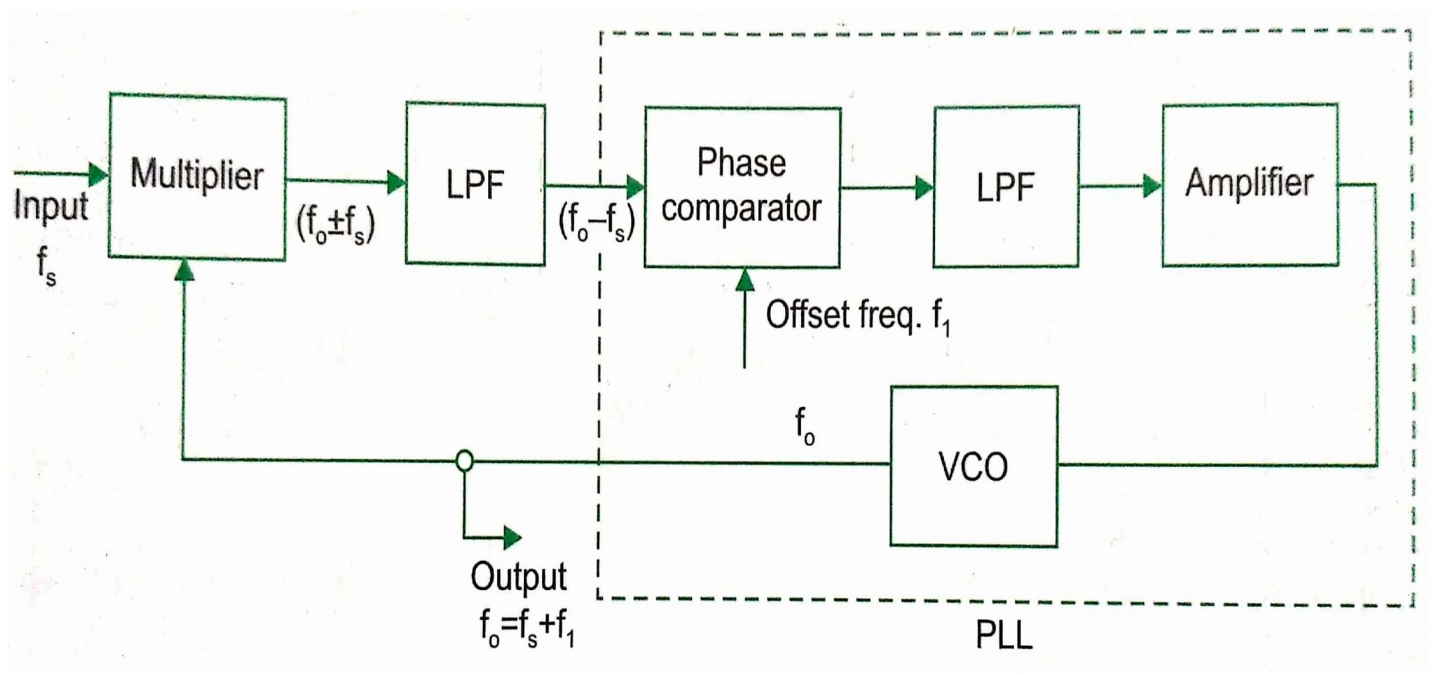
obtained after filtering high frequency signal by LPF. Therefore,

Demodulated output = $F_o - F_c + V_m \sin \omega t$ and VCO locked to F_c , therefore, $F_o = F_c$

Hence

Demodulated FM output = $V_m \sin \omega t$

PLL: Application-Frequency translator



The Schematic for shifting the frequency of an oscillator by a small factor is shown in the figure. It can be seen that the Mixer (multiplier) and a LPF1 is connected externally to the PLL. The signal F_s which has to be shifted and output frequency F_o of VCO are applied as inputs to the

mixer. The output of the mixer contains sum ($F_o + F_s$) and difference ($F_o - F_s$). However, the LPF passes only difference ($F_o - F_s$). The translation of Offset frequency F_1 (where, $F_1 \ll F_s$) is applied to the phase comparator of the PLL. When PLL is in Locked State,

Output of Phase Comparator Sum ($F_o - F_s + F_1$)
and Difference ($F_o - F_s - F_1$)

LPF2 passes difference component ($F_o - F_s - F_1$)

Therefore, $F_o - F_s = F_1$ (Locked)

$$F_o = F_s + F_1$$

Thus it is possible to shift incoming frequency F_s
by small factor F_1

ASSIGNMENT QUESTIONS

1. WHAT IS THE PURPOSE OF PHASE DETECTOR?
2. SKETCH AND LABEL A PLL-BASED FREQUENCY SYNTHESIZER?
3. WHAT IS THE OUTPUT OF A PLL WHEN NO INPUT SIGNAL IS PRESENT?
4. EXPLAIN THE PIN DIAGRAM OF IC566?
5. IF THE INPUT FREQUENCY AND THE VCO OUTPUT FREQUENCY ARE SUFFICIENTLY CLOSE TO EACH OTHER, WHAT WILL THE PLL DO?