

UNIT-06

Analog vs Discrete time signals, sample and hold circuits, ADC architecture (Flash ADC, Successive Approximation ADC, Dual slope ADC), DACs (Binary weighted resistors, R-2R DAC), INL & DNL

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The difference between analog vs discrete time signals

Analog signal	Digital signal
Analog signals are continuous signals.	Digital signals are not continuous, they are discrete signals.
We can represent analog signals in the form of sine waves.	We can represent digital signals in the form of square waves.
The values of voltage will be in a continuous range	The values of voltage will be discontinuous.
Records the information as it is.	Converts the information into binary form.
These signals are used in analog devices.	Digital electronic devices like computers, smartphones, smartwatches, etc. use these signals
Examples: Any natural sound, human voice, data read by analog devices.	Electronic signals, computer signals, data read by digital devices.

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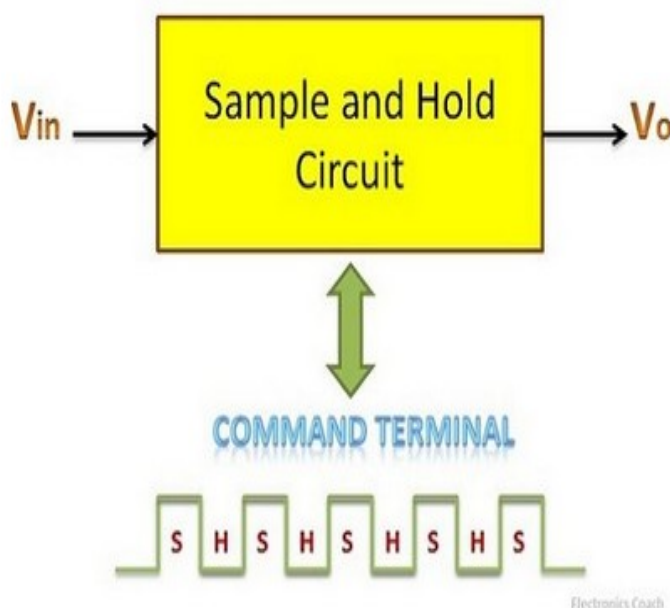
SAMPLE AND HOLD CIRCUITS:

Definition: *The Sample and Hold circuit is an electronic circuit which creates the samples of*

voltage given to it as input, and after that, it holds these samples for the definite time. The time during which sample and hold circuit generates the sample of the input signal is called sampling time. Similarly, the time duration of the circuit during which it holds the sampled value is called holding time.

Sampling time is generally between **1 μ s to 14 μ s** while the holding time can assume any value as required in the application.

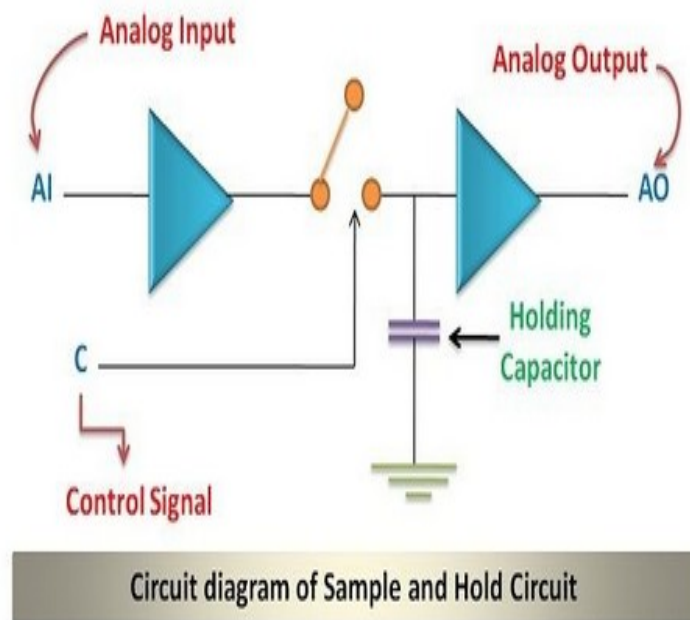
It will not be wrong to say that capacitor is the heart of sample and hold circuit. This is because the capacitor present in it charges to its peak value when the switch is opened, i.e. during sampling and holds the sampled voltage when the switch is closed.



Circuit Diagram of Sample and Hold Circuit

The diagram below shows the circuit of the sample and hold circuit with the help of an Operational Amplifier. It is

evident from the circuit diagram that two OP-AMPS are connected via a switch. When the switch is closed sampling process will come into the picture and when the switch is opened holding effect will be there.

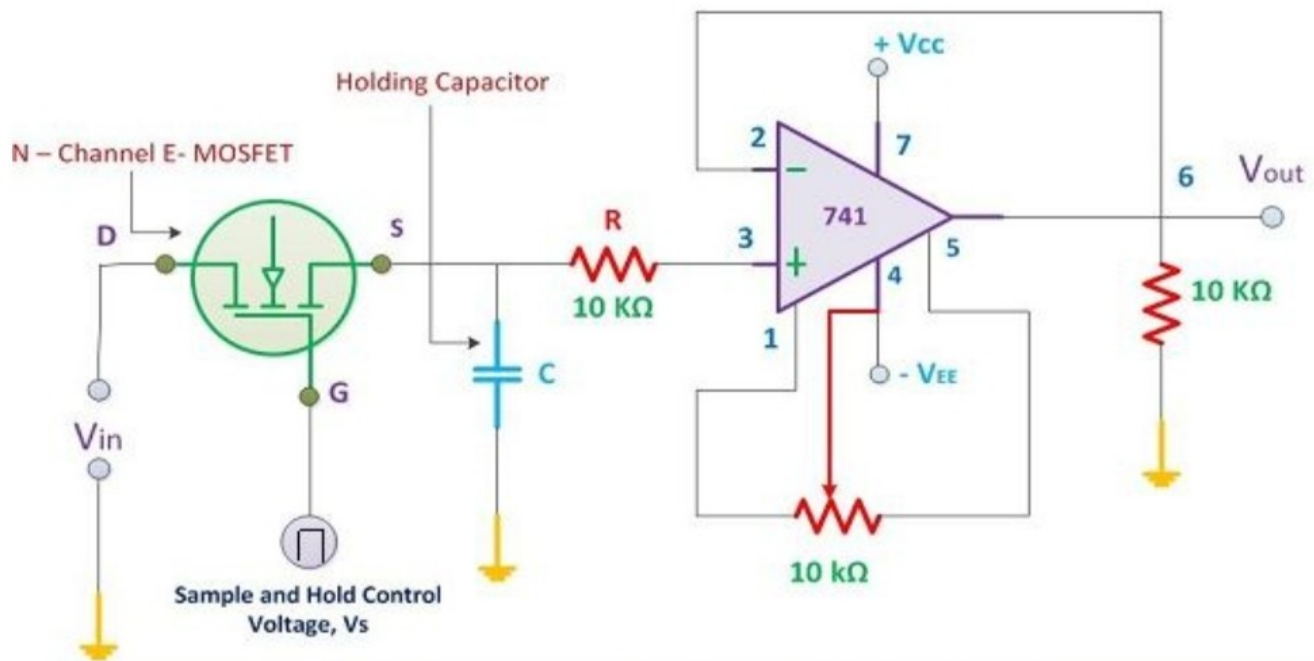


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The capacitor connected to the second operational amplifier is nothing but a holding capacitor.

Working of Sample and Hold Circuit

The working of sample and hold circuit can be easily understood with the help of working of its components. The main components which a sample and hold circuit involves is an **N-channel Enhancement type MOSFET**, a **capacitor** to store and hold the electric charge and a high precision **operational amplifier**.



Practical Circuit of Sample and Hold Circuit

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Input and Output Waveforms

The waveforms as described in the diagram clearly depicts the picture. It is evident from the waveform of the sample and hold circuit, that during the ON duration what will be the voltage at the output. During the OFF duration the voltage that exists at the output of OP-AMP.

Performance Parameters

- **Acquisition Time (T_{AC}):** The time required by the capacitor to get the charge of the input voltage applied to the sample and hold circuit. It is referred as acquisition time

Aperture Time (T_{AP}): *The aperture time can be defined as the time required by the capacitor to change its state from sampling to holding. Due to the propagation delay of switches, even after the hold command is given the capacitor still keeps on charging for the short duration of time. This is nothing but aperture time.*

1. **Voltage Droop:** The voltage droop is the voltage drop down in the capacitor due to leakage of charge by a capacitor. Ideally, we require capacitors which do not possess any leakage, but it is not possible practically. No matter how good quality material we use there will be some voltage drop.
2. **Hold Mode Settling Time:** After the generation of hold commands, the analogue input voltage which is used by the capacitor for charging takes some time to settle completely. This is called Hold Mode settling time.

Application of Sample and Hold Circuit

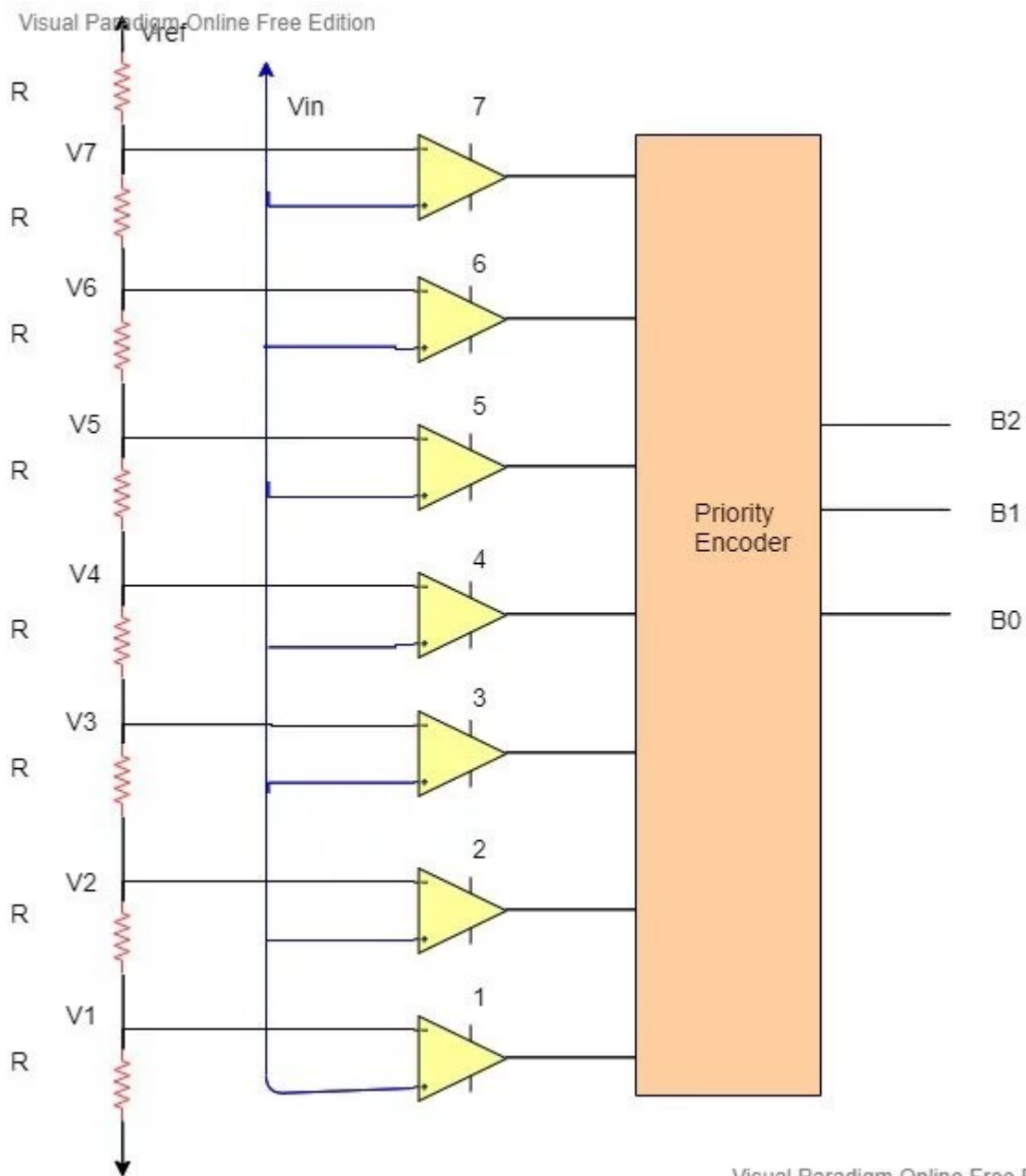
1. Data Distribution System
2. Sampling Oscilloscopes
3. Data Conversion System
4. Digital Voltmeters
5. Analog Signal Processing
6. Signal Constructional Filters

This completes the detailed description of the sample and hold circuit. Thus, in simple terms sample and hold circuit generates the samples of the analogue input signal and holds the latest sampled values for definite time and reflects it at the output.

3-bit Flash Analog to Digital Converter with Example Circuit

*we will discuss the workings of a flash ADC. A flash ADC, or flash analog-to-digital converter, is the fastest type of [ADC](#) among all the other ADCs. It is also known as a parallel analog-to-digital converter. It comprises high-speed comparators, resistive voltage divider circuits, and a priority encoder. The tutorial is a complete guide that includes its workings, advantages, disadvantages, and applications in the market.***Flash ADC Introduction**

An N-bit flash ADC consists of two powered N-1 comparators, two powered N numbers of matched resistors, and a priority encoder. The block diagram for the concept is provided below:



Main Components of Flash ADC

Before understanding the workings of the flash ADC, we should have knowledge of its components. A list of all the components of a flash ADC is provided below.

- Resistor voltage divider circuit
- Comparator
- Priority encoder

Resistor Voltage Divider Circuit

The resistive voltage divider is a simple circuit network of resistors that scales down an input voltage connected to it. It happens because of the distribution of the input voltage among all the

resistors. This circuit is useful for producing a reference voltage or stepping down the magnitude of a high voltage. We can derive the general formula for the circuit using Kirchhoff's laws.

If two resistors are connected in series, then the formula is as follows:

$$V_{out} = R_2 \times V_{in} / R_1 + R_2$$

Reference Voltage Formula

Let us suppose that V_1 is applied to the first comparator, and then this V_1 can be calculated as:

$$V_1 = R \times V_{ref} / R + 7R$$

$$V_1 = V_{ref} / 8$$

Now consider V_2 as the reference voltage for comparator number 2. So we can calculate the V_2 as:

$$V_2 = (R + R) \times V_{ref} / 8R$$

$$V_2 = 2 \times V_{ref} / 8$$

Reference Voltage	Calculation
V_3	$3 \times V_{ref} / 8$
V_4	$4 \times V_{ref} / 8$
V_5	$5 \times V_{ref} / 8$
V_6	$6 \times V_{ref} / 8$
V_7	$7 \times V_{ref} / 8$

Reference Voltage Calculation

To completely comprehend the working of the flash ADC, we take an example reference and input voltage, i.e., $V_{ref} = 8 \text{ V}$ and $V_{in} = 3.3 \text{ V}$, respectively.

Using the formula for specific measurements, we can calculate V_1 as follows:

$$V_1 = R \times 8 \text{ V} / R + 7R$$

$$V_1 = 8 \text{ V} / 8$$

$$V_1 = 1 \text{ V}$$

Hence, we can calculate all the reference voltages using the voltage divider formula provided in the table above.

$$V_2 = 2 \text{ V}$$

$$V_3 = 3 \text{ V}$$

$$V_4 = 4 \text{ V}$$

$$V_5 = 5 \text{ V}$$

$$V_6 = 6 \text{ V}$$

$$V_7 = 7 \text{ V}$$

Flash ADC Working

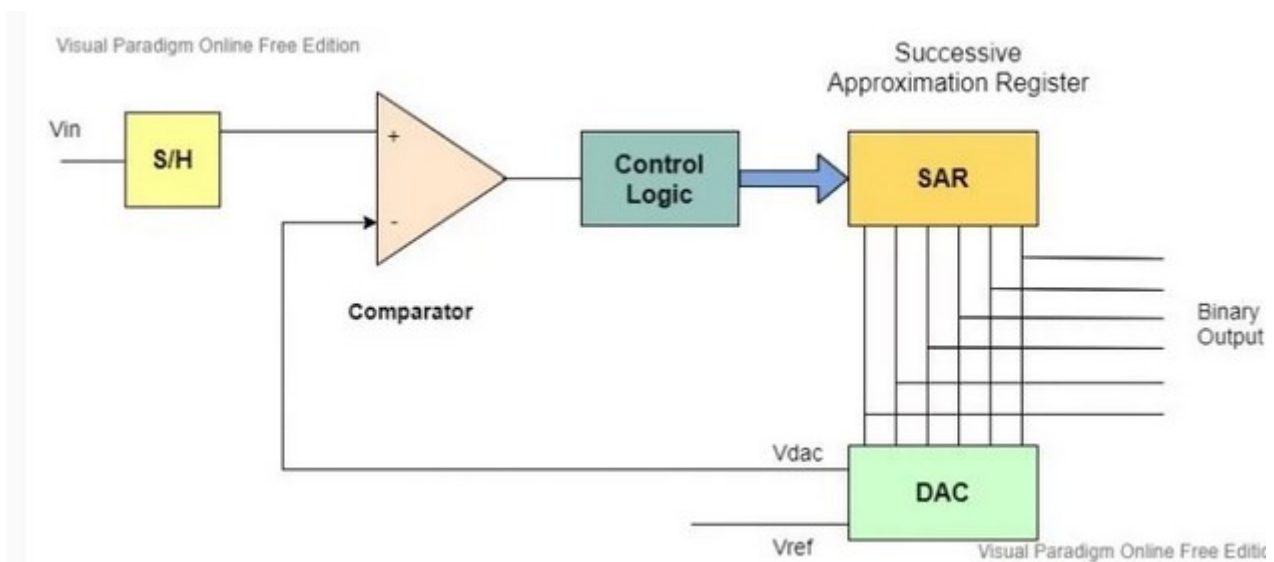
The analog input voltage is compared with all the comparator's reference voltages of the Flash analog to digital converter. After comparison, we notice that the reference voltages of the first three comparators, i.e., 1 V, 2 V, and 3 V, are less than the 3.3 V input. That is why the output of the first three comparators is high while the remaining comparators are in a low state.

The outputs of these comparators become the inputs of the priority encoder. We can see that there are seven reference voltages. Hence, the 8th input line is connected to logic 1 and is given the least priority. It means that it is a descending-order priority encoder. This helps in the case where all the comparator's output voltages are zero. Hence, importance will be given to the higher-priority outputs, so the encoder generates an all-zero output.

As three input lines of the encoder are high at the same time, priority will be given to the third input, and a corresponding output binary code is generated.

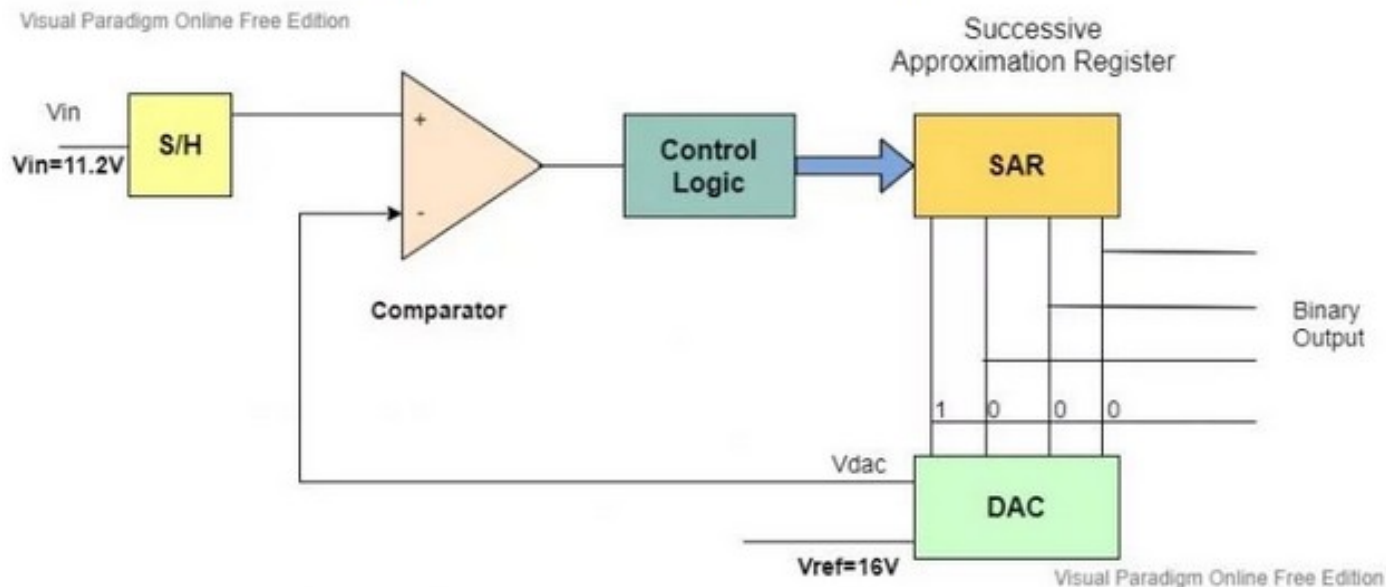
Successive Approximation ADC Introduction:

This ADC technique most frequently includes general applications. The ADC comprises a comparator, a digital-to-analog converter, a register, and a control circuit. The schematic is shown below:



At the point when the new conversion begins, the sample and hold circuit samples the input voltage. and then this sampled signal is compared with the output signal of the digital-to-analog converter

4-bit Successive Approximation ADC Example

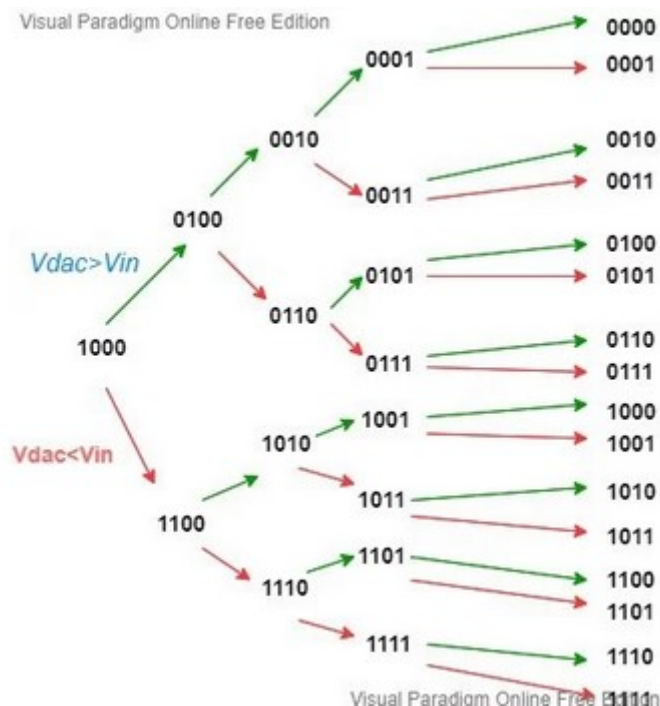


$$V_{out} = -V_{ref} \{ B_0 (1/16) + B_1 (1/8) + B_2 (1/4) + B_3 (1/2) \}$$

$$V_{out} = 8 \text{ Volts}$$

working of Successive Approximation ADC

As per our calculations, the output voltage of DAC is 8 volts, and V_{in} is 11.2 volts. So, this satisfies the condition $V_{in} > V_{dac}$, which results in no change in the most significant bit, and successive bits are set to 1.



Now, the code has become 1100. So, the output of the DAC corresponding to this

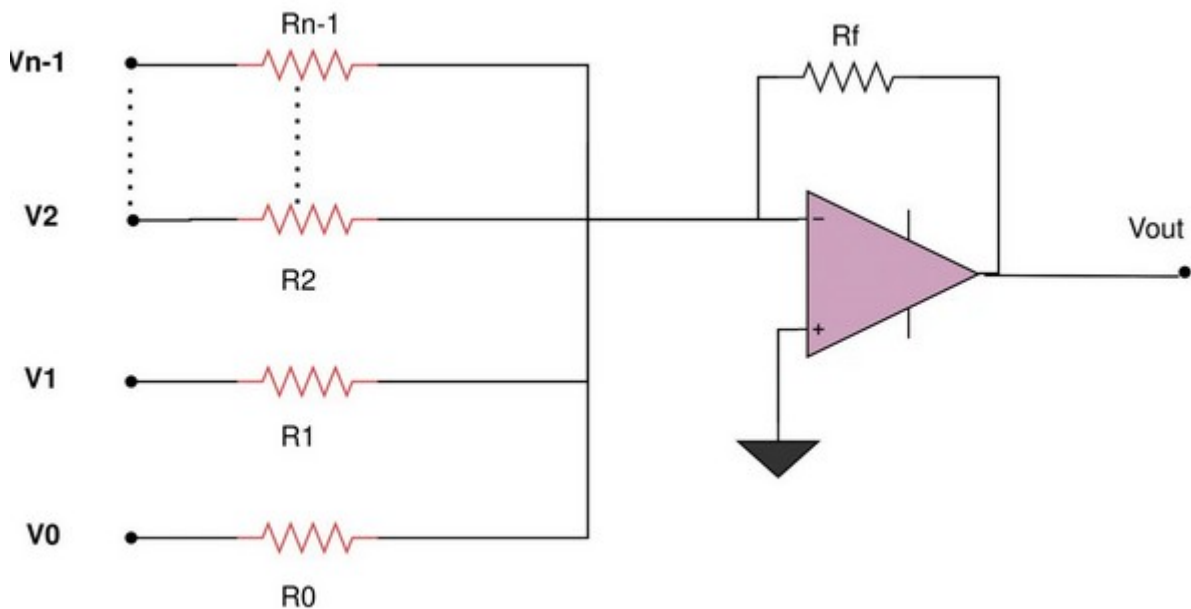
binary code is 12 volts; we measure it using the same output voltage formula. This is the new DAC voltage to be compared with.

What is a DAC?

A DAC is an electronic circuit that takes in digital data as input and transforms it into an analog output signal. It is actually the output voltage proportional to the binary code given at the DAC input and then used to drive various circuits. They have vast applications, but let us take a simple example of an audio system to showcase their importance.

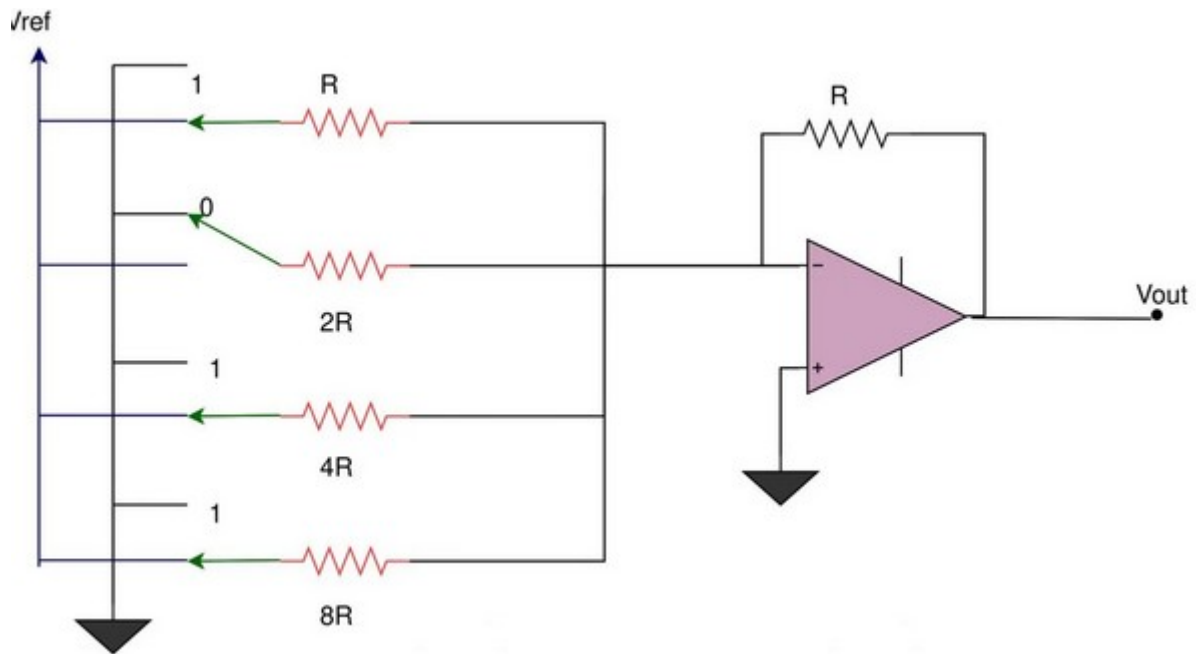
Binary Weighted Resistor DAC Working

The configuration uses a summing amplifier whose output voltage is proportional to the sum of the voltages applied at the input.



$$V_{out} = - \{ (R_f / R_0) V_0 + (R_f / R_1) V_1 + (R_f / R_2) V_2 + \dots + (R_f / R_{n-1}) V_{n-1} \}$$

Circuit Diagram:



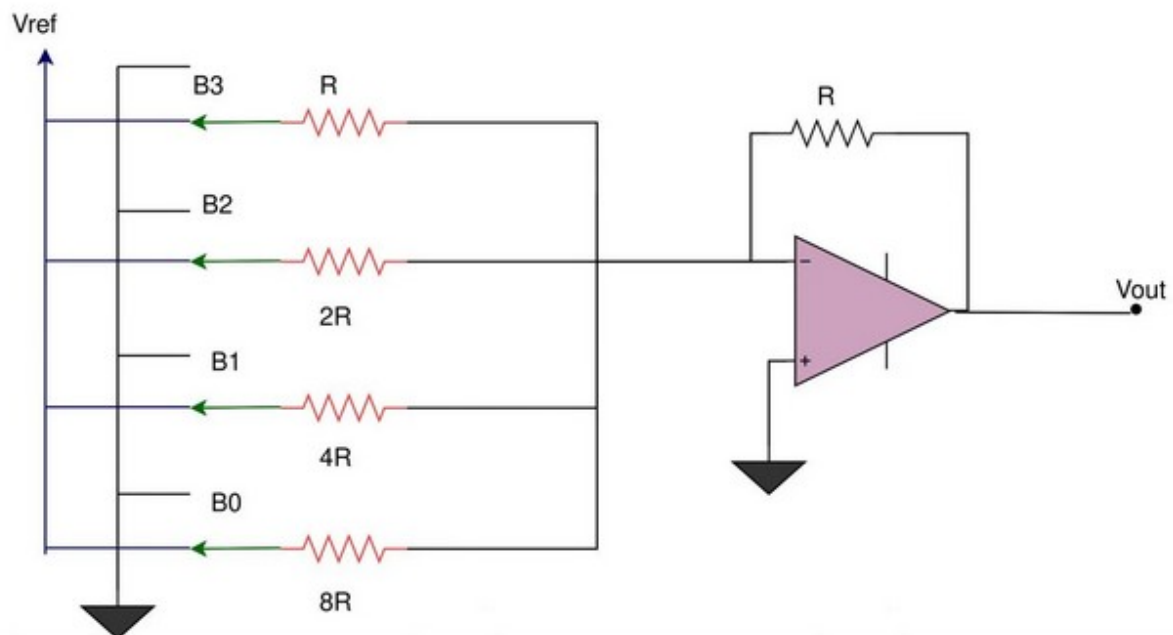
If resistors with precise values connect with each of the input voltages to scale the gain, it starts working as a DAC. All the input voltages connect to the same reference voltage, so the formula becomes:

$$V_{out} = - \{ (R_f / R_0) V_{ref} + (R_f / R_1) V_{ref} + (R_f / R_2) V_{ref} + \dots + (R_f / R_{n-1}) V_{ref} \}$$

$$V_{out} = - V_{ref} \{ (R_f / R_0) + (R_f / R_1) + (R_f / R_2) + \dots + (R_f / R_{n-1}) \}$$

Binary Weighted Resistor DAC Example

Let us take the example of a 4-bit binary code. Assuming $V_{ref} = 5\text{ V}$ and code = 1011, the weighted output voltage is:



4-bit binary weighted resistor DAC circuit

Binary Inputs		Vout		
B3	B2	B1	B0	Volts
0	0	0	0	-0
0	0	0	1	-0.625
0	0	1	0	-1.25
0	0	1	1	-1.875
0	1	0	0	-2.50
0	1	0	1	-3.125
0	1	1	0	-3.75
0	1	1	1	-4.375
1	0	0	0	-5.00
1	0	0	1	-5.625
1	0	1	0	-6.25
1	0	1	1	-6.875
1	1	0	0	-7.50
1	1	0	1	-8.125
1	1	1	0	-8.750
1	1	1	1	-9.375

Drawbacks

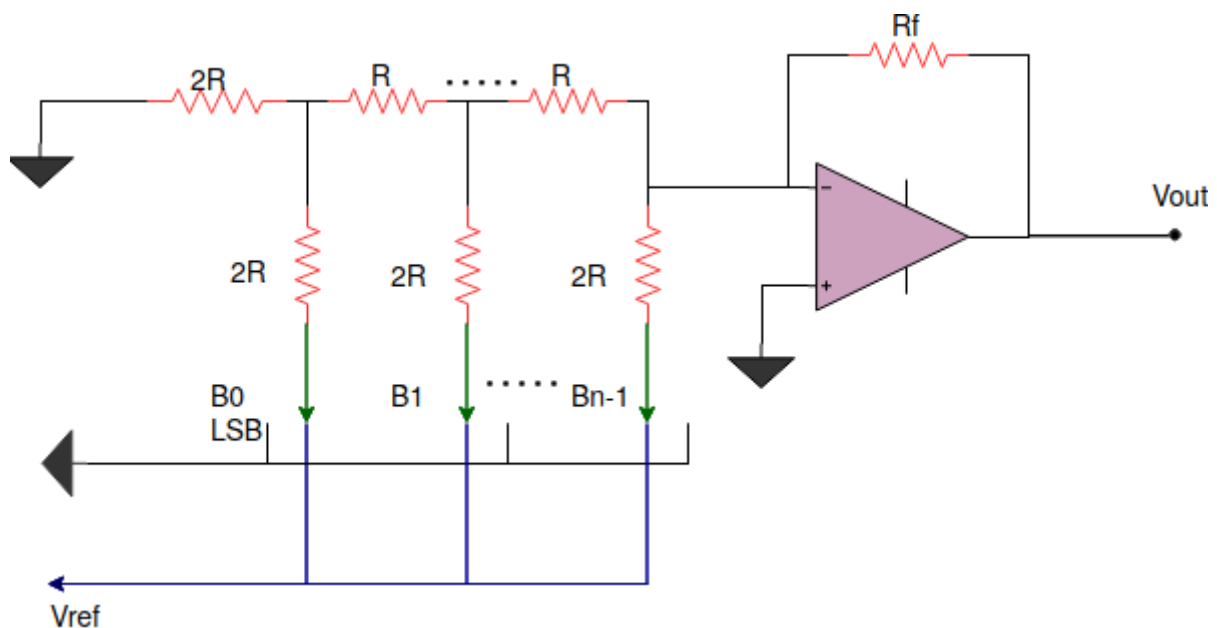
- The binary weighted DAC has quite a large gap between LSB and MSB resistors values and requires a very precise value of resistors.
- Hence, it becomes impractical for higher-order DACs and is suitable for lower-resolution DACs.
- The stability of the device is resistor-dependent. It is difficult to maintain an accurate resistance ratio with temperature variations.

Advantages

- It has a simple assembly.
- It has a fast conversion speed.
- Simple conversion circuit

R-2R Ladder DAC:

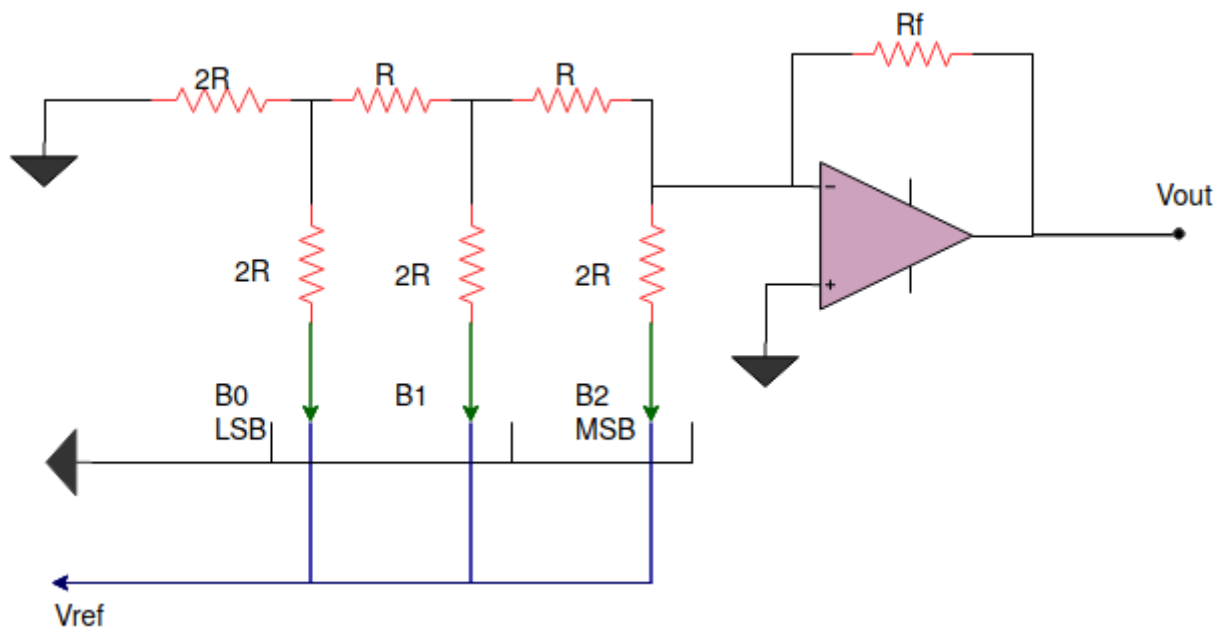
The R-2R configuration is a simple arrangement that consists of parallel and series resistors connected in cascaded form to an operational amplifier. We can use an operational amplifier in inverting or non-inverting form, depending on the polarity of the output voltage that we want to get from the DAC. R-2R ladder resistors act as voltage dividers along with the entire network, with the output voltage dependent on the input voltages.



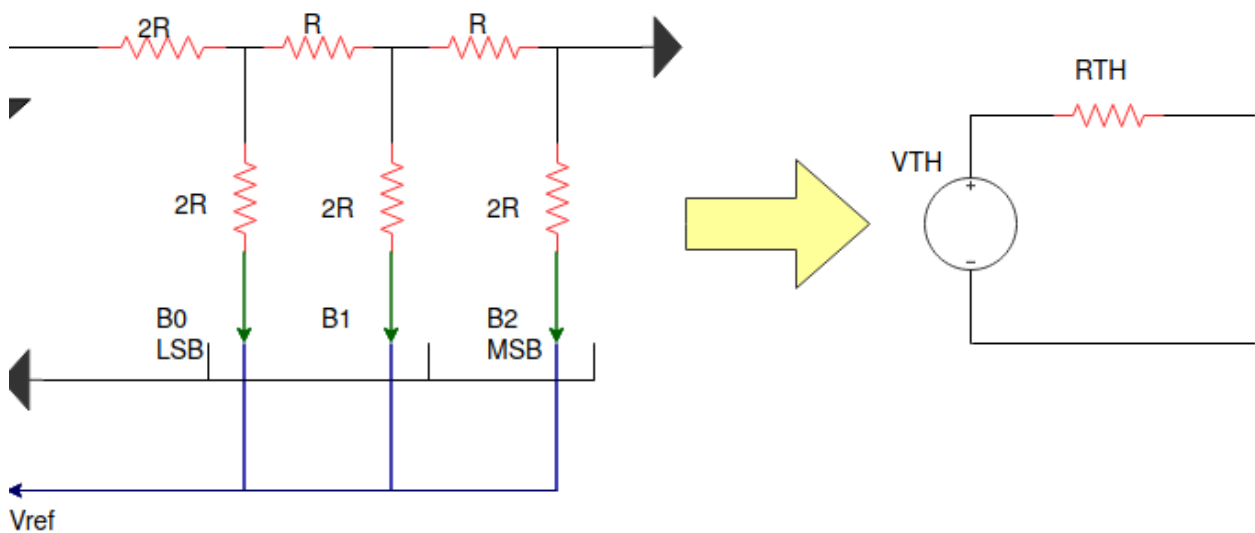
R-2R Ladder DAC Components

The ladder arrangement consists of two resistors, i.e., a base resistor R and a $2R$ resistor, which is twice the value of the base resistor. This feature helps to maintain a precise output analog signal without using a wide range of resistor values.

3-bit R-2R Ladder DAC Circuit Diagram



Working of Thevenin Theorem



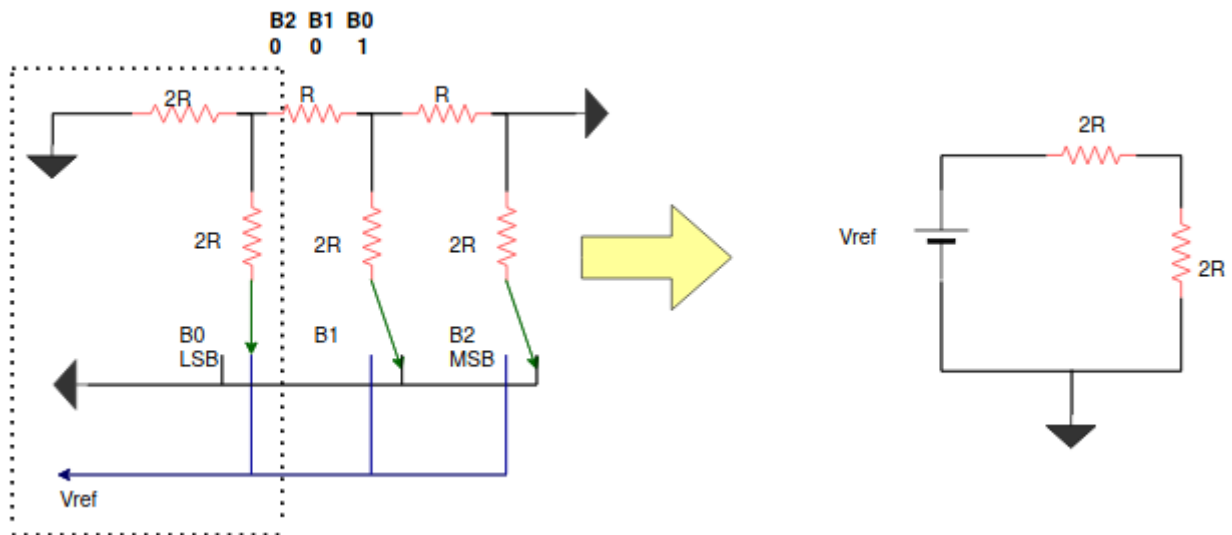
$$V_{Th} = 2R \times V_{ref} / 2R + 2R$$

$$V_{Th} = V_{ref} / 2$$

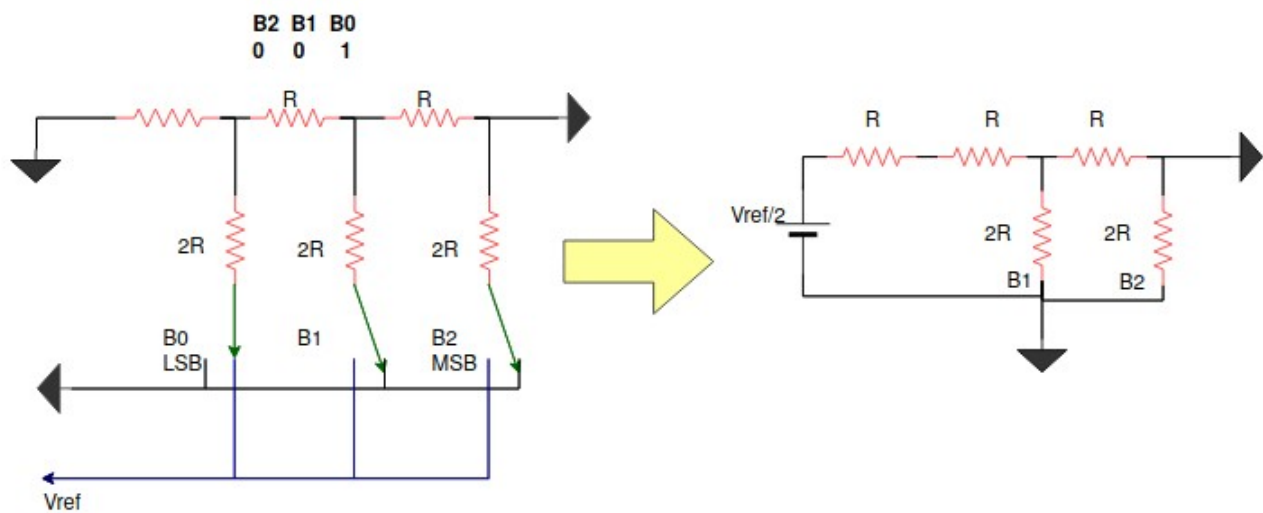
For measuring the Thevenin resistance, short circuit the reference voltage. Two resistances, 2R and 2R, become parallel to each other. So,

$$R_{Th} = 2R \parallel 2R$$

$$R_{Th} = R$$



First Equivalent Circuit



$$V_{Th} = (2R \times V_{ref}/2) / 2R + 2R$$

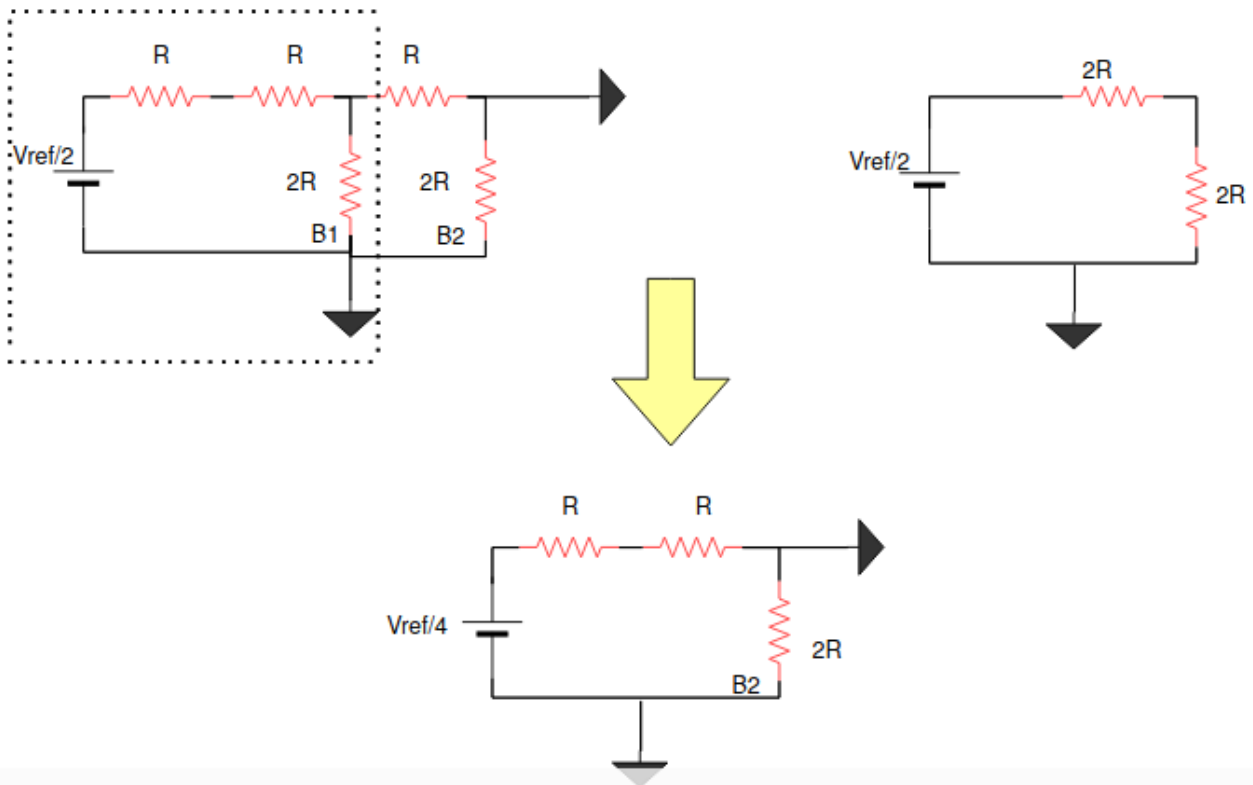
$$V_{Th} = V_{ref} / 4$$

$$R_{Th} = 2R \parallel 2R$$

$$R_{Th} = R$$

Second Equivalent Circuit:

B2 B1 B0
0 0 1

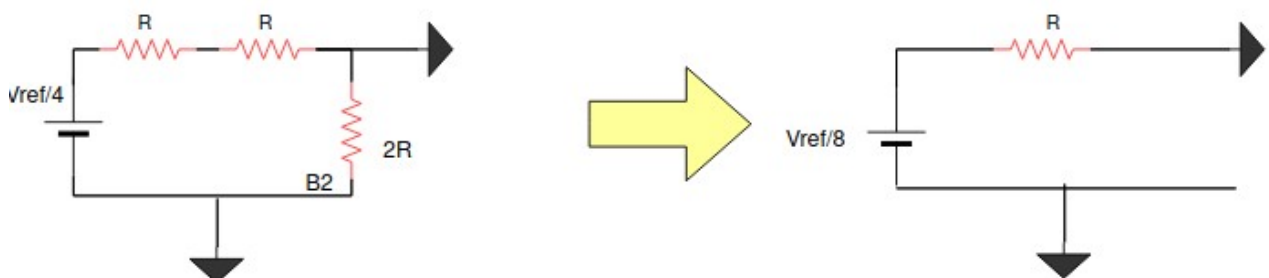


$$V_{Th} = (2R \times V_{ref}/4) / 2R + 2R$$

$$V_{Th} = V_{ref} / 8$$

$$R_{Th} = (R + R) \parallel 2R$$

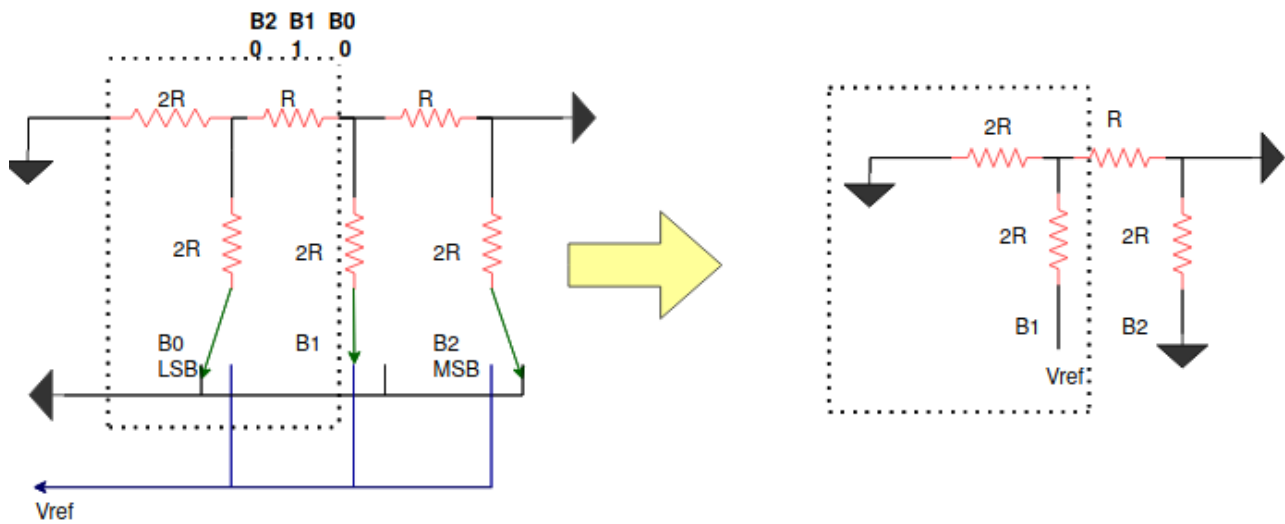
$$R_{Th} = R$$



When only bit B1 is high

The binary code is 010. It will be solved in a similar fashion. The first stage minimizes the dotted block. The combination of two $2R$ resistors is in series with R . The resultant resistance is

$$(2R \parallel 2R) + R = 2R$$



After transforming, the Thevenin equivalents are measured. V_{Th} and R_{Th} turn out to be

$$V_{Th} = (2R \times V_{ref}) / 2R + 2R$$

$$V_{Th} = V_{ref} / 2$$

$$R_{Th} = (R + R) \parallel 2R$$

$$R_{Th} = R$$

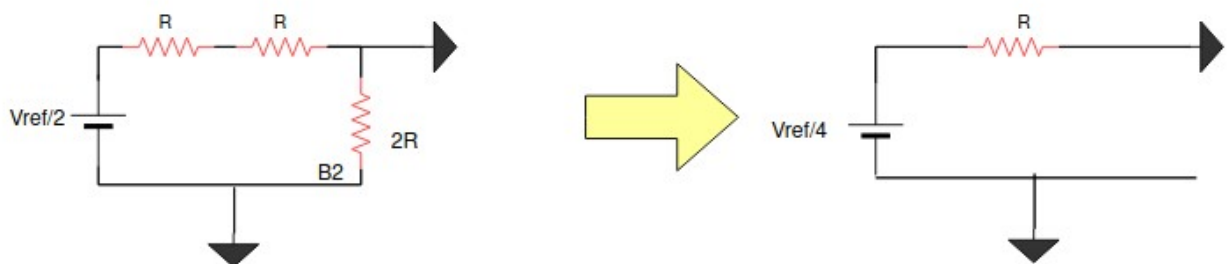
$$R_{Th} = (R + R) \parallel 2R$$

$$R_{Th} = R$$

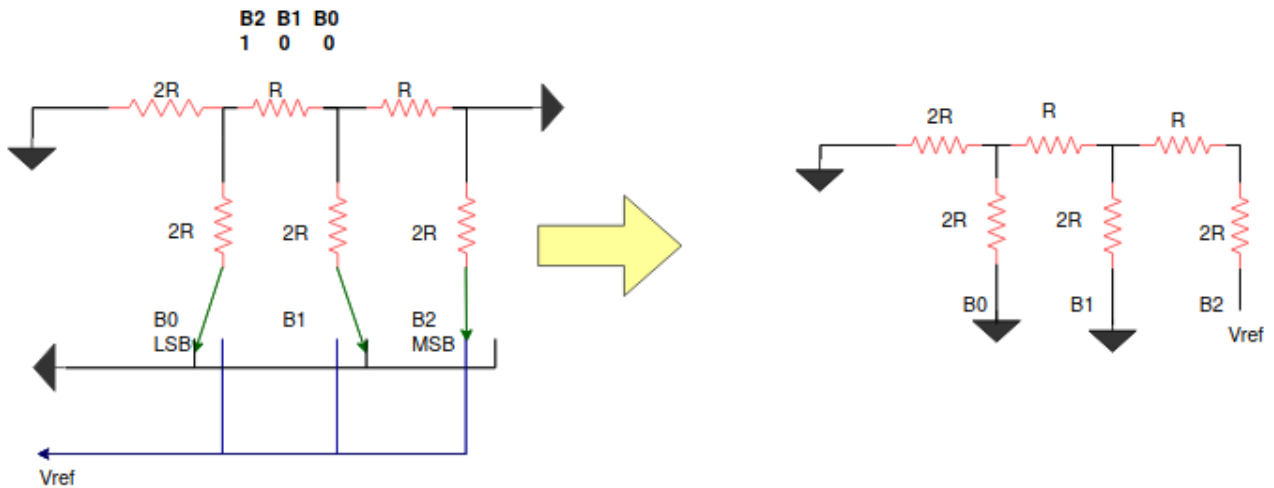
And V_{Th} ,

$$V_{Th} = (2R \times V_{ref}/2) / 2R + 2R$$

$$V_{Th} = V_{ref} / 4$$



When MSB Bit is high

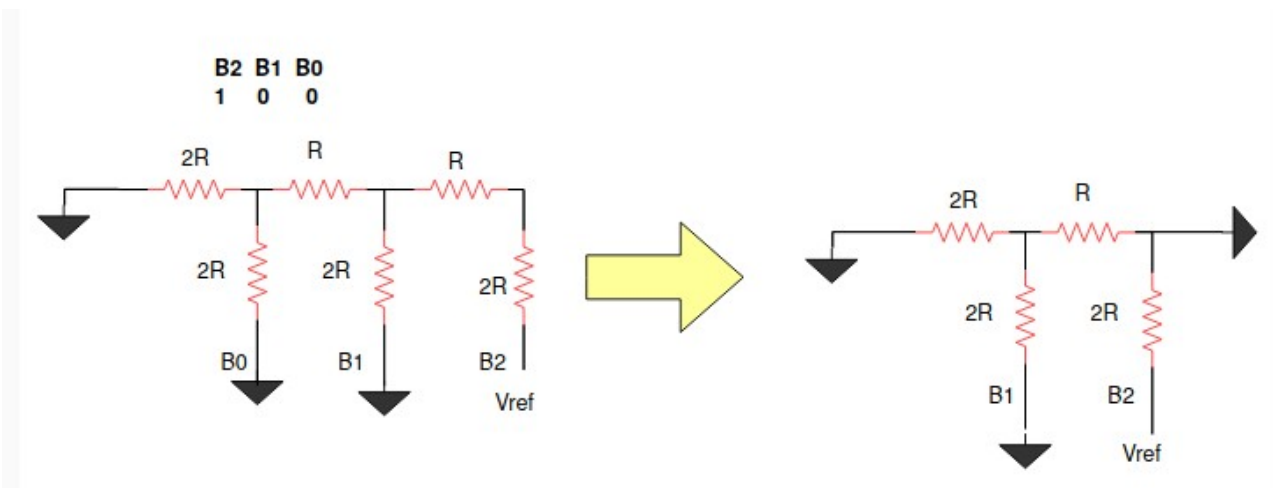


Starting from the left side of the circuit, the first three resistors, i.e., 2R, 2R, and R, result in the equivalent resistance 2R

$$(2R \parallel 2R) + R = 2R$$

So, now the circuit is reduced to the figure on the right.

$$(2R \parallel 2R) + R = 2R$$



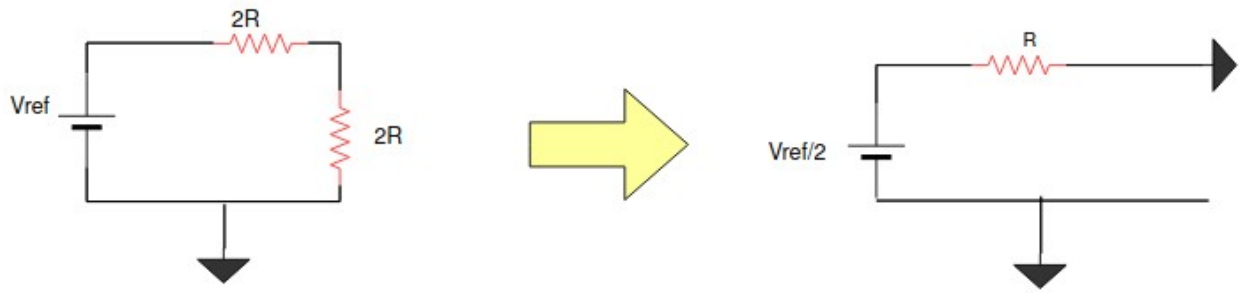
The right figure minimizes and becomes the left figure shown below. Now, measure the Thevenin V_{Th} and R_{Th} , and the final Thevenin voltage is $V_{ref}/2$.

$$V_{Th} = (2R \times V_{ref}) / (2R + 2R)$$

$$V_{Th} = V_{ref} / 2$$

$$R_{Th} = (R + R) \parallel 2R$$

$$R_{Th} = R$$



$V_{ref}/2$ is the output voltage of the R-2R Ladder network when MSB is high and the remaining bits are 0.

When all three bits are high

When all 3 bits connects to the reference voltage, the output voltage will be the sum or superposition of all three voltages.

$$V_{r-2r} = (V_{ref} / 2) + (V_{ref} / 4) + (V_{ref} / 8)$$

$$V_{r-2r} = 7V_{ref} / 8$$

Binary Inputs		Vout, Rf=4ohms, R=2ohms	
B2	B1	B0	Volts
0	0	0	-0
0	0	1	-1.25
0	1	0	-2.5
0	1	1	-3.75
1	0	0	-5.0
1	0	1	-6.25
1	1	0	-7.5
1	1	1	-8.75

Advantages

- It can be fabricated easily.
- The configuration requires only two resistors, with one being twice the other in value, instead of a wide range of resistors.
- The output resistance remains the same despite the number of bits.
- Increasing the resolution does not degrade the performance.

Disadvantages

- It has a slow conversion speed.

ASSIGNMENTS::::

- 1.what is the difference between Analog and discrete time signals?
- 2.Explain about sample and hold circuits?
- 3.Write the operation of FLASH ADC?
- 4.What is DAC?And explain binary weighted DAC and write the operations?
- 5.Draw the circuits and write the operation of R-2R ladder DAC?